A WIDE-SUPPLY RANGE HIGH-PSR BANDGAP VOLTAGE REFERENCE

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ABSTRACT

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Most precision references employ a PN junction diode voltage, since it is very predictable meaning that it does not vary significantly with process and its behavior over a given temperature range is well characterized. First-order and second-order references that base their operation on use of forward-biased diode voltage are named as *bandgap references* because the compensated reference output voltage is equal to or some fraction of the bandgap voltage of the material used in the process. However, since low-power consumption and low-supply levels are the main objectives of today's IC market, classical bandgap references leave much to be desired. This thesis targets a sub-1 V bandgap voltage reference circuit that can operate in (a) a wide supply voltage range (1 - 5.5) V, (b) a wide temperature range (-40 – 125) °C, and still can maintain a high PSR performance while consuming a total current of only 5 µA resulting in low power consumption. The proposed circuit is designed for AMS 0.35µ C35B4C3 process.

ÖZET

GENİŞ BESLEME ARALIKLI YÜKSEK PSR PERFORMANSLI BANT ARALIĞI GERİLİM KAYNAĞI

Günümüzde birçok hassas voltaj referans devresi yapısını düz kutuplanmış bir PN jonksiyonlu diyot gerilimi üzerine kurar. Bunun sebebi diyot geriliminin sıcaklıkla değişiminin iyi karakterize edilmiş olması ve proses değişimlerinde saçılımının fazla olmamasıdır. Düz kutuplanmış ve sıcaklık kompanzasyonu birinci ve ikinci dereceden sağlanmış olan gerilim devrelerinin genel adı *bant-aralığı* gerilim devreleridir. Bu ismi alma nedenleri ise sıcaklık kompanzasyonu gerçeklenmiş devrenin çıkış voltajının devrenin gerçeklendiği materyalin bant-aralığı geriliminin kendisi ya da bir katı olmasıdır. Öte yandan günümüz tüm devre pazarında trend teknolojinin de ilerlemesiyle bu devrelerin düşük gerilim ve düşük güç tüketmesidir. Bu gerçek göz önünde tutularak sunulan tez çalışmasi (a) minimum kaynak gerilimi 1 V olan ve (1-5.5) V gibi geniş bir kaynak gerilim aralığında çalışabilen, (b) (– 40-125) °C gibi geniş sıcaklık aralığında kompanzasyonu sağlanmış, ve bu şartlar altında bile kaynaktaki değişimleri iyi reddedebilen 1 V`un altında çıkış veren bir bant-aralığı devresinin tasarımını hedeflemektedir. Devre tarafından tüketilen toplam akım 5 µA ve düşük güç tüketimini garantilemektedir. Devrenin dizaynı için kullanılan teknoloji ise AMS 0.35µ C35B4C3 prosesidir.

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1. INTRODUCTION

1.1. Objectives

Voltage references are one of the most important building blocks of many electrical systems. The output of a voltage reference can simply be a naturally existing voltage which does not vary significantly depending on the operating conditions. Such voltage references are named as zero order references since one does not need to improve its accuracy. On the other hand, precision voltage references require special design techniques in order to cancel the components of the reference voltage that are changing linearly or nonlinearly with operating conditions such as temperature. The voltage references realized by canceling the linear components are named as first-order references, while the ones realized by canceling the nonlinear component in addition are named as second-order or higher-order references. The degree of a voltage reference is totally dictated by the accuracy requirements of the target application. Due to the shrinkage in device dimensions, mainly limited by the photolithography techniques, the dynamic operating range reduces and supply levels get lower which also keep the electrical fields present in devices at a tolerable level [1]. Thus, high-performance applications dictate the use of more precise voltage references with challenging specifications.

Today, various kinds of circuits such as phase-locked loops (PLLs), dynamic random access memories (DRAMs), oscillators, and converters require highly accurate voltage references in order to work properly. For example, the resolution of an analog-to-digital (A/D) or digital-to-analog (D/A) converter is limited by the precision of its reference voltage over the circuit's supply voltage and operating temperature ranges. Therefore, the precision voltage references play a pivotal role in today's high-level applications and are expected to fulfill some desired specifications such as

To be accurate over a wide-range of temperature and supply voltage,
Ability to operate at low-supply voltage levels and consume as low power as possible,
Ability to be less sensitive to variations occurring on the supply rail,
Exhibit as low noise as possible.

Most precision references employ the use of a PN junction diode voltage, since it is very predictable (it does not vary significantly over process and its behavior over a given

temperature range is well characterized). Zener-based voltage references and bandgap voltage references are the two commonly used types of references and include the diode voltage as their core building block. However, zener-based references are suitable for high voltage applications while the bandgap voltage references are easily adopted to low voltage applications [1].

Following the previously mentioned specifications, this study aims the design of a novel bandgap voltage reference circuit that is capable of (a) providing a sub-1 V reference output voltage, (b) operating in a wide-range of temperature and supply voltage, (c) exhibiting a high immunity to variations on the supply rail, and (d) consuming low-power.

1.2. Zener-Based Voltage References

The kinds of voltage references that make use of a zener diode operating in breakdown region are called Zener-based voltage references. The reason for reverse biasing the diode is that in this mode of operation the changes in the load-current results in less fluctuations in the diode voltage. Therefore the output resistance seen from the cathode of the diode typically varies between 10 and 300 Ω.

The zener diodes typically have a breakdown voltage between 5.5 to 8.5 V with a positive temperature drift approximately between +1.5 and 5 mV/°C. This temperature dependence of the zener diode can be compensated via using elements with negative temperature coefficients (TCs) such as forward-biased diodes (TC≈-2.2 mV/°C per diode). One such configuration is illustrated in Figure 1.1. Here the temperature drift of the zener voltage is compensated via the use of the network composed of a forward biased diode with resistors R_1 and R_2. These resistors are selected so that the positive temperature dependence of the zener voltage is compensated by the negative temperature dependence of
the forward-biased diode voltage. The resulting output voltage is given as

$$V_{REF} = V_Z + V_{BE}\left(1+\frac{R_2}{R_1}\right) \tag{1.1}$$

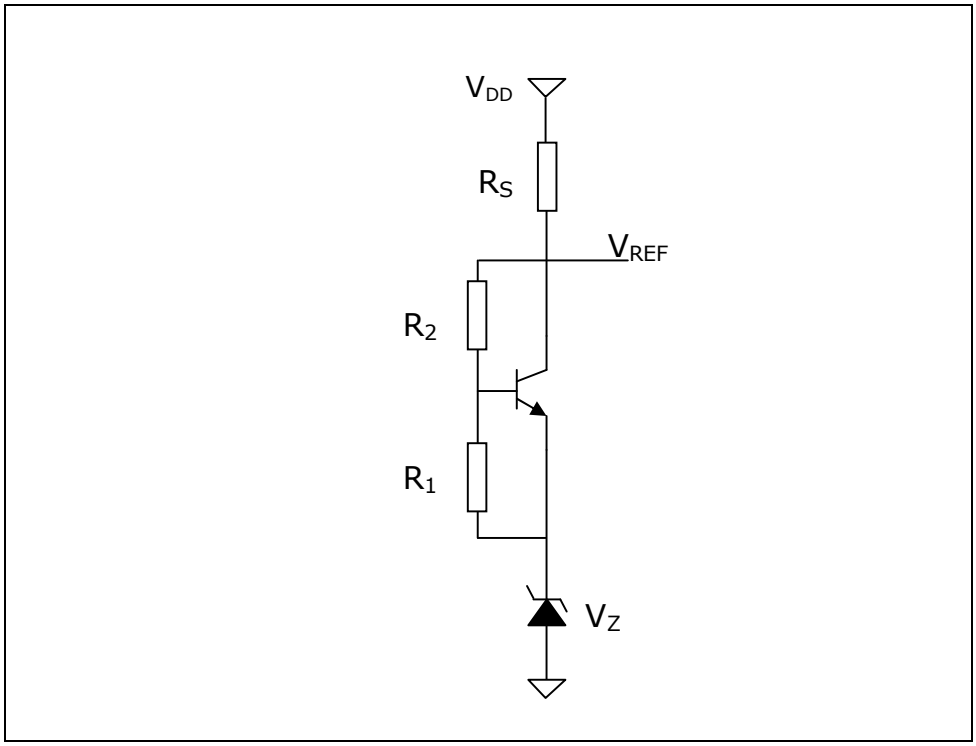

Figure 1.1. First-order zener-based voltage reference

where V_Z *is* the zener voltage and V_{BE} is the forward-biased diode voltage. Equation (1.1) reveals that, improving the temperature performance of the zener-based references comes at the expense of higher supply voltage than a zener-based reference without temperature performance enhancement. Therefore, zener-based voltage references are preferred in high-voltage applications with supply voltages ranging between 6 and 9 V [1].

1.3. Bandgap Voltage References

First-order and second-order voltage references that base their operation on the use of forward-biased diodes are named as *bandgap voltage references* because the temperature compensated reference output voltage is equal to or a fraction of the bandgap energy of the material used in the process. Bandgap voltage references are far more precise and suitable for operation at low-supply voltage levels than the zener-based ones. The main principle of the bandgap reference design is to cancel the linear temperature drift of a forward diode voltage whose behavior is complementary to absolute temperature (CTAT) with an artificially generated voltage component that is varying proportionally to absolute temperature (PTAT). This results in a first-order bandgap voltage reference with a reference output voltage whose value deviates significantly from the target value as the operation temperature range widens.

In order to obtain a reference output voltage with a rather less deviation from the target value over a wide temperature range, the nonlinear temperature drift of the forward diode voltage must also be compensated by generating nonlinear voltage components within the circuit. This type of temperature compensation is called as the second-order compensation or curvature-correction.

Figure 1.2 illustrates the cross-sectional view of this practical diode in detail. The parasitic vertical PNP BJT is formed by the p^+ implant (emitter), n-well (base), and p-substrate (collector). Here, the substrate is connected to ground with the n-well and thus a diode structure is obtained. During device operation, the current injected into the substrate must be collected efficiently, thus, good guard rings are used to surround the structure in order to protect this current to flow in other parts of the chip [2].

1.3.1. Bandgap Voltage Reference Terminology

In this section, often-encountered terms regarding the bandgap references are explained in detail.

Bandgap Energy**:** Bandgap energy of a semiconductor is measured in electron-volts (where 1 electron-volt, eV, is $1.6\text{x}10^{-19}$J). This is the energy difference between the conduction band and valence band of the semiconductor. The bandgap energy of silicon as a function of the temperature is given as

$$E_G(T) = 1.16 - (702\times10^{-6})\cdot\frac{T^2}{T+1108} \tag{1.2}$$

where the term T represents temperature in Kelvin degrees (273.15+°C). For the case of silicon, equation (1.2) reveals that the bandgap energy of silicon is approximately 1.1 eV at room temperature (300 °K) and decreases with increasing temperature resulting in a negative TC for diode voltage.

CTAT: This term stands for **c**omplementary **t**o **a**bsolute **t**emperature and used for defining the behavior of a quantity (i.e., current, voltage…etc.) that reduces in value with increasing temperature.

PTAT: This term stands for **p**roportional **t**o **a**bsolute **t**emperature and used for defining the behavior of a quantity that increases in value with increasing temperature.

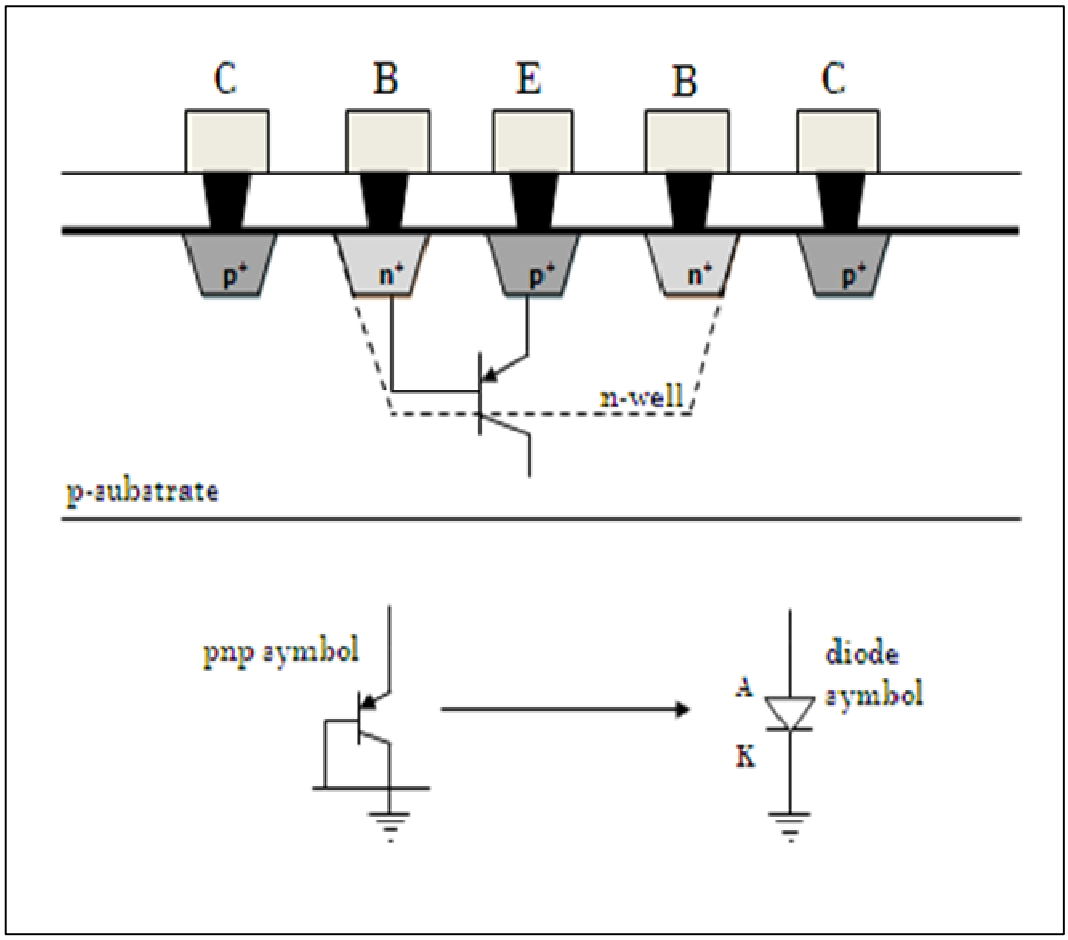

Figure1.2. Practicalrealization of a diode using a vertical parasitic PNP BJT

Temperature Drift and Temperature Coefficient (TC): The performance of a voltage reference is measured by its variation over operating conditions such as supply voltage or temperature. Temperature drift refers to the variations resulting from the steady-state changes in temperature and typical metric used for quantifying these variations is the temperature coefficient. TC is normally expressed in parts-per-million (ppm) per degree Celcius (ppm/°C) and the relation is given in equation (1.3) [1].

$$TC_{reference} = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} \tag{1.3}$$

Line Regulation (LNR): Line regulation of a voltage reference is another performance metric and it refers to the variations in reference voltage caused by the steady-state changes in the supply-voltage.

Initial Accuracy and Overall Accuracy: Initial accuracy actually represents the deviation of the measured value of the output voltage than the targeted one during design period. For this reason, design procedure must take process variations into account from die to die, wafer to wafer, and lot to lot. Therefore, in order to meet the target value of the reference output voltage a trim network must be included in the circuit. Overall accuracy, on the other hand, is determined primarily by the initial accuracy of the reference and secondarily by the temperature drift and the line regulation performance of the same circuit. The relation can be represented as given in equation (1.4)

$$Accuracy = \frac{\Delta V_{ref,IA} + \Delta V_{ref,T} + \Delta V_{ref,LNR}}{V_{ref}} \tag{1.4}$$

where the terms in the nominator represents the variations in the reference voltage due to process, temperature and supply voltage, respectively. The overall accuracy can be represented in parts-per-million (ppm), percent (%), or bits [1].

Power Supply Rejection (PSR): Power supply rejection (PSR) is the ability of a circuit to reject variations occurring in the power supply line. In other words, it can be explained as the gain from power supply line to the output of the circuit and it should be as low as possible. The relation is given in equation (1.5) and usually measured in decibel (dB).

$$PSR = 20\log\left(\frac{\Delta V_{\text{out}}}{\Delta V_{\text{supply}}}\right) \tag{1.5}$$

1.3.2. Classical Bandgap Voltage Reference Circuits

The first bandgap voltage reference was introduced by Robert Widlar in 1971 [3]. The simplified version of the circuit is illustrated in Figure 1.3. Here the transistor Q_2 is operated at a relatively higher current density than Q_1. Therefore, the difference between the base-emitter voltages of these transistors appears across the resistor R_3. This voltage difference, ΔV_{BE}, is a PTAT voltage and causes the current flowing through resistors R_2 and R_3 to be PTAT as well. The compensation of the output voltage at first-order is achieved by properly adjusting the resistor ratio R_2/R_3. The resulting voltage is equal to the extrapolated energy bandgap voltage

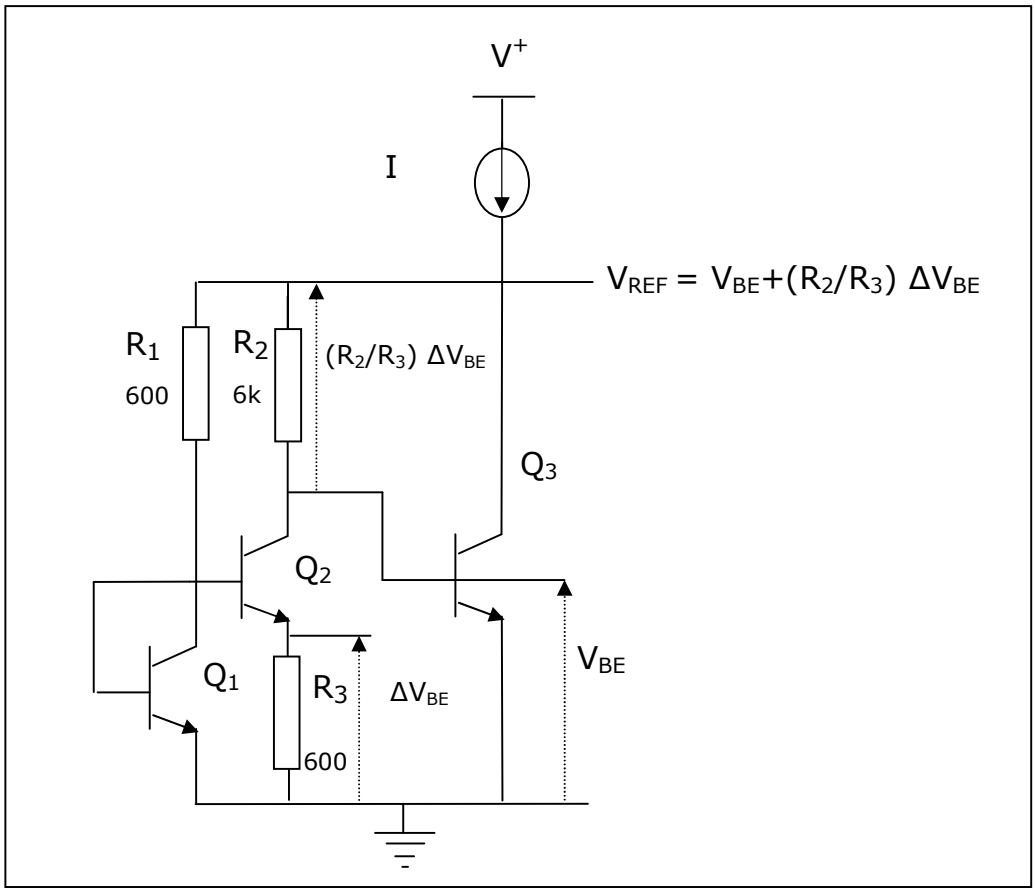

Figure 1.3. Widlar bandgap reference.

of silicon, approximately 1.205 V, and can be given as

$$V_{\mathrm{REF}} = V_{BE3} + \frac{R_2}{R_3}\Delta V_{BE} \tag{1.6}$$

where V_{BE3} is the base-emitter voltage of the transistor Q_3. The drawbacks of this topology are (a) the output voltage cannot be changed other than 1.205 V, and (b) the performance of the circuit is depending heavily on the current density of Q_3 which changes under varying loading conditions.

In 1974, Paul Brokaw proposed a new topology improving the performance of the Widlar bandgap voltage reference [4]. The illustrated topology in Figure 1.4 employs an operational amplifier responsible for equating the collector currents of transistors Q_1/Q_2 whose emitter current densities J_1/J_2 are different. In this case, the difference of the base-emitter voltages forms the PTAT voltage on resistor R_2 and therefore a PTAT current passing through R_1 and R_2. The temperature compensated voltage, which is approximately equal to 2.5 V and the reference output voltage can be formulated as

$$V_{\mathrm{REF}} = V_{\mathrm{BE}} + 2\frac{R_1}{R_2}\frac{kT}{q}\ln\left(\frac{J_1}{J_2}\right) \tag{1.7}$$

where k is Boltzmann's constant (1.38×10^{-23} Joules/Kelvin), T is the absolute temperature in Kelvin degrees (°K), and q is the magnitude of the electronic charge (1.602×10^{-19} Coulomb). The term, kT/q, on the right-hand side of the equation (1.7) is the thermal voltage, V_T, and it is a PTAT term. At room temperature V_T roughly equals to 25.7 mV. Examining equation (1.7) reveals that the ratio of the resistors R_1/R_2 can be used for adjusting V_{REF} to any desired value. Many of the bandgap voltage references base their principle on the Brokaw`s approach. However, since low supply voltage levels and power consumption are the main objectives of today's IC market, classical bandgap voltage references leave much to be desired. Implementing these references in low-cost standard CMOS processes with satisfying performance metrics causes new design approaches to be developed. The next section of this

1.4. Low-Voltage/Low-Power Bandgap Voltage Reference Design Approaches in CMOS Technology

A typical CMOS bandgap reference is shown in Figure 1.5. The reference output voltage V_{REF} of can be expressed as

$$V_{REF} = V_{EB2} + \frac{R_2}{R_1}V_T\ln\left(\frac{A_1}{A_2}\right) \tag{1.8}$$

where V_T is the thermal voltage and A_1/A_2 are the emitter junction areas of the bipolar junction transistors Q_1/Q_2. The first term on the right-hand side of the equation (1.8) is the CTAT term

and the second term is the PTAT term. Examining this architecture reveals that the minimum supply voltage for proper operation of the reference circuit can be expressed as

$$\min\{V_{DD}\} = V_{REF} + V_{DSsat\_M_2} \tag{1.9}$$

Typical value of V_{REF} is about 1.25 V, while the drain-source saturation voltage of M_2, V_{DSsat_M2}, ranges between 0.1 and 0.3 V resulting in a theoretical minimum supply voltage of approximately 1.4 V. However, as the technology scales down, so do the required supply voltage levels. Recent portable applications and medical implant devices demand supply voltage levels

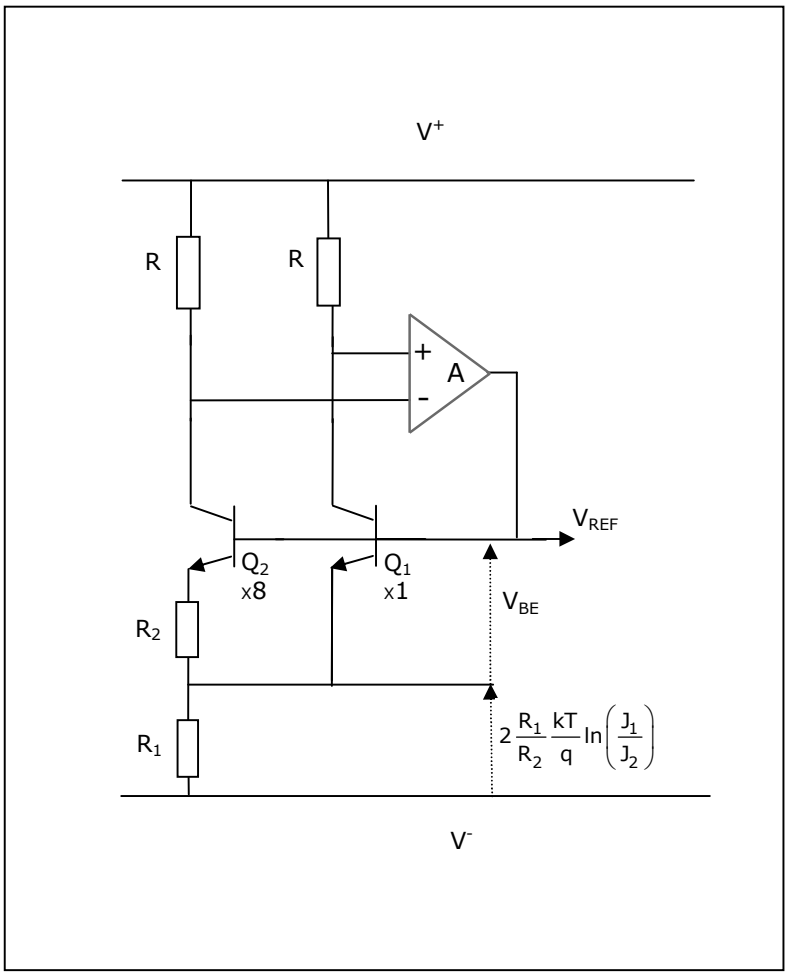

Figure 1.4. Brokaw bandgap voltage reference

around 1 V and even less. On the other hand, the threshold voltages of the devices do not scale at the same rate. Therefore, IC design becomes more challenging and conventional designs do not satisfy the need for operation at such low supply voltage levels.

Although the value of the reference output voltage can be lowered below the typical value 1.25 V using design techniques such as resistive subdivision or current mode techniques, design of error amplifiers below this value is one of the main bottlenecks residing before the circuit designers. As illustrated in Figure 1.5, error amplifier is the core component responsible for generating the PTAT component of the reference circuit. In order to design a reference circuit with tolerable accuracy, the error introduced by the error amplifier must be as low as possible which calls for a high open-loop gain. However, implementing high gain error amplifiers at low supply levels with high threshold transistors is very troublesome. As a result, new topologies adopting innovative methods are required. In this section, a literature review of reported low-voltage bandgap reference design approaches is presented.

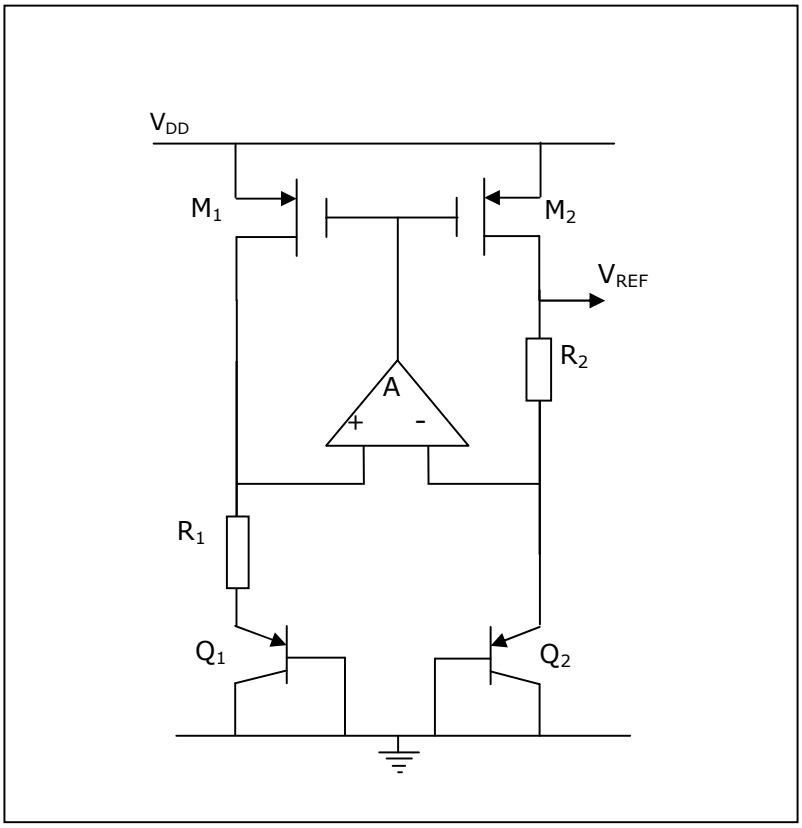

Figure 1.5. Typical CMOS bandgap voltage reference

1.4.1. Current-Summing and Voltage-Summing Bandgap Voltage Reference Circuits

Ripamonti *et al*. [5] proposed two alternative bandgap voltage reference circuits for low-supply voltages in a flash memory environment. Both of these circuits allow low-supply low-power operation. The first technique sums two currents with different temperature dependency on a resistor and the resistor value further controls the magnitude of the output reference voltage. The architecture of the current-summing circuit is illustrated in Figure 1.6.

The current-summing circuit is divided into three sub-blocks. The first block is a simple beta-multiplier current reference sourcing a PTAT current while the second block generating a CTAT current. These currents are then added and forced on the resistor R_{REF} and the reference output voltage V_{REF} is generated. The minimum supply voltage required for proper operation is the sum of the forward biased diode voltage, 0.7 V, and the drain-to-source voltage of the driving transistor, 0.2 V, yielding a total of 0.9 V. Figure 1.7 illustrates the architecture of the voltage-summing circuit. This topology, unlike the former one, employs a differential

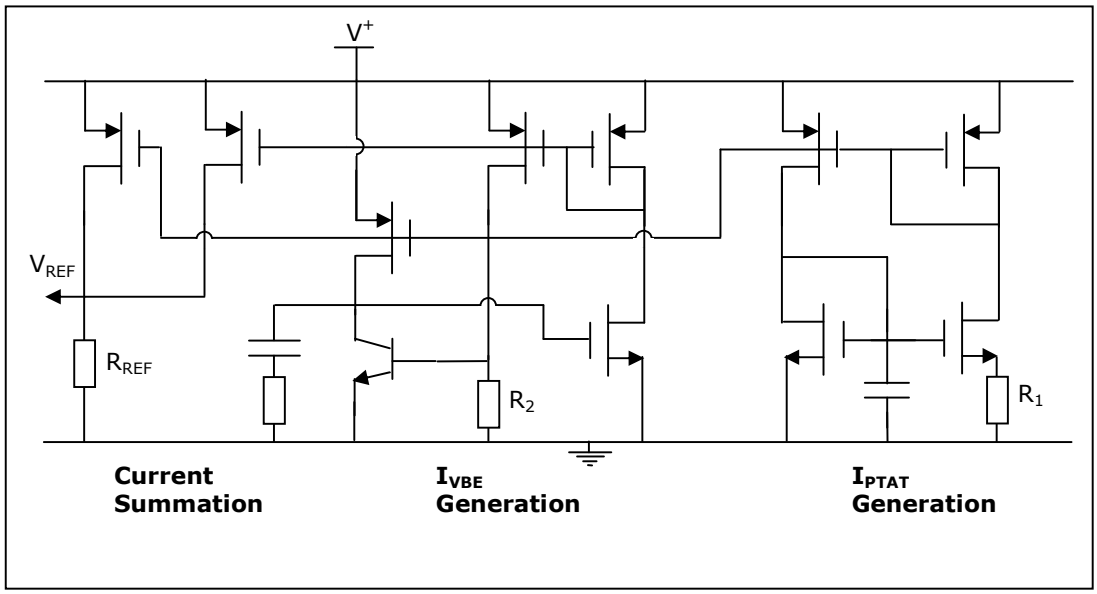

Figure 1.6. Architecture of the current-summing bandgap reference circuit

amplifier with unmatched bipolar input transistors whose offset voltage used for PTAT voltage generation. The output node of the circuit has a buffered structure that allows loads drawing current from this node; however, the current-mode topology should bias capacitive loads such as a gate of a MOSFET for performance purposes. On the other hand, using a differential amplifier increases the overall current consumption of the circuit which results in higher power consumption than the former architecture. In addition to that, the minimum supply voltage for proper operation of the voltage-summing circuit is higher than the current-summing circuit.

For these reasons, the author chose the current-mode topology to realize and tested the circuit through simulations performed in a supply voltage range of 0.9 to 2.5 V. The output voltage is found to change by at most 2%. The variation of the output voltage over temperature is also observed in a temperature range of -20 to 100 °C; however, a specific value is not mentioned.

1.4.2. Bandgap Voltage Reference Employing Dynamic Threshold MOS Transistors

Annema [6] proposes a bandgap voltage reference employing dynamic threshold MOS transistors instead of normal diodes. A DTMOST is simply a MOS transistor whose gate and backgate are interconnected and a cross-sectional view of this structure is shown in Figure 1.8. In a twin-well p-substrate CMOS process only the p-type DTMOST's can be used because the

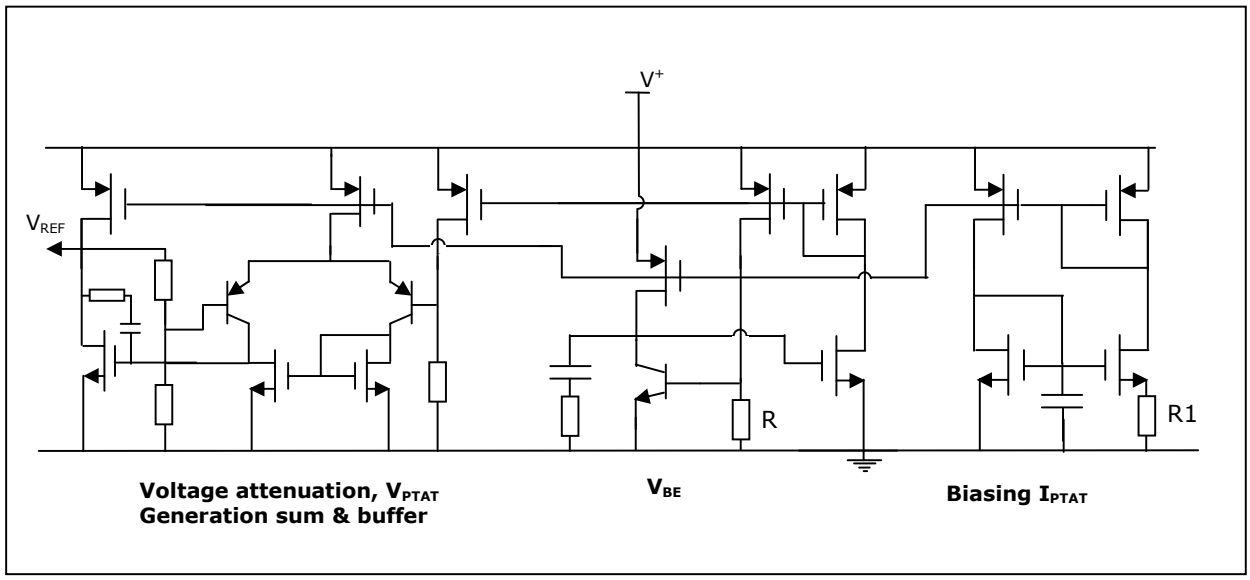

Figure 1.7. Architecture of the current-summing bandgap reference circuit

p-well of n-type DTMOST's has a low-ohmic path to the p-substrate which results in a poor control of the latter.

A DTMOST can be considered as (a) a lateral PNP bipolar transistor with an extra gate over the base, and (b) a PMOS transistor with a dynamically regulated threshold voltage (as gate-to-source voltage, V_{GS}, changes the threshold voltage of the device changes as well). The apparent bandgap for p-type DTMOS in a standard 0.35 µm CMOS process extrapolated to 0 °K is about 0.6 V and the temperature drift of V_{GS} at constant current is -1 mV/°K (which are half the values of a bipolar transistor or a diode) [7]. Figure 1.9 illustrates the low-voltage bandgap voltage reference circuit proposed by Annema. The circuit uses two apparent low material bandgap diodes (DTMOST diodes symbolized by gate-backgate interconnected PMOST diodes) with different sizes; therefore, a low reference output voltage is obtained. In addition the circuit employs a folded-cascode opamp with a DTMOST input stage. These devices need less V_{GS} than those of PMOS transistors. By doing so, the operation of the overall circuit at low supply levels is achieved. The reported circuit consumes a maximum of 1.2 µA of total current consumption in a temperature range -20 °C to 100°C. Reference output voltage varies 4.5 mV (which is reported as 2% change) in the given temperature range and supports operation at a minimum supply voltage level of 0.85 V. However, PSR performance of the circuit is found to be poor, therefore a new architecture with a multistage differential amplifier is designed at the cost of higher supply voltage (higher

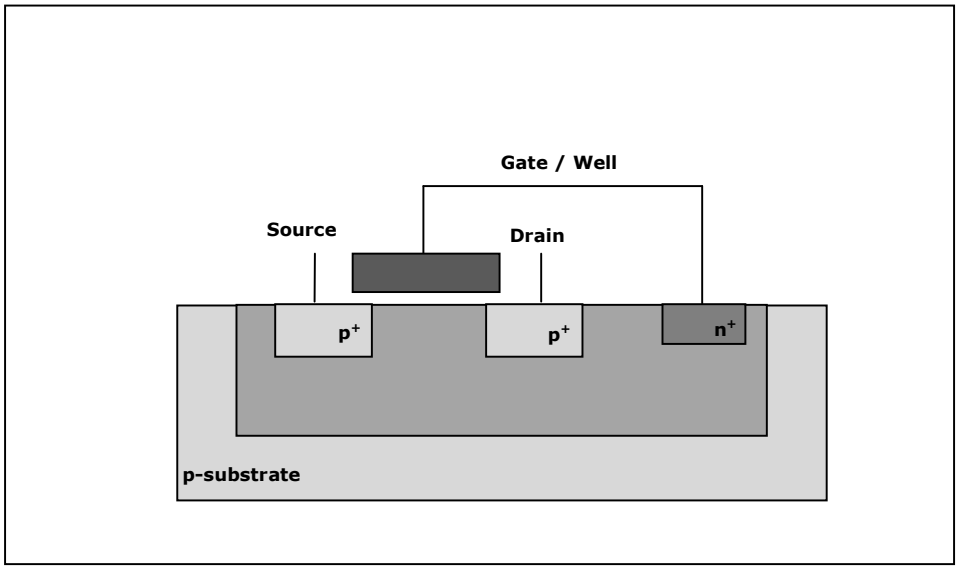

Figure 1.8. Cross-sectional view of a p-type DTMOST

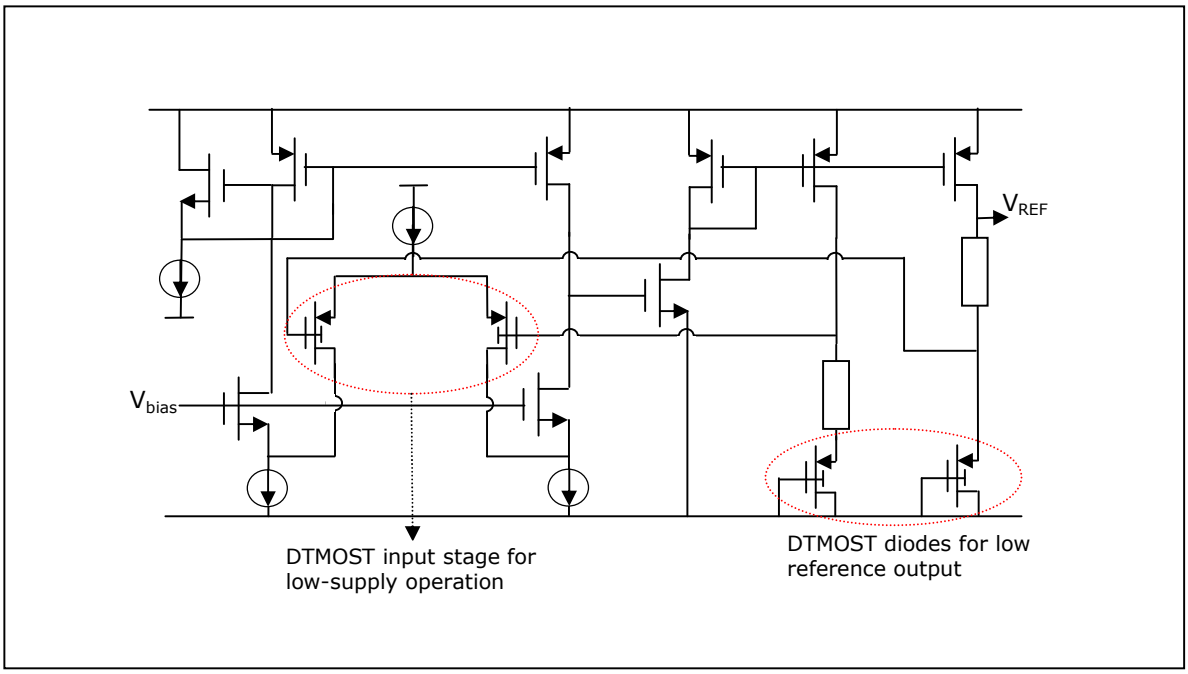

Figure 1.9. Architecture of the DTMOST bandgap voltage reference circuit

than 1.8 V) and current consumption (higher than 3 µA); therefore achieved 78 dB PSR performance at low frequencies.

1.4.3. Current-Mode Bandgap Voltage Reference

Banba *et al.* [7] proposed a current-mode topology in which a resistive divider network was employed at the input of the operational amplifier. Main idea is to generate PTAT and CTAT current components and further obtain a temperature-compensated current to be mirrored on a resistor to generate the reference output voltage. The architecture of the current-mode bandgap voltage reference is presented in Figure 1.10. Here R_1 generates a CTAT current component (which is proportional to forward-biased diode voltage V_{f1}) and this current is replicated at the inverting input of the error amplifier by the matched resistor R_2. PTAT current component, which is proportional to the potential difference between the forward- biased diode voltages dV_f, is generated by R_3. The sum of the currents are then mirrored by M_3 onto R_4 thus the reference output voltage is generated and can be expressed as

$$V_{REF} = \frac{R_4}{R_2}\left(V_{f1} + \frac{R_2}{R_3} dV_f \right) \tag{1.9}$$

where, by proper temperature compensation the term in the brackets yield a reference output voltage of 1.25 V. The resistor ratio R_4/R_2, on the other hand, can be used to adjust the reference output voltage below this value. However, the minimum supply voltage for proper operation of the error amplifier is 2.1 V. A solution to this problem is proposed by using native devices (devices with lower threshold voltages but require additional process steps); however, these devices are not readily available in a standard CMOS process therefore introduces higher cost to manufacturing. Experimental results report, reference output, V_{REF}, is 515 mV±1 mV at room temperature over the supply range, 2.2-4 V, and 515 mV±3 mV in the temperature range, 27 to 125 °C.

1.4.4. Modified Low-supply/Current-Mode Bandgap Voltage Reference with Improved PSR Performance

Waltari *et al.* [8] studied on the circuit proposed by [7] and improved the circuit performance through several modifications. The modified circuit is presented in Figure 1.11. One of the modifications is done on the supply voltage limitation of the opamp. The opamp used in [7] is achieving low-supply operation in the case of employing native mosfets. However, in [8], the resistors R_1 and R_2 are replaced with their series equivalents via placing resistor divider networks. In the proposed circuit, the opamp is now driven by the nodes $V_3$and V_4 thus

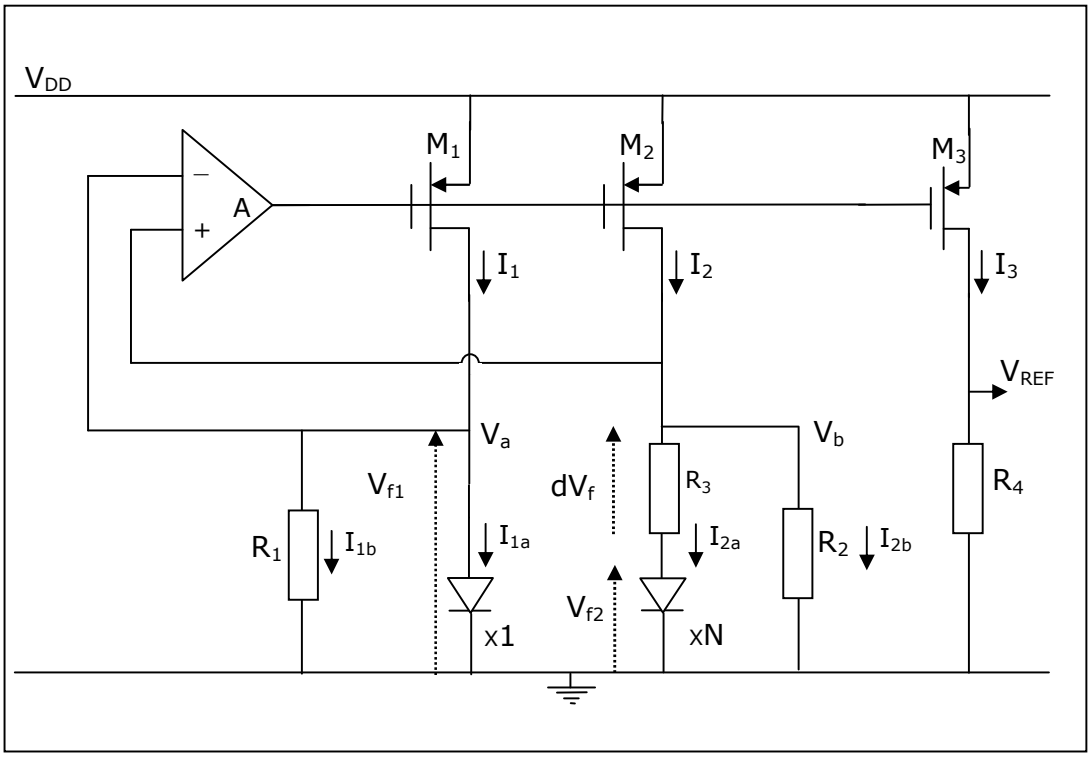

Figure 1.10. Current-mode bandgap voltage reference proposed by Banba *et al.*

allowing the BGR circuit operate at supply voltages as low as 0.95 V. The simulations performed on the circuit for the reference output in the temperature range, -20 °C - 100 °C, and over the supply voltage range 0.95 V to 1.5 V.

The variation over on the reference output over the supply voltage range has a spread of 24 %. The second improvement is done on the PSR performance of the BGR circuit. This is achieved via cascoding the current sources in the reference circuit. This results high output resistance for the current sources resulting in less sensitivity to the variation on the supply line.

1.4.5. Employing Transimpedance Amplifier (TIA) in a Bandgap Voltage Reference Circuit

The main bottleneck in low-voltage BGR design is that the common-mode range (CMR) limitation of the error amplifier used in the circuit. The variation of the diode voltage over temperature makes it difficult to design the input differential stage of the error amplifier. As an alternative to the method proposed in [8], Jiang *et al.* [9] came up with a different approach. The topology is based on the current-mode topology proposed by Banba *et al.* [7] and illustrated in Figure 1.12. The proposed technique is based on the use of a transimpedance amplifier (TIA). The idea is to remove the input differential stage of the opamp and replace it

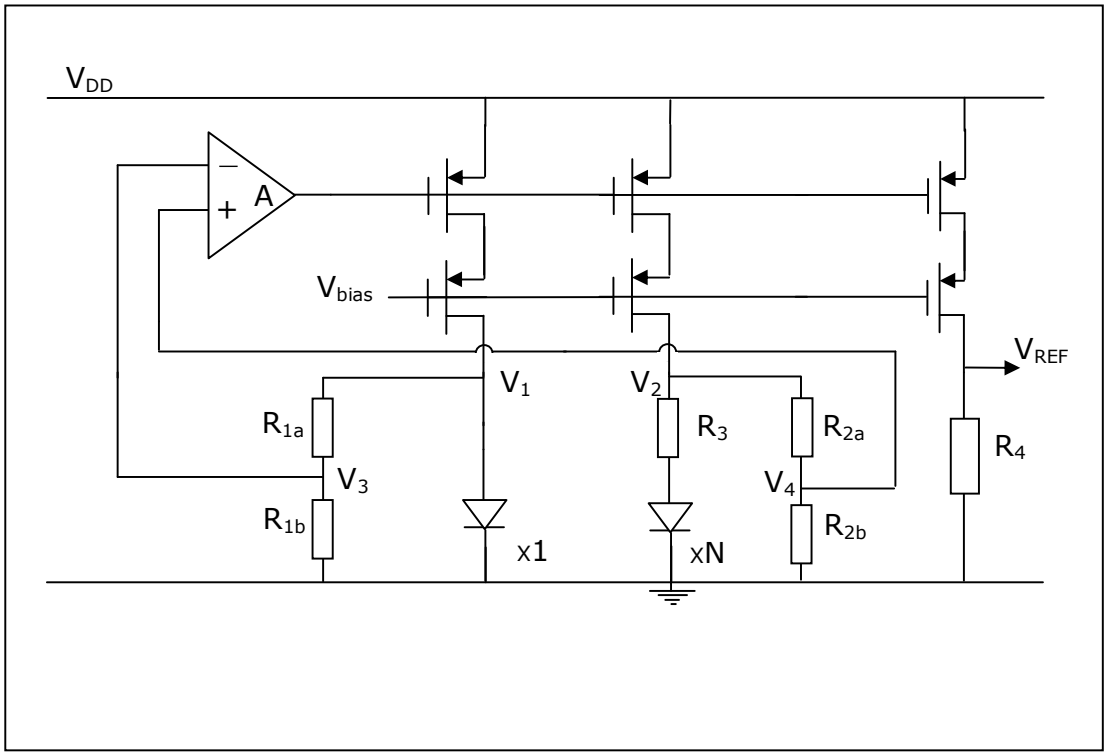

Figure 1.11. PSR-improved current-mode bandgap voltage reference

with resistors which are responsible for sensing the voltage difference to generate the PTAT current. The TIA has a very low input resistance and a very large impedance gain. The two inputs of the TIA are set to a fixed potential V_B at room temperature which is lower than one V_{EB}. The current I_1 is a PTAT current given by the expression

$$I_1 = \frac{1}{R_1} V_T \ln N \tag{1.10}$$

and this current is further summed with I_2 given by the expression

$$I_2 = \frac{1}{R_2}(V_{EB} - V_B) \tag{1.11}$$

The resulting sum of currents is mirrored by M_3 onto R_3; however, the additional current term V_B/R_2 must be eliminated. In order to do so, an artificially generated current which is equal to V_B/R_2 is injected to the output node of the circuit.

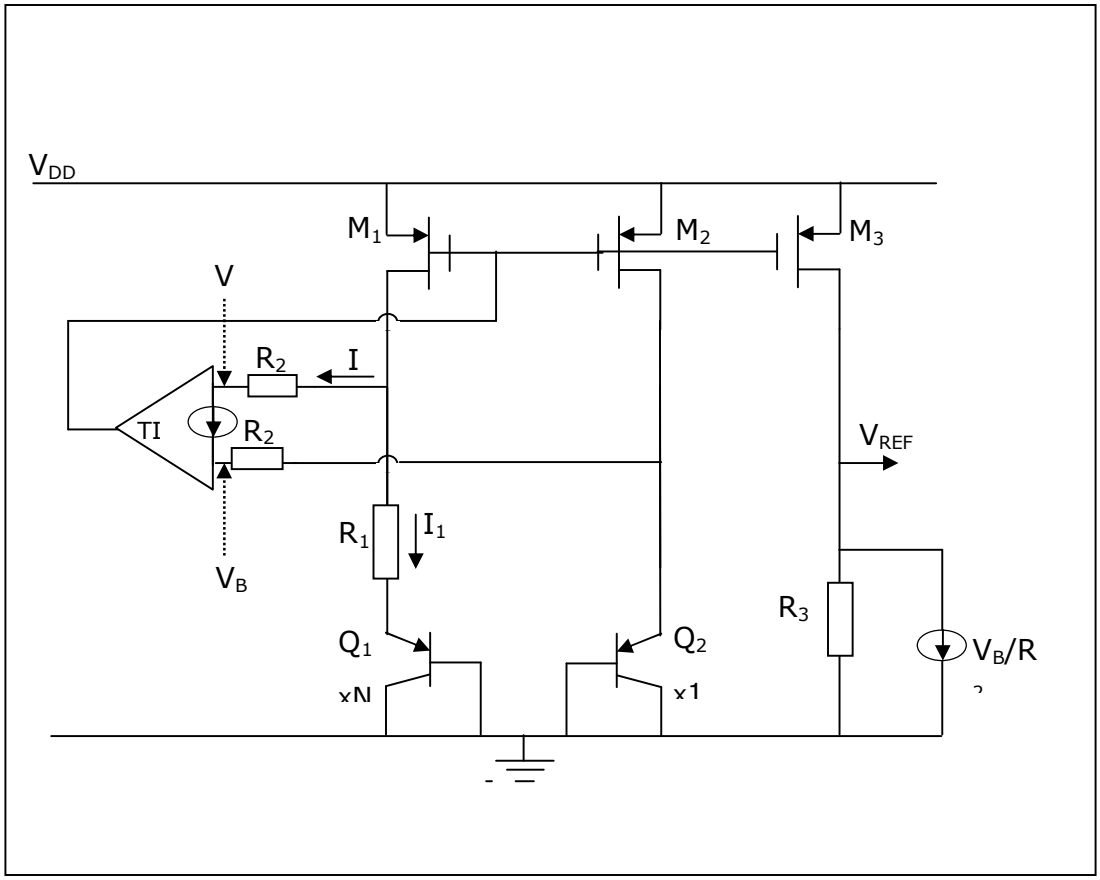

Figure 1.12. Bandgap voltage reference circuit employing TI

Reference output voltage now can be expressed as

$$V_{REF} = \frac{R_3}{R_2}\left(V_{EB} + \frac{R_2}{R_1} V_T \ln N \right) \tag{1.12}$$

Due to the high threshold voltages of the devices in the process at hand, this circuit is operated with a minimum supply voltage of 1.2 V and the reference output voltage is set to 1V. The reported variation of the reference output voltage over the temperature range 0 °C-100 °C is ±1 %. In addition the PSR performance at 1 kHz is measured to be 20 dB.

1.4.6. Two Alternative Techniques Proposed for Low-Supply Bandgap Voltage Reference Design

Examining the current-mode bandgap reference circuit in [7] reveals that the input stage of the opamp is implemented with depletion-mode PMOS transistors that make the circuit not

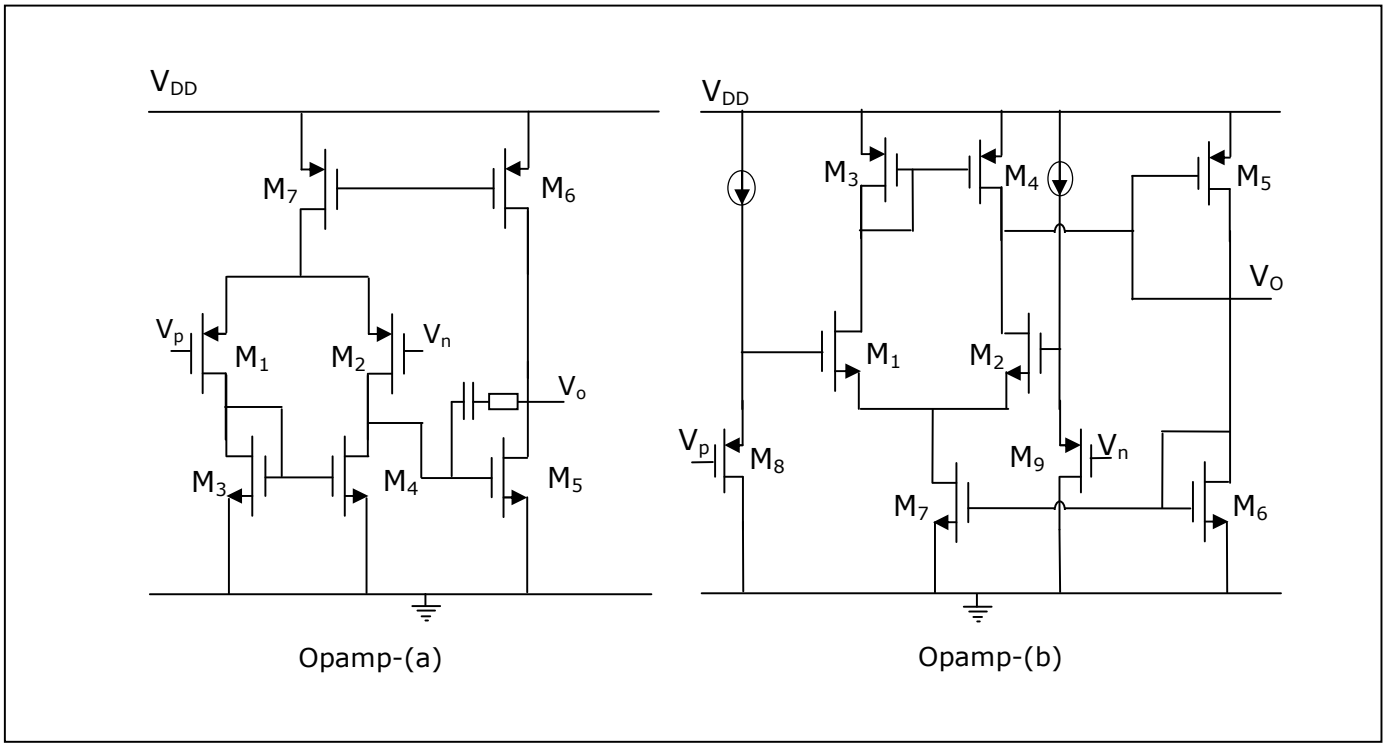

Figure 1.13: Opamps employing (a) weak inversion operation and (b) level shifters at the input

useful in standard, low-cost CMOS technologies in which these devices are rarely available and/or precisely modeled. In order to eliminate this limitation, Pierazzi *et al.* [10] presented two novel implementations of the current-mode bandgap voltage reference circuit supporting supply-levels as low as 0.9 V without deploying such special devices. The solutions proposed for opamp limitation are designing the opamp with (a) a PMOS input stage working in weak inversion, (b) an NMOS input stage with level shifters. The former implementation of the bandgap voltage reference circuit employing the opamp-(a) works properly with supply voltages down to 1.4 V. From this point on, the input devices of the opamp work in weak inversion mode reaching a bias current of few nAs. However, the opamp thus the bandgap reference circuit keeps on operating as the supply voltage reaches the minimum, 0.9 V. Below stage for low-supply operation of bandgap voltage reference circuit proposed in this value, there is not enough loop-gain to keep the bandgap voltage reference circuit at the correct bias value.The second proposed bandgap voltage reference circuit employs the opamp-(b). The opamp uses input level shifters realized by a couple of PMOS devices in order to provide a correct common-mode voltage at the input of the NMOS differential stage. The opamp can work supply levels down to 1.4 V; however, below this value the differential pair transistors enter nonsaturation region which causes a significant reduction in gain.

2. PROPOSED TOPOLOGY

2.1. Target Specifications

Up to this point, the desired characteristics of the voltage references are defined and the several approaches to implement them with lower reference output voltage and supply voltage levels are presented. Due to continuous reduction in supply voltage level and power consumption it is concluded that designing voltage references with high performance metrics in a standard CMOS process has become a challenging task.

As mentioned earlier, although providing a reference output voltage lower than conventional is possible, implementing error amplifiers at such low supply voltage levels is still a major bottleneck. In addition, low current consumption (especially dictated by portable applications) inevitably results in higher output noise and this has to be reduced to tolerable levels as much as possible.

In this chapter, a novel bandgap voltage reference circuit which is meeting the previously mentioned performance specifications will be presented. In order to do so, several target specifications are set. These can be listed as

Operation in a wide supply voltage range, 1 V to 5.5 V, with low power consumption (a maximum current consumption of 5 µA is set),
Low reference output voltage (500 mV-600 mV) and low output voltage variation over a wide-temperature range, typically -40 °C to +125 °C,
Less sensitivity to variations on the supply rail (high PSR),
Exhibiting low output noise as possible.

In the conclusion part of the thesis, the proposed bandgap voltage reference will be compared with recently reported bandgap voltage references and it will be concluded that the proposed topology is meeting the target specifications to an **extremely** satisfying extent.

2.2. Bandgap Voltage Reference Core Circuit

The architecture of the proposed bandgap voltage reference circuit is developed around thecore topology proposed in [11] and shown in Figure 2.1. This core topology is a

combination of (a) the popular low-voltage reference proposed in [7] and (b) a simplified derivative of the curvature-correction technique proposed in [12].

An operational transconductance amplifier (OTA) controlling the matched current sources M_1 and M_2 imposes identical voltages V_1/V_2 across Q_1 and the combination of R_O/Q_2, and thus generates I_{PTAT} in these branches. An I_{CTAT} is generated across R_1, and is replicated across R_2, which is matched to R_1. Therefore, the firs-order temperature dependence of I flowing through M_1 and M_2 is eliminated. The second-order (curvature-correction) compensation is accomplished by extracting a current $I_{CURV} \alpha\ Tln\ (T)$ from each input node of the OTA.

This is done by $M4/Q_3$ and matched resistors R_4/R_5. The temperature-independent current I is mirrored by M_3 onto R_3 to generate a scaled bandgap-reference voltage V_O.

The parameters[1] of this core topology are determined from a detailed analysis including the secondary effects such as the offset voltage at the input of the OTA (V_{OS}) and mismatches in resistor values (ΔR), mirrored currents (ΔI), and bjt forward current-gains (β_F). The resulting design equations are given as

$$R_1 = \frac{V_G(T_0)}{I} \tag{2.1}$$

where $V_G\ (T_0)$ is the bandgap voltage of silicon at a reference temperature T_0, e.g., 1.15 V at 300°K,

$$R_4 = R_5 = \frac{R_1}{C} \tag{2.2}$$

where C is a process-dependent constant with a typical value around 2.5,

$$R_3 = \frac{V_O(T_0)}{V_{BG}(T_0)} R_1 \tag{2.3}$$

[1] The design equations used to determine these parameters are the results of a detailed analytical analysis performed on the core topology given in Figure 2.1. The analyses regarding the first and second-order compensation scheme is in Appendix A.

And

$$\frac{R_0}{\ln N} = \frac{R_1}{V_{BG}(T_0) - V_O(T_0)} \frac{kT_0}{q} \tag{2.4}$$

Step-by-step analysis, given in detail in Appendix A, yields the BGR output voltage as

$$V_O(T) = \frac{R_3}{R_1}\left\{ V_1(T) + \frac{kT}{q}\left[\frac{R_1}{R_0}\ln N - \frac{R_1}{R_4}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N} \right) \right] + \frac{kT}{q}\frac{R_1}{R_4}\ln\frac{T}{T_0} \right\} \tag{2.5}$$

in which the term $\frac{R_1}{R_4}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N} \right)$ is introduced by curvature correction mechanism and must be satisfying the relation

$$\frac{R_1}{R_4}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N} \right) \ll \frac{R_1}{R_0}\ln N \tag{2.6}$$

In addition, the term $\frac{kT}{q}\frac{R_1}{R_4}\ln\frac{T}{T_0}$ is the curvature correction term introduced by the curvature correction network composed of resistors R_4/R_5, diode-connected bipolar transistor Q_3, and the current source M_4 in Figure 2.1. Examining the temperature compensation mechanism analyzed in Appendix A together with the reference output voltage expression given in equation (2.5) reveals that the linear and nonlinear temperature drift of the diode voltage V_1(T) are compensated by the terms $\frac{kT}{q}\frac{R_1}{R_0}\ln N$ and $\frac{kT}{q}\frac{R_1}{R_4}\ln\frac{T}{T_0}$, respectively.

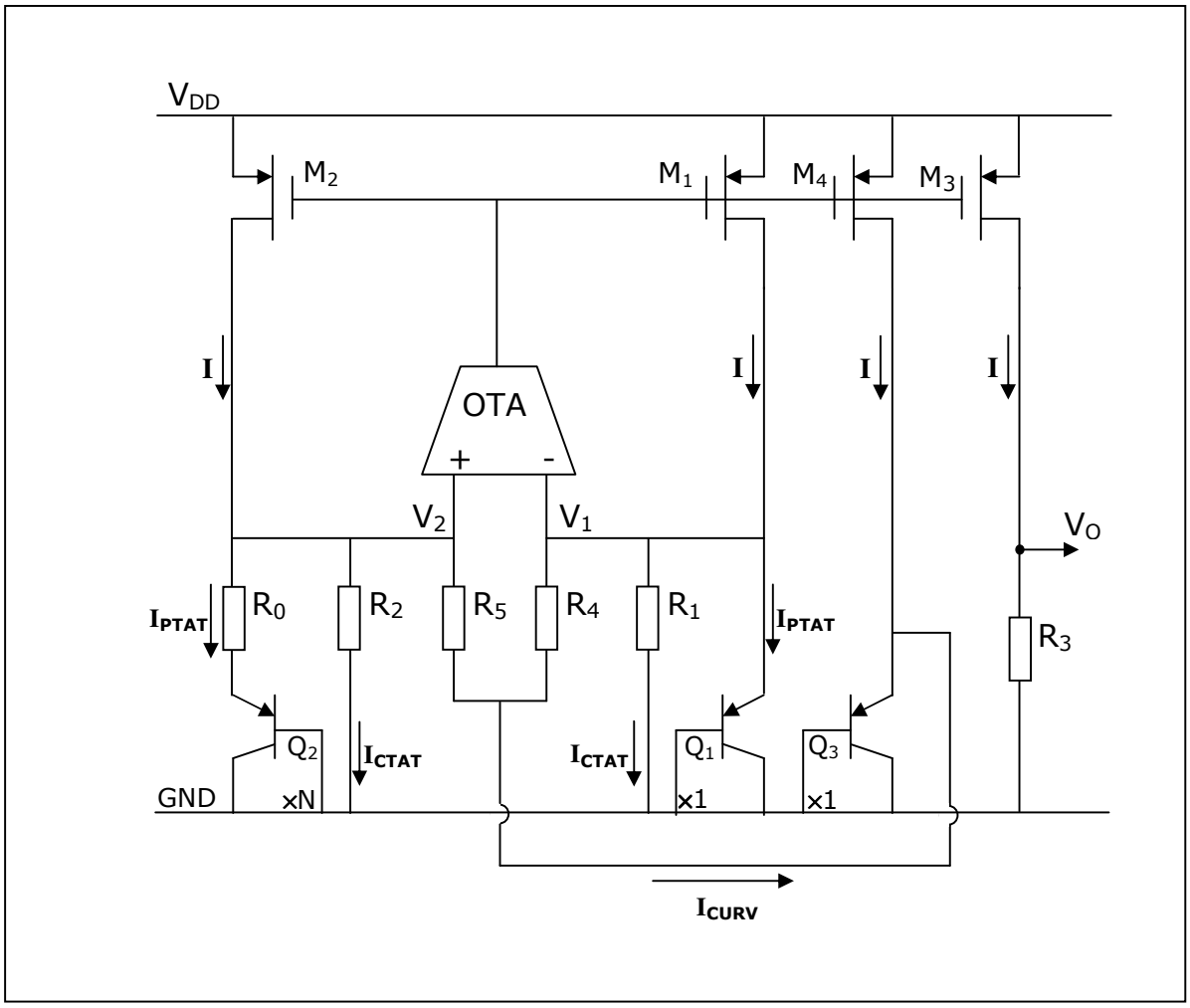

Figure 2.1. Malcovati topology

2.3. Problems with the Core Topology and Proposed Solutions

Considering the core circuit in Figure 2.1, it is seen that some of the target specifications which are set in section 2.1 cannot be satisfied with this topology at hand. To be specific, specifications on the power-supply input range and the PSR cannot be handled directly by the core. In this section, these problems are discussed and solutions are offered.

2.3.1. Power Supply Range Problem and Proposed Solutions

Adopted process for circuit realization is the AMS 0.35 µm CMOS technology (C35B4C3) which is a high performance digital and analog process comes with 4 metal layers, 2 poly layers, and a high resistance poly layer. This process includes two groups of MOS transistors supporting operation at supply levels up to 3.3 V and 5 V. In addition, AMS C35B4C3 technology comes with four types of parasitic vertical PNP device models named as

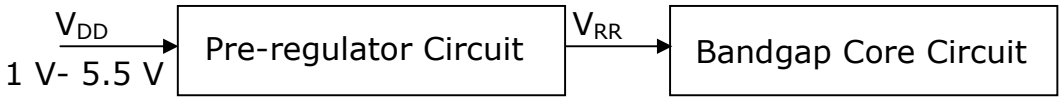

Figure 2.2. Proposed solution to power supply range problem.

VERT-LB, VERT-TYP, VERT-HB, and VERT-HS having β_F values of 2.3924, 5.9810, 9.5696, and 9.5696, respectively. Obviously, VERT-HB and VERT-HS have the same β_F values, however, these models are categorized as high-beta and high-speed respectively since some of their parameters are different.

Examining the core topology of Figure 2.1 with the available parasitic vertical PNP devices it is concluded that the base-emitter voltage V_1(T) of Q_1 is expected to vary typically between 370 mV and 740 mV over the very wide temperature range, -40 °C to +125 °C. Since V_2(T) is also to be held at the same value, the common-mode range (CMR) of the OTA should be as wide as 370 mV≤CMR≤740 mV. An OTA with an NMOS-only input stage cannot handle the lower end of this range. A PMOS-only input stage, on the other hand, cannot handle the upper end, because the supply can be as low as 1 V. A rail-to-rail input stage is therefore needed but, for such a stage to operate properly, V_{DD} must be larger than the sum of NMOS and PMOS threshold voltages plus two overdrive voltages plus two compliance voltages although this requirement is somewhat relaxed due to the inevitability of weak-inversion operation imposed by low power operation.

In AMS 0.35 µm CMOS process, just the sum of two threshold voltages equals 1.32 V for 5-V compliant devices and 0.91 V for 3.3-V compliant devices even if body effect is ignored. Therefore, it is virtually impossible to (a) operate the core topology from V_{DD}, whose specified maximum necessitates 5-V compliant devices, and (b) still expect proper functionality at supply voltages down to 1 V. This problem is considerably alleviated with 3.3-V devices but, then, V_{DD} must be stepped down first stepped down in order not to overstress these devices. For this reason, we decided to build the core with 3.3-V compliant devices, and to power it with a regulated supply V_{RR} from a pre-regulator, as explained graphically in Figure 2.2.

Another benefit of this pre-regulator is that it greatly relaxes the constraints imposed on the OTA by power-supply rejection specifications. As a matter of fact, a high PSR need alone

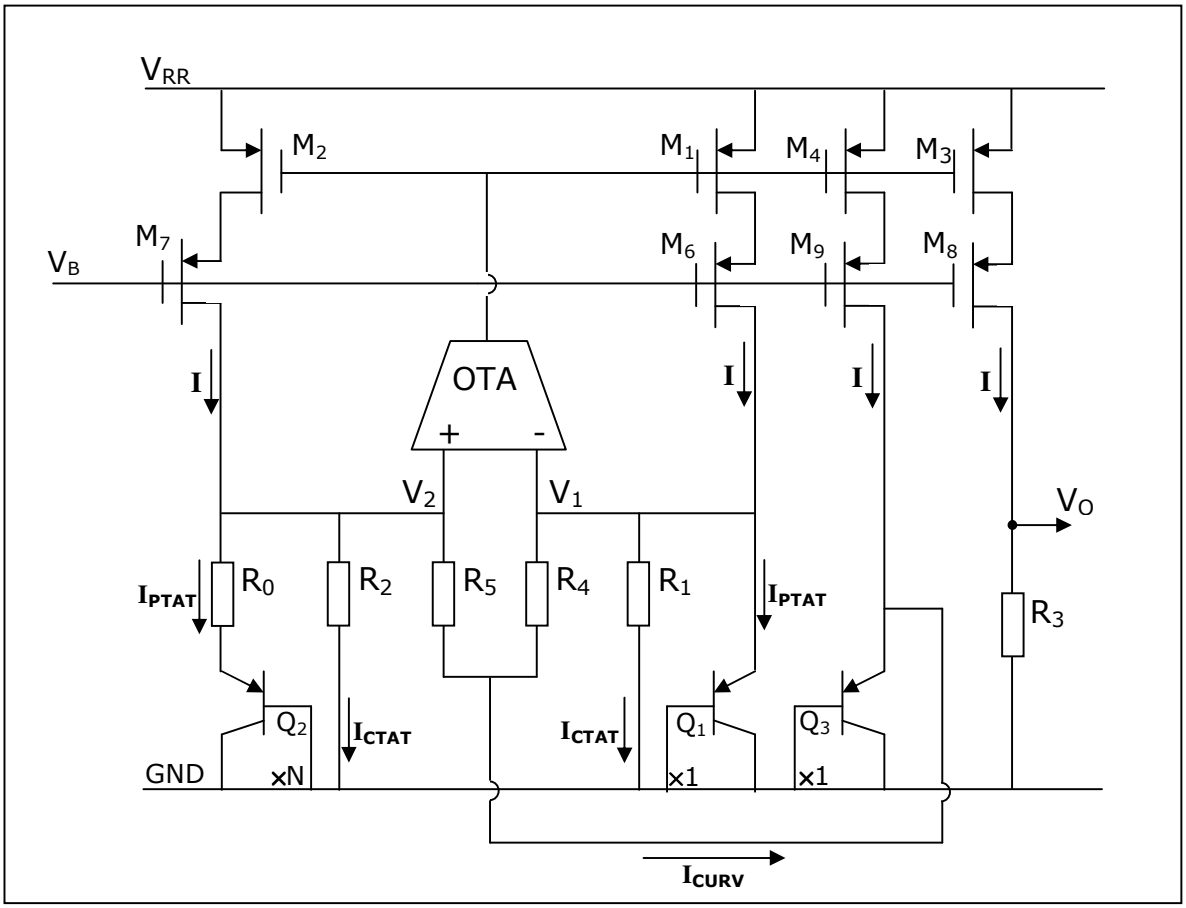

Figure 2.3: Cascoded current source network for improving PSR performance.

would necessitate it even if CMR were not a problem, as discussed in the following subsection.

2.3.2. Power Supply Rejection Problem and Proposed Solution

Initial study[2] of the bandgap core topology of Figure 2.1 revealed a serious PSR problem due to a systematic mismatch between the drain-source dynamic resistance of M_3 and those of M_1/M_2. The reason of mismatch is that the drain voltage of M_3 stays at the temperature-independent V_O somewhere between 500-600 mV, whereas the identical drain voltages V_1/V_2 of M_1/M_2 change between 370 mV-740 mV over the specified temperature range. While PSR from supply line to the two input nodes of OTA can be made large by raising the gain of OTA, that large PSR is replicated at the output only at the particular temperature for which $V_O=V_1=V_2$. Otherwise, PSR at the output is limited by the extent of mismatch, and therefore deteriorates rapidly as the drain-voltage mismatch grows at lower and higher temperatures.

[2] Detailed PSR analysis of the core circuit is performed and given in Appendix B.

This is a fundamental deficiency of any bandgap reference topology whose output node is outside its control loop but we must also recognize the fact that the topologies with in-loop output are not low-voltage compatible. The remedy for this PSR problem is cascoding of all four MOSFET's as shown in Figure 2.3, and biasing the common gate of the cascade devices $M_6/M_7/M_8/M_9$ with a V_{B1} whose PSR is as close to as 0 dB as possible.

2.4. Design

A circuit schematic of the overall bandgap voltage reference topology is presented in Figure 2.4. Start-up circuits are not shown in the schematic and will be illustrated at the end of this chapter.

2.4.1. Pre-regulator Circuit

The pre-regulator circuit is built with (a) a pass device M_{R16}, (b) an error amplifier comprising M_{R9}—M_{R15}, and a beta-multiplier bias generator comprising M_{R1}—M_{R8} together with R_{R1}, R_{R2} and R_{RS}. A voltage divider circuit built with R_{R3} and R_{R4} scales the supply V_{RR}, which is compared with a reference voltage applied to the gate of M_{R10} by the beta-multiplier circuit. All MOSFETs used in the circuit are 5-V compliant and qualified as low $-V_T$.

1 V supply is sufficient to operate a rail-to-rail input OTA built with 3.3-V devices of C35B4C3 but the gain and bandwidth performance falls short of what is needed to achieve a satisfying PSR. Therefore, we decided to set the regulated supply V_{RR} to 1.2 V, and design the pre-regulator circuit with a minimum dropout of 100 mV, and a minimum of 30 dB dc PSR in the regulated range, as depicted in Figure 2.5. Our target value for PSR at 10 kHz is 20 dB for the pre-regulator.

The simulated DC variation of V_{RR} with V_{DD} is given in Figure 2.6 over the specified temperature range. Although the pre-regulator will operate with constant load current for a given temperature range, the dc simulations are repeated for two cases, one for no loading, and another for a load current I_L=4 μA.

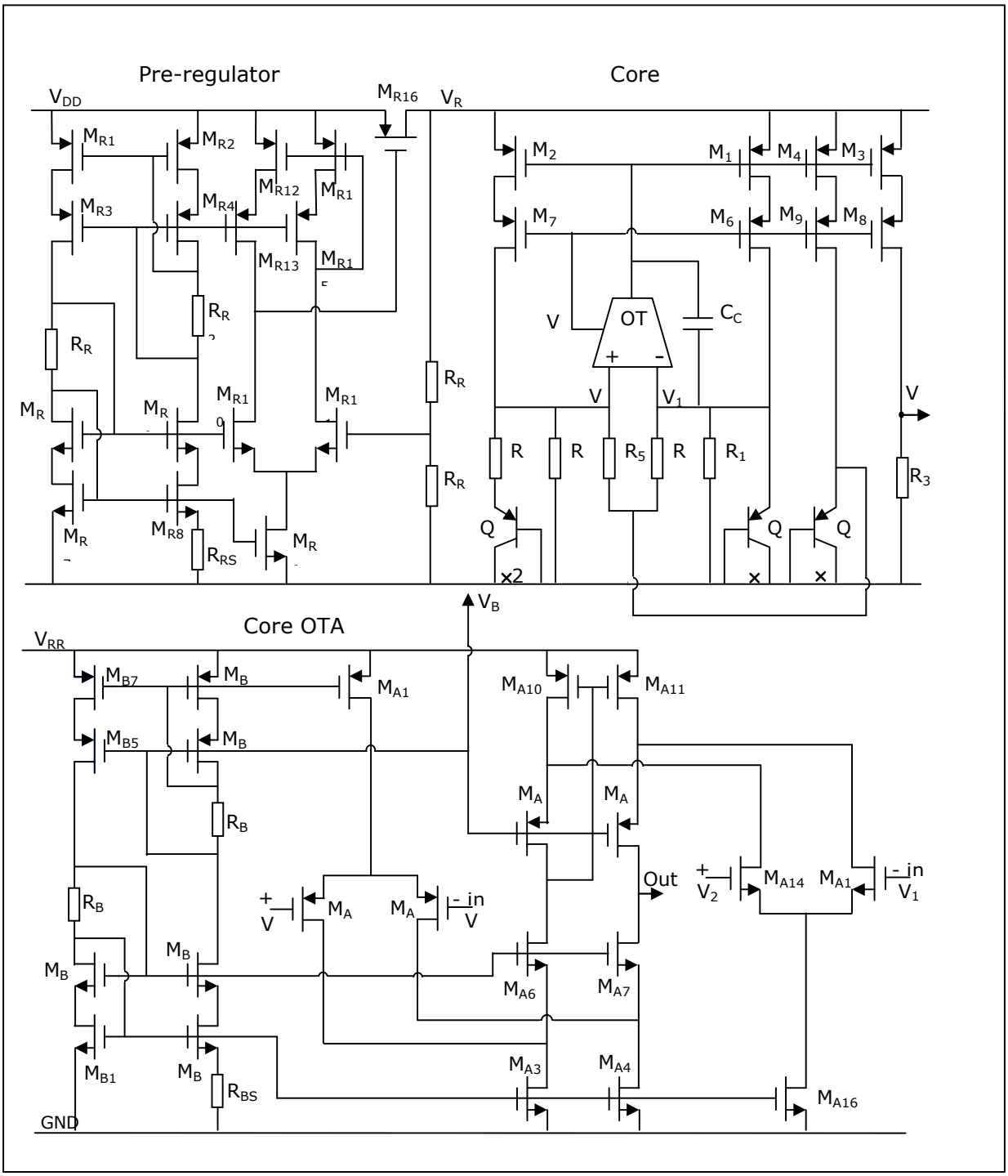

Figure 2.4: Proposed overall bandgap voltage reference topology.

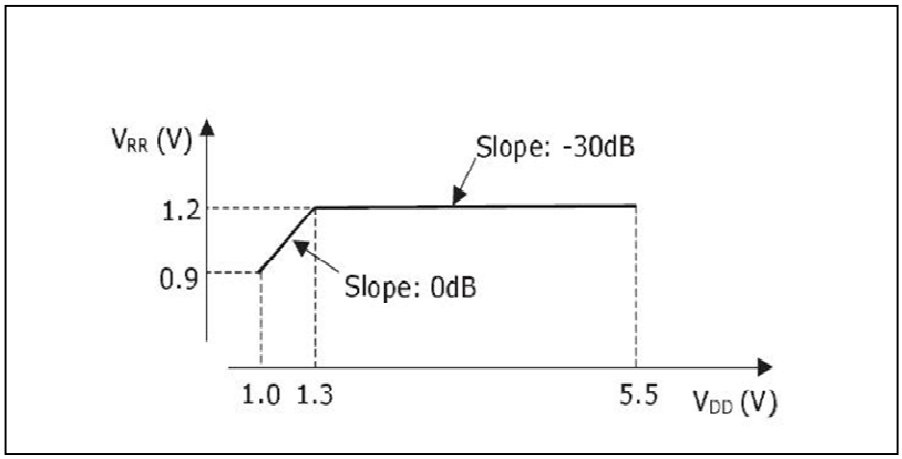

Figure 2.5: Pre-regulator target dc characteristics.

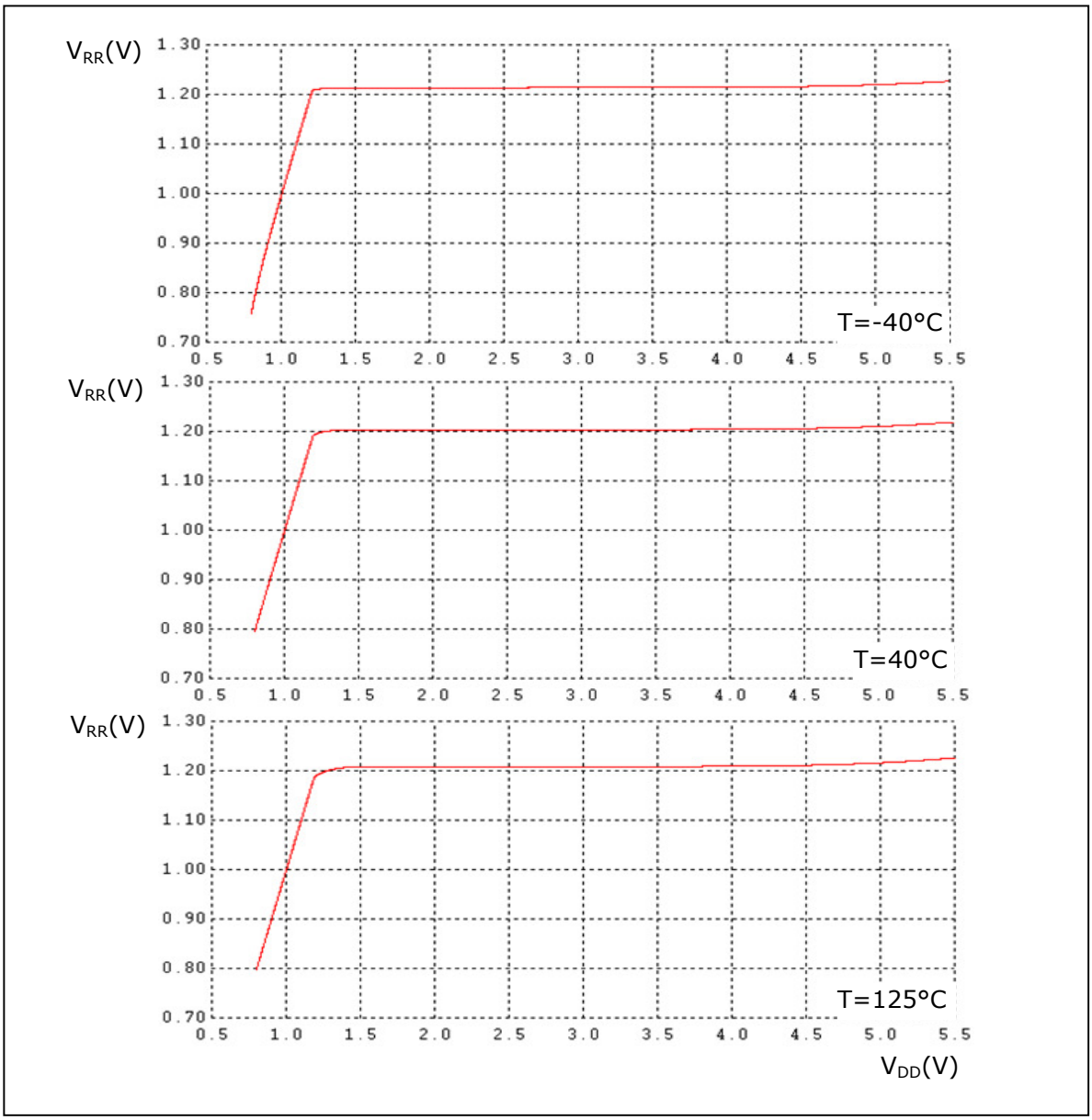

Figure 2.6. Variation of V_{RR} with V_{DD} for T=-40 °C, 40 °C, and 125 °

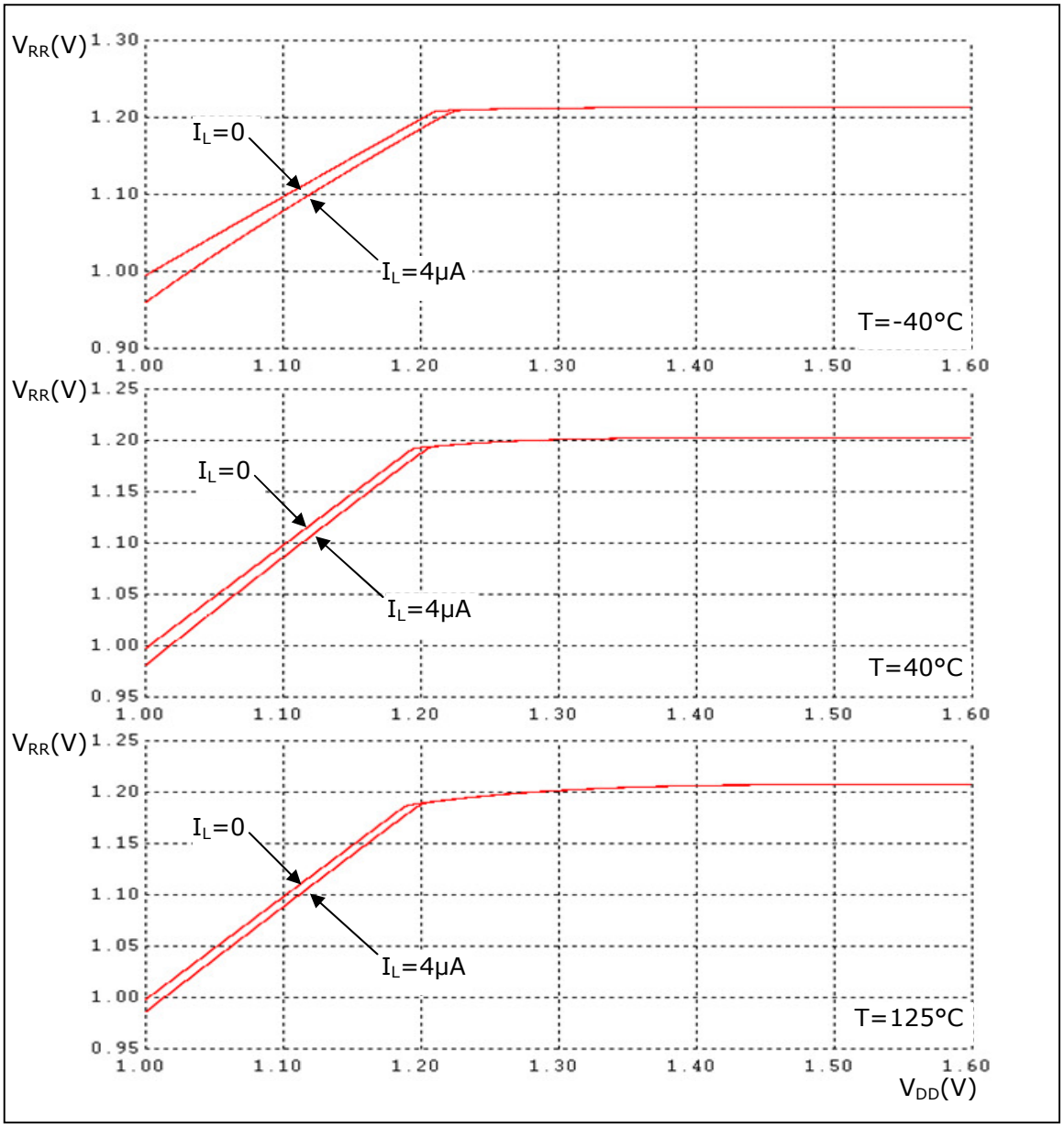

Figure 2.7. Variation of V_{RR} with V_{DD} for no loading and a load current I_L=4 μA

As observed in Figure 2.7, load current up to I_L=4 μA has no significant effect on the regulated range $V_{RR} \geq 1.3$ V. A weak sensitivity is observed only for the unregulated range for smaller values of V_{RR}.

Shown in Figure 2.8 is the current I_p drawn by the pre-regulator for its own consumption as a function of raw supply voltage.

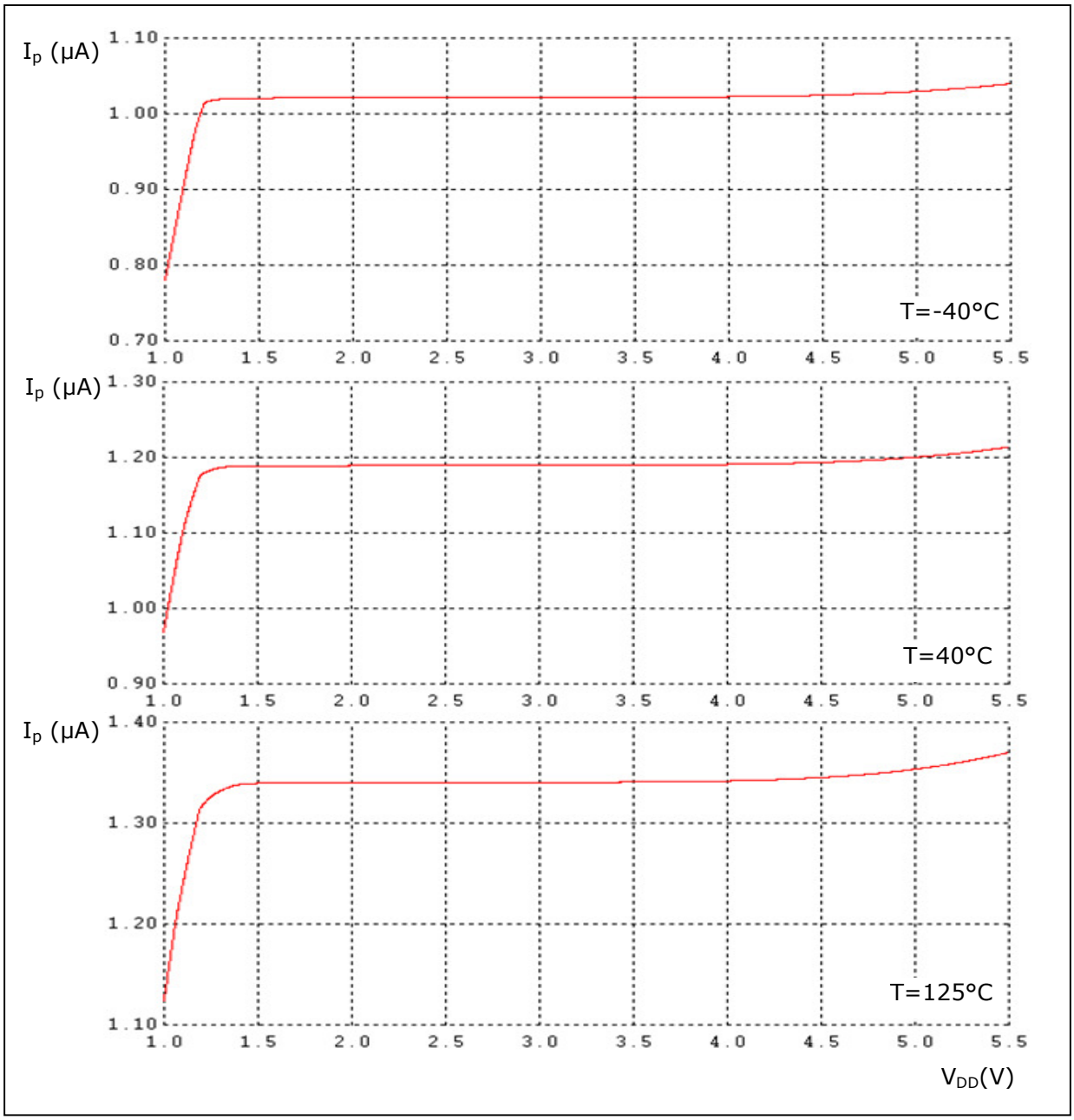

Figure 2.8. Current drawn by the pre-regulator circuit for its own consumption as a function of V_{DD}

As expected for the PTAT current-bias property of the beta-multiplier reference circuit, it is an increasing function of temperature but obviously it remains less than 1.36 µA for T=125 °C.

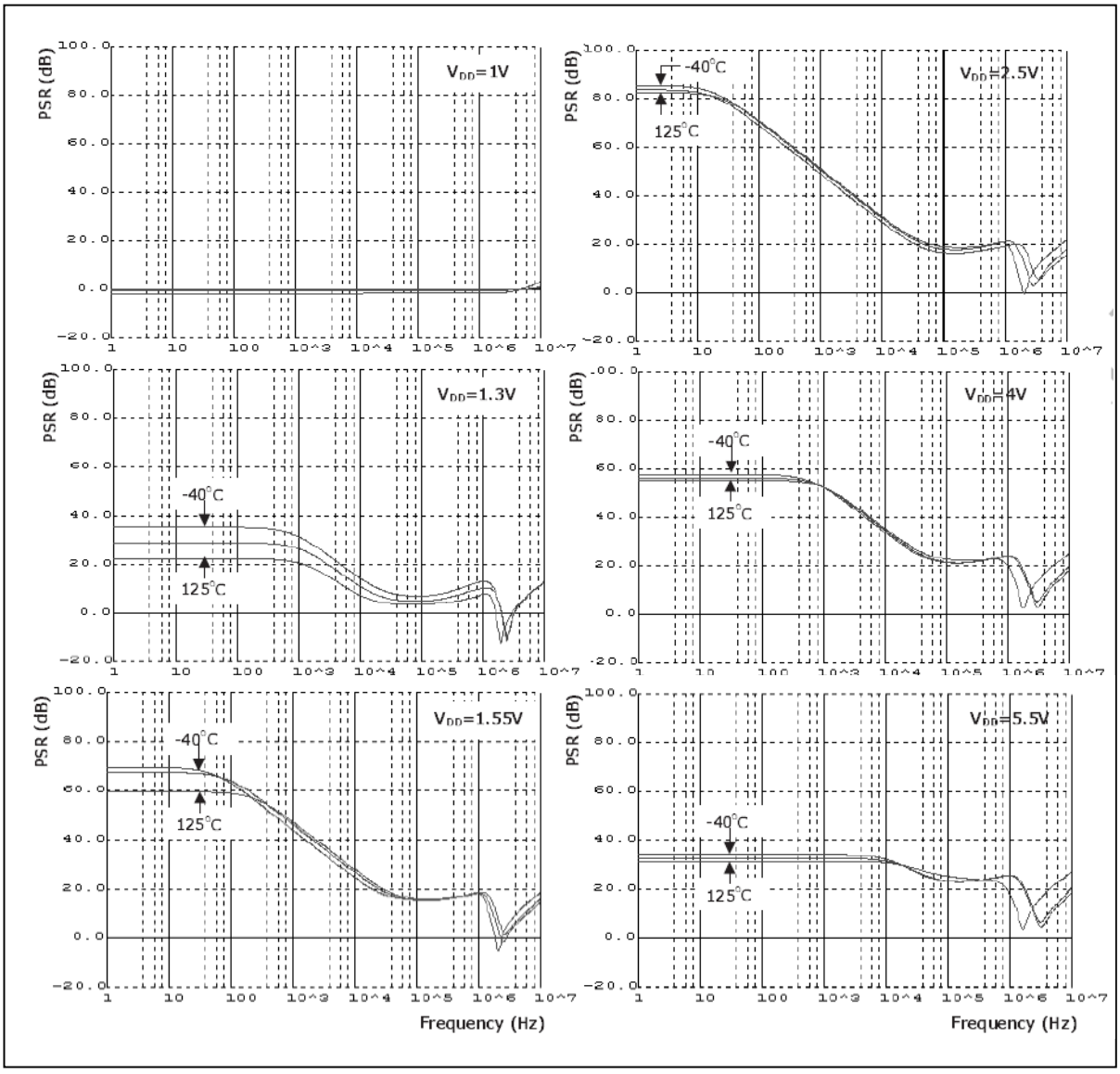

Figure 2.9. Pre-regulator PSR characteristics as a function of raw supply voltage V_{DD}

Simulated PSR performance of the pre-regulator is depicted in Figure 2.9 for the entire temperature range and six different values of V_{DD}. These simulations are conducted for 2.5 µA load current. PSR is approximately 0 dB for V_{DD}=1 V, as expected for the unregulated part of the pre-regulator transfer characteristic. At the lower end of V_{DD}=1.3 V of the regulated range, the 30 dB sub-spec is met with the exception of T=125 °C. What seriously falls short is the sub-spec for PSR at 10 kHz, whose target value is 20dB. Obviously the gain bandwidth (GBW) of the regulator is insufficient at his level of raw supply. DC PSR grows rapidly with V_{DD}, and reaches a peak over 80dB at 2.5 V. Although it declines for larger V_{DD}, the minimum 30 dB sub-spec is met all the way up to 5.5 V. PSR at 10 kHz is marginally below the sub-spec for V_{DD}=1.55 V but becomes compliant for larger values of V_{DD}.

2.4.2. Bandgap Reference Core Circuit

As mentioned previously, AMS C35B4C3 technology comes with four types of parasitic vertical PNP models. Q_1 and Q_3 are formed with these models and Q_2 is scaled by a factor of N=24 to minimize the spread of the resistors. In fact N can take values of 8, 24, 48 or even 80 since these integers can be used to realize common-centroid structures for better matching. However, as seen in equation (2.4), increasing the value of N further will not introduce a significant difference in $ln(N)$. Furthermore, an increasing N in the common-centroid structure comes with more errors since the separation of the devices increase [13].

Resistors of the core circuit are determined from (2.1) through (2.4) after allocating 375nA to I. All are high-resistivity poly resistors of TC_1=-750 ppm/°C and TC_2=3.82 ppm/°C. The target value of V_{BG} is set in the range 0.5 V to 0.6 V.

The OTA has a low-voltage folded-cascode topology with a rail-to-rail CMR. It is biased by a dedicated beta-multiplier, which also biases the cascode devices of the core circuit. Simulated PSR characteristics of the bandgap circuit employing a bjt with a β_F around 9 are shown in Figure 2.10 for T=-40 °C, T=40 °C, and T=125 °C.

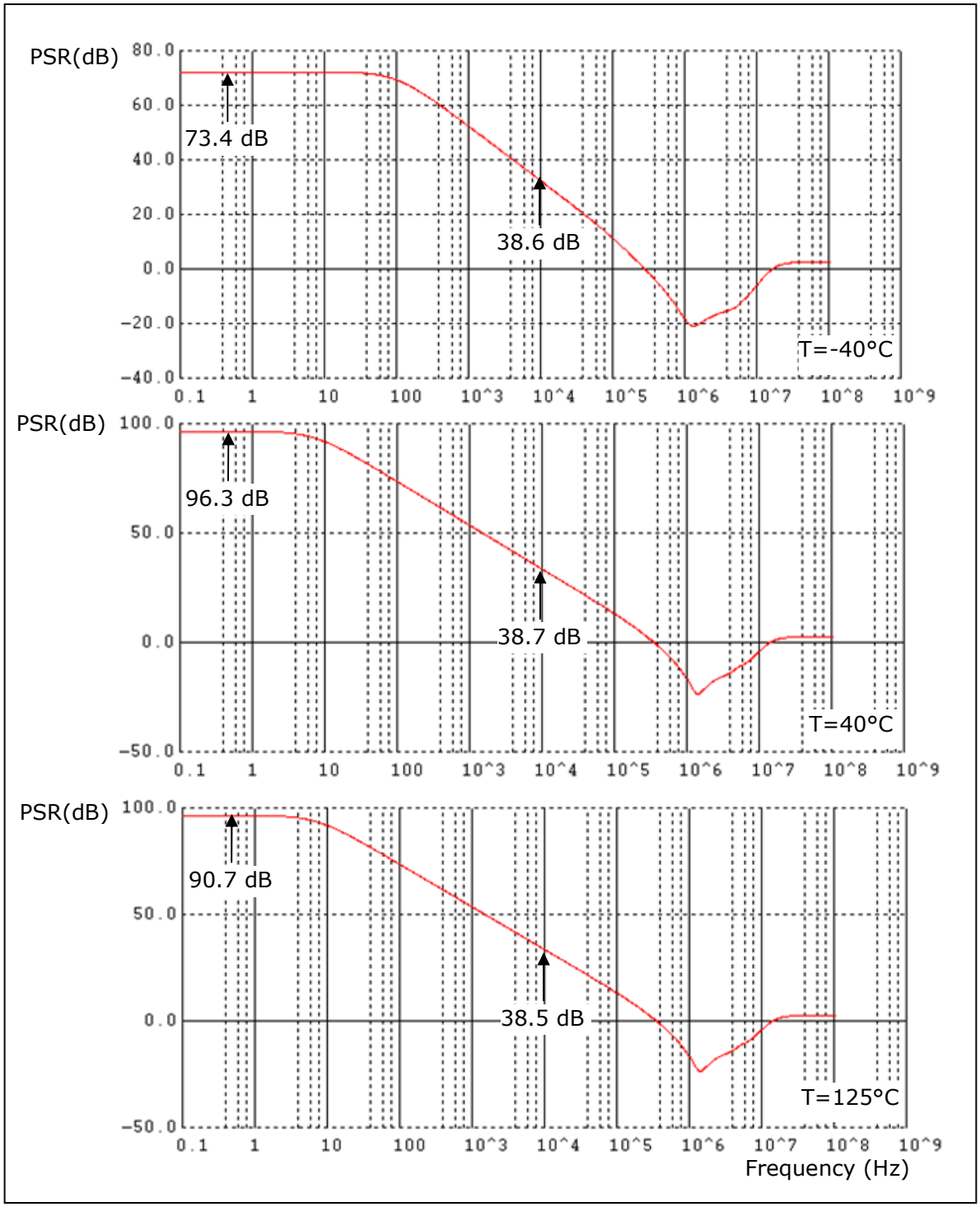

Figure 2.10. Bandgap core PSR characteristics as a function of temperature.

Table I: Simulated output voltage and current consumption of bandgap reference core circuit.

Temperature (°C)	**Output Voltage V_O (mV)**	**Current I_{RR} (µA)**
-40 °C	549.175	2.19
40 °C	550.615	2.65
125 °C	550.155	3.01

These simulations were conducted using an ideal voltage source for V_{RR}=1.2 V. However, the simulation results of the overall topology with each of the four bjt models are illustrated in the next chapter and detailed tables including the trimmed resistor values are given in Appendix C for further analysis.

The simulated output voltage V_O and current consumption I_{RR} of the bandgap core are given in Table I. Considering these together with the simulated performance of the pre-regulator, the overall BGR topology achieves a very satisfying PSR and low-current consumption resulting in low-power operation.

2.4.3. Start-up Circuits

The transient simulations performed on the overall topology revealed that the bandgap reference core was easily reaching the correct bias point without additional start-up circuits except the one for the pre-regulator. However, in order to prevent the circuit entering an undesired state during the operation we have added two start-up circuits to the bandgap reference core. The overall bandgap reference topology including the start-up circuitry is presented in Figure 2.11.

In addition to the pre-regulator start-up circuit, two start-up circuits one for the BGR core itself and another one for the core beta-multiplier current reference are designed. Initially, we wanted to use a single start-up circuit for both core OTA's biasing and for the core itself.

However, the beta-multiplier current reference is also biasing the cascode devices M_6/ M_7/M_8/M_9. Therefore, we had to use separate start-up circuits.

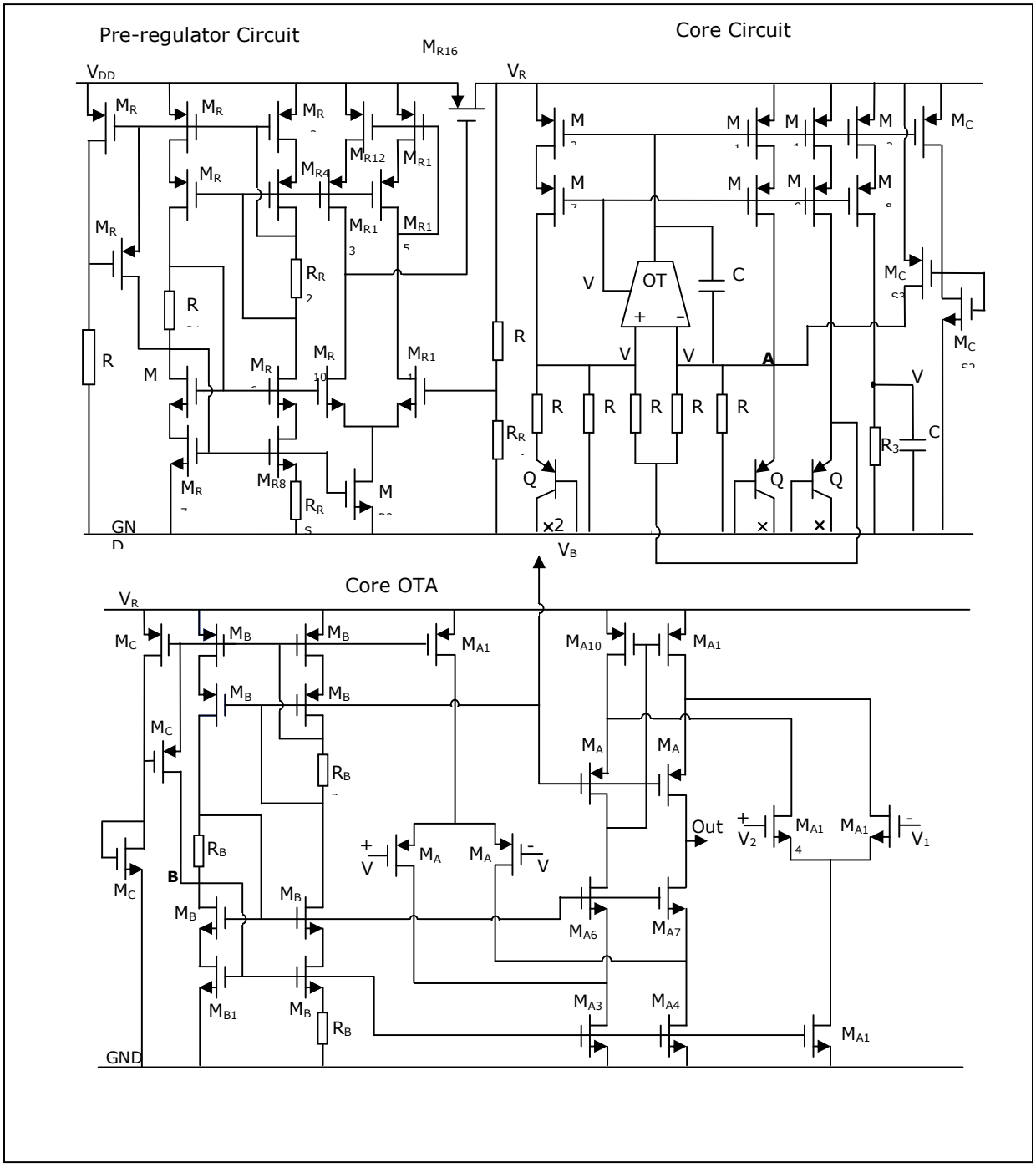

Figure 2.11. Overall bandgap voltage reference topology with start-up circuits included.

The gate of M_{CS1} is sensing the voltage at the common gates of the source devices $M_1/M_2/M_3/M_4$. When there is no current in the core circuit, the gates of $M_1/M_2/M_3/M_4$ are pulled high and the nodes at which the OTA's inputs are connected are pulled down. In this situation, the gate of M_{CS3} is pulled to ground, and it starts injecting current to node *A*. This causes V_1 to rise and OTA output voltage to fall, and thus force $M_1/M_2/M_3/M_4$ to conduct. Afterwards, M_{CS1} turns on and starts injecting current through M_{CS2}. The diode-connected M_{CS2}

with an aspect ratio being much smaller than 1 rises its gate-to-source voltage so that it raises the gate voltage of M_{CS3} up to V_{RR} thus turning off $M_{CS3.}$ M_{CB1}, on the other hand, is sensing the voltage at the gate of M_{B7}/M_{B8}. Similarly, when there is no current in the beta-multiplier circuit, the common gates of M_{B7}/M_{B8} are pulled high. In this case, M_{CB1} is off and M_{CB3} turns on injecting current to the circuit to node *B*. Then the beta-multiplier circuit starts and M_{CB1} starts conducting and the gate of M_{CB2} reaches up to V_{RR} thus turning M_{CB3} off.

2.4.4. Resistive Trimming Network

The temperature compensation of the bandgap reference circuit at first order and second order are performed via accurately setting the values of the resistors R_0, R_4 andR_5. The reason is that these resistors must meet a certain ratio with the resistor R_1 in order to cancel out the variation of the output voltage to a high extent in the specified wide temperature range. Therefore, we designed a trimmable resistive network for each of these resistors. The resistive network shown in Figure 2.12 has a fixed resistor R_i in series with an array of resistors of value *R,* 2*R*,4R, *8R* and 16*R*. The six terminals of this network are connected to external pins and with suitable external connections it is possible to change the values of the resistors R_0, R_4 and R_5 in a range of ± 15 % of their nominal values with a step size of 0.64 %. The R_i values for R_0 and $R_{4,5}$ are 378 kΩ and 855 kΩ while *R* values are 2.7 kΩ and 6.13 kΩ respectively.

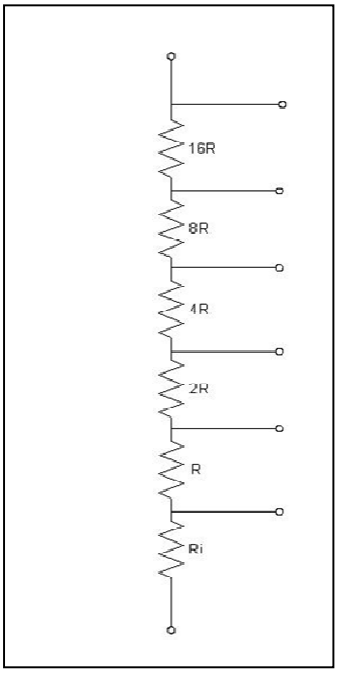

Figure 2.12. Resistive trimming network.

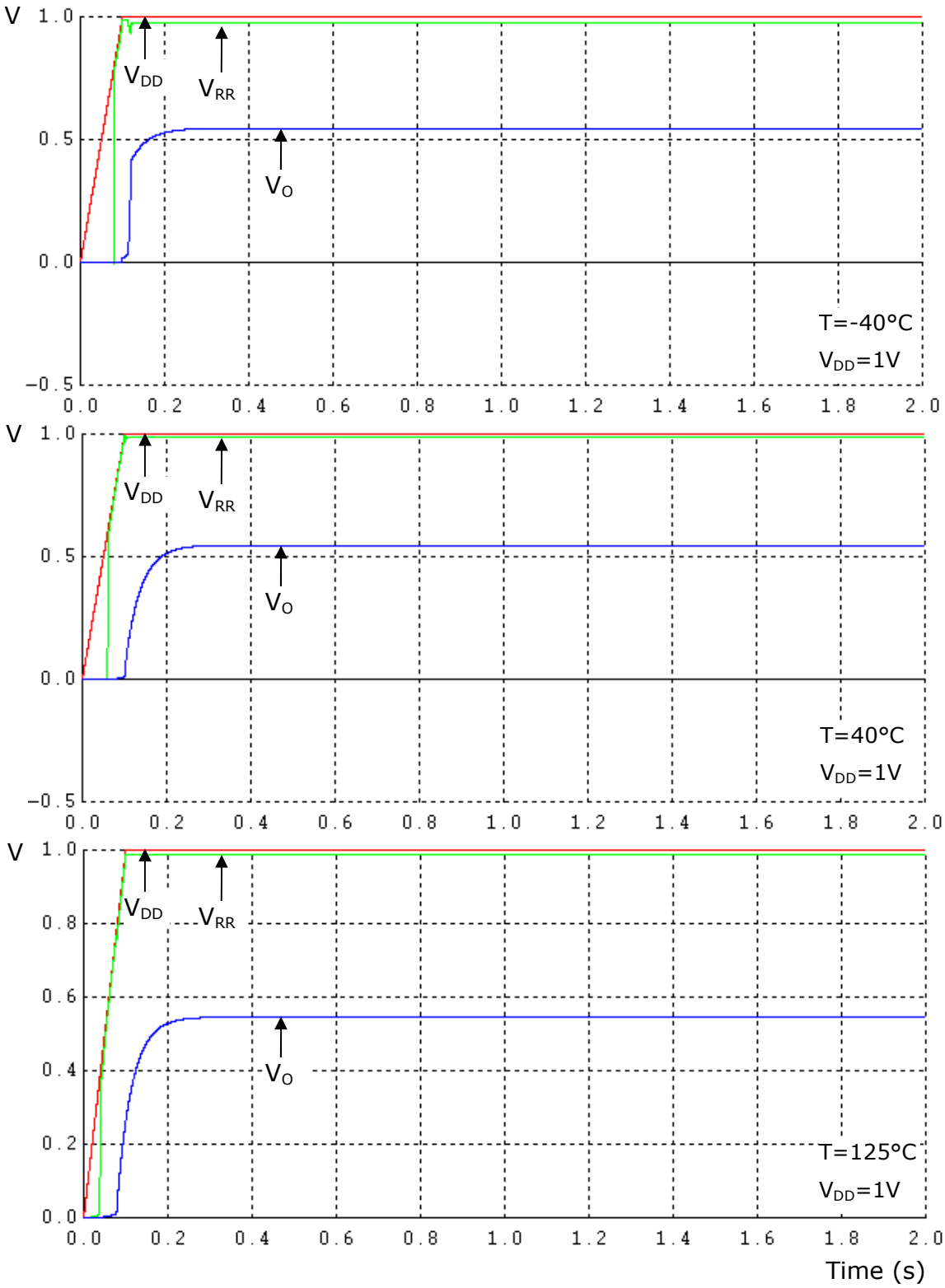

Figure 3.1. Waveforms of regulated supply voltage V_{RR} and the output voltage V_O in response to ramped supply voltage V_{DD}=1 V at T=-40 °C, 40 °C, and 125 °C.

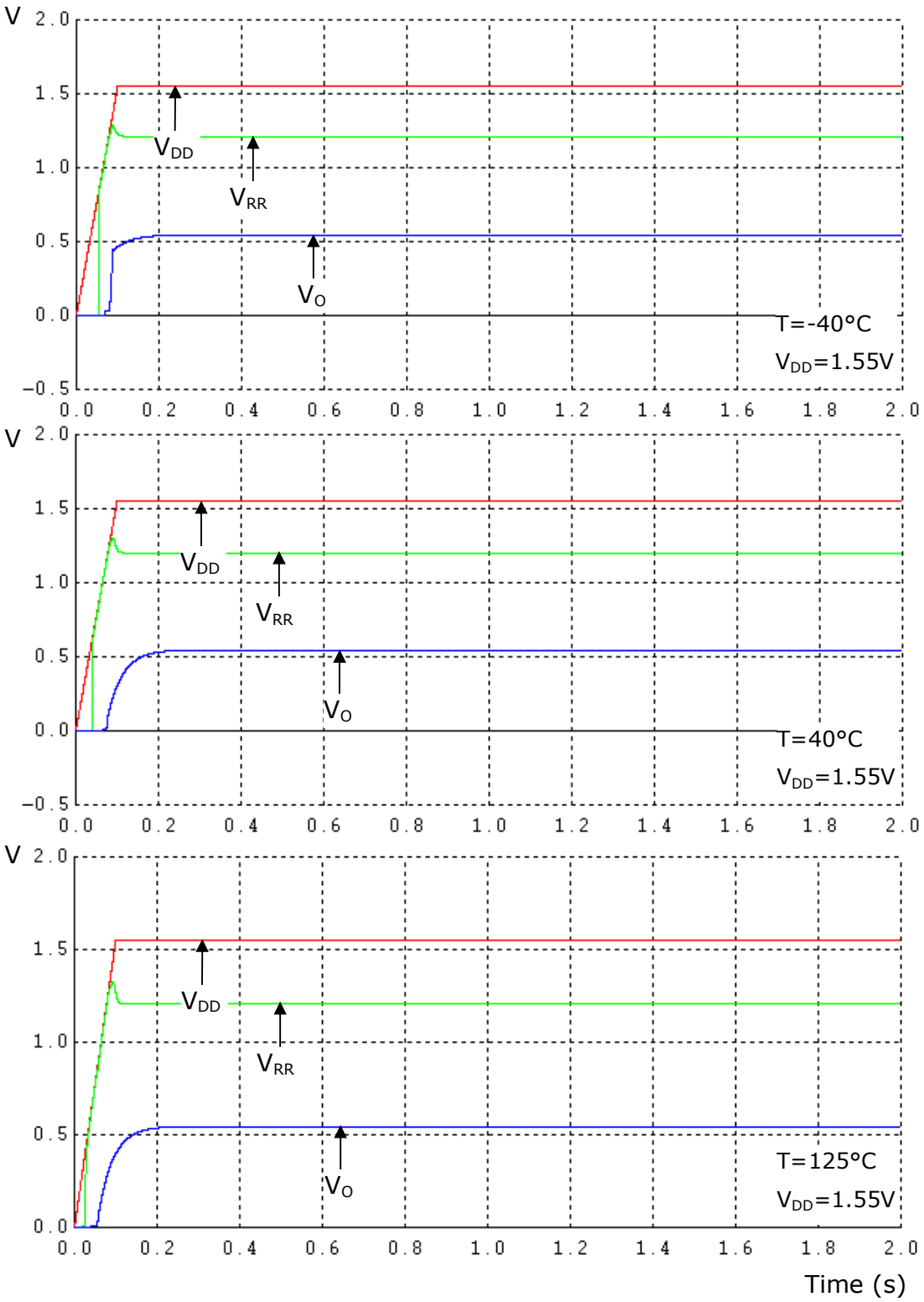

Figure 3.2. Waveforms of regulated supply voltage V_{RR} and the output voltage V_O in response to ramped supply voltage V_{DD}=1.55 V at T=-40 °C, 40 °C, and 125 °C.

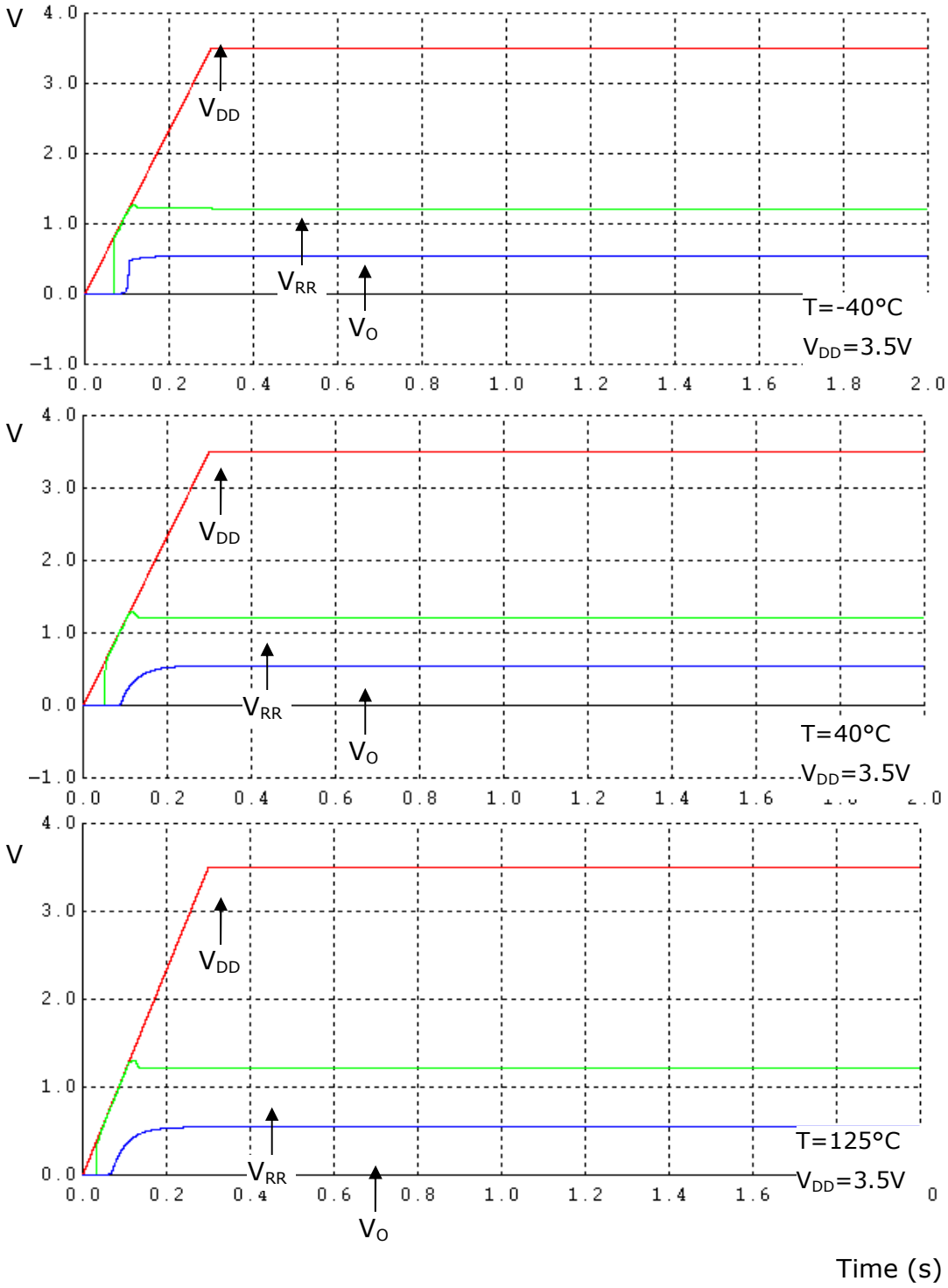

Figure 3.3. Waveforms of regulated supply voltage V_{RR} and the output voltage V_O in response to ramped supply voltage V_{DD}=3.5 V at T=-40 °C, 40 °C, and 125 °C.

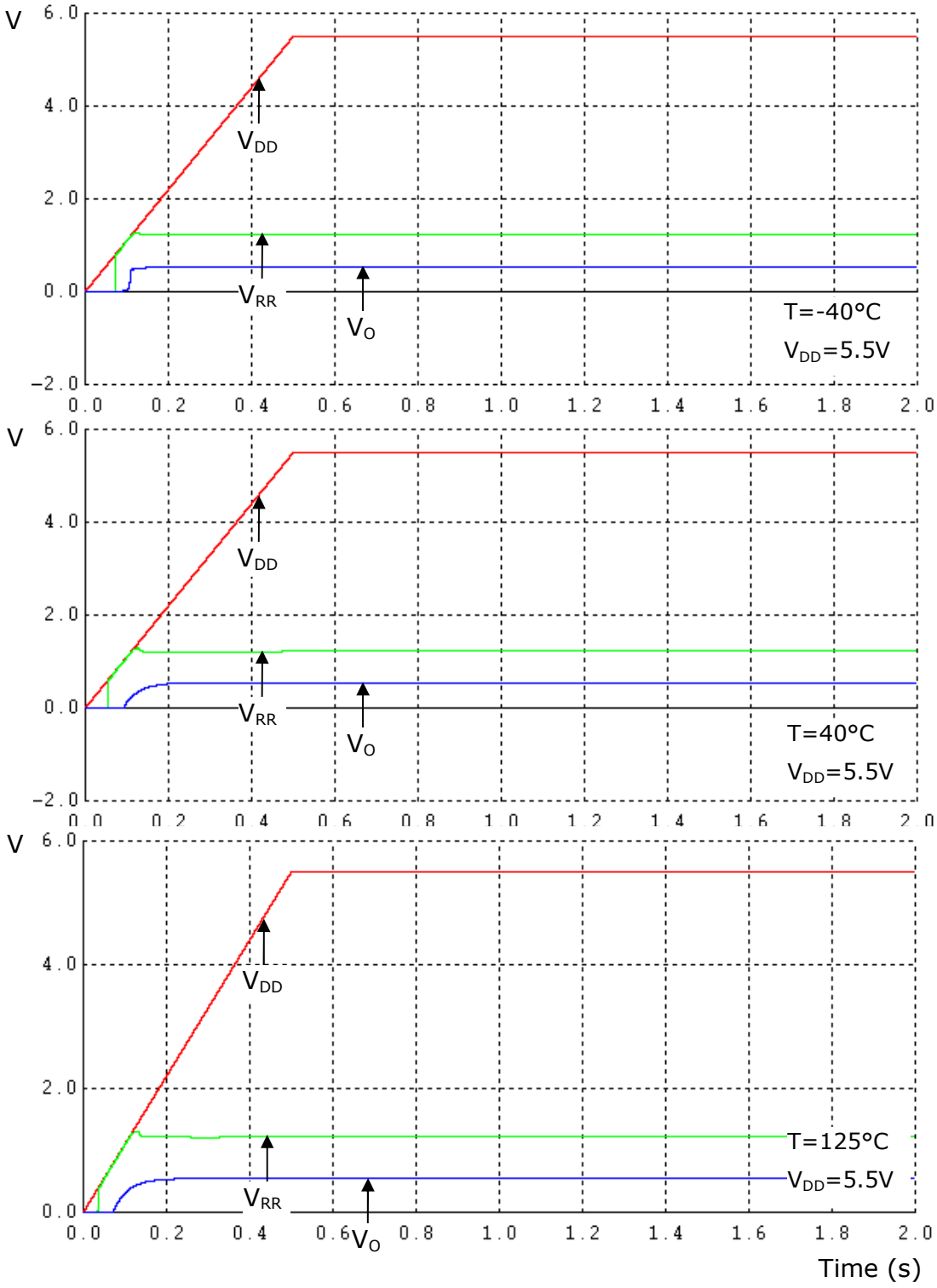

Figure 3.4. Waveforms of regulated supply voltage V_{RR} and the output voltage V_O in response to ramped supply voltage V_{DD}=5.5 V at T=-40 °C, 40 °C, and 125 °C.

3. VERIFICATION

The performance of the bandgap voltage reference topology of Figure 2.11 was verified through various types of simulations. Transient simulations were performed for verifying stability and start-up behavior. Operation-point simulations were performed for examining supply-current consumption, output voltage, and output voltage variation over temperature. AC simulations were conducted to measure the PSR performance of the circuit. Noise simulations were conducted measure the output noise. All simulations were run with BSIM3v3.2.4 typical model cards for the target technology.

3.1. Transient Behavior

Transient behavior is shown in Figure 3.1 through Figure 3.4 with the waveforms of V_{RR} and V_O obtained in response to ramping V_{DD} up from 0 V. The circuit remains stable for all four final levels of V_{DD} and all three temperatures (-40 °C, 40 °C, and 125 °C). The pre-regulator circuit starts up as V_{DD} approaches 0.7 V. Thereafter, V_{RR} tracks V_{DD} with a very small loss, and settles at 1.2 V for $V_{DD}\geq$1.3 V, as expected.

3.2. PSR Performance

PSR performance of the bandgap voltage reference circuit at dc and 10 kHz are illustrated in Figure 3.5 and Figure 3.6, respectively.

These simulations are performed with the four available bjt models in AMS 0.35 µm CMOS technology for four values of V_{DD} (1 V, 1.55 V, 3.5 V, 5.5 V) and repeated in a temperature range covering -50 °C to 180 °C. PSR values are read at DC and at 10 kHz. The detailed results at each temperature value are presented on the tables given in Appendix C. It should be noted that the fluctuations seen on the graphics presented in Figure 3.5, Figure 3.6, and the tables in Appendix C are due to convergence problems encountered in the simulations.

PSR results for V_{DD}=1 V which are illustrated in Figures 3.5 and 3.6 are satisfying although the pre-regulator circuit is not working at this supply. On the other hand, in the regulated range, the PSR performance both at DC and 10 kHz are somewhat magnificent. The reason for the decrease in the PSR performance in high supply levels approaching to 5.5 V is that the performance of the pre-regulator decreases at these levels as mentioned in the previous chapter.

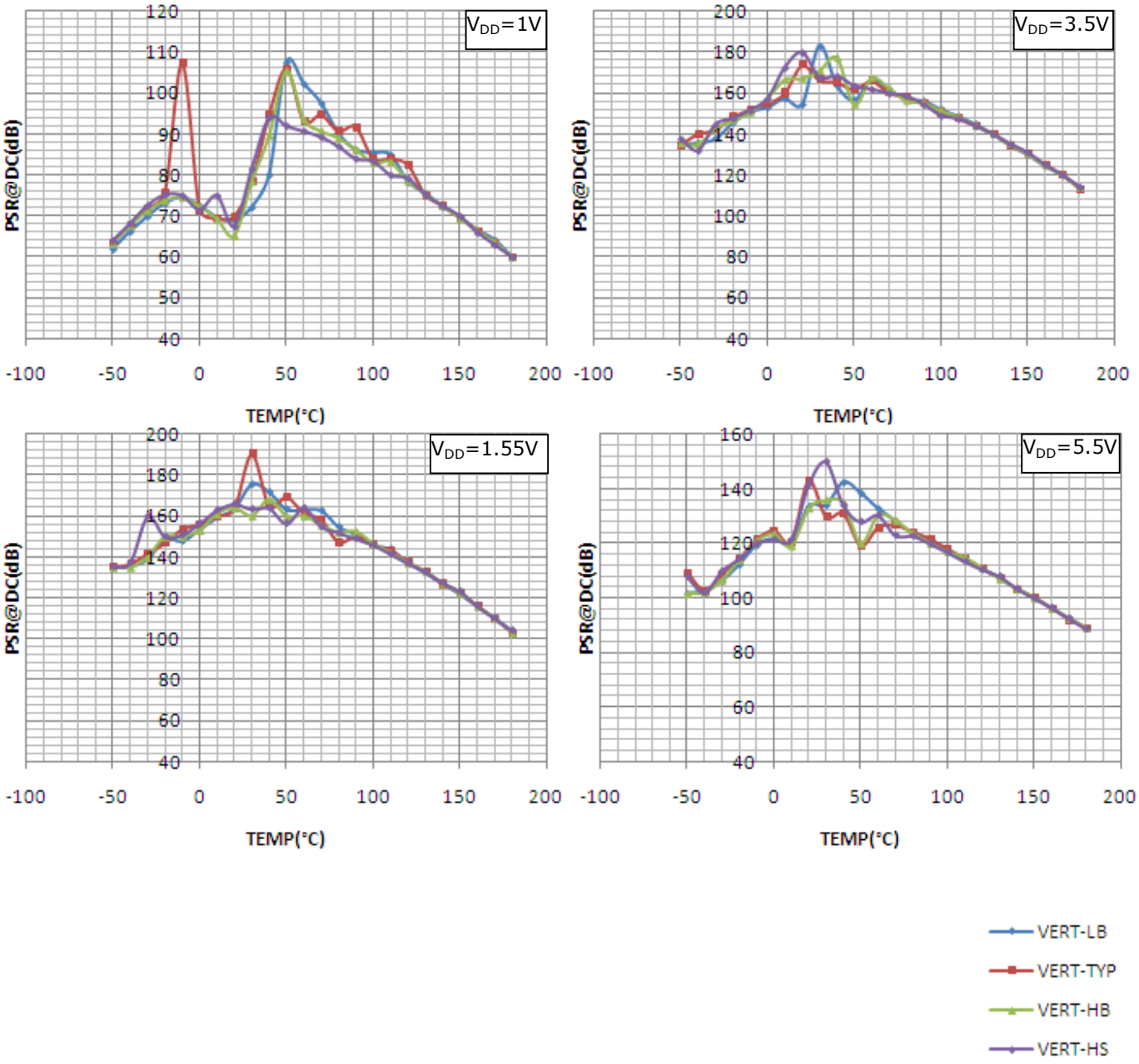

Figure 3.5. DC and low-frequency PSR performance of the proposed circuit realized with different bjt models available in AMS C35B4C3 CMOS technology

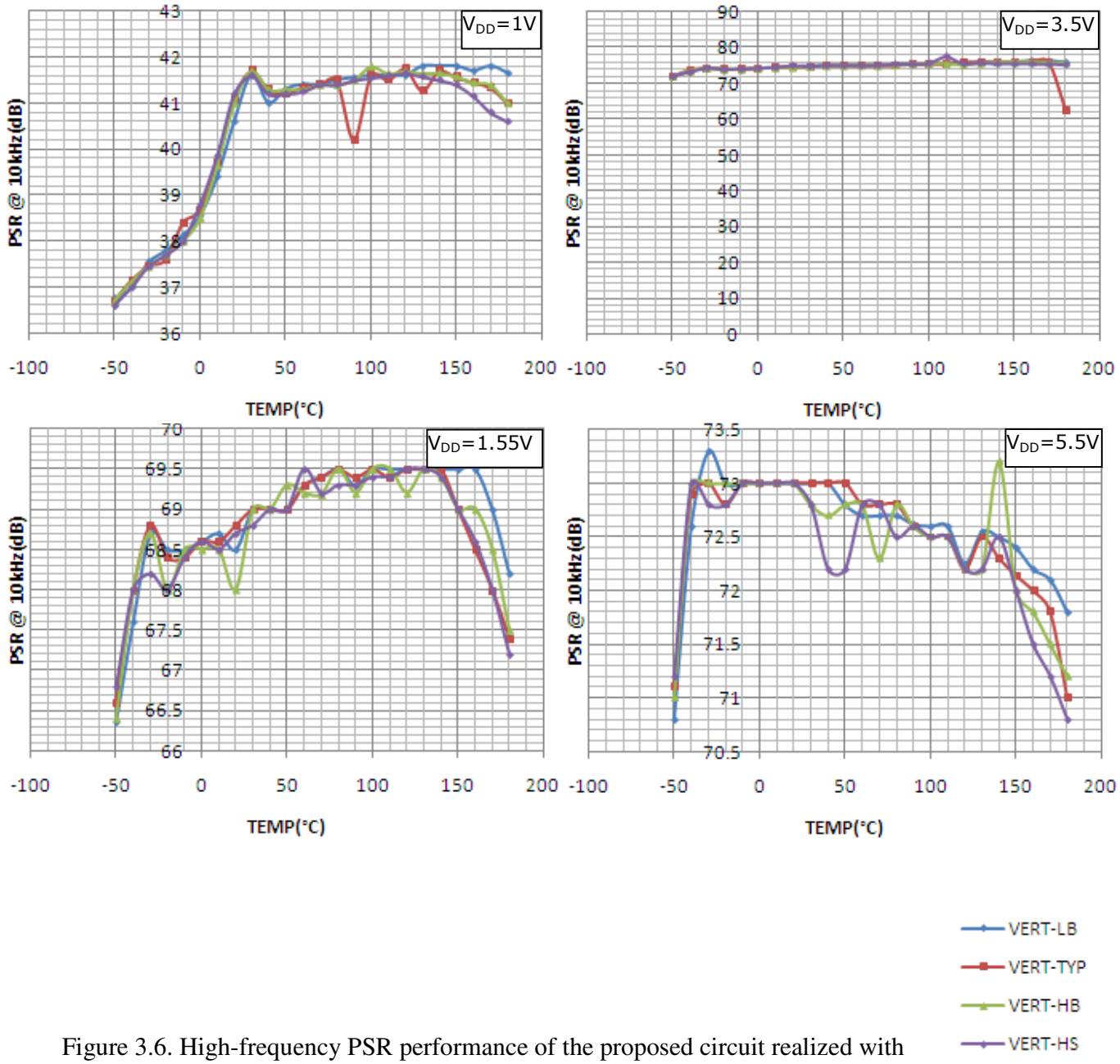

Figure 3.6. High-frequency PSR performance of the proposed circuit realized with different bjt models available in AMS C35B4C3 CMOS technology.

3.3. Operation-Point Simulations

Output voltage V_O, output voltage variation $\Delta V_O/V_O\ (T_0)\ (\%)$, and supply-current I_{DD} values are obtained with operation-point simulations are shown graphically in Figure 3.7, Figure 3.8, and Figure 3.9, respectively. Detailed data can be found on the tables provided in Appendix C. The values of the critical values of the resistors $R_0/R_{4,5}$ for proper compensation of the temperature dependence of the output voltage are also given on these tables for each bjt models of the given technology.

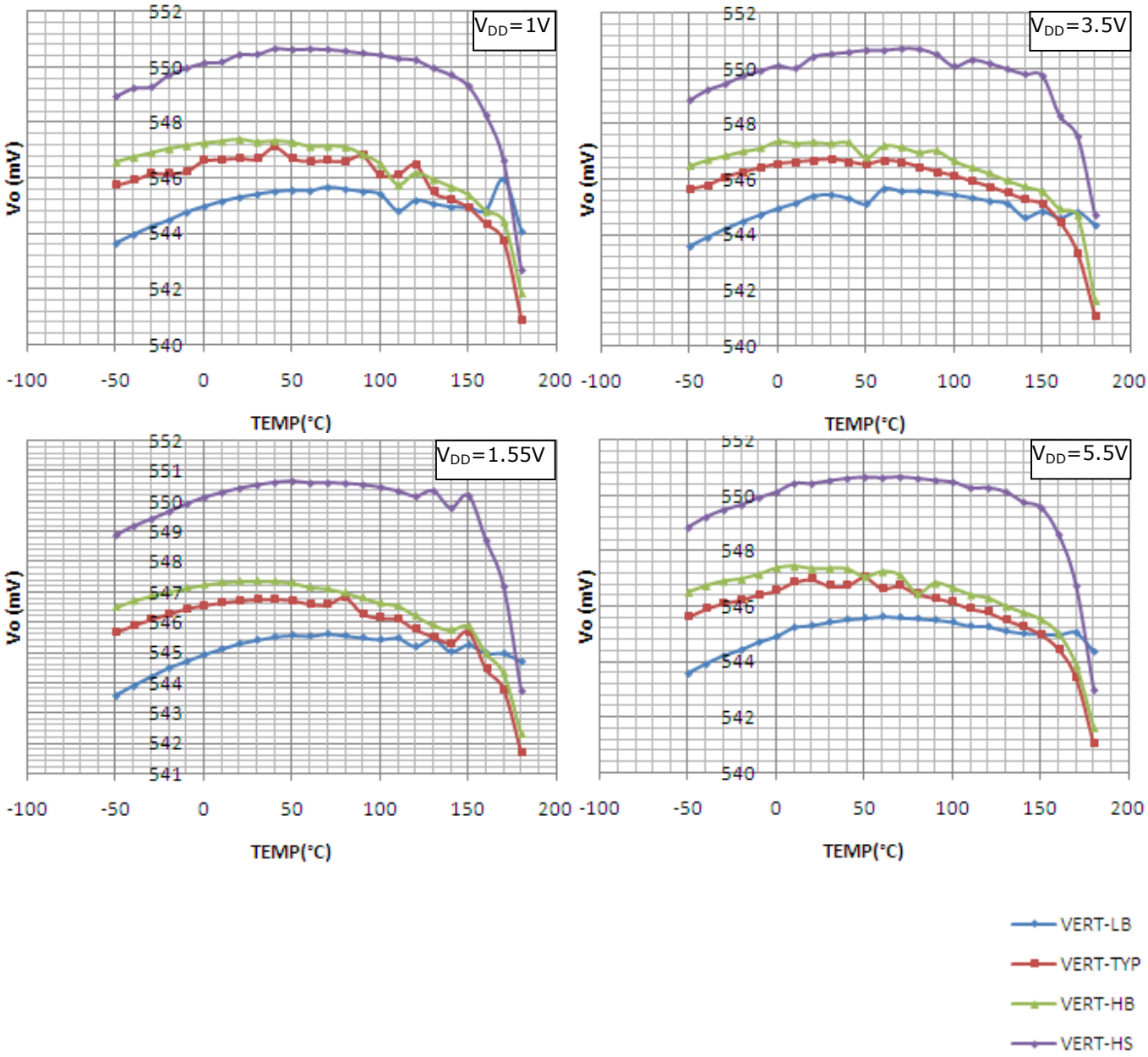

Figure 3.7. Output voltage V_O at four V_{DD} values and for four bjt models of AMS C35B4C3 technology.

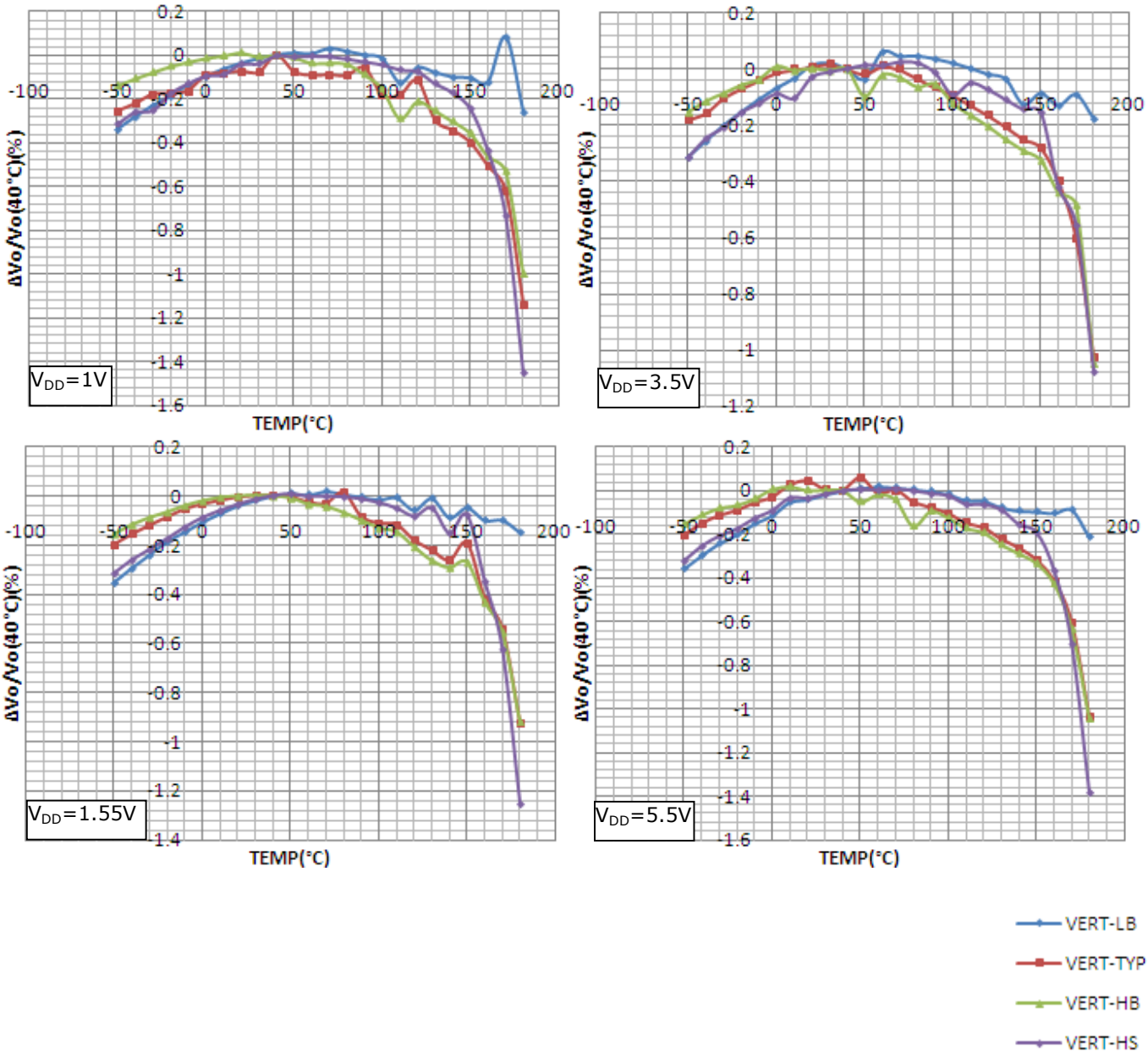

Figure 3.8. Output voltage variation $\Delta V_O/V_O\,(T_0)\,(\%)$ at four V_{DD} values and for four bjt models of AMS C35B4C3 technology

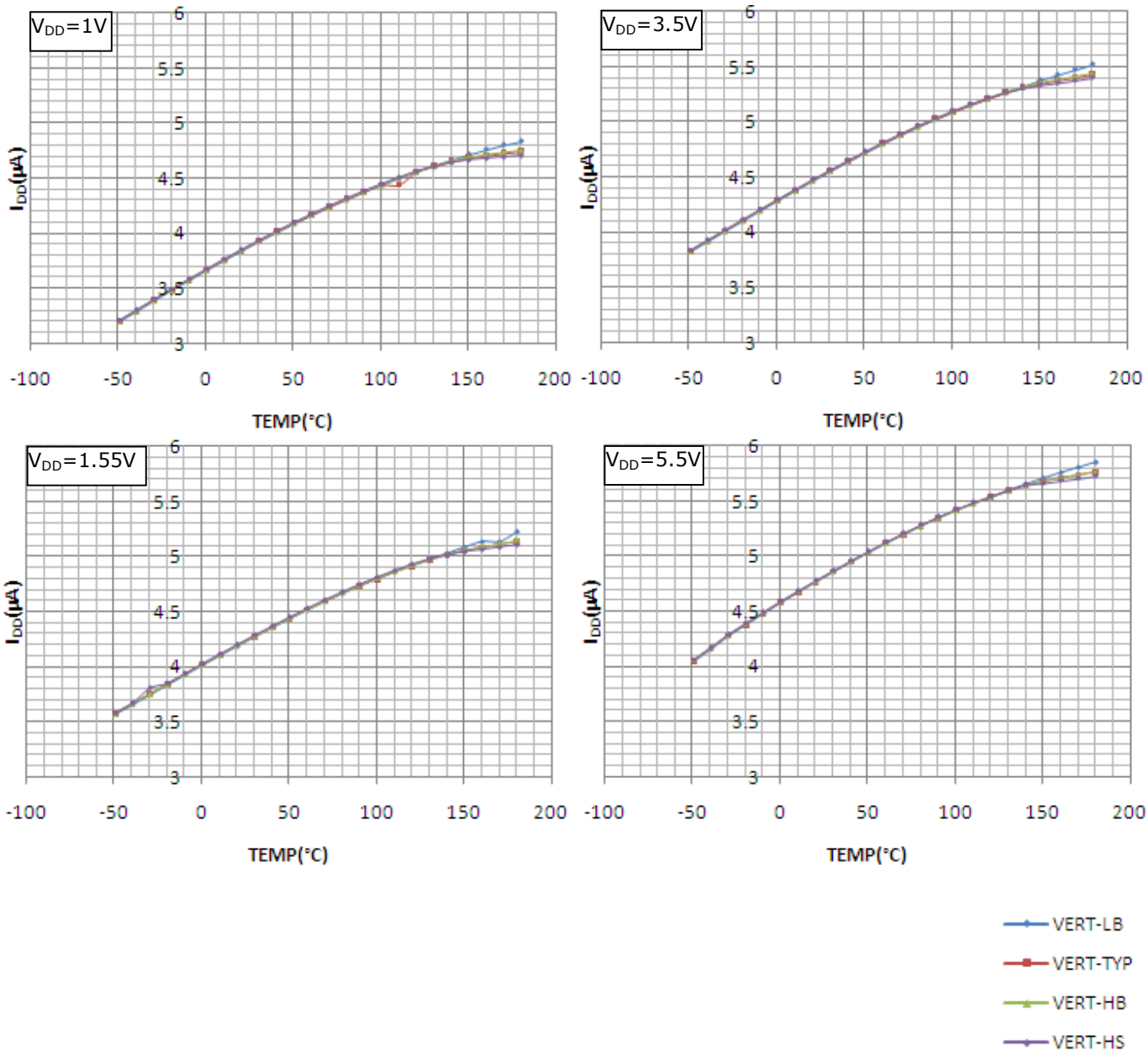

Figure 3.9. Current consumption I_{DD} of the overall bandgap voltage reference circuit at four supply levels and in the temperature range -50 °C to 180 °C

As can be seen from Figure 3.8 the relative variation of the output voltage is so perfect that it stays less than 0.29 % in the temperature range -40 °C to 125 °C and less than 1 % in the range -50 °C to 180 °C.

Total current consumption I_{DD} of the overall bandgap voltage reference circuit illustrated in Figure 3.9 proves the low-power operation over the wide supply range thanks to the beta-multiplier circuits employed in the topology. Indirect dependence of the current consumption

on V_{DD} is more pronounced at higher levels of supply voltage. On the other hand, the main increase in the current consumption is seen over the wide temperature range of operation because of the PTAT characteristic of the beta-multiplier current reference. The current consumption of the reference circuit can be appreciated a lot since even for the highest supply value 5.5 V it slightly exceeds 5 µA at 125 °C and less than 6 µA at 180 °C.

3.4. Noise Analysis

Initial noise simulations performed on the reference topology indicated a thermal-noise dominated total output noise of 489 µVrms for a 100 kHz bandwidth and T=125 °C. In addition to this, output noise stays above 400 µVrms in a temperature range -40 °C to 125 °C. This result is actually inevitable under such low current levels with such high resistance values adopted in the circuit. To prove the point, suppose that the highest supply current I_{DD} value 5 µA is used in its entirety just to generate a reference output voltage of 400 mV. This combination would result in a relatively small value for R_3 (80 kΩ), hence the smallest noise voltage. For a 100 kHz bandwidth the noise of this single resistor alone would be 13.2 µVrms at T=125 °C. In the present design, R_3 is on the order of mega-ohms, thus generating approximately 57 µVrms alone. As a matter of fact, the noise-power density of a second-order compensated bandgap reference with a given reference voltage can only be influenced by the designer via manipulating the current consumption.

For a given current consumption, the signal-to-noise ratio is independent of the value of the reference voltage and the size of the transistors used does not affect the noise level [14]. It is important to note that unless the output is loaded with significant capacitance, total noise within the true bandwidth is considerably large. This is due to the fact that noise bandwidth is actually determined by the large gain-bandwidth product (2.3 MHz) of the OTA needed to provide the high PSR specifications. Therefore, in order to improve the noise performance, the output of the reference circuit is loaded with a capacitance C_L of 25 pF as illustrated in Figure 2.11 which also improved the PSR performance at high-frequencies as can be seen in Figure 3.6. This capacitance further reduces the true bandwidth below 100 kHz mark and results in a total output noise no more than 230 µVrms over the temperature range -40 °C to 125 °C.

The graphical illustration of the output noise performance of the bandgap reference circuit is presented in Figure 3.10 at four supply levels and for four bjt models over the temperature range -50 °C to 180 °C. Detailed results can be found on the tables presented in Appendix C.

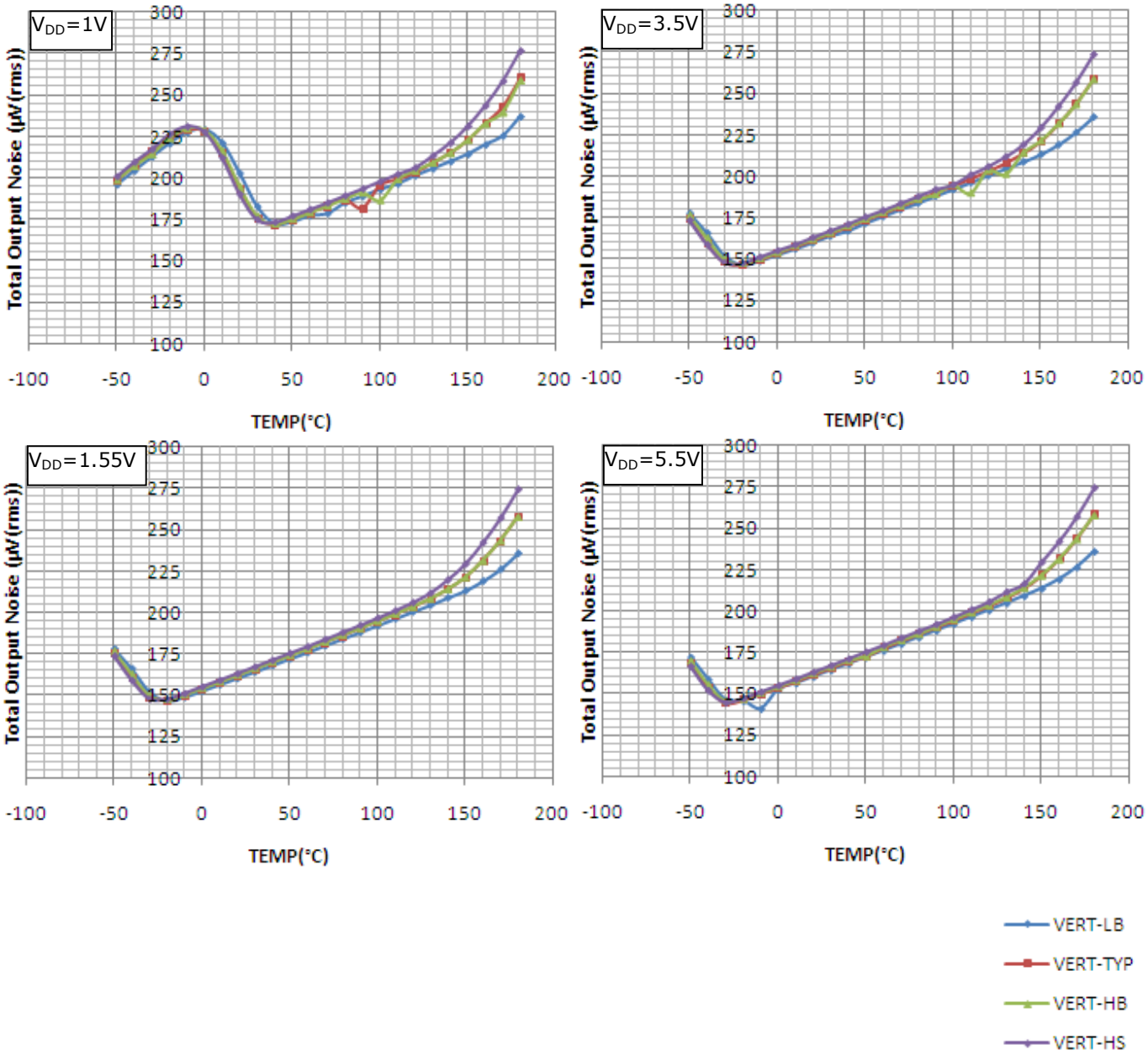

Figure 3.10. Total output noise of the proposed bandgap reference at four V_{DD} values and for four bjt models over the temperature range -50 °C to 180 °C

4. CONCLUSIONS AND COMPARISONS

Simulations performed on the proposed bandgap voltage reference circuit revealed that all of the target specifications are met successfully. The proposed circuit is capable of generating a sub-1V reference output voltage around 550 mV and operating in a wide range of supply voltages and temperatures from 1 V to 5.5 V and -40 °C to 125 °C, respectively.

The variation of the reference output voltage with temperature is less than 0.29 % and calculated TC is 10 ppm/°C which is fantastic for the wide temperature range of operation. Of course, this is the result of the strong curvature-correction mechanism employed in the circuit. As a result of the incorporated pre-regulator circuit; the variation of the output voltage is less than 0.086 mV/V throughout the entire supply voltage range. One radical contribution of the pre-regulator circuit to the bandgap voltage reference manifests itself in the PSR performance in the regulated range of $V_{DD}\geq$1.3 V. Examining the graphical illustrations in the verification chapter and the tables of Appendix C, it is seen that at 1 V supply level the circuit achieves a dc PSR of more than 80 dB and at 10 kHz more than 37 dB. Moreover, in the regulated range PSR at dc and low-frequencies stays well above 100 dB over the entire supply voltage and temperature range reaching a maximum of 170 dB. At high-frequencies PSR performance is again highly satisfying since it is above 37 dB and 67 dB for V_{DD}=1 V and $V_{DD}\geq$ 1.3V, respectively.

Another achievement of the proposed circuit is on its power consumption. Although the overall circuit incorporates many circuit blocks, weak inversion operation limits the total current consumption of the circuit which is no more than 5.53 µA at the highest supply voltage and temperature value of 5.5 V and 125 °C, respectively. This situation certainly widens the use of the proposed circuit in battery operated systems which require low-power consumption. Table II is a brief comparison of the proposed bandgap voltage reference with the recently reported references in literature. Examining the table reveals that the proposed circuit reflects its huge potential in finding use of today's high-performance applications.

Table II. Comparison of the proposed circuit with recently reported studies.

COMPARISON CHART	**This Work**	**Becker-Gomez *et al.*[15]**	**Pan *et al.* [16]**	**De Vita *et al.* [17]**	**Wang *et al.* [18]**	**De Vita *et al.* [19]**	**Leung *et al.* [20]**
Technology	0.35 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	0.35 µm CMOS	0.6 µm BICMOS	0.35 µm CMOS	0.6 µm CMOS
Supply Voltage	1 to 5.5 V	1.1 to 1.8 V	0.98 to 1.5 V	1.5 to 4.3 V	2.7, 4, and 5.5 V	0.9 to 4 V	0.98 to 1.5 V
Reference Voltage	546.74 mV	1.012 V	500 mV	670 mV	1.25 V	891 mV	603 mV
Supply Current	<5.5 µA	<14 µA	N/A	<0.11 µA	N/A	<0.055 µA	<18 µA
Temperature Range	-40 to 125 °C	0 to 100 °C	-40 to 85 °C	0 to 80 °C	-25 to 110 °C	0 to 80 °C	0 to 100 °C
Temperature Coefficient (TC)	10 ppm/°C	4 ppm/°C	7.04 ppm/°C	10 ppm/°C	6.5 ppm/°C	12 ppm/°C	15 ppm/°C
Line Regulation	0.086 mV/V	N/A	N/A	0.27 %/V	N/A	1.6 mV/V	±2.2 mV
PSR @DC and Low-Frequency	>80 dB for 1 V >135 dB for *VDD*>1.3 V	75 dB	120 dB	47 dB	>100 dB	59 dB	44 dB
PSR @DC at High-Frequencies	> 41 dB for1 V >69 dB for *VDD*>1.3 V	23 dB	N/A	40 dB	N/A	52 dB	17 dB

APPENDIX A: DETAILED ANALYSIS OF THE BANDGAP REFERENCE CORE TOPOLOGY AND TEMPERATURE COMPENSATION SCHEME

A.1. Analysis without Curvature-Correction (Secondary Effects Included)

In this appendix provides a detailed analysis of the current mode circuit proposed by [7] is presented. The curvature correction network proposed by [11] will be inserted later in this appendix and the curvature-correction mechanism starting with Tvidis' V_{BE} vs T expression [21] is also examined in detail and resulting design equations are derived. Entire derivations are performed by Dr. Cilingiroglu.

The circuit to be used for the analysis is given in Figure A1. In the circuit analysis, the secondary effects such as the offset voltage at the input of the OTA (V_{OS}) and mismatches in resistor values (ΔR), mirrored currents (ΔI), and bjt forward current-gains (β_F) are all included so that they can be minimized during the design process.

Emitter currents I_3 and I_4 of the transistors Q_1 and Q_2 respectively can be written as

$$I_3 = \frac{1+\beta_{F1}}{\beta_{F1}} I_{S1} e \frac{q}{kT} V_1 \tag{A.1}$$

$$I_4 = \frac{1+\beta_{F2}}{\beta_{F2}} I_{S2} e \frac{q}{kT} V_3 \tag{A.2}$$

Emitter-base voltages V_3 of Q_2 and V_1 of Q_1 which is equal to V_2 with an offset voltage V_{OS} respectively are written as

$$V_3 = V_2 - R_0 I_4 \tag{A.3}$$

$$V_2 = V_1 + V_{OS} \tag{A.4}$$

Substituting equation A4 in A3 and then A3 in A2 yields I_4 as

$$I_4 = \frac{1+\beta_{F2}}{\beta_{F2}} I_{S2} e \frac{q}{kT} \left(V_1 + V_{OS} - R_0 I_4\right) \tag{A.5}$$

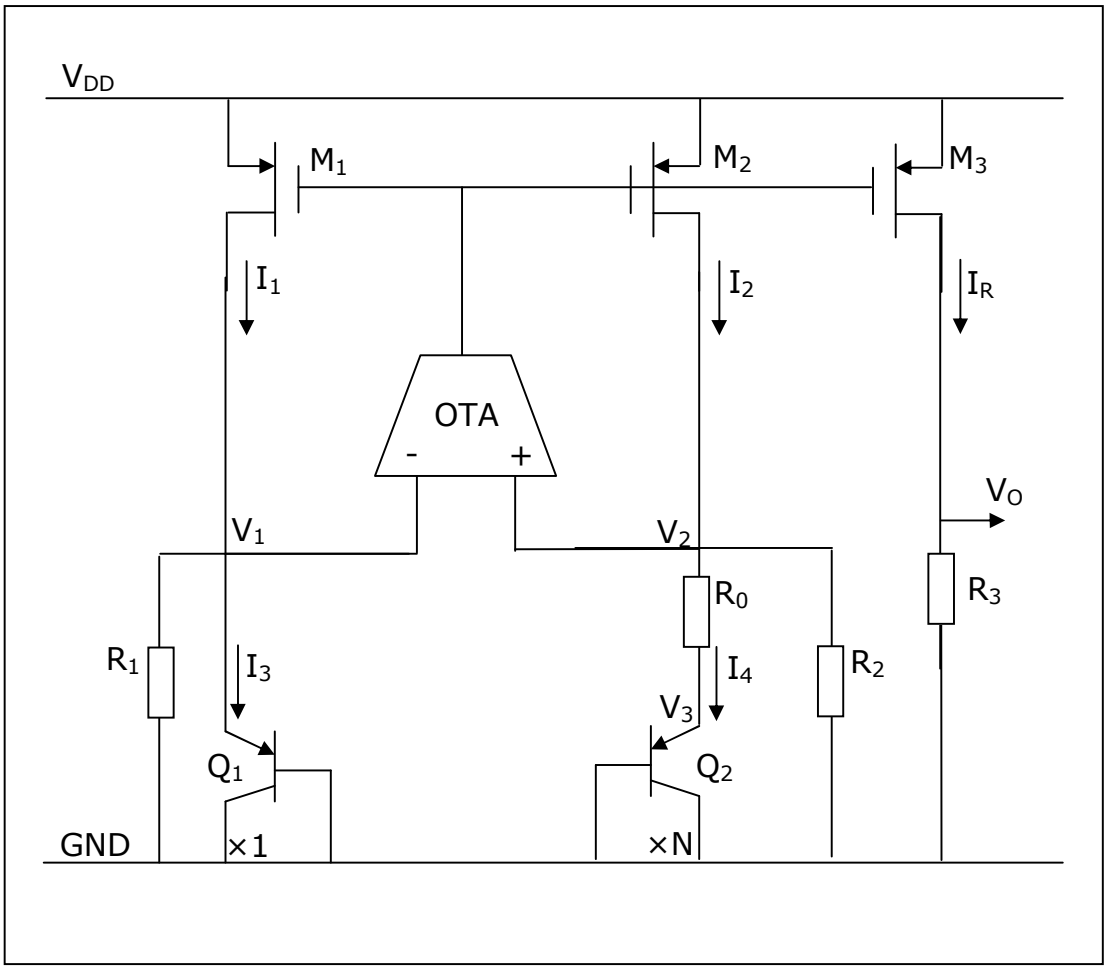

Figure A.1. Bandgap voltage reference core circuit without curvature-correction network

Currents I_1 and I_2 sourced to the bandgap core by transistors M_1/M_2 are given as

$$I_1 = I_3 + \frac{V_1}{R_1} \tag{A.6}$$

$$I_2 = I_4 + \frac{V_1 + V_{OS}}{R_2} \tag{A.7}$$

Substituting equation A1 in A6, I_1 is rewritten as

$$I_1 = \frac{1+\beta_{F1}}{\beta_{F1}} I_{S1} e^{\frac{q}{kT}V_1} + \frac{V_1}{R_1} \tag{A.8}$$

Substituting equation A5 in A7 I_2 becomes

$$I_2 = \frac{1+\beta_{F2}}{\beta_{F2}} I_{S2} e^{\frac{q}{kT}(V_1+V_{OS}-R_0 I_4)} + \frac{V_1+V_{OS}}{R_2} \tag{A.9}$$

Since M_1 and M_2 are matched devices these currents can be equated to each other with assuming a current-mismatch of ΔI_1 as

$$I_2 = I_1 + \Delta I_1 \tag{A.10}$$

Using equation A10 in A9 yields

$$I_1 = \frac{1+\beta_{F2}}{\beta_{F2}} I_{S2} e^{\frac{q}{kT}(V_1+V_{OS}-R_0 I_4)} + \frac{V_1+V_{OS}}{R_2} - \Delta I_1 \tag{A.11}$$

Via equating A8 to A11 the following relation is obtained

$$I_1 = \frac{1+\beta_{F1}}{\beta_{F1}} I_{S1} e^{\frac{q}{kT}V_1} + \frac{V_1}{R_1} = \frac{1+\beta_{F2}}{\beta_{F2}} I_{S2} e^{\frac{q}{kT}(V_1+V_{OS}-R_0 I_4)} + \frac{V_1+V_{OS}}{R_2} - \Delta I_1 \tag{A.12}$$

Forward current gains β_{F1}/β_{F2} of the transistors Q_1/Q_2 are equated to each other with a possible beta-mismatch of $\Delta\beta_F$ as

$$\beta_{F2} = \beta_{F1} + \Delta\beta_F$$

and the relation between their saturation current densities I_{S1}/I_{S2} can be expressed as

$$I_{S2} = N I_{S1}$$

In addition to these relations, CTAT current generating resistors R_1 and R_2 are equated to each other again with a possible resistor-mismatch of ΔR as

$$R_2 = R_1 + \Delta R$$

The relationship between forward-beta values can be further expressed as

$$\frac{1+\beta_{F2}}{\beta_{F2}} = \frac{1+\beta_{F1}+\Delta\beta_F}{\beta_{F1}+\Delta\beta_F} = \frac{1+\beta_{F1}}{\beta_{F1}} + \frac{\Delta\beta_F}{\beta_{F1}}$$

and the latter relationship together with all the former ones are employed in the following equality of the current I_1 and I_2 as

$$\frac{1+\beta_{F1}}{\beta_{F1}} I_{S1} e^{\frac{q}{kT}V_1} + \frac{V_1}{R_1} = \left(\frac{1+\beta_{F1}}{\beta_{F1}} + \frac{\Delta\beta_F}{\beta_{F1}}\right) N I_{S1} e^{\frac{q}{kT}V_1} e^{\frac{q}{kT}(V_{OS}-R_0 I_4)} + \frac{V_1+V_{OS}}{R_1+\Delta R} - \Delta I_1$$

After this point, the current I_2 is extracted from this relationship through the following steps:

$$e^{\frac{q}{kT}(V_{OS}-R_0 I_4)} = \frac{\frac{1+\beta_{F1}}{\beta_{F1}} I_{S1} e^{\frac{q}{kT}V_1} - \frac{V_{OS}}{R_1} + \frac{V_1}{R_1}\frac{\Delta R}{R_1} - \Delta I_1}{\left(\frac{1+\beta_{F1}}{\beta_{F1}} + \frac{\Delta\beta_F}{\beta_{F1}}\right) N I_{S1} e^{\frac{q}{kT}V_1}}$$

$$V_{OS} - R_0 I_4 = \frac{kT}{q}\left[\frac{1}{N}\left(1 - \frac{\Delta\beta_F}{1+\beta_{F1}} + \frac{\frac{V_1}{R_1}\frac{\Delta R}{R_1} + \Delta I_1 - \frac{V_{OS}}{R_1}}{I_3}\right)\right]$$

Using equation A7 for I_4 in the latter equation and solving for I_2 yields

$$I_2 = \frac{V_1}{R_2} + \frac{V_{OS}}{R_0 \parallel R_2}\frac{1}{R_0}\frac{kT}{q}\left(\frac{N}{1 - \frac{\Delta\beta_F}{1+\beta_{F1}} + \frac{\frac{V_1}{R_1}\frac{\Delta R}{R_1} + \Delta I_1 - \frac{V_{OS}}{R_1}}{I_3}}\right)$$

The current I_2 is further mirrored by M_3 onto R_3 and the reference voltage V_O is formulated as

$$V_O = I_2 R_3$$

$$V_O = \frac{R_3}{R_2}\left[V_1 + \frac{R_2}{R_0}\frac{kT}{q}\ln\frac{N}{1+\Delta} + \left(1+\frac{R_2}{R_0}\right)V_{OS} \right]$$

where Δ given by A13 and V_{OS} are the secondary effect terms that should be minimized as much as possible by electrical and physical design techniques.

$$\Delta = \frac{\frac{V_1}{R_1}\frac{\Delta R}{R_1} + \Delta I_1 - \frac{V_{OS}}{R_1}}{I_3} - \frac{\Delta\beta_F}{1+\beta_{F1}} \qquad \text{(A.13)}$$

A.2. Tsividis' V_{BE} vs. T Expression

In order to compensate the output voltage of the bandgap reference circuit the temperature dependency of the base-emitter voltage of a bjt should be well understood. Tsividis [21] performed a detailed analysis for predicting the temperature behavior of the I_C-

V_{BE} characteristics of bjts. This analysis is repeated to derive a relationship of the emitter voltage represented with V of the diode-connected parasitic vertical PNP transistor used in the proposed circuit as a function of temperature T. Figure A.2 illustrates a diode-connected PNP transistor with an emitter current I flowing through it. Emitter current I is given as

$$I = \frac{1+\beta_F}{\beta_F} I_S e^{\frac{q}{kT}V}$$

and the emitter voltage V is extracted from this relation as

$$V = \frac{kT}{q}\ln\left(\frac{\beta_F}{1+\beta_F}\frac{I}{I_S}\right)$$

Reverse saturation current I_S is expressed as

$$I_S = \frac{A_q}{G_b} n_i^2 \frac{kT}{q}\mu_p$$

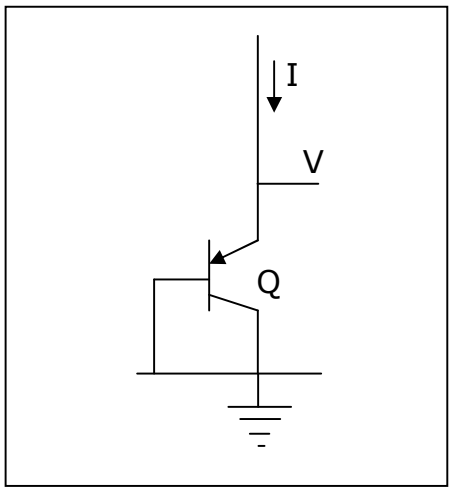

Figure A.2. Diode-connected PNP transistor

expanding intrinsic carrier concentration n_i in the latter expression I_S becomes

$$I_S = M\frac{kT}{q}\mu_p T^3 e^{\frac{-E_g(T)}{kT}}$$

Where

$$M = \frac{A_q}{G_b}C^2$$

Assuming $\frac{\beta_F}{1+\beta_F} = 1$ and independent of temperature, the variation of V with respect to the temperature can be derived via writing it for a reference temperature T_0 and a varying temperature T and taking the difference as follows

$$V(T) = \frac{kT}{q}\ln\frac{I(T)e^{\frac{E_g(T)}{kT}}}{M\frac{kT}{q}\mu_p(T)T^3}$$

$$V(T_0) = \frac{kT_0}{q}\ln\frac{I(T_0)e^{\frac{E_g(T_0)}{kT_0}}}{M\frac{kT_0}{q}\mu_p(T_0){T_0}^3}$$

$$\frac{q}{kT}V(T) - \frac{q}{kT_0}V(T_0) = \ln\frac{I(T)e^{\frac{E_g(T)}{kT}}T_0\mu_p(T_0)T_0^3}{I(T_0)e^{\frac{E_g(T_0)}{kT_0}}T\mu_p(T)T^3}$$

$$\frac{q}{kT}V(T)-\frac{q}{kT_0}V(T_0)=\ln\frac{I(T)}{I(T_0)}+\frac{E_g(T)}{kT}-\frac{E_g(T_0)}{kT_0}+4\ln\frac{T_0}{T}+\ln\frac{\mu_p(T_0)}{\mu_p(T)}$$

$$V(T)-\frac{T}{T_0}V(T_0)=\frac{kT}{q}\ln\frac{I(T)}{I(T_0)}+\frac{E_g(T)}{q}-\frac{T}{T_0}\frac{E_g(T_0)}{q}+4\frac{kT}{q}\ln\frac{T_0}{T}+\frac{kT}{q}\ln\frac{\mu_p(T_0)}{\mu_p(T)}$$

Temperature dependency of the emitter current I is represented as follows where α is 1 if the current flowing through emitter is a PTAT current and 0 if it is temperature-independent.

$$I(T)=I_0T^{\alpha}$$

$$I(T_0)=I_0T_0^{\alpha}$$

$$V(T)=\frac{E_g(T)}{q}+\frac{T}{T_0}\left(V(T_0)-\frac{E_g(T_0)}{q}\right)+\frac{kT}{q}(4-\alpha)\ln\frac{T_0}{T}+\frac{kT}{q}\ln\frac{\mu_p(T_0)}{\mu_p(T)}$$

Temperature dependency of mobility μ_p is represented as a function of temperature as follows where $\gamma \cong 0.5$

$$\mu_p(T)=\mu_{p0}T^{-\gamma}$$

$$\mu_p(T_0)=\mu_{p0}T_0^{-\gamma}$$

Using the latter two mobility expressions and rearranging $V(T)$, Tsividis' expression is obtained as

$$V(T)=V_G(T)+\frac{T}{T_0}\left(V(T_0)-V_G(T_0)\right)+\frac{kT}{q}(4-\gamma-\alpha)\ln\frac{T_0}{T} \qquad \text{A14}$$

where $V_G(T)$ and $V_G(T_0)$ are bandgap voltage of the silicon at an arbitrary temperature T and reference temperature T_0, respectively. Variation of V with T at first and second-order can be derived via successively differentiating equation A14 with respect to T.

$$\frac{dV(T)}{dT}=\frac{V(T_0)-V_G(T_0)}{T_0}+\frac{dV_G(T)}{dT}-\frac{k}{q}(4-\gamma-\alpha)\left(\ln\frac{T}{T_0}+1\right)$$

$$\frac{d^2V(T)}{dT} = \frac{d^2V_G(T)}{dT} - \frac{k}{q}\frac{(4-\gamma-\alpha)}{T}$$

A.3. Analysis with Curvature-Correction (Secondary Effects Excluded)

Curvature-correction method of the bandgap voltage reference circuit is proposed by [12] and implemented by [11]. Basic idea is to correct the nonlinear term $\frac{kT}{q}(4-\gamma-\alpha)\ln\frac{T_0}{T}$ in A14 by a proper combination of V across a junction with a temperature–independent current (α=0) and V across a junction with a PTAT current (α=1). Via inspecting the circuit in Figure 2.1, we see that the current in the bipolar transistors Q_1 and Q_2 is a PTAT current with α=1, while the current in the p-channel transistors M_1/M_2 is at first-order temperature-independent.

This T-independent current is further mirrored by transistor M_4 and injected into the diode-connected bipolar transistor Q_3 resulting in V with α=0. The curvature-correction is achieved by placing two matched resistors R_4/R_5 in between the nodes at which emitters of bipolar transistors are connected and exhibiting different α values. By doing so, a nonlinear current is created to cancel out the nonlinear temperature dependency of the first-order temperature compensated currents of M_1/M_2.

Before proceeding any further, we need to derive the bandgap reference output voltage V_O for the case of curvature-correction network (composed of $R_4/R_5/Q_3/M_4$) is inserted. Simplified circuit for the analysis is given in Figure A3 and the derivation steps are given as follows:

Emitter voltage of Q_1 is

$$V_1 = \frac{kT}{q}\ln\frac{I_3}{I_S} \tag{A.15}$$

V_1 is also equal to the sum of voltages formed on Q_2 and R_0 as

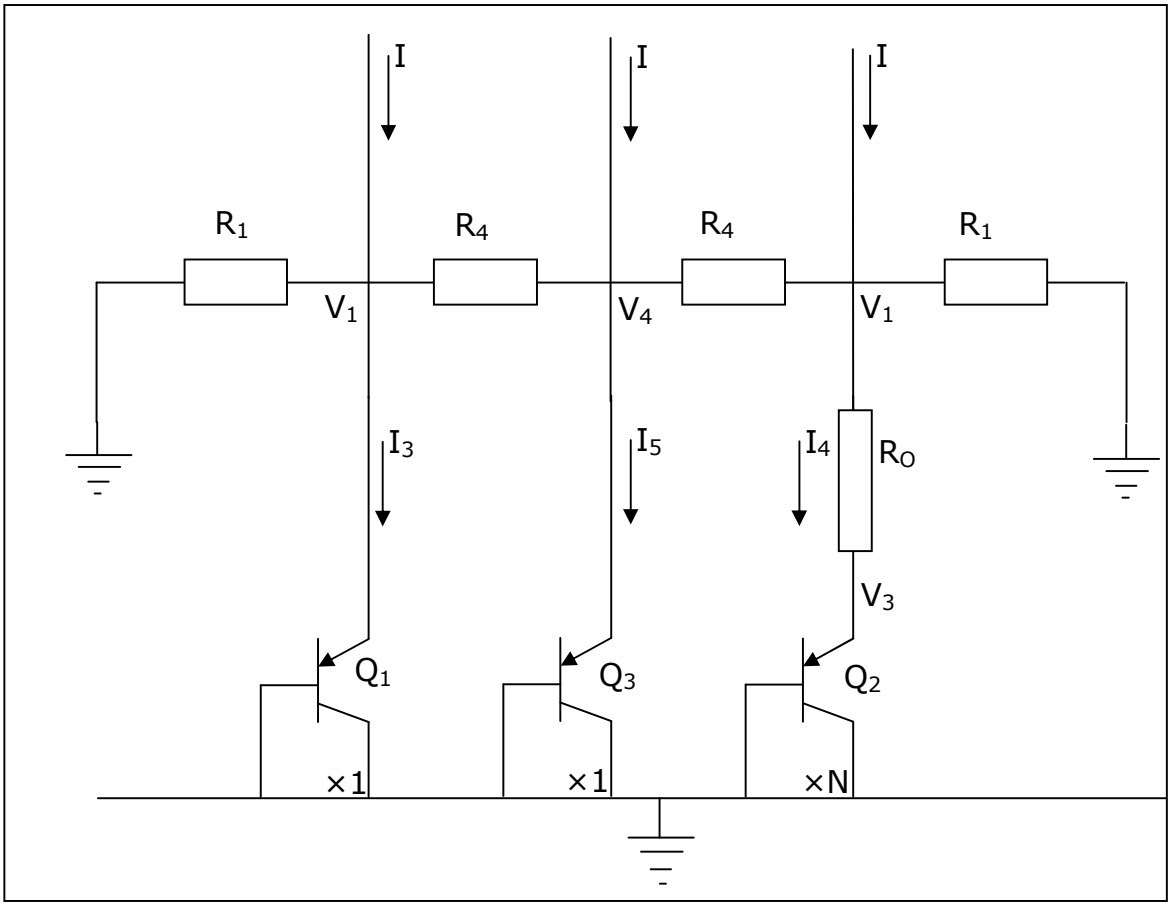

Figure A.3: Simplified circuit for curvature correction analysis.

$$V_1 = I_4 R_0 + \frac{kT}{q} \ln \frac{I_4}{N I_S} \tag{A.16}$$

Also

$$I_4 = I_3 \tag{A.17}$$

Equating A15 to A16 yields

$$I_4 = I_3 = \frac{1}{R_0} \frac{kT}{q} \ln N \tag{A.18}$$

Emitter voltage V_4 of Q_3 is

$$V_4 = \frac{kT}{q} \ln \frac{I_5}{I_S} \tag{A.19}$$

Using A15 and A19

$$V_4 - V_1 = \frac{kT}{q} \ln \frac{I_5}{I_3} \tag{A.20}$$

Performing KCL at V_4 yields

$$I = 2\frac{V_4 - V_1}{R_4} + I_5 \tag{A.21}$$

Using A20 and A21

$$I = \frac{2}{R_4} \frac{kT}{q} \ln \frac{I_5}{I_3} + I_5 \tag{A.22}$$

Performing KCL at V_1 yields

$$I = I_3 + \frac{V_1}{R_1} - \frac{V_4 - V_1}{R_4} \tag{A.23}$$

Using A20 and A23 yields

$$I = I_3 + \frac{V_1}{R_1} - \frac{1}{R_4} \frac{kT}{q} \ln \frac{I_5}{I_3} \tag{A.24}$$

By solving I_5 from A22 and substituting it into A24 to find out the final expression for I, it is seen that there is no analytical solution. So an approximation is made as follows:

If

$$\frac{2}{R_4} \frac{kT}{q} \ln \frac{I_5}{I_3} \ll I \tag{A.25}$$

then A22 yields

$$I_5 \cong I$$

Using this equality in A24

$$I = I_3 + \frac{V_1}{R_1} - \frac{1}{R_4}\frac{kT}{q}\ln\frac{I}{I_3} \tag{A.26}$$

Using $V_O = IR_3$ and A18 in A26 output voltage V_O can be expressed as

$$V_O = \frac{R_3}{R_0}\frac{kT}{q}\ln N + \frac{R_3}{R_1}V_1 - \frac{R_3}{R_4}\frac{kT}{q}\ln\left(\frac{IR_0}{\frac{kT}{q}\ln N}\right)$$

$$V_O = \frac{R_3}{R_1}\left[V_1 + \frac{R_1}{R_0}\frac{kT}{q}\ln N - \frac{R_1}{R_4}\frac{kT}{q}\ln\left(\frac{\frac{kT_0}{q}IR_0}{\frac{kT_0}{q}\frac{kT}{q}\ln N}\right)\right]$$

$$V_O = \frac{R_3}{R_1}\left[V_1 + \frac{R_1}{R_0}\frac{kT}{q}\ln N - \frac{R_1}{R_4}\frac{kT}{q}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N}\right) - \frac{R_1}{R_4}\frac{kT}{q}\ln\frac{T_0}{T}\right]$$

Finally reference output voltage V_O of the curvature-corrected bandgap reference is

$$V_O = \frac{R_3}{R_1}\left[V_1 + \frac{kT}{q}\left[\frac{R_1}{R_0}\ln N - \frac{R_1}{R_4}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N}\right)\right] + \frac{R_1}{R_4}\frac{kT}{q}\ln\frac{T}{T_0}\right] \tag{A.27}$$

where $\frac{R_1}{R_4}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N}\right)$ is an additional term introduced by curvature-correction and must be much lower than $\frac{R_1}{R_0}\ln N$.

A.4. Temperature Compensation of Reference Output Voltage at First-Order and Second-Order

Nominal Reference Voltage at $T=T_0$

$$V_O(T_0)=\frac{R_3}{R_1}\left(V_1(T_0)+\frac{R_1}{R_0}\frac{kT_0}{q}\ln N\right) \tag{A.28}$$

For A25

$$\frac{2}{R_4}\frac{kT_0}{q}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N}\right)\ll 1 \tag{A.29}$$

where $\frac{2}{R_4}\frac{kT_0}{q}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N}\right)$ is the total current going away from V_4 to V

and

$$\frac{1}{R_4}\frac{kT_0}{q}\ln\left(\frac{IR_0}{\frac{kT_0}{q}\ln N}\right)\ll I_3 \tag{A.30}$$

Obviously A30 overrides A29. Therefore, A30 has to be satisfied for design. Current I can then be expressed as

$$I \cong \frac{V_1(T_0)}{R_1} + \frac{1}{R_0}\frac{kT_0}{q}\ln N \tag{A.31}$$

First-Order Temperature Compensation of Reference Output Voltage

T-dependent terms of A14 and A27 are equated with proper sign to cancel them out as

$$\frac{V_G(T_0) - V_1(T_0)}{T_0} = \frac{R_1}{R_0}\frac{k}{q}\ln N \tag{A.32}$$

This turns A28 into

$$V_O(T_0) = \frac{R_3}{R_1}V_G(T_0) \tag{A.33}$$

and A31 into

$$I(T_0) = \frac{V_G(T_0)}{R_1} \tag{A.34}$$

Second-Order Temperature Compensation of the Reference Output Voltage

In A14 and A27 equate the $\frac{kT}{q}\ln\frac{T}{T_0}$-dependent terms as

$$-\frac{kT}{q}(4-\gamma-\alpha)\ln\frac{T}{T_0} + \frac{kT}{q}\frac{R_1}{R_4}\ln\frac{T}{T_0} = 0$$

which yields

$$\frac{R_1}{R_4} = 4 - \gamma - \alpha$$

where $\gamma \approx 0.5$ and $\alpha = 1$ due to the PTAT characteristic of emitter current of Q_1. Therefore, resistor ratio becomes

$$\frac{R_1}{R_4} \cong 2.5 \tag{A.35}$$

Circuit Design Plan:

If I can be specified from a given current budget, the following design plan must be executed:

1. Calculation of R_1 from A34,
2. Calculation of R_4 from A35,
3. Calculation of R_3 from A33, and
4. Calculation of $\frac{R_0}{\ln N}$ from A32 for a previously chosen N.

APPENDIX B: PSR ANALYSIS OF BANDGAP CORE CIRCUIT

PSR analysis of the bandgap core circuit in its original form given in Figure 2.1 (without the curvature-correction network) is performed in this section. The analysis is done on a simplified equivalent circuit presented in Figure B1. As previously explained, PSR is simply the voltage gain from circuit supply v_{dd} to bandgap reference output v_o which is usually expressed in decibels. This gain, $v_o/v_{dd,}$ should be as low as possible in order to achieve a high PSR performance.

Output voltage signal, $v_{o,}$ is formed by (a) directly through v_{dd} (the gain from source-to-drain of M_3) and (b) indirectly through v_{dd} by the gate voltage signal v_3 (the voltage gain from the common gates of $M_1/M_2/M_3$-to-drain of M_3).

Derivation starts with formulating the output voltage v_o in terms of the small signal parameters g_{m3} and r_{ds3} together with the signals v_{dd} and v_3. This relation is given in B1.

$$v_o = R_3\left(g_{m3}\left(v_{dd} - v_3\right) + \frac{v_{dd} - v_o}{r_{ds3}} \right)$$

$$v_o = g_{m3}\left(R_3 \parallel r_{ds3}\right)\left(v_{dd} - v_3\right) + \frac{R_3}{R_3 + r_{ds3}} v_{dd} \tag{B.1}$$

The voltage signal v_3 is actually a combination of (a) the variation produced by v_{dd} at the inputs of the core OTA (with a source-to-drain gain of M_1/M_2) and thus further at the output of the OTA (the resulting variation is further multiplied with the open-loop gain A_O) and (b) the variation between the input voltages of the OTA v_1/v_2 multiplied by A_O.

Representing the total gain from v_{dd} to the output of the OTA with $A_{d,}$ we can formulate the voltage signal v_3 as given in equation B2.

$$v_3 = A_d v_{dd} + A_o(v_2 - v_1)$$

$$v_{dd} - v_3 = \left(1 - A_d\right) v_{dd} - A_o\left(v_2 - v_1\right) \tag{B.2}$$

The voltage signal v_3 is actually a combination of (a) the variation produced by v_{dd} at the inputs of the core OTA (with a source-to-drain gain of M_1/M_2) and thus further at the output of the OTA (the resulting variation is further multiplied with the open-loop gain A_O) and (b) the variation between the input voltages of the OTA v_1/v_2 multiplied by A_O.

Representing the total gain from v_{dd} to the output of the OTA with $A_{d,}$ we can formulate the voltage signal v_3 as given in equation B2.

$$v_3 = A_d v_{dd} + A_o (v_2 - v_1)$$

$$v_{dd} - v_3 = (1 - A_d) v_{dd} - A_o (v_2 - v_1) \tag{B.2}$$

In order to derive the expression of the differential input voltage expression v_2-v_1 of the core OTA, resistance values at the input are lumped as R_a and R_b.

$$R_a = R_1 \parallel r_e$$

$$R_b = R_1 \parallel (R_0 + r_e)$$

Afterwards, v_2 and v_1 can be written by equations B3 and B4, respectively and the differential input voltage can be derived as in B5.

$$v_2 = R_b \left(g_m (v_{dd} - v_3) + \frac{v_{dd} - v_2}{r_{ds}} \right)$$

$$v_2 = g_m (R_b \parallel r_{ds})(v_{dd} - v_3) + \frac{R_b}{R_b + r_{ds}} v_{dd} \tag{B.3}$$

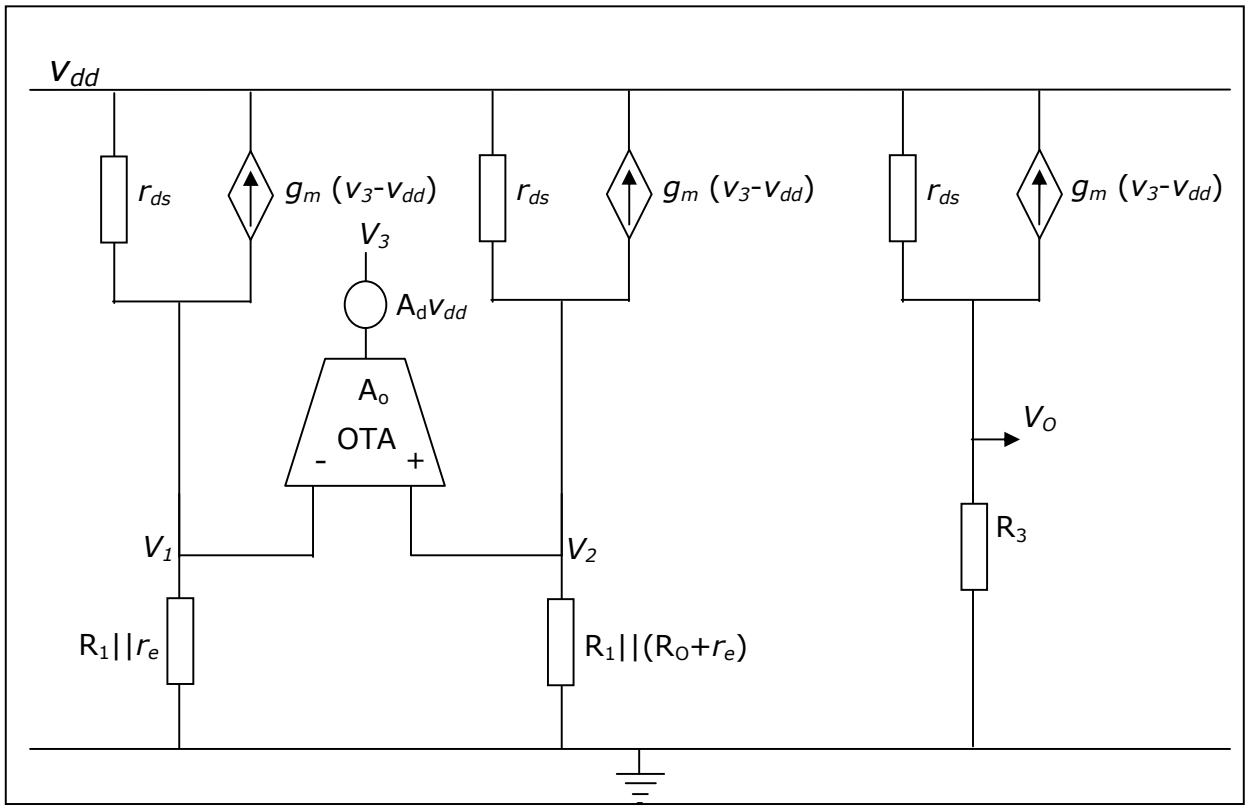

Figure B.1. Equivalent bandgap reference core circuit for PSR analysis

$$v_1 = R_a\left(g_m\left(v_{dd} - v_3\right) + \frac{v_{dd} - v_1}{r_{ds}} \right)$$

$$v_1 = g_m\left(R_a \parallel r_{ds}\right)\left(v_{dd} - v_3\right) + \frac{R_a}{R_a + r_{ds}} v_{dd} \tag{B.4}$$

$$v_2 - v_1 = g_m\left[\left(R_b \parallel r_{ds}\right) - \left(R_a \parallel r_{ds}\right)\right]\left(v_{dd} - v_3\right) + \left(\frac{R_b}{R_b + r_{ds}} - \frac{R_a}{R_a + r_{ds}} \right) v_{dd} \tag{B.5}$$

By substituting B5 in B2 we obtain the relationship given by equation B6 and furthermore, by inserting B6 in the general expression given in B1 the v_o expression turns into B7.

$$v_{dd} - v_3 = \left(1 - A_d\right) v_{dd} - A_o g_m\left[\left(R_b \parallel r_{ds}\right) - \left(R_a \parallel r_{ds}\right)\right]\left(v_{dd} - v_3\right) - A_o\left(\frac{R_b}{R_b + r_{ds}} - \frac{R_a}{R_a + r_{ds}} \right) v_{dd}$$

$$\left(1 + A_o g_m\left[\left(R_b \parallel r_{ds}\right) - \left(R_a \parallel r_{ds}\right)\right]\right)\left(v_{dd} - v_3\right) = \left(1 - A_d - A_o\left(\frac{R_b}{R_b + r_{ds}} - \frac{R_a}{R_a + r_{ds}} \right) v_{dd} \right) \tag{B.6}$$

$$v_o = \left(g_{m3}\left(R_3 \parallel r_{ds}\right) \frac{1 - A_d - A_o\left(\frac{R_b}{R_b + r_{ds}} - \frac{R_a}{R_a + r_{ds}}\right)}{1 + A_o g_m\left[\left(R_b \parallel r_{ds}\right) - \left(R_a \parallel r_{ds}\right)\right]} + \frac{R_3}{R_3 + r_{ds}} \right) v_{dd} \quad \text{(B.7)}$$

Lumped resistors R_a/R_b are expanded as

$$\frac{R_b}{R_b + r_{ds}} - \frac{R_a}{R_a + r_{ds}} = \frac{R_b - R_a}{\left(R_a + r_{ds}\right)\left(R_b + r_{ds}\right)} r_{ds}$$

$$R_a = R_1 \parallel r_e = \frac{R_1 r_e}{R_1 + r_e}$$

$$R_b = R_1 \parallel \left(R_0 + r_e\right) = \frac{R_1\left(R_0 + r_e\right)}{R_1 + R_0 + r_e}$$

$$R_b - R_a = \frac{{R_1}^2 R_0}{\left(R_1 + R_0 + r_e\right)\left(R_1 + r_e\right)}$$

Assuming $r_e \ll R_1$ yields

$$R_b - R_a \cong \frac{R_1 R_0}{R_1 + R_0}$$

$$R_a \cong r_e$$

$$R_b \cong \frac{R_1 R_0}{R_1 + R_0} = R_1 \parallel R_0$$

If $r_e \ll r_{ds}$, then, B7 turns into

$$\frac{v_o}{v_{dd}} = \left[g_{m3}\left(R_3 \parallel r_{ds3}\right) \frac{1 - A_d - A_o\left(\dfrac{R_1 \parallel R_0}{\left(R_1 \parallel R_0\right) + r_{ds}} - \dfrac{r_e}{r_{ds}}\right)}{1 + A_o g_m \left(R_1 \parallel R_0 \parallel r_{ds} - r_e\right)} + \frac{R_3}{R_3 + r_{ds3}} \right]$$

$$= g_{m3}\left(R_3 \parallel r_{ds3}\right) \frac{1 - A_d - A_o\left(\dfrac{R_1 \parallel R_0}{\left(R_1 \parallel R_0\right) + r_{ds}}\right)}{1 + A_o g_m \left(R_1 \parallel R_0 \parallel r_{ds}\right)} + \frac{R_3}{R_3 + r_{ds3}}$$

Since $g_{m3} = g_m$ and $A_o g_m \left(R_1 \parallel R_0 \parallel r_{ds}\right) \gg 1$ equation B1 turns into B8 as

$$\frac{v_o}{v_{dd}} = \left(R_3 \parallel r_{ds3}\right) \frac{1 - A_d - A_o\left(\dfrac{R_1 \parallel R_0}{\left(R_1 \parallel R_0\right) + r_{ds}}\right)}{A_o g_m \left(R_1 \parallel R_0 \parallel r_{ds}\right)} + \frac{R_3}{R_3 + r_{ds3}} \tag{B.8}$$

$$= \frac{R_3 \parallel r_{ds3}}{R_1 \parallel R_0 \parallel r_{ds}}\left(\frac{1}{A_o} - \frac{A_d}{A_o}\right) - \frac{R_3 \parallel r_{ds3}}{r_{ds}} + \frac{R_3}{R_3 + r_{ds3}}$$

In equation B8 the term A_d/A_O is actually the inverse of the power-supply-rejection-ratio (PSRR) of the core OTA, thus can be represented with *1/PSRR*. In addition to that, assuming $r_{ds} \gg R_1 \parallel R_O$ and R_3 the final representation of the gain from v_{dd} to the bandgap reference output v_o can be written as in B9 and PSR in decibels as in B10.

$$\frac{v_o}{v_{dd}} = \frac{R_3}{R_1 \parallel R_0}\left(\frac{1}{A_o} - \frac{1}{PSRR}\right) - \frac{R_3}{r_{ds}} + \frac{R_3}{r_{ds3}} \tag{B.9}$$

$$PSR = 20\log\left(\frac{v_o}{v_{dd}}\right) = 20\log\left[\frac{R_3}{R_1 \parallel R_0}\left(\frac{1}{A_o} - \frac{1}{PSRR}\right) - \frac{R_3}{r_{ds}} + \frac{R_3}{r_{ds3}}\right] \tag{B.10}$$

APPENDIX C: TABLES REPRESENTING SIMULATION RESULTS OF PROPOSED BANDGAP VOLTAGE REFERENCE

Table C1. Operation-point, noise, and ac simulation results for β=2.3926 at 1 V supply voltage

BJT MODEL	VERT- LB	VDD=1V	β=2.3926
R_0			434.7k
$R_{4,5}$			952.6k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (µA)	OUTPUT NOISE (µV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	543.6546	-0.3394	3.1951	195.9591	62.00	36.75
-40	543.9665	-0.2822	3.2910	204.4504	66.30	37.00
-30	544.2458	-0.2310	3.3886	212.8379	70.00	37.55
-20	544.4779	-0.1885	3.4836	220.9072	73.12	37.80
-10	544.7638	-0.1361	3.5721	227.5961	74.65	38.12
0	544.9683	-0.0986	3.6633	229.3468	72.55	38.56
10	545.1504	-0.0652	3.7531	221.3594	69.74	39.40
20	545.2978	-0.0382	3.8407	202.9778	69.00	40.60
30	545.4122	-0.0172	3.9262	182.7566	72.20	41.60
40	545.5060	0.0000	4.0088	172.3368	80.17	41.00
50	545.5510	0.0082	4.0878	173.4935	107.60	41.30
60	545.5328	0.0049	4.1640	177.2004	102.30	41.40
70	545.6601	0.0282	4.2378	178.5884	97.60	41.40
80	545.5902	0.0154	4.3081	184.9324	90.20	41.50
90	545.5019	-0.0008	4.3757	188.9444	86.20	41.55
100	545.4116	-0.0173	4.4402	193.1320	85.50	41.60
110	544.8167	-0.1264	4.5004	196.4688	85.00	41.60
120	545.1862	-0.0586	4.5597	201.4944	78.35	41.60
130	545.0655	-0.0808	4.6149	205.6696	75.65	41.80
140	544.9530	-0.1014	4.6668	210.0000	72.33	41.80
150	544.9306	-0.1055	4.7157	214.4761	69.70	41.80
160	544.8346	-0.1231	4.7595	220.2271	66.60	41.70
170	545.9529	0.0819	4.8016	225.6102	64.20	41.80
180	544.0870	-0.2601	4.8333	237.2762	60.00	41.65

Table C2. Operation-point, noise, and ac simulation results for β=5.9812 at 1V supply voltage

BJT MODEL		VERT- TYPICAL	VDD=1V			β=5.9812
R_0						421.2k
$R_{4,5}$						952.6k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	545.7342	-0.2549	3.1998	198.4943	63.60	36.70
-40	545.9153	-0.2218	3.2953	207.1231	67.84	37.15
-30	546.1507	-0.1788	3.3953	215.6385	71.80	37.45
-20	546.1674	-0.1757	3.4831	223.3830	75.80	37.60
-10	546.2396	-0.1625	3.5751	228.9104	107.44	38.40
0	546.6277	-0.0916	3.6670	228.0350	71.60	38.68
10	546.6716	-0.0835	3.7563	214.9418	69.30	39.72
20	546.7287	-0.0731	3.8440	193.6491	70.00	41.10
30	546.6983	-0.0787	3.9289	175.7839	78.40	41.70
40	547.1287	0.0000	4.0122	171.7556	94.72	41.30
50	546.7166	-0.0753	4.0895	174.9285	106.00	41.20
60	546.6190	-0.0932	4.1655	178.8854	93.14	41.35
70	546.6370	-0.0899	4.2399	183.0300	94.74	41.40
80	546.6196	-0.0930	4.3090	186.8154	90.74	41.50
90	546.8135	-0.0576	4.3773	181.6590	91.80	40.20
100	546.1277	-0.1830	4.4397	195.4482	84.00	41.60
110	546.1277	-0.1830	4.4397	198.9974	84.00	41.50
120	546.4940	-0.1160	4.5592	203.2240	82.46	41.75
130	545.4975	-0.2981	4.6086	209.2008	75.20	41.27
140	545.2470	-0.3439	4.6516	214.9418	72.50	41.70
150	544.9378	-0.4004	4.6844	222.7105	69.50	41.56
160	544.3487	-0.5081	4.7077	232.8089	66.50	41.45
170	543.7383	-0.6197	4.7280	242.8991	63.55	41.33
180	540.8912	-1.1400	4.7450	260.1922	60.00	41.00

Table C3. Operation-point, noise, and ac simulation results for β=9.5698 at 1V supply voltage

BJT MODEL	VERT- HB	VDD=1V	β=9.5698
R_0			421.2k
$R_{4,5}$			946.5k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	546.5809	-0.1399	3.2020	198.7460	63.34	36.70
-40	546.7595	-0.1073	3.2975	207.3644	67.75	37.12
-30	546.9137	-0.0791	3.3921	214.4761	71.28	37.45
-20	547.0648	-0.0515	3.4854	224.0535	73.80	37.70
-10	547.1734	-0.0317	3.5776	230.0000	74.60	38.00
0	547.2680	-0.0144	3.6686	228.9104	72.30	38.50
10	547.3300	-0.0031	3.7582	216.5640	69.30	39.65
20	547.4032	0.0103	3.8457	194.9358	65.20	41.00
30	547.3080	-0.0071	3.9305	176.9180	78.42	41.70
40	547.3469	0.0000	4.0128	172.3368	89.60	41.30
50	547.2939	-0.0097	4.0913	175.2141	105.40	41.30
60	547.1484	-0.0363	4.1669	179.1647	93.50	41.30
70	547.1534	-0.0354	4.2404	183.3030	90.70	41.40
80	547.1221	-0.0411	4.3106	187.4299	89.00	41.40
90	546.8608	-0.0888	4.3775	191.0497	86.20	41.50
100	546.5070	-0.1534	4.4409	186.5475	83.00	41.80
110	545.7605	-0.2898	4.4999	199.2485	83.15	41.65
120	546.1824	-0.2128	4.5584	204.4504	78.50	41.70
130	545.9552	-0.2543	4.6103	209.2844	75.32	41.65
140	545.6889	-0.3029	4.6541	215.1743	72.50	41.66
150	545.3893	-0.3577	4.6874	222.9343	69.43	41.58
160	544.8076	-0.4639	4.7112	232.8090	66.33	41.45
170	544.4359	-0.5318	4.7324	239.7915	63.65	41.40
180	541.8604	-1.0024	4.7503	259.0366	60.00	41.00

Table C4. Operation-point, noise, and ac simulation results for β=9.5698-HS at 1 V supply voltage

BJT MODEL	VERT- HS	VDD=1V	β=9.5698
R_0			410.4k
$R_{4,5}$			952.6k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (µA)	OUTPUT NOISE (µV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	548.9463	-0.3136	3.2074	200.4993	64.00	36.60
-40	549.2472	-0.2590	3.3033	209.2844	68.20	37.00
-30	549.2919	-0.2509	3.4001	217.0253	72.65	37.45
-20	549.7170	-0.1737	3.4918	226.0530	75.20	37.70
-10	549.9720	-0.1274	3.5846	230.8679	75.00	38.00
0	550.1550	-0.0941	3.6757	227.5961	71.47	38.80
10	550.1988	-0.0862	3.7662	211.8962	75.00	39.85
20	550.4584	-0.0390	3.8537	189.7366	67.50	41.20
30	550.4711	-0.0367	3.9388	174.3559	81.50	41.60
40	550.6734	0.0000	4.0211	172.9161	94.00	41.20
50	550.6422	-0.0057	4.0995	176.6352	92.00	41.20
60	550.6649	-0.0015	4.1758	180.5547	90.70	41.25
70	550.6525	-0.0038	4.2490	184.6618	89.28	41.40
80	550.5939	-0.0144	4.3191	188.9444	87.00	41.40
90	550.5190	-0.0280	4.3869	193.1320	84.00	41.50
100	550.4484	-0.0409	4.4501	197.4841	83.40	41.55
110	550.3210	-0.0640	4.5103	201.9900	80.00	41.60
120	550.2670	-0.0738	4.5656	205.9126	79.20	41.65
130	549.9722	-0.1273	4.6115	213.0727	75.20	41.58
140	549.7364	-0.1702	4.6456	220.9072	72.50	41.50
150	549.3304	-0.2439	4.6687	231.0844	70.00	41.40
160	548.2650	-0.4374	4.6838	243.5159	66.00	41.15
170	546.6245	-0.7353	4.6967	258.4569	63.00	40.80
180	542.6597	-1.4553	4.7085	276.7670	60.00	40.60

Table C5. Operation-point, noise, and ac simulation results for β=2.3926 at 1.55 V supply voltage

BJT MODEL		VERT- LB		VDD=1.55V		β=2.3926
R_0						434.7k
$R_{4,5}$						952.6k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	543.5742	-0.3548	3.5678	178.1710	135.00	66.35
-40	543.8939	-0.2962	3.6566	166.2897	135.60	67.60
-30	544.1885	-0.2422	3.7470	152.2410	139.17	68.70
-20	544.4852	-0.1878	3.8371	146.7458	149.10	68.50
-10	544.6998	-0.1484	3.9265	148.9950	148.00	68.50
0	544.9259	-0.1070	4.0148	152.6824	153.77	68.60
10	545.1107	-0.0731	4.1029	156.4707	159.48	68.70
20	545.2869	-0.0408	4.1892	160.3295	163.82	68.50
30	545.4088	-0.0185	4.2745	164.2171	175.80	69.00
40	545.5095	0.0000	4.3578	168.1468	172.00	69.00
50	545.5646	0.0101	4.4393	172.0933	163.50	69.00
60	545.5347	0.0046	4.5183	175.9490	163.30	69.30
70	545.6074	0.0179	4.5954	180.0482	162.92	69.40
80	545.5492	0.0073	4.6675	184.1078	155.00	69.50
90	545.4842	-0.0046	4.7373	188.1587	151.20	69.30
100	545.4237	-0.0157	4.8023	192.2614	146.00	69.50
110	545.4698	-0.0073	4.8653	196.3341	144.00	69.50
120	545.1912	-0.0583	4.9238	200.5509	137.30	69.50
130	545.4539	-0.0102	4.9823	204.5873	132.50	69.50
140	545.0255	-0.0887	5.0360	209.0708	127.00	69.50
150	545.2458	-0.0483	5.0903	213.2666	122.00	69.50
160	544.9652	-0.0998	5.1393	219.0863	116.00	69.50
170	544.9652	-0.0998	5.1393	226.1761	110.30	69.00
180	544.6939	-0.1495	5.2322	235.7563	104.00	68.20

Table C6. Operation-point, noise, and ac simulation results for β=5.9812 at 1.55 V supply voltage

BJT MODEL		VERT- TYPICAL		VDD=1.55V		β=5.9812
R_0						421.2k
$R_{4,5}$						952.6k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (µA)	OUTPUT NOISE (µV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	545.6595	-0.1989	3.5725	175.3555	135.00	66.60
-40	545.8890	-0.1569	3.6615	161.3593	136.70	68.00
-30	546.0872	-0.1207	3.7515	148.9341	141.70	68.80
-20	546.2702	-0.0872	3.8412	147.0182	146.80	68.40
-10	546.4485	-0.0546	3.9300	150.2064	153.70	68.40
0	546.5559	-0.0350	4.0182	154.0205	156.00	68.60
10	546.6435	-0.0189	4.1055	157.9128	160.00	68.60
20	546.7138	-0.0061	4.1920	161.7031	163.70	68.80
30	546.7489	0.0003	4.2768	165.8177	190.40	69.00
40	546.7471	0.0000	4.3599	169.8322	165.00	69.00
50	546.7217	-0.0046	4.4411	173.8607	169.50	69.00
60	546.5977	-0.0273	4.5196	177.8090	161.50	69.30
70	546.5758	-0.0313	4.5961	181.9985	158.50	69.40
80	546.8149	0.0124	4.6694	185.8794	147.30	69.50
90	546.2828	-0.0849	4.7372	190.3118	150.20	69.40
100	546.1352	-0.1119	4.8018	194.5281	146.00	69.50
110	546.1012	-0.1181	4.8640	198.7807	143.10	69.40
120	545.7541	-0.1816	4.9215	203.2838	137.55	69.50
130	545.5322	-0.2222	4.9750	208.1486	133.00	69.50
140	545.3071	-0.2634	5.0211	214.0191	127.00	69.50
150	545.6909	-0.1932	5.0605	221.1757	122.80	69.00
160	544.4548	-0.4193	5.0875	231.6040	116.00	68.50
170	543.7917	-0.5405	5.1145	243.6374	110.00	68.00
180	541.6974	-0.9236	5.1435	258.1346	103.00	67.40

Table C7. Operation-point, noise, and ac simulation results for β=9.5698 at 1.55 V supply voltage

BJT MODEL	VERT- HB	VDD=1.55V	β=9.5698
R_0			421.2k
$R_{4,5}$			946.5k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	546.4901	-0.1555	3.5747	176.6792	135.10	66.40
-40	546.7010	-0.1169	3.6636	162.7871	135.00	68.00
-30	546.8601	-0.0879	3.7536	149.8887	140.00	68.70
-20	546.9809	-0.0658	3.8430	147.3922	150.00	68.00
-10	547.1251	-0.0395	3.9321	150.4602	150.00	68.50
0	547.2295	-0.0204	4.0201	154.3208	153.00	68.50
10	547.3089	-0.0059	4.1078	158.1719	161.00	68.50
20	547.3413	0.0000	4.1937	162.1519	164.00	68.00
30	547.3541	0.0024	4.2786	166.1147	160.00	69.00
40	547.3411	0.0000	4.3615	170.1442	168.00	69.00
50	547.2943	-0.0086	4.4430	174.1761	160.00	69.30
60	547.1593	-0.0332	4.5212	178.1304	160.00	69.20
70	547.1053	-0.0431	4.5978	182.3263	155.55	69.18
80	546.9695	-0.0679	4.6699	186.4808	152.00	69.50
90	546.8003	-0.0988	4.7389	190.6467	152.50	69.20
100	546.6328	-0.1294	4.8032	194.8811	146.50	69.50
110	546.5342	-0.1474	4.8655	199.1398	142.00	69.50
120	546.2065	-0.2073	4.9231	203.6102	137.00	69.20
130	545.9009	-0.2631	4.9768	208.4378	133.00	69.50
140	545.7439	-0.2918	5.0234	214.2215	127.20	69.40
150	545.8621	-0.2702	5.0626	221.3216	122.50	69.00
160	544.9704	-0.4331	5.0911	231.4687	116.00	69.00
170	544.3040	-0.5549	5.1186	243.4684	110.00	68.50
180	542.2957	-0.9218	5.1477	257.8577	103.00	67.50

Table C8. Operation-point, noise, and ac simulation results for β=9.5698-HS at 1.55 V supply voltage

BJT MODEL	VERT- HS	VDD=1.55V	β=9.5698
R_0			410.4k
$R_{4,5}$			952.6k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (µA)	OUTPUT NOISE (µV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	548.8732	-0.3163	3.5804	174.0152	135.20	66.80
-40	549.1747	-0.2616	3.6697	159.1711	137.20	68.00
-30	549.4066	-0.2195	3.8068	148.0237	160.00	68.20
-20	549.6473	-0.1757	3.8495	147.9036	150.00	68.00
-10	549.9069	-0.1286	3.9389	151.3146	151.00	68.40
0	550.1215	-0.0896	4.0272	155.3023	156.50	68.60
10	550.2811	-0.0606	4.1150	159.2657	163.00	68.50
20	550.4204	-0.0353	4.2013	163.2818	166.00	68.70
30	550.5349	-0.0145	4.2867	167.3173	163.50	68.80
40	550.6150	0.0000	4.3697	171.4165	164.00	69.00
50	550.6570	0.0076	4.4513	175.5223	156.50	69.00
60	550.5968	-0.0033	4.5298	179.5105	164.00	69.50
70	550.6019	-0.0024	4.6065	183.8298	155.00	69.20
80	550.5879	-0.0049	4.6788	188.0533	152.00	69.30
90	550.5423	-0.0132	4.7482	192.3317	149.00	69.30
100	550.4582	-0.0285	4.8123	196.6776	146.00	69.40
110	550.3337	-0.0511	4.8738	201.1670	141.50	69.40
120	550.1548	-0.0836	4.9297	206.0416	137.00	69.50
130	550.3386	-0.0502	4.9792	211.7675	132.80	69.50
140	549.7739	-0.1528	5.0152	219.7793	127.40	69.40
150	550.1812	-0.0788	5.0450	229.2482	123.20	69.00
160	548.6943	-0.3488	5.0643	242.1135	116.00	68.60
170	547.1723	-0.6252	5.0846	256.8693	110.00	68.00
180	543.7058	-1.2548	5.1073	274.1137	104.00	67.20

Table C9. Operation-point, noise, and ac simulation results for β=2.3926 at 3.5 V supply voltage

BJT MODEL	VERT- LB	VDD=3.5V	β=2.3926
R_0			434.7k
$R_{4,5}$			952.6k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	543.5870	-0.3133	3.8221	177.7638	134.50	72.00
-40	543.9000	-0.2559	3.9146	165.8312	135.60	73.20
-30	544.2040	-0.2002	4.0084	151.9868	137.65	74.30
-20	544.4663	-0.1521	4.1012	146.6287	145.40	74.00
-10	544.7083	-0.1077	4.1938	148.9966	150.80	74.00
0	544.9339	-0.0663	4.2851	152.6433	152.95	74.20
10	545.1190	-0.0324	4.3752	156.2049	157.25	74.50
20	545.3750	0.0146	4.4648	160.0000	154.35	74.60
30	545.4258	0.0239	4.5519	164.0121	183.00	75.00
40	545.2955	0.0000	4.6367	167.0329	163.60	75.00
50	545.1049	-0.0350	4.7193	171.7556	156.50	75.00
60	545.6396	0.0631	4.8015	175.7839	166.60	75.00
70	545.5560	0.0478	4.8792	180.0000	161.50	75.00
80	545.5591	0.0483	4.9534	183.8477	157.00	75.40
90	545.5021	0.0379	5.0233	188.1488	156.00	75.40
100	545.4237	0.0235	5.0897	192.0937	152.00	75.45
110	545.3187	0.0043	5.1528	196.2141	148.60	75.60
120	545.2021	-0.0171	5.2123	200.4993	144.73	75.70
130	545.1098	-0.0341	5.2697	204.6948	140.00	76.00
140	544.6165	-0.1245	5.3234	208.8061	134.30	76.00
150	544.8290	-0.0855	5.3778	213.3072	130.00	76.00
160	544.5924	-0.1289	5.4267	219.0890	124.40	76.40
170	544.8073	-0.0895	5.4738	226.4950	120.00	76.30
180	544.3370	-0.1758	5.5200	235.7965	113.50	76.00

Table C10. Operation-point, noise, and ac simulation results for β=5.9812 at 3.5 V supply voltage

BJT MODEL		VERT- TYPICAL	VDD=3.5V			β=5.9812
R_0						421.2k
$R_{4,5}$						952.6k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	545.6688	-0.1809	3.8270	174.9285	134.70	72.00
-40	545.7997	-0.1570	3.9189	159.3737	140.00	73.80
-30	546.0914	-0.1036	4.0128	148.6068	142.00	74.30
-20	546.2767	-0.0697	4.1053	146.9693	148.30	74.00
-10	546.4331	-0.0411	4.1972	150.0000	152.00	74.00
0	546.5849	-0.0133	4.2884	153.9480	155.00	74.30
10	546.6428	-0.0027	4.3783	157.7973	160.00	74.50
20	546.7021	0.0081	4.4671	161.5549	173.75	74.50
30	546.7503	0.0169	4.5543	165.5294	166.40	74.75
40	546.6578	0.0000	4.6392	169.7056	165.40	75.00
50	546.5631	-0.0173	4.7219	173.7814	162.00	75.00
60	546.7060	0.0088	4.8030	177.7638	166.00	75.00
70	546.6432	-0.0027	4.8804	181.9340	160.33	75.00
80	546.4719	-0.0340	4.9538	186.0107	158.00	75.00
90	546.2978	-0.0659	5.0239	190.2629	154.80	75.40
100	546.1508	-0.0927	5.0892	194.4222	150.55	75.50
110	545.9497	-0.1295	5.1518	198.7460	147.60	75.40
120	545.7548	-0.1652	5.2096	203.2240	144.00	76.00
130	545.5322	-0.2059	5.2634	208.0865	140.00	76.00
140	545.2904	-0.2501	5.3101	214.0093	134.70	76.00
150	545.1195	-0.2814	5.3475	221.1334	130.40	76.00
160	544.4613	-0.4018	5.3761	231.5067	124.65	76.00
170	543.3493	-0.6052	5.4022	243.7211	120.00	76.00
180	541.0475	-1.0263	5.4303	258.4569	113.20	62.60

Table C11: Operation-point, noise, and ac simulation results for β=9.5698 at 3.5 V supply voltage.

BJT MODEL	VERT- HB	VDD=3.5V	β=9.5698
R_0			421.2k
$R_{4,5}$			946.5k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (µA)	OUTPUT NOISE (µV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	546.4964	-0.1532	3.8291	176.3519	135.33	72.00
-40	546.7071	-0.1147	3.9213	162.4807	135.14	73.50
-30	546.8620	-0.0864	4.0139	149.6662	142.80	74.30
-20	547.0185	-0.0578	4.1075	147.3091	146.82	74.00
-10	547.1318	-0.0371	4.1990	150.3329	150.68	74.00
0	547.3827	0.0087	4.2905	153.9480	157.60	74.20
10	547.3048	-0.0055	4.3803	158.1138	166.70	74.40
20	547.3460	0.0020	4.4689	161.8641	167.30	74.50
30	547.3035	-0.0058	4.5559	165.8312	171.10	74.70
40	547.3350	0.0000	4.6411	170.0000	177.52	74.90
50	546.7996	-0.0978	4.7228	174.0689	154.50	75.00
60	547.2178	-0.0214	4.8044	178.0449	167.50	75.10
70	547.1660	-0.0309	4.8820	182.2086	162.60	75.00
80	546.9822	-0.0645	4.9554	186.2793	156.40	75.20
90	547.0417	-0.0536	5.0259	188.9444	155.45	75.50
100	546.6682	-0.1218	5.0908	194.6792	151.50	75.60
110	546.4342	-0.1646	5.1532	189.7366	148.40	75.50
120	546.2209	-0.2035	5.2114	203.4698	144.20	75.20
130	545.9663	-0.2501	5.2652	201.0870	140.00	75.70
140	545.7471	-0.2901	5.3122	214.0093	135.20	76.00
150	545.5568	-0.3249	5.3504	221.3594	130.40	76.00
160	544.9283	-0.4397	5.3796	231.5067	124.65	76.00
170	544.6916	-0.4830	5.4083	243.1049	120.00	75.80
180	541.5882	-1.0500	5.4345	258.2634	113.50	75.80

Table C12: Operation-point, noise, and ac simulation results for β=9.5698-HS at 3.5 V supply voltage.

BJT MODEL	VERT- HS	VDD=3.5V				β=9.5698 HS
R_0						410.4k
$R_{4,5}$						952.6k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (µA)	OUTPUT NOISE (µV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	548.8651	-0.3161	3.8347	173.4935	137.70	72.00
-40	549.2381	-0.2483	3.9275	158.7450	132.00	73.20
-30	549.4508	-0.2097	4.0204	147.9864	144.70	74.30
-20	549.7413	-0.1569	4.1140	147.6482	147.80	73.95
-10	549.9239	-0.1238	4.2058	151.3274	151.70	74.00
0	550.1098	-0.0900	4.2971	155.2417	157.45	74.20
10	550.0263	-0.1052	4.3869	158.7450	172.60	74.50
20	550.4372	-0.0305	4.4765	163.0950	180.00	75.00
30	550.5388	-0.0121	4.5641	167.0923	167.70	74.80
40	550.6054	0.0000	4.6493	171.1724	168.40	75.00
50	550.6765	0.0129	4.7325	175.4992	163.65	75.00
60	550.6711	0.0119	4.8131	179.4435	162.00	75.00
70	550.7356	0.0236	4.8909	183.5755	160.00	75.10
80	550.7155	0.0200	4.9650	187.8829	158.70	75.40
90	550.5228	-0.0150	5.0341	192.0937	154.50	75.40
100	550.0943	-0.0928	5.0988	194.9358	149.05	75.60
110	550.3232	-0.0513	5.1616	200.9975	147.50	77.50
120	550.1955	-0.0744	5.2182	205.9126	144.00	75.50
130	549.9990	-0.1101	5.2665	211.8962	140.00	75.70
140	549.8118	-0.1441	5.3040	219.0890	135.20	75.50
150	549.7485	-0.1556	5.3325	229.3468	131.00	75.50
160	548.2823	-0.4219	5.3515	242.0743	125.00	75.50
170	547.5383	-0.5570	5.3743	256.5151	120.00	75.40
180	544.6739	-1.0773	5.3993	273.4958	114.00	75.30

Table C13: Operation-point, noise, and ac simulation results for β=2.3926 at 5.5 V supply voltage.

BJT MODEL		VERT- LB		VDD=5.5V		β=2.3926
R_0						434.7k
$R_{4,5}$						952.6k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	543.5708	-0.3582	4.0465	172.1443	101.74	70.80
-40	543.9050	-0.2969	4.1602	158.7344	102.67	72.60
-30	544.2065	-0.2417	4.2782	146.2472	106.30	73.30
-20	544.4206	-0.2024	4.3802	145.6234	112.30	73.00
-10	544.7045	-0.1504	4.4817	140.8849	119.40	73.00
0	544.9030	-0.1140	4.5803	152.5573	121.75	73.00
10	545.2338	-0.0533	4.6746	156.2260	120.00	73.00
20	545.3044	-0.0404	4.7675	160.2602	133.50	73.00
30	545.4304	-0.0173	4.8585	164.1460	134.00	73.00
40	545.5248	0.0000	4.9471	168.0635	142.40	73.00
50	545.5748	0.0092	5.0340	172.0273	138.40	72.80
60	545.6298	0.0192	5.1166	175.9884	132.75	72.70
70	545.5984	0.0135	5.1973	180.0069	128.25	72.70
80	545.5597	0.0064	5.2735	184.0428	123.65	72.70
90	545.5118	-0.0024	5.3463	188.1008	121.58	72.62
100	545.4345	-0.0166	5.4145	192.1863	117.00	72.60
110	545.2844	-0.0441	5.4785	196.3083	114.25	72.60
120	545.2663	-0.0474	5.5371	200.4431	110.60	72.25
130	545.1067	-0.0766	5.5993	204.6281	107.20	72.55
140	545.0196	-0.0926	5.6543	208.9832	103.40	72.50
150	545.0010	-0.0960	5.7079	213.5359	100.00	72.40
160	544.9639	-0.1028	5.7584	219.0637	96.25	72.20
170	545.0462	-0.0877	5.8059	226.2840	92.55	72.10
180	544.3644	-0.2127	5.8524	235.8634	89.00	71.80

Table C14: Operation-point, noise, and ac simulation results for β=5.9812 at 5.5 V supply voltage.

BJT MODEL	VERT-TYPICAL	VDD=5.5V				β=5.9812
R_0						421.2k
$R_{4,5}$						952.6k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (µA)	OUTPUT NOISE (µV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	545.6254	-0.2052	4.0514	168.4821	109.25	71.10
-40	545.9156	-0.1522	4.1651	154.0857	102.60	72.90
-30	546.1147	-0.1157	4.2828	144.7353	108.57	73.00
-20	546.2406	-0.0927	4.3842	146.4628	114.25	72.80
-10	546.4342	-0.0573	4.4855	150.1188	121.20	73.00
0	546.5733	-0.0319	4.5836	153.9152	124.50	73.00
10	546.8746	0.0232	4.6781	157.6741	120.50	73.00
20	546.9799	0.0425	4.7710	161.6112	142.80	73.00
30	546.7603	0.0023	4.8608	165.7552	129.54	73.00
40	546.7475	0.0000	4.9494	169.7650	130.74	73.00
50	547.0598	0.0571	5.0360	172.7681	119.00	73.00
60	546.6633	-0.0154	5.1185	177.8603	125.60	72.80
70	546.7486	0.0002	5.1990	181.8677	126.50	72.80
80	546.4556	-0.0534	5.2742	186.0871	124.00	72.80
90	546.3112	-0.0798	5.3463	190.2535	121.40	72.60
100	546.1618	-0.1071	5.4142	194.4623	117.75	72.50
110	545.9231	-0.1508	5.4772	198.7589	114.35	72.50
120	545.7999	-0.1733	5.5344	203.1786	110.50	72.20
130	545.5227	-0.2240	5.5932	207.9967	107.20	72.50
140	545.3012	-0.2645	5.6395	213.7750	103.00	72.30
150	544.9998	-0.3197	5.6767	221.3594	100.00	72.14
160	544.4699	-0.4166	5.7068	231.3006	96.00	72.00
170	543.4367	-0.6055	5.7338	243.5159	92.00	71.8
180	541.0617	-1.0399	5.7625	258.2634	88.80	71.00

Table C15: Operation-point, noise, and ac simulation results for β=9.5698 at 5.5 V supply voltage.

BJT MODEL		VERT- HB		VDD=5.5V		β=9.5698
R_0						421.2k
$R_{4,5}$						946.5k
TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	546.4989	-0.1539	4.0535	169.9117	101.5	71.00
-40	546.7258	-0.1123	4.1672	155.3705	102.00	73.00
-30	546.8987	-0.0807	4.2849	145.3409	106.5	73.00
-20	546.9749	-0.0668	4.3861	146.7651	114.00	73.00
-10	547.1351	-0.0375	4.4875	150.3994	121.00	73.00
0	547.3698	0.0054	4.5860	154.0779	123.50	73.00
10	547.4373	0.0177	4.6795	157.9556	119.00	73.00
20	547.3470	0.0012	4.7721	162.0802	133.00	73.00
30	547.3536	0.0024	4.8626	166.0421	136.00	72.80
40	547.3403	0.0000	4.9512	170.0588	135.00	72.70
50	547.0598	-0.0512	5.0360	172.7267	120.00	72.80
60	547.2347	-0.0193	5.1197	178.1572	130.50	72.80
70	547.1167	-0.0409	5.2000	182.2635	128.50	72.30
80	546.4503	-0.1626	5.2743	186.0107	123.80	72.80
90	546.8213	-0.0948	5.3479	190.5885	120.00	72.60
100	546.6543	-0.1253	5.4158	194.7819	117.00	72.50
110	546.4019	-0.1714	5.4788	199.0728	114.80	72.50
120	546.2849	-0.1928	5.5358	203.4698	111.00	72.20
130	545.9862	-0.2474	5.5949	208.2786	107.00	72.20
140	545.7613	-0.2885	5.6421	214.0093	103.40	73.20
150	545.5145	-0.3336	5.6800	221.5897	100.00	72.00
160	545.0020	-0.4272	5.7105	231.4303	96.00	71.80
170	543.8618	-0.6355	5.7373	243.6185	92.50	71.50
180	541.6123	-1.0465	5.7666	258.0697	88.83	71.20

Table C16: Operation-point, noise, and ac simulation results for β=9.5698-HS at 5.5 V supply voltage.

BJT MODEL	VERT- HS	VDD=5.5V	β=9.5698
R_0			410.4k
$R_{4,5}$			952.6k

TEMP (°C)	V_O (mV)	$\Delta V_O/V_O(40°C)$ (%)	IDD (μA)	OUTPUT NOISE (μV(rms))	PSR@DC (dB)	PSR@10kHz (dB)
-50	548.8505	-0.3203	4.0593	166.7812	108.00	71.20
-40	549.2206	-0.2531	4.1734	152.2169	102.00	73.00
-30	549.4757	-0.2067	4.2911	144.9924	110.00	72.80
-20	549.6538	-0.1744	4.3925	147.4754	114.50	72.80
-10	549.9222	-0.1256	4.4942	151.3218	120.00	73.00
0	550.1165	-0.0904	4.5927	155.2127	121.40	73.00
10	550.4337	-0.0327	4.6870	159.0691	121.40	73.00
20	550.4287	-0.0337	4.7796	163.2145	141.50	73.00
30	550.5331	-0.0147	4.8706	167.2094	150.00	72.80
40	550.6140	0.0000	4.9591	171.3504	134.00	72.20
50	550.6598	0.0083	5.0452	175.4593	128.00	72.20
60	550.6353	0.0039	5.1281	179.5132	130.40	72.80
70	550.6662	0.0095	5.2089	183.7770	123.00	72.80
80	550.6147	0.0001	5.2848	187.9993	122.80	72.50
90	550.5455	-0.0124	5.3569	192.0937	120.00	72.60
100	550.4869	-0.0231	5.4247	196.4688	116.85	72.50
110	550.2768	-0.0612	5.4873	200.9975	113.40	72.50
120	550.2689	-0.0627	5.5427	205.6696	110.50	72.20
130	550.1337	-0.0872	5.5967	211.6601	108.00	72.20
140	549.7643	-0.1543	5.6454	216.5640	103.50	72.50
150	549.5629	-0.1909	5.6617	229.5648	100.00	72.00
160	548.5987	-0.3660	5.6832	242.0743	96.50	71.50
170	546.7462	-0.7025	5.7035	256.9046	92.50	71.20
180	542.9884	-1.3849	5.7262	274.4084	88.70	70.80

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