6-BIT FLASH ANALOG-TO-DIGITAL CONVERTER

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Submitted to the Institute of Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Master of Science
in
Electrical & Electronics Engineering

Yeditepe University
2010

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ABSTRACT

6-BIT FLASH ANALOG-TO-DIGITAL CONVERTER

The purpose of this thesis is to design a converter with low power consumption and high sampling rate using a different structure from conventional flash analog-to-digital converters. The designed novel voltage comparator circuit and the following structure enable to overcome the speed problems of conventional voltage comparators. Moreover, the ROM can be driven without encoder circuit with the help of decision circuit.

As in conventional Flash ADC designs, voltage comparator circuits compare input voltages against reference voltages in this designed Flash ADC. However, instead of producing a digital signal, voltage comparators produce a current at the output. The current has the highest value in only one voltage comparator. This current is detected by a current comparator which produces a digital “1”. The outputs of voltage comparators can have very close values at the boundaries of reference voltages. Therefore, two current comparators can produce “1” at the same time. In this situation, decision circuit determines the highest current by the help of latch circuit. The ROM circuit can be driven without producing thermometer code and encoder circuit.

As a result, 6-bit, 1GS/s Flash ADC is designed in TSMC 180nm CMOS for 1.8V operation. This converter is arranged to operate between -40°C and 120°C. All design steps and details are shown in this thesis. Verification of designed circuits and all system has been carried out by simulations. Also, this work is compared against some of the Flash ADC converters which have same technology and similar specifications, the results are presented in this thesis.

ÖZET

6-BIT FLAŞ ANALOG-DIJITAL ÇEVİRİCİ

Bu tezde geleneksel Flaş Analog-Dijital çeviricilerden farklı bir yapı kullanılarak daha yüksek hızlarda örnekleme yapabilen ve daha az güç tüketen bir çevirici tasarlamak amaçlanmıştır. Farklı gerilim karşılaştırıcı devresi ve sonrasında kullanılan yapı, geleneksel çeviricilerde karşılaştırıcı devresinin neden olduğu hız problemlerinin aşılmasını ve kodyayıcı devresine gerek kalmaksızın ROM devresini sürebilmesini sağlar. Bu sayede daha yüksek hızlarda çalışabilen ve kodlayıcı devresine ihtiyaç duymayan çevirici tasarlanmıştır.

Geleneksel tasarımlarda olduğu gibi, bu tasarımda da gerilim karşılaştırıcı devreleri, giriş gerilimini referans gerilimleri ile karşılaştırır. Fakat, farklı olarak çıkışta dijital bir işaret değil, bir akım üretir. Tek bir gerilim karşılaştırıcıda en yüksek değere sahip olan bu akım bir akım karşılaştırıcı sayesinde tesbit edilir ve bu akım karşılaştırıcısının çıkışından "1" elde edilir. Sınır noktalarında gerilim karşılaştırıcılarının akımları çok yakın değerlere sahip olabilir ve iki tane akım karşılaştırıcı aynı anda dijital "1" üretebilirler. Bu durumda karar devresi bir latch devresi yardımıyla en büyük değere sahip akımı belirler. Bu sayede termometre kodu oluşturulmadan ve kodlayıcı devresine gerek kalmadan Flaş Analog-Dijital çeviricinin çıkışında bulunan ROM sürülebilir.

Bu yapı kullanılarak 6-bit çözünürlüğünde, 1GHz frekansında örnekleme yapabilen, 1.8 V ile beslenen bir Flaş Analog-Dijital çevirici TSMC 180nm CMOS teknolojisi ile tasarlanmıştır. Bu çeviricinin -40°C ile 120°C aralığında çalışması için gerekli ayarlamalar yapılmıştır. Bütün tasarım adımları ve detayları anlatılmış, tasarlanan devrelerin ve tüm sistemin similasyon sonuçları gösterilmiştir. Bu çalışma, literaturde yer alan aynı teknolojiyle tasarlanmış ve benzer özelliklerdeki bazı Flaş Analog-Dijital çeviriciler ile karşılaştırılmıştır.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS / ABBREVIATIONS

D	Value of digital output code
$F_{sampling}$	Ideal sampling frequency
F_{max}	Highest frequency of the sampled signal
g_m	Transconductance
k	Boltzman constant
q	Magnitude of electrical charge
Q_e	Quantization error
T	Temperature
V_{LSB}	Least significant bit in volts
V_{REF}	Reference voltage of resistor ladder
V_T	Thermal voltage
V_{TH}	Threshold voltage

ADC	Analog-to-Digital Converter
BW	Bandwidth
DNL	Differential nonlinearity
LSB	Least significant bit
MSB	Most significant bit
T/H	Track-and-Hold

1. INTRODUCTION

Analog-to-digital conversion is an electronic process in which a continuously variable analog signal is changed, without altering its essential content, into binary numbers. In spite of the fact that, digital systems do not have the same amount of accuracy as analog signals, they need to be converted to digital signals. The benefit is that, digital signals can be manipulated, processed faster, and recorded in smaller domain. Nowadays, very high speed analog-to-digital converters are necessary for many applications which need high sampling rate and resolution such as data recording and wireless communication. Flash ADCs are the fastest way of converting an analog signal to a digital signal. Flash converters have high conversion rates such as 1Gsample/second, and resolution is generally limited to 8-bits, and they consume large amount of power in comparison with other types of analog-to-digital converters.

Some published performance metrics of flash ADCs are given in Table 1.1. Presently, the fastest CMOS ADC is a 6-bit, 3.5 GS/s, 0.9 V, 98 mW Flash ADC in 90nm CMOS [1]. There are higher-speed ADCs up to 24 GS/s, but these ADCs are fabricated in SiGe or BiCMOS [5].

Table 1.1. Performance metrics of some fabricated Flash ADCs

Reference	Deguchi,Suwa[1]	Wei,Chio [2]	Scholtens[3]	Choi, Abidi[4]
Technology	90 nm CMOS	90 nm CMOS	180 nm CMOS	350 nm
Supply Voltage	0.9 V	1.2 V	1.95 V	3.3 V
Resolution	6 bit	6 bit	6 bit	6 bit
Sample Rate	3.5 GS/s	1.2 GS/s	1.6 GS/s	1.3 GS/s
Power	98 mW	41 mW	328 mW	545 mW

In this thesis, a novel 6-bit, 1 GS/s Flash ADC is designed in TSMC 180 nm CMOS technology for 1.8 V operation. The novelty is in the comparator architecture, which eliminates hardware overhead of thermometer coding. In the design procedure, the most

important specification has been sampling speed, so all blocks are designed for maximum speed. This converter includes (a) double sampling track and hold circuit based on source follower, (b) resistor string, (c) preamplifier, (d) voltage comparator, (e) current comparator and ROM circuits. All these circuits are described with their design procedure and their simulated verifications are presented. Top level system performance is also evaluated with simulation.

2. FUNDAMENTALS OF ANALOG-TO-DIGITAL CONVERSION

2.1. TYPICAL FLASH ADC ARCHITECTURE

A typical flash ADC as shown in Figure 2.1 includes a resistor string, a track-hold (T/H), and comparator, decoder circuits. “N” bit converter contains 2^N resistors to divide the reference voltage into 2^N-1 quantization levels. Each quantization voltage level is applied to a different comparator. 2^{N-1} comparators compare each quantization voltage levels against input voltage and results in a thermometer code at the outputs of the comparator. When comparator’s analog input voltage is higher than the voltage on resistor string, it produces a “1”, and otherwise the comparator creates a “0”.

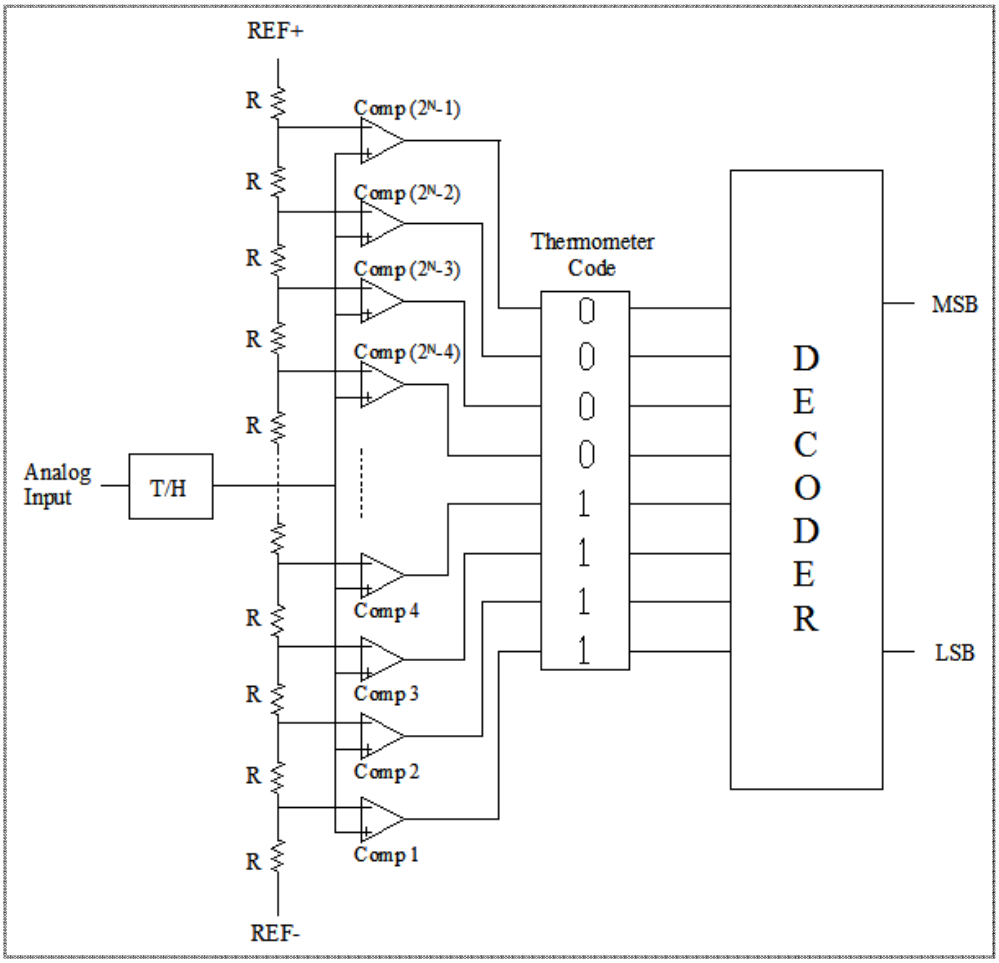

Figure 2.1. A Typical Flash ADC Architecture

Therefore, a thermometer code shows zeros and ones as shown in Figure 2.1. The point where the code changes from ones to zeros is the point where the input signal becomes smaller than the respective comparator reference voltage levels. Then, a digital thermometer decoder circuit converts the compared data into an N-bit digital word.

Advantage of this conversion is the speed. However, these converters have large area and high power consumption because of 2^N-1 comparators. The speed is limited by the switching time of the comparators and the digital logic. Also, other important criterion is accuracy. It depends on the matching of the resistor string and the input offset voltage of the comparators.

2.2. TRACK-AND-HOLD (T/H) CHARACTERISTICS

Track-and-hold (T/H) circuit is the entry circuit for ADCs. T/H circuit tracks the analog signal during the time required to sample the signal, and holds it until ADC completes all processing on this signal. Absence of this component may cause the degradation of signal during digitization and it causes accuracy problems. Therefore, T/H is a critical part of ADC to avoid the degradation of signal. Speed and accuracy of ADC can be limited by T/H.

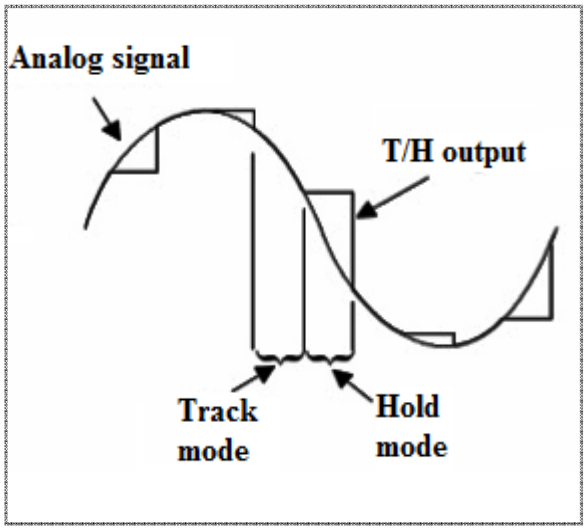

Figure 2.2. The output of a T/H circuit [6]

The output of track-and-hold circuit is shown in Figure 2.2. In track-and-hold circuit, a finite period of time is needed for the sampling and analog signal can continue to vary in this time. After sampling mode, the hold mode takes place until the next period.

A track-and-hold circuit is shown in Figure 2.3. In this circuit, when switch S1 is turned on, tracking command is issued and analog signal appears at the output. A time is required for the analog input signal to appear at the output of the T/H circuit within a specified tolerance. This time is known as "acquisition time" as shown in Figure 2.4. The worst-case happens for the acquisition time, when the input signal suddenly changes from zero to maximum voltage. Track-and-hold circuits use amplifiers or buffers, therefore acquisition time is the function of this buffer's specifications. Amplifier's slew rate and phase margins are the two critical parameters which determine "overshoot", which causes longer settling time and longer acquisition time. Also T/H circuits error tolerance extremely depends on amplifier's offset, gain error and linearity.

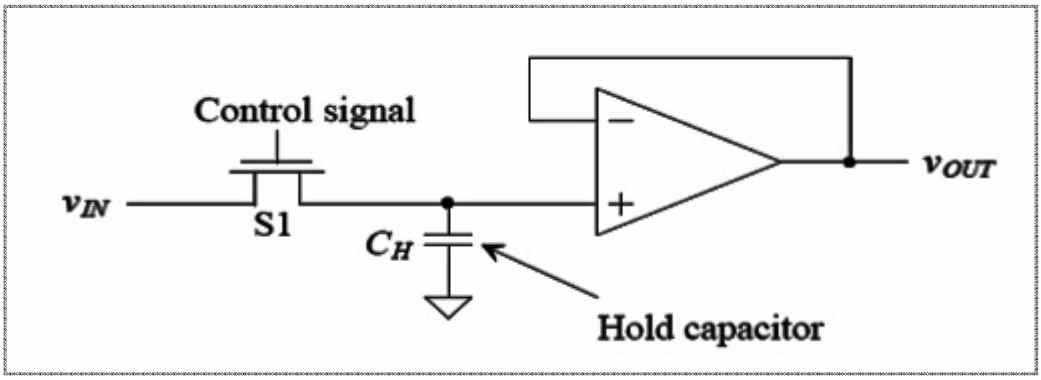

Figure 2.3. Track-and-hold (T/H) circuit [6]

Hold mode occurs when the S1 switch is turned off in the T/H circuit in Figure 2.3. The voltage on C_H capacitor is protected until S1 switch is turned on and the output is held in this voltage level. Also this mode has some specific errors. Pedestal error occurs as a result of charge injection and clock feedthrough. These errors and leakage currents cause voltage changes at the output as seen in Figure 2.4 [6]. Some methods will be shown through the following sections which are used for eliminating these errors.

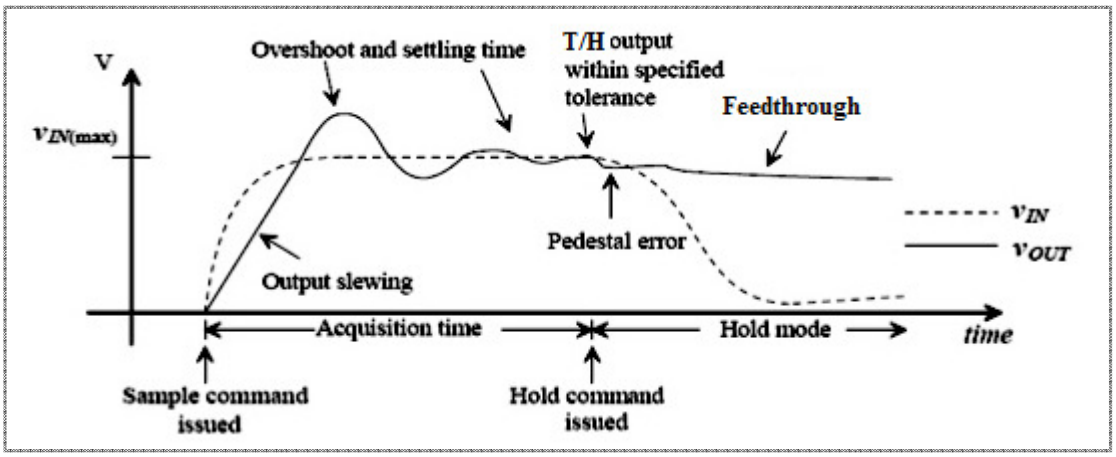

Figure 2.4. Typical errors in T/H [6]

2.3. ANALOG-TO-DIGITAL CONVERTER SPECIFICATIONS

2.3.1. Sampling Rate and Resolution

The analog signal is continuous and infinite valued, whereas the digital signal is discrete with respect to time and quantized.

The accuracy of the digitized signal is based on two factors of the converter: the sampling rate and the resolution. The difference between an analog signal and its digital counterpart diminishes with the increasing resolution and sampling rate.

Sampling rate indicates how many samples the ADC can process in a time unit and Nyquist Criterion defines how fast the sampling rate must be in order to represent an analog signal accurately. Nyquist Criterion is

$$F_{sampling} = 2F_{\max} \tag{2.1}$$

where $F_{sampling}$ is the ideal sampling frequency required to accurately represent the analog signal and F_{max} is the highest frequency of the sampled signal.

Resolution is the other important parameter to accurately convert analog signal to digital signal. The resolution of the converter specifies the number of quantization levels, which is produced over the range of analog values. It is defined in bits. Resolution or quantization level should be determined according to application. Each application has its own requirements.

2.3.2. Quantization Error

In analog-to-digital conversion, an analog signal with an infinite number of values has to be quantized into an N-bit digital word. Converter needs to detect changes in the input signal on the order of 1 part in 2^N, which is the number of quantization level. Since analog signal is an infinite valued quantity whereas the output is discrete valued, an error occurs as a result of quantization. The difference between the actual analog input and the value of output given in voltage is described as quantization error, Q_e. Its formulation is

$$Q_e = V_{IN} - V_{staircase} \tag{2.2}$$

and $V_{staircase}$ is

$$V_{staircase} = D.\frac{V_{REF}}{2^N} = D.V_{LSB} \tag{2.3}$$

where D is the value of digital output code, V_{REF} is the reference voltage of resistor ladder, i.e. it is the voltage range of total quantization levels. The least significant bit (LSB) refers to the rightmost bit in the digital word and V_{LSB} is the value of least significant bit in volts.

Transfer curve of an ideal 3-bit ADC is shown in Figure 2.5.a [6] and its quantization error is shown in Figure 2.5.b [6]. Figure 2.5.b is produced to subtract analog-input signal from output (staircase) in accordance with (2.2).

In Figure 2.5.b, quantization error can be between 1 LSB and 0 LSB. It is centered about ½ LSB. If this centered point shifted to zero, the error would be at most ± ½ LSB.

This can be handled by shifting transfer curve ½ LSB to left. This is an ideal ADC quantization error.

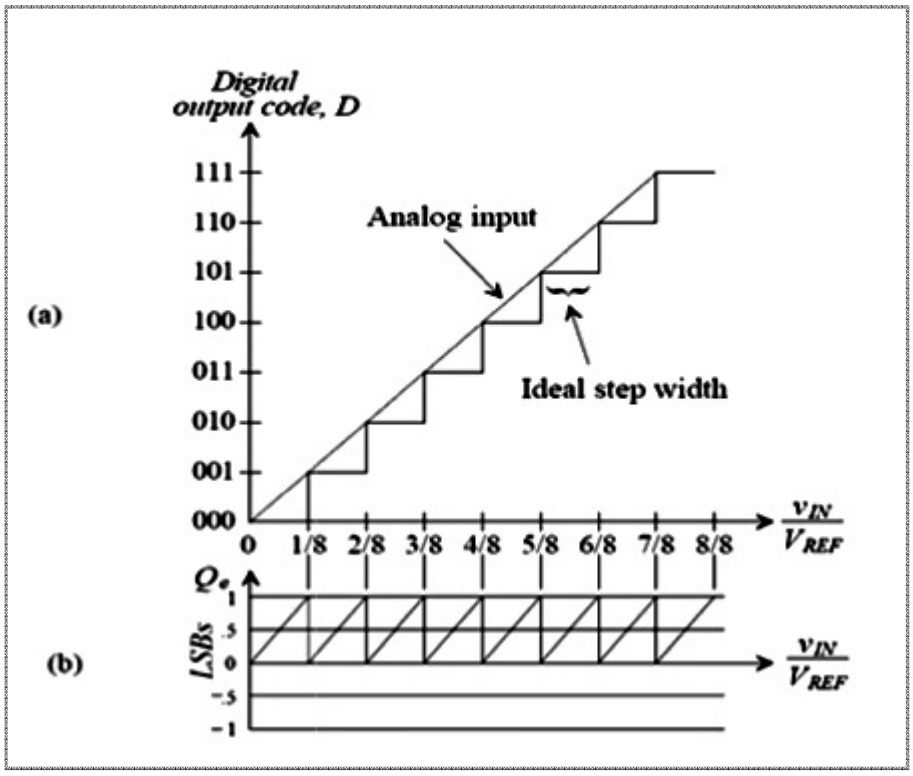

Figure 2.5. (a) Shows transfer curve of an ideal 3-bit ADC (b) shows its quantization error [6]

2.3.3. Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the actual step width of a non-ideal converter and the ideal step width. Its formulation is

$$DNL = Actual\ step\ width - Ideal\ step\ width \tag{2.4}$$

The step widths can be expressed in unit of volts or LSB. So, the ideal step width is given by

$$V_{idealstepwidth} = \frac{V_{REF}}{2^N} = 1LSB \tag{2.5}$$

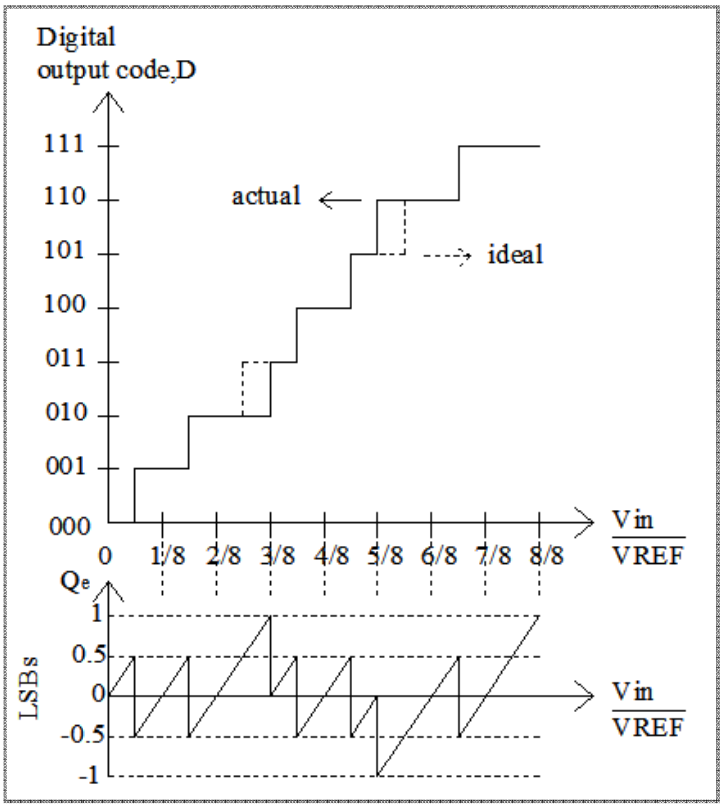

Figure 2.6. Shows the transfer curve for a non-ideal 3-bit ADC and quantization error illustrating differential nonlinearity [6]

The DNL of a converter can be calculated from (2.4) as shown in Figure 2.6 [6]. Since ideal step width of the 000 transition is ½ LSB, then DNL_0=0. The step widths associated with 001 and 100 are equal to 1 LSB; therefore, DNL_1 and DNL_4 are zero. Other step widths are not equal to ideal values. DNL_2 and DNL6 is 0.5 LSB. DNL_3 and DNL_5 is -0.5 LSB. Also Figure 2.6. shows relation between DNL and quantization error. When DNL increases, the quantization error increases. They are directly related to each other.

2.3.4. Missing Codes

In any analog-to-digital converter processing, when a DNL is equal to -1 LSB, total width of the corresponding step is completely missing. This situation is called as “missing code”. As shown in Figure 2.7 [6], 101 code is missing code and its DNL is -1 LSB. Also 010 code has 2 LSB and DNL is equal to +1 LSB, but does not have missing code.

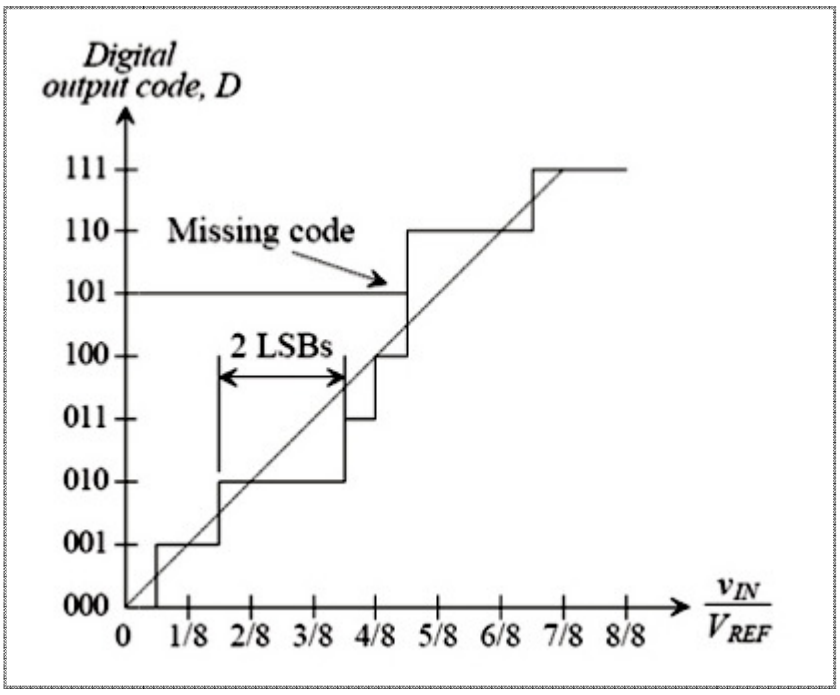

Figure 2.7. Transfer curve of a non-ideal 3-bit ADC with missing codes [6]

2.3.5. Offset and Gain Error

If there is a difference between the value of the first code transition and the ideal value of ½ LSB, this difference is called “offset error”. As shown in Figure 2.8 offset error has a constant value, and when offset error is ignored, the quantization error becomes ideal [6].

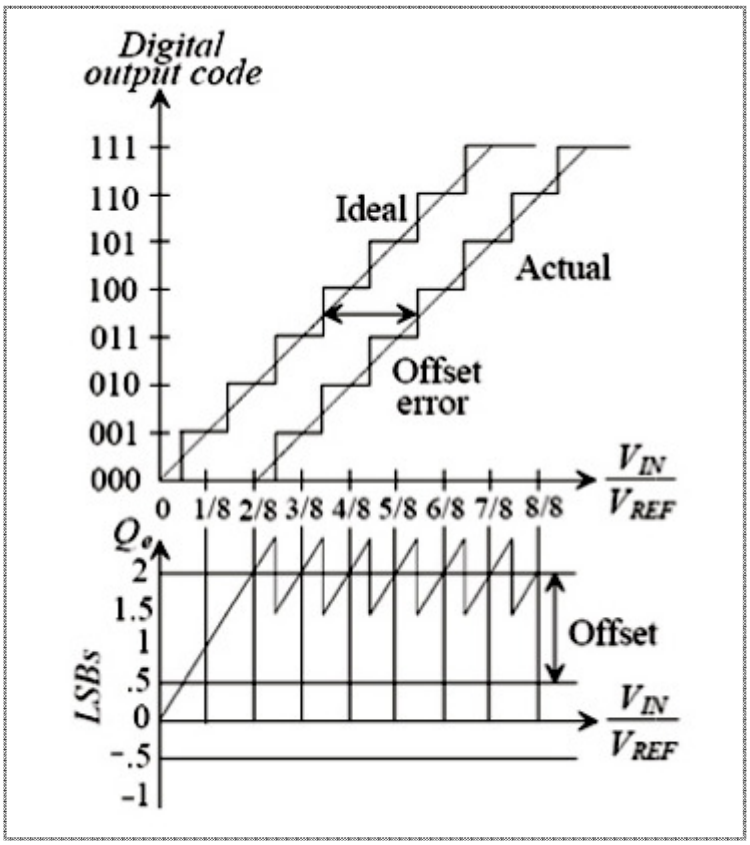

Figure 2.8. Transfer curve illustrating offset error [6]

Gain error is the difference in the slope of a straight line drawn through the transfer characteristic of the non-ideal converter and the slope of 1 which is slope of an ideal ADC as shown Figure 2.9 [6]. This error is also known as “scale factor error”.

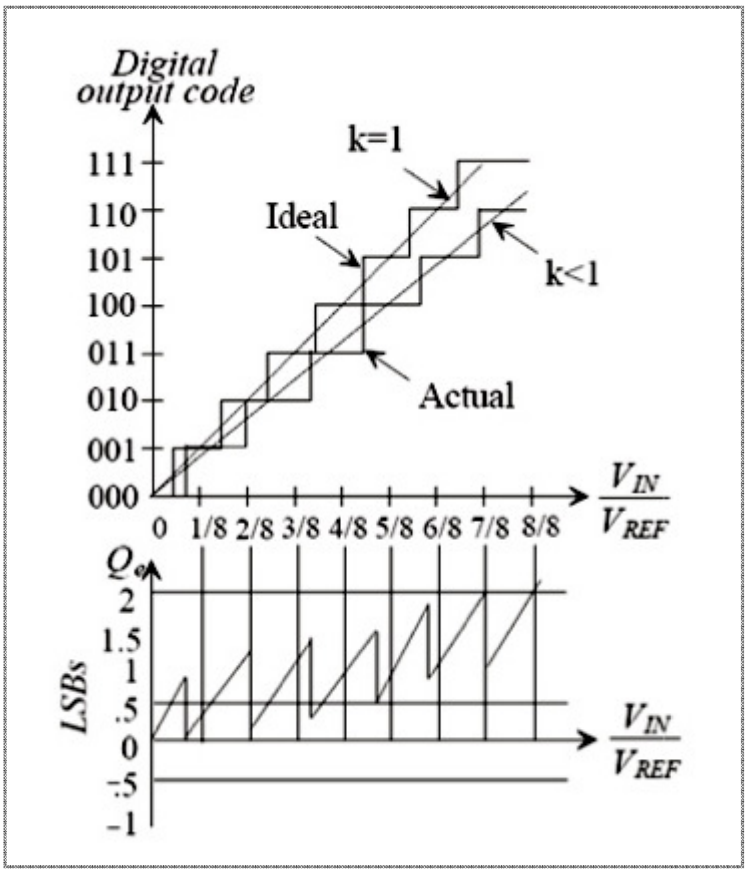

Figure 2.9. Transfer curve illustrating gain error [6]

Figure 2.9. shows a non-ideal analog-to-digital converter which has gain error, and its quantization error gets larger with increasing transitions

2.3.6. Aliasing

Aliasing would occur when Nyquist Criterion is ignored. Nyquist Theorem requires that the signal must be sampled with at least two times higher frequency than the actual signal. If the sampling frequency is less than that amount of sampling frequency, aliasing occurs.

An example of aliasing is shown in Figure 2.10 [6]. An analog signal is being sampled with ignoring Nyquist theorem. Sampling frequency is taken smaller than the frequency of actual signal. Therefore, totally different signal is sampled.

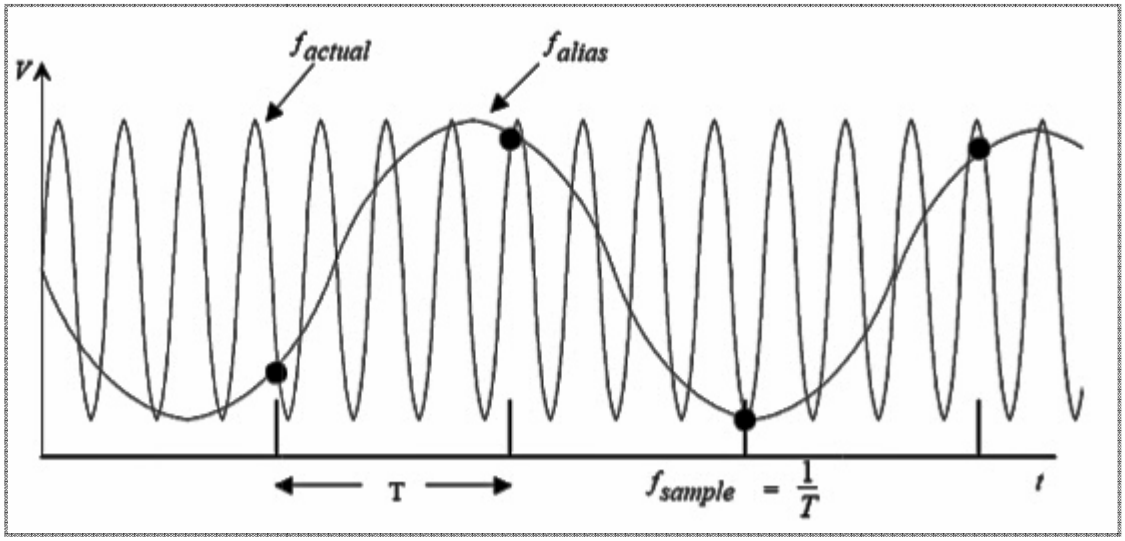

Figure 2.10. An example of aliasing is shown, the reason of which is choosing a sampling frequency which is smaller than twice the frequency of the actual signal [6]

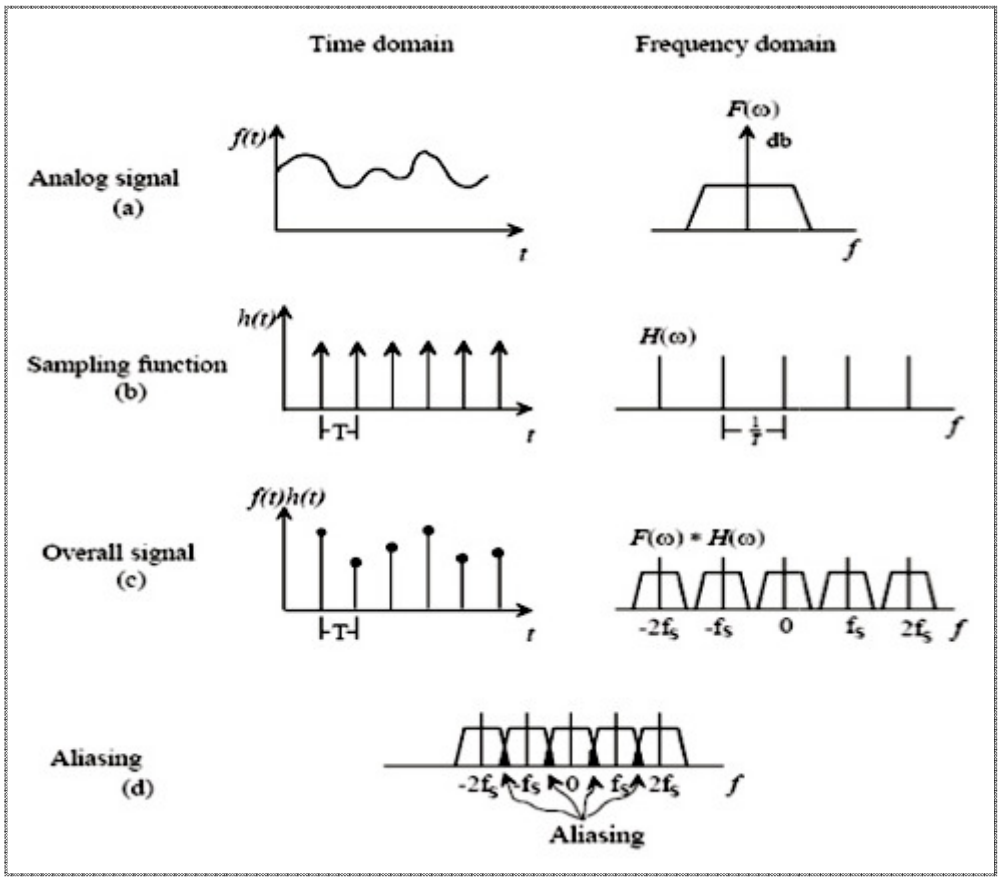

Figure 2.11. Examination of aliasing in time domain and frequency domain [6]

Frequency domain analysis can be more suitable to understand aliasing. An analog signal is shown in time domain and frequency domain in Figure 2.11a [6]. This analog signal is sampled with the sampling function which is shown in Figure 2.11b [6]. Sampling occurs with period T, and its frequency domain response is impulses with value of 1 and 1/T frequency. Impulses of sampling signal is multiplied by the amplitude of analog signal, and sampled signal occurs as shown Figure 2.11c [6]. If sampling time increases that means sampling frequency decreases and impulses in the frequency domain become closer. This results in Figure 2.11d, which illustrates the aliasing as signals are beginning to overlap [6].

Aliasing can be eliminated by sampling at higher frequencies and by filtering the analog signal before sampling and removing any frequencies that are greater than one-half the sampling frequency.

3. PROPOSED FLASH ADC

Conventional Flash ADCs produce thermometer code, which needs to be encoded to drive ROM. Therefore, proposed Flash ADC does not produce thermometer code and directly drives ROM. The current comparator and decision circuit is designed to eliminate the encoder circuit. The objective of this stage is to handle maximum sampling rate. Fully differential 6-bit 1 GS/s flash analog-to-digital converter is designed for this purpose in TSMC 180 nm CMOS technology. As seen in Figure 3.1 architecture of flash converter can be defined in four stages;

1. Track-and-Hold circuit,
2. Resistor String, Preamplifier and Voltage Comparator,
3. Current Comparator and Decision circuit,
4. ROM.

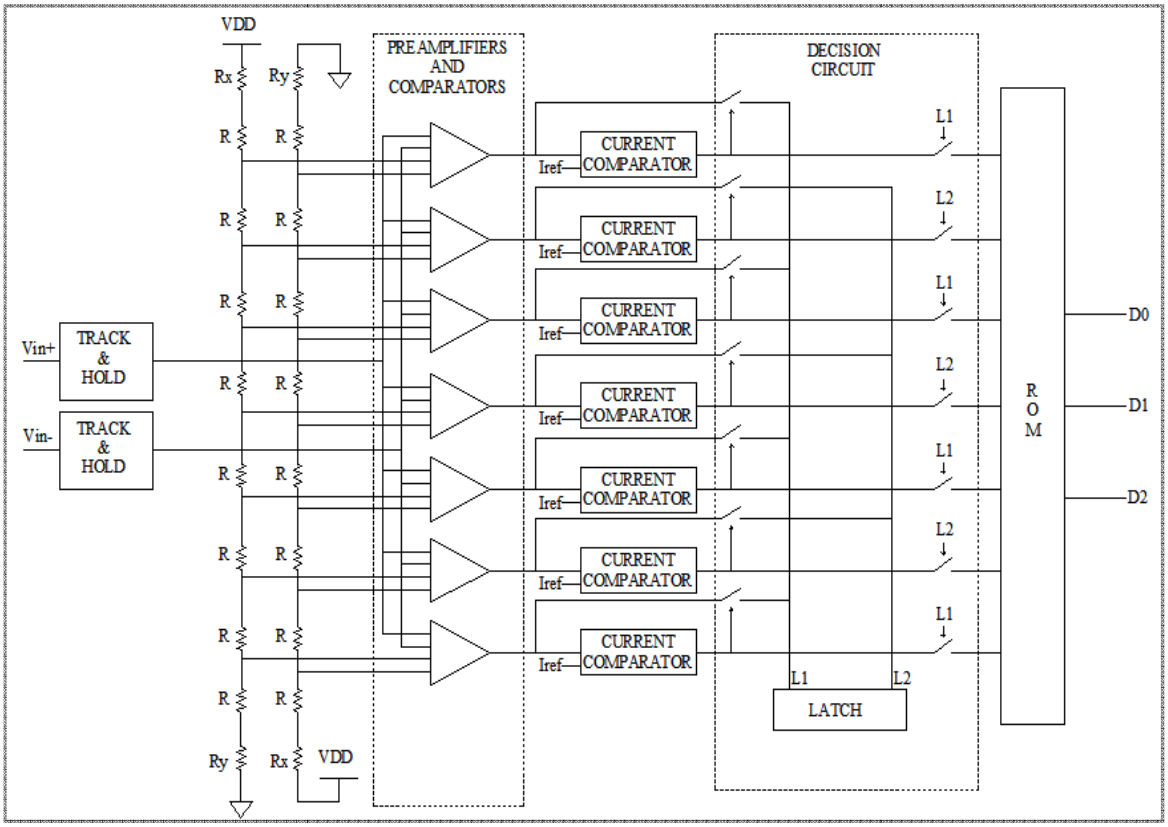

Figure 3.1. Proposed Flash ADC Architecture

The track-and-hold or T/H circuit is used in the front-end element for analog-to-digital converter. Differential analog input signals are entered to T/H circuit which samples signals at 500 MHz clock frequency, but each T/H circuit block contains two identical circuits which are operating with inverted clocks, which results in signal sampling at 1GS/s. These sampled signals, which are the outputs of T/H circuits, are input of preamplifiers.

Resistor string determines reference voltages of the preamplifier. Resistor ladder is built by 15 Ω resistors. Value of resistors has critical importance, because sampled signals at 1 GHz clock frequency can cause ripples on reference voltages. If the resistor's values are higher than 20 Ω, these ripples' peak values become too high and cause longer settling time for providing correct reference voltages. That may lead to accuracy problems at high speed conversion as 1 GS/s.

Preamplifier's inputs are reference voltages from resistor string and sampled voltages from track-and-hold circuit. The outputs of preamplifiers are the inputs of voltage comparators. Preamplifier's cut-off frequency is arranged 2.2 GHz to give response to input voltage changes at 1 GHz. Another important parameter is the input capacitance of preamplifier, as it affects the resistor strings voltage ripples and track-and-hold settling time. Also, differential structure of proposed Flash ADC eliminates errors which are caused by noise.

Voltage Comparator is the novel part of this design. Inputs of voltage comparator are outputs of the preamplifiers circuits. Voltage comparator output is current which is produced with respect to outputs of preamplifier. The produced current is the input of current comparator circuit which compares it with a reference current. The current comparator gives "1", when input current is higher than the reference current; otherwise it gives "0". In this topology, only one or two "1"s are produced. If the input voltage is very close to any reference voltage, these nearest two voltage comparators can create two higher currents than the reference current. So, two current comparators give "1". After topology creates two "1"s, decision circuit determines the highest current by mirroring these two currents to latch circuit. Therefore, the smaller current will be eliminated and decision circuit produce only one "1". This "1" drives ROM circuit. So, the analog input signal is

converted to digital signal without thermometer coding. Voltage comparator, current comparator and decision circuit's details will be presented in next chapters.

At the output stage, D type flip-flop is used to hold output of ROM in exactly 1ns. Input waveforms of ROM and D-type flip-flop are shown next chapters.

3.1. PROOF OF VOLTAGE COMPARATOR CONCEPT

This thesis is based on a novel voltage comparator structure which eliminates hardware overhead of thermometer coding. The novel comparator schematic is given in Figure 3.2. Some simulations and formulations will be given below for proof of the concept.

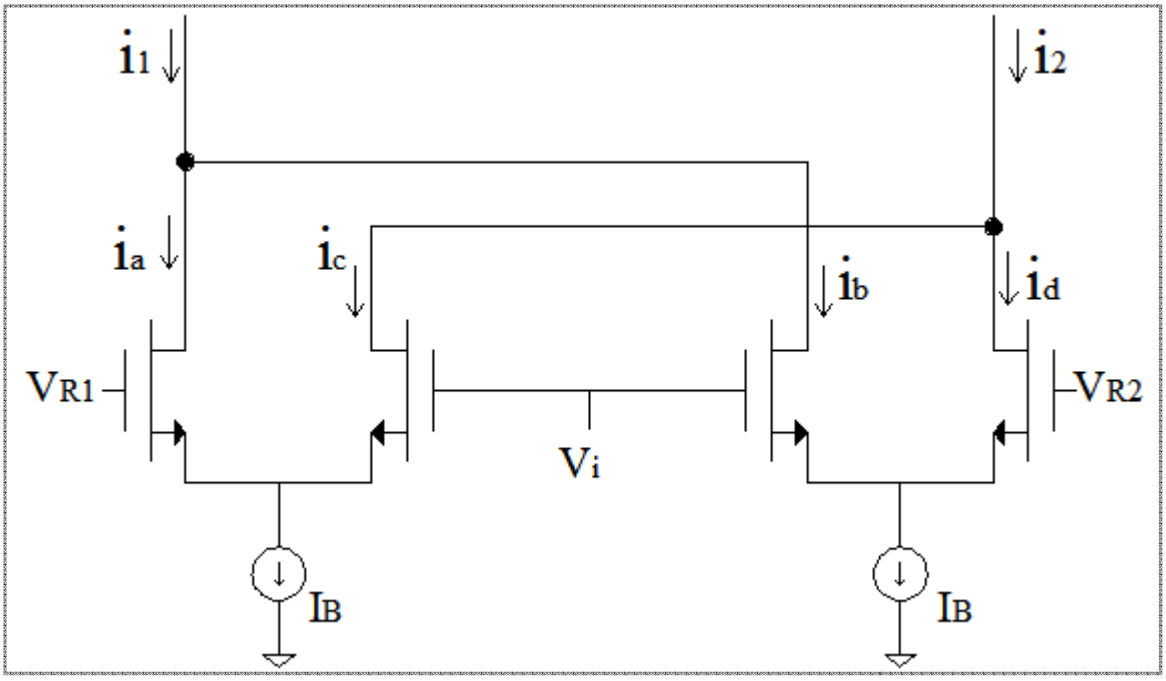

Figure 3.2. Schematic of proposed comparator

The voltage comparator contains two bias current sinks; I_B. V_{R1} and V_{R2} are reference voltages and input voltage is Vi. i_1 is the sum of currents i_a and i_b, i_2 is the sum of currents i_c and i_d. A DC simulation is run to understand the circuit's response. Input signal is swept from 0.4 V to 1.6 V and references are chosen as V_{R1}=1 V and V_{R2}=1.2 V. When

input voltage is 0.4 V, current i_c and i_b are zero. So, all currents are sunk by i_a and i_d. Input voltage becomes closer to V_{R1}, i_c starts to increase and i_a starts to decrease, same response for i_b and i_d is seen when input voltage comes closer to V_{R2}. i_c and i_a intersect when input voltage is equal to reference voltage V_{R1}. i_b and i_d intersect when input voltage is equal to reference voltage V_{R2}. Responses of all these currents are shown in Figure 3.3.

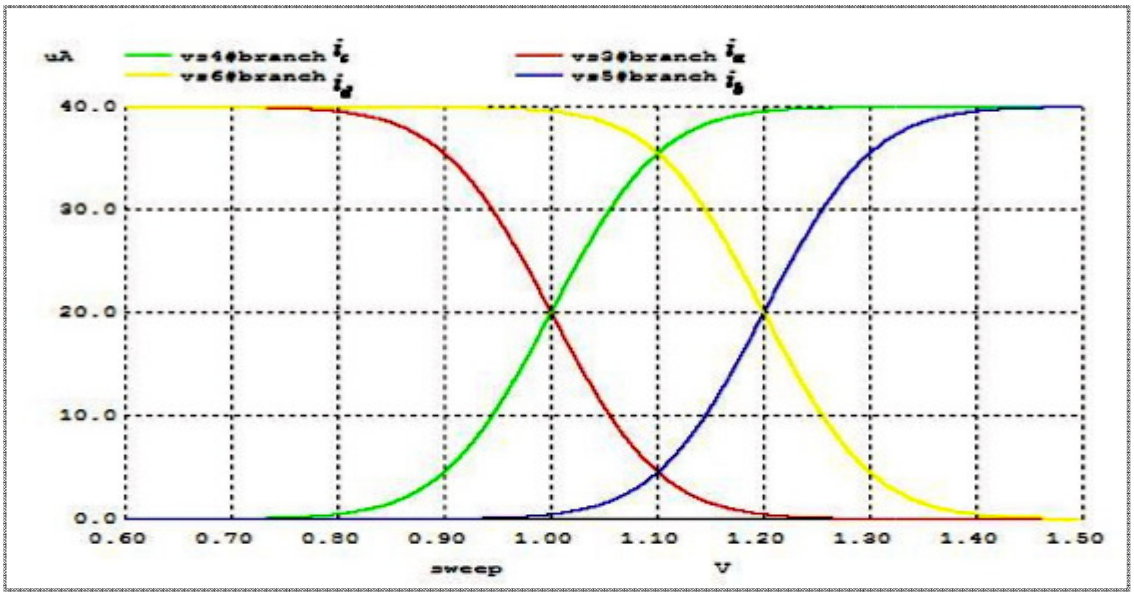

Figure 3.3. DC simulation to recognize currents (i_a, i_b, i_c, i_d) behavior [24]

At the same simulation, i_1 and i_2 occur as shown in Figure 3.4. Current i_2, which is shown with green line, increases in the related reference points. This property is used in this flash analog-to-digital converter. If input voltage is between the reference points of the voltage comparator, that comparator creates the highest current according to other voltage comparators. This will determine the correct comparator and correct output.

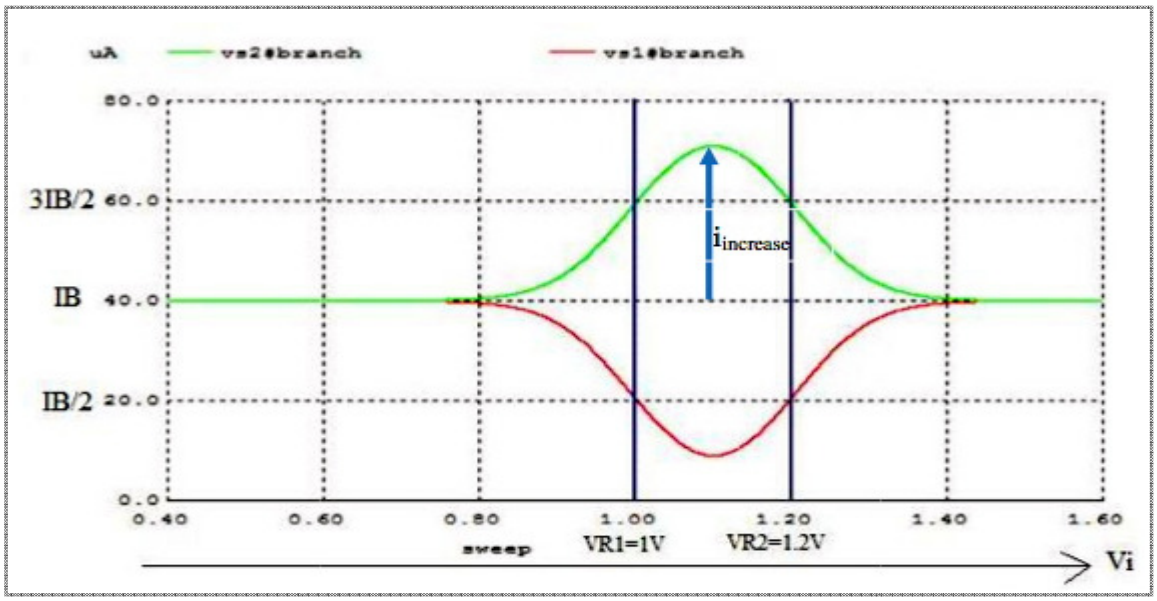

Figure 3.4. DC sweep of input voltage and currents i_1 and i_2 [24]

$i_{increase}$ shows the current increase in Figure 3.4, it can be formulate as shown below;

$$i_{increase} = \frac{I_B}{2} + \frac{g_m}{2}(V_{R2} - V_{R1} - (V_{GS} - V_{TH})) \tag{3.1}$$

V_{TH} is the threshold voltage and g_m is can be written as

$$g_m = \frac{2I}{(V_{GS} - V_{TH})} \tag{3.2}$$

$i_{increase}$ becomes

$$i_{\text{increase}} = \frac{I_B}{2} \cdot \frac{V_{R2} - V_{R1}}{V_{GS} - V_{TH}} \tag{3.3}$$

In this flash analog-to-digital converter topology, voltage comparator's current, which is increasing with related reference voltage, will be used. Therefore, just right branch of the voltage comparators will be mirrored for other circuits of Flash ADC.

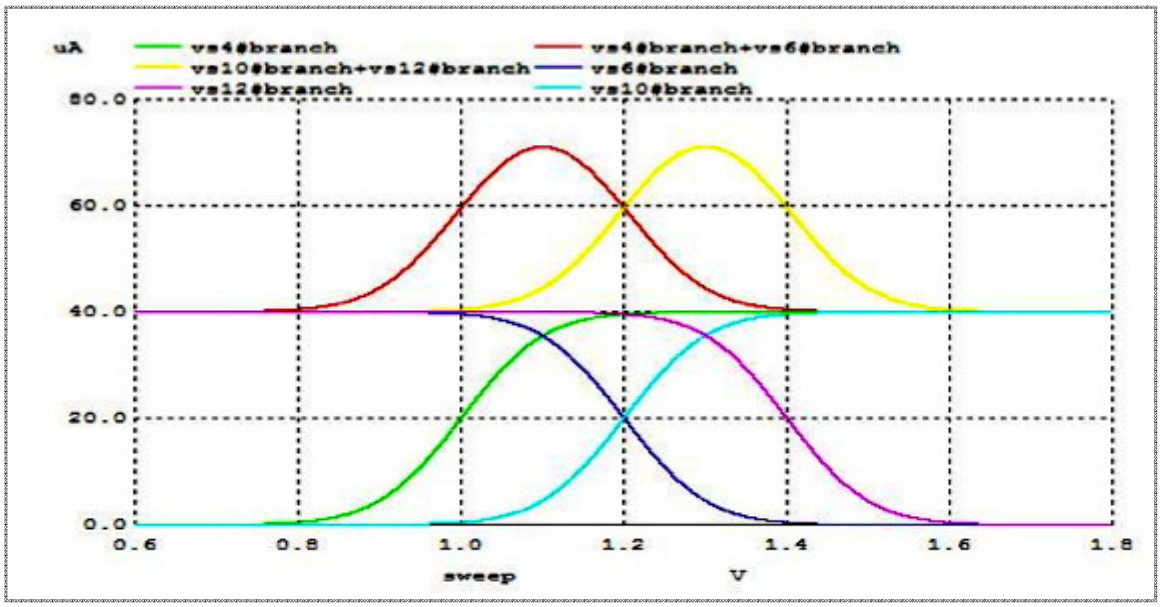

Figure 3.5. Right branch currents of two comparators which reference voltages difference is chosen 200 mV [24]

Other important subject is voltage differences for comparators. In these simulations the difference "V_{R2}-V_{R1}" is chosen as 200 mV. Figure 3.5 shows another simulation which has two comparators and their reference voltage difference is 200 mV and right branch of comparators' currents are shown with red line and yellow line. Reference points are 1 V, 1.2 V and 1.4 V. Difference of currents is observable. However, in this converter design 1LSB is nearly 20 mV, so reference voltages difference is 20 mV. If same simulations are run with changing the reference voltage difference to 20 mV, this simulation results are given in Figure 3.6. As shown in Figure 3.6, difference of voltage comparator's currents is not distinguishable. Also, this situation is not usable to detect the highest current to determine correct output.

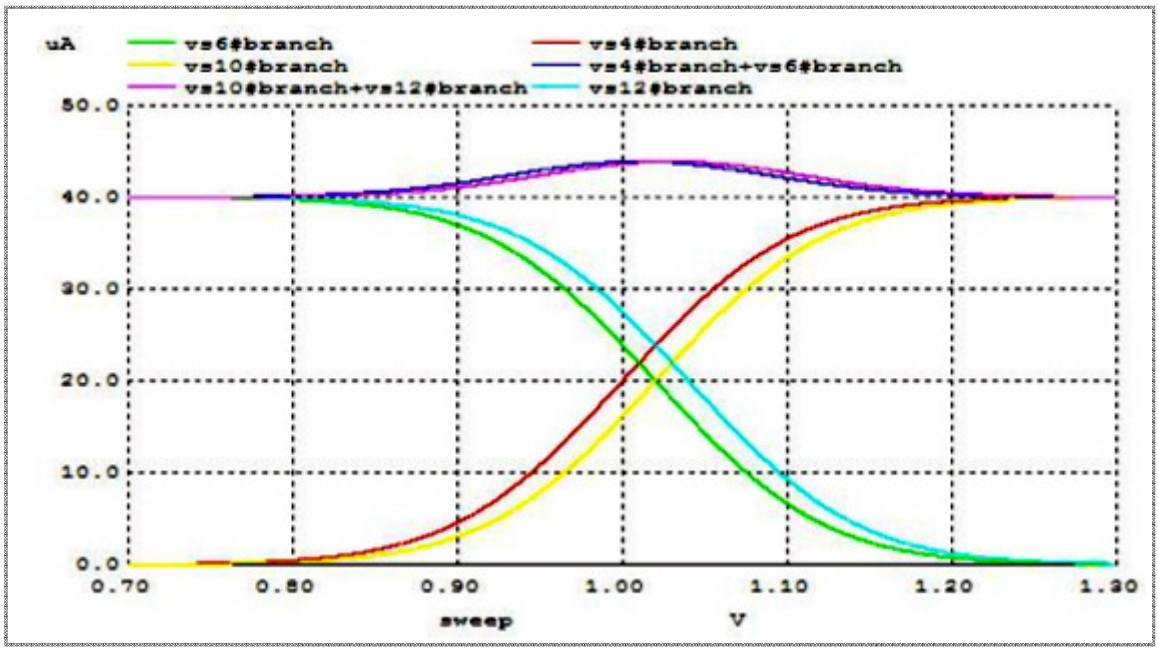

Figure 3.6. Right branch currents of two comparators which reference voltages' difference is chosen 20 mV [24]

As seen obviously in simulations, this comparator structure is need preamplifier circuit.

3.2. PREAMPLIFIER DESIGN

Preamplifier circuit includes five stages, first of which is differential amplification stage, that is shown in Figure 3.7. It amplifies the difference between differential input and the differential reference. The differential input, which is Vip - Vin, is fed from T/H circuit. Differential reference, which is Vrp - Vrn, is fed from resistor ladder.

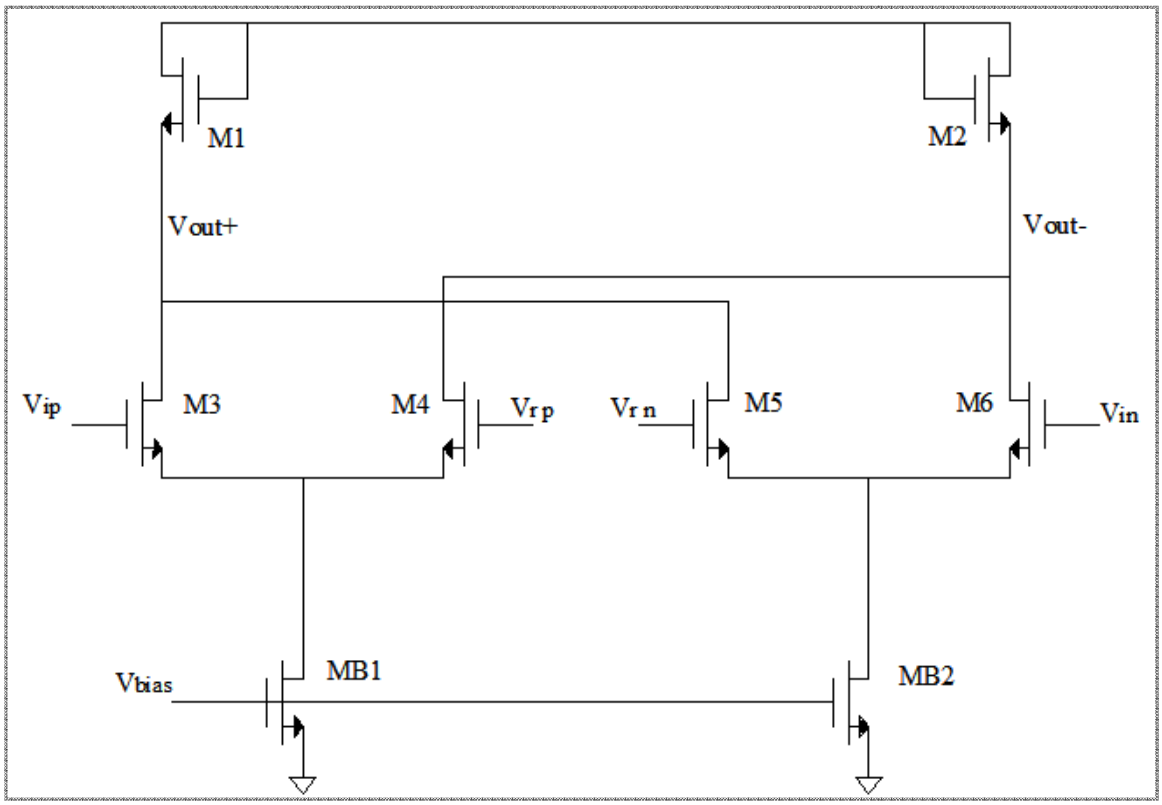

Figure 3.7. Differential Amplifier

The input amplifier sizing is a trade–off between bandwidth BW and gain [7, 8]. Driver transistors (M3-to-M6) with longer channel widths cause lower BW and high gain. M1 and M2 also affect the gain of the amplifier. If these transistors' length increases, the bandwidth of amplifier increases as well.

Input stage of the preamplifier design is shown in Figure 3.7. The objective of this stage is to handle maximum bandwidth. The gain is achieved from other stages of amplifier circuit. Therefore, the widths of amplifier's driver transistors are chosen as 0.8 µm; the width and length of M1 and M2 are 1.2 µm and 0.6 µm respectively. Bias currents nearly settle to 100 µA. The input capacitance of amplifier is 1.4 fF because of the very small value of driver transistors.

Other stages of preamplifier contain four cascaded amplifiers as shown in Figure 3.8. These four amplifiers have same transistor sizes. As illustrated in the full schematic of preamplifier, all stages are driven by same bias voltage. However, MB1 and MB2 are

identical and their width is 4 µm. MB3-MB6 are identical and their width is 10µm. Therefore, each of these four amplifiers is biased with 250 µA. Also eachone's gain is approximately 2.

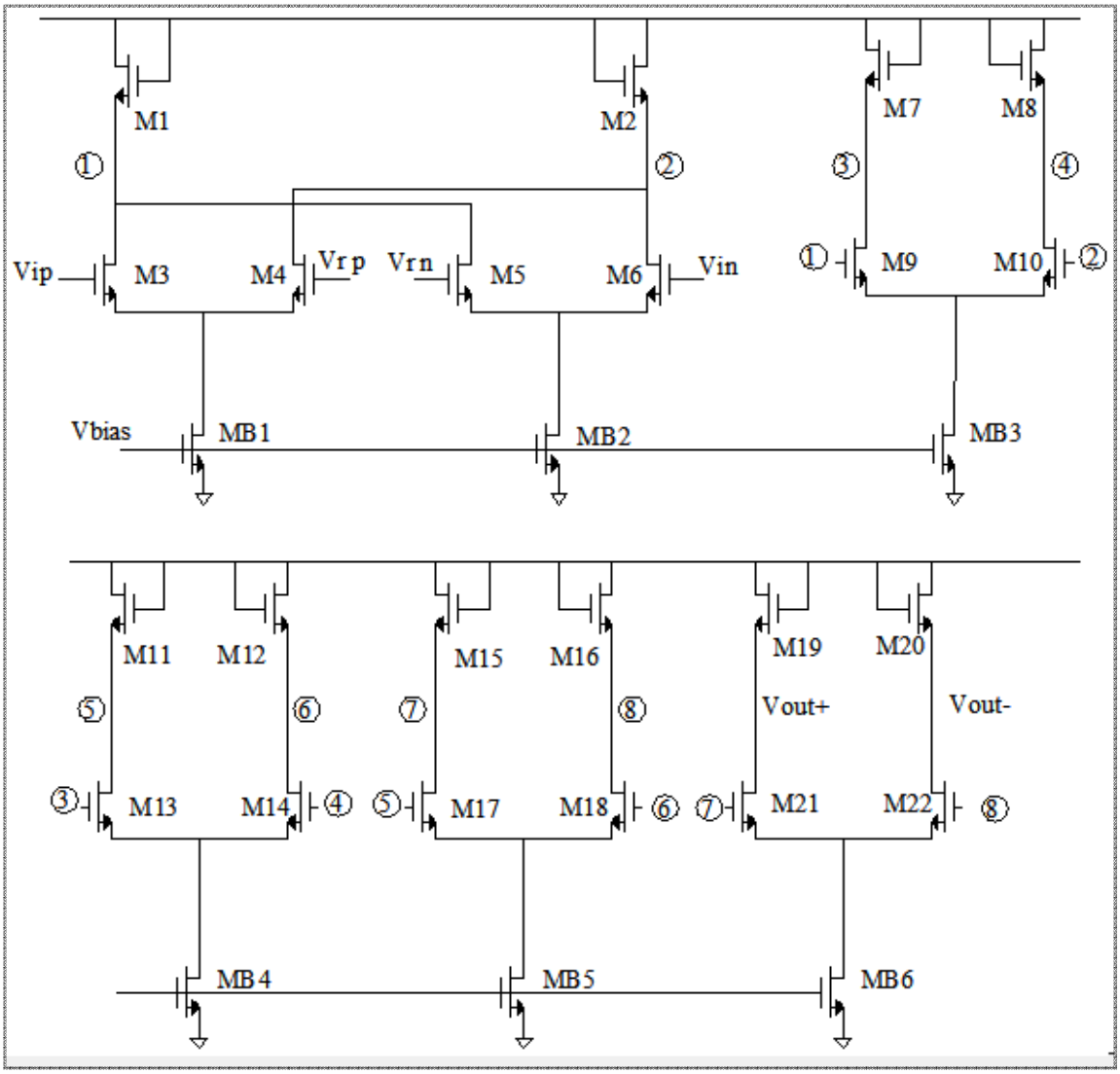

Figure 3.8. Full schematic of Preamplifier

As a result, the total gain is nearly 20 and cut-off (-3 dB point) frequency is arranged to 2.2 GHz. This cut-off frequency value gives nearly 0.14 ns rise time for amplifier's output or comparator's input. The preamplifier needs 2.33 mW to achieve the specifications which are given above.

Differential preamplifier and voltage comparator connection is shown in Figure 3.9. Full schematic of 6-bit Flash ADC contains 64 preamplifier and 63 voltage comparator circuits. Current at the right branch of voltage comparator is mirrored by the identical transistors as shown in Figure 3.9. M1-M8 are identical transistors. Because of identical sizes, same gate and source connections, the currents of M2-M4 and M6-M8 are identical. These mirrored currents are used as input of current comparator and latch circuit, which are presented at next chapter.

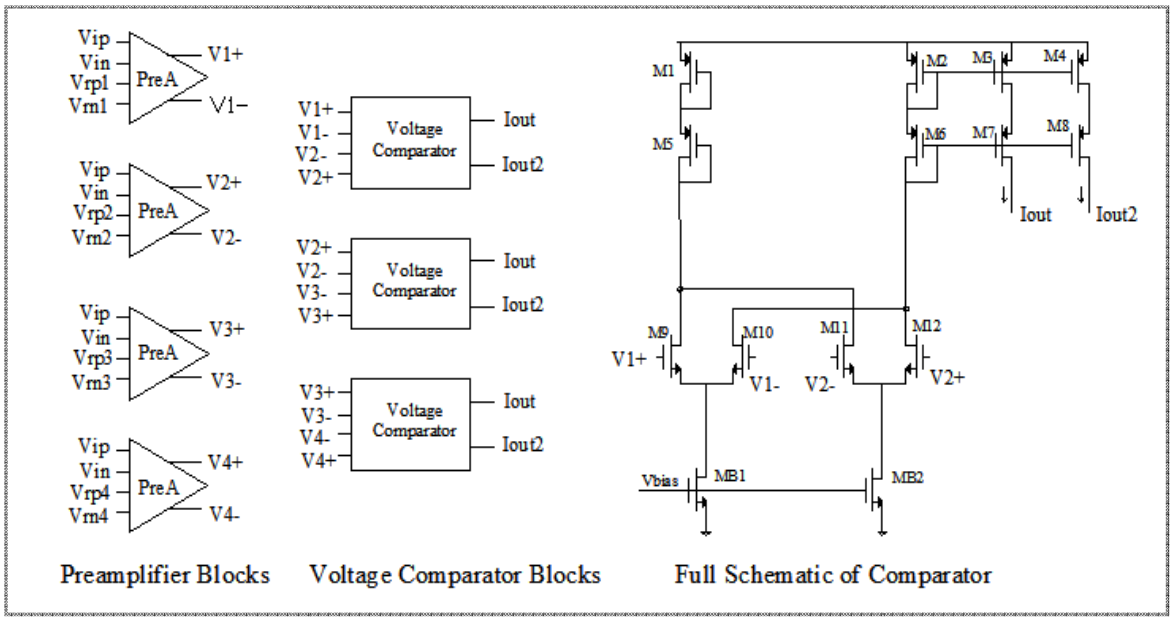

Figure 3.9. Preamplifiers and voltage comparators connections and schematic of comparator

Voltage comparator's bias currents are arranged to 40 µA. Output of voltage comparator is increasing up to 60 µA for selected comparator. A DC simulation is run for 4 amplifiers and 3 voltage comparators as shown in Figure 3.9. The result of this simulation is given in Figure 3.10. In the selected range currents are increasing up to 58.8 µA and for stable condition, which the voltage comparator's input is out of the range, the current is 40 µA.

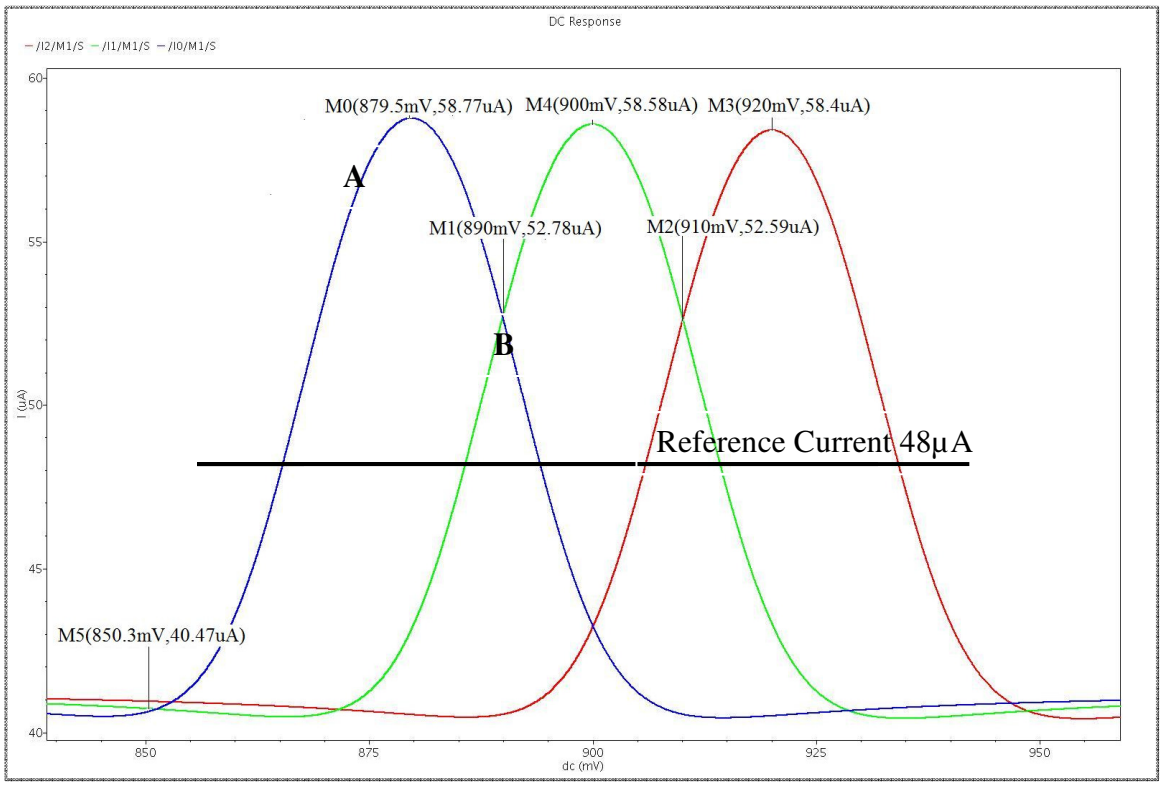

Figure 3.10. The DC sweep simulation of 3 voltage comparators [25]

The outputs of the voltage comparator are mirrored currents; these currents will be used as input of current comparators' circuits which determines the higher currents than 48µA. If any voltage comparator's output is at the point A, the current comparator which is driven by blue signal will give "1". However, if the voltage comparator output is at the point B, there will be two current comparators which have "1" at their outputs. Blue signal and green signal are higher than 48µA at the point B. At that point, system needs another decision circuit which compares these two currents. This decision circuit will be presented through the following chapters.

3.3. CURRENT COMPARATOR

Current comparator is a fundamental component of current-mode circuits. Current-mode circuit is considered to be an alternative to voltage-mode circuit for high-speed and low-power applications [9]. The current comparator process is injecting one or two current flowing into the comparator and distinguishing whether the current is positive or negative.

This process is compatible with the system which is presented in previous chapters. Also, the system needs a current comparator which determines the higher current values than reference current value as shown in Figure 3.10. Therefore, the current comparator circuit is adapted to this flash analog-to-digital converter from reference [10]. The schematic of current comparator is illustrated in Figure 3.11.

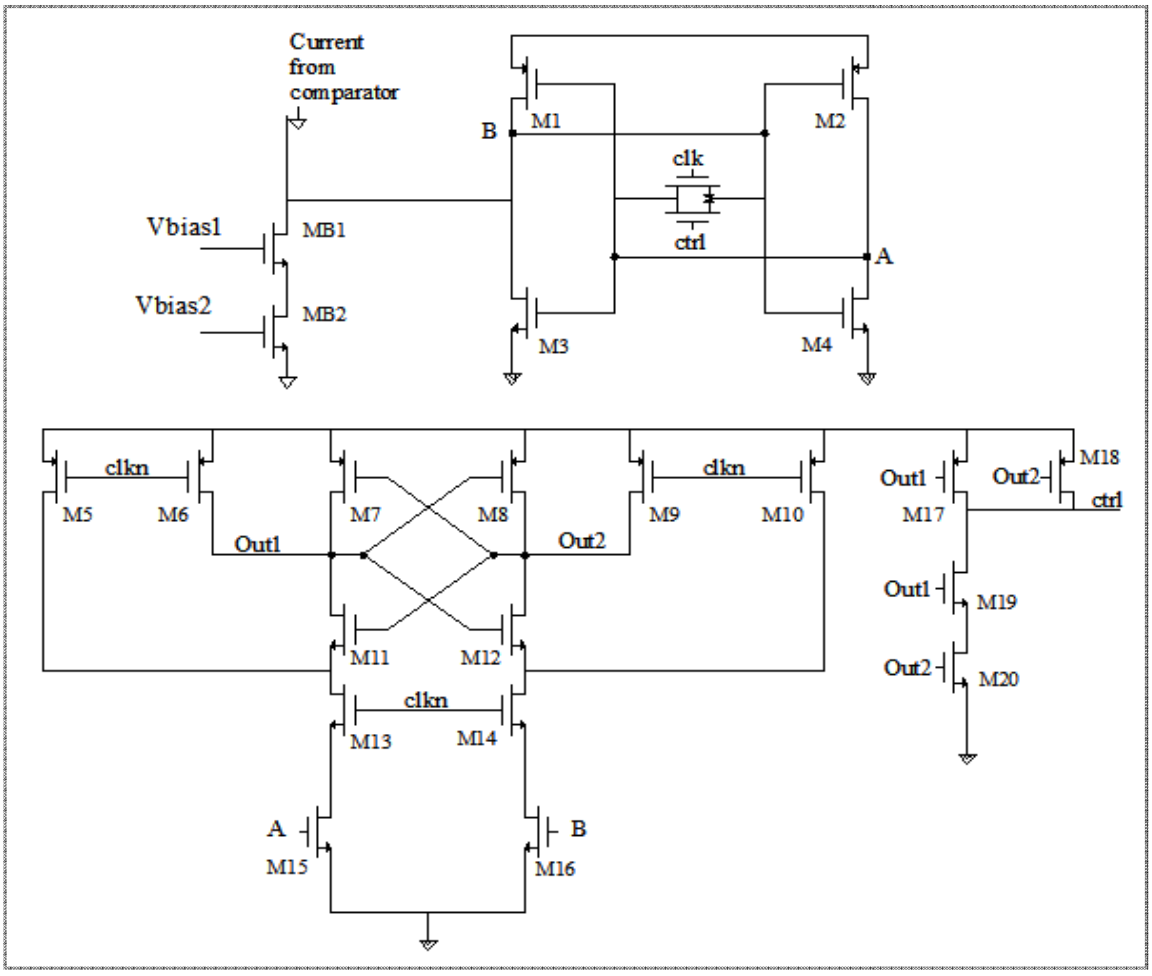

Figure 3.11. The schematic of the current comparator

Input of the current comparator is the output of the voltage comparator which is shown in Figure 3.9. Current which is flowing from voltage comparator meets a reference current at the input of current comparator. This reference current is produced by transistors MB1 and MB2 as shown in Figure 3.11. These transistors are driven by bias circuits which will be presented in next chapters. The reference current, which flows through MB1 and MB2, is set to 48 µA.

Voltage comparator's output can be higher than 48μA, as the point A shown in Figure 3.9. In this situation, same amount of current must flow through M3 transistor, which is shown in the schematic of the current comparator. When clk is high, it is in sampling phase. Points A and B are forced to the quiescent points. When clk and ctrl signals go to zero, regeneration phase starts and voltage of point B starts to increase and point A starts to decrease.

Point A and point B are the input voltages of dynamic latched comparator's drivers, which are M15 and M16. M7, M8, M11, M12 compose the latch structure, and M13, M14 are used for power reduction. These transistors are driven by signal clkn. When clkn is low, M5, M6, M9 and M10 drain goes to VDD. M13 and M14 is cut-off. In this situation, there is no current flow through the comparator. When clkn is high, M5, M6, M9 and M10 are cut-off. The current starts to flow through M13 and M14 based on the input voltages which are A and B. Output is determined by the latch structure.

Outputs, out1 and out2 drive a NAND circuit which is composed of transistors M17, M18, M19 and M20. Its output is ctrl, which is used as reset phase on this structure.

Figure 3.12 shows a transient simulation result of current comparator. Input signals; A and B, clock signal; clk and clkn, outputs; out1 and out2, and their change with time are shown in the Figure 3.12 as explained above.

This current comparator gives two output, out1 and out2. Out2 is used for output of current comparator block. Therefore, this signal is buffered with 3 inverters. Buffered signal is illustrated in Figure 3.13.

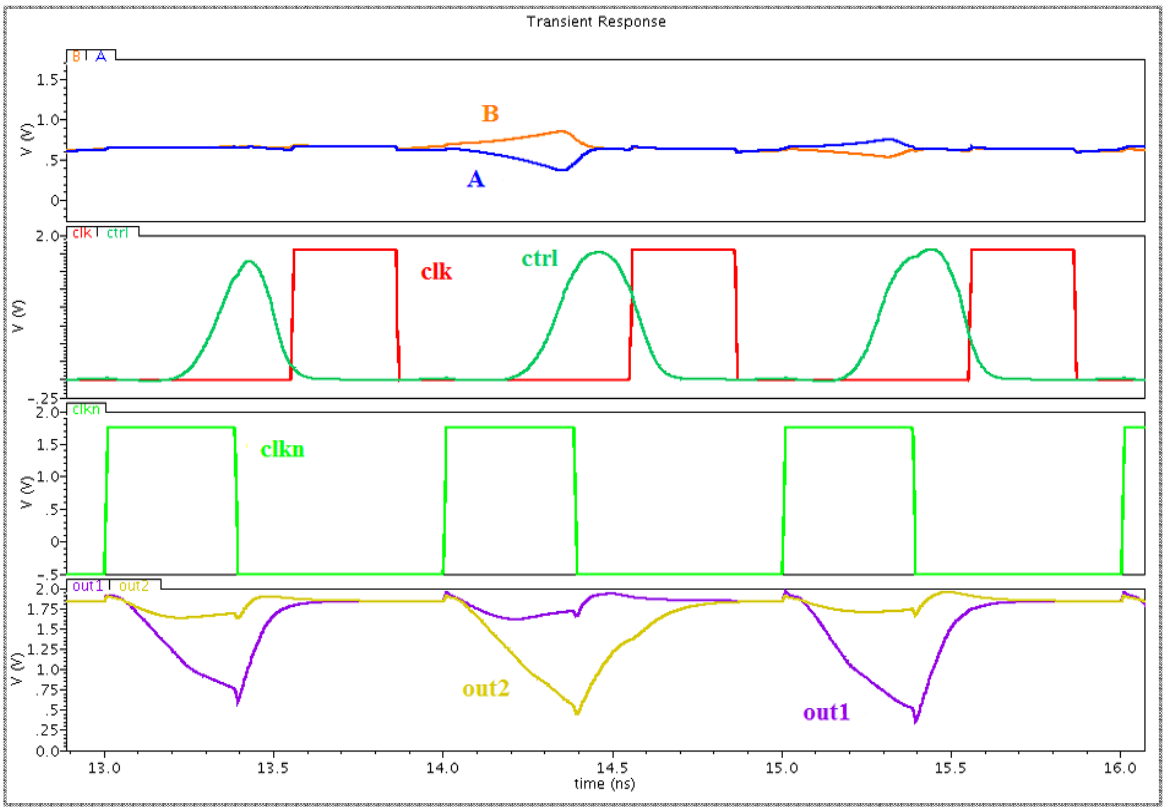

Figure 3.12. Transient simulation of current comparator [25]

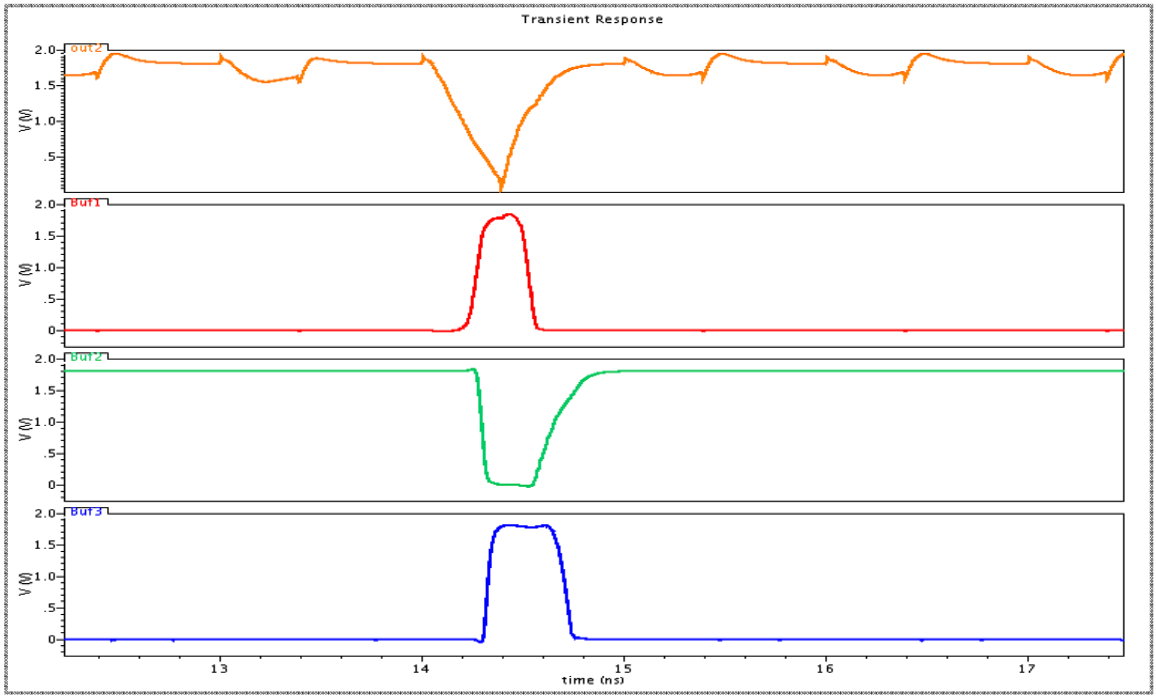

Figure 3.13. Out2 and buffered out2 by 3 inverters [25]

In buffer design, second inverter's pmos's channel width is chosen as 2 times smaller than nmos to increase rising time as shown in Figure 3.13. This provides longer pulse width for output of comparator.

As a result, the current comparator' sampling frequency is 1 GHz and sensitivity is 0.5 µA. Average power consumption is 269 µW. Maximum power efficiency is achieved by transistors M13, M14 and control signal clkn. When clkn is low, these transistors are cut-off and there is a supply current only during clkn is high. Signal clkn and power consumption are shown in Figure 3.14.

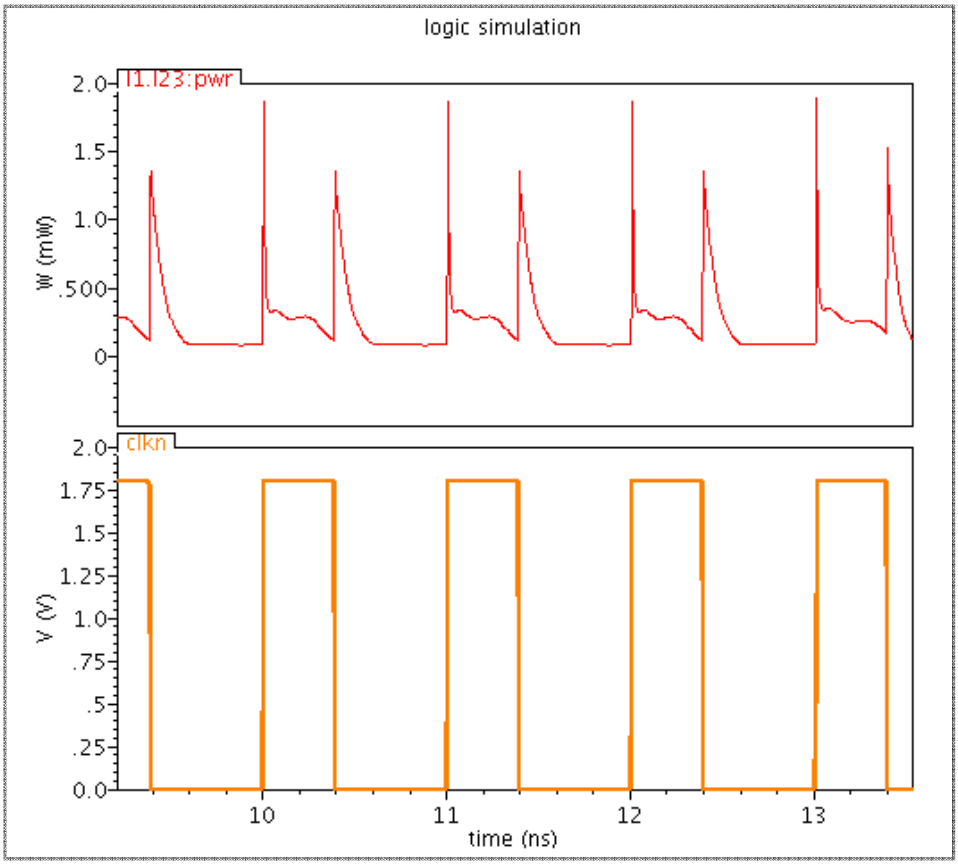

Figure 3.14. Power consumption of current comparator and signal clkn relation [25]

The dynamic latch comparator which is used in this current comparator topology, provides highest speed and power efficiency, but causes more kickback noise [11, 12]. This kickback noise originates from the rail-to-rail change on the drains M15 and M16. The voltage variation couples through gate-drain capacitance and causes input voltage

variation [10, 11]. The reference current is decreased to prevent any accuracy problem which is caused by the kickback noise. Decreasing the reference current to 48 µA provides enough range to produce higher voltage difference between nodes A and B. It eliminates accuracy problem which is caused by the kickback noise.

3.4. DECISION CIRCUIT DESIGN

Decision circuit determines the quantization level, if two current comparator circuits give high at their outputs. This state of flash analog-to-digital converter is shown in Figure 3.10 with point B. Also, decision circuit must provide a quantization level, when only one current comparator output is high. This circuit contains mirror circuit, two different buffer circuits, 3 switches for each one of 2^{N-1} steps and it contains one latch circuit and 2 buffers as shown in Figure 3.15.

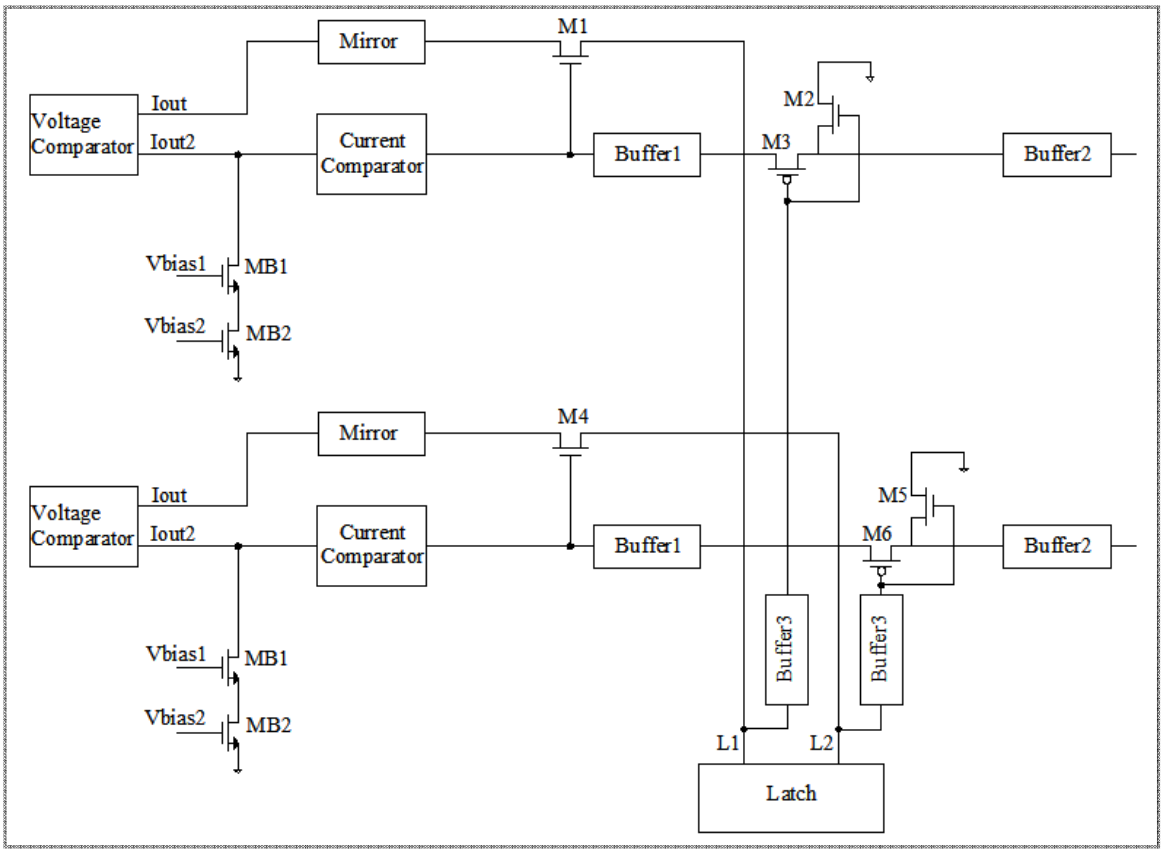

Figure 3.15. Schematic of decision circuit with voltage comparator, current comparator and reference current circuit

Decision circuit can encounter with two states, one of which takes place when the two current comparators give high at the output. Other takes place when only one comparator gives high signal. If there is high signal at the output of two current comparators, these high signals drive nmos switches M1 and M4 as illustrated in Figure 3.15. These transistors enter saturation from cut-off. M1 and M4 transistors flow currents which are mirrored from comparator circuits by mirror blocks. These currents are the inputs of latch block. Latch block determines the highest current and this branch goes to low and other branch goes to high. Assume that L1 branch goes to low. L1 node value is buffered by buffer3 and it drives pmos transistor M3. M3 conducts buffered high signal to buffer2 and nmos transistor M2 enters cut-off from saturation. Meanwhile, L2 node is high and high signal is buffered by buffer3. This signal drives transistors M5 and M6. The latch circuits output is pulled up to VDD when there is no any current flowing to the latch. Therefore, transistors M5, M6 stay in the same conditions. M2 and M5 provide outputs stay low when there is no sampling. Decision circuit can encounter with other state which is only one comparators output is high. System works as same as presented above.

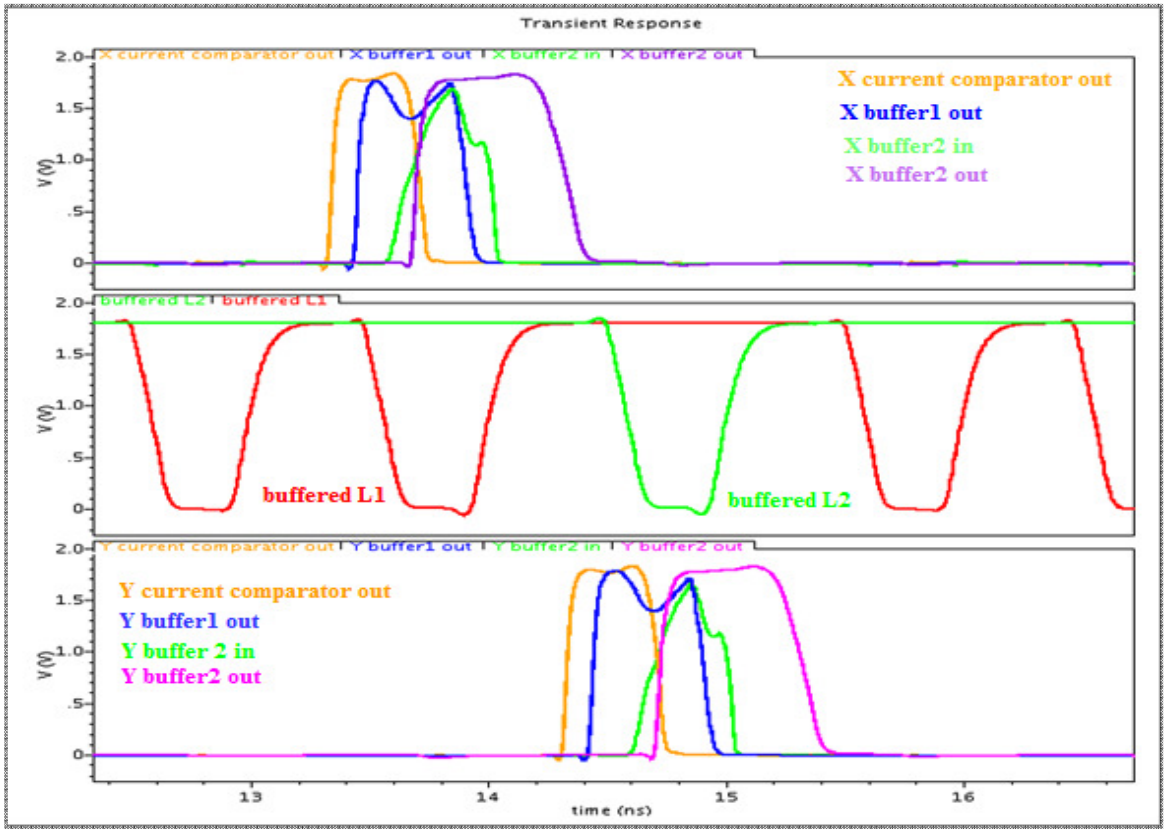

Figure 3.16. Transient simulations results of decision circuit [25]

Transient simulations results of the decision circuit are given in Figure 3.16. Simulation results are marked as X and Y before the block names. These notations show two different circuits of quantization levels. X current comparator output drives M1 transistor and it toggles L1 node of latch from high to low. This node is buffered by buffer3 and simulation result is given in Figure 3.16 named as buffered L1. Buffer L1 drives pmos M3 transistor. Drain of M3 is named as "X buffer1 out". M3 conducts this signal to buffer2 and it's named as "X buffer2 in". The last output of decision circuit for each quantization level is the output of buffer2. The last output signal is named as "X buffer2 out" in this simulation. In other sampling period, Y current comparator output is high and it toggles L2 node of latch from high to low. Buffering and switching process are same for Y circuits in this sampling period.

One of the most important processes is timing of latch and delays of buffers in this topology. Signal at the drain of M3 and M6 must be high before latch toggles to low, and must go to low, before latch toggles to high as illustrated in Figure 3.17. If latch toggles to low, before drain of M3 or M6 go to low, a voltage value holds at parasitic caps of the buffer 2 input, until next latching time. This situation causes quantization error and increase in differential nonlinearity (DNL). Increase of DNL cause quantization errors as explained in chapter 2.4.2.

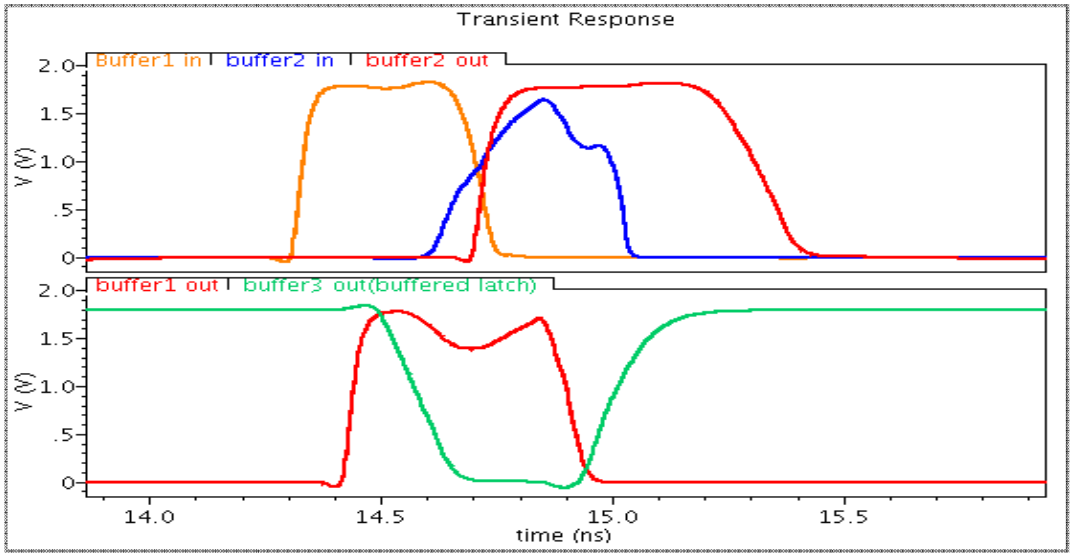

Figure 3.17. Transient simulation shows latching time and delay of buffers [25]

Timing is critical issue; as designed flash ADC has 1 GHz sampling rate. Current comparator sampling time and output generation time are important in order to compare significant current at current comparator and mirror significant current to latch circuit.

Current comparator stops sampling when clkn (presented section 3.3.) goes to high. Therefore, clkn signal must start to rise to high, when output of voltage comparator reaches the correct current level. Otherwise, output of voltage comparator can be compared against wrong current value. This timing is shown with simulation results in Figure 3.18. Current of X voltage comparator reaches the expected value at 13ns and clkn starts to rise at this point to sampling at right time. Other important point is mirroring current to latch circuit by help of M1 or M4 nmos transistor. When M1 and M4 enter the saturation mode, expected current value must also be provided at that time. This is illustrated in Figure 3.18. When X current comparator output goes to high, expected current is still at the same value. This current mirrored to latch by M1 switch and latch signal, which is shown in Figure 3.18, goes to low in order to produce last output of decision circuit and it is named as "out3".

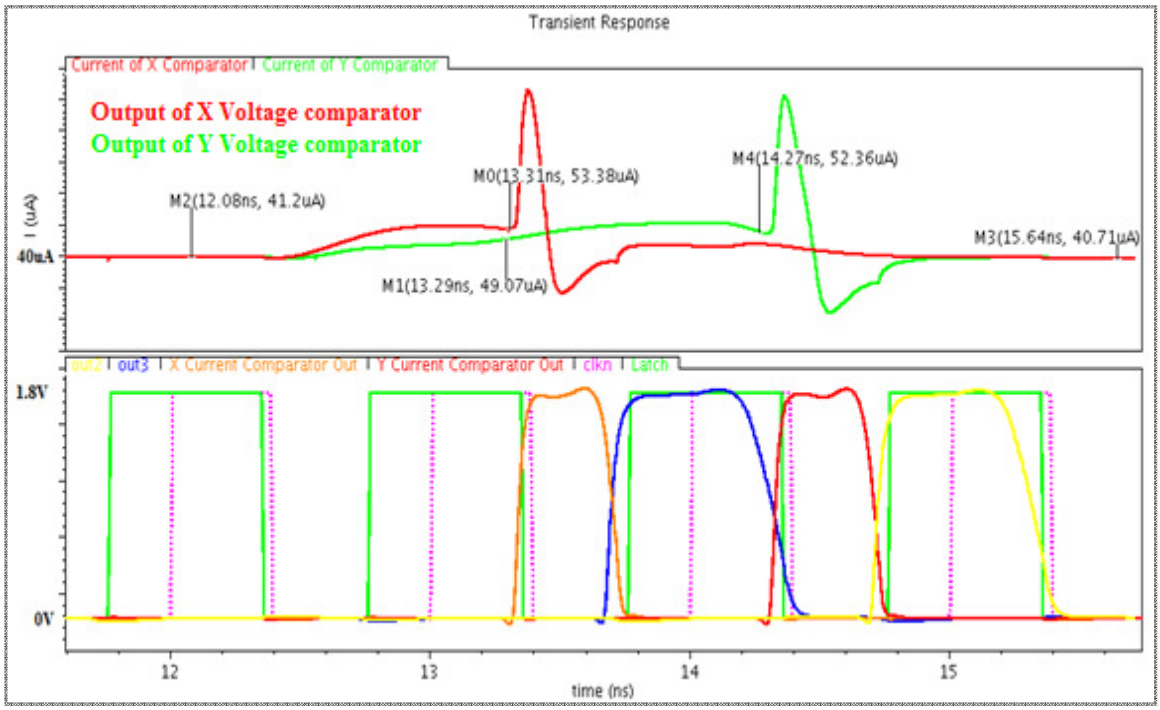

Figure 3.18. Transient responses of comparators' currents, timing of latch and current comparator [25]

3.4.1. Mirror Blocks

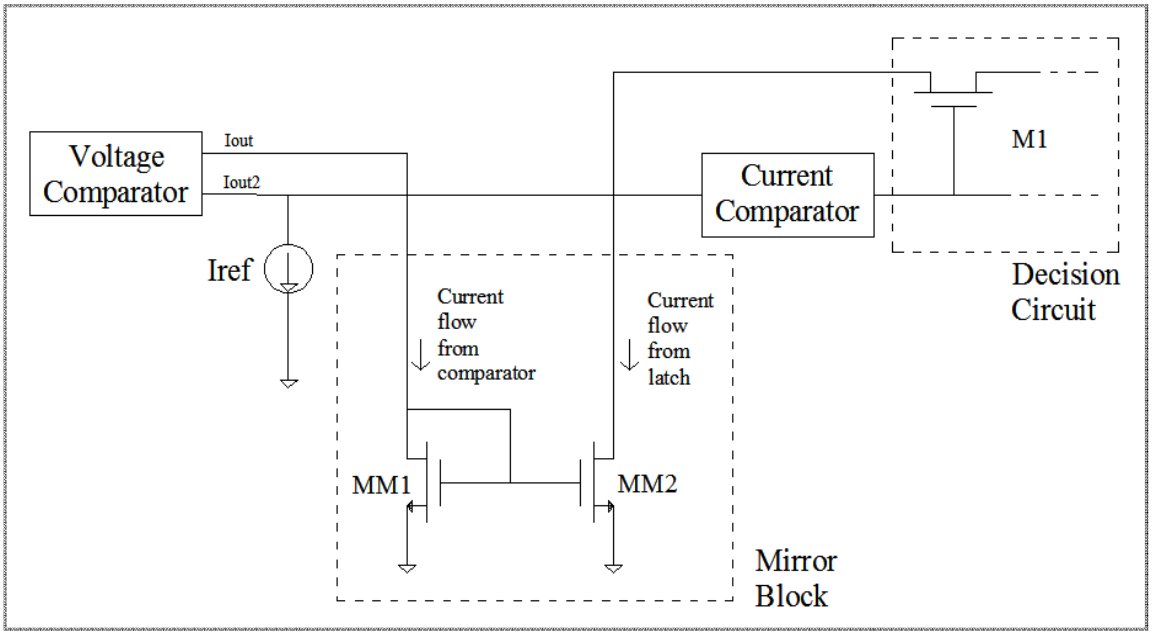

Figure 3.19. Schematic of mirror block

Mirrored currents; Iout and Iout2 on comparator topology, which is shown in Figure 3.9, flow through transistor MM1 which is shown in Figure 3.19. If switch M1, which is in decision circuit, is closed. The current flow on transistor MM1 is mirrored to transistor MM2, as MM1 and MM2 have same gate-source voltages. Channel width of MM2 is 4 times longer than channel width of MM1. The reason is the increase in the current difference on the branches of latch circuit. If two sequential current comparators give high, it means these comparator's current are very close. Increasing the channel width of MM2 is the way of increasing the difference of these currents.

3.4.2. Latch

Schematic of latch circuit is given in Figure 3.20. L1 and L2 nodes of latch are pulled up to VDD by switches MS1-MS4. Currents of selected comparators are mirrored to latch's nodes L1 and L2. Latch toggles according to the currents value when latch signal goes to low. Higher current's node voltage starts to decrease and this node toggles to "1" and other toggles to "0".

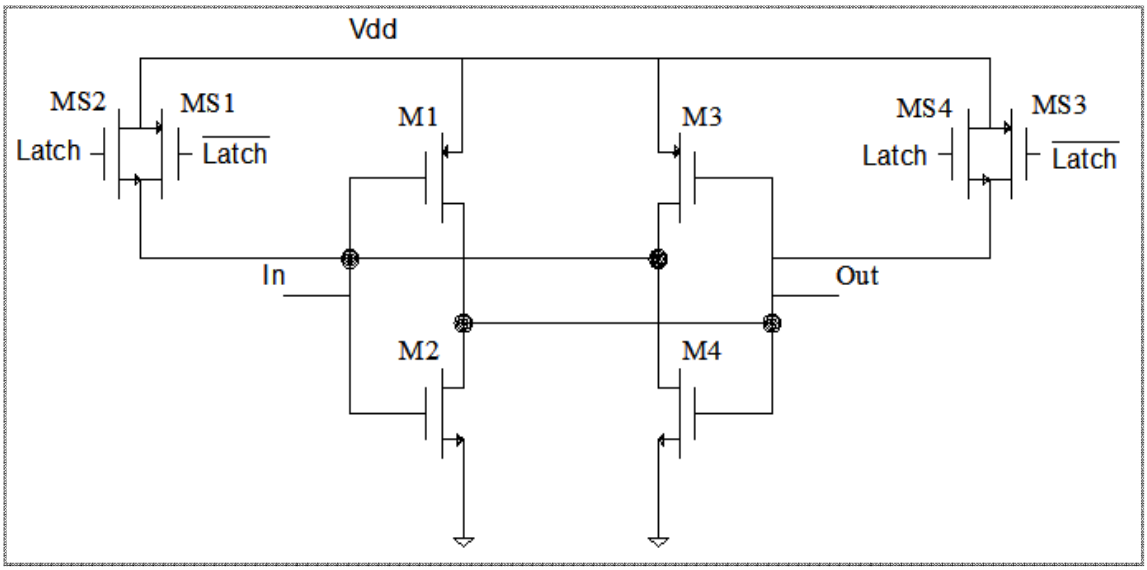

Figure 3.20. Schematic of latch circuit

3.4.3. Buffers

Buffers are used in decision circuit as shown in Figure 3.15. These buffers include NOT gates and they are used to regenerate signals according to buffer's threshold. Also, buffers are used to regenerate signals with larger pulse width.

3.4.3.1. Buffer 1

This buffer consists of four NOT gates as illustrated in Figure 3.21. First inverter is built by transistors M1, M2. Channel widths of M1 and M2 are chosen 1µm and 2µm respectively. M1 is pmos transistor and shortest channel width provides longer low to high rise time. This process achieves longer pulse width according to input signal's pulse width.

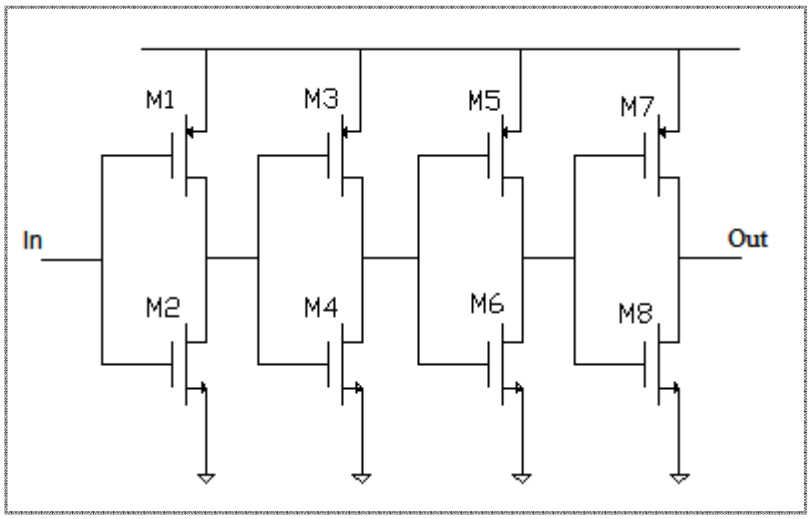

Figure 3.21. Schematic of Buffer 1

The remaining three inverters are identical to eachother. Channel width of M3, M5, and M7 is 1.5µm and channel width of M4, M6 and M8 is 0.5µm. Lengths of all transistors are 0.2µm. These three inverters provide necessary delay time for timing with buffered latch signal as shown in Figure 3.17.

3.4.3.2. Buffer 2

This buffer contains two inverters as illustrated in Figure 3.22. Pmos transistor M1 channel width is chosen 0.4µm and nmos transistor M2 channel width is chosen 5µm to decrease the threshold of the inverter. Channel width of M3 is 2µm and M4's width is 0.25µm. This buffers threshold is 550mV.

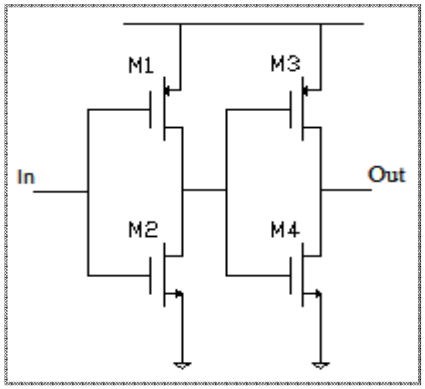

Figure 3.22. Schematic of Buffer 2

Threshold is chosen very low to catch all possible outputs of decision circuits, even though they have very low peak value as 550 mV. This has great importance at high temperatures, because signal's rise and fall time increase and peak value of same nodes decrease; such as input of buffer 2. This situation is shown in the simulation in Figure 3.23.

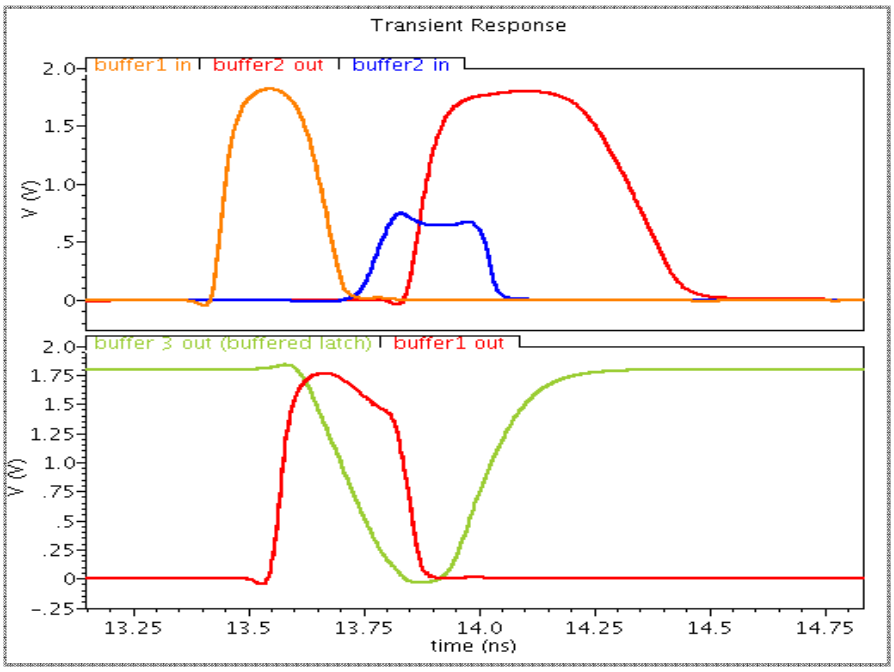

Figure 3.23. Buffered signals at 120 °C [25]

3.4.3.3. Buffer 3

Buffer 3 is used to regulate the latch signal. It contains two identical inverters as shown in Figure 3.24.

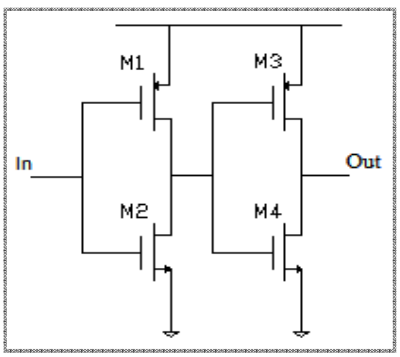

Figure 3.24. Schematic of Buffer 3

3.5. ROM

"N" bit ROM circuit converts 2^N quantization levels to "N" output. ROM of designed 6-bit flash analog-to-digital converter has 64 inputs and 6 outputs. However, 3-bit configuration of a ROM circuit is illustrated in Figure 3.25 for convenience.

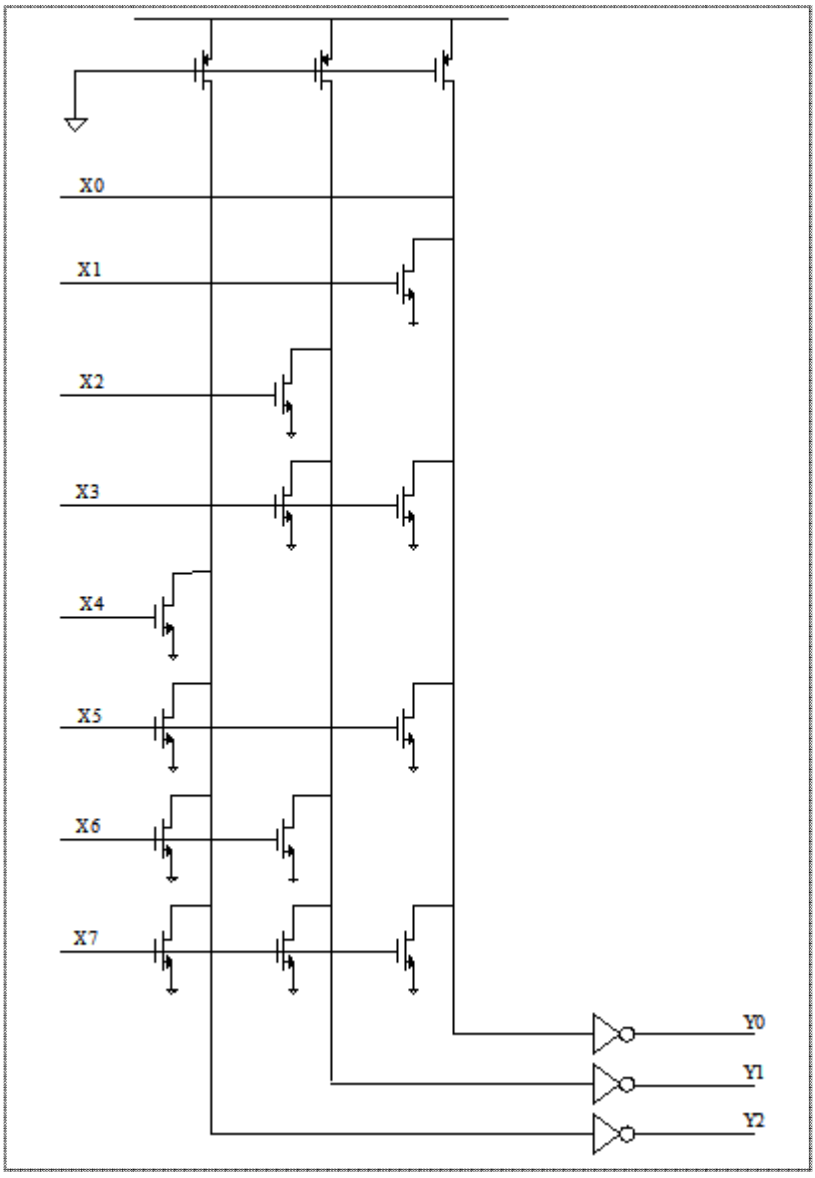

Figure 3.25. 3-bit ROM Circuit

There are 3 columns for outputs and 8 rows for inputs. At the top of each column there is a PMOS transistor which makes the rest of the columns digitally "1" . Every row

as tied up to the gates of NMOS transistors and their drains are connected to the columns in order to select the necessary output. When sampling occurs, only one row is digitally "1", others must be "0". When a row is digitally one, transistors of which the gates are connected to the row make the corresponding columns zero and values drive inverters at the bottom of the columns. Inputs and outputs occur as shown Table 3.1.

Table 3.1. Inputs and Outputs of 3-bit ROM

Inputs of ROM $X_7\,X_6\,X_5\,X_4\,X_3\,X_2\,X_1\,X_0$	**Outputs of ROM**
0 0 0 0 0 0 0 1	0 0 0
0 0 0 0 0 0 1 0	0 0 1
0 0 0 0 0 1 0 0	0 1 0
0 0 0 0 10 0 0	0 1 1
0 0 0 1 0 0 0 0	1 0 0
0 0 1 0 0 0 0 0	1 0 1
0 1 0 0 0 0 0 0	1 1 0
1 0 0 0 0 0 0	1 1 1

Rom circuit is driven by buffer 2 which is in decision circuit and each output of ROM drives a D Flip-Flops, D Flip-Flop holds sampled signal exactly 1ns.

3.6. TRACK-and-HOLD

The track-and-hold or T/H circuit is used in the front-end element for analog-to-digital converter. The T/H circuit is widely used to avoid the degradation of signal by holding the analog sample static during digitization. The speed and the accuracy of the converter are highly dependent on the performance of the T/H circuit [14].

The T/H circuit employs a MOS switch to track and hold an analog signal. Using the MOS switch exhibits signal distortion at the T/H output caused by the channel charge injection, and clock feedthrough as mentioned section 2.3. These are major factors that

contribute to discrepancy from ideal performances [1, 13]. For charge injection and clock feedthrough cancellation, dummy transistor technique has been introduced.

T/H circuit can be built by using opamp or source follower to drive preamplifiers in converter designs. T/H circuits, which are using source follower, reaches higher sampling rates against to opamp used topologies. Some published high sample rate flash analog-to-digital converter's using source follower based T/H circuits [1, 2, 4, 7, 15].

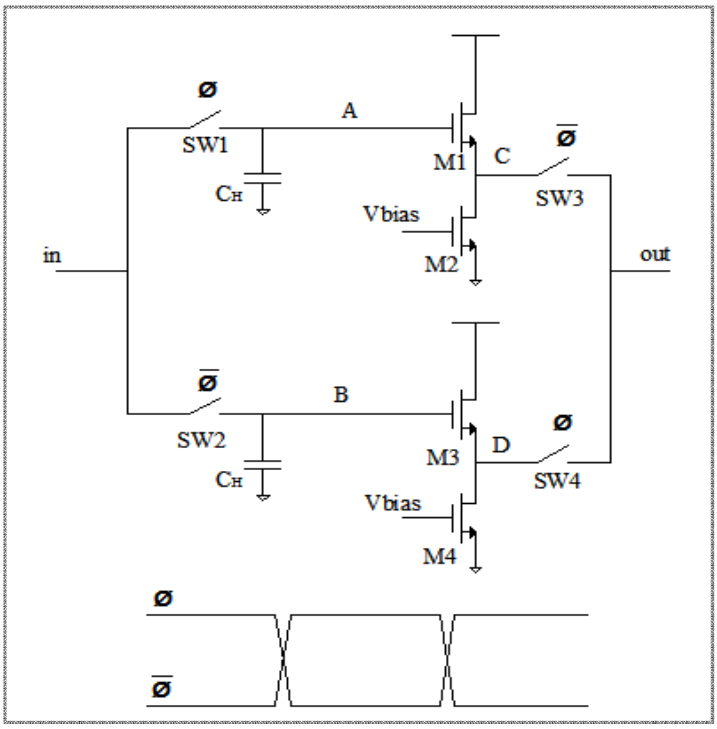

Figure 3.26. Schematic of designed T/H Circuit

Designed T/H circuit's schematic is shown in Figure 3.26. This topology provides double sampling. Compared to conventional T/H configuration the double sampling gives a factor of two increase in sampling rate [14]. SW1 and SW2 switches are driven by complementary clocks. When SW1 is in tracking mode, SW2 is in holding mode. SW3 turn switch on when SW2 is in holding mode and SW4 turn switch on when SW1 is in holding mode. T/H circuit's switches are driven by 500 MHz clock (Ø) frequency. However, sampling rate is 1 GS/s because of double sampling.

T/H circuit include nmos source follower which shift down the voltage level on sampling capacitances. Input of T/H is arranged to between 1.8 V to 1 V. Because of shifting down the voltage, output of T/H circuit is between nearly 1V and 400 mV. So, the differential resistor string is set according to output values of T/H.

Two identical T/H circuit is used in this flash analog-to-digital converter for differential inputs.

3.6.1. Switch Structure

Each T/H circuit consist 4 switches, they cause sampling errors because of charge injection and clock feedthrough effects.

When the MOSFET switch is on, the voltage V_{IN} produces a charge under the gate oxide. When the MOSFET turns off, this charge is injected on to the capacitor and into V_{IN} as illustrated in Figure 3.27. The injection on source-driven node has no effect. However, the charge injected onto C_{LOAD} results change in voltage. This injection is equally distributed on these two nodes. So, the injection on C_{LOAD} is the half of total injection.

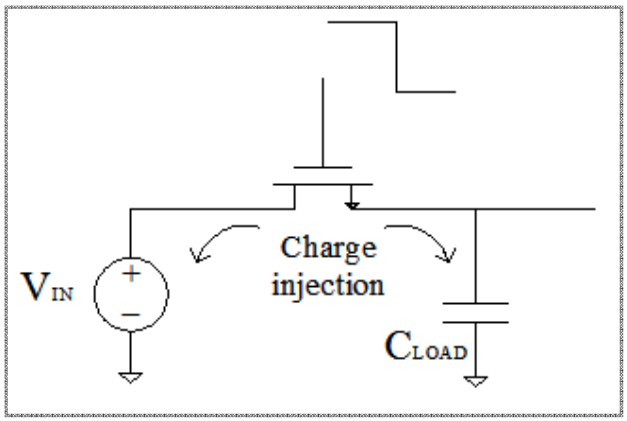

Figure 3.27. Charge injection

The gate-drain and gate-source capacitances of MOSFET are modeled as shown in Figure 3.28. When the gate clock signal goes high, the clock signal feeds through the gate-source and gate-drain capacitances. Input signal, V_{IN}, is also connected to the load

capacitor. As a result, C_{LOAD} is charged to V_{IN}. However, when the clock signal goes to low, the switch turns off, a capacitive voltage divider exits between the gate-source capacitance and load capacitance.

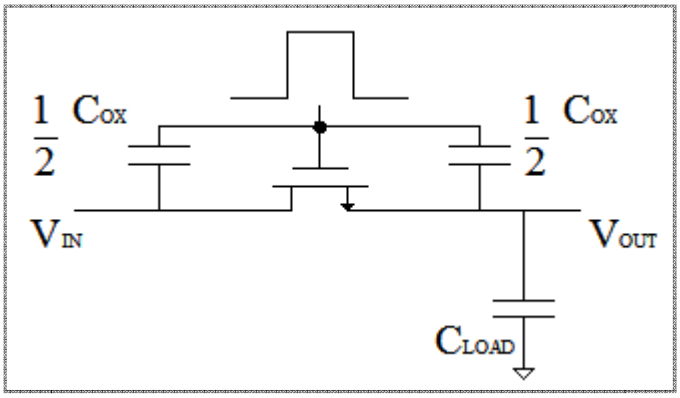

Figure 3.28. Clock feedthrough

Charge injection and clock feedthrough effects are reduced by using dummy switch and transmission gate as shown in Figure 3.29.

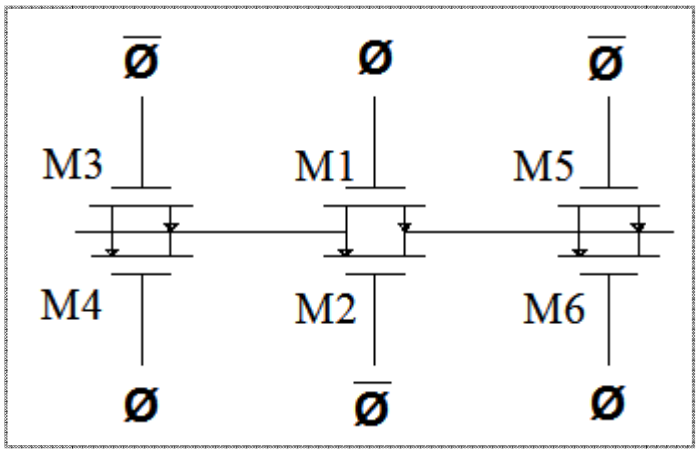

Figure 3.29. Schematic of switch structure which is used in T/H circuit

Sizes of dummy switches M3, M5 and M4, M6 are one-half of M1 and M2 respectively. When M1 turns off, half of the channel charge is injected toward the dummy switch. Drain and source of M2 is shorted. Therefore, the charge injected M1 is matched by the charge induced by M2, and the overall charge injection is cancelled.

100 MHz sinusoidal input signal is applied to T/H circuit. Input signal and sampled signals on points A and B, which are marked in Figure 3.26, is shown with simulations in Figure 3.30. When point A is at the track mode, point B is at the hold mode as shown in transient simulation.

Signals at points C and D, which are marked in Figure 3.27, are shown in Figure 3.31. These signals are between 1.05 V and 420 mV, as shifted by source followers. Output signal is the addition of hold modes of points C and D. Output of T/H circuit is also shown in Figure 3.31.

This Flash ADC contains two T/H circuits due to differential inputs. Therefore, two T/H circuit will be run by same clocks. Differential sinusoidal input signal and differential sampled signals are shown in Figure 3.32.

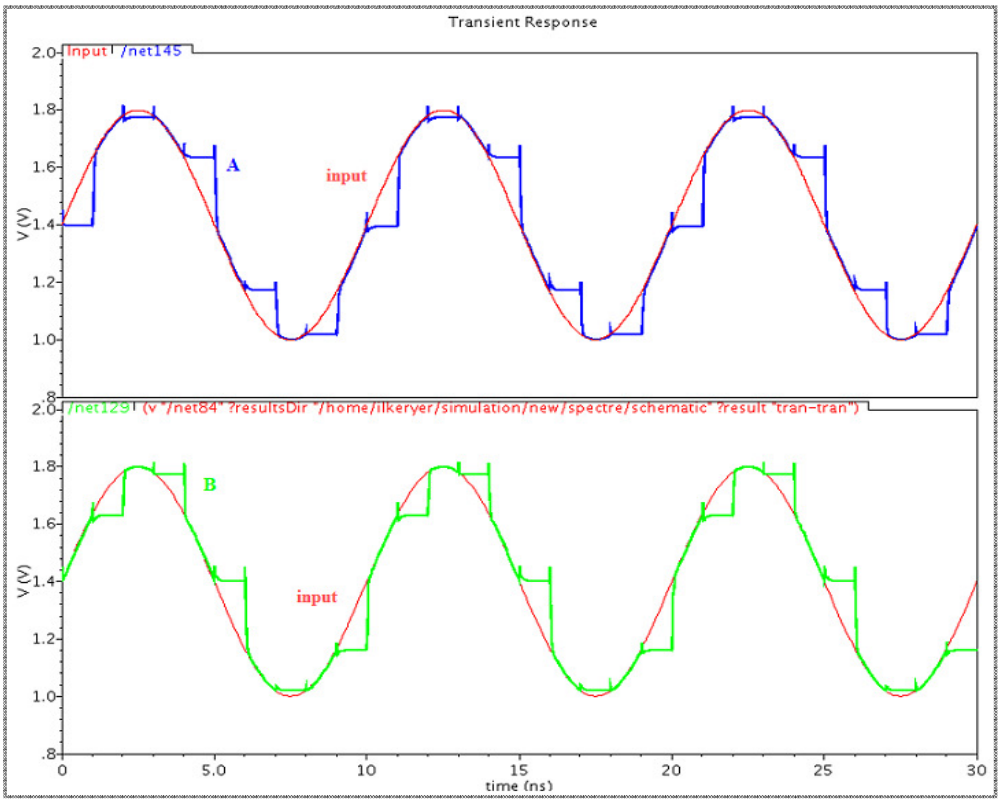

Figure 3.30. Input signal and sampled signals at points A and B [25]

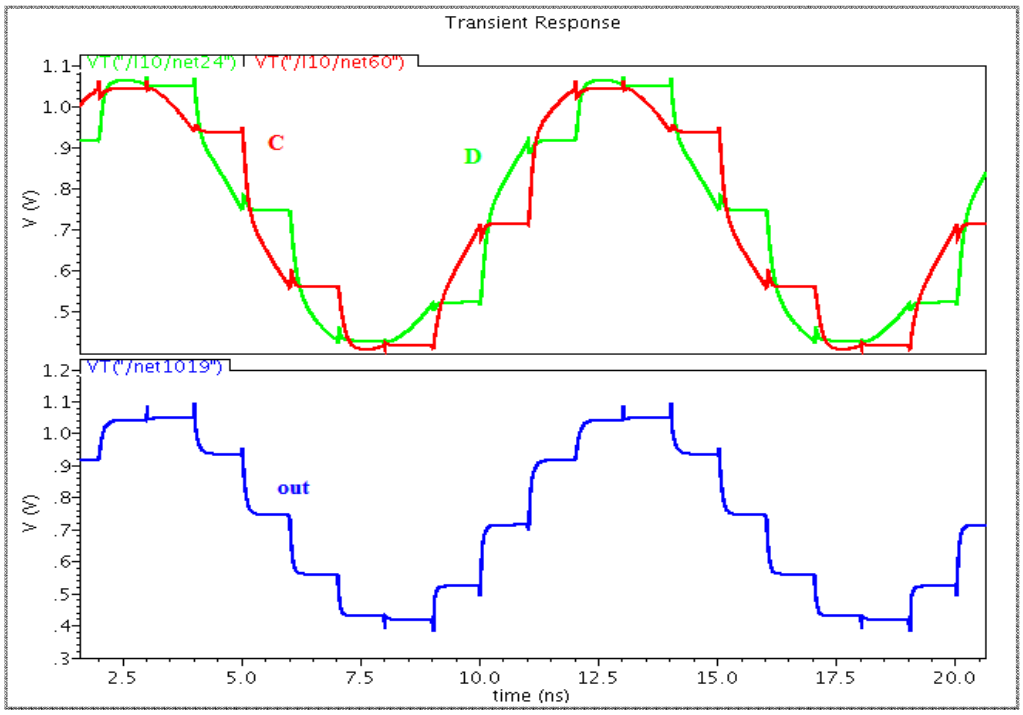

Figure 3.31. Output of T/H and signals of point C and D [25]

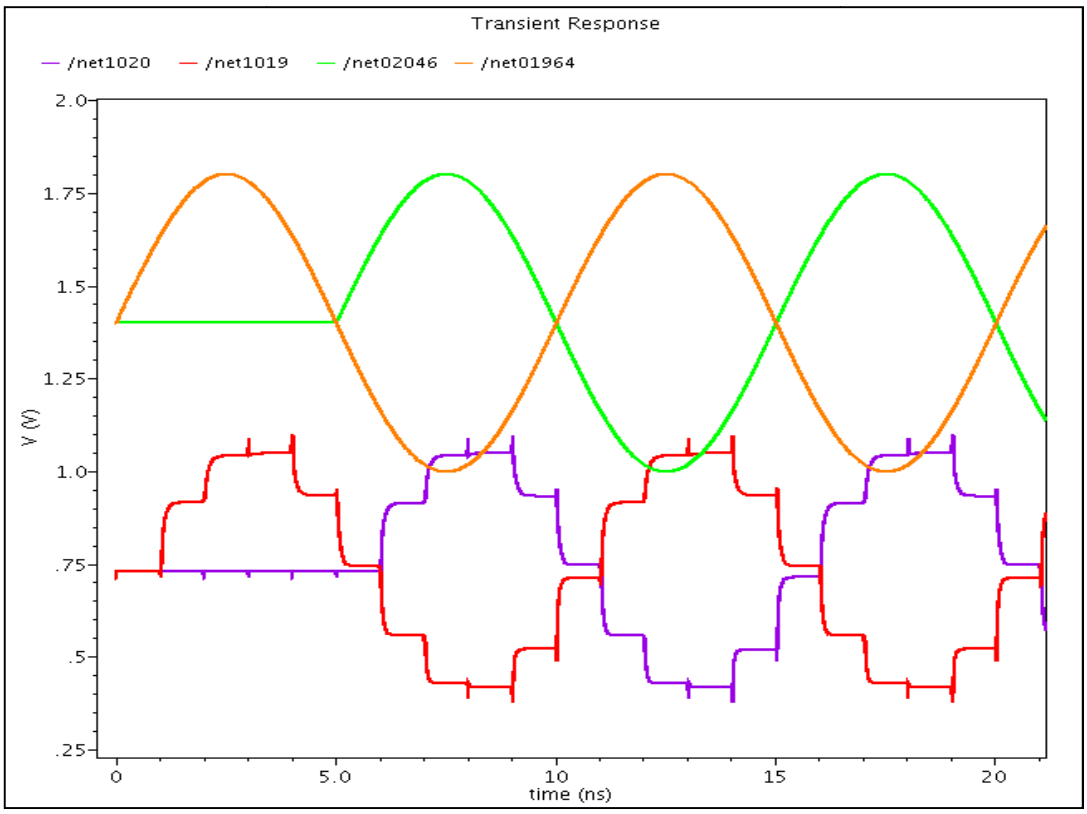

Figure 3.32. Differential input signals and sampled signals [25]

3.7. RESISTOR STRING

Flash ADC produces reference voltages by resistor strings. Two identical resistor strings are used to refer preamplifier circuits. Due to the differential structure, two resistor strings are connected to preamplifiers as shown in Figure 3.33.

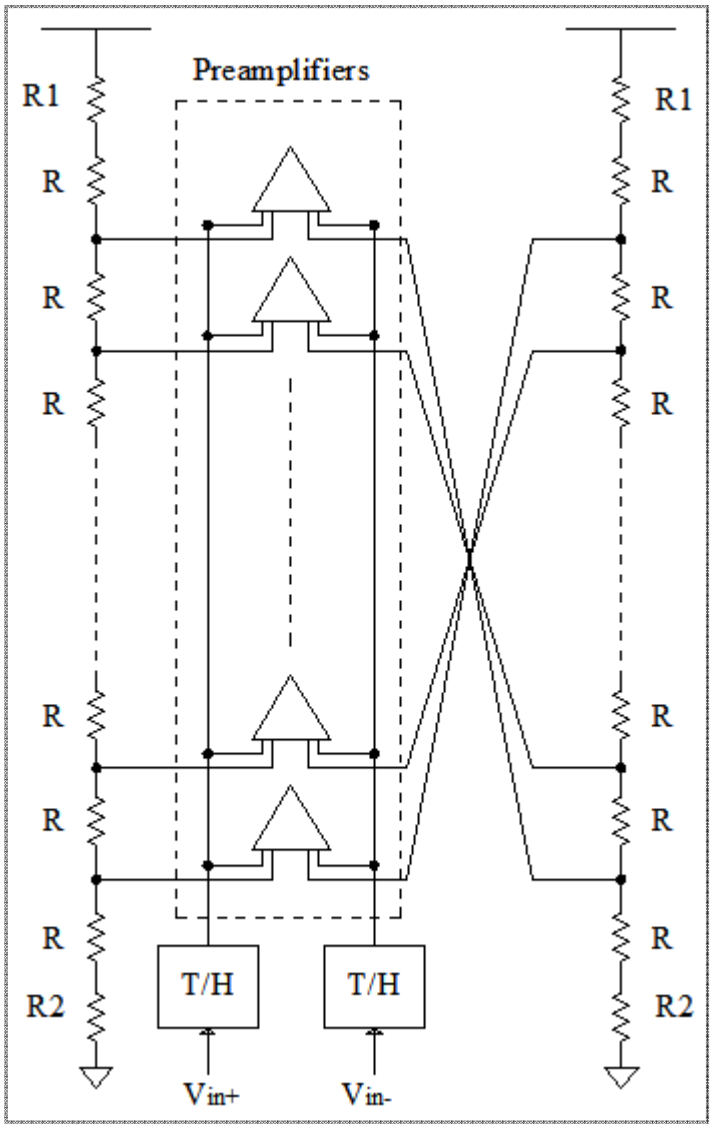

Figure 3.33. Schematic of Differential Resistor String

Resistor R1, R and R2 are chosen 1.17 KΩ, 16.54 Ω, and 658.3 Ω respectively to produce voltages 1.05 V to 420 mV with 10 mV steps.

3.8. BIAS CIRCUITS

A bandgap reference is an important circuit which is used as a voltage reference in ADC, regulators and memories. It is also used to generate an on-chip current reference [16]. Preamplifier, comparator, track-and-hold and reference current for current comparator need bias voltages. Therefore, the bandgap voltage reference circuit is used to produce necessary bias voltages, which is published in [17].

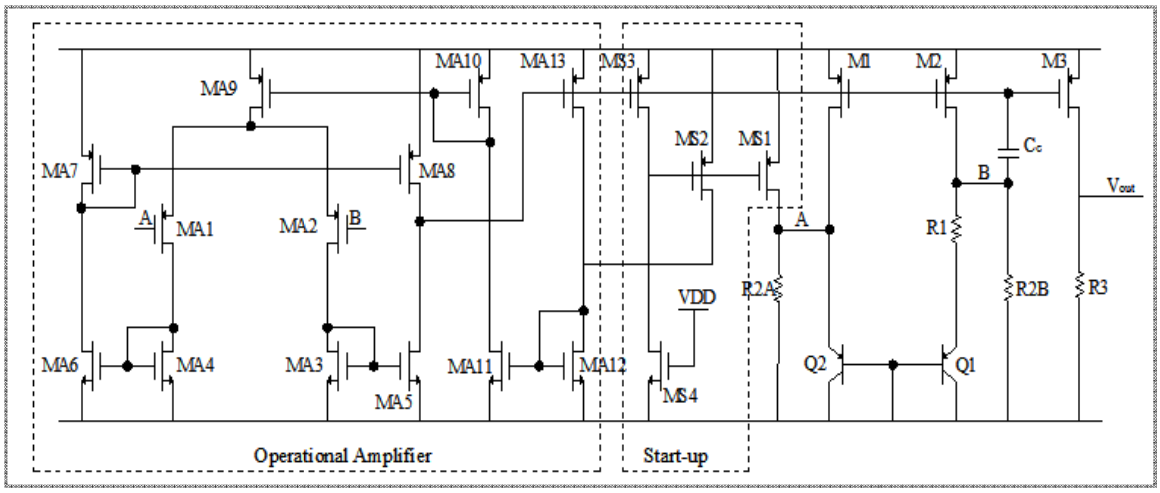

Figure 3.34. Schematic of bandgap voltage reference circuit

Bandgap voltage reference (BGR) circuit contains operational amplifier and start-up circuit as shown in Figure 3.34. The resistors R2A and R2B are connected to the differential inputs of amplifier by nodes A and B. Output of amplifier drives M1 and M2 which are identical transistors. It completes a feedback loop. The amplifier forces the nodes A and B have the same potential. The currents through R2A and R2B are the same when these transistors are identical. The total current through M1 or M2 is given by

$$I = \frac{V_{EB2}}{R_{2A}} + \frac{\Delta V_{EB}}{R_1} \tag{3.4}$$

V_{BE2} is the voltage on PNP BJT Q2 and ΔV_{EB} is the difference between Q1 and Q2. ΔV_{EB} is given by

$$\Delta V_{EB} = \frac{kT}{q} \ln N = V_T \ln N \tag{3.5}$$

V_T is thermal voltage and N is the emitter area ratio of Q1 and Q2. If (3.5) is written in (3.4). The result becomes

$$I = \frac{V_{EB2}}{R_{2A}} + \frac{V_T \ln N}{R_1} \tag{3.6}$$

V_{BE2} / R_{2A} is known as complementary to absolute temperature (CTAT) current and $V_T \ln N / R_1$ is known as proportional to absolute temperature (PTAT) current. They have opposite temperature coefficients. So, appropriately trimming the ratio of R2A and R1 provides bandgap voltage reference with low sensitivity to the varying temperature. Output voltage of BGR can be arranged by changing the value of R3.

The bandgap reference voltage circuit's amplifier part prevents voltage variations at the output circuit and capacitor C_C plays a role to ensure the stability of the feedback loop.

Start-up circuit consist transistor MS1, MS2, MS3, MS4 as shown in Figure 3.34. It provides start-up current for Q2 and opamp. MS4's gate is connected to VDD. The gate voltages of M1, M2, M3 and MS3 are pulled high, when the circuit has no current. The drain voltages of MS3 and MS4 are pulled low, that turns on MS1 and MS2. Current is injected to the bandgap by MS1 and to the amplifier by MS2. Then the amplifier starts to operate and progressively pulls down the output voltage of amplifier. This causes to increase at the drain voltages of MS3 and MS4. Therefore, MS1 and MS2 enter cut-off. MS4 transistor length must be chosen much higher than width to ensure a complete cut-off MS1 and MS2.

This bandgap voltage reference circuit provides voltages which are stable and low sensitive to temperature variation from -40 °C to 125 °C. The bias voltage values of the flash analog-to-converter's circuits are given in Table 3.2.

Table 3.2. Bias Voltages of Circuits

Circuits	Bias Voltages
Amplifier	663.5 mV
Comparator	621.5 mV
Current Reference Bias 1	1.1358 V
Current Reference Bias 2	593.1 mV
T/H	Changing with Temperature

Temperature variations of these bias voltages are determined by temperature sweep simulation as shown in Figure 3.35.

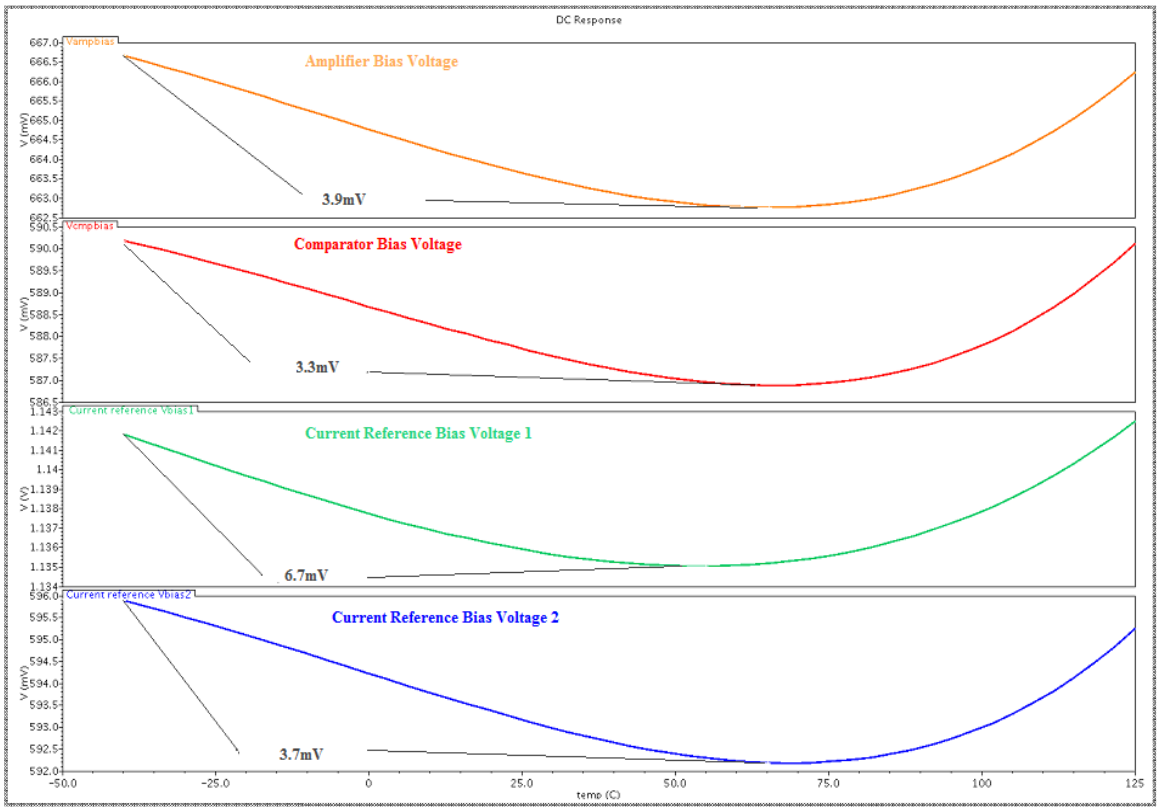

Figure 3.35. Temperature sweep -40 °C to 125 °C and bias voltage variations [25]

Bias voltage of T/H circuit is designed as PTAT (proportional to absolute temperature) since T/H circuit contains source followers, and their currents are decreasing with increasing temperature. This situation is suppressed by increasing bias voltage by

temperature as shown in Figure 3.36. Otherwise, the current change of source followers can cause offset errors with varying temperature.

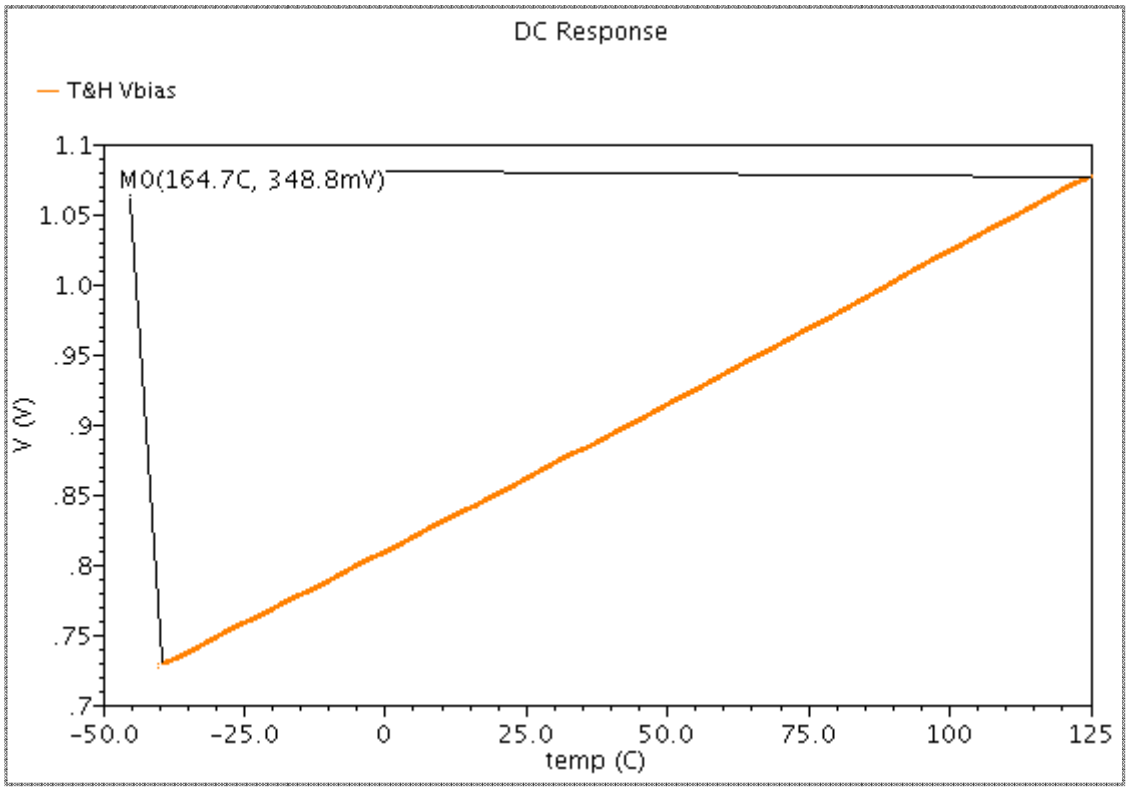

Figure 3.36. Bias voltage variation of track-and-hold circuit respect to temperature [25]

4. TOP LEVEL SIMULATION RESULTS

In the flash analog-to-digital converter design, all blocks are separately designed and simulated. After completion of blocks, they are connected and all system simulated with different input signals and varying temperature values.

4.1. SIMULATIONS WITH DIFFERENT INPUTS

Designed Flash Analog-to-Digital Converter can convert differential input signal signals up to 500 MHz with 1 GS/s rate. Three different input signals are applied to the converter for testing. Square wave signals are applied for all possible quantization levels and determined outputs are correct or not. Then differential sinusoidal input signal is applied 100 MHz to 500 MHZ. The ramp signal is also applied. Same applied wave forms of input signals are given in Figure 4.1.

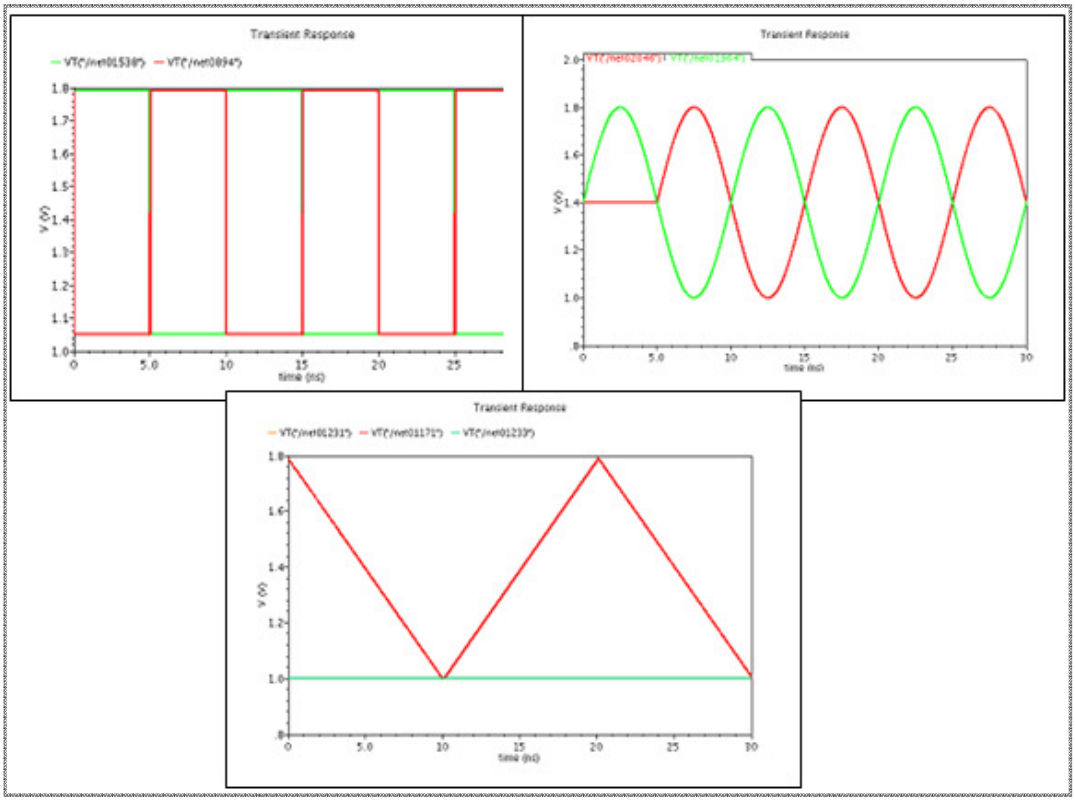

Figure 4.1. Same applied wave forms as differential input [25]

100 MHz sinusoidal differential signal is applied to the designed Flash ADC, and output is detected by 30 ns transient simulation. Outputs of decision circuit are shown in Figure 4.2. The decision circuit of Flash ADC gives an output at 1ns. These outputs drive ROM circuit. 100 MHz sinusoidal signal is converted to 6-bit digital signal at 1 GHz sampling rate.

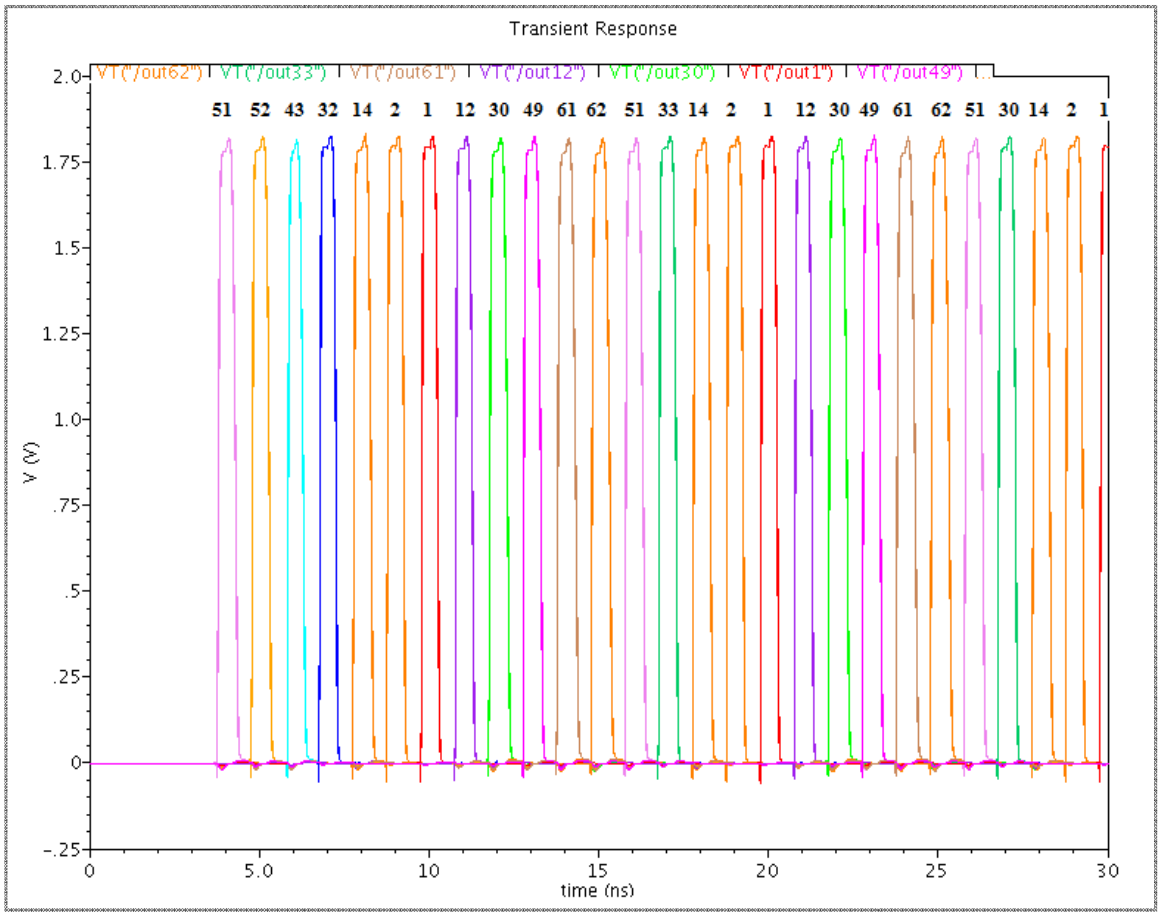

Figure 4.2. Output of decision circuit (input of ROM) for 100 MHz sinusoidal differential input signal, sampling rate is 1 GHz [25]

D Flip-Flops are used at the output of ROM circuit to handle the digital signal exactly 1ns and to refresh the output at each 1ns. Outputs of 6 D Flip-Flops are given in Figure 4.3. This is the final outputs of the designed Flash ADC.

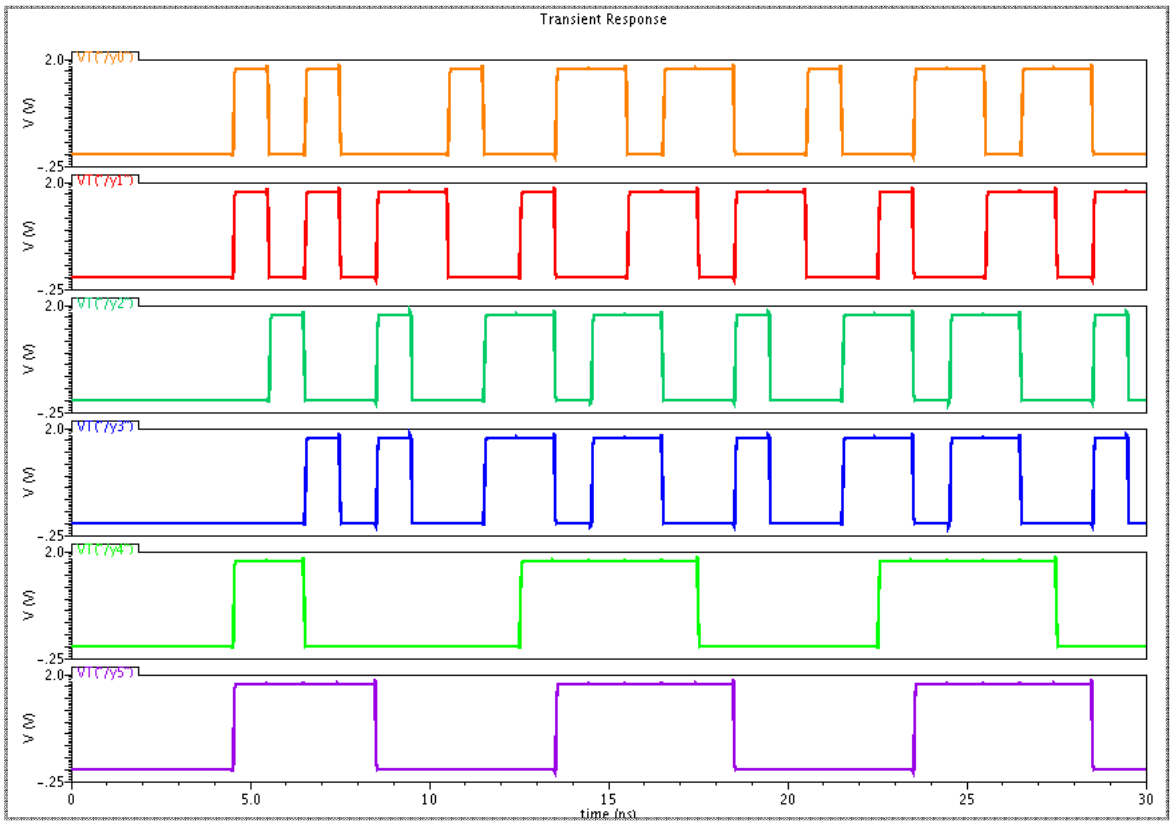

Figure 4.3. Output of designed Flash ADC for 100 MHz sinusoidal input signal [25]

4.2. TEMPERATURE

Designed Flash ADC is tested at various temperature values. Some calibrations are done to take same outputs for different temperature values. One of them is the reference current setting. At higher temperatures current comparator does not work properly, due to the decrease of comparator's currents. Therefore, the problem is solved by decreasing the current reference value by bias circuit. Other calibration is the T/H circuit bias voltage setting. The bias voltage of T/H increases with temperature as presented in the previous chapter. It provides stable sampling at varying temperatures.

100 MHz sinusoidal differential input signal is applied to the Flash ADC. Figure 4.4 shows outputs of decision circuit with varying temperature -40 °C to 125 °C.

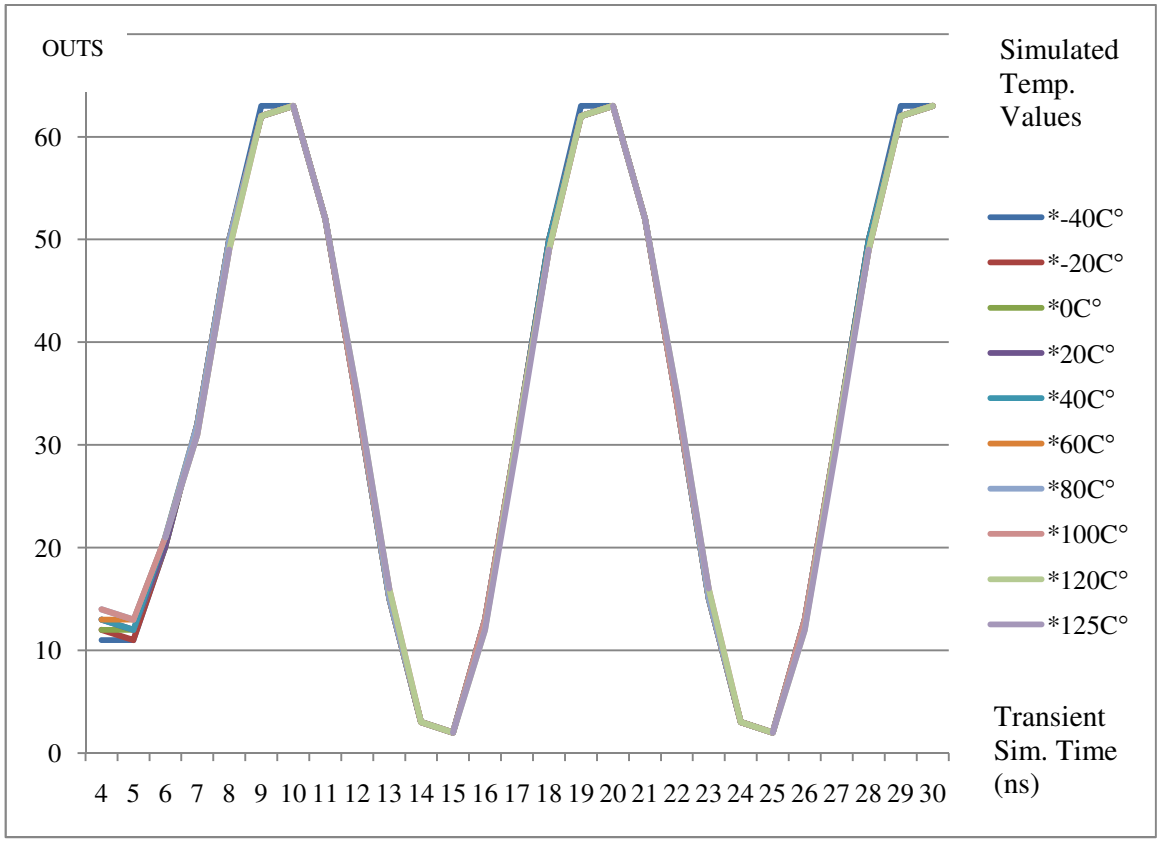

Figure 4.4. Temperature Simulations

Figure 4.4 is provided from Table 4.1 which represents the detailed simulation results. Designed Flash ADC is working properly temperatures between -40 °C to 120 °C. Higher values than 120 °C causing missing codes as illustrated in Table 4.1.

Table 4.1. Detailed Temperature Simulation Results

Temperatures	OUTPUTS																											
-40°C	11	11	20	32	50	63	63	52	34	15	3	2	13	31	50	63	63	52	34	15	3	2	13	31	50	63	63	
-20°C	12	11	20	32	50	62	63	52	34	15	3	2	13	31	50	62	63	52	34	15	3	2	13	31	50	62	63	
0°C	12	12	20	32	50	62	63	52	34	15	3	2	13	31	50	62	63	52	34	15	3	2	13	31	50	62	63	
20°C	13	12	20	32	50	62	63	52	34	15	3	2	13	31	50	62	63	52	34	15	3	2	13	31	50	62	63	
40°C	13	12	21	32	50	62	63	52	34	15	3	2	13	31	50	62	63	52	34	15	3	2	13	31	50	62	63	
60°C	13	13	21	32	50	62	63	52	34	15	3	2	13	31	49	62	63	52	34	15	3	2	13	31	49	62	63	
80°C	14	13	21	32	50	62	63	52	34	15	3	2	13	31	49	62	63	52	34	15	3	2	13	31	49	62	63	
100°C	14	13	21	31	49	62	63	52	34	16	3	2	13	31	49	62	63	52	34	16	3	2	13	31	49	62	63	
120°C			21	31	49	62	63	52	35	16	3	2	12	31	49	62	63	52	35	16	3	2	12	31	49	62	63	
125°C			21	31	49		63	52	35	16		2	12	30	49		63	52	35	16		2	12	30	49		63	

sample time (ns)	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

4.3. POWER CONSUMPTION

Total power consumption of designed 1 GS/s 6-bit flash analog-to-digital converter is 276.39 mW. Detailed power consumption of the all circuit is given in Table 4.2.

Table 4.2. Distribution of Power Consumption

Circuits	Power Consumption	# of Circuits	Total
Preamplifier	2.5 mW	64	160 mW
Comparator	250 µW	63	15.75 mW
Current Comparator	269 µW	63	18.64 mW
Latch	14 mW	1	14 mW
Current Reference	72 µW	63	4.5 mW
T/H	8.3 mW	2	16.6 mW
Resistor String	1.1 mW	2	2.2 mW
ROM	0.8 mW	1	0.8 mW
Bias for preamplifier	5.8 mW	1	5.8 mW
Bias for comparator	6.7 mW	1	6.7 mW
Bias for T/H	9.7 mW	2	19.4 mW
Bias for Current Ref.	12 mW	1	12 mW

Maximum power consumption is performed by preamplifier circuits with 57,9%. The preamplifier is the key circuit to reach 1 GS/s sampling rate and 6-bit resolution. Higher bandwidth and gain need higher power. Distribution of power consumption is also shown in percentile zones in Figure 4.5.

The total power consumption's transient simulation is shown in Figure 4.6.

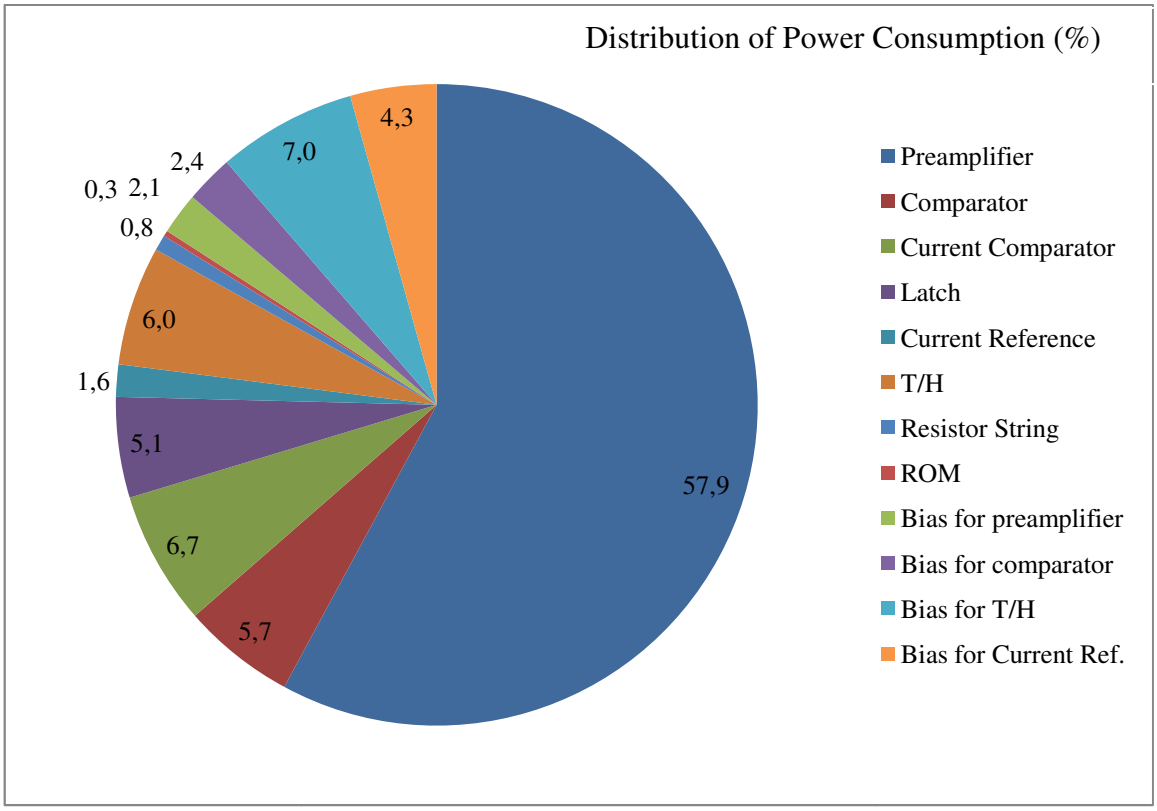

Figure 4.5. Power consumption distribution with percentile zones

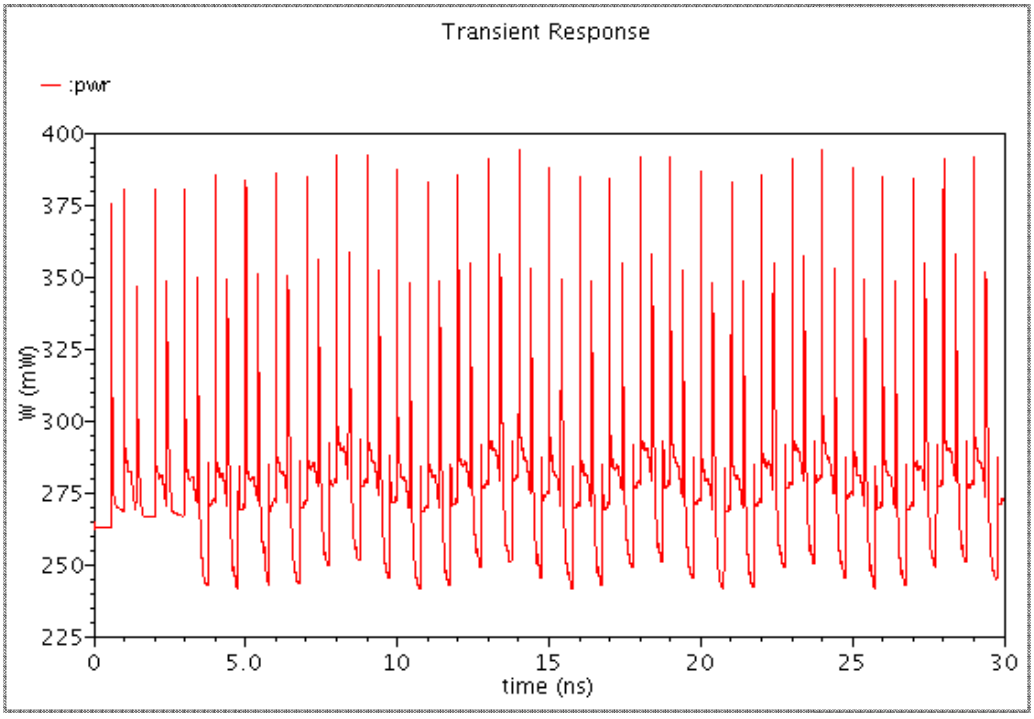

Figure 4.6. Total power consumption with respect to time at 1 GS/s [25]

5. CONCLUSION

This thesis presents a Flash Analog-to-Digital Converter structure which consists of novel voltage comparators and a decision circuit. When Flash ADC is considered without track-and-hold circuit in conventional structures, input signal is directly connected to the inputs of the comparators. Therefore, the speed of Flash ADC is limited by the comparators [18]. In this thesis, the designed novel voltage comparator and the decision circuit provide high sampling rates such as 1GS/s. Also, this Flash ADC architecture eliminates thermometer coding. Outputs of comparators do not need to be encoded by another circuit, as only one comparator produces a "1" in 2^N-1. Therefore, this structure besides avoids a bubble error which is a major cause of bit errors for high speed Flash ADCs [22].

As a result, fully differential, 6-bit, 1 GS/s Flash Analog-to-Digital Converter is designed in TSMC 180nm CMOS technology for 1.8 V operation. A double sampling T/H circuit is used as front-end circuit to avoid signal degradation. Verification of all system has been carried out by simulations. Total power consumption of Flash ADC is 276.39 mW. Designed converter can operate in wide temperature range -40 °C to 120 °C.

Some published performance metrics of Flash ADCs which are designed in 180nm CMOS technology, are compared with this work in Table 5.1. In reference [3], Flash ADC operates at 1.95 V and needs 2.35 V digital supply to reach 1.6 GS/s, because of that it has high power consumption. Another Flash ADC, which has high power consumption rate, is given in reference [19]. This Flash ADC reached 1GS/s sampling rate with time interleaved method. Work in reference [22] has higher sampling rate and it reaches these values by using distributed track-and-hold pre-comparators and modified encoder. Modified encoder is solving bubble error problems with applying "clustering method" [23]. This work also overcomes speed limitations by inserting clocked timing buffers into the encoder circuits. Works in references [20] and [21] have lower resolution values against to other works. Reference [20] has minimum power consumption, as it is 5-bit and its architecture provides conversion capability with 15+1 comparators instead of 31. Reference [21] has higher power consumption than [20]. However work in [21] reaches

4GS/s for 4-bit conversion. Therefore, all these Flash ADCs have different solutions on comparator and encoder structures to reach high sampling rates.

Table 5.1. Performance metrics of some Flash ADCs

References	This work	[3]	[20]	[21]	[19]	[22]
Publication Year	-	2002	2007	2007	2008	2009
Technology	180 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS
Supply Voltage	1.8 V	1.95 V-2.35 V	1.8 V	1.8 V-2.5 V	1.8 V	1.8 V
Resolution	6-bit	6-bit	5-bit	4-bit	6-bit	6-bit
Sampling Rate	1 GS/s	1.6 GS/s	1 GS/s	up to 4 GS/s	1 GS/s	1.6 GS/s
Input Signal Frequency	up to 500 MHz	up to 660 MHz	up to 500 MHz	up to 1.5 GHz	up to 500 MHz	up to 793 MHz
Power Consumption	276.4 mW	328 mW	63 mW	530 mW	550 mW	300 mW
Temperature	-40 °C to 120 °C	-	-	-	-	-

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