ACTIVE FREQUENCY MULTIPLIER by 8 MMIC in SiGe HBT TECHNOLOGY

by
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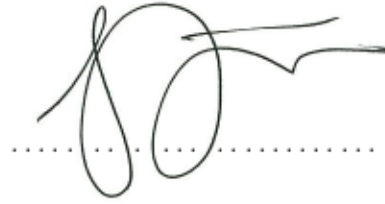Electrical and Electronics Engineering

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ABSTRACT

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Generation of low phase noise RF signals is crucial for a range of applications including communication systems and radars. Doppler radar is a type of radar that estimate the velocity of object by the help of Doppler effect. Slow moving objects causes small Doppler shifts relative to the fast moving objects in reflected signal's frequency. Thus resolvability of the radar is directly related to phase noise of signals. This thesis focuses on the design of low phase noise active frequency multiplier by 8 in SiGe HBT technology. Multiplier core consists three cascaded mixers which are used as a frequency doubler. The mixer topology used in this thesis is the Gilbert mixer, one of the most popular mixer topologies in the literature. This thesis also covers the design of automatic gain control loop which is used to ensure constant output power for various input power conditions.

ÖZET

SiGe HBT TEKNOLOJİSİNDE AKTİF FREKANS ÇARPICI

Düşük faz gürültülü RF işaret üretimi bir çok uygulama için oldukça önemlidir. Bu uygulamalara modern komünikasyon sistemleri ve radar uygulamaları örnek verilebilir. Doppler radar, hareketli cisimlerin hızlarını Doppler etkisinden faydalanarak tespit eden bir radar çeşididir. Yavaş hareket eden cisimler, hızlı hareket eden cisimlere göre yansıyan işaret üzerinde görece daha az faz kaymasına sebep olmaktadır. Bu nedenle radarın çözünürlüğü işaret kaynağının faz gürültüsü ile doğrudan orantılıdır. Bu tez SiGe HBT teknolojisinde ürettirilen aktif sekize çarpıcı tümdevresinin tasarımını incelemektedir. Literatürdeki en popüler karıştırıcılardan biri olan Gilbert karıştırıcı, sekize çarpıcı devrede frekans katlayıcı olarak kullanılmıştır. Tezde ayrıca farklı giriş güçleri için sabit çıkış gücü elde etmek amacıyla tasarlanan otomatik kazanç kontrol çevrimi ve ona bağlı çevre blokları olan tepe sezici, gerilim kontrollü kazanç katı ve sayısal analog çeviricinin tasarımı incelenmektedir.

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LIST OF SYMBOLS/ABBREVIATIONS

SRD   Step Recovery Diode

NLTL   Nonlinear Transmission Lines

PLL   Phase-Locked Loop

VGA   Variable-Gain Amplifier

DAC   Digital to Analog Converter

GSG   Ground Signal Ground

GSGSG   Ground Signal Ground Signal Ground

PPF   Poly Phase Filter

SSB   Single Sideband

MMIC   Monolithic Microwave Integrated Circuit

HBT   Heterojunction Bipolar Transistor

1. INTRODUCTION

This thesis documents the work done on design, and testing of an active frequency multiplier MMIC in SiGe HBT Technology. The motivation of this work and an overview of the existing frequency multiplication techniques are described in this chapter. Technical specifications of the target multiplier are also described in this chapter. The first phase of the work involves two prototype dies. Their design, simulation and testing are described in chapter 2. The second phase of the work involves final prototype die that consist of modifications according to the the first phase dies testing. Its design, modifications and testing are described chapter 3. Chapter 4 concludes the thesis with a summary of the performances of final prototype and possible improvements and future work are also discussed.

1.1. MOTIVATION

Realizing a 9520 MHz signal with a phase noise performance better than -130 dBc/Hz at 1 kHz offset is the ultimate aim of this work. A low phase noise high frequency signal can be synthesized by either:

(a) using an exotic high frequency resonator, or

(b) multipliying the frequency of an ordinary crystal resonator.

A comparative evaluation of these two techniques is possible through the expression [6].

$$\frac{N_{op}}{C} \propto \frac{f_o^2}{Q^2} \tag{1.1}$$

where $\frac{N_{op}}{C}$: is the single sideband phase noise density to carrier ratio, f_o : is the carrier frequency and Q : is the quality factor of a resonant circuit.

Due to physical characteristic of piezoelectric devices, maximum frequency of quartz crystal resonators is limited around 150 MHz [7] and its optimal phase noise performance is at around 100 MHz [8]. Instead of using quartz crystal resonators, using higher frequency resonator causes lower phase noise charateristic because of both high frequency and lower Q values [6]. This makes using frequency multiplier inevitable to get higher frequency signals. Effect of frequency multiplication on phase noise can be formulated as in equation (1.2). As a result of this identity, input signal phase noise will be degraded by about 18 dB after 8 factor frequency multiplication.

$$N_{addition} = 20log(M) \tag{1.2}$$

Instead of using crystal resonator and multiplier, high frequency signal can be directly synthesized by using more complex resonators such as: optical electronic oscillator using fiber-delay-line resonator, dielectric resonator oscillator (DRO), sapphire-loaded cavity stabilized oscillator (CSO), optical femtosecond-comb divider with calcium stabilized reference oscillator [5]. However these resonators are not cost efective and has not got small form factors. Obviously, frequency multiplication is a more convenient way of creating high frequency signals due to these reasons.

1.2. FREQUENCY MULTIPLICATION OVERVIEW

1.2.1. Step Recovery Diode (SRD) Frequency Multiplication

Step recovery diodes are highly non-linear devices. During forward bias cycle they have high capacitance and during reverse bias cycle they have low capacitance values. Utilizing this non-linear behaviour, SRDs can be used as a harmonic generator. Main problem with SRD frequency multiplication is selecting the desired harmonic frequency component while suppressing the unwanted ones. There are also limited range of input frequency and power. Step recovery diodes are specially designed and manufactured

as discrete components, and are not feasible for integrated circuit design. Since the scope of this thesis is integrated circuit frequency multiplier design, SRD frequency multipliers are not viable [9–13].

1.2.2. Nonlinear Transmission Lines (NLTL) Frequency Multiplication

Essentially, nonlinear transmission lines are used as a pulse sharpener to produce picosecond pulse and comb generator(harmonic generator). There are several publications related to pulse compression and frequency multiplication using NLTL [13–16]. Nonlinear transmission lines can be realized as an artificial transmission line by replacing the capacitor with varactors as seen in Fig. 1.1. These varactors can be realized using reverse biased diodes or CMOS transistors. Because of the superior performance of Schottky diode(lower breakdown, higher ft), they are preferred over regular pn junctions diodes [17, 18]. Although the majority of the previous works involve Schottky diodes and NLTLs in GaAs technology, there are a few papers reporting Schottky diodes in SiGe technology [19].

During the last 5-10 years period, there has been an increase in the number of publications reporting NLTLs fabricated at standard CMOS process. These works involve, nodes varying between 65 nm and 0.25 um and frequency as high as 160 GHz [15,20–24].
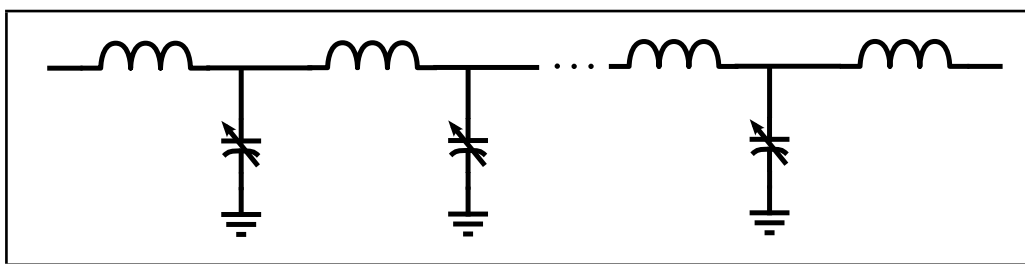
Figure 1.1: Nonlinear transmission lines

Following are the problems associated with NLTL frequency multiplication.

- Requires a high input power (> 10 dBm)
- Causes a high conversion loss (> 25 dB)
- Selecting the desired harmonic and suppressing the unrelated ones requires high order filters.

- System performance is highly sensitive to varactor's parameters [17].

To overcome these problems, gain blocks and bandpass filters should be added to the system as seen in Fig. 1.2.
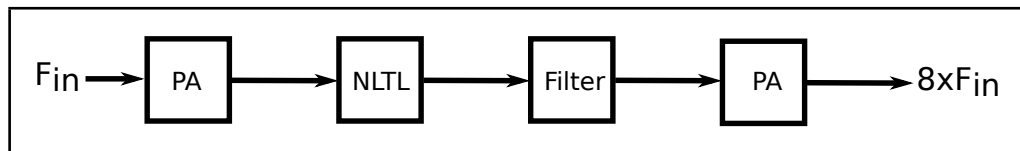
Figure 1.2: NLTL system design

1.2.3. Phase Locked Loop

Probably the most popular method for frequency synthesis is using a phase-locked loop (PLL). Main components of PLL can be seen in Fig. 1.3. The fundamental PLL consists phase/frequency detector (PFD), charge pump, low-pass filter, voltage controlled oscillator (VCO) and frequency divider. VCO generates a signal whose frequency is proportional to a control voltage. This control voltage is created by PFD and charge pump. PFD compares reference signal with output signal generated by VCO, and in turn generates an error voltage. Unwanted high frequency signals are suppressed by the low-pass filter. As a result of the closed control loop, the phase of the input reference signal and the VCO output signal are synchronized. Phase noise performance is dominated by reference signal's phase noise at low frequencies and by VCO's phase noise at higher frequencies. This behavior can be observed in Fig. 1.4, 1.5, and 1.6 which are reported in three separate publications [1], [2], [3]. Notice the peak or flat area where the VCO starts to dominate phase noise performance. Location of this peak is purely determined by the loop bandwidth of the PLL.
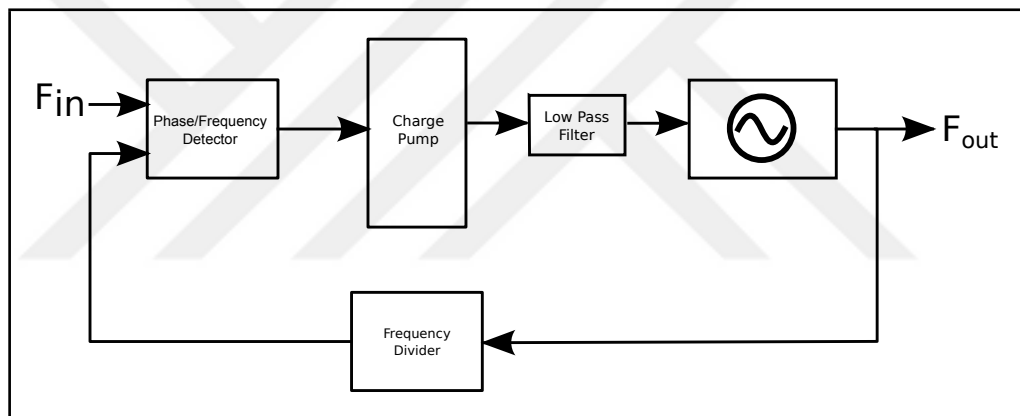
Figure 1.3: Phase locked loop.
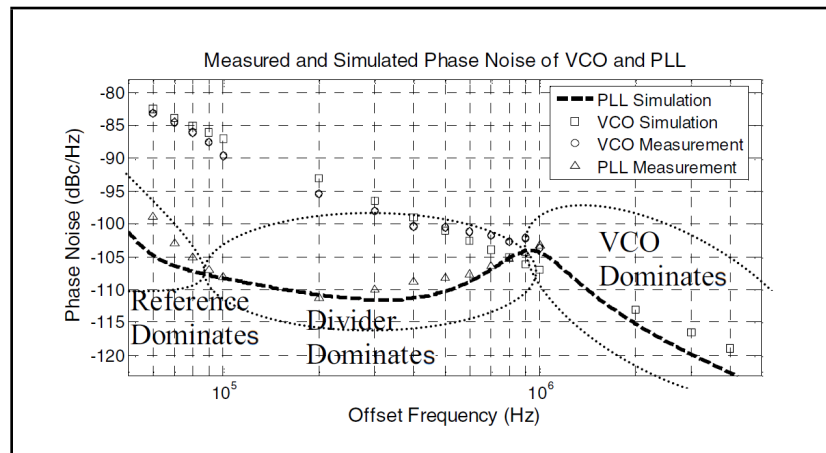
Figure 1.4: Phase noise performance according to [1]
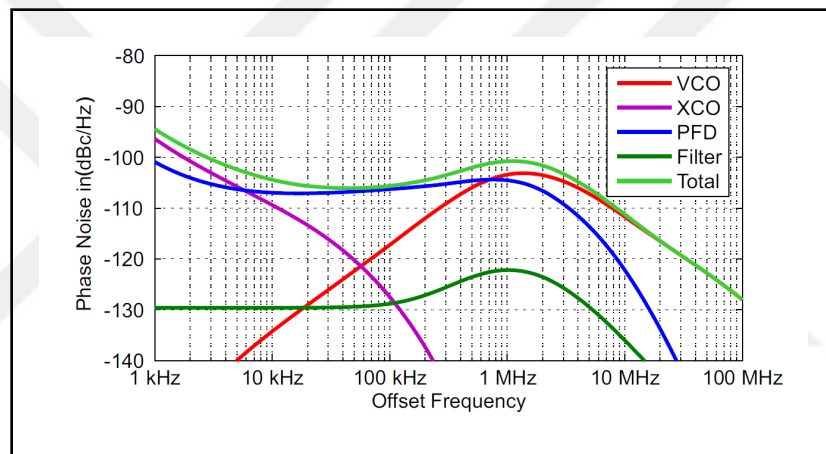
Figure 1.5: Phase noise performance according to [2]
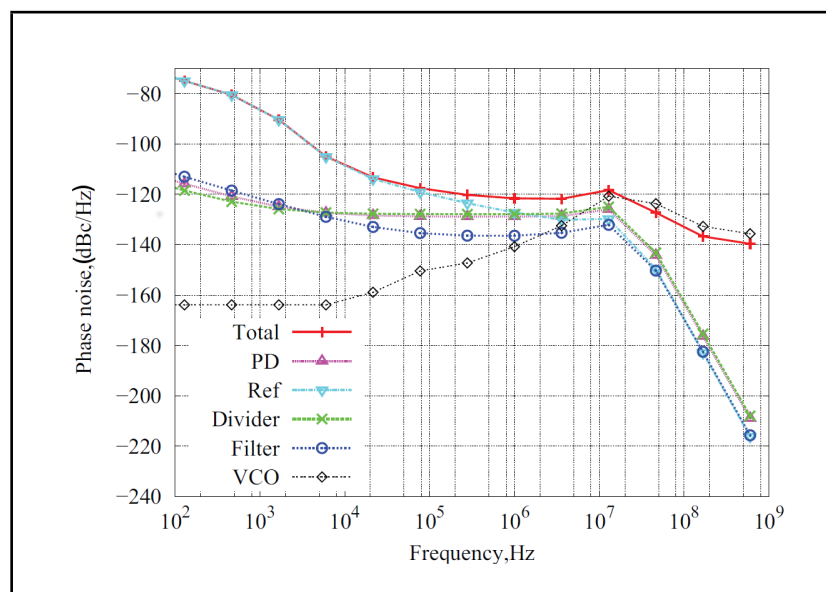
Figure 1.6: Phase noise performance according to [3]

1.2.4. Mixer Based Frequency Multiplication

Mixer is a non-linear device that produces new frequency component from signals applied to it. Input frequencies and corresponding output frequencies are shown in Fig. 1.7. If two signals with identical fundamental frequency are applied to RF and LO ports of the mixer, it will generate an output signal with double the input frequency. Mixers are extensively used as frequency doublers or triplers by using this identity [25–27].
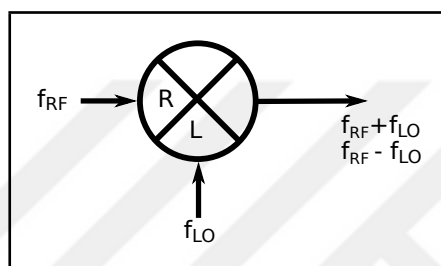
Figure 1.7: Ideal mixer

1.3. PROPOSED TOPOLOGY

1.3.1. Target Specification

Target specification of chip is listed in Table 1.1. Reference commercial product Hittite HMC444LP4 specifications is also listed in given table.

Up to this point, frequency multiplication techniques are presented. Considering the target process technology in Section 1.3.2, mixer based multiplication topology is chosen as a candidate to realize our design.

1.3.2. Target Process Technology

For design and manufacturing, a 0.13 μm SiGe BiCMOS technology with $f_T = 250$ GHz and $f_{max} = 300$ GHz npn-HBTs transistors is chosen. The transistors with high f_T will provide design robustness at high frequencies. Their high breakdown voltages will make 0 dBm output power possible as well. Candidate technology also comprises

Table 1.1: Target specification

	Target Specification	Hittite HMC444LP4
Operating Voltage	4 V	5 V
Input Frequency	1190 MHz	1237.5 to 1400 MHz
Output Frequency	9520 MHz	9900 to 11200 MHz
Phase Noise	$\leq$ -130 dBc/Hz @ 1 kHz	-136 dBc/Hz @ 100 kHz
Input Power Range	-10 dBm to 5 dBm	-15 dBm to 5 dBm
Output Power	0 dBm ($\pm$ 1 dBm)	6 dBm
Sub-Harmonic Suppression	$\leq$ 30 dBc	25 dBc
Input Return Loss	$\leq$ 15 dB	22 dB
Output Return Loss	$\leq$ 10 dB	7 dB
Operating Temperature	-40°C to 85°C	-40°C to 85°C

low voltage and high voltage PMOS and NMOS transistors. CMOS transistors can be used at logic portion of chips. As for passive components, there are several type of resistors with different sheet resistances and thermal coefficients and MIM(Metal Insulator Metal) capacitor. Technology also offers two layers of thick metal. Thanks to these thick metals, high Q and low loss inductors can be manufactured.

1.3.3. Evolution of Design

After choosing the mixer based topology, our next decision, is on the factor of frequency multiplication assigned to each stage. Targeted overall frequency multiplication is 8. There are different multiplication factor configurations that can be used in mixer based topology. Three of them can be seen in Fig. 1.8.

Multiplication by 4 using mixers requires design of harmonic mixers. Complexity of harmonic mixers are relatively higher than conventional mixers. Thus we have decided to use multiplication factor as 2 and the number of cascaded mixer stages as 3. After this decision system design has become as seen in Fig. 1.9.
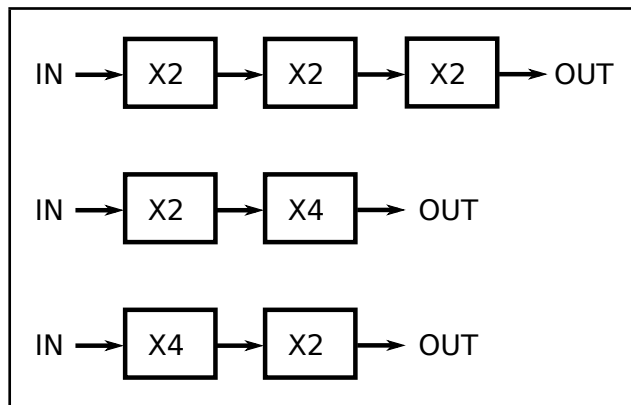
Figure 1.8: Different multiplication factor configurations
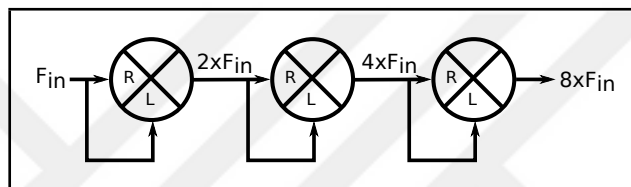
Figure 1.9: System level evolution 1

From mathematical perspective, mixing operations is identical to multiplication. So the mathematical representations of mixing operation can be written as follows. From electrical perspective the constant $\frac{1}{2}$ in (1.3) means DC unbalance in mixers. DC unbalance in mixers causes increase in harmonic contents of output signal. Since the harmonic power level is yet another specifications, this is not desired.

$$\sin(\Theta) * \sin(\Theta) = \frac{1}{2} - \frac{1}{2}\cos(2\Theta) \tag{1.3}$$

Instead of multiplying two sine, multiplying a sine and a cosine removes the constant as seen in (1.4).

$$\sin(\Theta) * \cos(\Theta) = \frac{1}{2}\cos(2\Theta) \tag{1.4}$$

From electrical perspective, to convert a sine into cosine requires 90° phase shift. With the addition of these additional blocks, system design evolves into what is shown in Fig. 1.10.
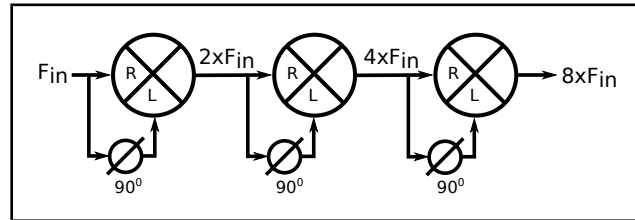
Figure 1.10: System level evolution 2

Since the harmonic content of the multiplied output signal is another design concern, using double balanced mixer seems a good choice. This requires converting the original single-ended input signal to a differential signal and doing the opposite at the end of the frequency conversion as shown in Fig. 1.11.
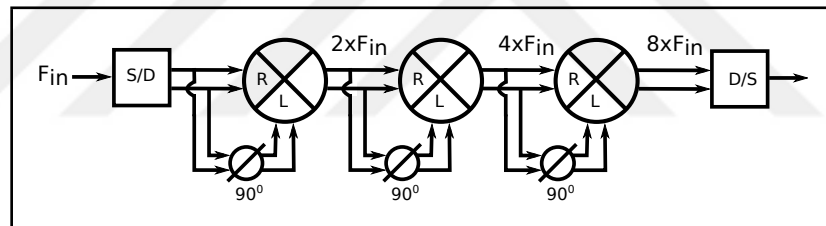
Figure 1.11: System level evolution 3

As seen in (1.4), each frequency multiplication halves the signal level. This results in a 9 dB loss in the output signal power level. The loss in power can be compensated either adding gain to each mixer or using a power amplifier at the end of the conversion. We adopted a hybrid approach in which each mixer is furnished with a certain amount of gain and an additional gain stage is added at the end of the chain as shown in Fig. 1.12.

In Table 1.1, it is stated that the output power level should be 0 dBm regardless of the input power level. One way of achieving constant power at the output is to saturate (clip) each stage's output at 0 dBm. Another way of fulfilling this requirement is to use a variable gain amplifier (VGA) that can control its gain according the power level of the output. Sensing the power level can be done by peak detectors. Indeed a peak detector simply creates a DC signal at its output proportional to its input power level.
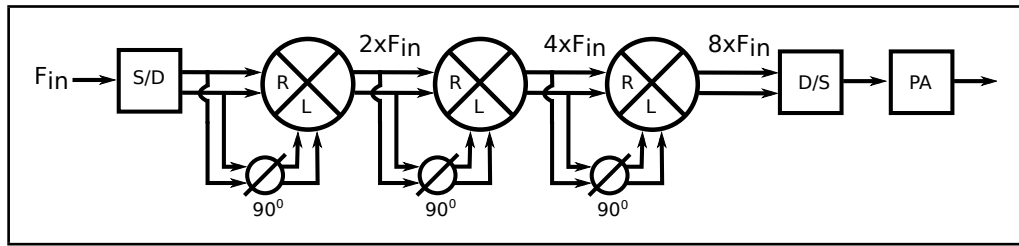
Figure 1.12: System level evolution 4

After that, created DC signals can be compared with a certain reference and hence the gain of VGA can be set.

Setting the gain of VGA necessitates a control loop that adjusts the VGA's control signal. From control theory perspective, all closed loop systems have a risk of oscillation. Therefore, the stability of the control loop must be studied carefully. The traditional way of designing stable systems is to find the transfer function and hence determine the poles and zeros of system. There are several well-known theories for studying the stability of linear time invariant systems including Barkhausen, Nyquist or Routh-Hurwitz stability criterion. However the transfer function of mixers are non-linear; and it requires a more complex analysis [28].

Regardless of the linearity of the system, unconditional stability of the closed loop continuous-time system requires setting of the time constant of the loop extremely high relative to the response time of the system. Using continuous time control loop may have some drawbacks on overall system. There is a trade-off between simulation CPU time and loop time constant of continuous time systems. To simulate the settling behaviour may take unreasonable time such as on the order of days or weeks while using transient simulation. CPU time of transient simulator depends on several factors. One of them is maximum switching frequency of signals which are on the order of 10 GHz in the present case. For example, considering settling time of loop as $5\,ms$ means 50 million transition of 10 GHz signal. A Better way of simulating such a system is the circuit envelope simulation. However circuit envelope simulation was not among the simulation capability available to use. Instead of using continuous time system we decided to use a discrete-time system. Control loop consists on-chip reference generator,

comparator, digital control logic and digital to analog converter (DAC). Control loop works as follows. DC signal generated by peak detector is compared with DC reference signal generated by on-chip reference generator via comparator. If output power level is lower than 0 dBm, comparator generates logic low signal and if output power level is higher than 0 dBm, comparator generates logic high signal. Digital control logic decides to increase or decrease its digital output according to the comparator output signal. Generated digital signal is converted to analog signal and applied to variable gain amplifier (VGA) control inputs and it sets its gain. Avoiding possible stability problems and for staying on the safe side, control loop was not closed inside the chip. Digital control logic and comparator will be realized with discrete components on PCB. Finally system design evolves to what is shown in Fig. 1.13.
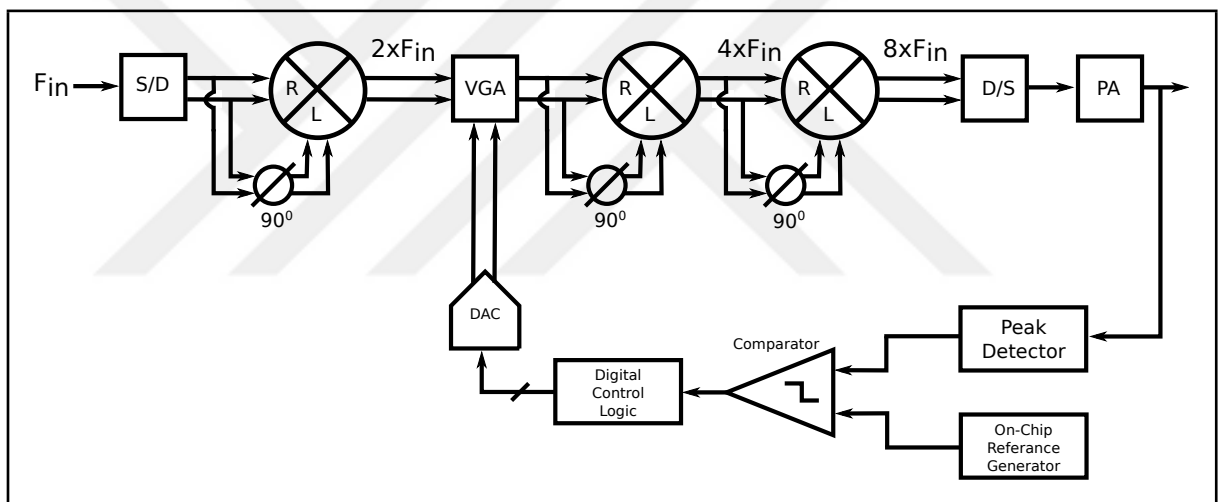
Figure 1.13: System level evolution 5

Considering the complexity of system it is divided into three pieces as seen in Fig. 1.14. Die 1 and Die 2 has been taped-out first and according to their measurement results Die 3 is taped out afterwards.
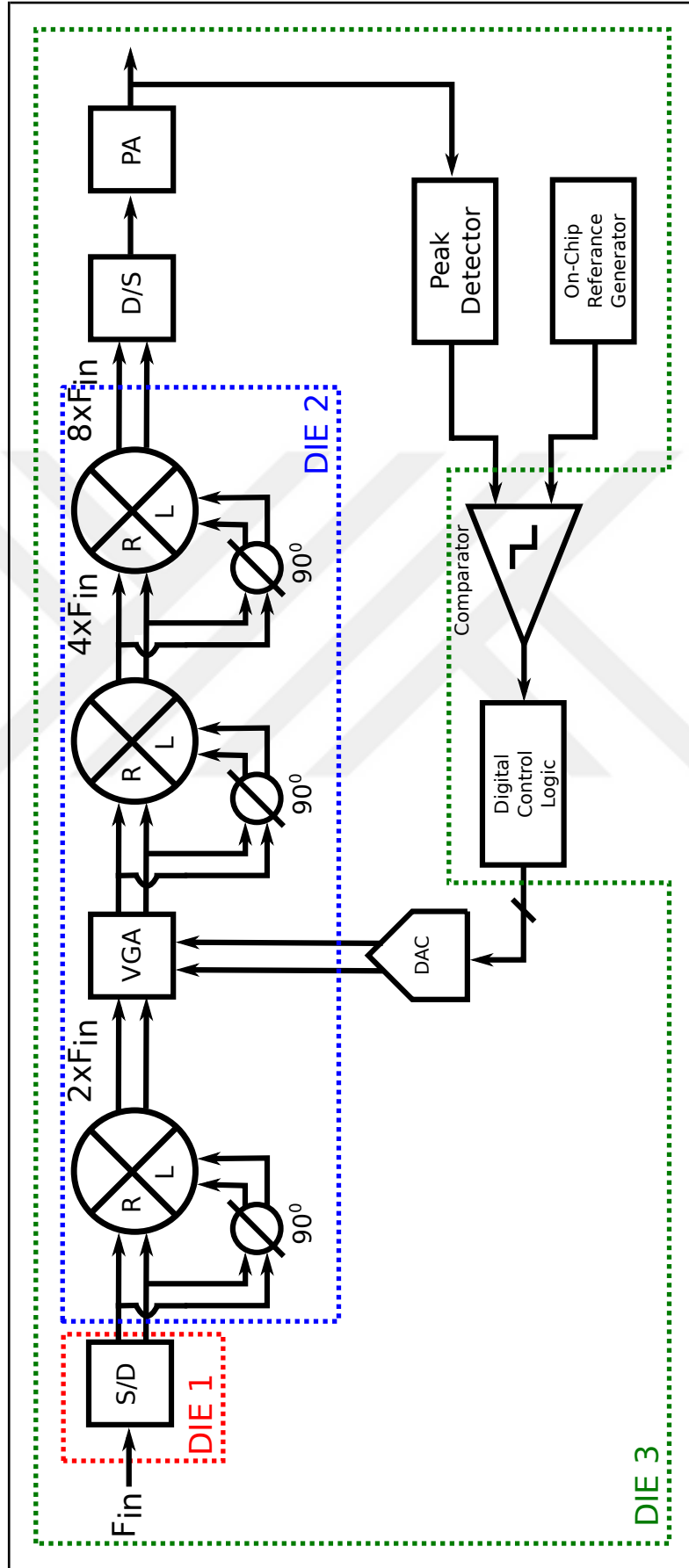
Figure 1.14: Fabricated dies

2. FIRST PHASE

2.1. GOALS of FIRST PHASE

Goals of the first phase include:

(a) the validation of the noise model of the devices provided by the foundry, and

(b) the validation of the performance the core circuitry, blocks, and the topology.

To fulfil these needs, testability of prototype is considered as first concern. The following steps are taken in physical design for increasing the test coverage of the prototype:

- Observation nodes (pads) were placed on the chip.
- All bias currents can be measured and adjusted from outside the chip
- All bias voltages can be measured and adjusted from outside the chip
- Supply voltages of different sub-blocks are separated by introducing dedicated pads
- Focused Ion Beam (FIB) facilities are introduced for debugging purposes such as separating cascaded sub-blocks, trimming passive components etc.

2.2. DIE 1 - THE BALUN

2.2.1. Design

Converting single ended signal to differential signals requires balun or transformer. Firstly, active balun topologies are examined. However every active device on signal paths has a negative impact on the phase noise performance. At target technology, emitter-collector breakdown voltage for high speed bipolar transistors is around 1.7 V. Considering the need to accommodate high input power level, a lossy passive balun was preferred. The rat-race hybrid coupler design of [29] is adopted. The schematic drawing of it can be seen in Fig. 2.1. Its ABCD-matrix is given by (2.1). Transmission

(ABCD) matrix is another set of parameters that can be used to represent two port networks like Z-parameters or Y-parameters. Since cascaded network two or more two-ports can be easily analyzed by multiplying the individual transmission (ABCD) matrices, it can be very useful especially in microwave network analysis.
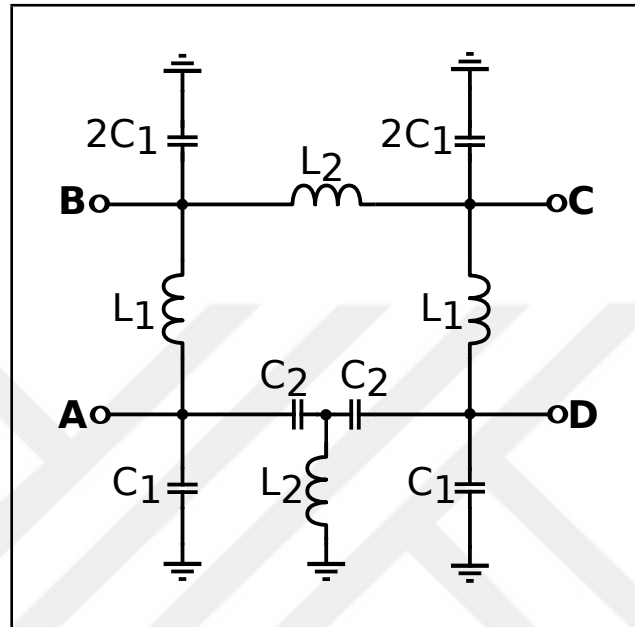
Figure 2.1: The rate-race hybrid coupler

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - \dfrac{1}{\omega^2 L_2 C_2} & \dfrac{-j}{\omega C_2}\left(2 - \dfrac{1}{\omega^2 L_2 C_2}\right) \\ \dfrac{-j}{\omega L_2} & 1 - \dfrac{1}{\omega^2 L_2 C_2} \end{bmatrix} \tag{2.1}
$$

Although the passive element values can be calculated from (2.1), results will not be satisfactory because of the parasitic inductances and capacitance . Since it will be used as balun, its fourth terminal is terminated with a resistor. An additional inductance is added to its input port in order to improve the input return loss. Resulting three-port device is shown in Fig. 2.2. Outputs are connected to poly phase filter in order to add loading effect on simulation and optimization process.
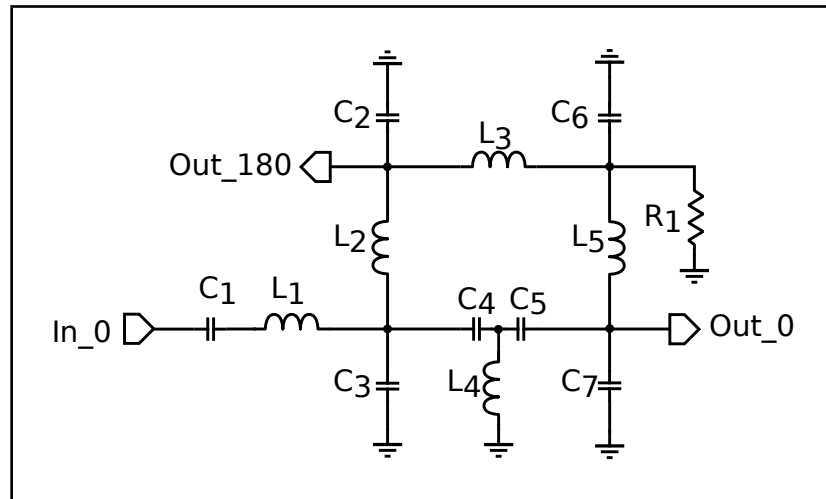
Figure 2.2: The balun

The component values are found by using Agilent's ADS optimization tool iteratively as follows:

1. Two optimization goals are determined :
   - Phase unbalance $< 5^o$
   - Amplitude unbalance < 1 dB

2. Using ideal components, simulation environment is created.

3. Using Agilent's ADS optimization tool and harmonic balance simulation, all element values are found for given goals.

4. Using Agilent Momentum 3D planar electromagnetic (EM) simulator, physical design of inductors are realized according to optimization results.

5. Physical design of balun is realized. EM simulation of whole balun was done.

6. Using Agilent's ADS optimization tool and harmonic balance simulation, all element values are optimized again by taking interconnect parasitics into account.

7. Physical design of balun is realized for new element values. EM simulation of whole balun is done again.

8. Using Agilent's ADS optimization tool and harmonic balance simulation, capacitors and resistor values are optimized again by taking interconnect parasitics into account with EM model of inductances.

9. Physical design of balun is realized for new element values. EM simulation of whole balun is done one more time.

Final component values are given in Table 2.1.

Table 2.1: Balun element values

C_1	3.45 pF	L_1	1.6 nH
C_2	0.7 pF	L_2	3.1 nH
C_3	0.29 pF	L_3	2.3 nH
C_4	2 pF	L_4	3.3 nH
C_5	3.55 pF	L_5	0.8 nH
C_6	11.82 pF	R_1	300 Ω
C_7	1.06 pF		

The final layout of the balun is given in Fig. 2.3. Final balun die dimension is 1.8 mm by 1.2 mm. Input and outputs of the balun are marked on the layout. All other pads are connected to ground plane.
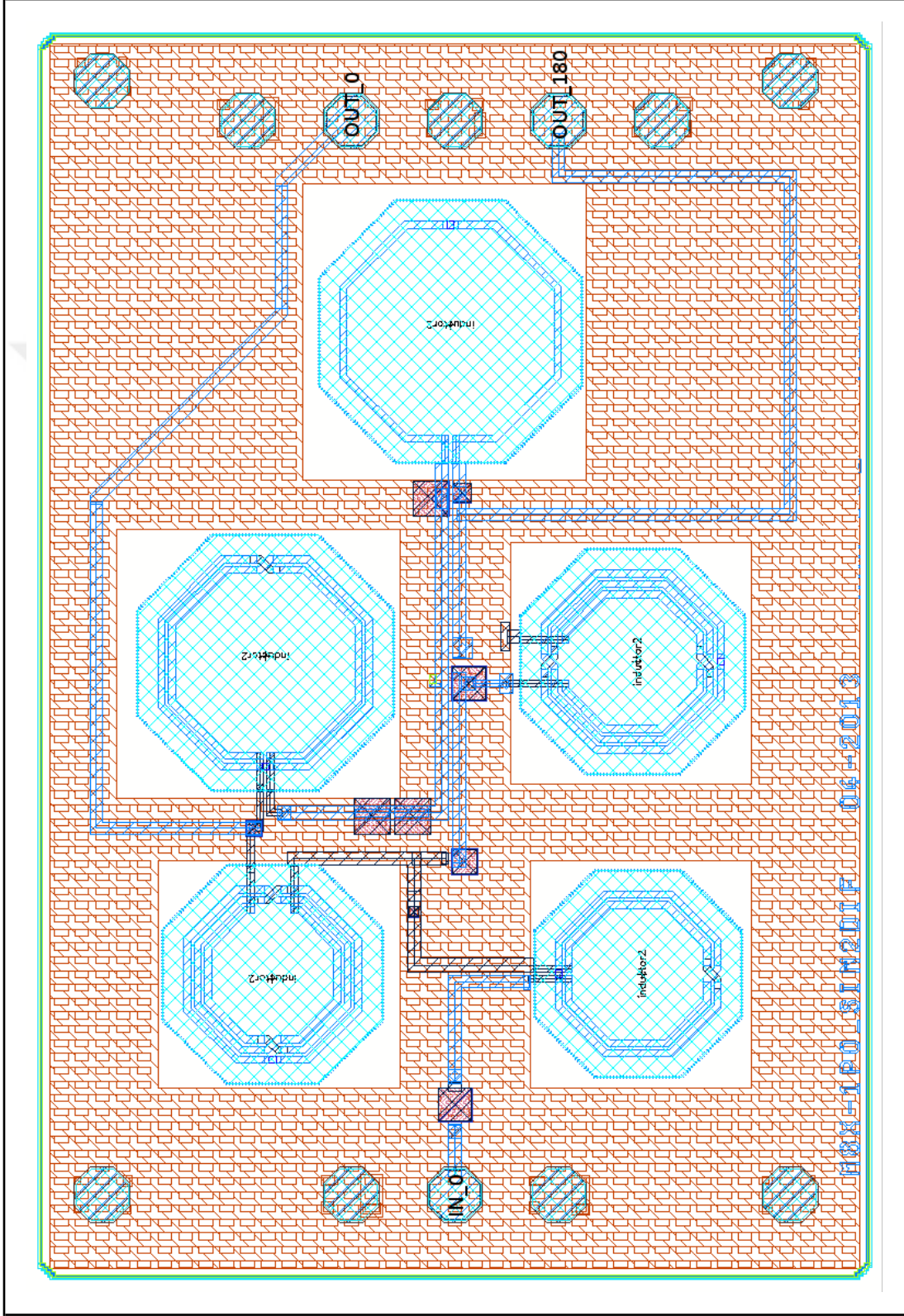
Figure 2.3: The layout of the balun

2.2.2. Simulation

After final optimization, EM model of the balun is created by Momentum EM simulation and is simulated using Agilent Harmonic Balance simulation. In Fig. 2.4, the transient input and outputs of the balun are plotted. In Fig. 2.5 and Fig. 2.6, the frequency spectrum of input and outputs were plotted. As seen in Fig. 2.6, amplitude imbalance is less than 1 dB. In Fig. 2.7, phase difference of outputs is plotted. As seen in that figure, phase imbalance is less than 2°. Since the balun will be at the input of the overall system, its input return loss becomes critical. Related plot can be seen in Fig. 2.8. Targeted input return loss is -15 dB, and simulation results satisfies this specification.

There is no concrete variation data for inductors provided by foundry. The inductor absolute value depends on the substrate thickness below inductor, metal width and thickness. However it is expected that the variations at these parameters will have negligibly small effects on the inductor value. Capacitor absolute value variation is expected around $\pm 10\%$ for corner cases. Designed balun is simulated for capacitance variation. Simulation results show that variation on capacitance value is acceptable for overall system performance.
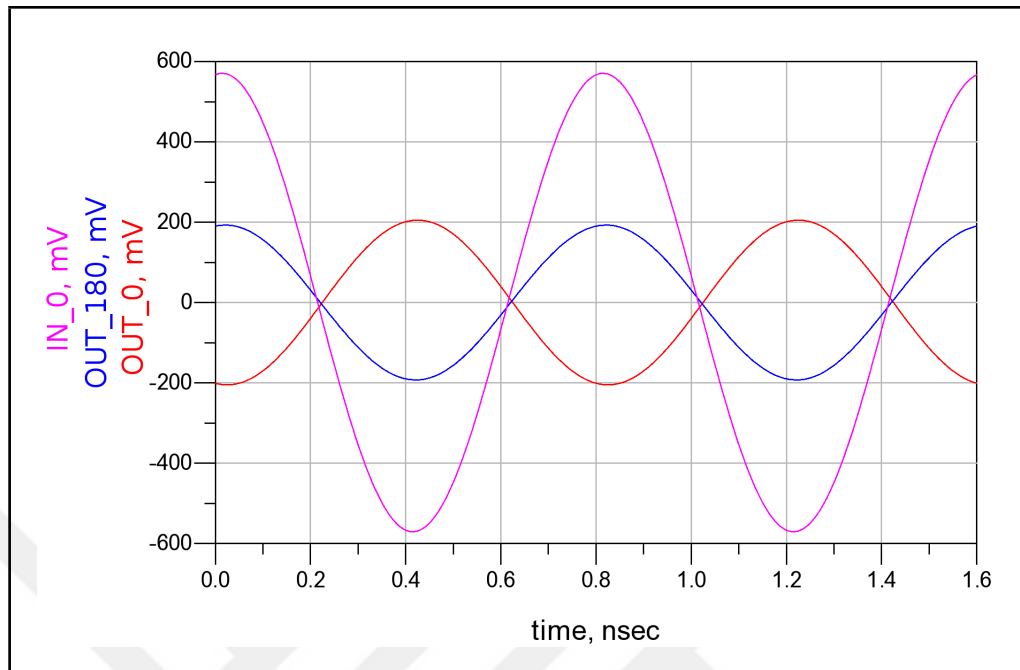
Figure 2.4: The transient input and outputs of balun
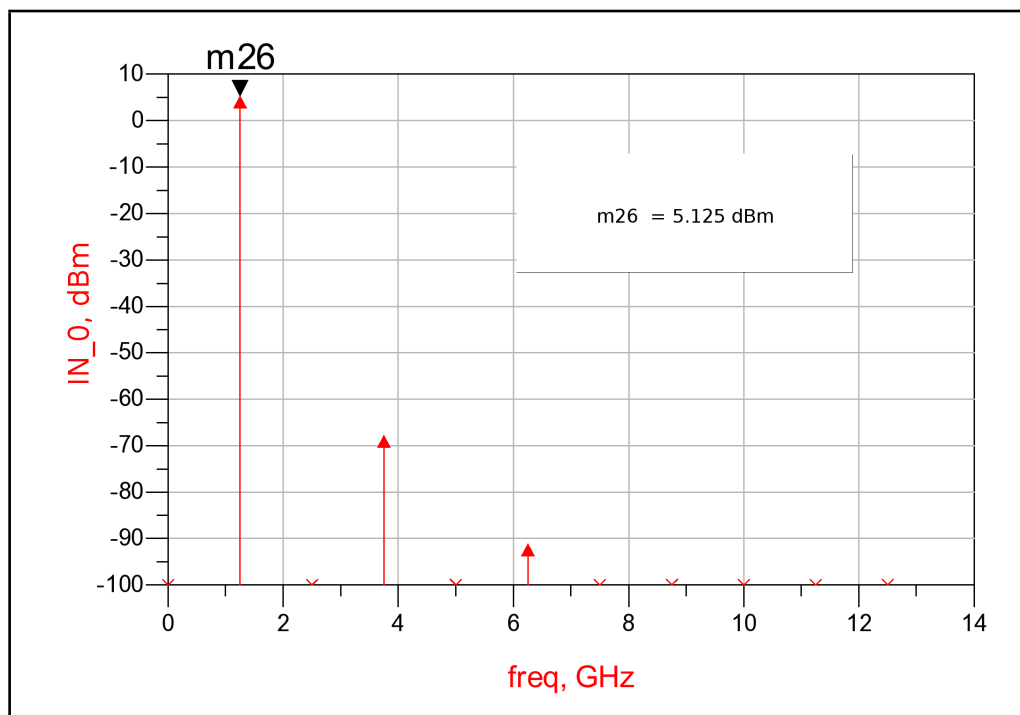
Figure 2.5: The input frequency spectrum of balun
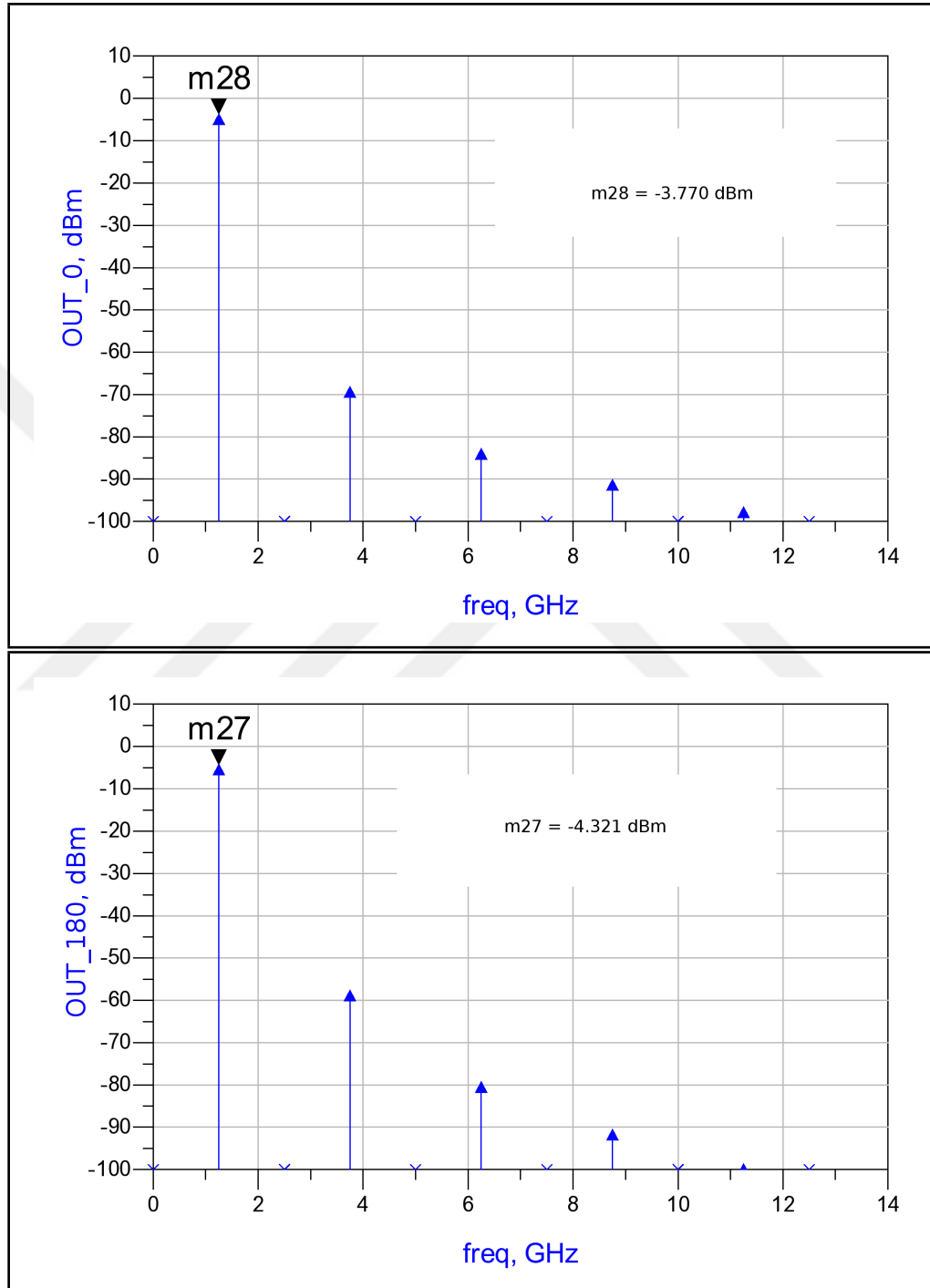
Figure 2.6: The output frequency spectrum of balun
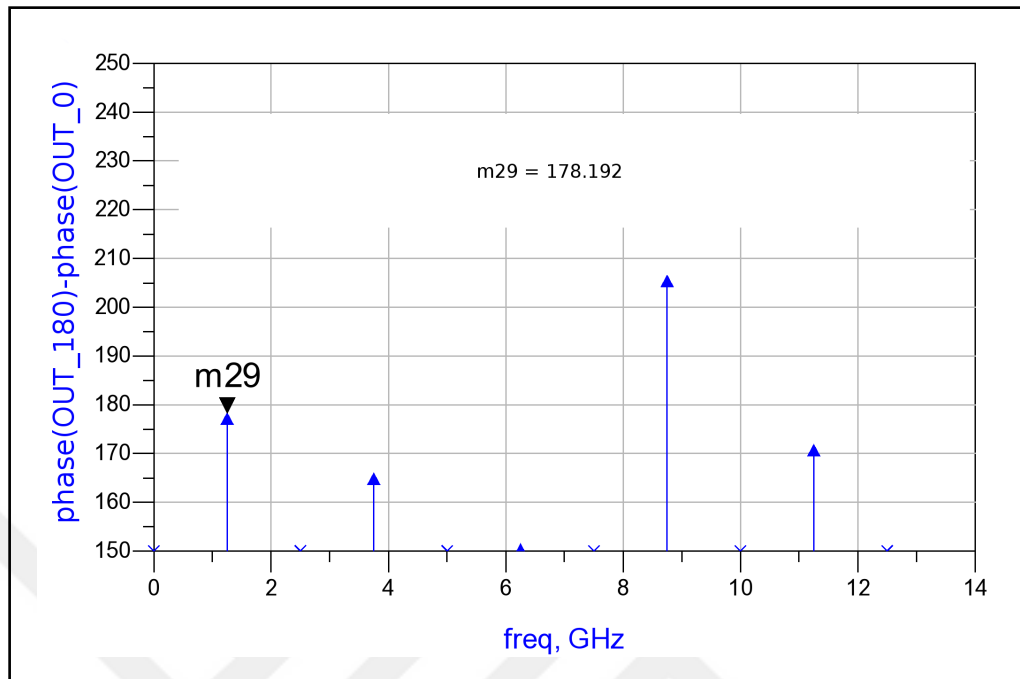
Figure 2.7: The output phase of balun
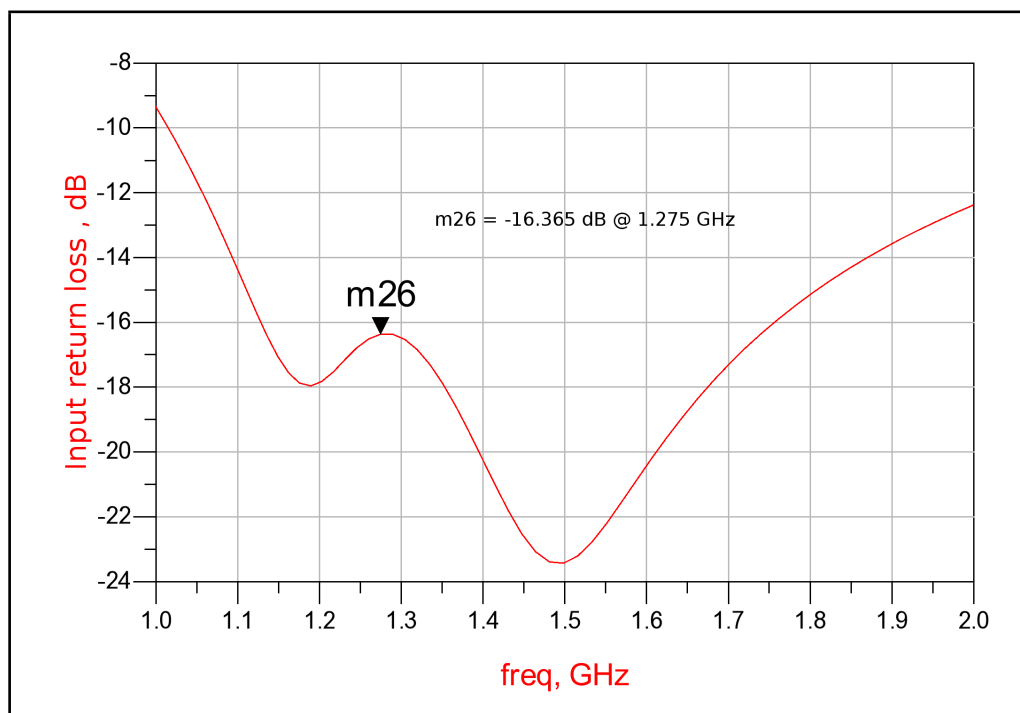
Figure 2.8: The input return loss of balun

2.2.3. Testing

The chip photomicrograph of the balun is given in Fig. 2.9. Input and outputs of balun are marked on it. Due to package parasitics, the balun is measured using RF probes and probe station without packaging. For this purpose balun die was first attached to a conductive carrier. For the input Picoprobe 110H-GSG-150-LP and for the output Picoprobe 67A-GSGSG-150-DP probes are used. For measurement, Agilent N5257A PNA Network Analyzer is used. After calibrating the network analyser with Picoprobe CS-5 calibration substrate, the balun is measured for different configurations. Related measurement setup can be seen in Fig. 2.10. As mentioned, the balun is designed with polyphase filter but taped out as an individual die. Therefore five different measurements are taken by terminating the idle port with 50 Ω termination or leaving it open and corresponding simulations are repeated for these configurations. All these measurements were taken on two different samples.
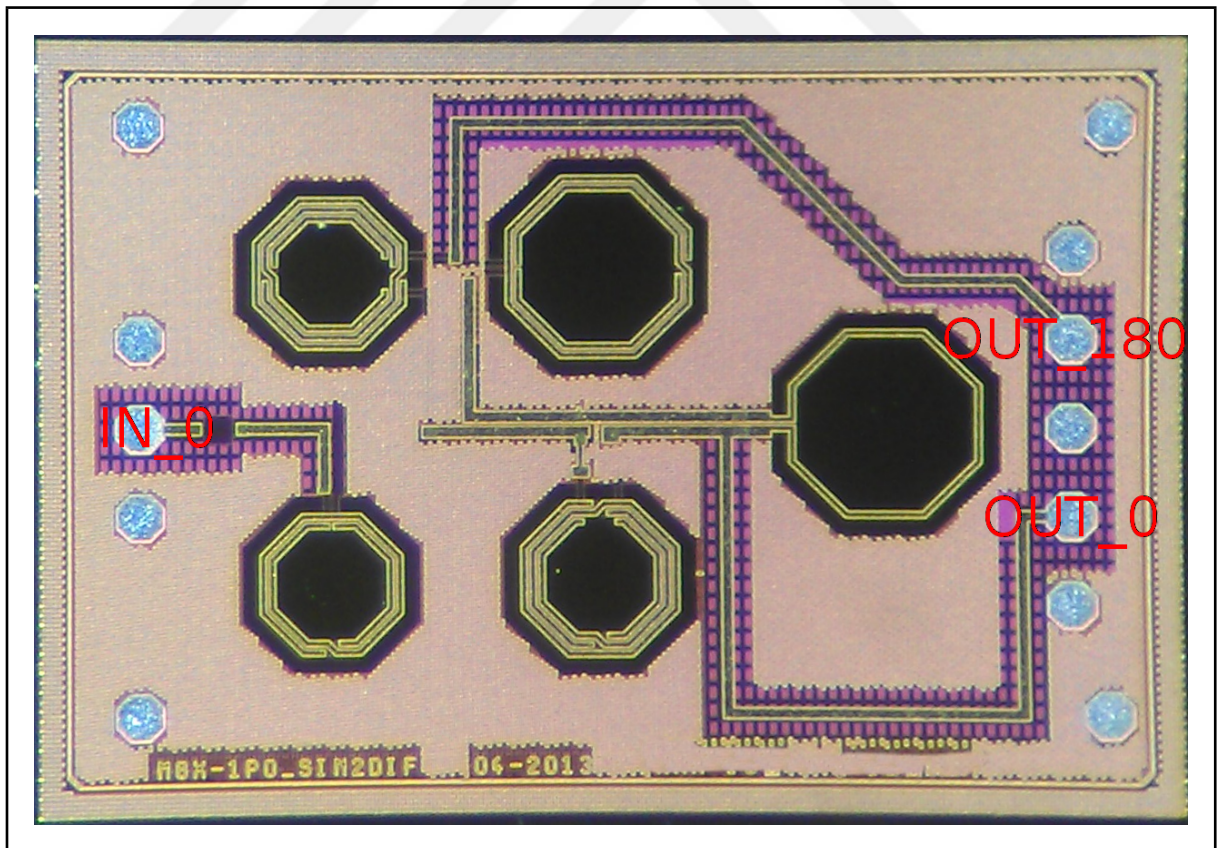
Figure 2.9: The chip photomicrograph of the balun
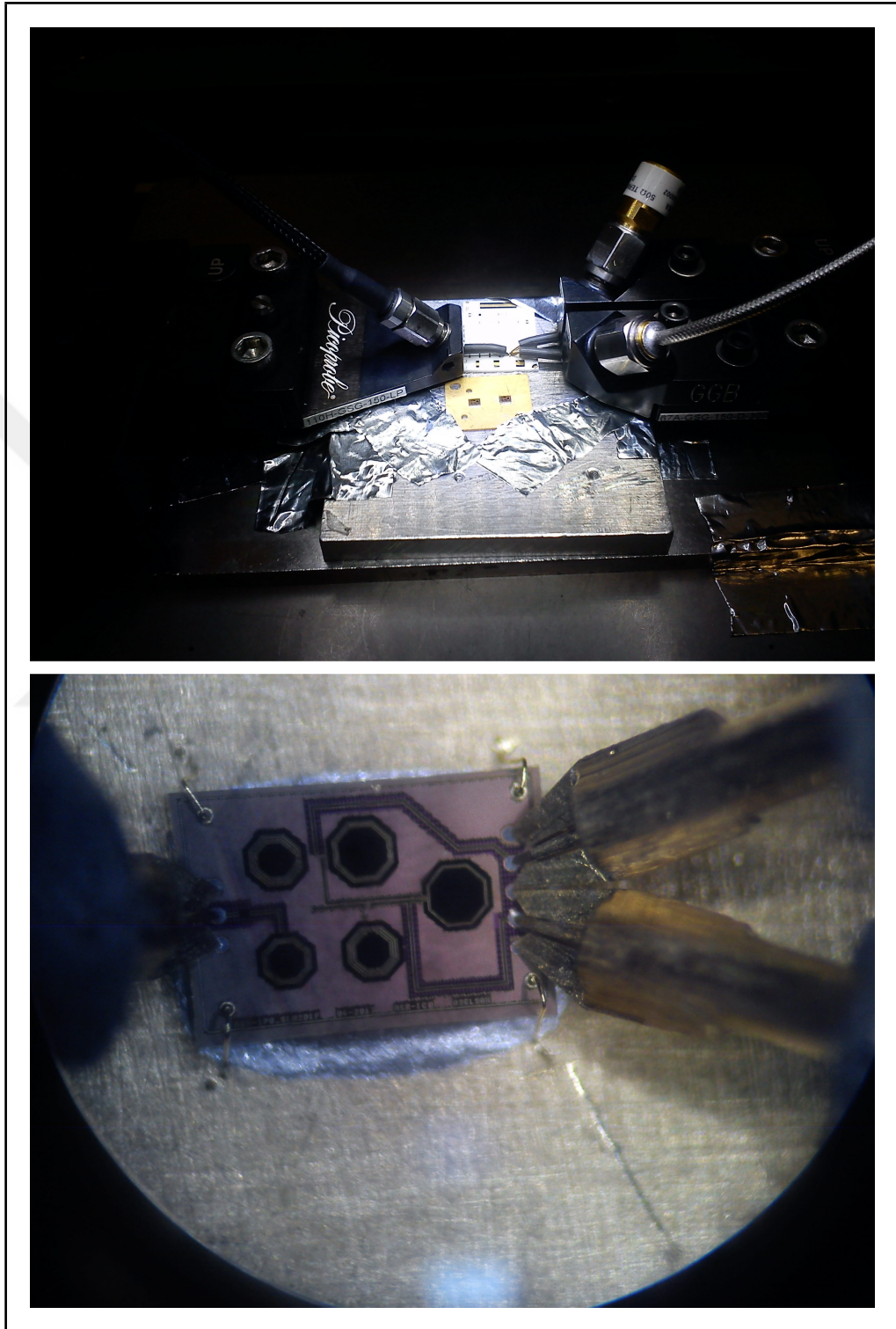
Figure 2.10: The measurement setup of balun

For measurement 1, idle terminal was terminated with 50 Ω. Related configuration and port numbers are given in Fig. 2.11. The original measurement results from network analyzer is in Fig. 2.12. To compare the measurement results, the same configuration is simulated with Agilent S-paramaters simulation and results are plotted in Fig. 2.13. In Fig. 2.13, red lines represent simulation results and the others are measurement of two different samples. Measurement results of the two samples show close correlation between samples. There is a slight difference between simulation and measurement of two samples. These differences may be due to the component variations. As seen in Fig. 2.13, peaks shift to lower frequency which is an indication of higher capacitor or inductor values.
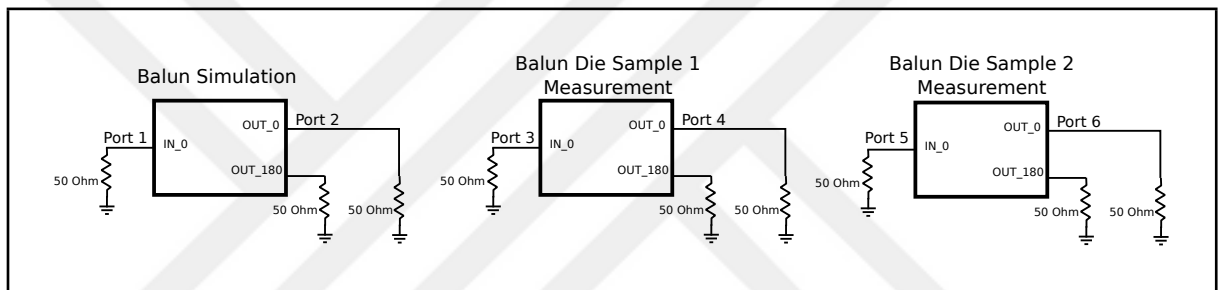
Figure 2.11: The measurement 1 configuration
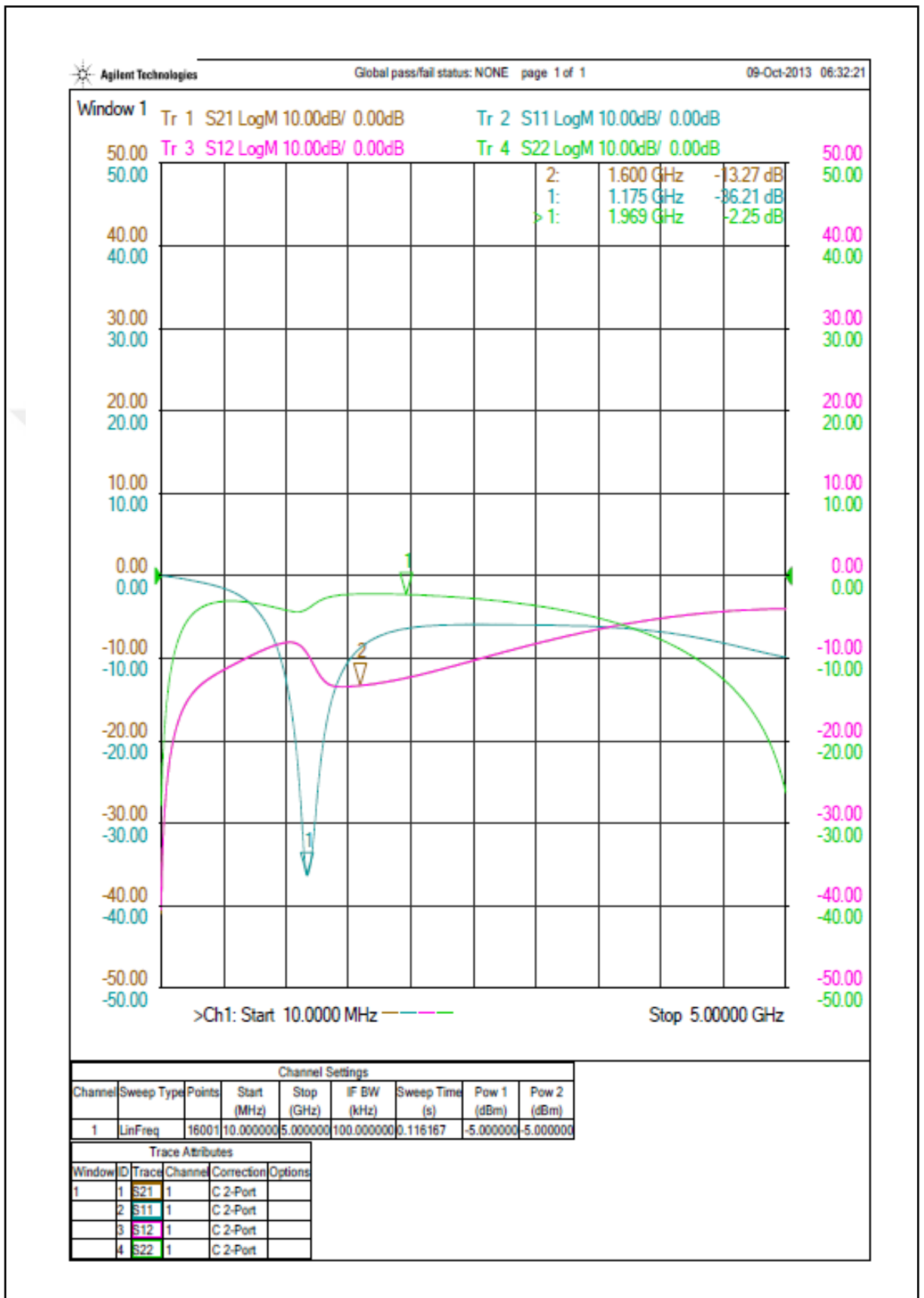
Figure 2.12: The measurement 1 original results from network analyzer
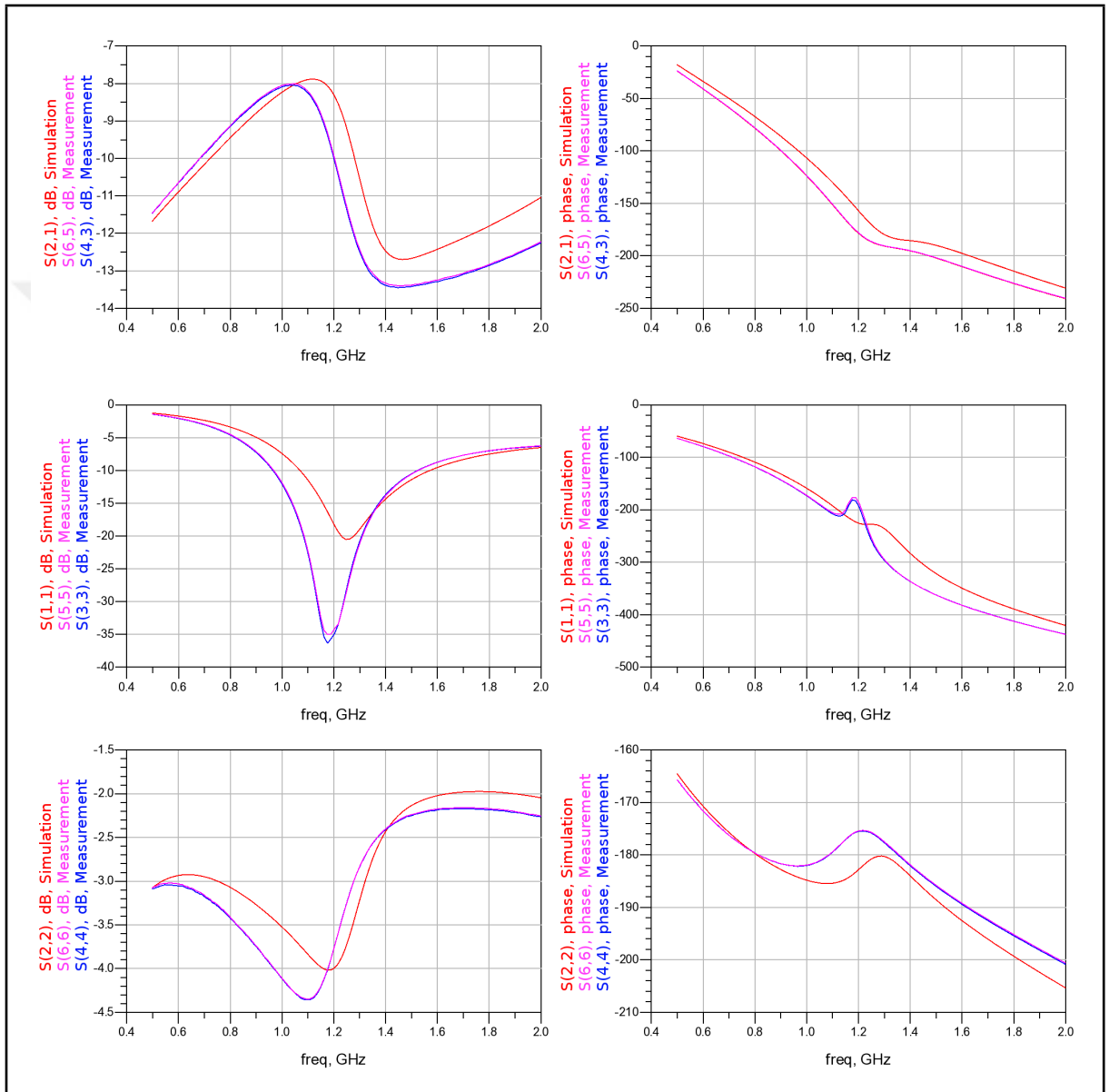
Figure 2.13: The measurement 1 comparison of original results from network analyzer and simulation

For measurement 2, idle terminal is left open. Related configuration and port numbers are given in Fig. 2.14. The original measurement results from network analyzer is in Fig. 2.15. To compare the measurement results, same configuration is simulated with Agilent S-paramaters simulation and results are plotted in Fig. 2.16. In Fig. 2.16, red lines represent simulation results and the others are measurement of two different samples. Measurement results of two samples show close correlation between samples except one graph. There is some differences between simulation and measurement of the two samples. As seen in Fig. 2.16, peaks also shift to lower frequency which is an indication of higher capacitor or inductor values.
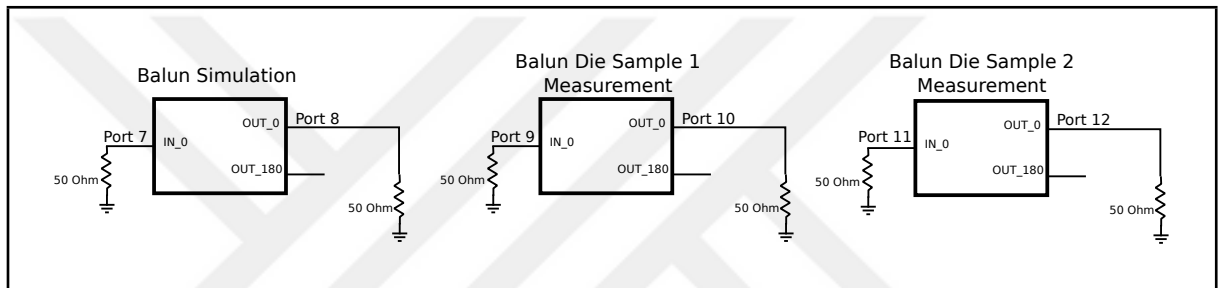
Figure 2.14: The measurement 2 configuration
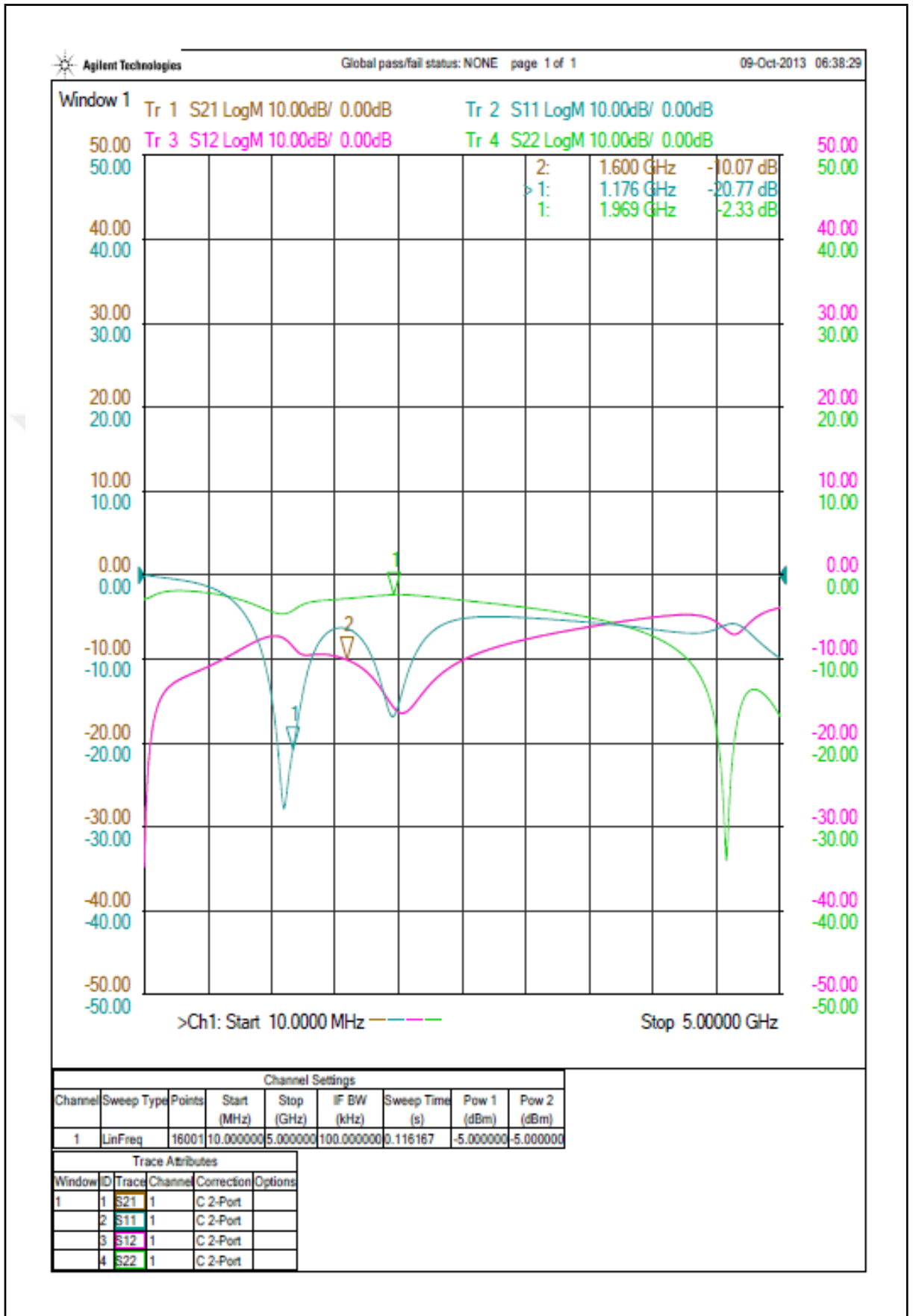
Figure 2.15: The measurement 2 original results from network analyzer
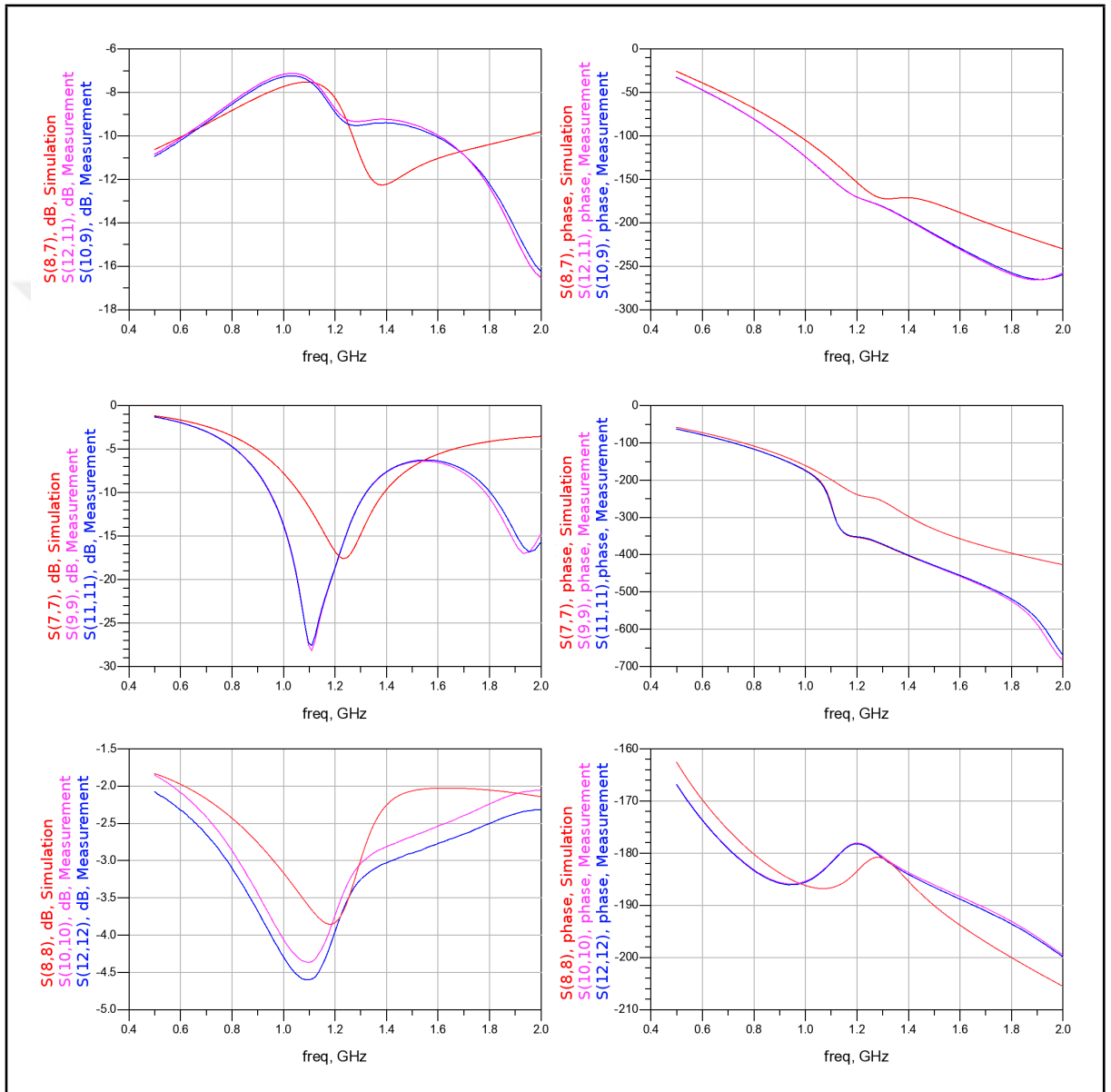
Figure 2.16: The measurement 2 comparison of original results from network analyzer and simulation

For measurement 3, idle terminal is left open. Related configuration and port numbers are given in Fig. 2.17. The original measurement results from network analyzer is in Fig. 2.18. To compare the measurement results, same configuration was simulated with Agilent S-paramaters simulation and results are plotted in Fig. 2.19. In Fig. 2.19, red lines represent simulation results and the others are measurement of two different samples. Since two ports are left open, there are only one-port measurement results. Measurement results of two samples show close correlation between samples. The major difference between measurement and simulation are the shifts at peak frequencies.
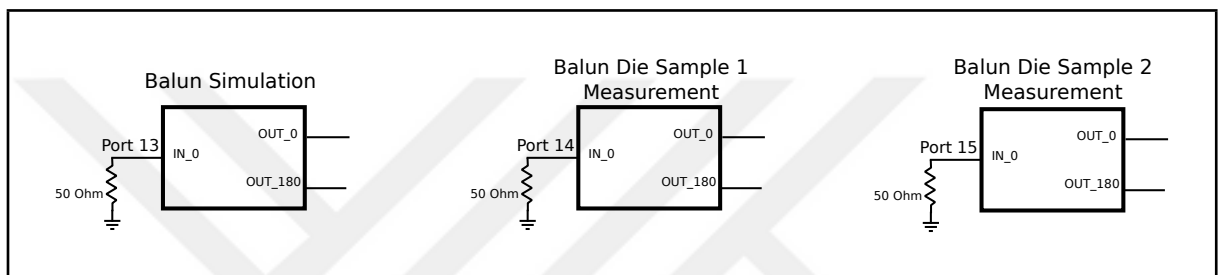
Figure 2.17: The measurement 3 configuration
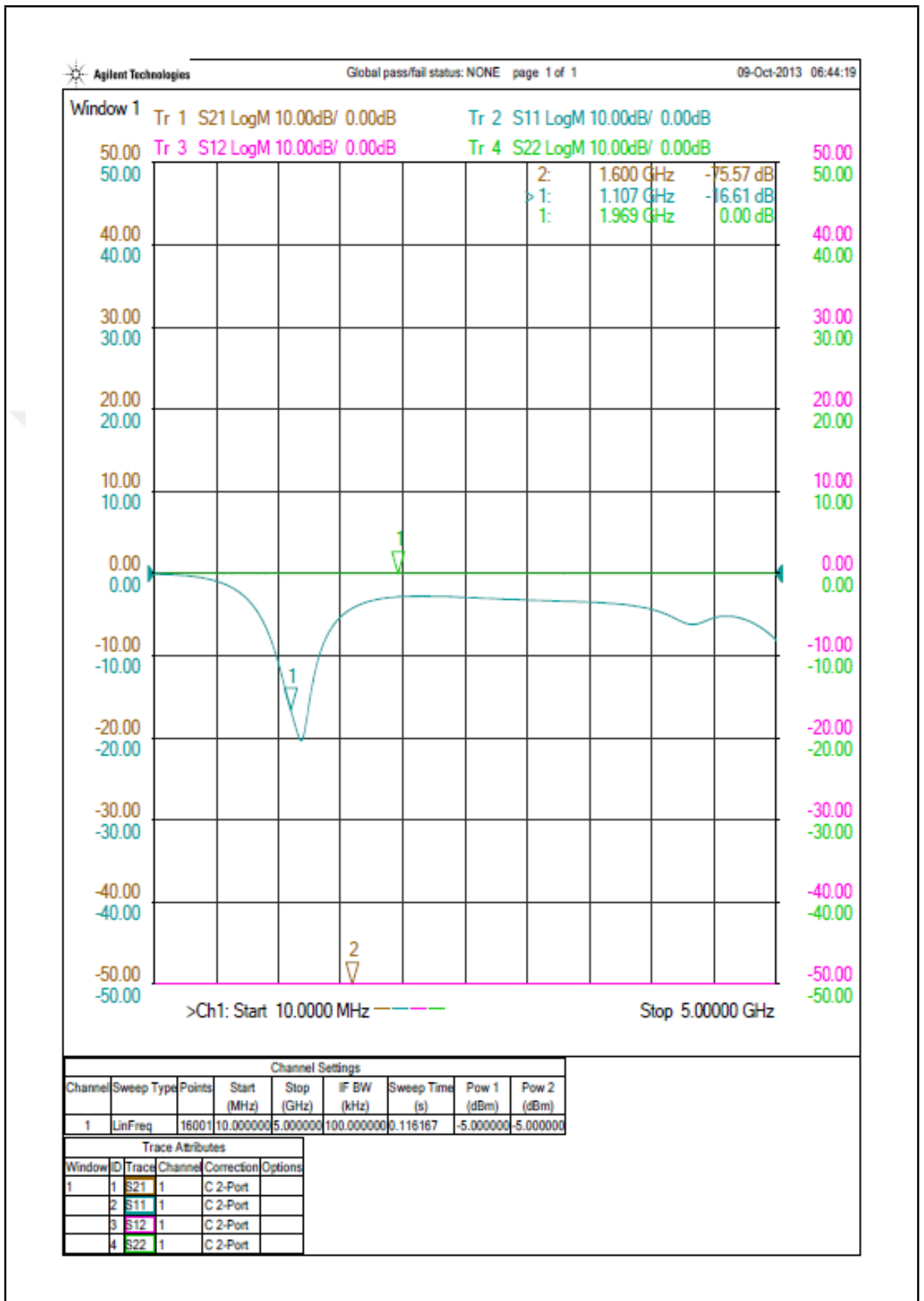
Figure 2.18: The measurement 3 original results from network analyzer
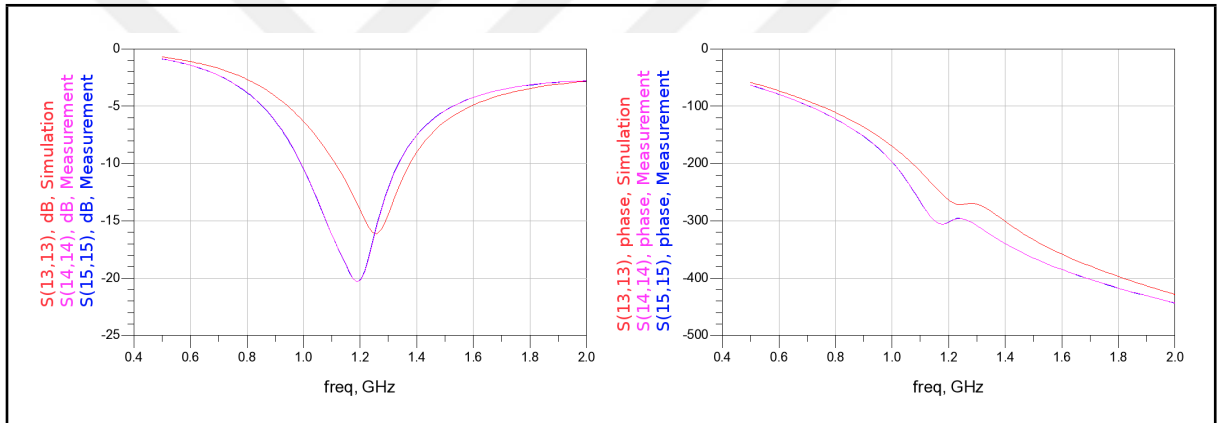
Figure 2.19: The measurement 3 comparison of original results from network analyzer and simulation

For measurement 4, idle terminal is terminated with 50 Ω. Related configuration and port numbers are given in Fig. 2.20. The original measurement results from network analyzer is in Fig. 2.21. To compare measurement results, same configuration is simulated with Agilent S-paramaters simulation and results are plotted in Fig. 2.22. In Fig. 2.22, red lines represent simulation results and the others are measurement of two different samples. Measurement results of two samples show close correlation between samples. There is a difference between peak values and frequencies between measurements and simulation.
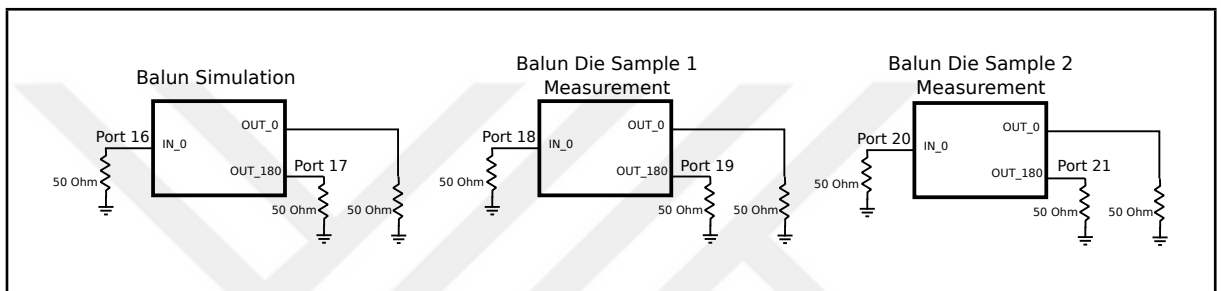
Figure 2.20: The measurement 4 configuration
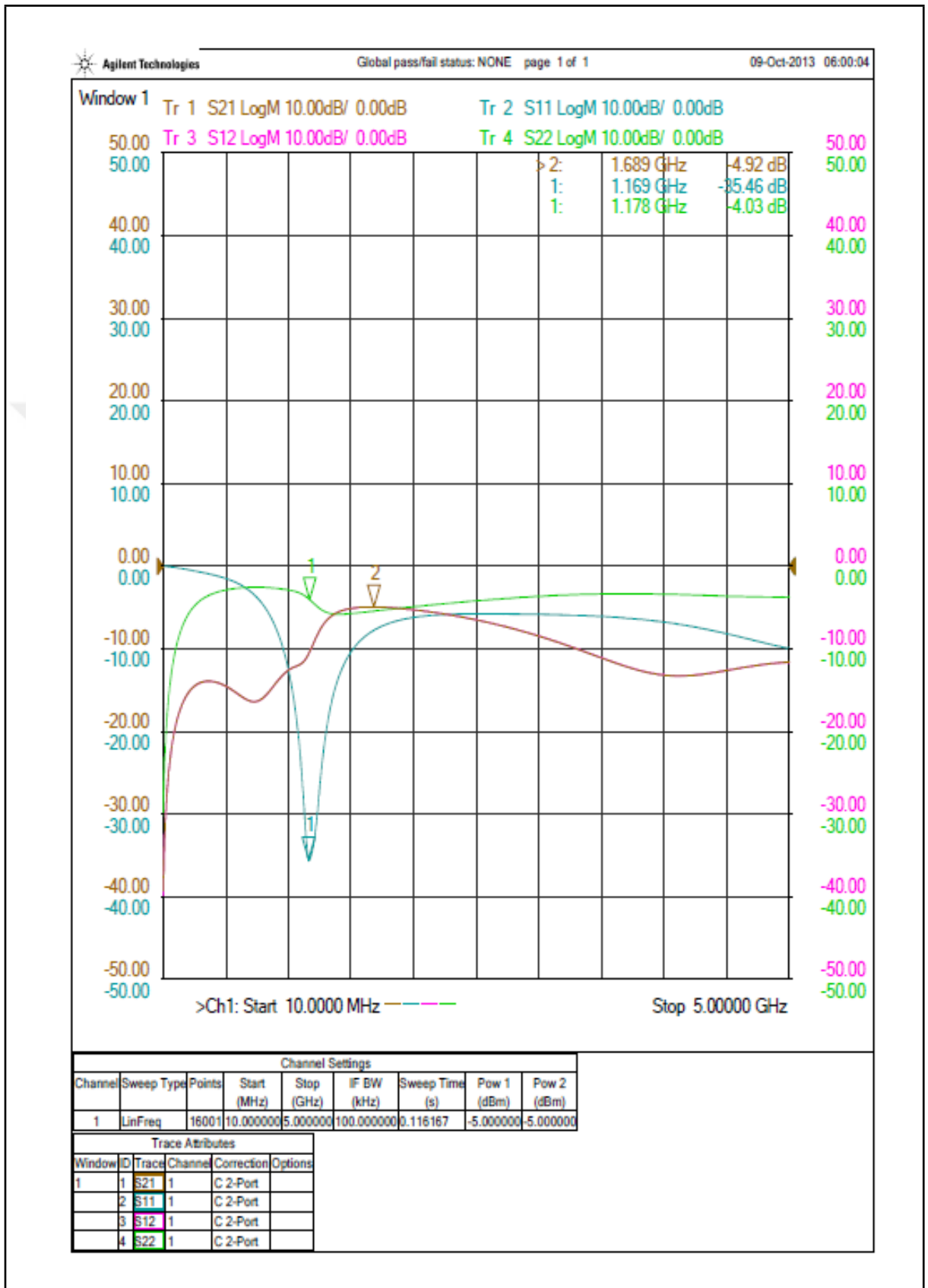
Figure 2.21: The measurement 4 original results from network analyzer
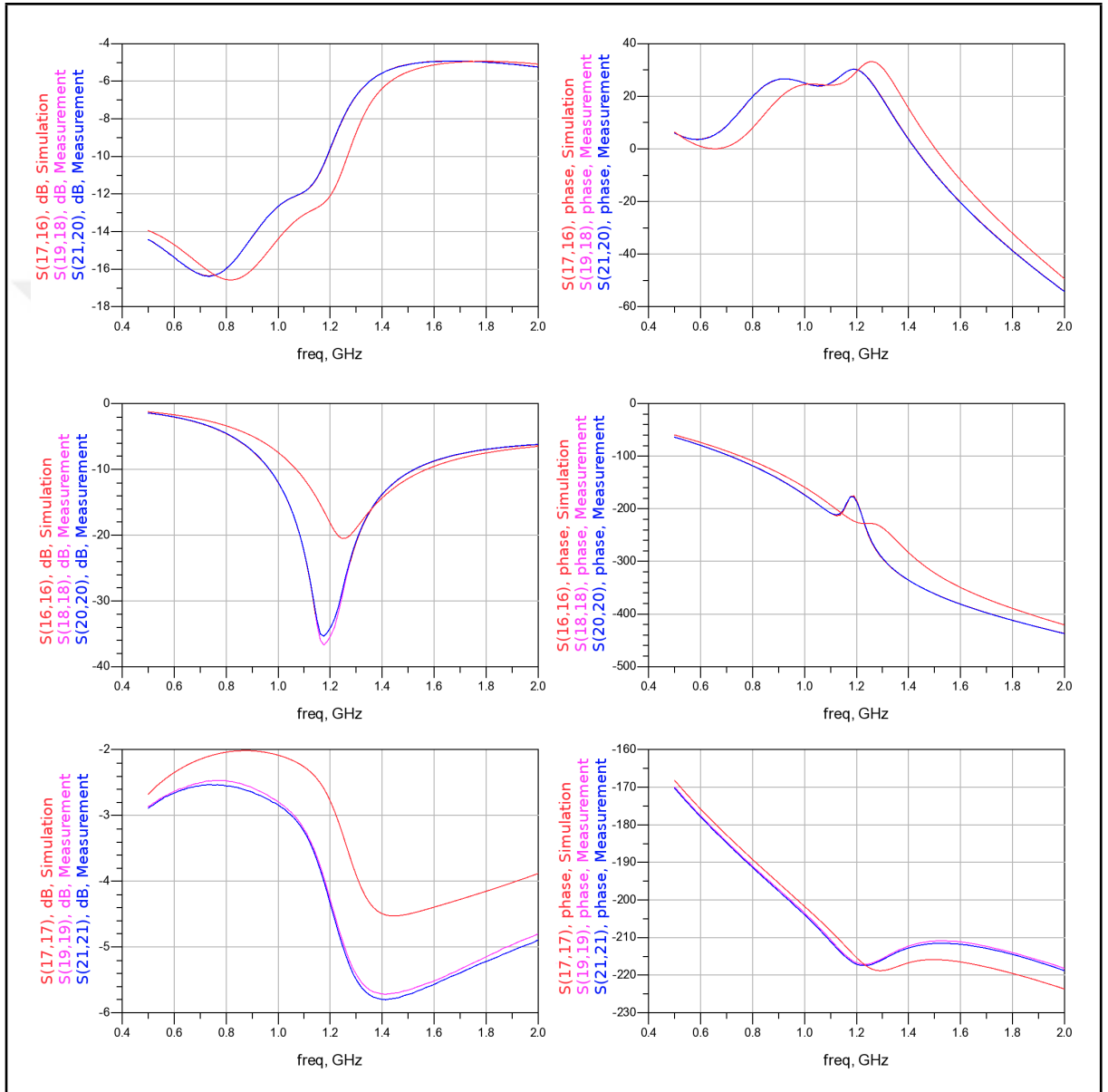
Figure 2.22: The measurement 4 comparison of original results from network analyzer and simulation

For measurement 5, idle terminal is terminated with 50 Ω. Related configuration and port numbers are given in Fig. 2.23. The original measurement results from network analyzer is in Fig. 2.24. To compare measurement results, same configuration is simulated with Agilent S-paramaters simulation and results are plotted in Fig. 2.25. In Fig. 2.25, red lines represent simulation results and the others are measurement of two different samples. Measurement results of two samples show close correlation between samples. There is difference between simulation and measurement of two samples in terms of peak values and frequency.
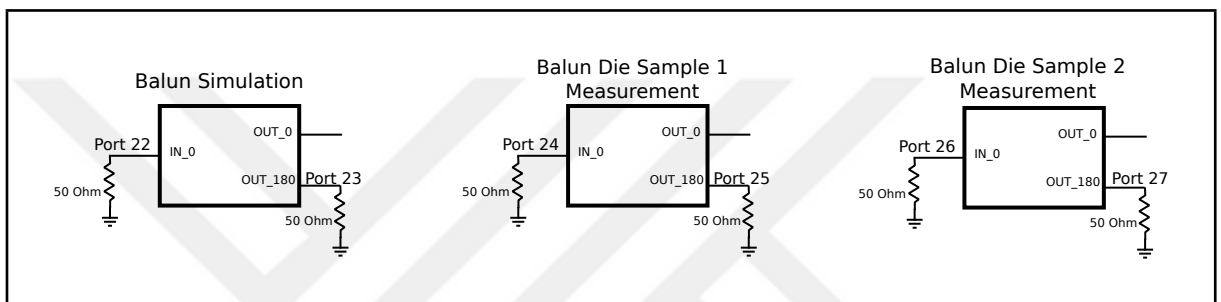
Figure 2.23: The measurement 5 configuration
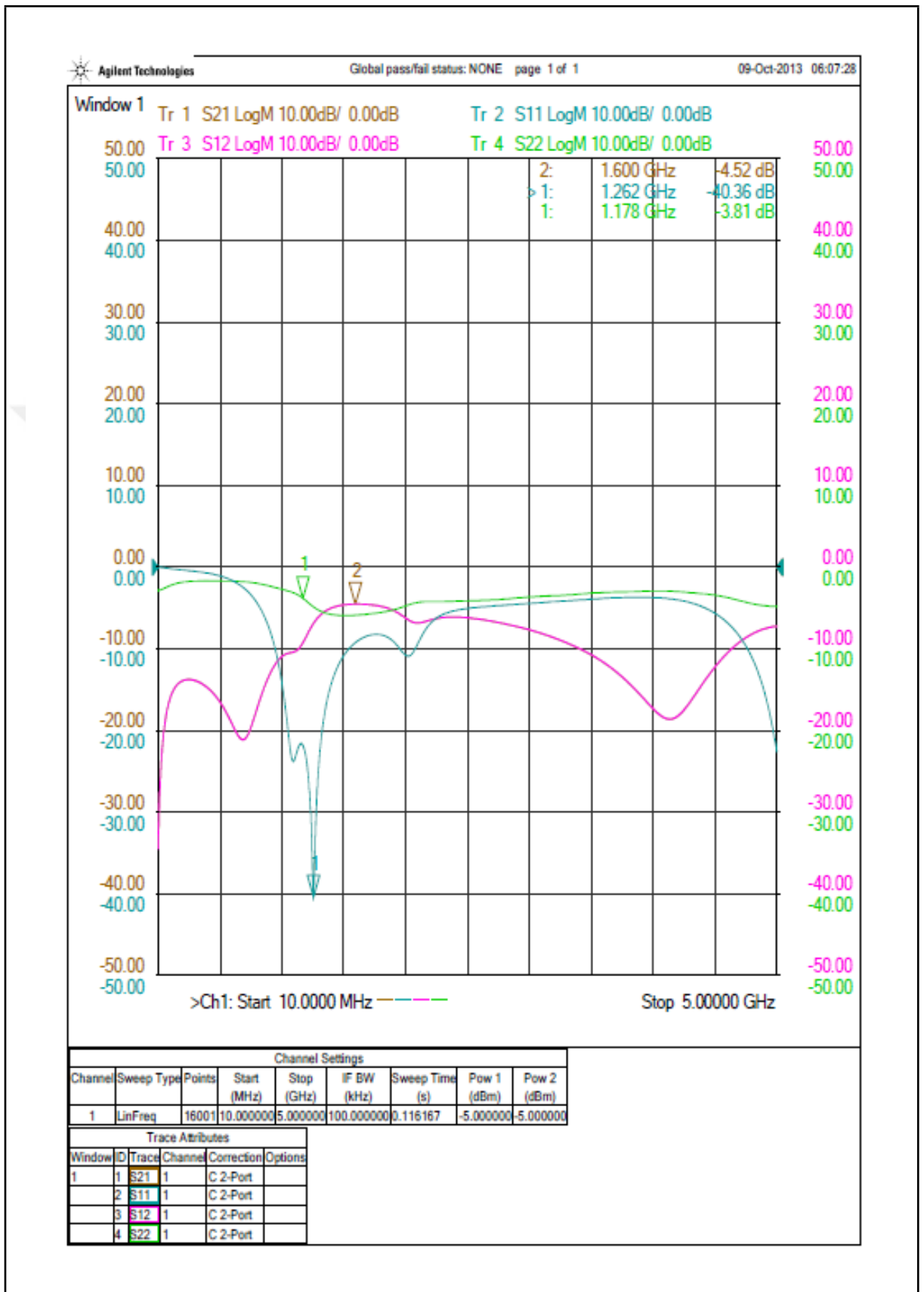
Figure 2.24: The measurement 5 original results from network analyzer
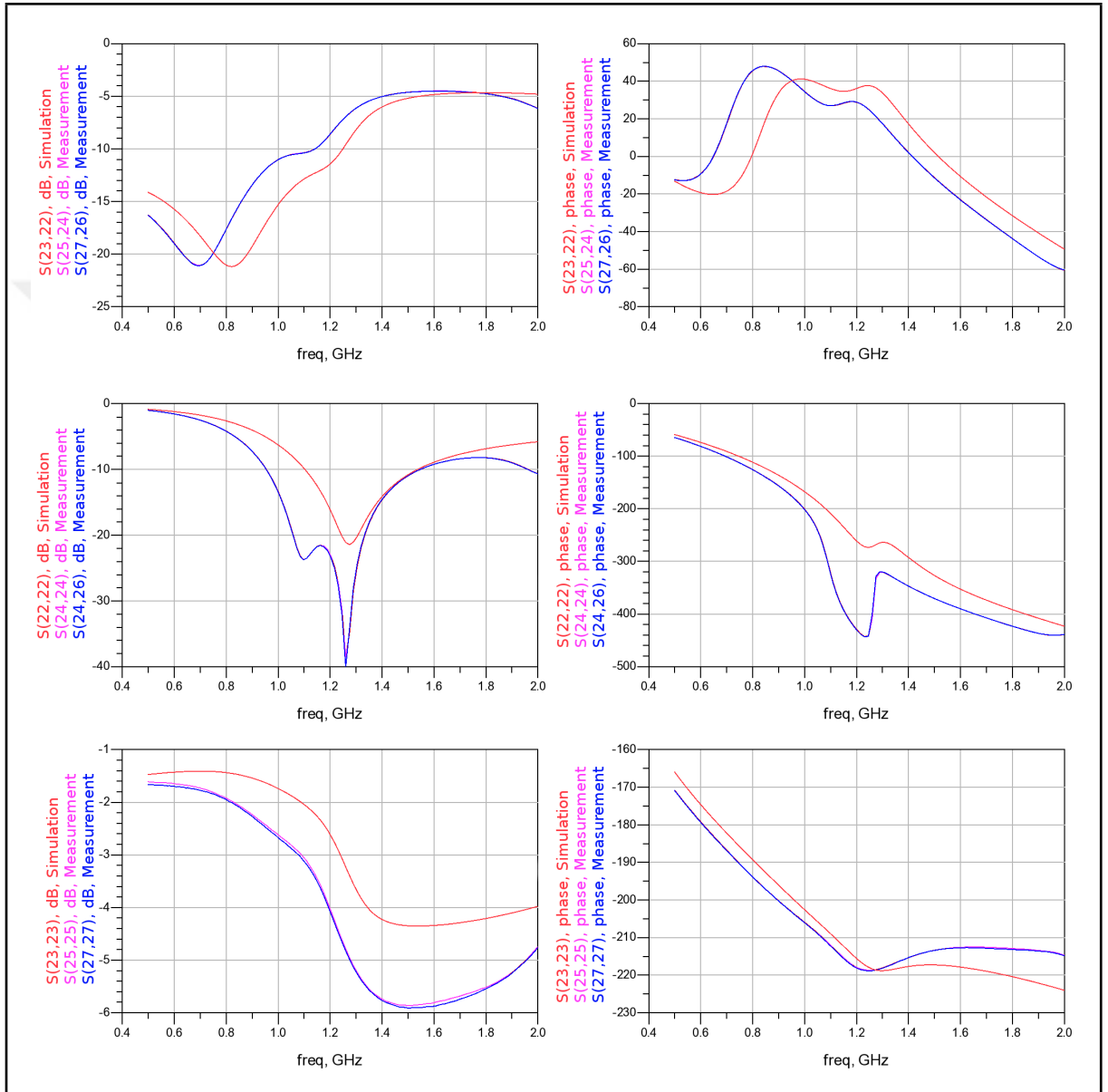
Figure 2.25: The measurement 5 comparison of original results from network analyzer and simulation

2.2.4. Results

In order to convert single ended signal to differential signal, passive balun was designed, realized and measured. There is a difference between in resonances(peak) values and frequencies. These may be caused by either higher components values than expected or parasitic components which were not modelled during simulations such as metal fill structures. All measurements were taken on two different samples, and majority of the measurements show close correlation for two different samples. Although measuring only two samples is not enough to characterize process variation, measurement results are promising. Thus measurement results given in section 2.2.3 show that designed balun measurement and simulation results are close enough to integrate it with the overall system at the next tape-out.

2.3. DIE 2 - M8X CORE

As mentioned before in order to reduce the complexity of system, the whole system was divided into three tape-out/dies. Die 2 consists of the blocks shown in Fig. 2.26.
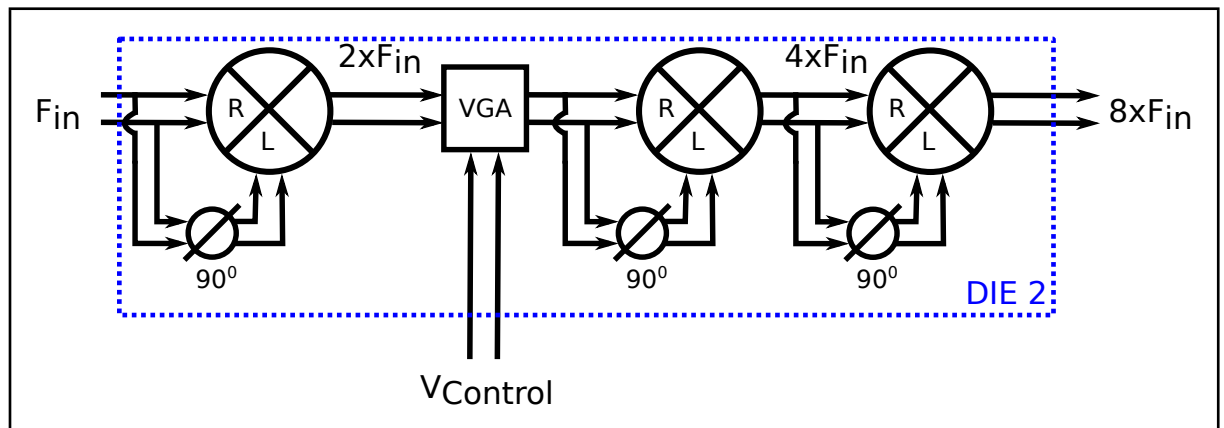
Figure 2.26: Die 2 - M8X core

2.3.1. Polyphase Filters

According to (1.4), a 90° phase shift is required for eliminating DC unbalance at the output of the mixer. This phase shift is realized using the poly phase filter shown in

Fig. 2.27 [30–32]. Resistor and capacitor values optimized as to minimize the phase noise and unbalance. A polyphase filter was placed before each mixer and therefore a total of three such filters exists inside system. Final component values are given in Table 2.2.
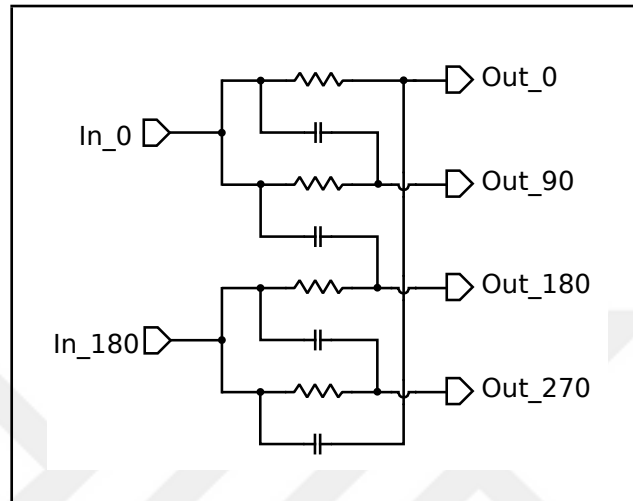
Figure 2.27: Poly Phase Filter

Table 2.2: Poly phase filter component values

Poly Phase Filter 1	
R	60 Ω
C	2.1 pF
Poly Phase Filter 2	
R	160 Ω
C	0.4 pF
Poly Phase Filter 3	
R	80 Ω
C	0.43 pF

Poly phase filters are simulated using Agilent Harmonic Balance simulation. One of the poly phase filters' output transient responses is plotted in Fig. 2.28. Poly phase filters are simulated for device mismatch and process variations using Monte-Carlo

analysis. Resistor and capacitor values are spread around $\pm 10\%$ for process variations, and foundry provided values are used for device mismatch. Phase unbalance due to variations at the outputs are negligible for overall system performance.
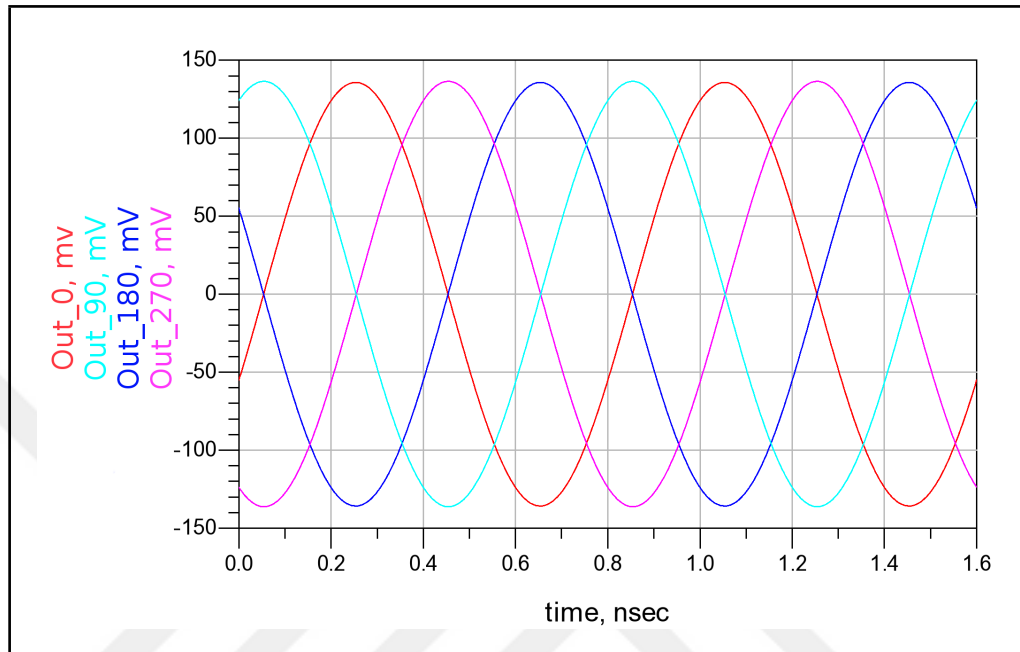
Figure 2.28: Poly phase filter transient simulation result

2.3.2. Mixer - Frequency Doubler

As mentioned in Section 1.3.3, three cascaded frequency doublers were used for multiplier core. A well-known mixer topology called Gilbert multiplier was preferred as a frequency multiplier. A Gilbert multiplier has a low conversion-loss and a good IF/LO isolation. Due to its double balanced structure, it suppresses even numbered harmonics [33, 34]. Its circuit schematic is given in Fig. 2.29. The bias current and the geometry of transistors are chosen so as to maximize f_T and minimize noise contribution of transistors. To isolate DC bias conditions of the two connected blocks, capacitive coupling is used between blocks as shown in Fig. 2.30. C_1 and C_2 are the coupling capacitors. R_1 and R_2 constitute a voltage divider for setting the base bias voltages of the transistors. To reduce the kick back of RF signals onto the biasing voltage, we deploy $R_3 \approx 2k\Omega$, $R_4 \approx 2k\Omega$ and $C_3 \approx 4pF$. To reduce oscillation tendency and the quality factor of C_3 capacitor, a small resistor $R_3(\approx 100\Omega)$ is added. These

biasing voltages can be set and observed off chip. Bias current(IBias) can be set by trimming a potentiometer on the PCB. By that way, gain and biasing voltages of each block can be set individually for debugging purposes.
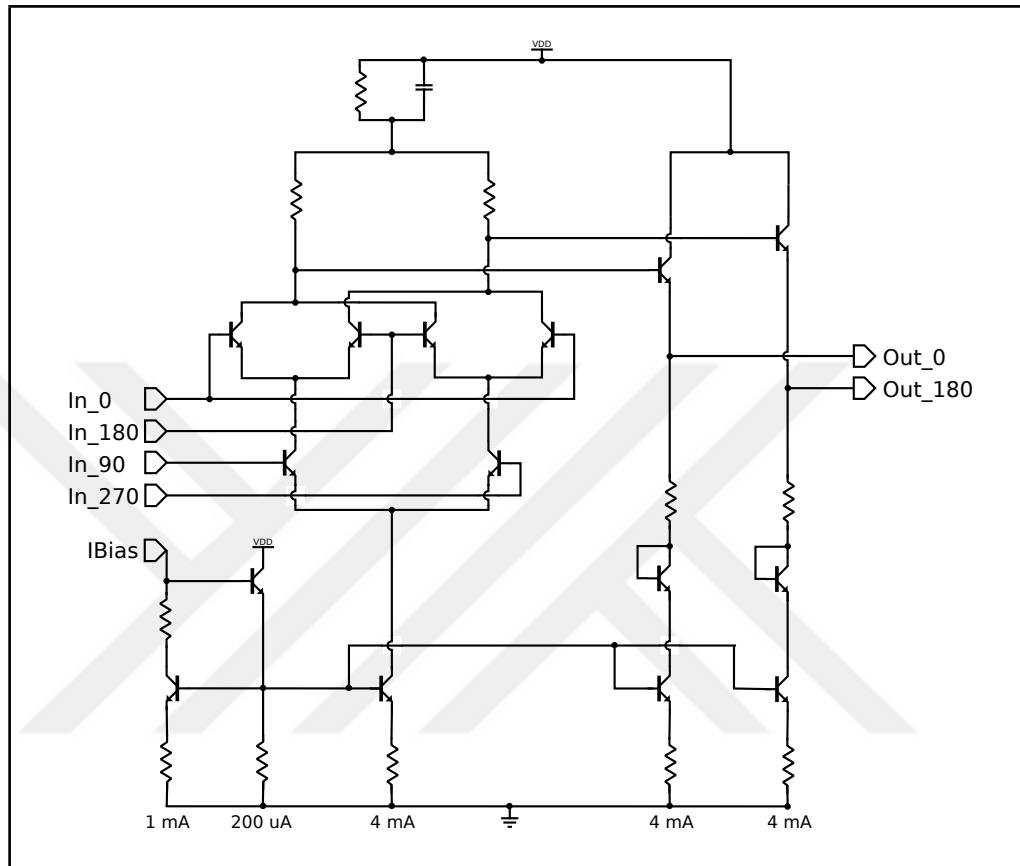
Figure 2.29: Gilbert multiplier
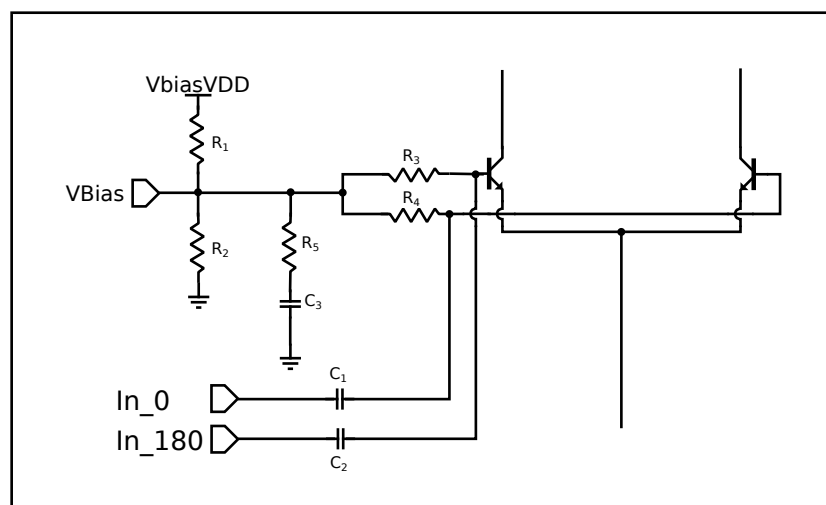
Figure 2.30: Gilbert multiplier capacitive coupling and bias network

A frequency doubler was simulated with Agilent Harmonic Balance simulation. 1.25 GHz differential sinusoidal input is applied to polyphase filter inputs and frequency doubler is fed by its output. The transient response of frequency doubler is shown in Fig. 2.31. In figure, red and purple line represent outputs of the poly phase filter with 90° phase shift, and the blue line represents the mixer outputs. As seen in figure, input signal frequency is doubled at the output of the mixer. In Fig. 2.32, the frequency
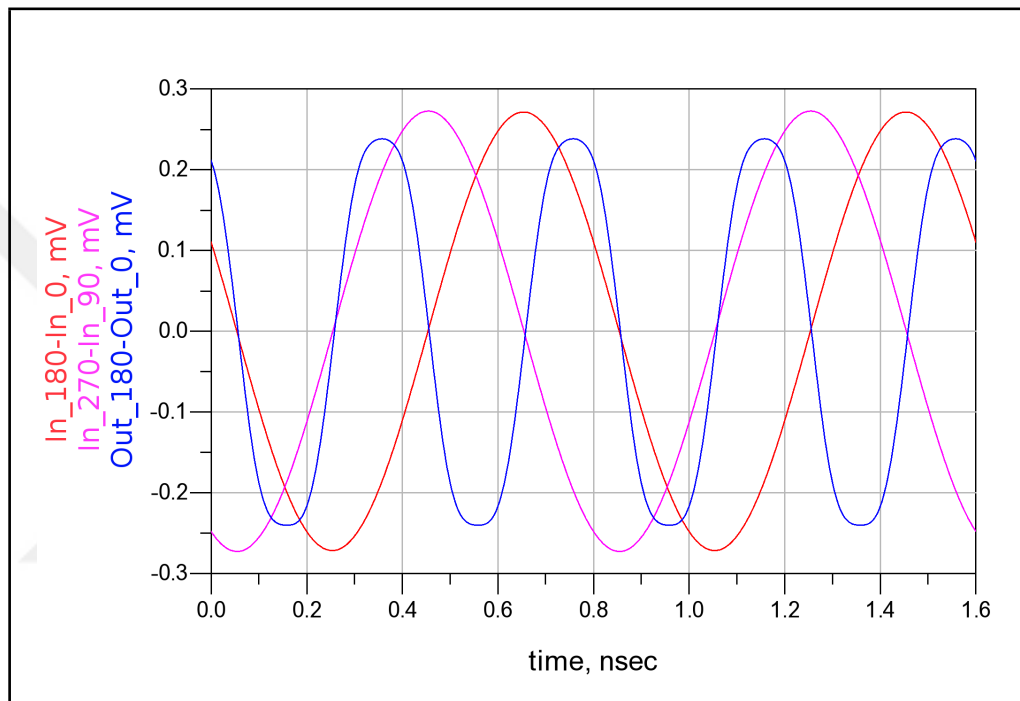
Figure 2.31: Transient response of freqeuncy doubler

spectrum of poly phase filter output are plotted. In figure, marker m106 and m113 show the output power of poly phase filter. There is a negligible amplitude unbalance at the outputs. Fig. 2.33 shows the output frequency spectrum of frequency doubler. In this figure, marker m121 shows the harmonic level at $7.5\,GHz$. It is higher than systems specifications and it will be suppressed later by a low-pass filter.
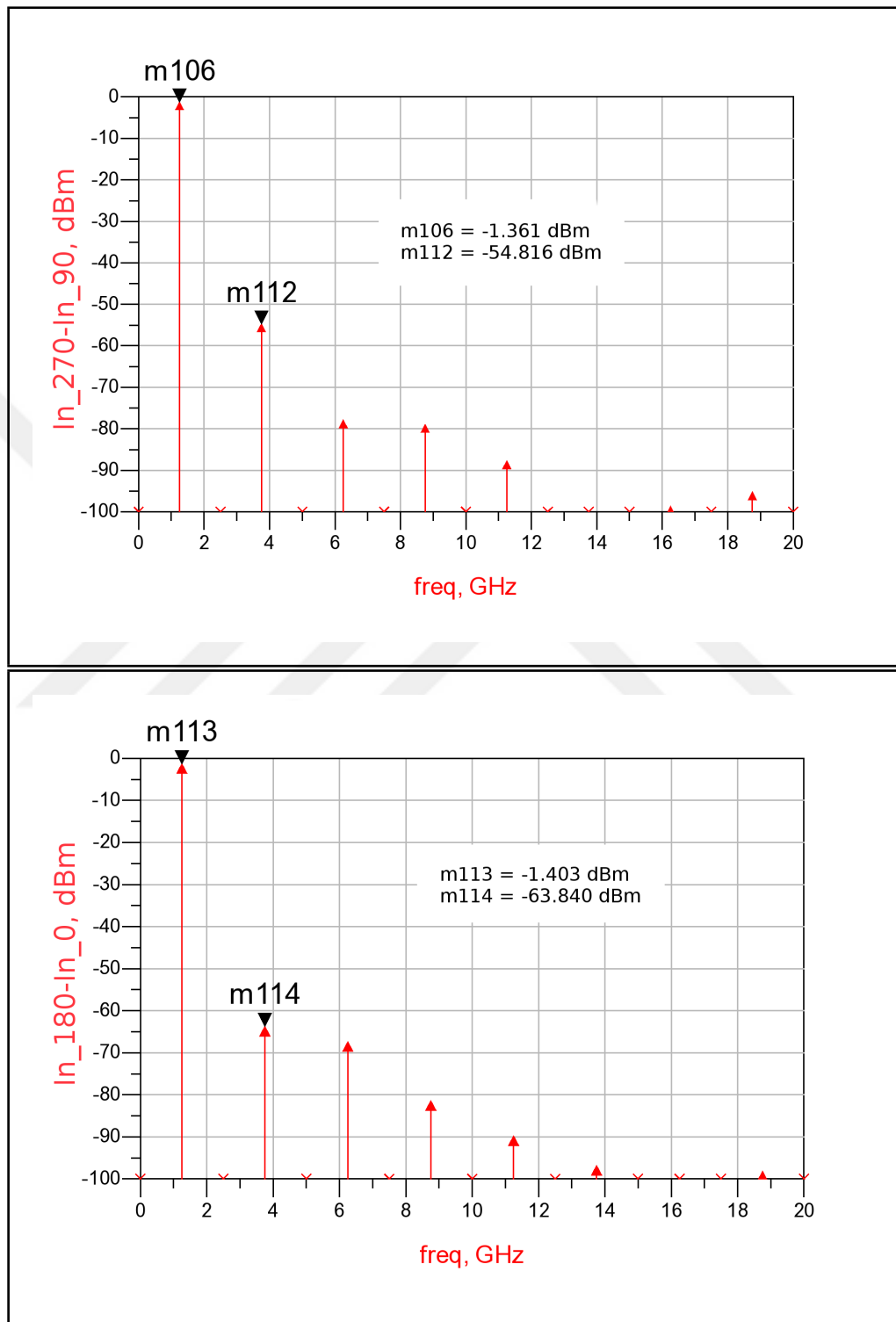
Figure 2.32: Inputs frequency spectrum of frequency doubler
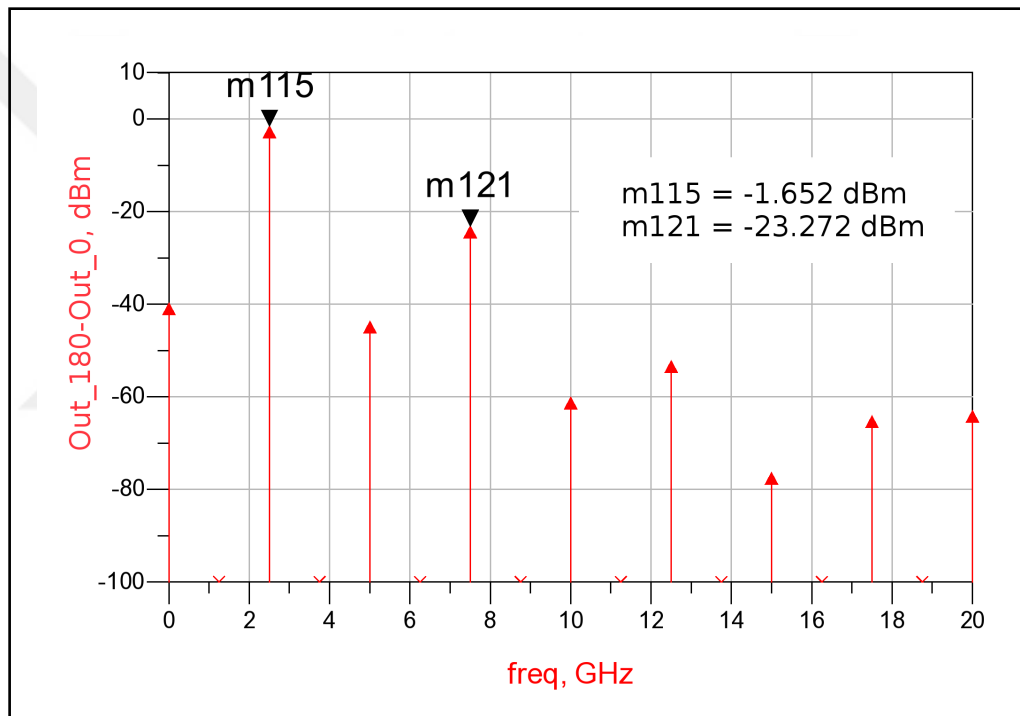
Figure 2.33: Output frequency spectrum of frequency doubler

2.3.3. VGA - Variable Gain Amplifier

In order to maintain a constant 0 dBm output power regardless of the input power level, a variable gain amplifier is designed. A Gilbert multiplier VGA topology is chosen for signal flow compatibility. A schematic drawing of the VGA is given in Fig. 2.34 [35]. Same DC biasing network and coupling capacitors as frequency doubler were used for the VGA. In this prototype, VGA control voltages are applied from outside the chip.
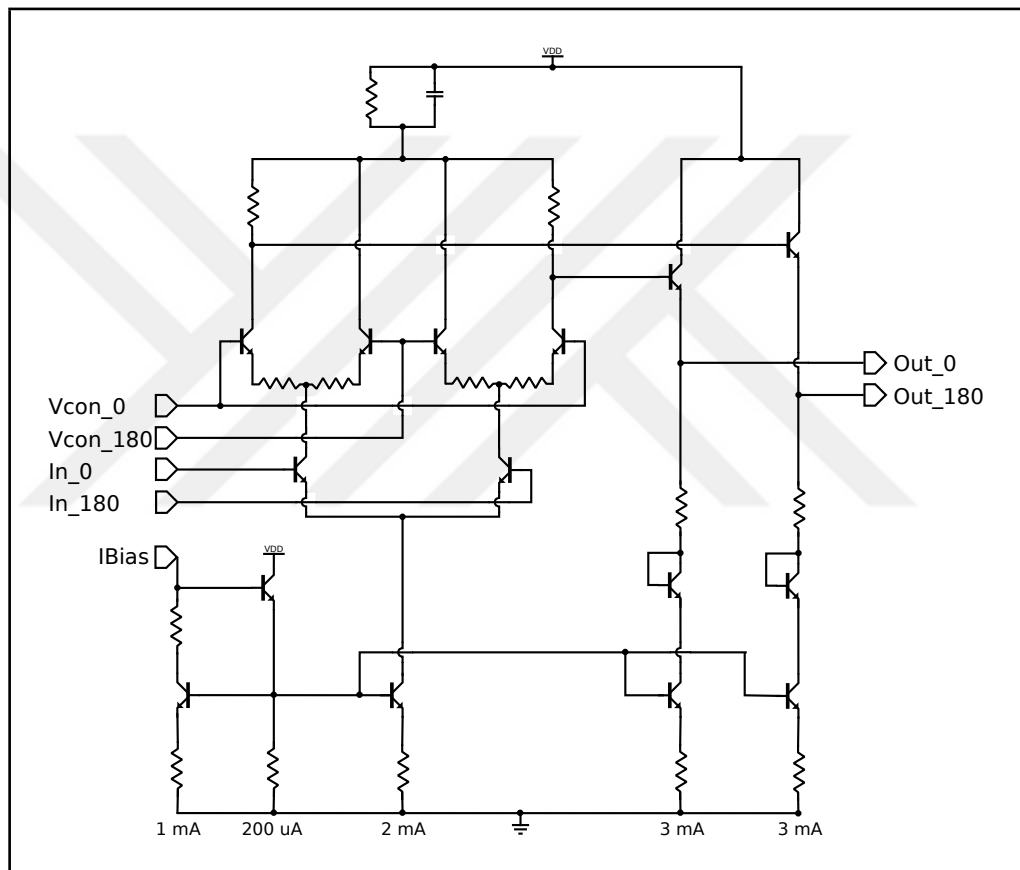
Figure 2.34: Variable gain amplifier

A bipolar transistor (BJT) differential pair is linear only for small portion of its input voltage range. For any input overdrive voltage(V_{id}) greater than about $3V_T$, output voltage becomes independent from input voltages. This behaviour can be easily formulated by referring to the following DC transfer characteristic of the differential pair [4].

$$V_{od} = V_{o1} - V_{o2} = \alpha_F I_{TAIL} R_C \tanh\left(\frac{-V_{id}}{2V_T}\right) \tag{2.2}$$

where the electrical variables are marked in Fig. 2.35, V_{id} is $V_{i1} - V_{i2}$, V_T is the thermal voltage and α_F is the common-base current gain factor. V_T is approximately 26 mV at 300 ^{0}K. In order to increase the range of linear portion, emitter degeneration resistors
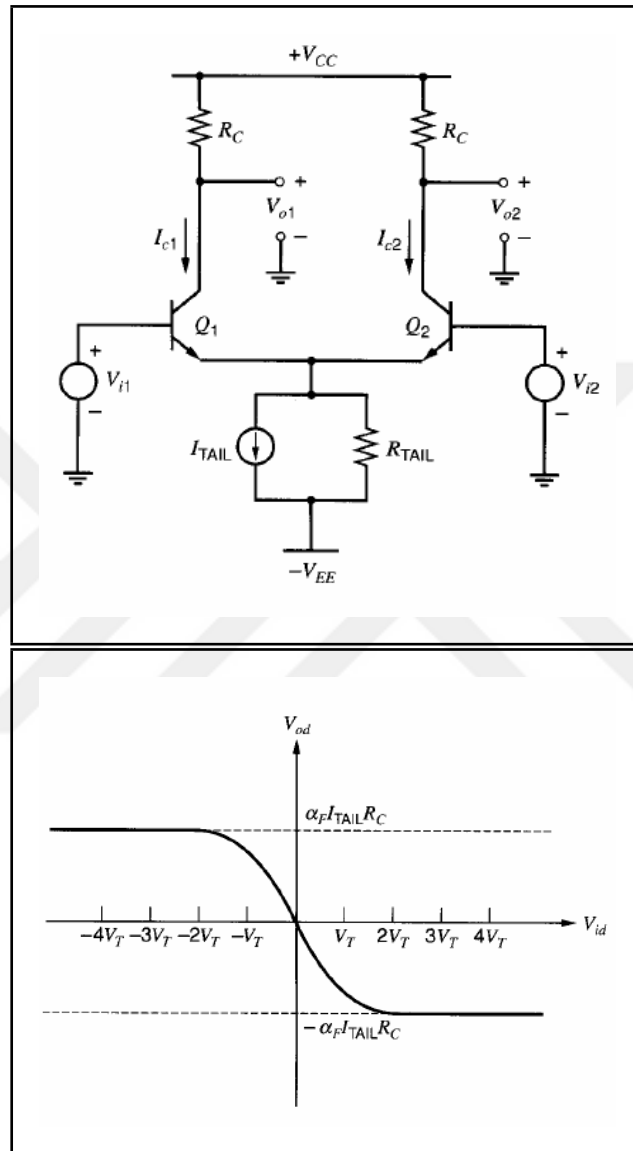
Figure 2.35: Bipolar transistor differential pair and its output voltage [4]

should be added. Resulting circuit diagram and output waveform are given in Fig. 2.36. As seen from the waveform, linear region is directly proportional to the resistance of the resistor. Emitter degeneration resistors are also shown in Fig. 2.34 in series with BJT emitters. VGA was simulated with Agilent Harmonic Balance simulation. Shown in Fig. 2.37 is the variation of output power with input power various values of the control voltage $Vcon = Vcon_{180} - Vcon_0$. The reader is referred to Fig. 2.34 for the

49
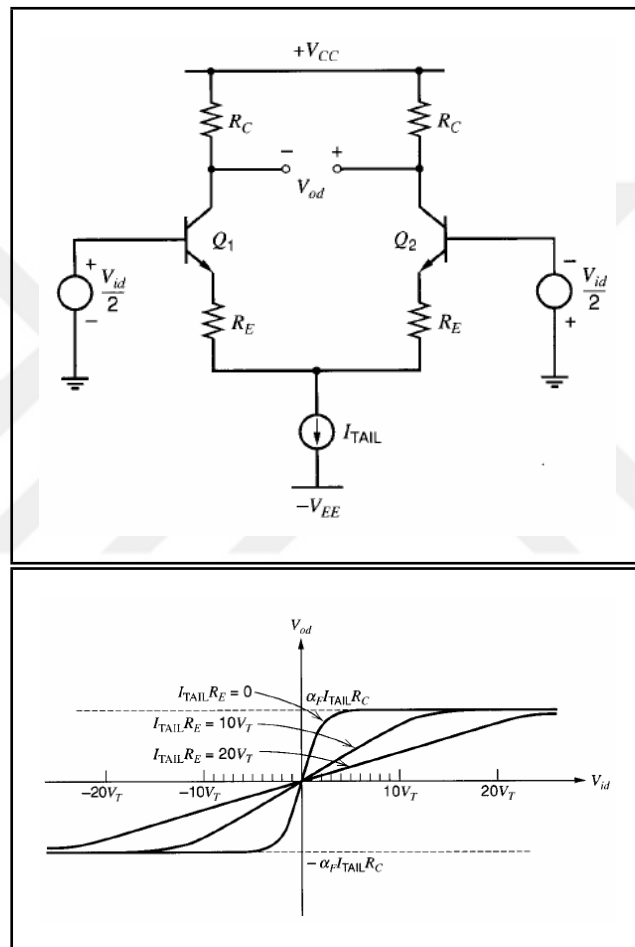
Figure 2.36: Bipolar transistor differential pair with emitter degeneration and its output voltage [4]

definition of $Vcon_{180}$ and $Vcon_0$. This figure shows that for any VGA input power between -15 dBm and 0 dBm, there is such a VGA control voltage that can set the output power around 0 dBm. In Fig. 2.38, VGA output power is plotted as a function
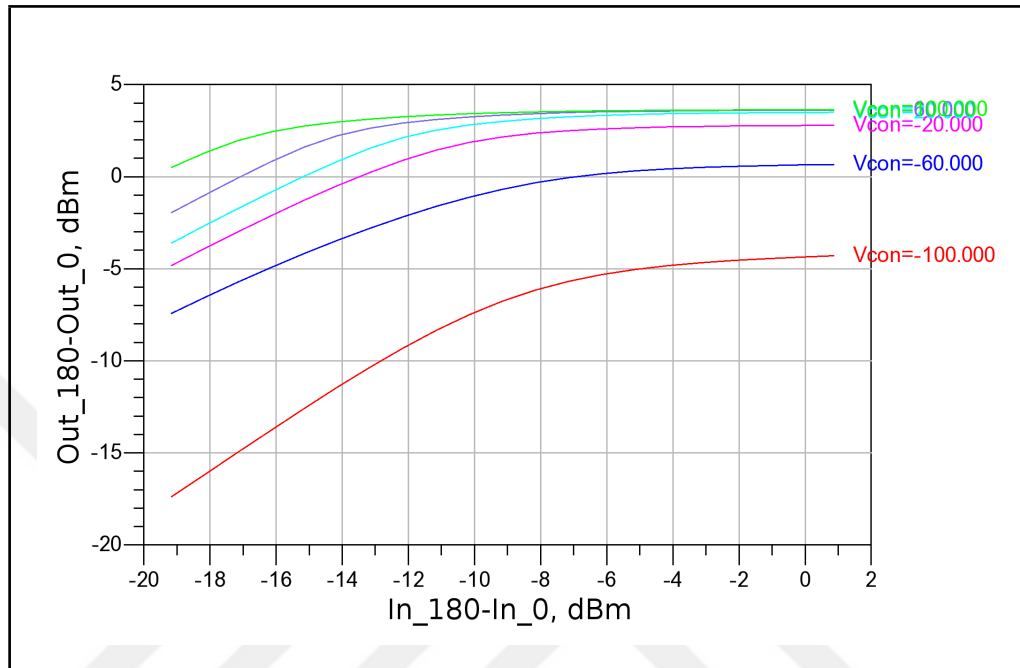
Figure 2.37: VGA output power for different control voltages and input powers

of VGA control voltage for a fixed input power -15 dBm. With the addition of emitter degeneration resistors, linear portion of VGA control voltage range is increased to 150 mV. Transient response of VGA for different VGA control voltage is plotted in Fig. 2.39 for an input power -15 dBm. The effect of VGA control voltage on the VGA output amplitude is clearly seen in this figure.
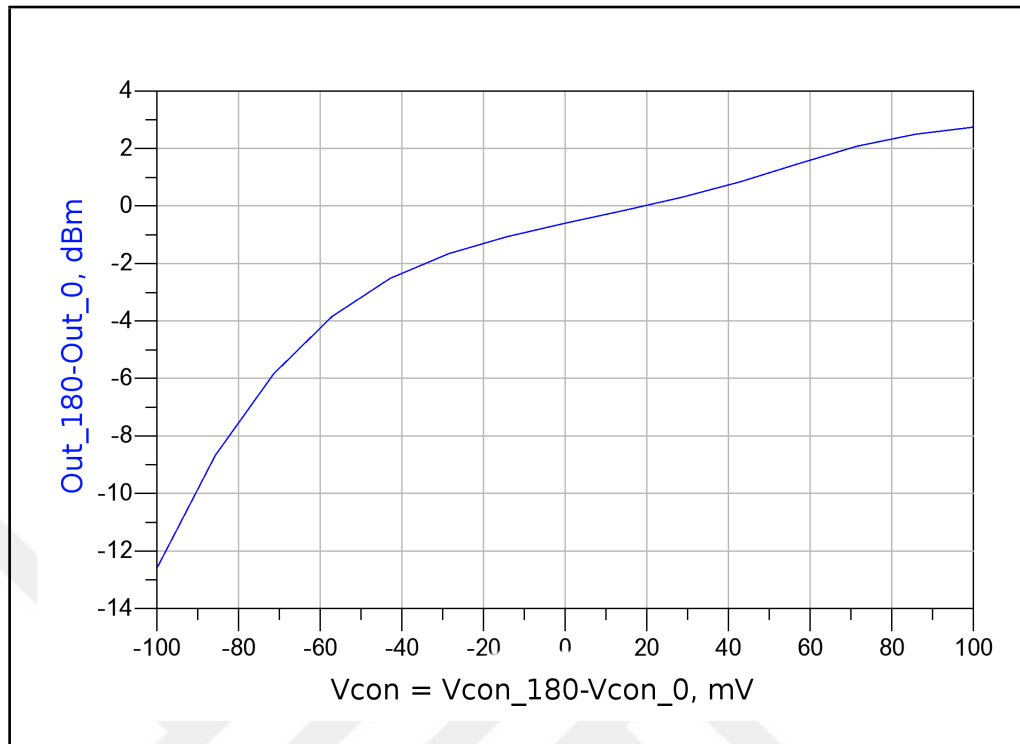
Figure 2.38: Change of VGA output power with VGA control voltage for $-15\,dBm$ VGA input power
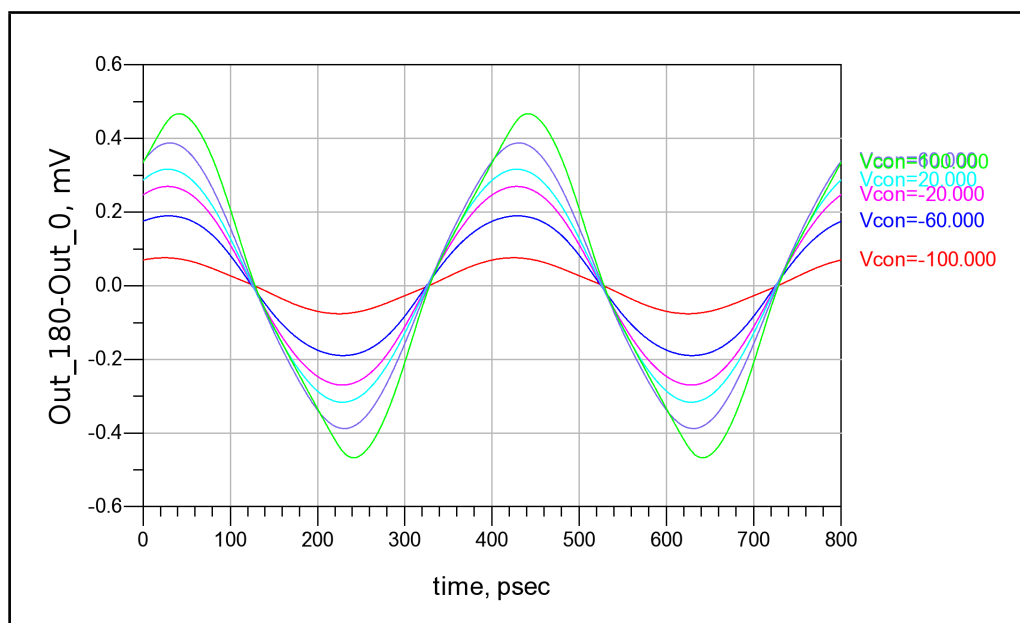
Figure 2.39: Transient response of VGA for different control voltages

2.3.4. Die 2 - M8X Core System-Level Pre-layout Simulations

System level block diagram of M8X Core is shown in Fig. 2.40. After the design and simulation of sub-blocks, system level simulation was performed with Agilent Harmonic Balance simulator to see whether the combination of sub-blocks meets the system requirements. The gain of sub-blocks is tuned to meet specifications. At this section, signals from first poly phase to third frequency doubler is plotted. All waveforms plotted here are for the same input power (-1 dBm), VGA control voltage $Vcon_{180} = Vcon_0$ and biasing currents, IBias which is explicitly marked in Fig. 2.29 and Fig. 2.34, as 1 mA. Naming suffix in figures is given in Table 2.3.

Table 2.3: Naming suffix in figures

Name	Definition
M1	Input of M8X Core
PPF_M1	Output of first poly phase filter
M2	Output of first frequency doubler
VGA_M2	Output of VGA
PPF_M2	Output of second poly phase filter
M4	Output of second frequency doubler
PPF_M4	Output of third poly phase filter
M8	Output of third frequency doubler and output of M8X Core
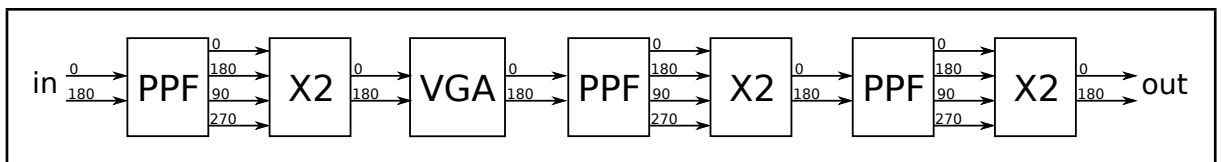
Figure 2.40: Block diagram of Die 2

In Fig. 2.41.a transient representation is plotted and in Fig. 2.41.b frequency spectrum of input signal is plotted. In this figure, input power is -1 dBm which is also input power of the system at simulation results given in this section and harmonic level is as low as -60 dB. From this point forward, the changes in the signal power and the rise

at the harmonic level will be observed. First polyphase filter generates two 90° out of phase signals. Related waveforms are in Fig. 2.41.c and Fig. 2.41.d. 90° phase shifted signal can be clearly seen in Fig. 2.41.c. In Fig. 2.41.d, amplitude imbalance of two differential 90° out of phase signals is about 0.150 dB and the harmonic contribution of the polyphase filter is negligible. First frequency doubler outputs can be seen in
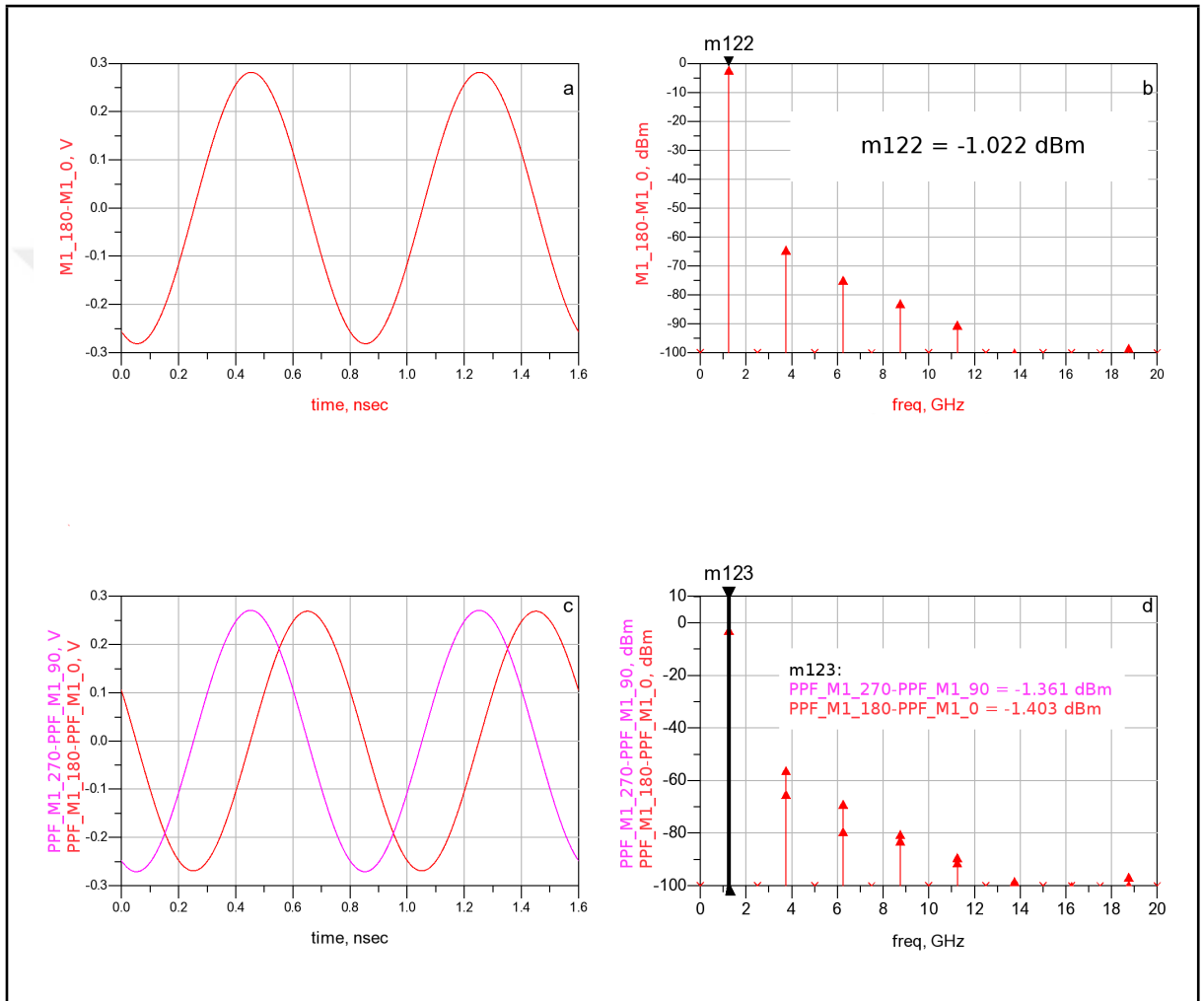
Figure 2.41: a. Transient input signal b. Frequency spectrum of input signal c. Transient output signal of 1st PPF d. Frequency spectrum of 1st PPF output

Fig. 2.42.a-b. Transient outputs are not that informative since they do not give any solid indication of the change in harmonic contents clearly. In Fig. 2.42.b, the marker m126 represents the output power of first frequency doubler as -1.652 dBm and its insertion loss is about 0.25 dB. The increase in harmonic contents is more dramatic at the output of this block. Since input power of the frequency doubler is relatively large signal($>> 3V_T$), this behaviour can also be explained by (2.2). From markers m126

and m127, the highest harmonic is about 22 dB below main signal. Such a harmonic level is out of target specification and it should be filtered out by a bandpass filter in future designs. In Fig. 2.42.c-d consequent VGA outputs are plotted. Insertion loss of VGA is almost 0 dBm and harmonic level is about 15 dBm. Although input power of first frequency doubler and VGA is about the same, there is a significant visual difference between figures 2.42.a and 2.42.c. Thus harmonic contribution of VGA at higher frequencies is worse than frequency doubler due to topological difference. Second polyphase filter outputs are in Fig. 2.43. Since transfer function for outputs
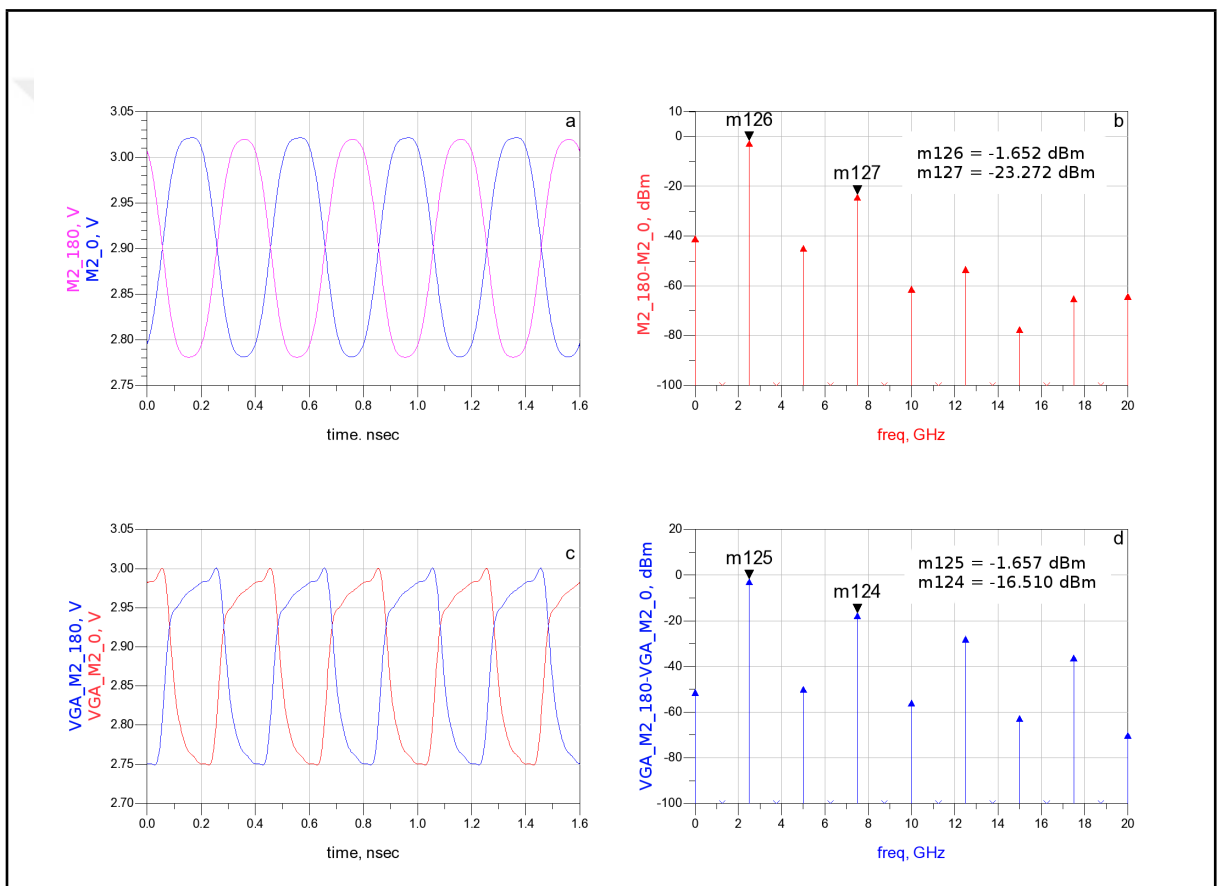
Figure 2.42: a. Transient output signal of 1st frequency doubler b. Frequency spectrum of 1st frequency doubler output c. Transient output signal of VGA d. Frequency spectrum of VGA output

are not identical, there is a difference at the harmonic content of the outputs. One of the outputs transfer function can be thought as a low pass response and other one as a high pass response [32]. Low pass branch suppresses the high frequency components at the input signal. Also poly phase filters shapes the phase of one of input signal with -45°

and other one with 45°. This causes different phases in harmonic contents at individual outputs and different transient response as a result of summing harmonics at different phases. Consequent frequency doubler outputs are in Fig. 2.44. Insertion loss of the
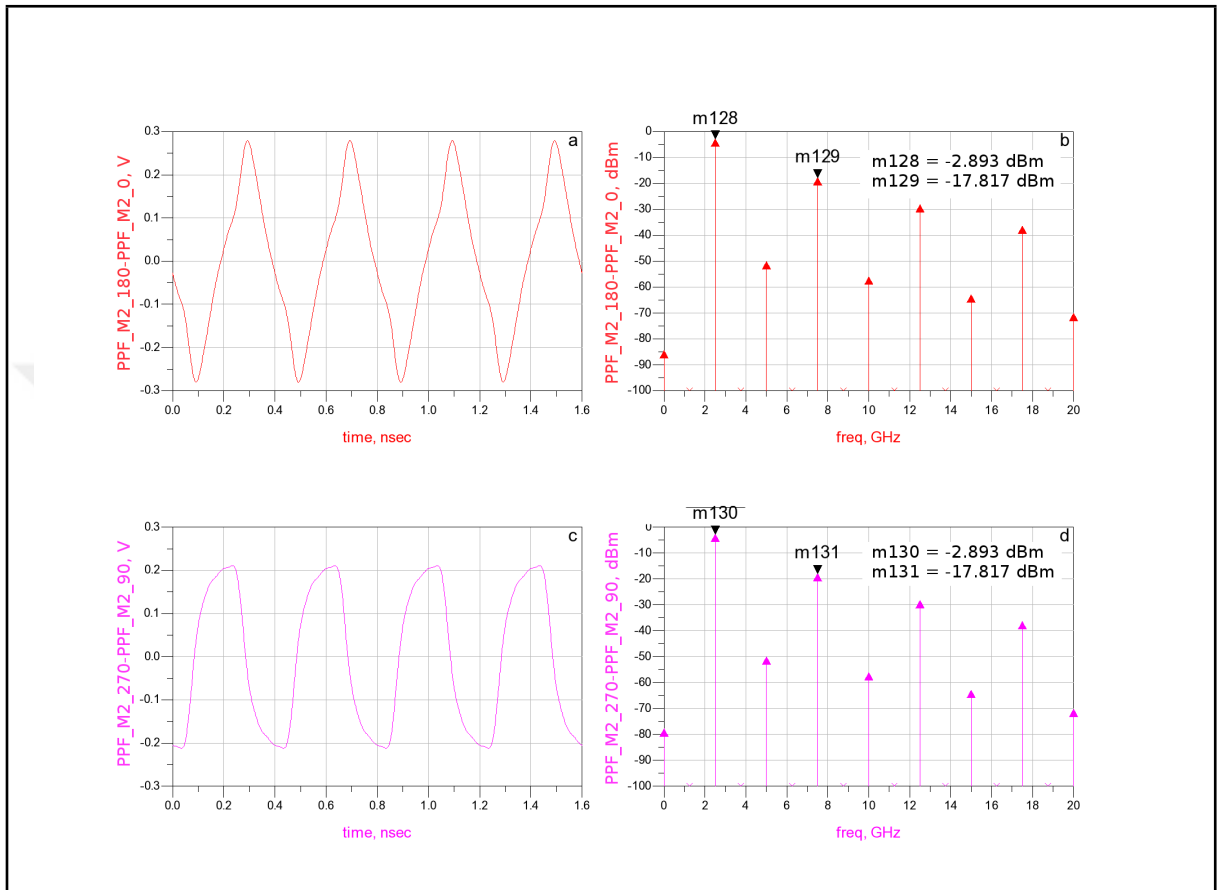
Figure 2.43: a.First transient output signal of 2nd PPF b. Frequency spectrum of 2nd PPF first output c. Second transient output signal of 2nd PPF d. Frequency spectrum of 2nd PPF second output

second frequency doubler is about 2 dB and harmonic level is about 16 dB. There is a significant rise at the higher frequency harmonics due to mixing effect of previous stages. Outputs the third poly phase filter are shown in Fig. 2.45. Insertion loss is about 1 dB and harmonic contribution is negligible. In Fig. 2.46, third frequency doubler and the output of M8X Core is plotted. Since this frequency doubler works relatively at high frequencies compared to previous doublers, its insertion loss is higher and is about 4 dB. The output power is about -9.5 dBm which is out of target specification. This also implies the need for a power amplifier, just as planned at the system architecture level in Fig. 1.14. Also notice that this is pre-layout simulation and after parasitic extraction
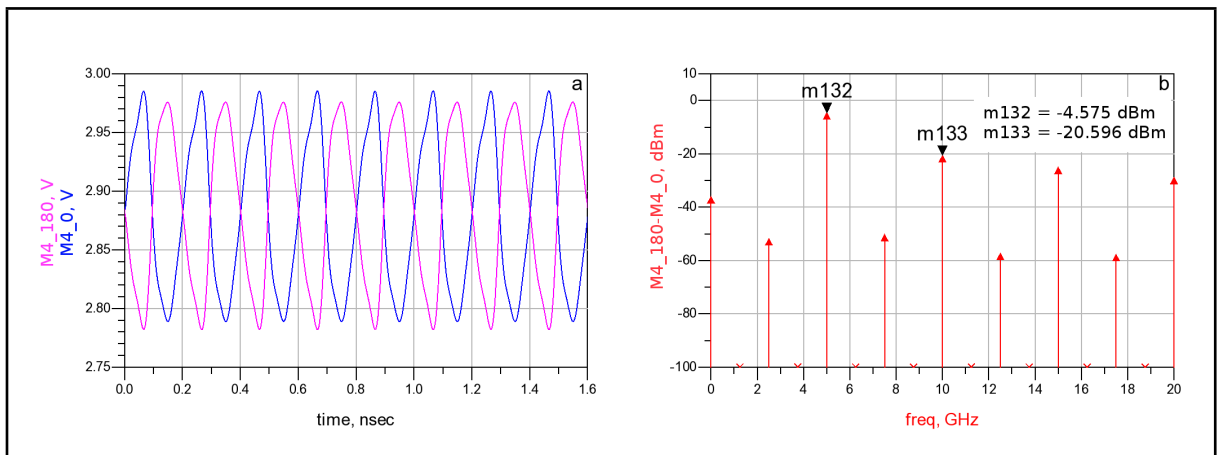
Figure 2.44: a. Transient output signal of 2nd frequency doubler b. Frequency spectrum of 2nd frequency doubler output
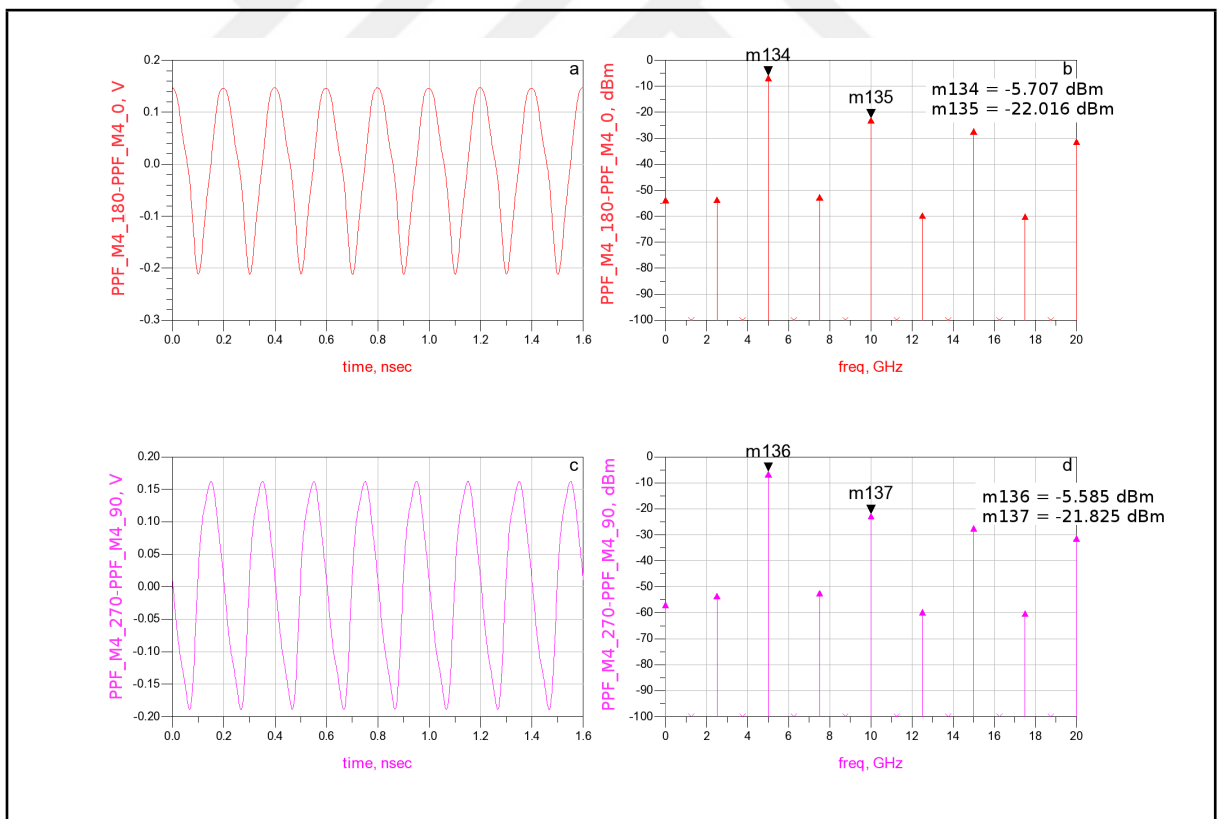
Figure 2.45: a.First transient output signal of 3rd PPF b. Frequency spectrum of 3rd PPF first output c. Second transient output signal of 3rd PPF d. Frequency spectrum of 3rd PPF second output

the output power will be much lower. Main signal at 10 GHz is at about −9 dBm and its closest harmonic is about 15 dB below. The effect of harmonics can be clearly seen in Fig. 2.46.a. Harmonic level is also unsatisfactory in terms of target specification. At next design iteration, there will be some frequency selective structures, low pass filters or LC tuned loads, to address harmonic level problem. In Fig. 2.47, phase noise
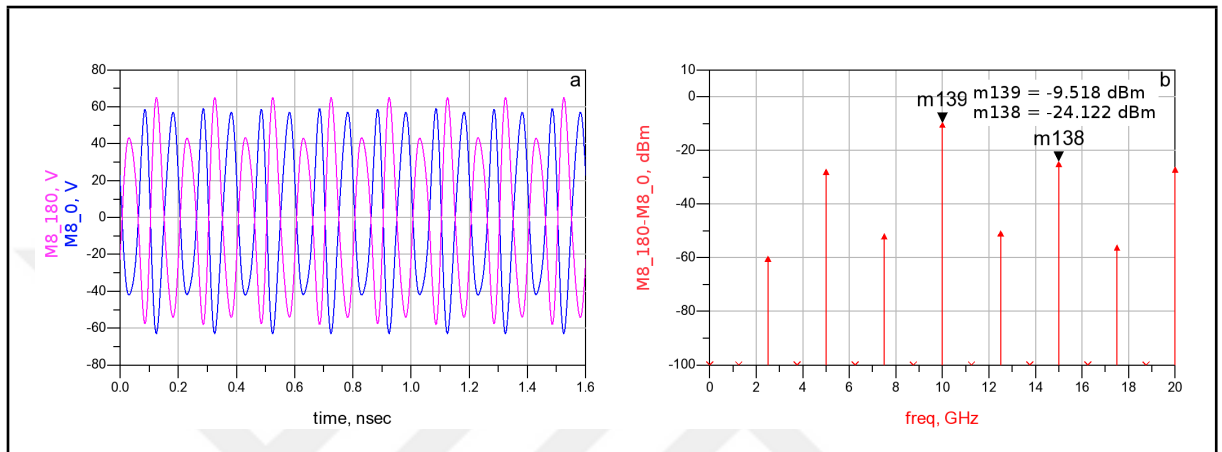
Figure 2.46: a. Transient output signal of 3rd frequency doubler b. Frequency spectrum of 3rd frequency doubler output

of input and output of M8X core is plotted. SSB phase noise of input signal at 1 kHz offset is −173.1 dBc/Hz which is almost numerical noise floor of simulator. SSB phase noise of M8X core at 1 KHz offset is $−133.9 dBc/Hz$ which is better than the target specifications given at table 1.1. There is still some headroom for additional blocks such as power amplifier in terms of target phase noise specification. Fig. 2.48 represents the variation of single side band phase noise at 1 kHz offset with input power and VGA control voltage. This figure shows that there is such a VGA control voltage which satisfies the SSB phase noise specifications for any input power greater than -10 dBm.
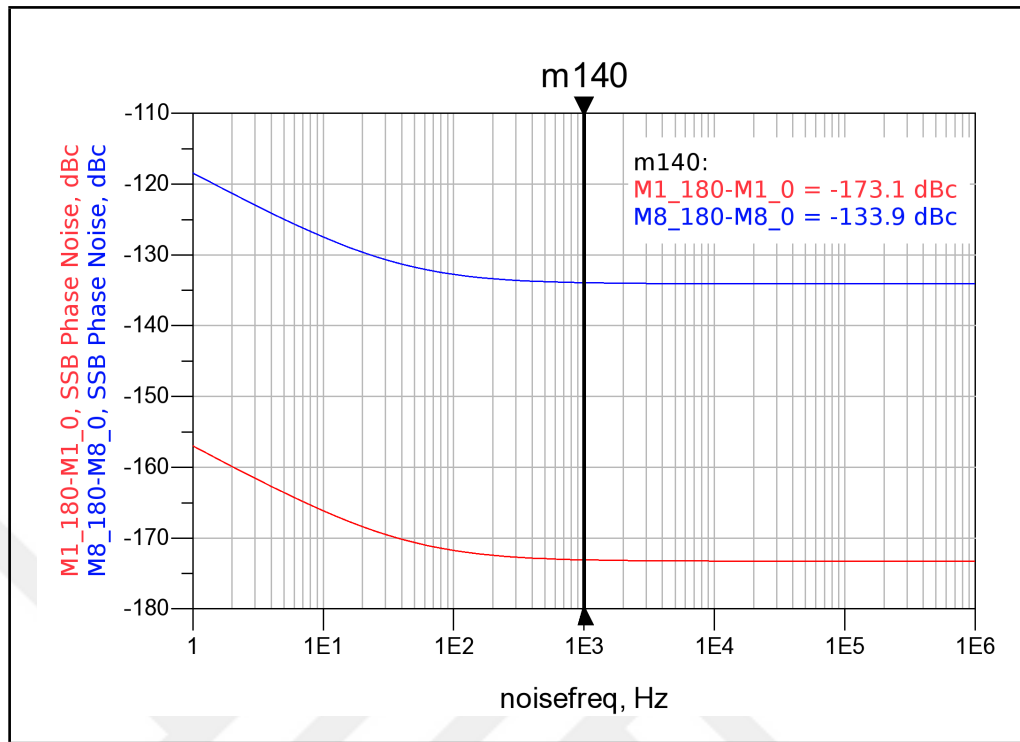
Figure 2.47: Phase noise of input and output signal
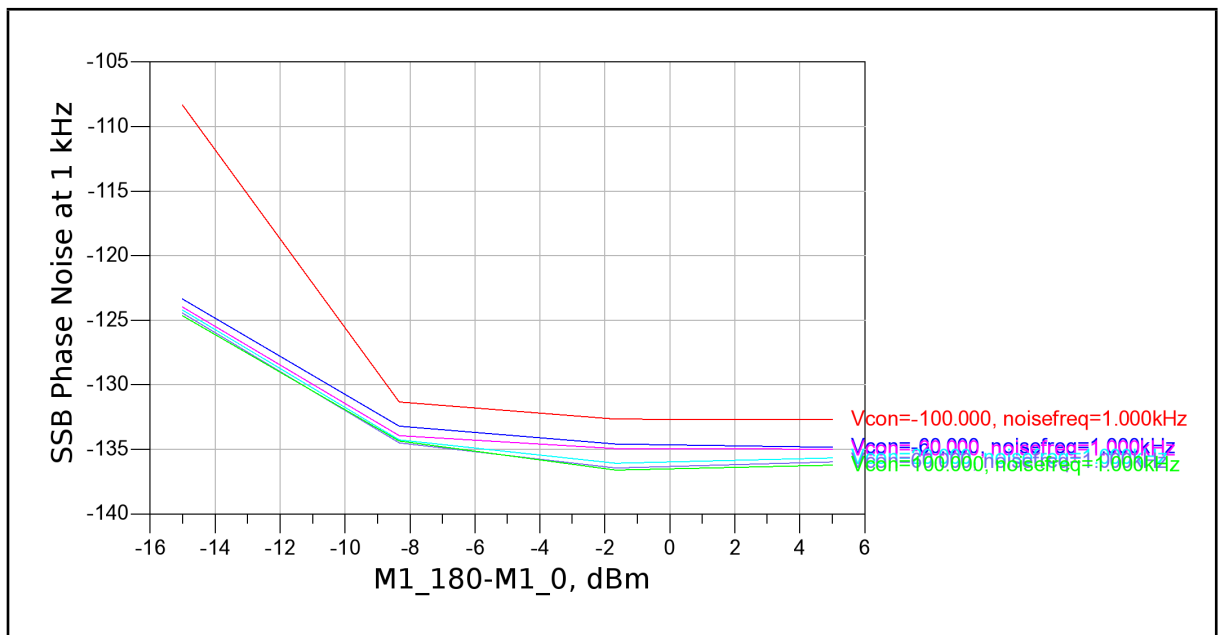
Figure 2.48: Phase noise of output signal for different VGA control voltages and
input powers

2.3.5. Die 2 - M8X Core Layout

After the completion of electrical design and simulation of the M8X Core, physical design was done by using Cadence Layout Editor. For DRC and LVS verification, Assura toolset was used. Final layout is given in Fig. 2.49 and input/output descriptions are listed in Table 2.4. Final M8X Core die dimesion is 2.28 mm by 1.175 mm.
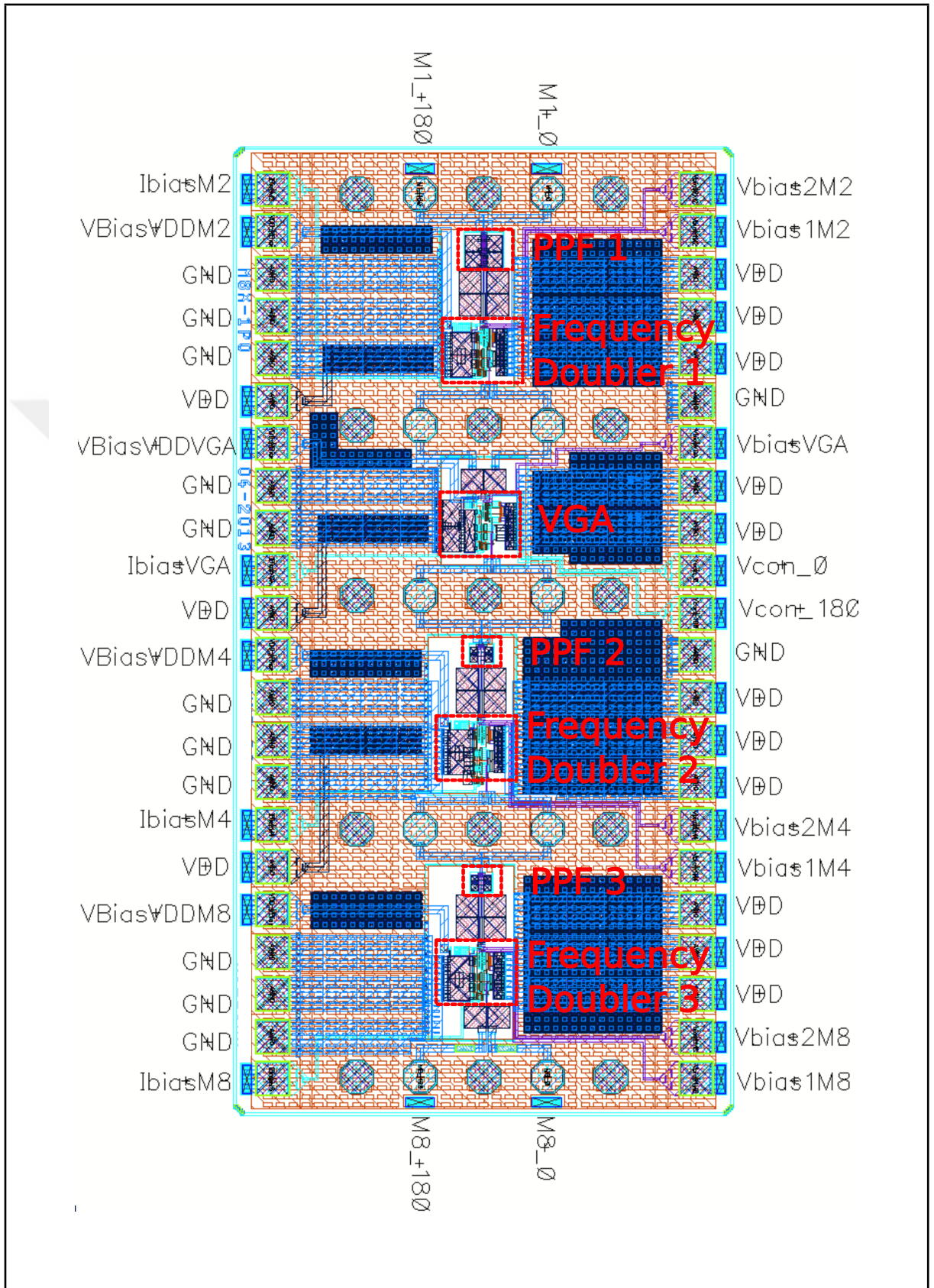
Figure 2.49: Die 2 - M8X core layout

Table 2.4: M8X core input and output descriptions

Name	Nominal Value	Description
VDD	4 V	Positive power supply
GND	0 V	Positive power supply reference
M1_0, M1180	-	Differential input signal
M80, M8180	-	Differential output signal
IbiasM2	1 mA	1st Frequency doubler biasing current
VBiasVDDM2	4 V	1st Frequency doubler biasing voltage power supply
Vbias1M2	2.2 V	1st Frequency doubler 1st biasing voltage
Vbias2M2	3.4 V	1st Frequency doubler 2nd biasing voltage
IbiasVGA	1 mA	VGA biasing current
VBiasVDDVGA	4 V	VGA biasing voltage power supply
VbiasVGA	2.2 V	VGA biasing voltage
Vcon_0, Vcon_180	3.3 V	VGA control voltage
IbiasM4	1 mA	2nd Frequency doubler biasing current
VBiasVDDM4	4 V	2nd Frequency doubler biasing voltage power supply
Vbias1M4	2.2 V	2nd Frequency doubler 1st biasing voltage
Vbias2M4	3.4 V	2nd Frequency doubler 2nd biasing voltage
IbiasM8	1 mA	3rd Frequency doubler biasing current
VBiasVDDM8	4 V	3rd Frequency doubler biasing voltage power supply
Vbias1M8	2.2 V	3rd Frequency doubler 1st biasing voltage
Vbias2M8	3.4 V	3rd Frequency doubler 2nd biasing voltage

2.3.6. Die 2 - M8X Core Post Layout Simulation

All post layout simulations are made using Cadence Spectre RF simulator's PSS(Periodic Steady State) analysis. In Fig. 2.50, frequency spectrum of M8X Core output is shown. Due to layout parasitics, there is a 2.75 dB drop at the output power.
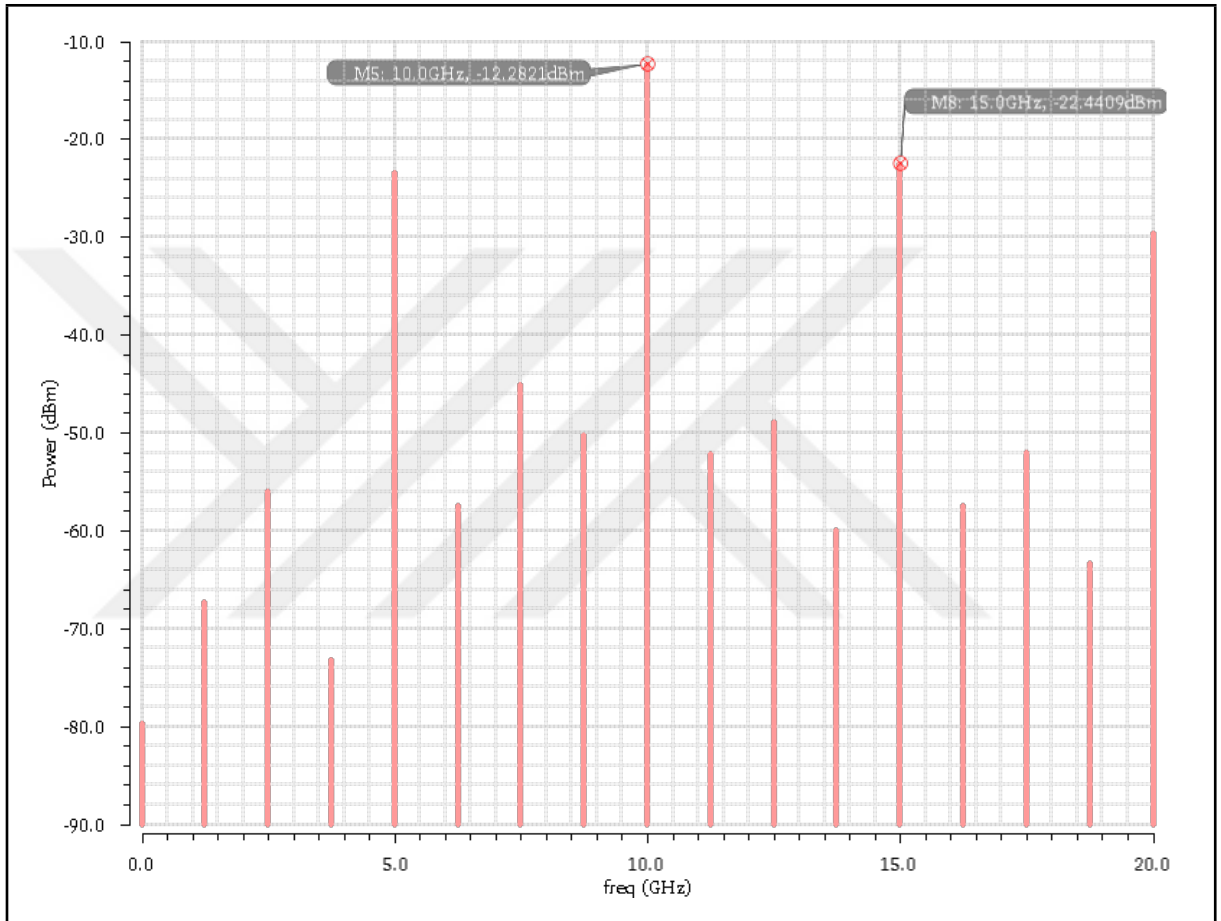
Figure 2.50: Frequency spectrum of 3rd frequency doubler output with layout parasitics

2.3.7. Die 2 - M8X Core Packaging

Two batches of prototypes were fabricated in CLCC68 package with separate bonding patterns. The batch with the bonding diagram shown in Fig. 2.51 was used for phase noise and frequency spectrum measurements. The second batch, where bonding diagram is given in Fig. 2.52, comprise the balun and M8X Core. Note that one of the differential outputs of M8X Core was terminated with 50Ω on package for enabling

testing with Ground-Signal-Ground(GSG) RF probes. This bonding diagram is used at frequency spectrum measurements.

.
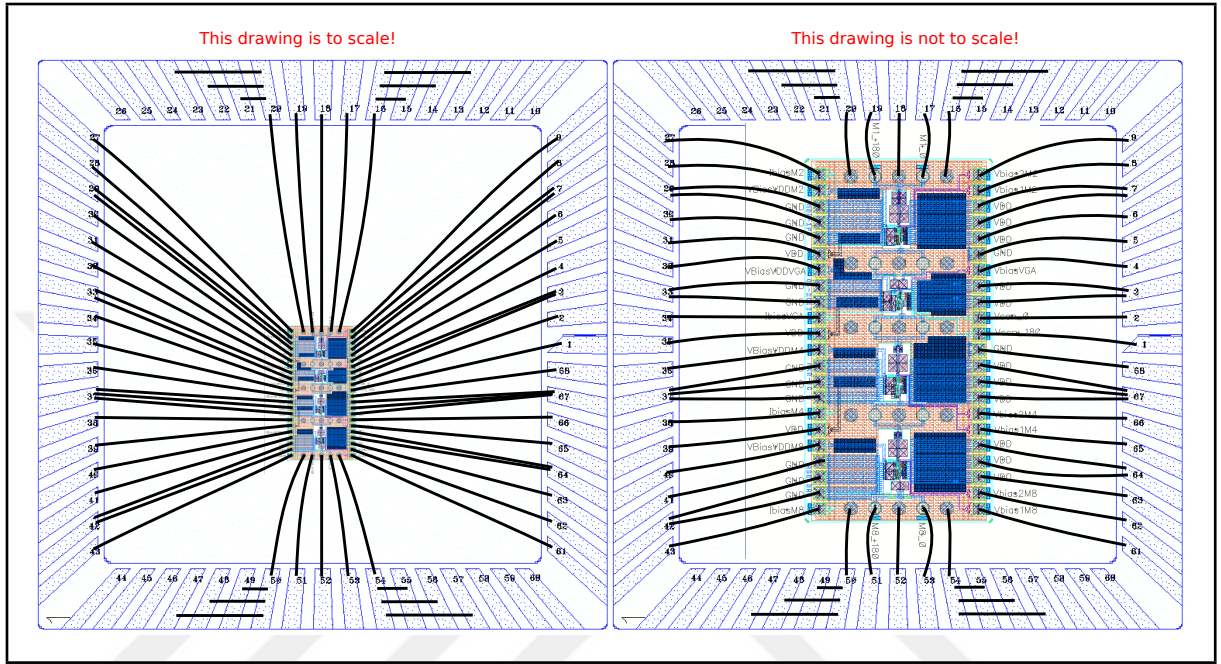
Figure 2.51: M8X core bonding plan 1

2.3.8. Die 2 - M8X Core Test Board Design

For testing of M8X core, the testbench shown in Fig. 2.53 was designed. The PCB housing this testbench is depicted in Fig. 2.53. It has the following features:

- Positive power supplies are filtered with a series inductor and a shunt capacitance.
- An on-board balun T1(Mini-Circuits ADTL 2-18) is used to generate a local differential signal from the single ended signal applied by the A4 SMA connector.
- Differential signal can also be applied from an external balun via A3 and A5 SMA connectors.
- Differential output signal of M8X core can be observed via A1 and A2 SMA connectors.
- Frequency doublers and VGA bias currents can be set through trimming potentiometers(U1, U2, U3, U4).
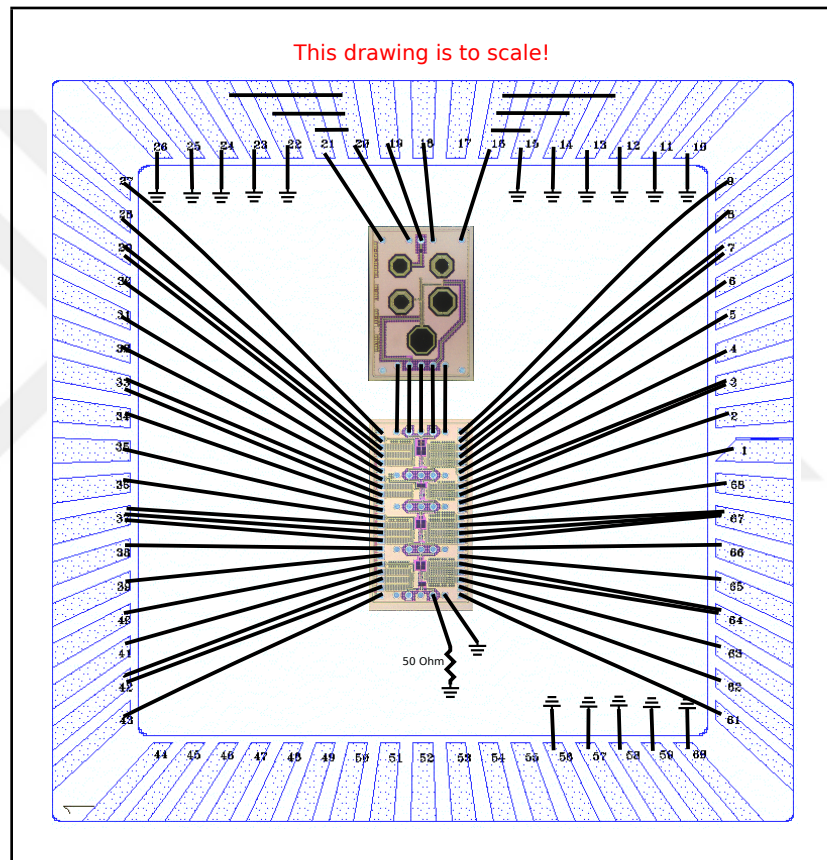
Figure 2.52: M8X core bonding plan 2

- Test points(J*) are added for setting and observing the biasing voltage of frequency doublers and VGA.
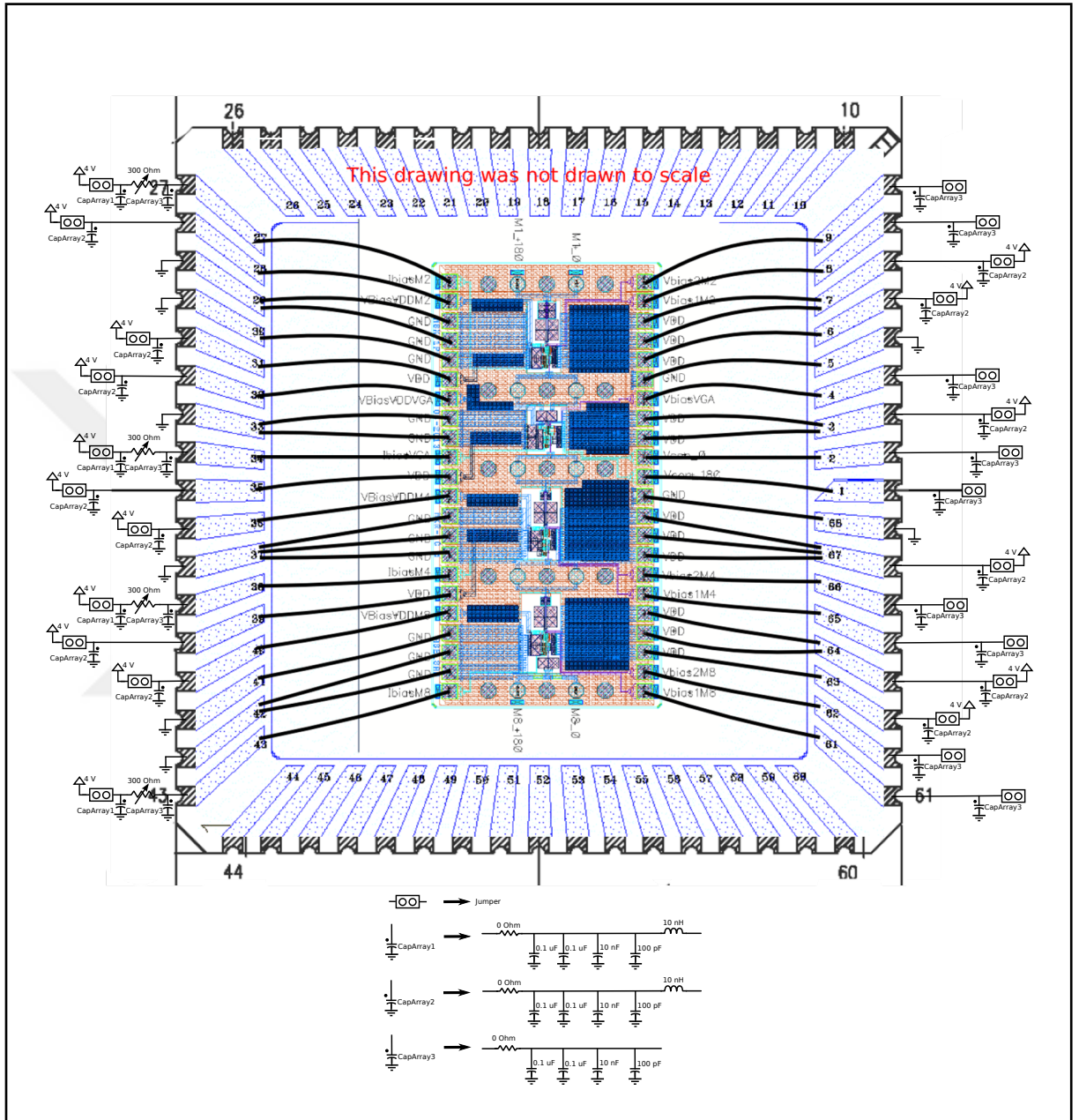
Figure 2.53: M8X core testbench
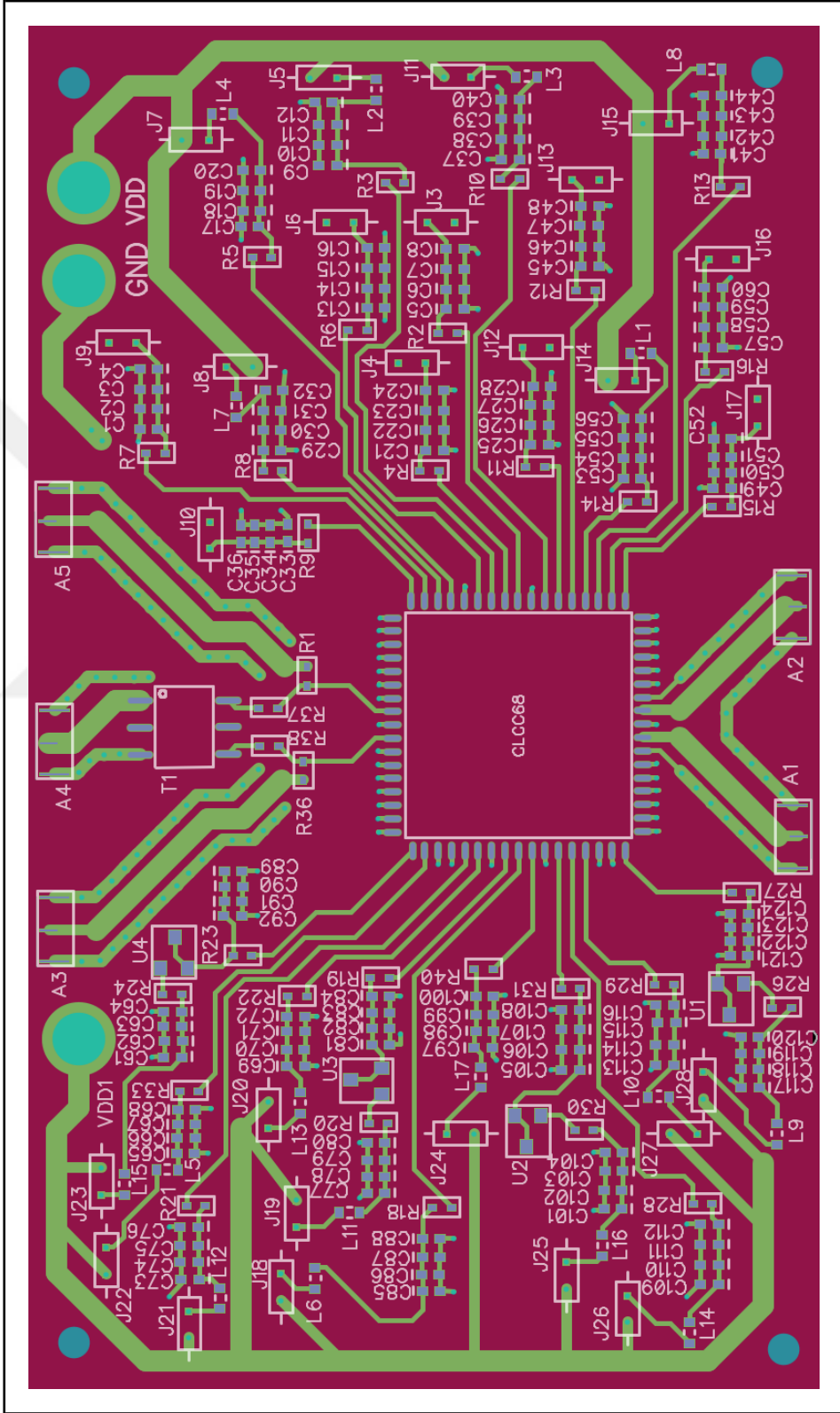
Figure 2.54: M8X core test board

2.3.9. Die 2 - M8X Core DC Testing

The first step of testing is the setting of the biasing currents of frequency doublers and VGA. Biasing currents are observed through the test points and trimming potentiometers(U1, U2, U3, U4) and are set until bias currents reach 1 mA. The measurement values of the DC biasing voltage of frequency doublers and VGA are listed in Table 2.4. Supply currents of sub-blocks are measured on three different chips. The measurement results are compared with simulated values in Table 2.5. A very tight distribution and close to perfect agreement with simulation are observed.

Table 2.5: M8X core supply current measurement

Block Name	Chip 1 supply current	Chip 2 supply current	Chip 3 supply current	Simulation supply current
Frequency Doubler 1	13.1 mA	12.31 mA	12.7 mA	12 mA
VGA	8.6 mA	8.06 mA	8.62 mA	8 mA
Frequency Doubler 2	15.6 mA	16.34 mA	16.54 mA	16 mA
Frequency Doubler 3	12.9 mA	12.51 mA	12.39 mA	12 mA

2.3.10. Die 2 - M8X Core Frequency Spectrum Testing

Frequency spectrum measurements conducted on for two different chips. An Agilient N9030A PXA Signal Analyzer is used in these tests. The first test was conducted on a chip attached to the PCB. M8X Core bonding diagram shown in Fig. 2.51 applies to this test. However since package and PCB are not designed for high freqeuncy application, there was an unknown insertion loss and used the cable used for testing also has about 1.5 dB insertion loss. The uncertainty at the insertion loss comes from the absence of accurate CLCC68 package and bond-wire model. A typical measured

spectrum is shown in Fig. 2.55. To check the correlation between simulation and test
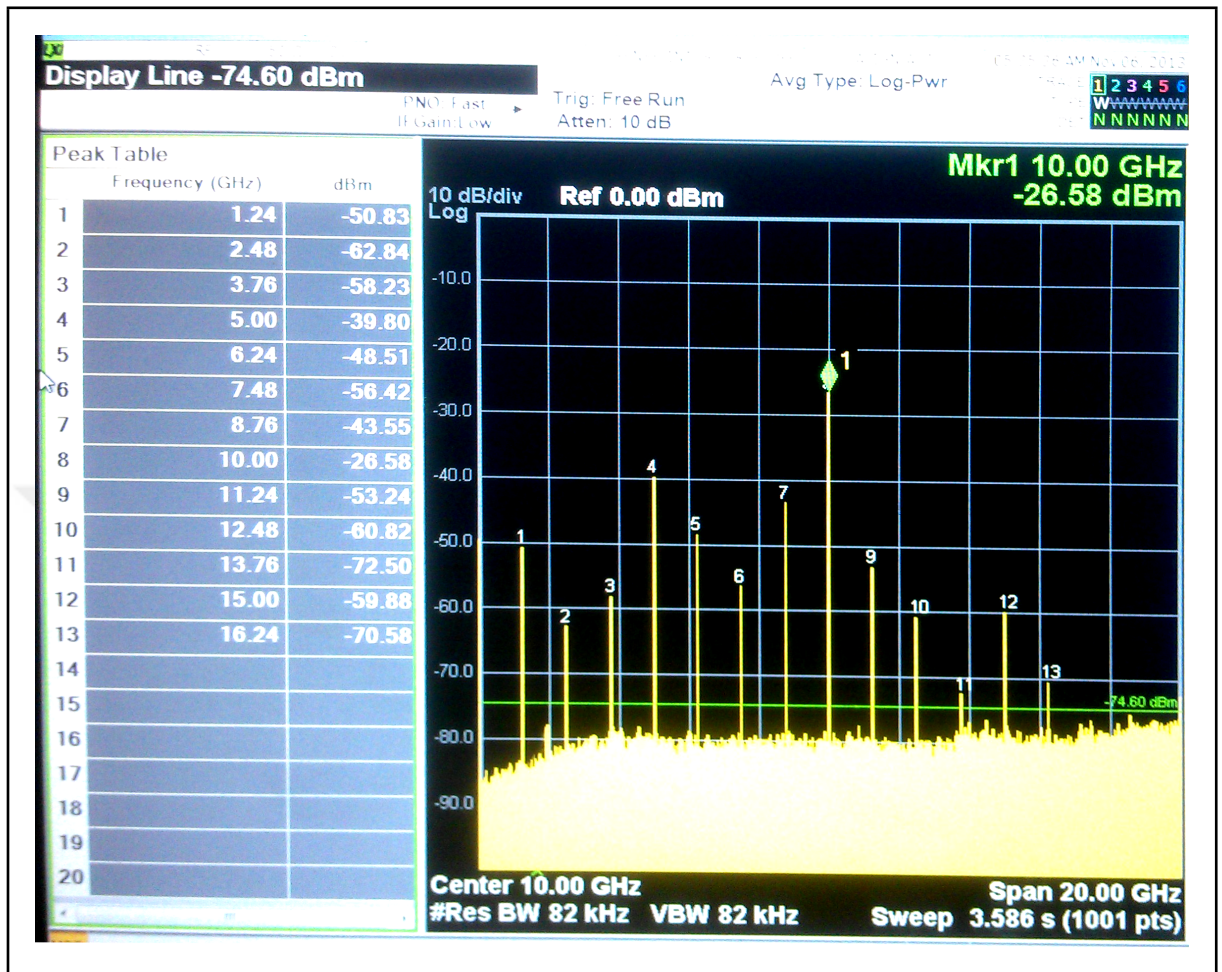
Figure 2.55: Sample screenshot of spectrum measurements.

results, approximate parasitic losses(package, bondwire) are added to the simulation environment and the simulation was repeated. Added bondwire model and component values are given in Fig. 2.56 and Table 2.6. Fig. 2.57 shows the measured and
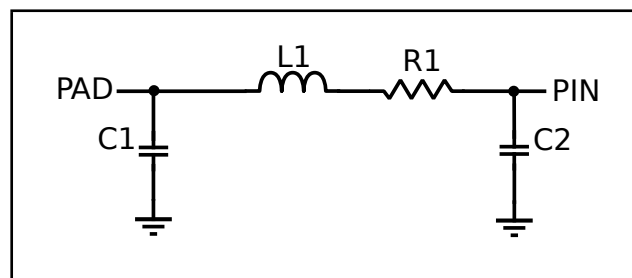
Figure 2.56: Bond wire model

simulated output power versus with power. As seen from the figure there is close

Table 2.6: Bond wire model component values

Component Name	RF Inputs	RF Outputs
C1	100 fF	100 fF
C2	1 pF	1 pF
L1	1 nH	2 nH
R1	100 mΩ	100 mΩ

agreement between simulation and test results. A second measurement was made by
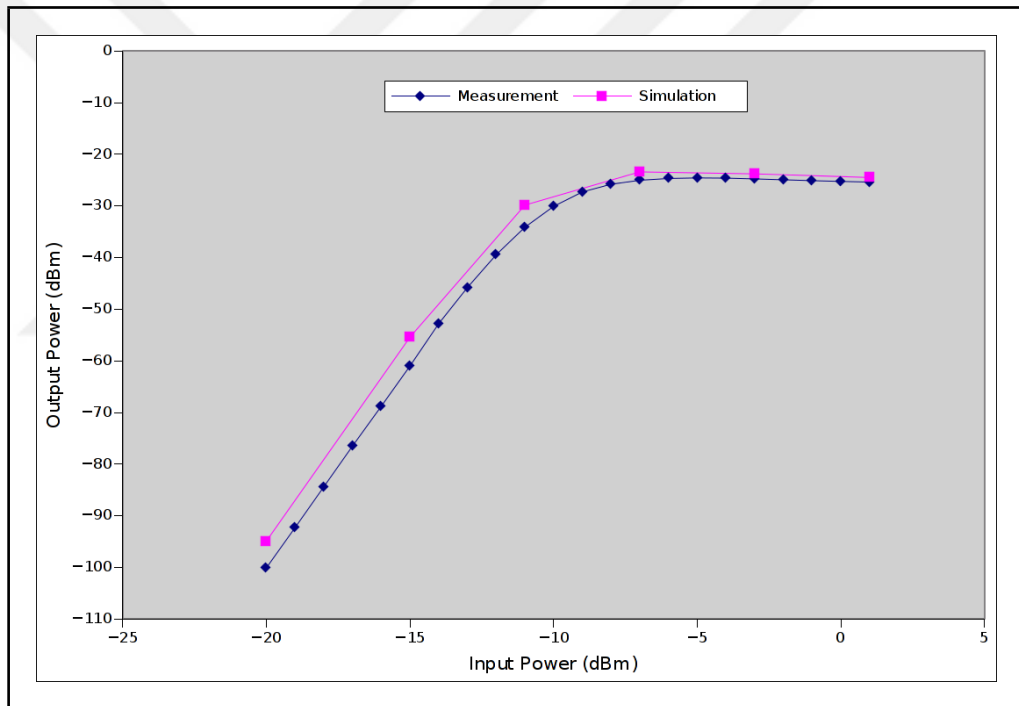
Figure 2.57: Input power vs output power.

using M8X Core bonding plan 2 in Fig. 2.52 and Fig. 2.58. During this measurement, a Picoprobe 40A-GSG-150-DP RF was used. The measurement environment is depicted in Fig. 2.59.

Shown in Fig. 2.60 are two measurement results obtained for two different level of input power (-6 dBm and -8 dBm). The harmonic level observed in these tests is higher than expected. Main signal and harmonic at half frequency is almost same which is not the
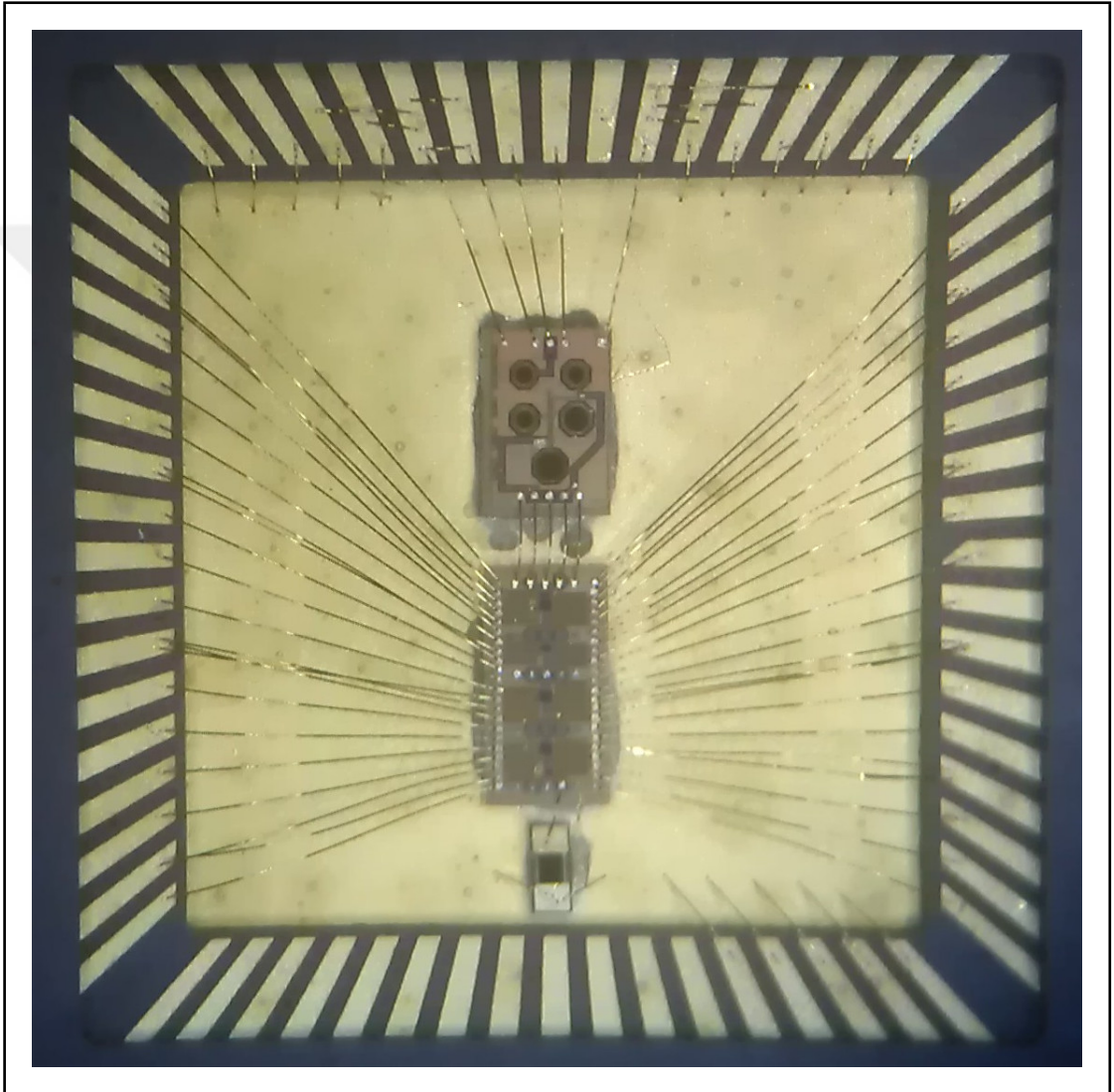
Figure 2.58: M8X Core bonding plan 3 photo

Figure 2.59: Measurement environment

case observed in simulations and previous testing conducted on bonding plan 1.
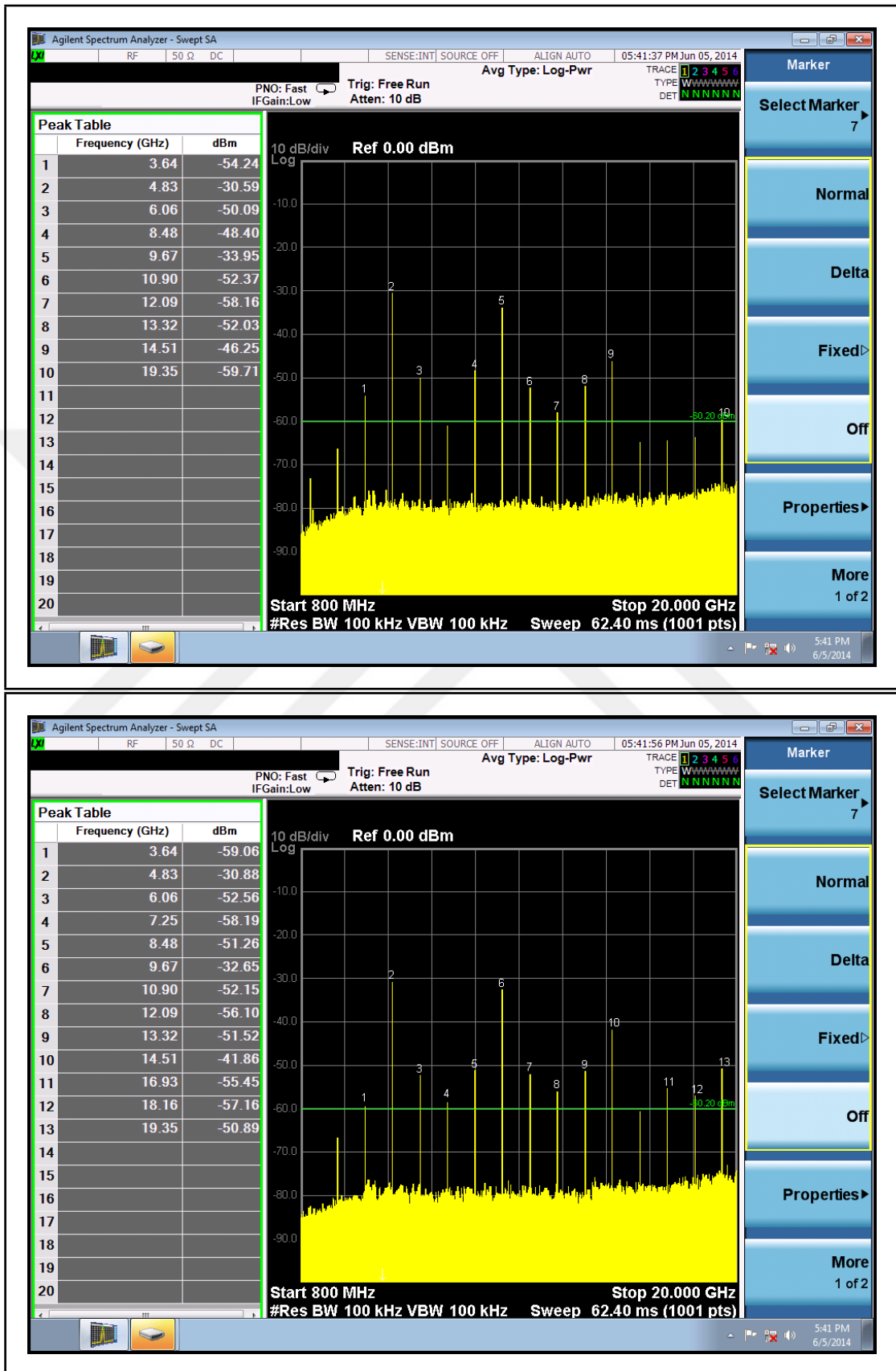
Figure 2.60: Sample screenshot of spectrum measurements

2.3.11. Die 2 - M8X Core Phase Noise Testing

As modelled by (1.2), frequency multiplication degrades phase noise. In the present design, theoretically phase noise is expected to worsen by 18 dB. Therefore, to measure a simulated -130 dBc/Hz phase noise at 1 kHz offset at the output of the M8X Core input, signal source phase noise should be better than -148 dBc/Hz. Generating such a low noise at 1 GHz is not trivial and such low noise crystal can cost more than \$20,000. One of the publications about the complexity of generating and measuring low phase noise signal at 10 GHz is given in [5] and corresponding plot is in Fig. 2.61. In figure, red line represents the low noise quartz crystal with perfect multiplier. Measured phase noise at 1 kHz offset is about -120 dBc/Hz. Since at our case, we do not have a perfect multiplier or such a low noise signal source, measuring a low phase noise at the output of M8X Core will require special measurement methods and devices.

The first set of phase noise measurements are conducted with an Agilient E5052B Signal Source Analyzer and an Agilient E5053A Microwave Downcoverter. As a signal source Rohde&Schwarz SMA100A Signal Generator is used. At SMA100's datasheet, phase noise performance is defined as $-132dBc/Hz$ at $1kHz$ offset. Measurement result can be seen in Fig. 2.62.

In order to prove input signal SSB phase noise is the limiting factor, a second measurement was taken with signal source which has a better SSB phase noise characteristic. Second measurement was made using ultra low phase noise signal source and OEwaves' Ultra-High Performance Automated Phase Noise Measurement System. Hittite's HMC444 GaAs HBT MMIC x8 Active Frequency Multiplier was also characterized as a reference for M8X Core testing. Since signal power level is below $-20dBm$, three cascaded Hittite's HMC-C072 Ultra Low Phase Noise Amplifiers were used at the output of M8X Core and one HMC-C072 was used at Hittite's reference product. Results are summarized in Table 2.7. M8X Core Simulation results shown in this table are different from those in Fig. 2.47. This is because we resimulated M8X Core with the phase noise profile of the signal source used in measurements. This measurement shows that, measurement SSB phase noise of M8X core is still limited by input sig-
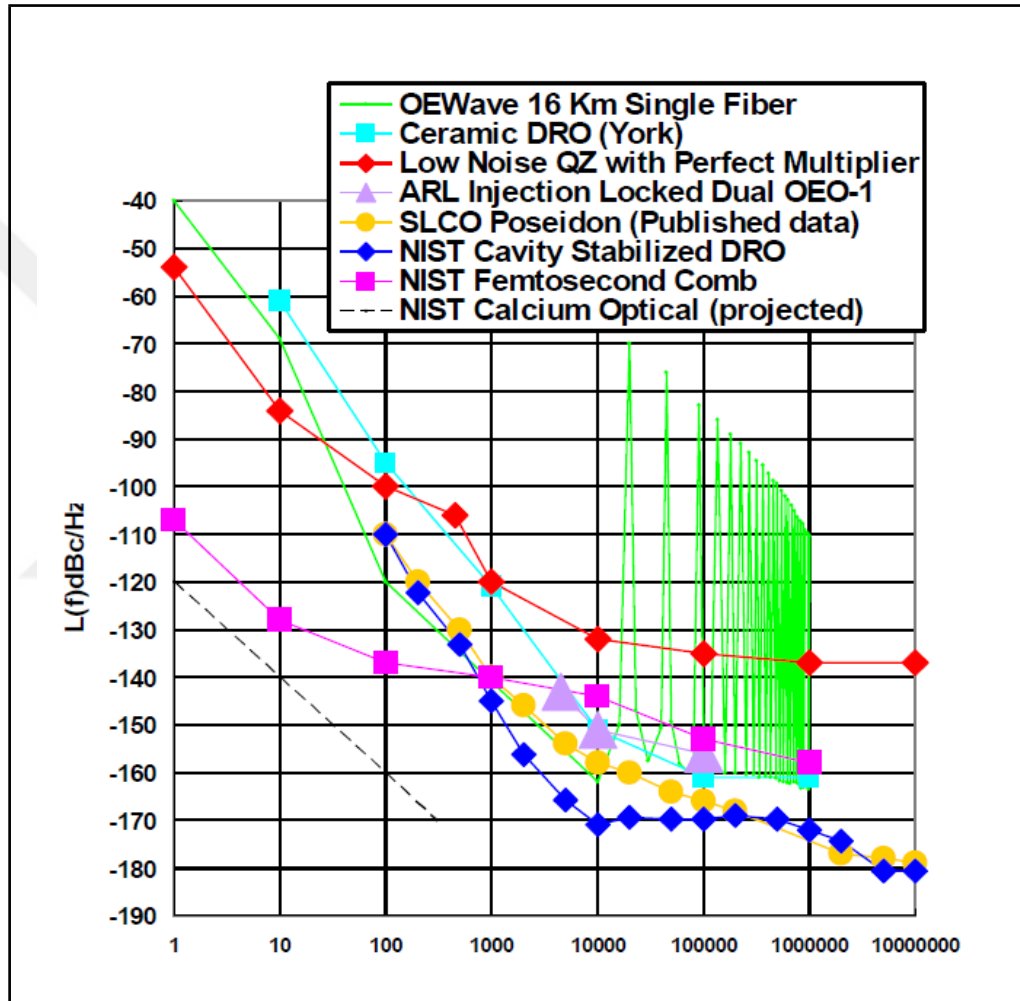
Figure 2.61: Eight L(f) plots of different classes of oscillators with a normalized frequency of 10 GHz according to [5].

Figure 2.62: Agilent E5052B Signal Source Analyzer & SMA100 phase noise measurement

nal source. Thus in order to measure targeted SSB phase noise specifications, higher performance signal source is required.

Table 2.7: Phase noise measurement(dBc/Hz)

Frequency	Signal Source	M8X Core Measurement	M8X Core Simulation	HMC444 Measurement	HMC444 Datasheet Data
100 Hz	-137	-85	-118	-88	-122
1 kHz	-152	-115	-131	-122	-130
10 kHz	-153	-135	-131	-132	-136
100 kHz	-156	-135	-133	-132	-136
1 MHz	-156	-135	-133	-132	-136

2.3.12. Results

M8X Core tests indicate the following for spectral performance:

- Measured output power level is closely correlated to post layout simulation but it is much lower than the target specifications. To overcome this problem individual block gains should be increased.
- VGA control voltages have some effect on the output gain but control range should be increased.
- Harmonic levels are too high. However this is not a big issue. It can be solved by adding frequency selective elements(filters) to final chip.

Phase noise performance could not be characterized accurately due to signal source limitations. However comparison with HMC444 indicated that M8X core would satisfy target phase noise specifications.

As mentioned in Section 2.1, main goals of this phase is validation of noise models of devices and chosen topology. Although there are some problems at signal and harmonic power levels, those can be easily solved by modifying the blocks. Foundry provided noise models are good enough to design new prototype and it is expected that new chip will fulfil target specifications.

3. SECOND PHASE

3.1. GOALS of SECOND PHASE

After the measurements of first prototypes, the shortcomings of the first phase of design were determined and taken into consideration in the next phase of prototyping. The goal of this second phase is to fully satisfy the target system specification given in Table 1.1. The second phase of the work involves one prototype die. Its design, modifications to the first phase design, simulation and testing are described in this chapter. All simulation results given in this chapter belongs to system level simulations. All blocks modified within the whole system to observe effects of individual modification to system performance. Thus all the simulation results given in this chapter belong to system level simulation. All simulations given in this chapter belong to "typical" process corner, unless otherwise stated. In Fig 3.1, final system level design is given. Notice that VGA was moved after the second frequency doubler. Additional blocks was added: differential to single ended converter(D/S), power amplifier(PA), peak detector, on-chip reference generator and digital to analog converter(DAC).
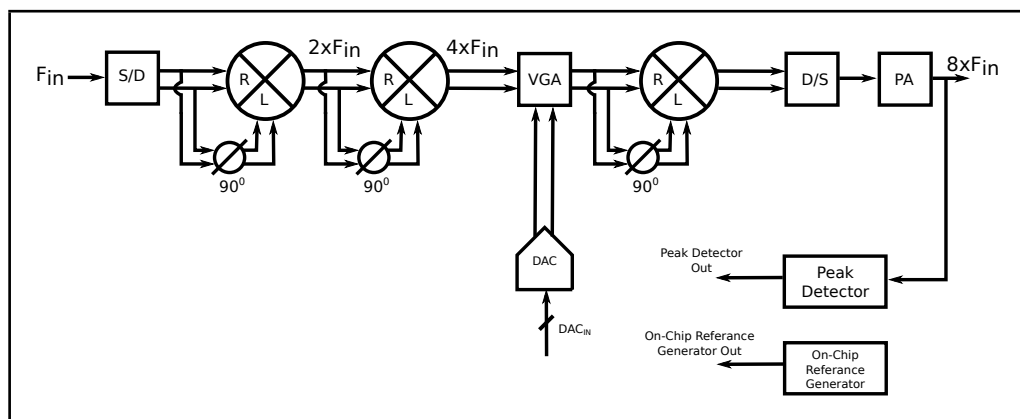
Figure 3.1: Second phase system level

3.2. MODIFICATIONS

3.2.1. First Frequency Multiplier

First action is taken against the overall system gain. As seen in Fig 2.57, for low input power(<-10 dBm), output power is below -40 dBm. To fulfil output power specification, at least 40 dB gain is needed in the last frequency doubler or amplifier. Designing such an high gain amplifier at 10 GHz is not trivial. Thus it was decided to compensate low input power at first frequency doubler. First frequency doubler was modified such that the emitter follower at its output is replaced with two cascaded saturation cells. Capacitive coupling is used between the frequency doubler and the saturation cells to isolate their DC bias points.
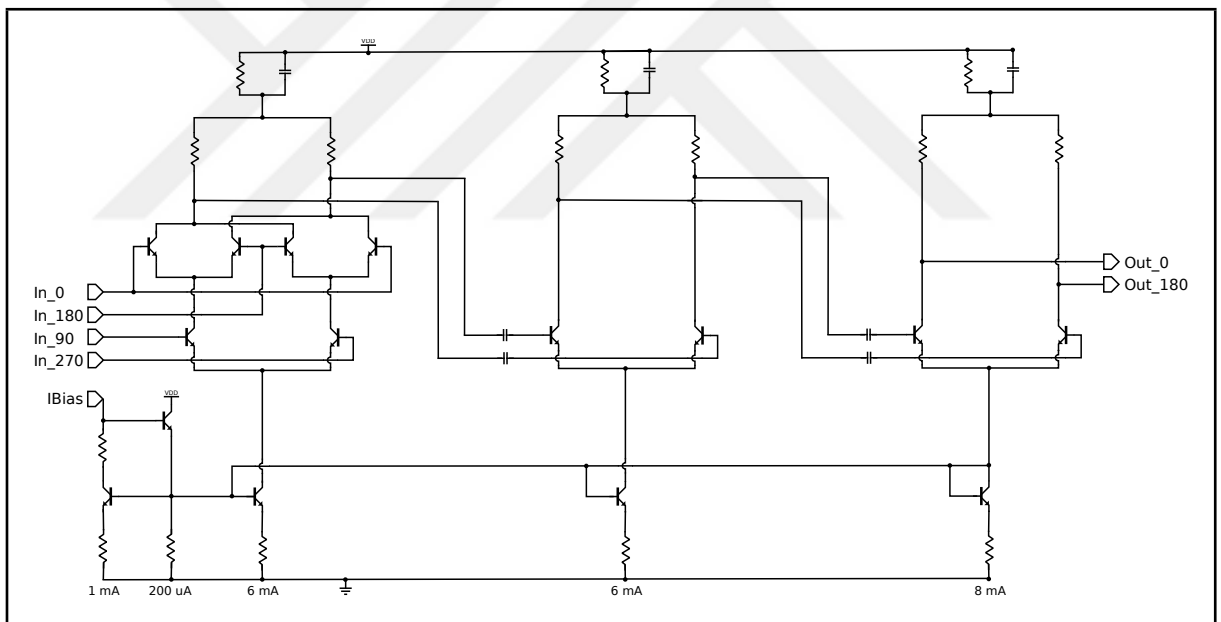
Figure 3.2: First frequency doubler with saturation cell.

Initial design has only one saturation cell however during corner analyses at low power inputs, it is seen that one saturation cell is not sufficient. In Fig 3.3, blue plot is output of frequency doubler, red plot is output of first saturation cell and green plot is output of second saturation cell. As seen from this figure one saturation cell is not sufficient for input power levels below -6 dBm(red plot), however with addition of second saturation cell, it is possible to take almost constant output power(green plot).
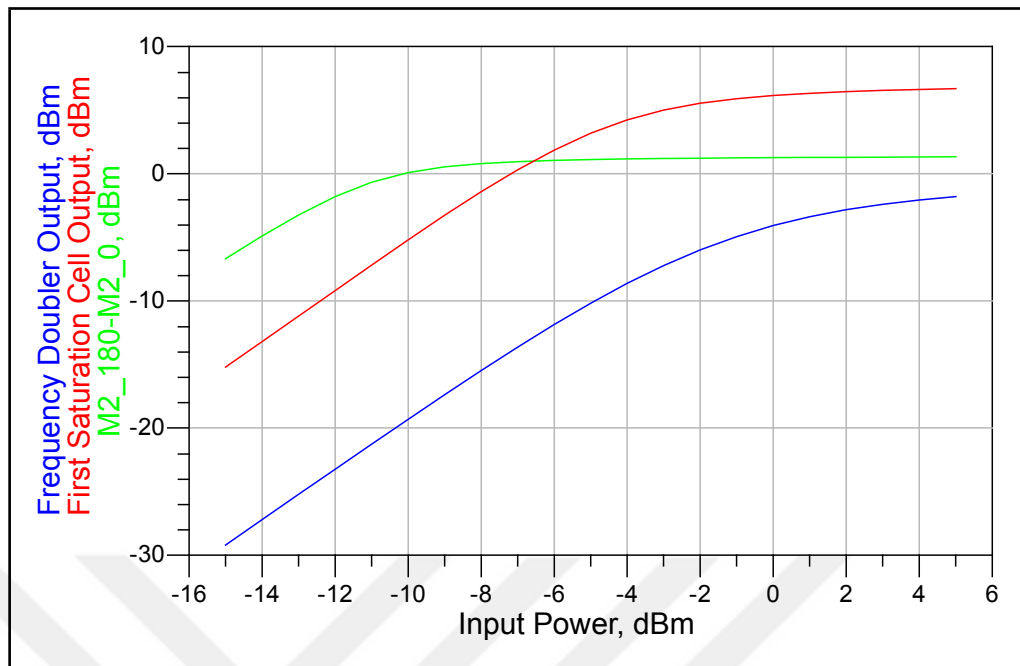
Figure 3.3: First frequency doubler with saturation cell simulation.

In Fig 3.4, the output of the first frequency doubler with saturation cells are plotted for three different corners(typical, worst and best). There is about 6 dB variation at the output power for -10 dBm input power. This variation will be compensated with VGA at later stages.
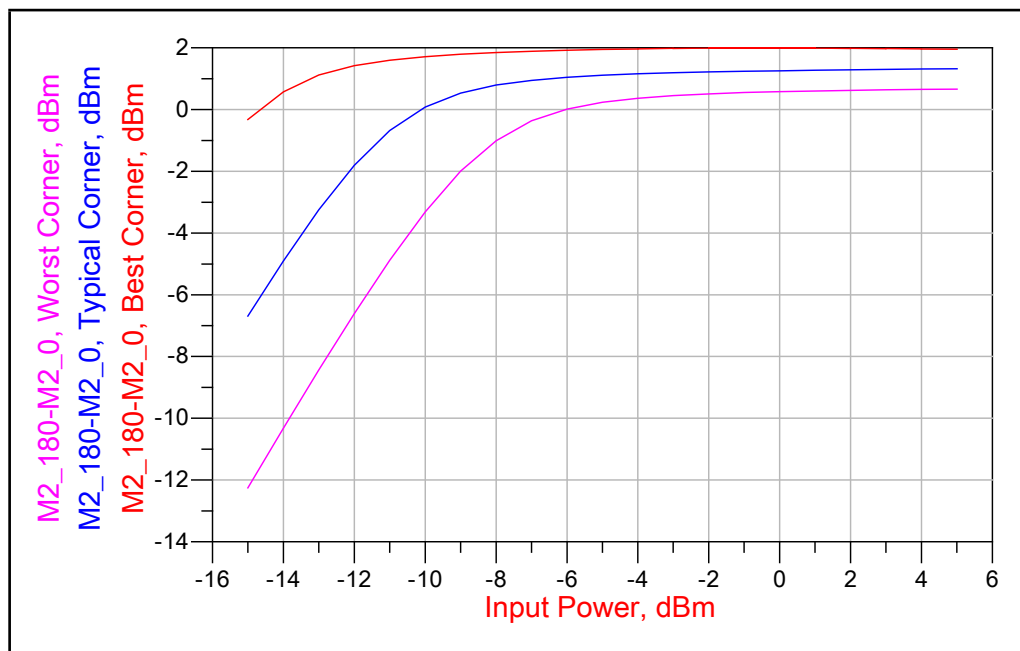
Figure 3.4: First frequency doubler with saturation cell corner simulation.

Main problem related to the saturation cell is its harmonic contents. Since it saturates the input signal to maximum level, it creates high power harmonic components as seen in Fig 3.5. In this figure output of saturation cell is plotted for 5 dBm input power. Harmonics are only 10 dB below the main signal for the given input power. Since it is out of target specifications, they have to be suppressed at later stages. In Fig 3.6,
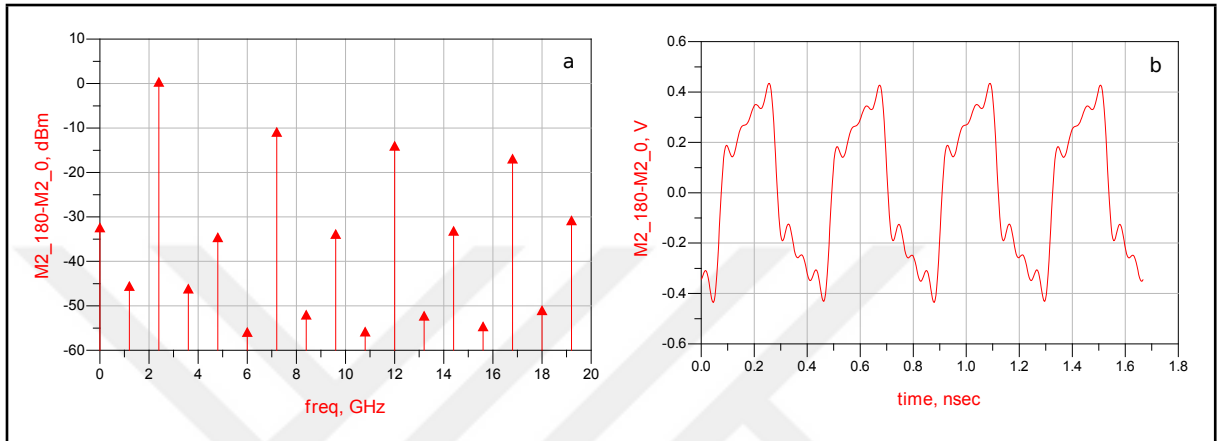
Figure 3.5: First frequency doubler with saturation cell transient and harmonic simulation for 5 dBm input power

same outputs are plotted for -10 dBm input power. As seen from the figures, harmonic levels are becoming better for low input powers.
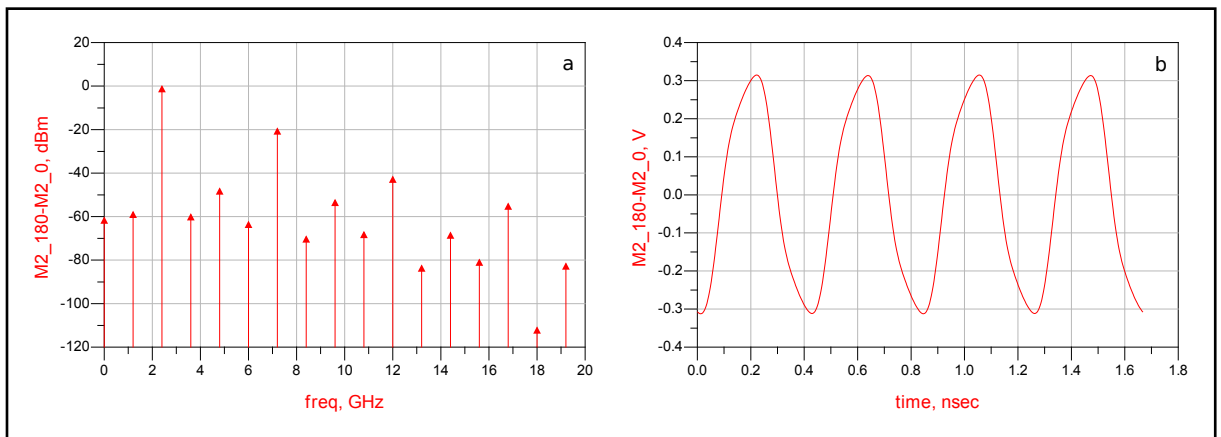
Figure 3.6: First frequency doubler with saturation cell transient and harmonic simulation for -10 dBm input power

3.2.2. Second Frequency Multiplier

Two modifications has been made on the second frequency multiplier. First, emitter
follower tail current is increased in order to counter the effect of process variations on
the gain. Second, a capacitor is added between load resistors to shape its frequency
response to low-pass. By that way, harmonics at frequencies higher than the main
frequency will be filtered out. The value of the capacitor was found using AC simulation
with layout parasitics.
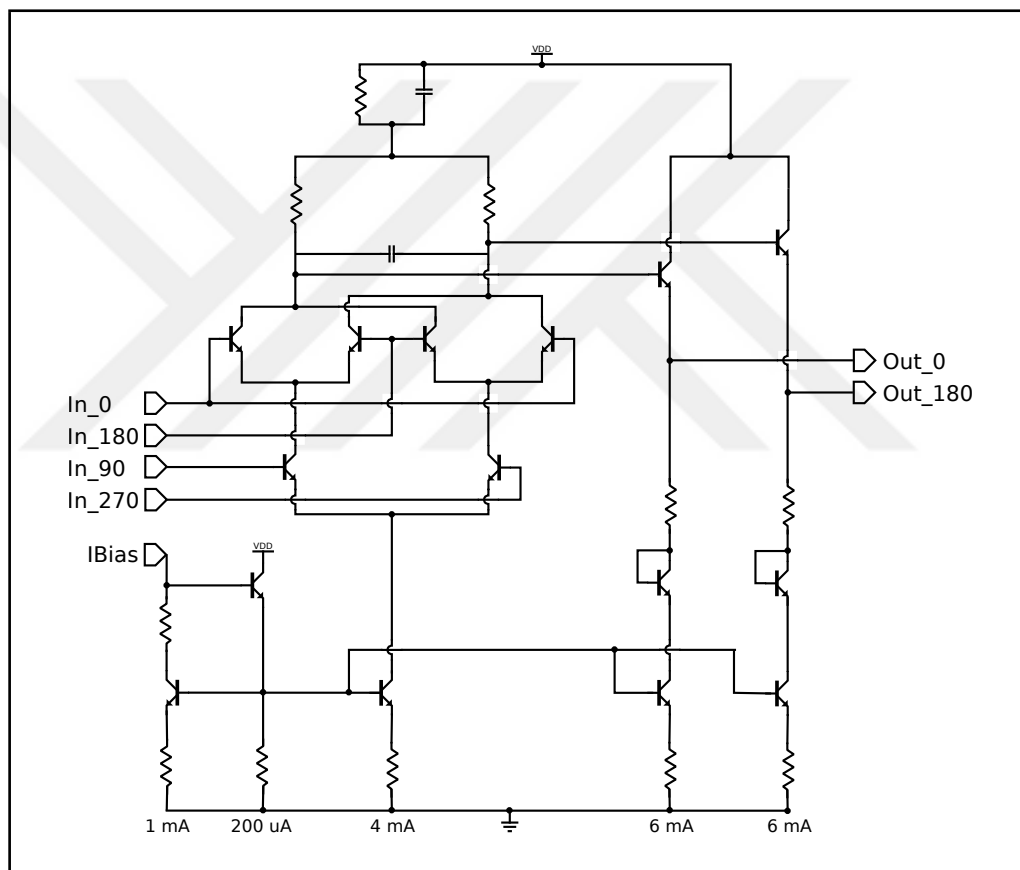
Figure 3.7: Second frequency doubler.

In Fig 3.8, harmonic balance simulation result is plotted for -10 dBm input power and
in Fig 3.9, harmonic balance simulation result is plotted for 5 dBm input power. As
seen from these figures, harmonic contents are still higher than target specifications.

In Fig 3.10, the output power of second frequency doubler was plotted for three different
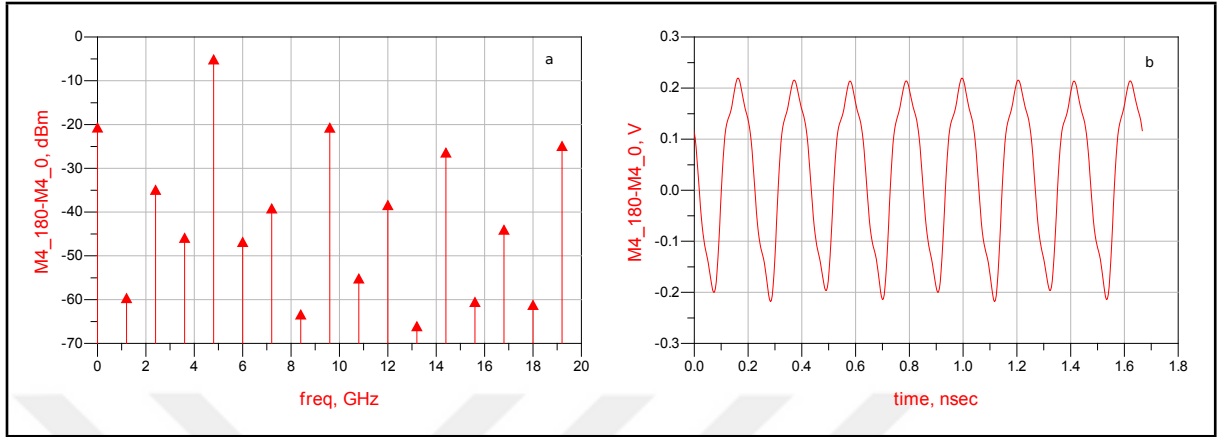
Figure 3.8: Second frequency doubler transient and harmonic simulation for -10 dBm input power
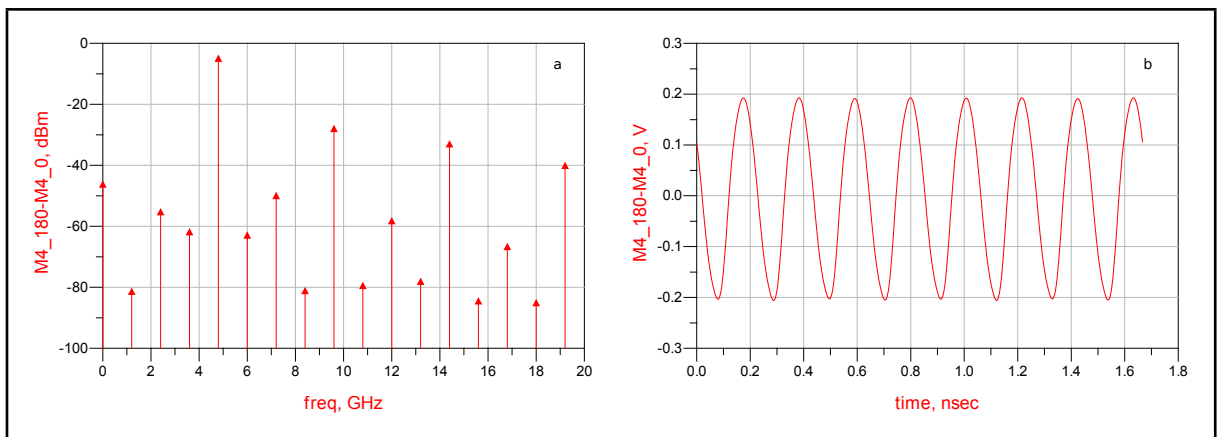
Figure 3.9: Second frequency doubler transient and harmonic simulation for 5 dBm input power

corners(typical, worst and best). There is almost constant output power for input power higher than -10 dBm.
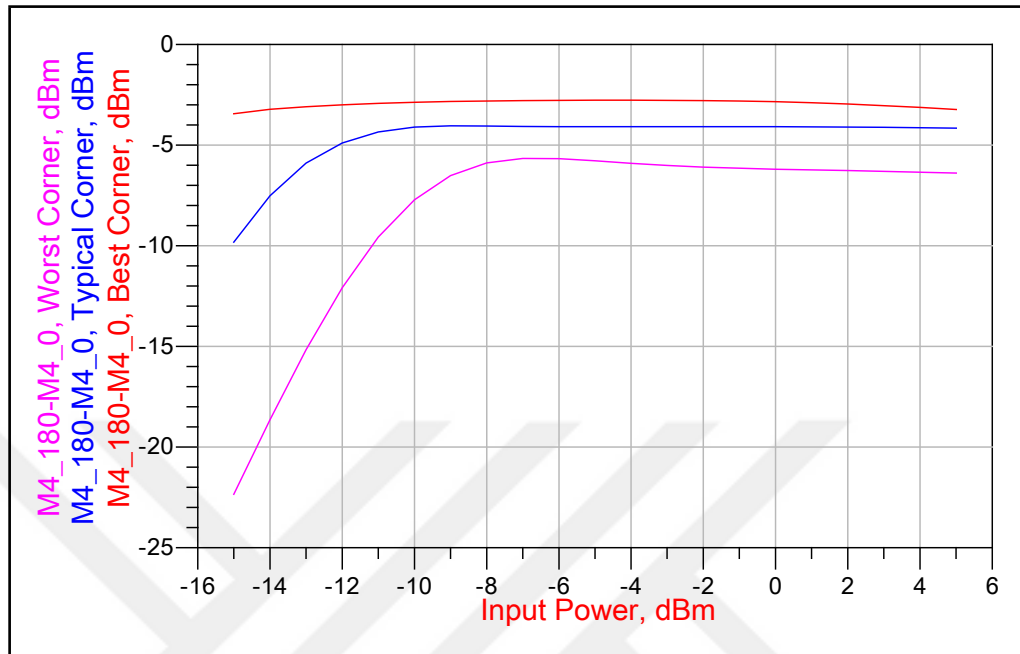
Figure 3.10: Second frequency doubler corner simulation.

3.2.3. Variable Gain Amplifier

Same modification as second frequency multiplier was made on VGA which are increasing tail current and shaping its frequency response to low pass. Corresponding figure can be seen in Fig 3.11.
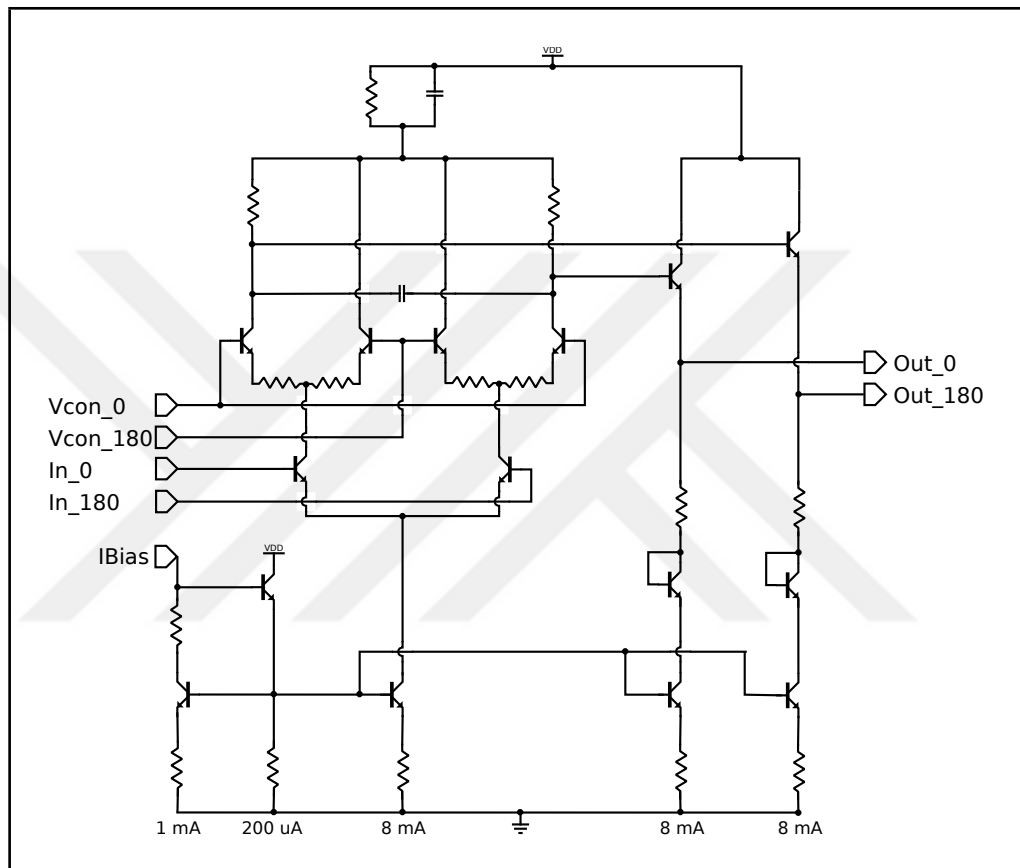
Figure 3.11: Variable gain amplifier- VGA

In Fig 3.12, VGA output is plotted for 5 dBm input power and -50 mV VGA control voltage. At this plot, closest harmonic is only 17 dB below main signal. In Fig 3.13, VGA output power is plotted for two different input power and VGA control voltages. This plot shows that VGA output power can be set to 0 dBm by tuning VGA control voltage for both -15 dBm and 5 dBm input power.

Fig 3.14 and Fig 3.15 are the output variation of VGA with process corners for -10 dBm and 5 dBm input power, respectively. As seen in these figures, VGA output can be set around 0 dBm for all process corners. By that way, almost constant power at
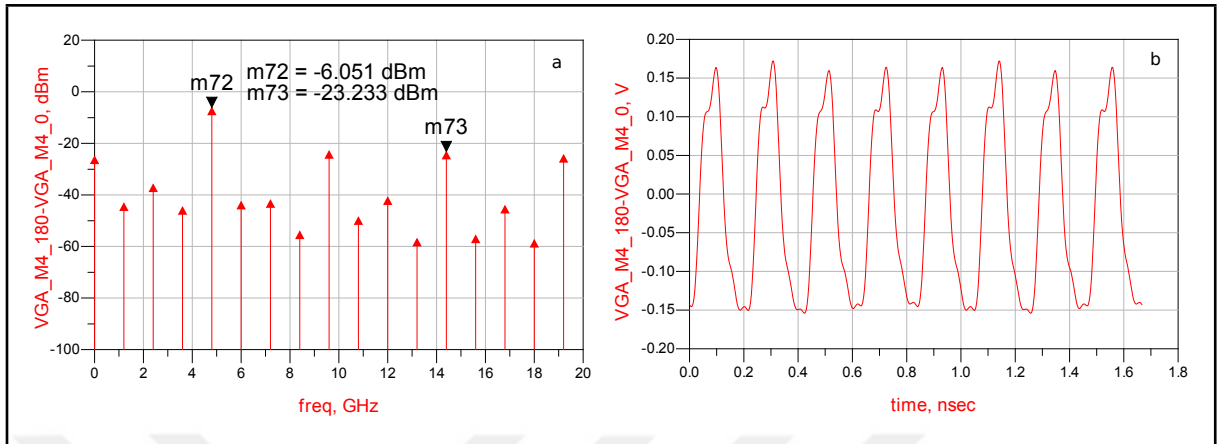
Figure 3.12: VGA output for 5 dBm input power and -50 mV VGA control voltage
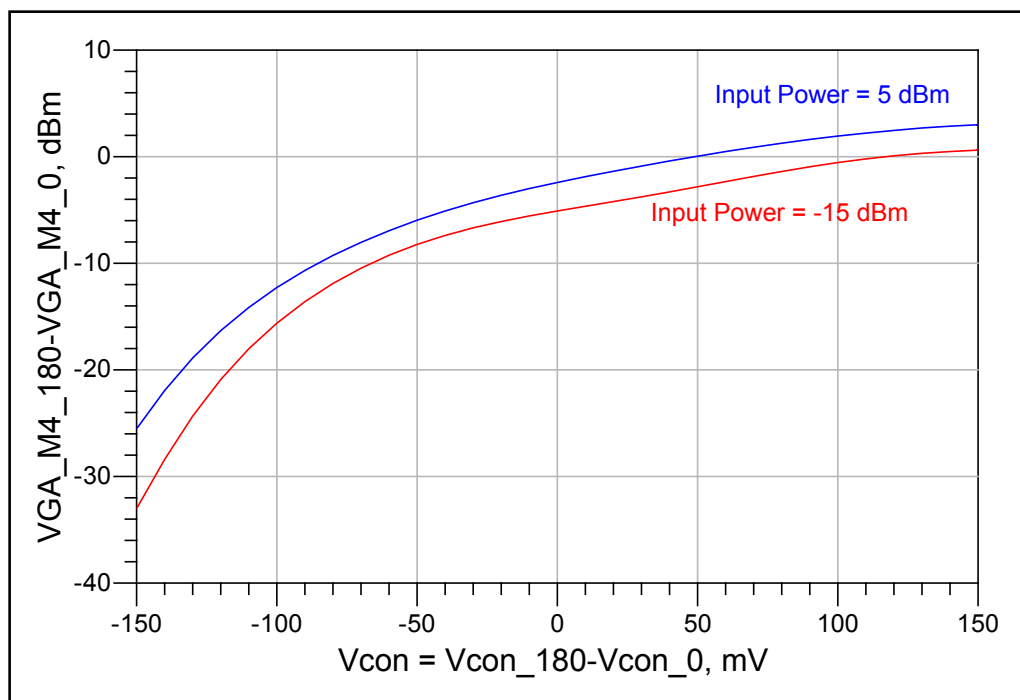
Figure 3.13: VGA output power for different control voltages and input powers

the output of VGA is guaranteed regardless of input power and process corner.
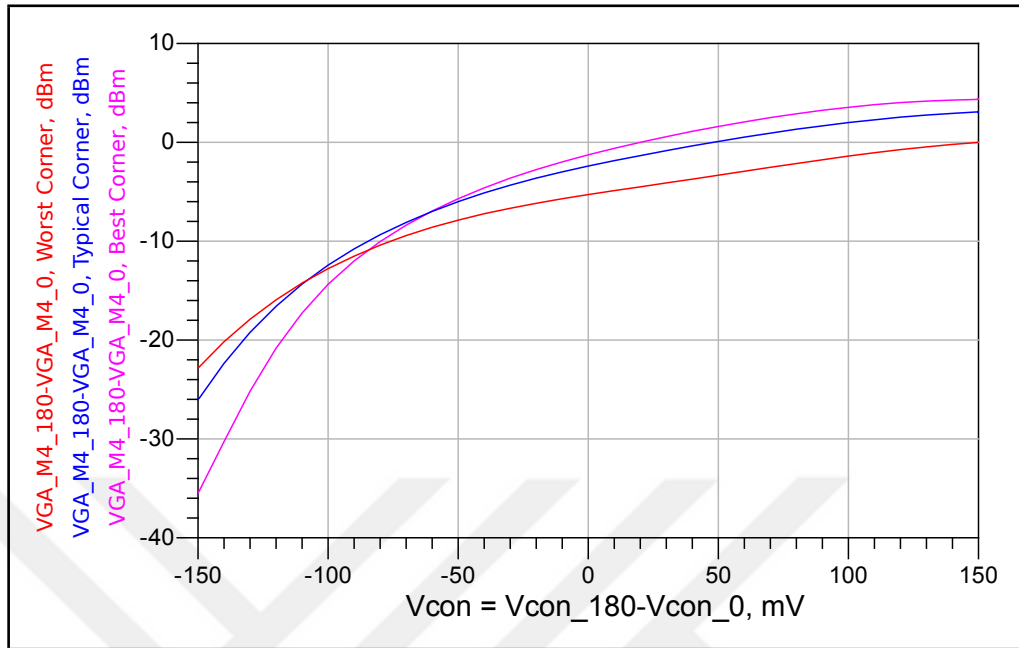
Figure 3.14: VGA corner simulation for -10 dBm input power
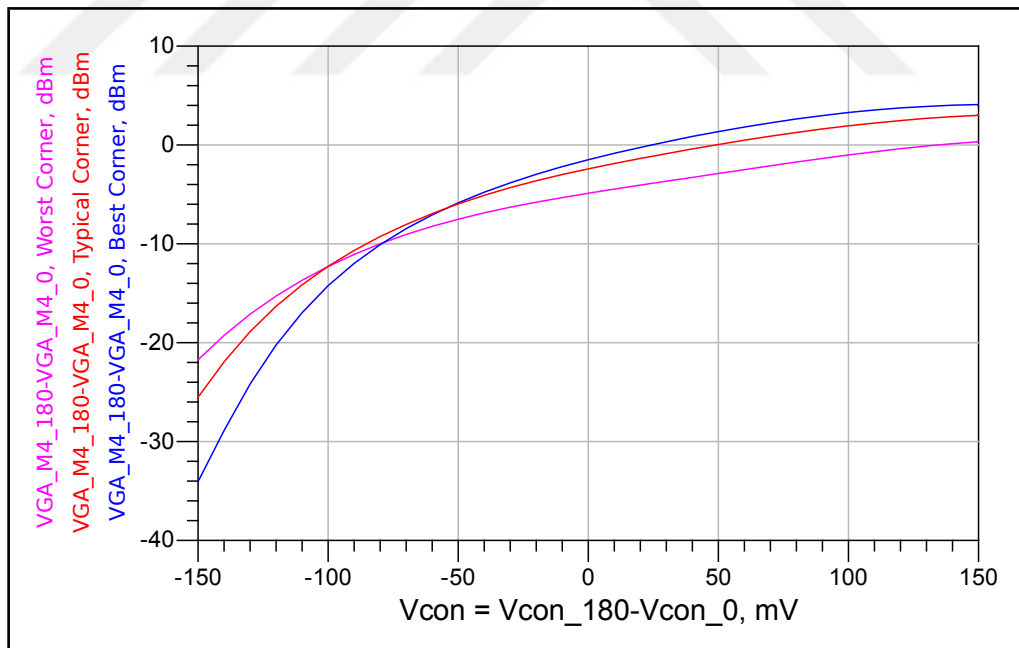
Figure 3.15: VGA corner simulation for 5 dBm input power

3.2.4. Third Frequency Multiplier

Two major modification was made on third frequency multiplier which is given in Fig 3.16.
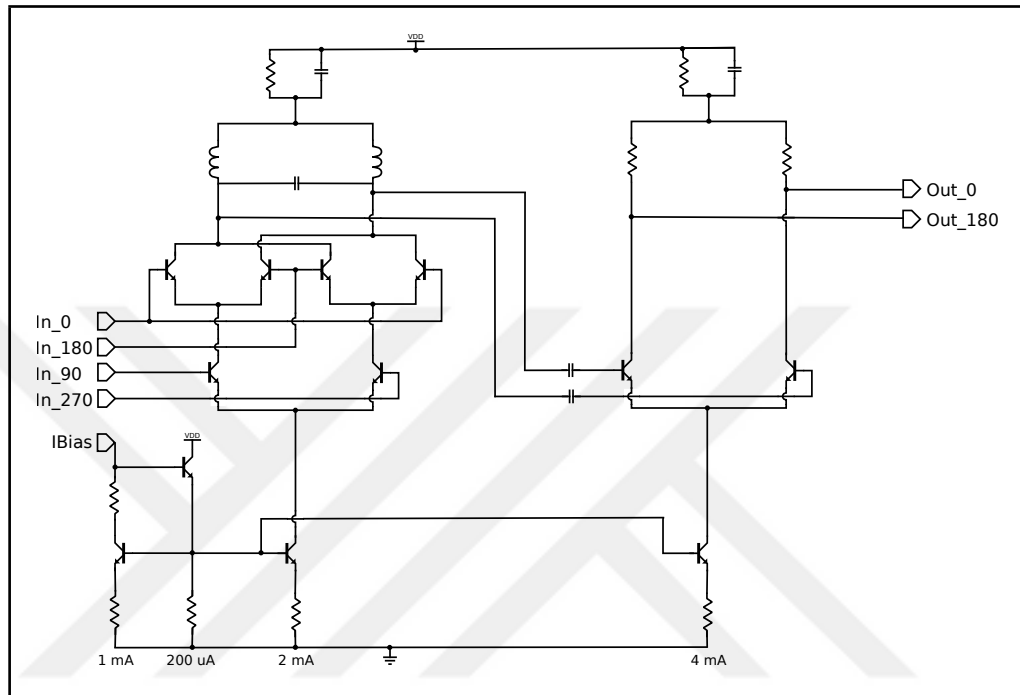
Figure 3.16: Third frequency doubler.

Firstly, frequency doubler core is loaded with resistor in the previous version. It is replaced with a LC tank. LC tanks or LC resonant circuits can be treated as bandpass filters. They have high impedance at their resonant frequency and low impedance at out of the band. Their bandwidth is directly proportional to the Quality factor(Q) of inductor. Resonant frequency of LC tanks is as follow.

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

where f_o is the resonant frequency, L is the inductor value and C is the capacitor value. Resonant frequency is directly related to the inductor value and the capacitor value. Thus the process variation in capacitor absolute value can be as high as $\pm 10\%$, the

variation at resonant frequency will be unacceptable. The variation at the resonant frequency caused by process variation is given in Fig 3.17. As seen in figure, the capacitor absolute value variation results in almost 1 GHz variation at resonant variation.
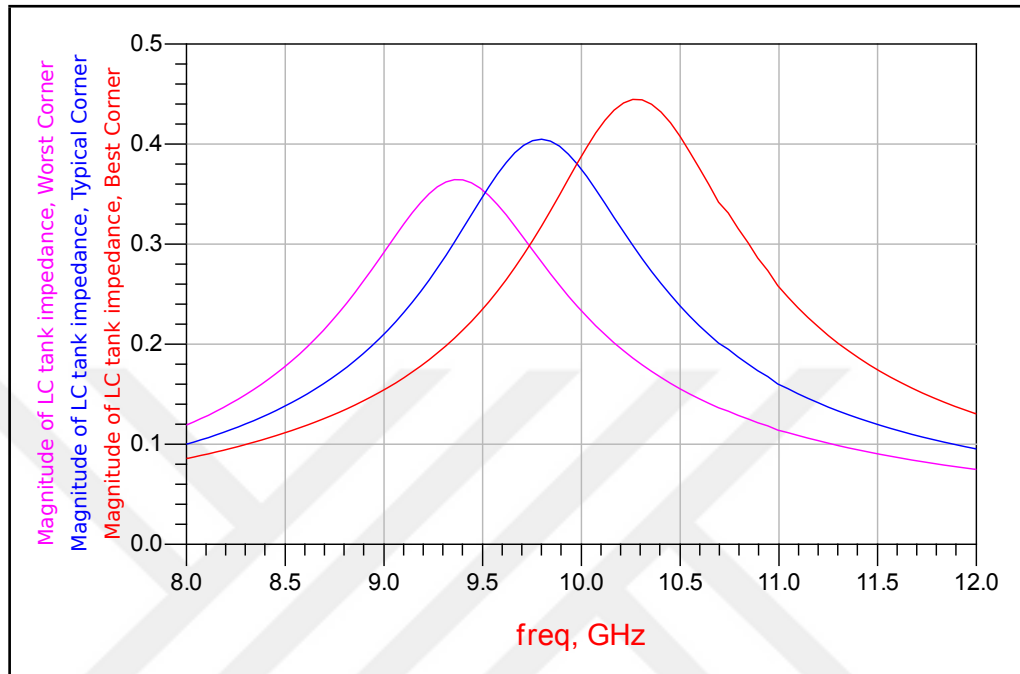
Figure 3.17: Variation of LC tank resonant frequency by process corners.

In order to compensate the variation of the capacitor value, tunable LC tank with variable capacitor is deployed in the third frequency multiplier. Variable capacitor design is given in Fig 3.18. Ctune1 and Ctune2 can be set individually via a switch located on the PCB. LC tank was designed by considering layout parasitics.
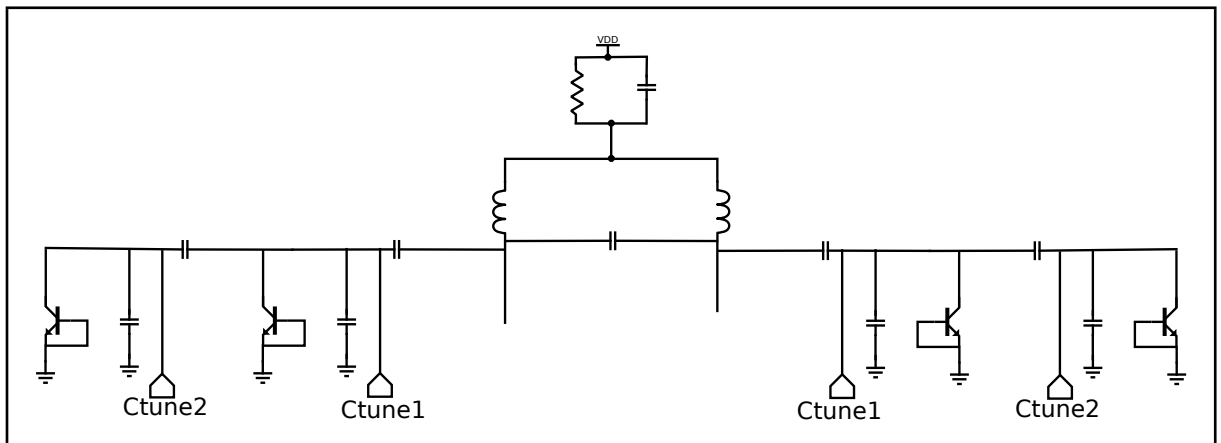
Figure 3.18: Third frequency doubler's LC tank with variable capacitor.

In Fig 3.19, Fig 3.20 and Fig 3.21, magnitude of LC tank impedance is plotted for four different switch(Ctune1 and Ctune2) configuration for three process corners. As seen from these plots, magnitude of LC tank impedance can be set 0.3 at around 9.5 GHz by choosing proper switch configuration for all process corners.
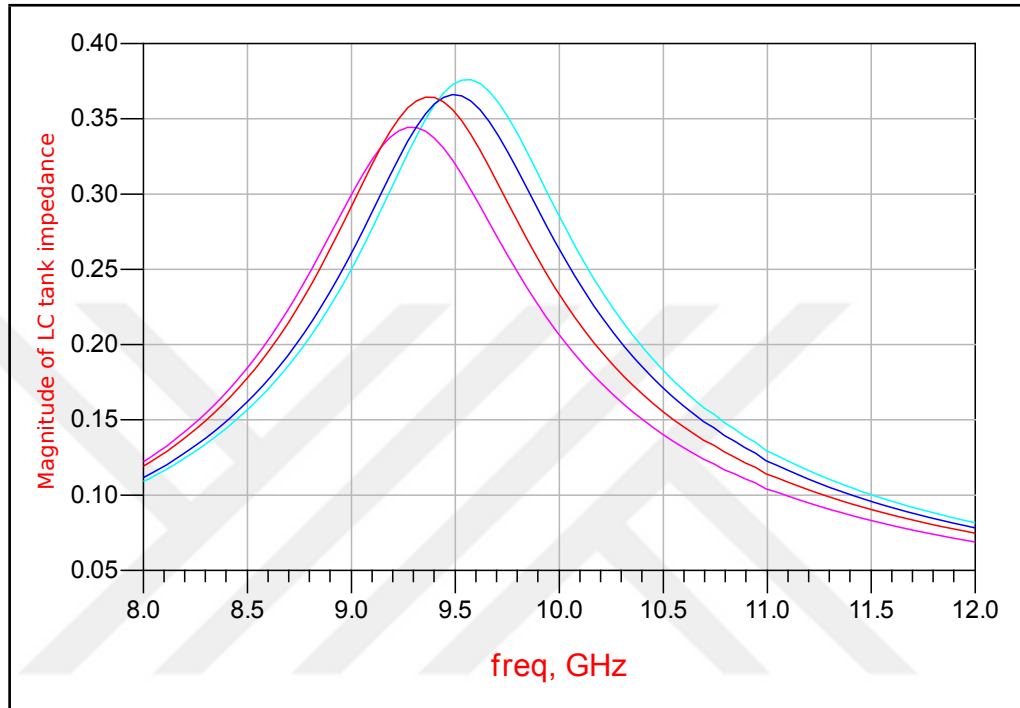
Figure 3.19: Variation of LC tank resonant frequency by four different switch configuration for typical corner.
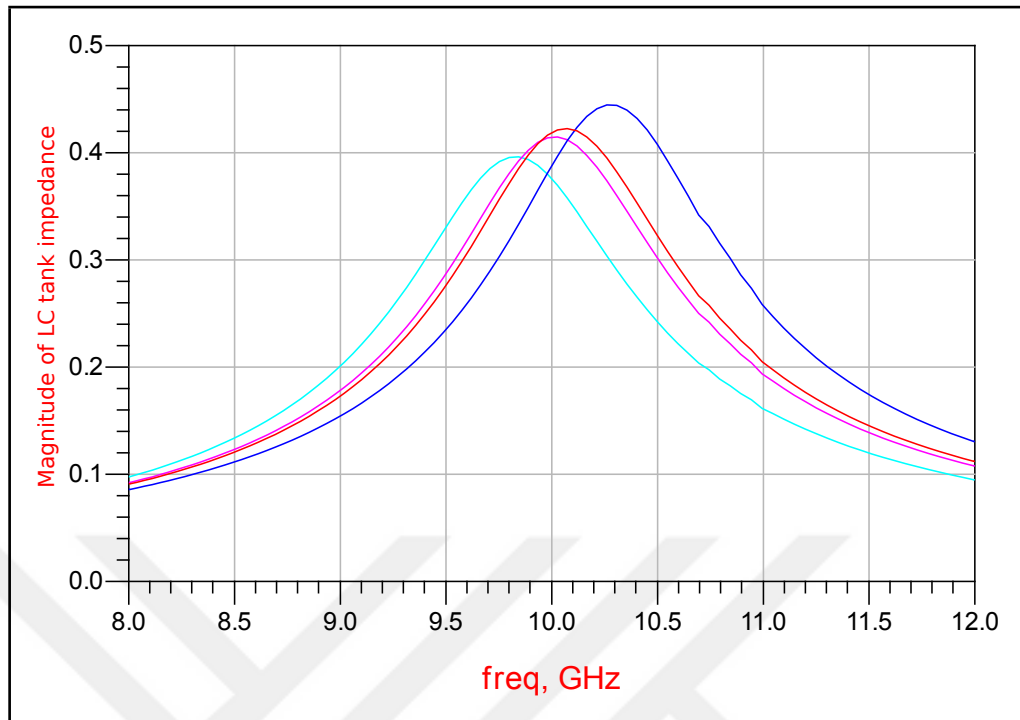
Figure 3.20: Variation of LC tank resonant frequency by four different switch configuration for best corner.
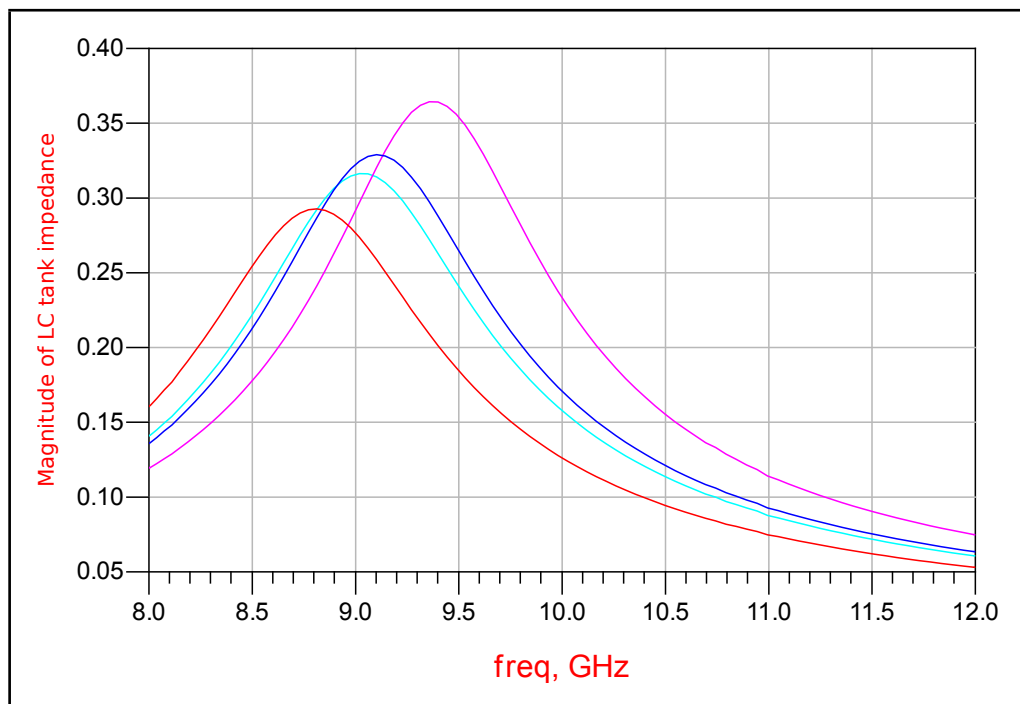
Figure 3.21: Variation of LC tank resonant frequency by four different switch configuration for worst corner.

In order to reduce the oscillation tendency, emitter followers at the output are replaced with differential pair gain stage. In Fig 3.22, third frequency doubler output is plotted for 5 dBm input power and -50 mV VGA control voltage and in Fig 3.23, third frequency doubler output was plotted for -10 dBm input power and -50 mV VGA control voltage. Notice that output power is almost the same for the two different input power in both plots. Secondly, harmonics are filtered out by LC tank. There is a significant difference between this plot and Fig 3.12 in terms of harmonic contents
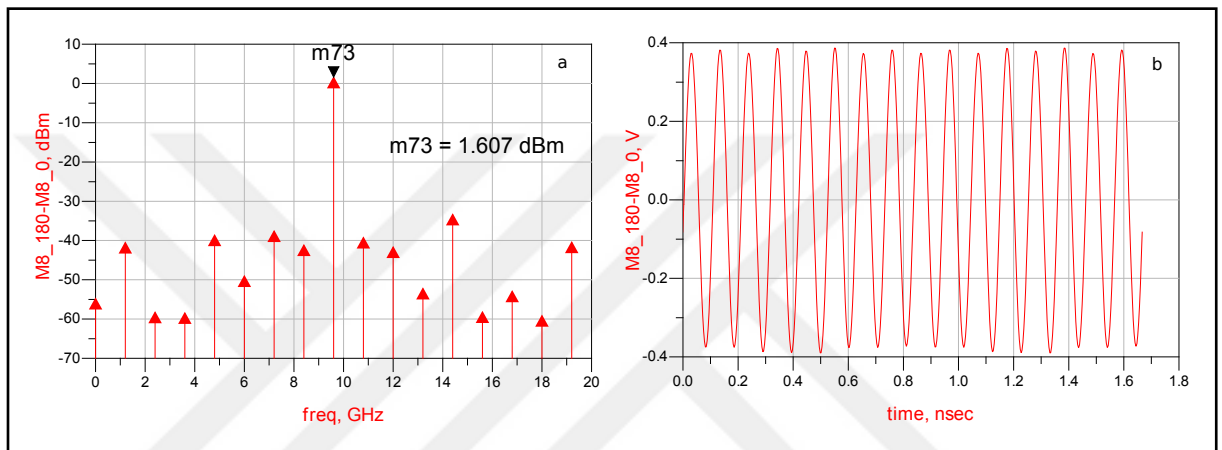
Figure 3.22: Third frequency multiplier output power for 5 dBm input power and -50 mV VGA control voltage(Vcon)
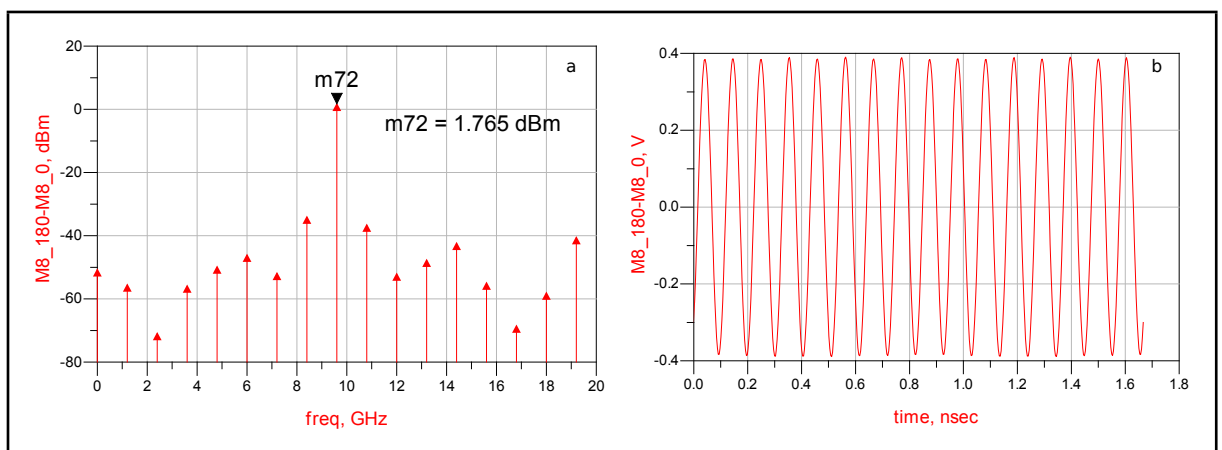
Figure 3.23: Third frequency multiplier output power for -10 dBm input power and -50 mV VGA control voltage(Vcon)

3.3. NEW BLOCKS

3.3.1. Differential Signal to Single Ended Signal Converter

In order to convert the differential signal to single ended signals, totem-pole pushpull topology is used. Schematic drawing is given in Fig 3.24. Two matched transistors are used at the output stage. Positive cycles of input signals conducted by emitter follower and negative cycles of the input signal conducted by common emitter part of the circuit.
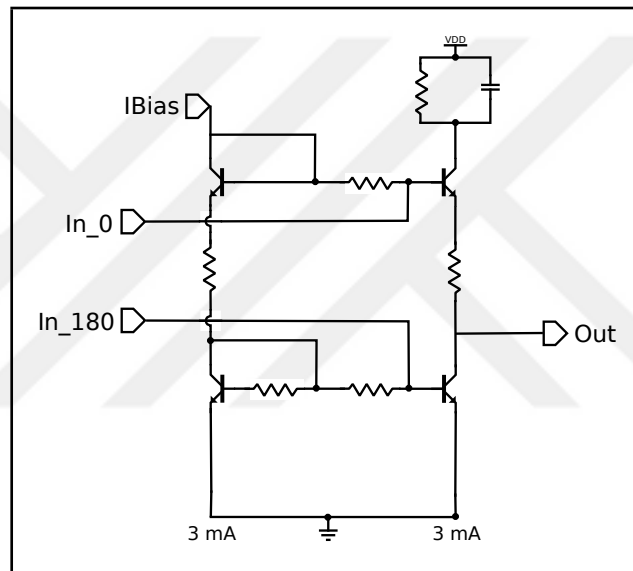
Figure 3.24: Differential to single ended converter.

Ideally, In_0 and In_180 input signals are perfectly out of phase by 180°. And the outputs of emitter follower and common emitter are also out of phase by 180°. Thus the combination of these stages firstly rectifies the input signal and then sums them. Mismatch at the phase of emitter follower and common emitter stage can cause increase in harmonic contents. Phase and gain of emitter follower and common emitter was simulated by AC analysis and it is plotted in Fig 3.25. Phase mismatch of emitter follower is 2.360^o and phase mismatch of common emitter is 5.460^o. Gain of emitter follower is almost 0 dB and gain of common emitter is 1.173 dB.

In Fig 3.26, output of differential to single ended converter (D2S) is plotted for 5 dBm input power and -50 mV VGA control voltage. Insertion loss of D2S is about 1.5 dB.
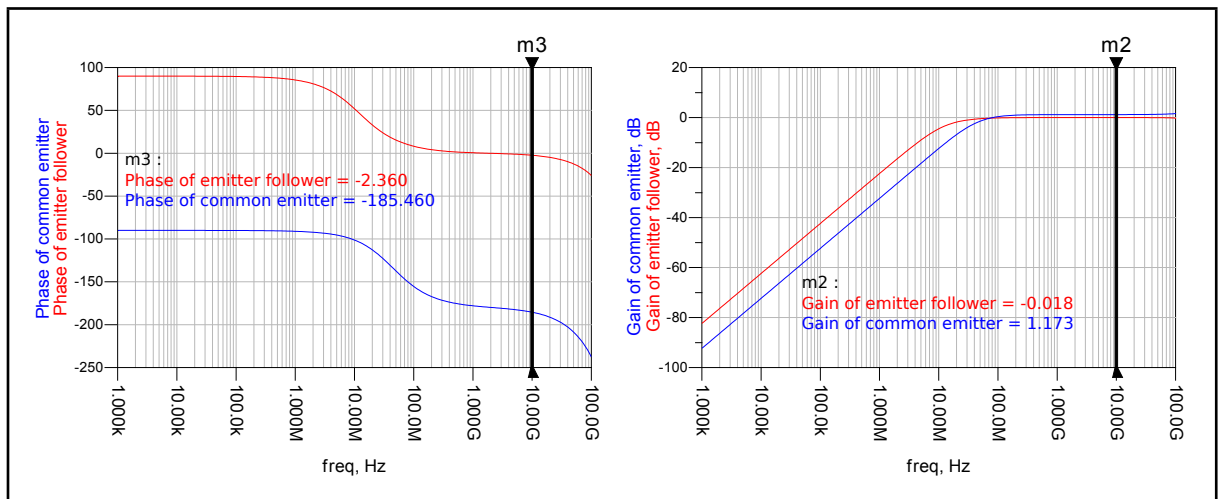
Figure 3.25: Small Signal characteristic of emitter follower and common emitter

Due to the characteristic of differential ended signalling even numbered harmonics are subtracted from each other. From this point of circuits, all signals are single ended, thus even numbered harmonics will be higher. This behaviour can be observed in Fig 3.26 marker m74.
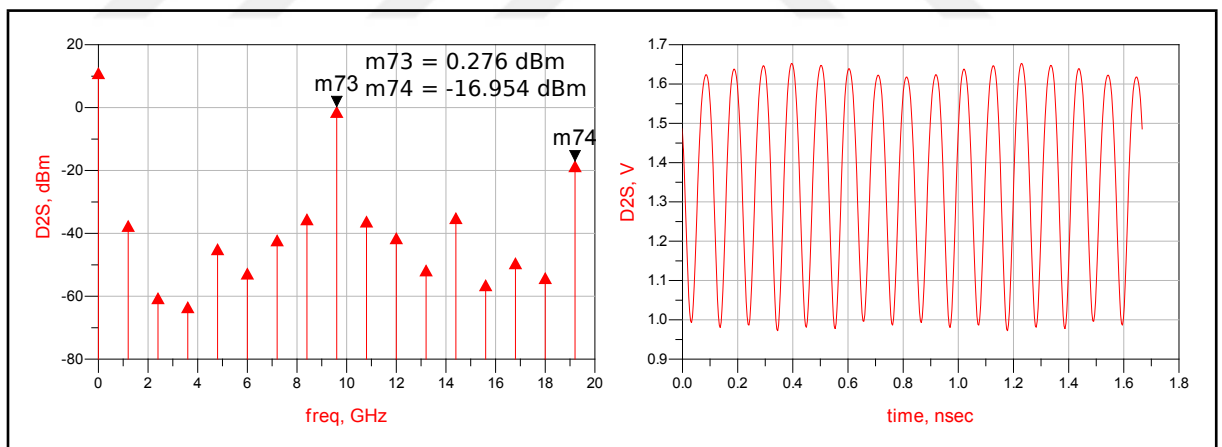
Figure 3.26: Output of differential to single ended converter

3.3.2. Power Amplifier and Output Matching

For additional gain, power amplifier given in Fig 3.27 is designed. T2 transistor marked in figure is cascode transistor with high breakdown voltage. There is a trade-off between transistor's breakdown voltage and f_T. Since T2 transistor can be considered non-switching transistor, it does not need to have high f_T. Same variable capacitor given

in Fig 3.18 is also deployed in this stage.
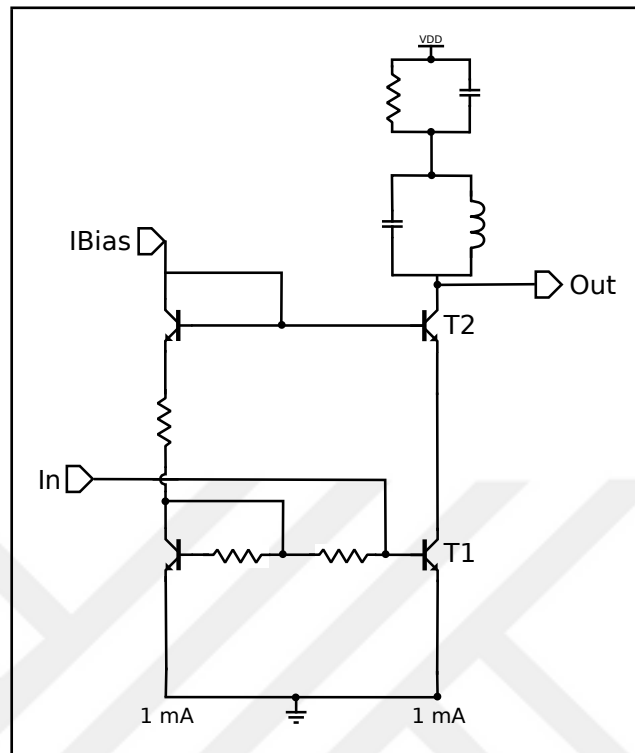
Figure 3.27: Power amplifier.

In Fig 3.28, output of power amplifier (PA) is plotted for 5 dBm input power and -50 mV VGA control voltage. Gain of amplifier is about 3 dB.
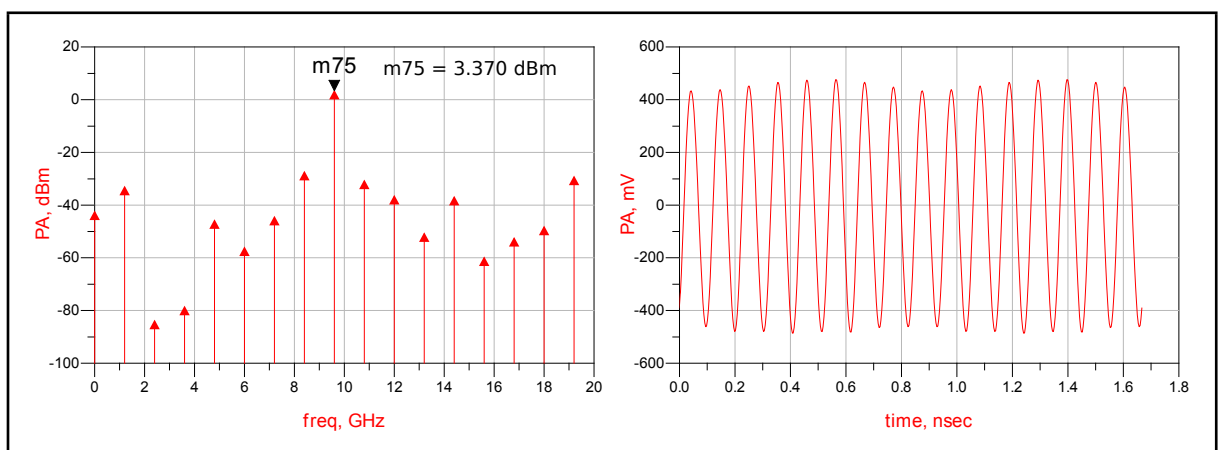
Figure 3.28: Output of power amplifier

Since power amplifier is the last stage, there is an additional specification. Output return loss should be better than 10 dB. Since parasitics at the output paths may effect

return loss, output path was co-designed with power amplifier. Output path, which is given in Fig 3.29, was simulated with Agilent Momentum 3D planar electromagnetic (EM) simulator. Output return loss is plotted in Fig 3.30. As seen from this figure, output return loss satisfies the target specifications.
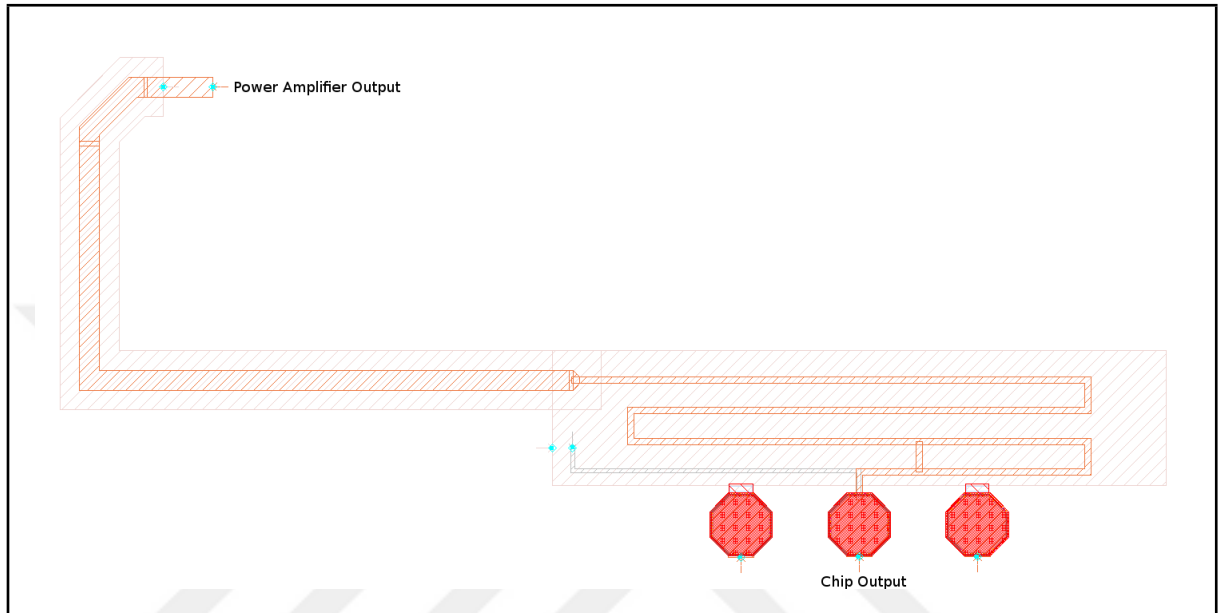
Figure 3.29: Output path.
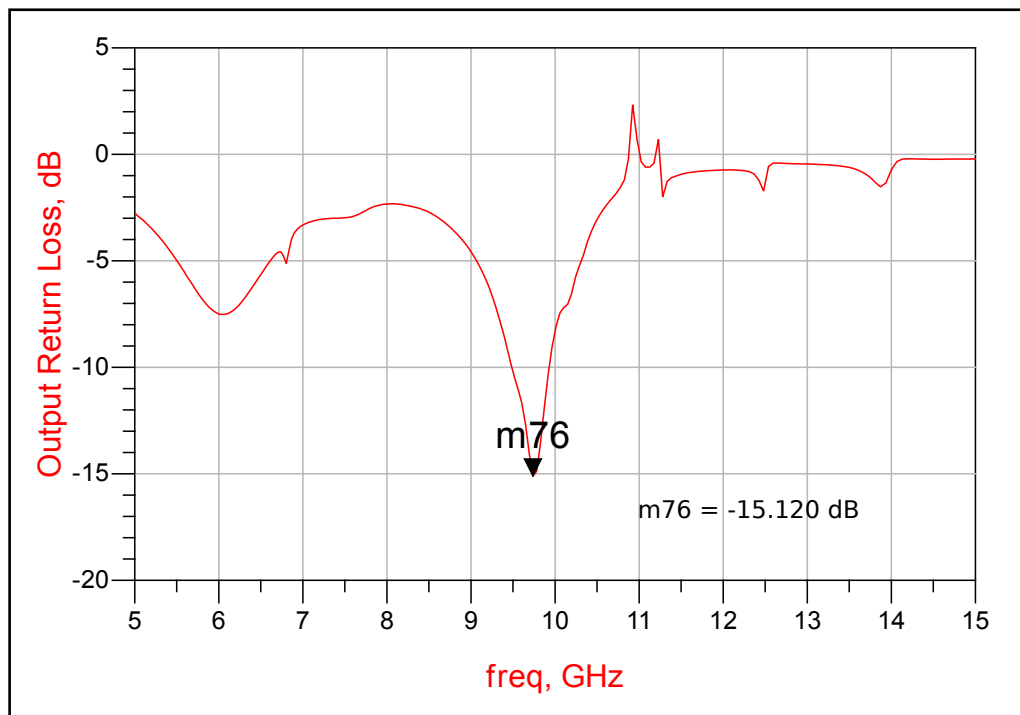
Figure 3.30: Output return loss

In Fig 3.31, output of M8X phase 2 is plotted for 5 dBm input power and -50 mV VGA control voltage. Output power is 3.369 dBm and harmonic level is 28 dBc. In Fig 3.32, output of M8X phase 2 is plotted for 5 dBm input power and -90 mV VGA control voltage. Output power is -0.303 dBm and harmonic level is 30 dBc. In Fig 3.33, output of M8X phase 2 is plotted for -10 dBm input power and -85 mV VGA control voltage. Output power is 0.468 dBm and harmonic level is 29 dBc. As seen from these figures, output power can be set around 0 dBm by setting VGA control voltage and harmonic level is about 29 dBc.
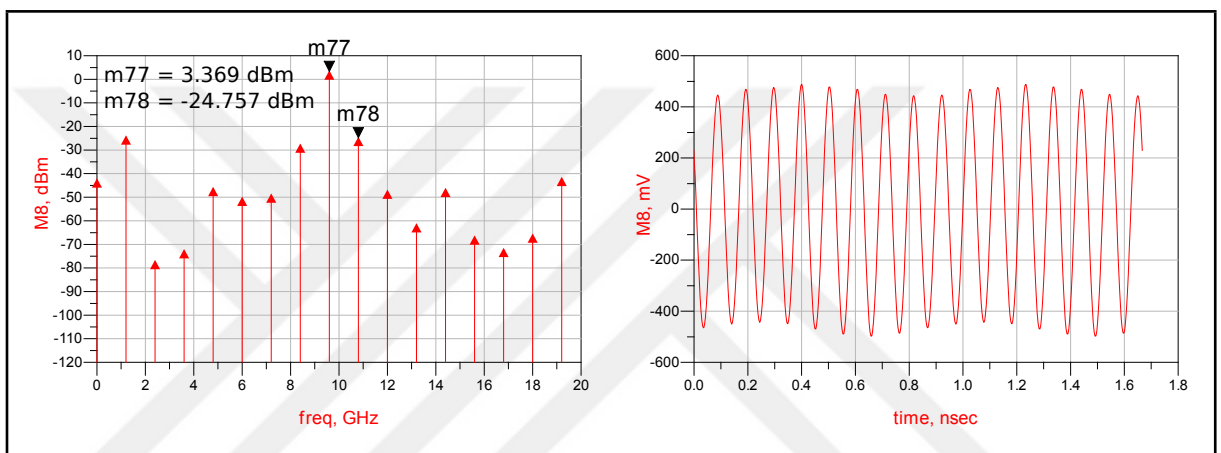
Figure 3.31: Output of M8X phase 2 for 5 dBm input power and -50 mV VGA control voltage.
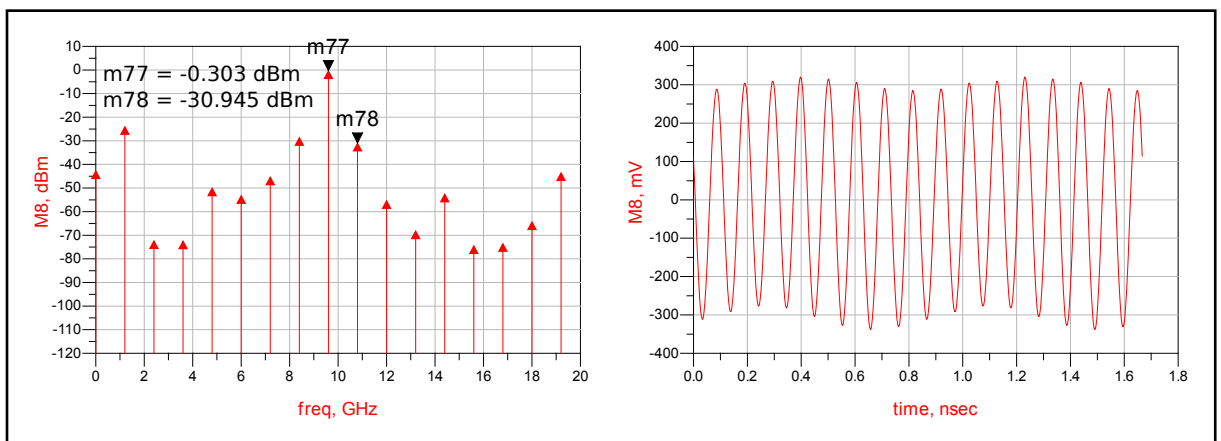
Figure 3.32: Output of M8X phase 2 for 5 dBm input power and -90 mV VGA control voltage.

In Fig 3.34, SSB phase noise of input signal and SSB phase noise of M8X phase 2 is given. In figure output SSB phase noise is -130.197 dBc/Hz which is satisfies the target
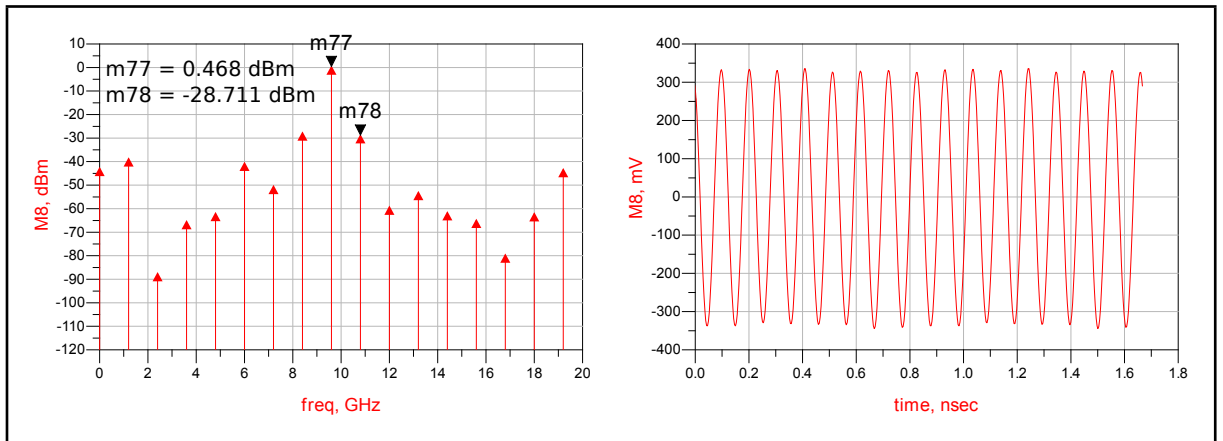
Figure 3.33: Output of M8X phase 2 for -10 dBm input power and -85 mV VGA control voltage.

specifications.
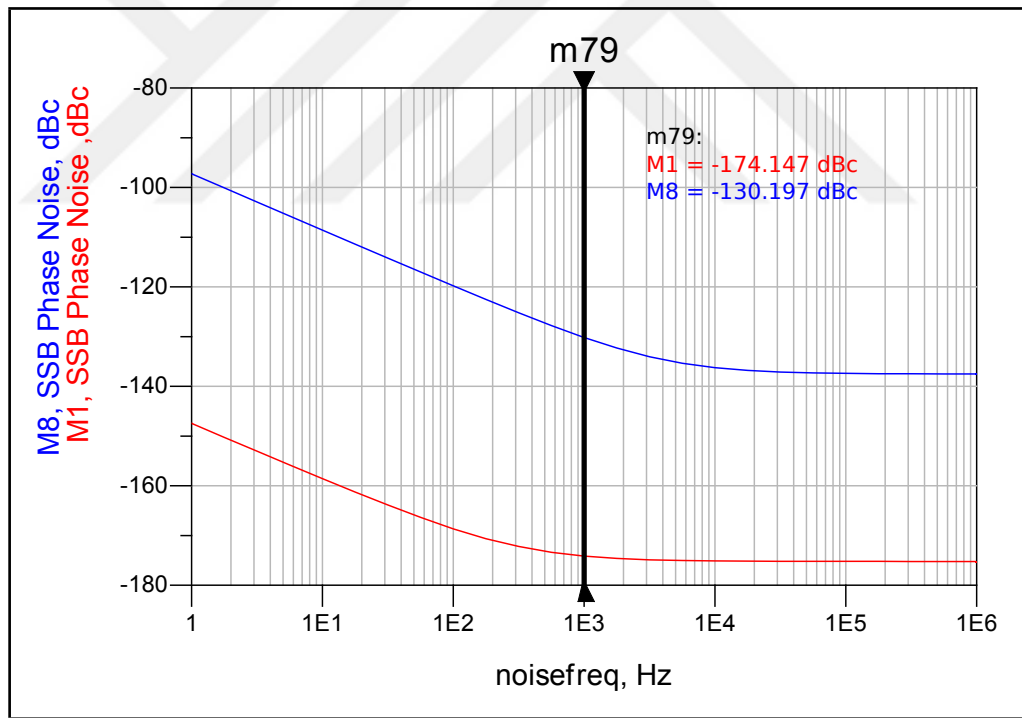
Figure 3.34: Phase noise of M8X phase 2's input and output signal.

In Table 3.1, the variation of output power of M8X phase 2 is given by input power and VGA control voltage for typical process corner. For all input power, output power can be set around 0 dBm by setting VGA control voltage. In Fig 3.35, the variation of single side band phase noise at 1 kHz offset is given by input power and VGA control voltage for typical process corner. Targeted SSB phase noise can be satisfied for 5 dBm

and 0 dBm input power.

Table 3.1: M8X phase 2 output power (dBm) vs input power and VGA control
voltage for typical process corner

	Input Power				
	-15 dBm	-10 dBm	-5 dBm	0 dBm	5 dBm
Vcon = -100 mV	-7.205	-2.336	-2.448	-2.341	-2.306
Vcon = -95 mV	-5.452	-1.263	-1.394	-1.295	-1.255
Vcon = -90 mV	-3.961	-0.356	-0.507	-0.410	-0.363
Vcon = -85 mV	-2.709	0.413	0.245	0.341	0.395
Vcon = -80 mV	-1.664	1.068	0.884	0.978	1.040
Vcon = -75 mV	-0.791	1.622	1.428	1.518	1.588
Vcon = -70 mV	-0.059	2.090	1.891	1.974	2.050
Vcon = -65 mV	0.555	2.482	2.281	2.355	2.434
Vcon = -60 mV	1.071	2.803	2.607	2.665	2.741
Vcon = -55 mV	1.505	3.055	2.873	2.910	2.981
Vcon = -50 mV	1.868	3.243	3.086	3.101	3.167

In Table 3.2, the variation of output power of M8X phase 2 is given by input power
and VGA control voltage for typical process corner. For all input power, output power
can be set around 0 dBm by setting VGA control voltage.

In Table 3.3, the variation of output power of M8X phase 2 is given by input power and
VGA control voltage for typical process corner. For -15 dBm input power, maximum
output power is about -9.9 dBm and input power higher than -10 dBm, maximum
output power is around -0.7 dBm. In terms of output power specification, M8X phase
2 does not satisfy the targeted specifications. In Fig 3.36, the variation of single side
band phase noise at 1 kHz offset is given by input power and VGA control voltage for
worst process corner. Targeted SSB phase noise can be satisfied only for 5 dBm input
power.
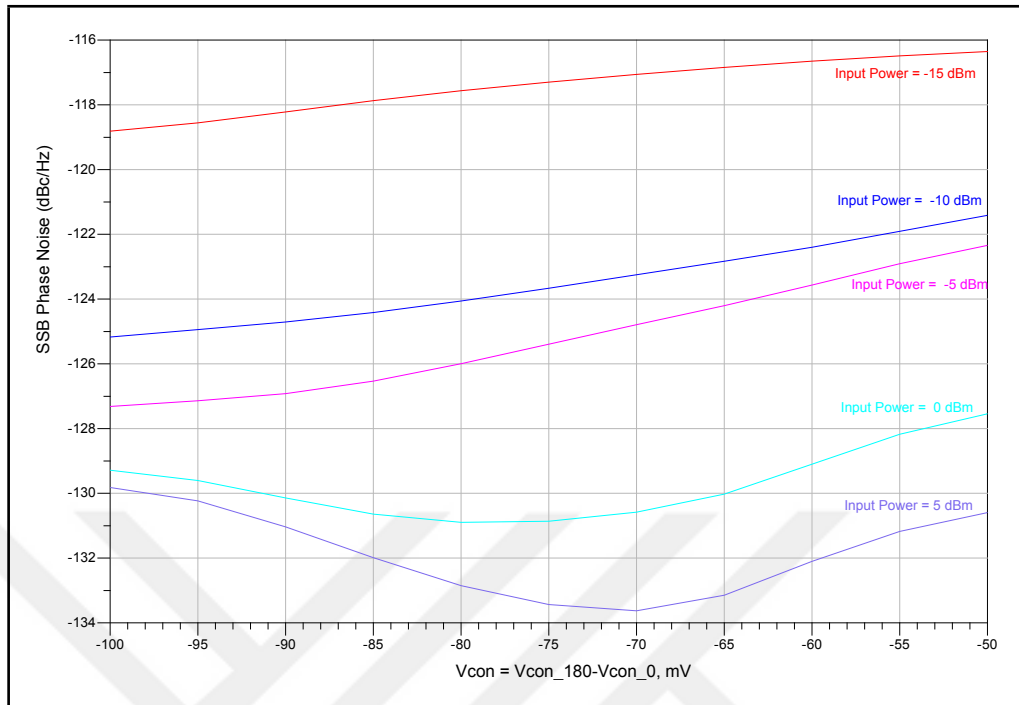
Figure 3.35: M8X phase 2 SSB phase noise (dBc/Hz) vs input power and VGA control voltage for typical process corner.

Table 3.2: M8X phase 2 output power (dBm) vs input power and VGA control voltage for best process corner

	Input Power				
	-15 dBm	-10 dBm	-5 dBm	0 dBm	5 dBm
Vcon = -120 mV	-9.873	-9.058	-8.517	-8.516	-8.809
Vcon = -110 mV	-3.307	-2.734	-2.486	-2.597	-2.998
Vcon = -100 mV	0.393	0.508	0.604	0.463	0.308
Vcon = -90 mV	1.738	1.637	1.964	1.853	1.460
Vcon = -80 mV	2.506	2.189	2.539	2.551	2.325
Vcon = -70 mV	2.411	2.325	2.445	2.472	2.332
Vcon = -60 mV	2.439	2.410	2.473	2.499	2.377
Vcon = -50 mV	2.471	2.446	2.503	2.528	2.417

Table 3.3: M8X phase 2 output power (dBm) vs input power and VGA control voltage for worst process corner

	Input Power				
	-15 dBm	-10 dBm	-5 dBm	0 dBm	5 dBm
Vcon = -50 mV	-24.472	-4.536	-3.984	-4.217	-4.318
Vcon = -22 mV	-22.091	-3.151	-2.705	-2.885	-2.971
Vcon = 5 mV	-20.305	-2.327	-1.964	-2.093	-2.165
Vcon = 33 mV	-18.651	-1.753	-1.488	-1.564	-1.617
Vcon = 61 mV	-16.818	-1.319	-1.165	-1.192	-1.222
Vcon = 89 mV	-14.579	-1.017	-0.956	-0.946	-0.957
Vcon = 117 mV	-12.154	-0.832	-0.830	-0.799	-0.797
Vcon = 144 mV	-10.541	-0.728	-0.758	-0.716	-0.707
Vcon = 172 mV	-10.007	-0.679	-0.723	-0.677	-0.663
Vcon = 200 mV	-9.901	-0.665	-0.711	-0.665	-0.649
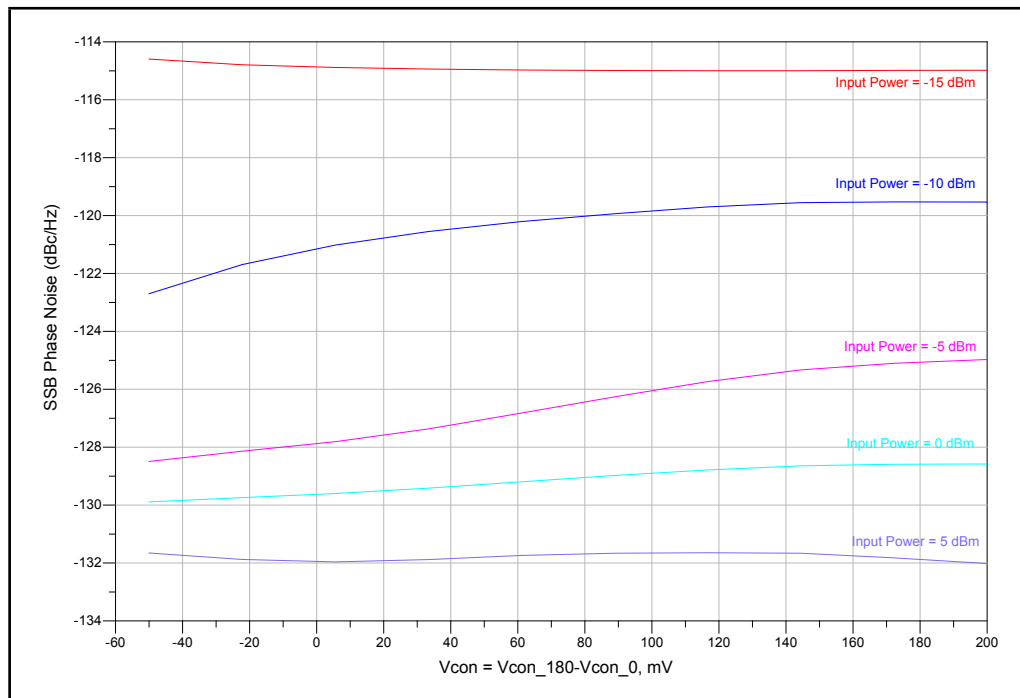
Figure 3.36: M8X phase 2 SSB phase noise (dBc/Hz) vs input power and VGA control voltage for worst process corner.

3.3.3. Peak Detector and On-Chip Reference Generator

In order to convert output power of frequency multiplier to DC signal, peak detector given in Fig 3.37 is designed. In peak detector design, Schottky diode was used. While regular diodes have a voltage drop about 0.6-0.7 V, Schottky diodes have a voltage drop at about 0.3-0.4 V. This will provide higher peak detector gain and input sensitivity. In Fig 3.38, transient settling behaviour of the peak detector is given for different input powers for typical process corner. In Table 3.4, peak detector output is given for different input powers and process corners.
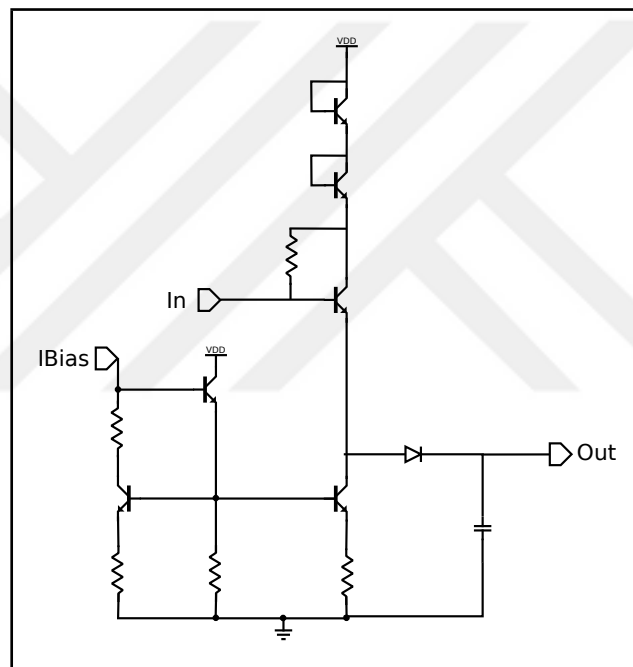
Figure 3.37: Peak detector
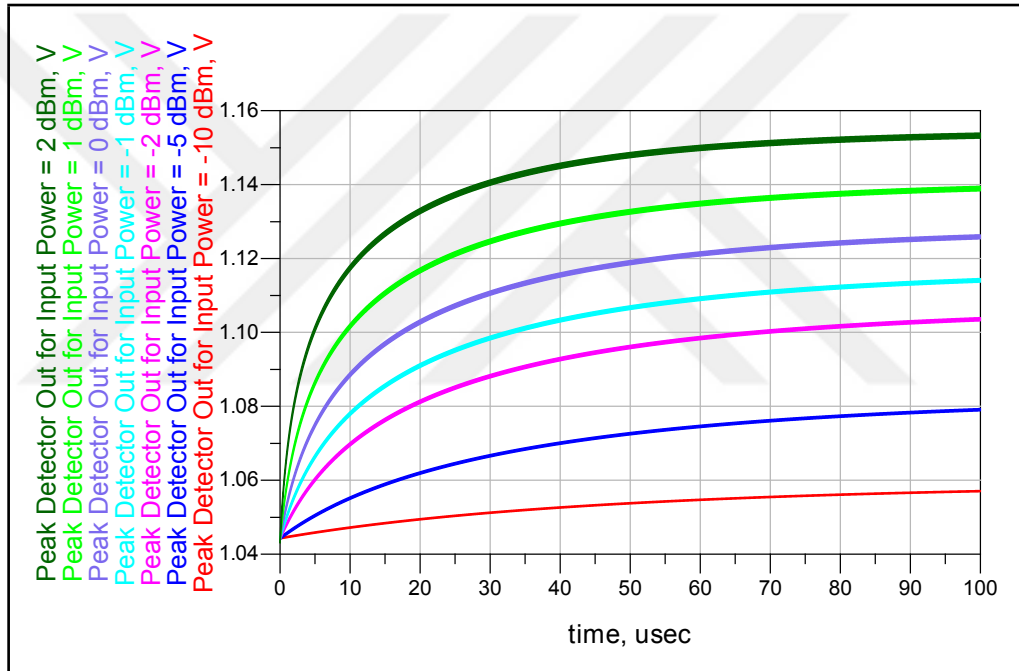
Figure 3.38: Peak detector output for various input powers

Table 3.4: Peak detector, on-chip reference generator output and their difference for different input powers and process corners

Input Power	Worst Process Corner			Typical Process Corner			Best Process Corner		
	Peak Detector Out	Reference Out	Difference	Peak Detector Out	Reference Out	Difference	Peak Detector Out	Reference Out	Difference
-10 dBm	0.828 V	1.213 V	0.385 V	1.057 V	1.392 V	0.335 V	1.090 V	1.414 V	0.324 V
-5 dBm	0.850 V	1.213 V	0.363 V	1.079 V	1.392 V	0.313 V	1.097 V	1.414 V	0.317 V
-2 dBm	0.875 V	1.213 V	0.338 V	1.103 V	1.392 V	0.289 V	1.110 V	1.414 V	0.304 V
-1 dBm	0.885 V	1.213 V	0.328 V	1.114 V	1.392 V	0.278 V	1.117 V	1.414 V	0.297 V
0 dBm	0.897 V	1.213 V	0.316 V	1.126 V	1.392 V	0.266 V	1.128 V	1.414 V	0.286 V
1 dBm	0.910 V	1.213 V	0.303 V	1.139 V	1.392 V	0.253 V	1.137 V	1.414 V	0.277 V
2 dBm	0.925 V	1.213 V	0.288 V	1.154 V	1.392 V	0.239 V	1.156 V	1.414 V	0.258

As seen from the table, peak detector output is purely related with process corner. For 0 dBm input power, peak detector output can vary from 1.128 V to 0.897 V. Since the output power will be determined by observing the peak detector output, it will cause an error term. Thus in order to reduce this error, an on-chip reference is designed. The on-chip reference generator uses a copy of the peak detector at the output. Input of peak detector is generated from the input of M8X. Since the input power may change between -10 dBm and 5 dBm, buffer given in Fig 3.39 is designed and placed before the reference peak detector. By considering the worst (slowest) process corners, peak detector reference buffer designed as seven stage. Output swing magnitude can be set by "SwingRef" input. In future phases, the output of the peak detector will be subtracted from the on-chip reference generator. Then the decision of the VGA control voltage will be given based on this result. The output of the peak detector, the output of the on-chip reference generator and their difference is given in Table 3.4 for three process corners. As seen from the table, while peak detector output variation is about 0.231 V for process corners, peak detector and on-chip reference generator output difference is as low as 30 mV. If desired, this variation can also be compensated by tuning "SwingRef" input of the on-chip reference generator.
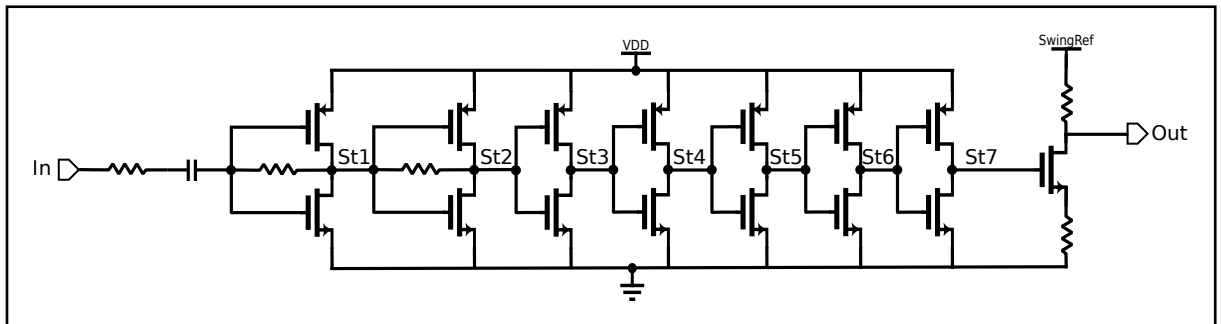
Figure 3.39: Peak detector reference buffer

3.3.4. Digital to Analog Converter - DAC

In order to generate VGA control voltages, digital to analog converter (DAC) given in Fig 3.40 was designed. It is simply a binary weighted DAC. Its least significant bit and output range can be set outside the chip via IBias input. For 7 uA nominal IBias current, its least significant bit is 3.5 mV and its output range is 224 mV. Its output characteristic is given in Fig 3.41.
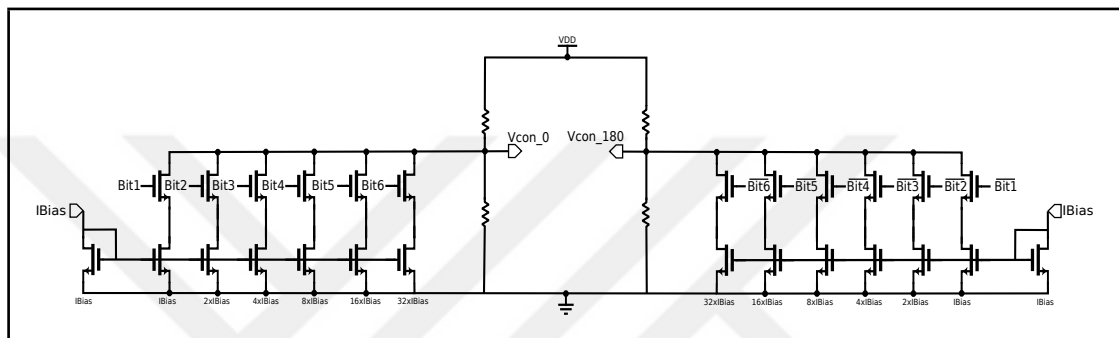
Figure 3.40: Digital to analog converter - DAC
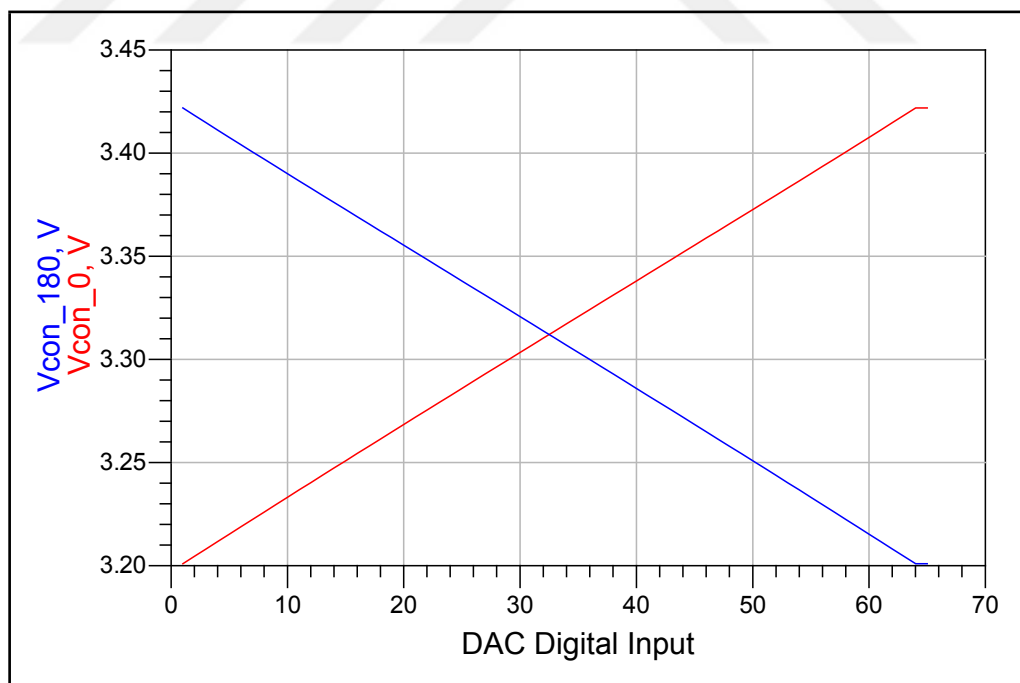
Figure 3.41: VGA control DAC output characteristic

3.3.5. Bias Current Generation

1 mA bias current of each stage is generated from 1.2 V voltage reference which can be set outside the chip. 1.2 V voltage reference will be generated by the bandgap voltage reference in future phases. Designed bias current generator is given in Fig 3.42. 1.2 V voltage reference is converted to current by "R1" resistor. Then it is distributed to other stages by using current mirrors. One of the current mirror outputs can be observed from outside the chip to measure bias current.
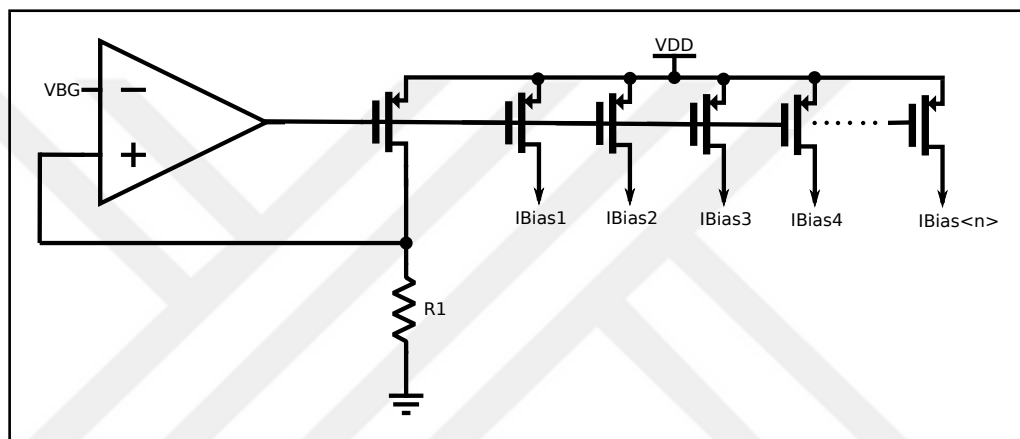
Figure 3.42: Bias current generation

3.4. M8X PHASE 2 LAYOUT

After the completion of electrical design and simulation of the M8X phase 2, physical design is done in Cadence Layout Editor. For DRC and LVS verification, Assura toolset is used. Final layout is given in Fig. 3.43 and input/output descriptions are listed in Table 3.5. Final M8X phase 2 die dimesion is 2.34 mm by 2.44 mm.
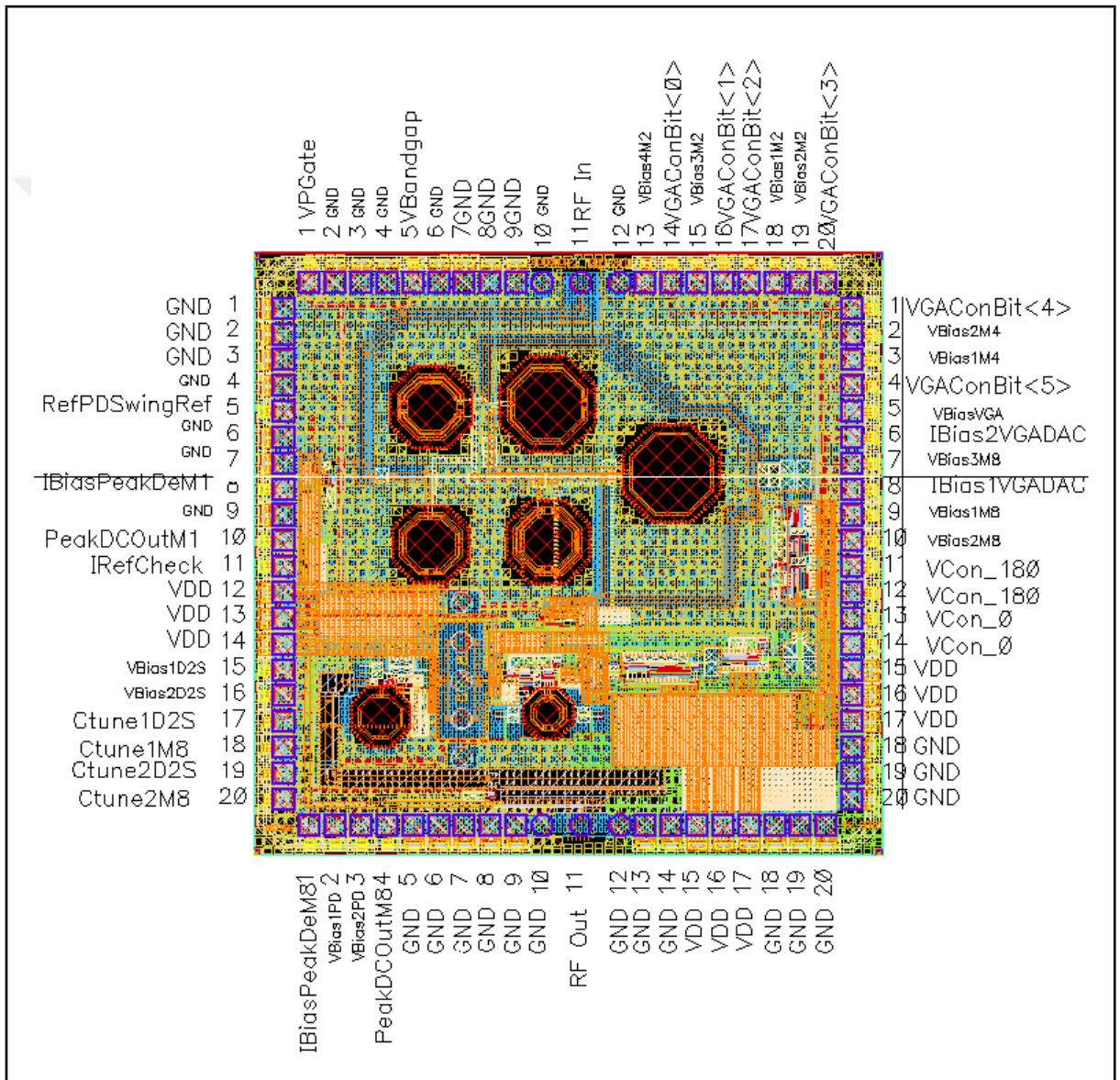
Figure 3.43: M8X phase 2 Layout

Table 3.5: M8X phase 2 input and output descriptions

Name	Nominal Value	Description
VDD	4 V	Positive power supply
GND	0 V	Positive power supply reference
RF In	-	Input signal
RF Out	-	Output signal
VPGate	-	Bias current generation opamp output
VBandgap	1.2 V	Bias current generation voltage reference
VGAConBit<5:0>	-	VGA control DAC digital input
Vcon_180, Vcon_0	-	VGA control voltage
VBias*M*	-	Observation outputs for biasing voltage
IBias1VGADAC, IBias2VGADAC	7 uA	VGA control DAC biasing current
PeakDCOutM8	-	Peak detector DC output
PeakDCOutM1	-	Reference peak detector DC output
Ctune1D2S, Ctune2D2S, Ctune1M8, Ctune2M8	-	LC tank variable capacitor control voltage
IRefCheck	1 mA	Bias current generation output observation current
RFPDSwingRef	-	Reference peak detector buffer swing reference

3.5. M8X PHASE 2 PACKAGING

Parasitic capacitance of the package and bonding wire inductance has negative effects on performance in terms of output power and output return loss. Thus QFN32 package was chosen due to its low parasitic capacitance and inductance values. Bonding plan is given in Fig 3.44 and its photomicrograph is given in Fig 3.45.
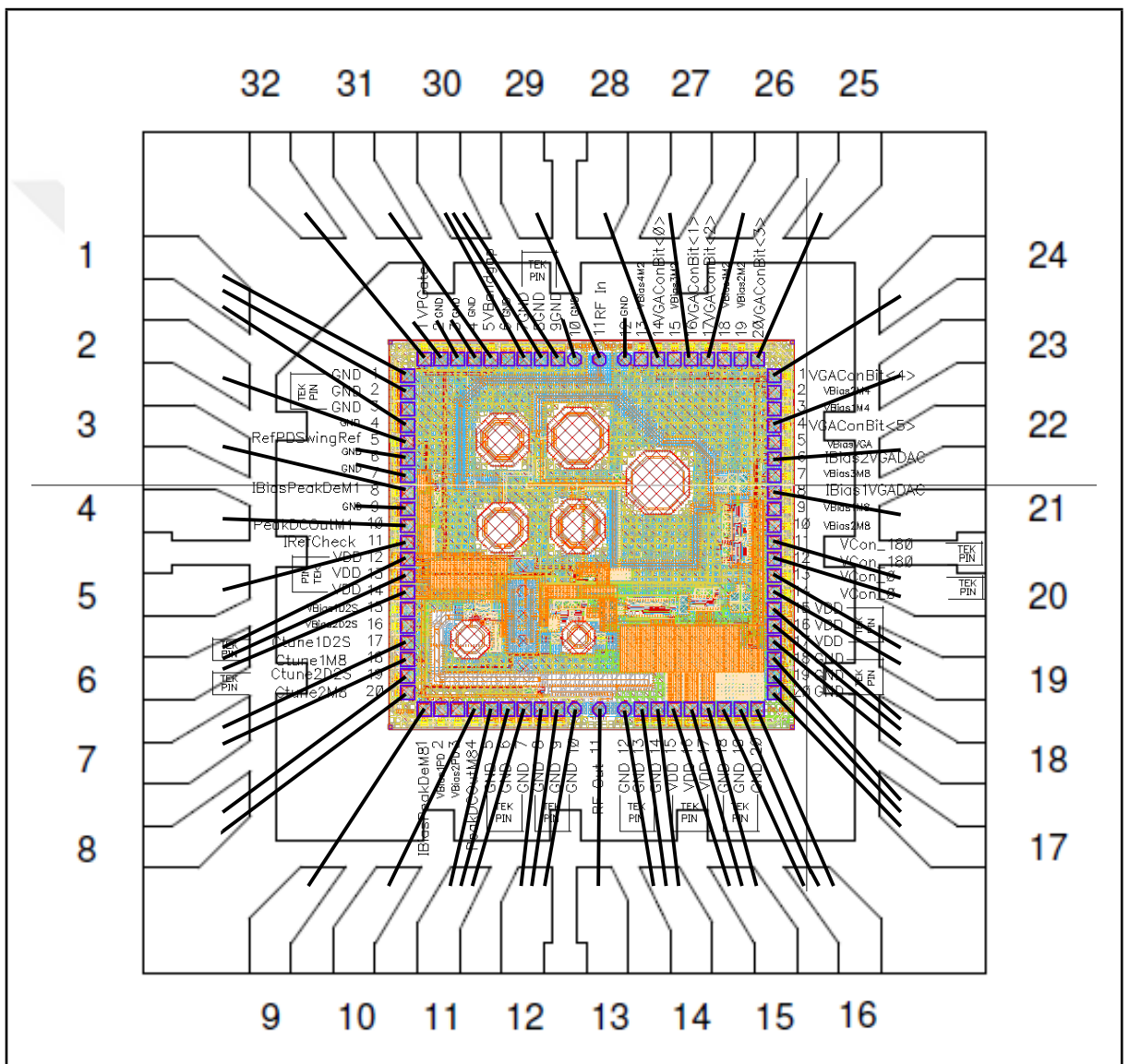
Figure 3.44: M8X phase 2 bonding plan
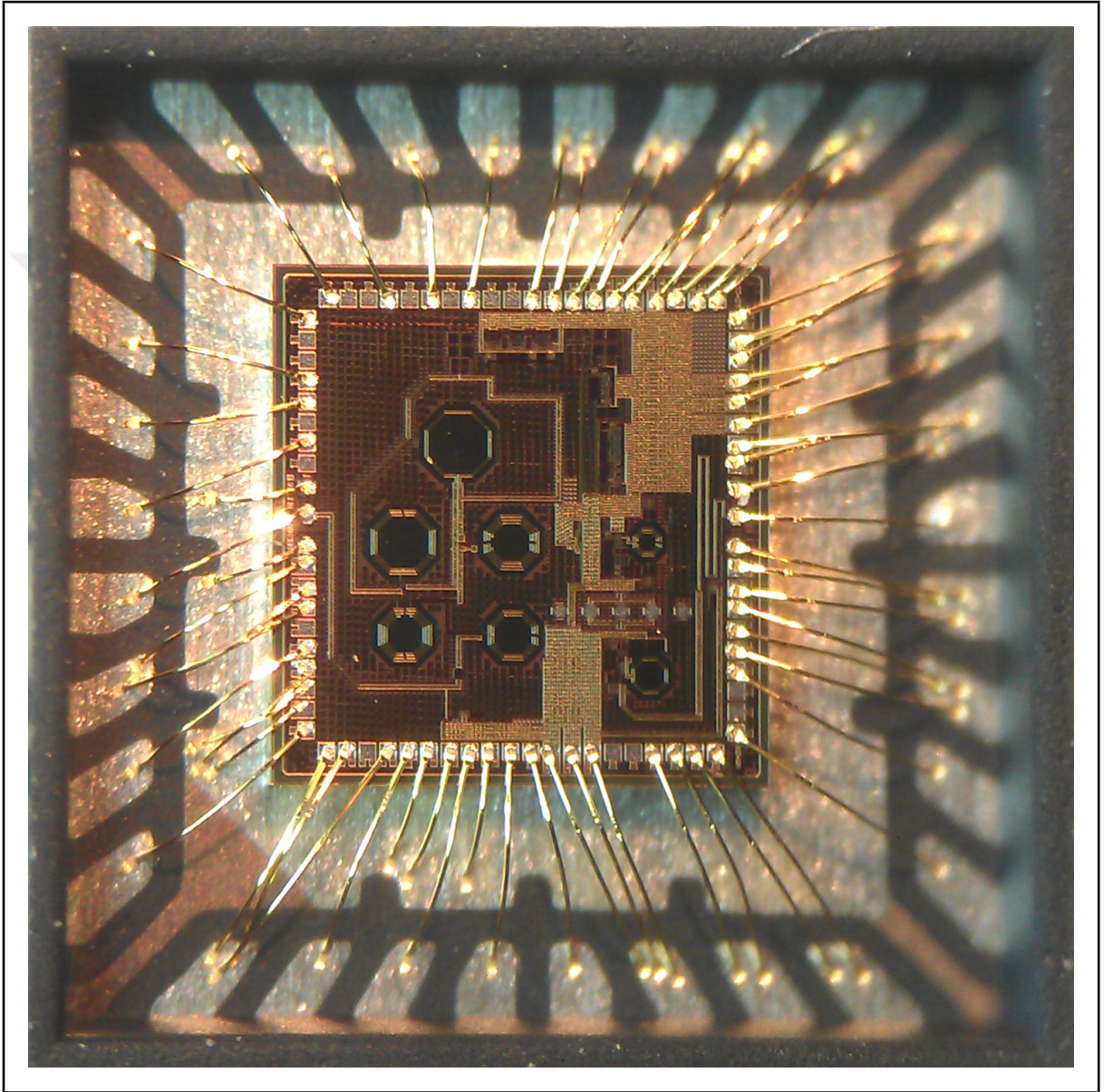
Figure 3.45: M8X phase 2 bonding plan photomicrograph

3.6. M8X PHASE 2 TEST BOARD DESIGN

For testing of M8X Phase 2, the PCB given in Fig 3.46 is designed. As mentioned in section 3.3.2, output of the M8X phase 2 die matches to 50 Ω and its output return loss is given in Fig 3.30. After addition of bond-wire and package model given in Fig 3.47, output return loss can be seen in Fig 3.48.
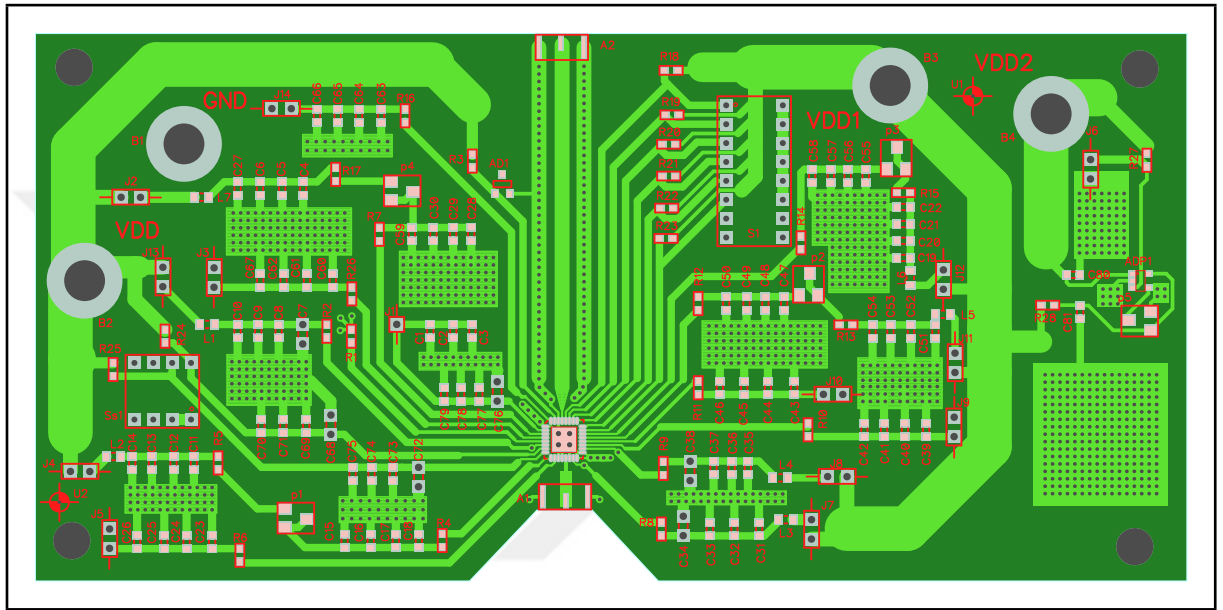
Figure 3.46: M8X phase 2 test board
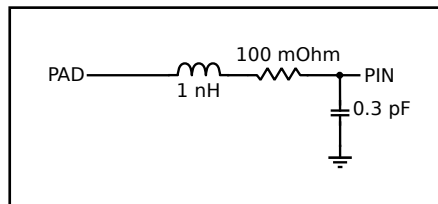
Figure 3.47: Bond wire and package parasitic model

As seen from the figure, bond-wire and package parasitics have negative impact on such parameter. For M8X phase 2's PCB, Taconic RF-35 substrate used. Its dielectric constant is 3.5 and its thickness is 0.76 mm. In order to match output of the package to 50 Ω, stepped transmission line is used on RF-35 substrate. Dimension of stepped transmission line is given in Fig 3.49. With the addition of stepped transmission line, output return loss will be in the range of target specification as seen in Fig 3.50.
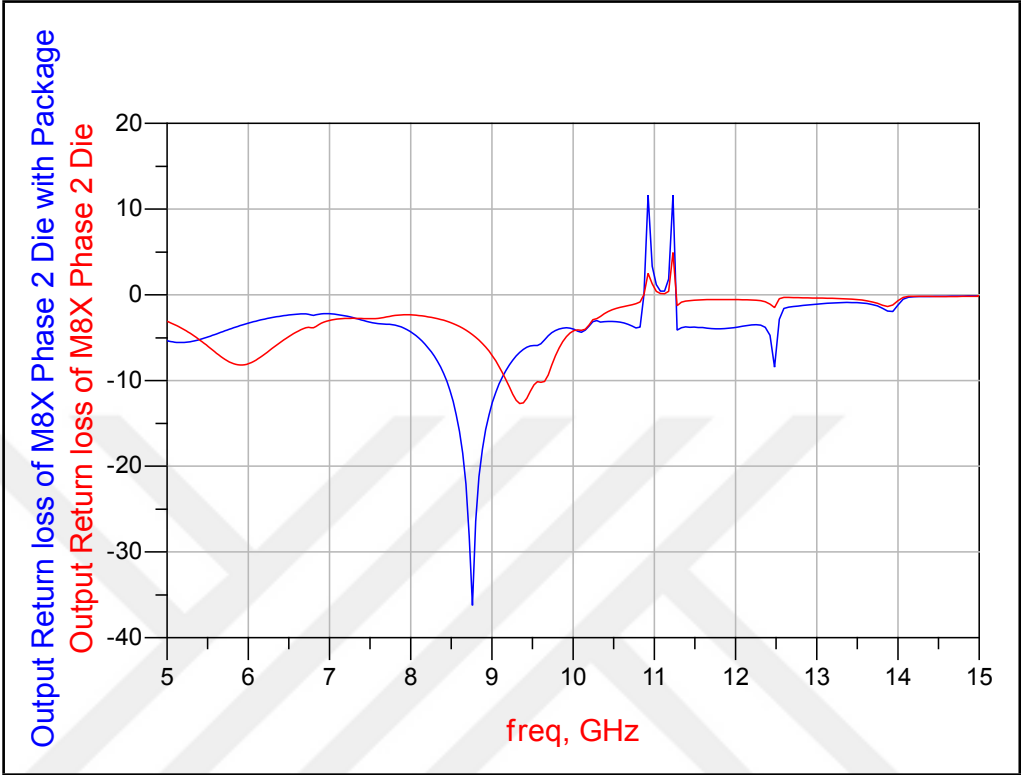
Figure 3.48: Output return loss of M8X phase 2 with bond wire and package parasitics
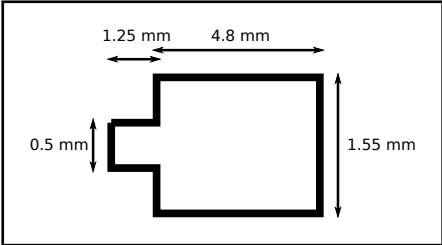
Figure 3.49: Stepped transmission line
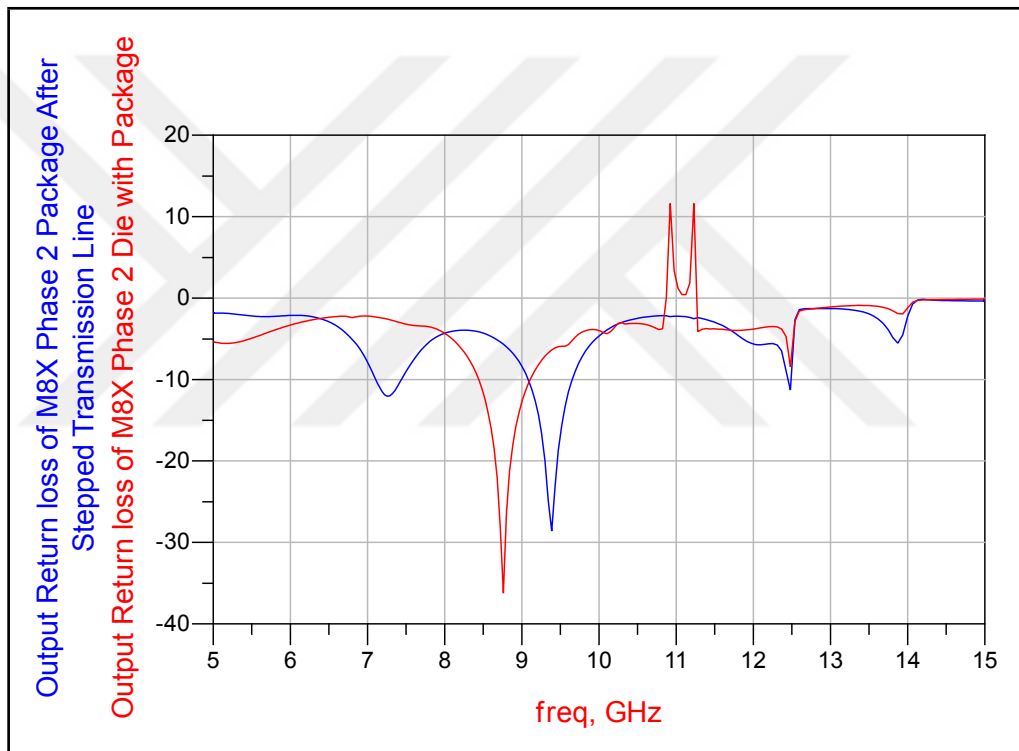
Figure 3.50: Output return loss of M8X phase 2 with stepped transmission line

3.7. M8X PHASE 2 TESTING

All measurements given in this chapter are conducted on one sample and all measurement results are preliminary test results.

3.7.1. M8X Phase 2 DC Testing

4 V supply voltage of M8X phase 2 is derived from 5 V by using Analog Device ADP123 CMOS linear regulator located on PCB. The output of regulator is set to 4 V by trimming potentiometer. Bandgap voltage reference is generated on PCB by using Analog Devices AD1580 1.2 V precision shunt voltage reference.

As mentioned in Section 3.3.5, one of the bias current can be observed outside the chip. Its nominal simulation value is 1 mA and is measured on PCB as 0.93 mA.

Simulated supply current of M8X phase 2 is 94 mA. It is measured as 105 mA on test board. There is approximately 10% variation on supply and bias current.

3.7.2. M8X Phase 2 Frequency Spectrum Testing

Rohde&Schwarz SMA100 and Agilent N9030A PXA signal Analyzer used for frequency spectrum testing. During following measurements, VGA set to maximum gain. In Fig. 3.51, the output spectrum of M8X phase is given for 5 dBm input power. The output power is about -12.5 dBm which is lower than simulation results. Simulated output power is around 0 dBm. Nearest harmonic is 25 dB below main signal component.

In Fig. 3.51, the output spectrum of M8X phase is given for -10 dBm input power. The output power is about -16.17 dBm. Harmonic level is about 3 dB which certainly much higher than simulation results. During frequency spectrum measurements, it is observed that harmonic contents are inversely proportional to input power. Lower input power causes higher harmonic contents.
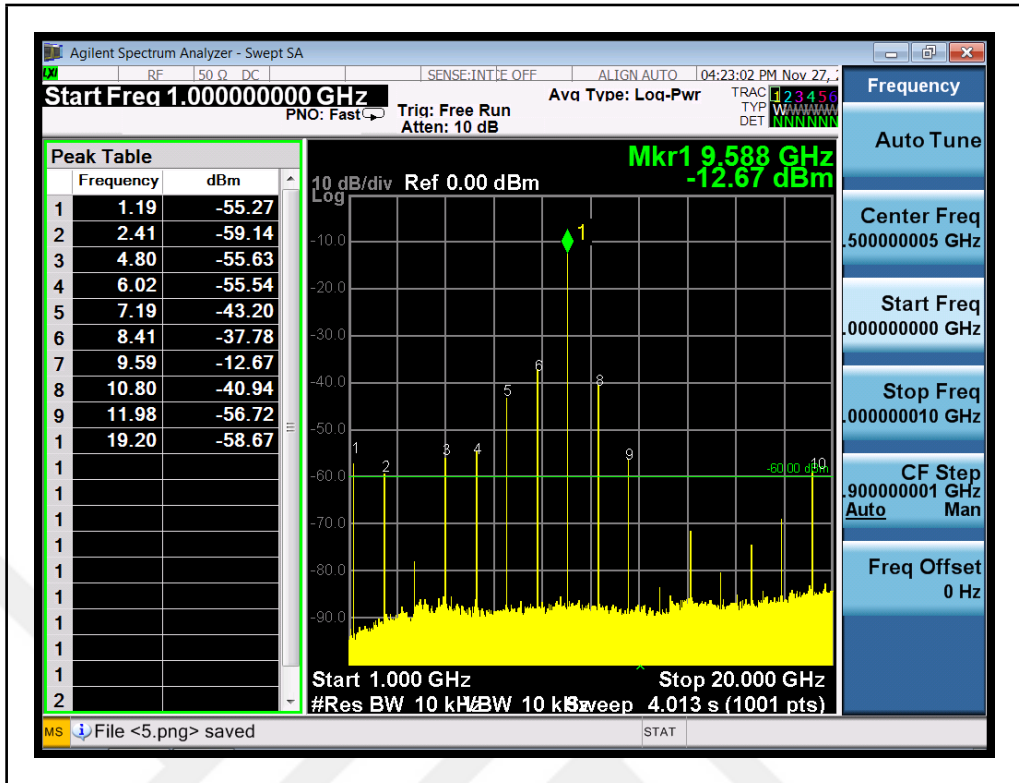
Figure 3.51: Output of M8X phase 2 for 5 dBm input power.
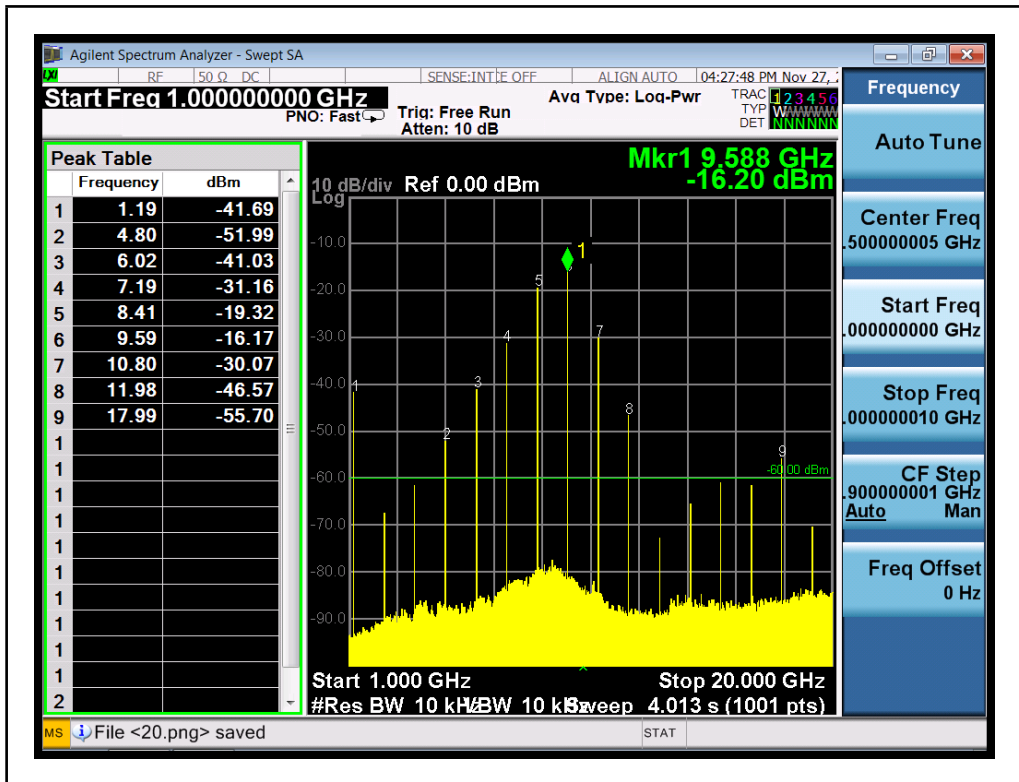
Figure 3.52: Output of M8X phase 2 for -10 dBm input power.

In Fig. 3.53, output power of M8X phase 2 versus input power is given. As seen from the figure, almost constant output power can be observed for input power as low as -10 dBm.
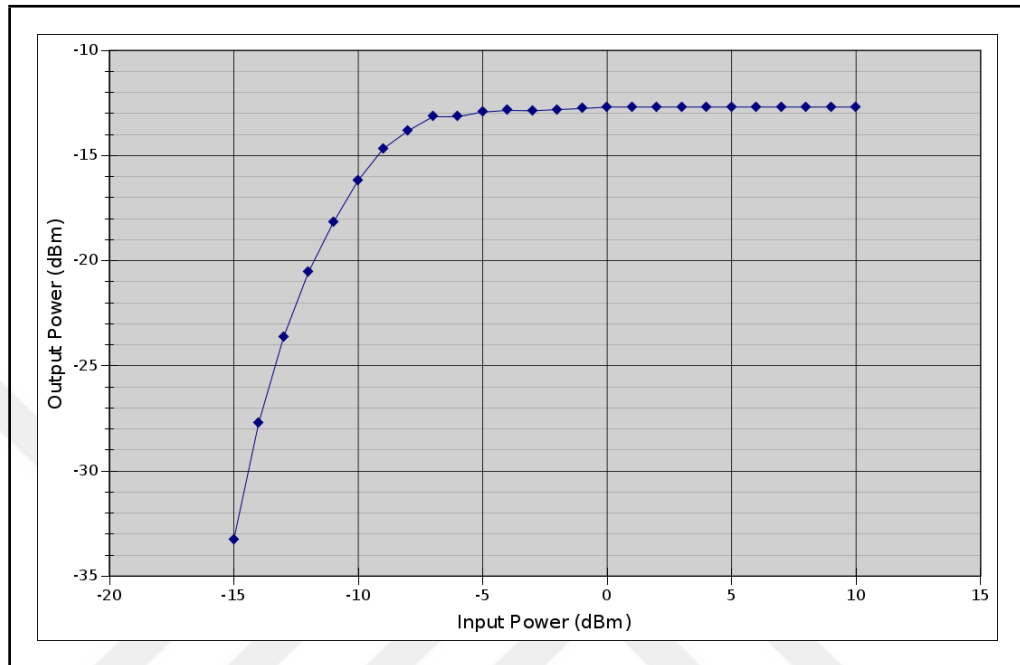
Figure 3.53: Output of M8X phase 2 vs. input power.

3.7.3. M8X Phase 2 Phase Noise Testing

Phase noise measurements conducted with an Agilient E5052B Signal Source Analyzer and an Agilient E5053A Microwave Downcoverter. As signal source Rohde&Schwarz SMA100A Signal Generator used. In order to get a better phase noise performance, outputs of two SMA100A were combined with power combiner. In Fig. 3.54, the SSB phase noise characteristic of related SMA100A is given.

In order to eliminate the effect of low output power on the measurement sensitivity, Hittite HMC903 low noise amplifier is used at the output. The SSB phase noise characteristic of M8X phase 2 is given in Fig. 3.55.

SSB phase noise characteristic of Hittite HMC444 is also measured with same signal source. Related measurement results is given in Fig. 3.55.

Figure 3.54: SSB phase noise measurement of combined SMA100A.
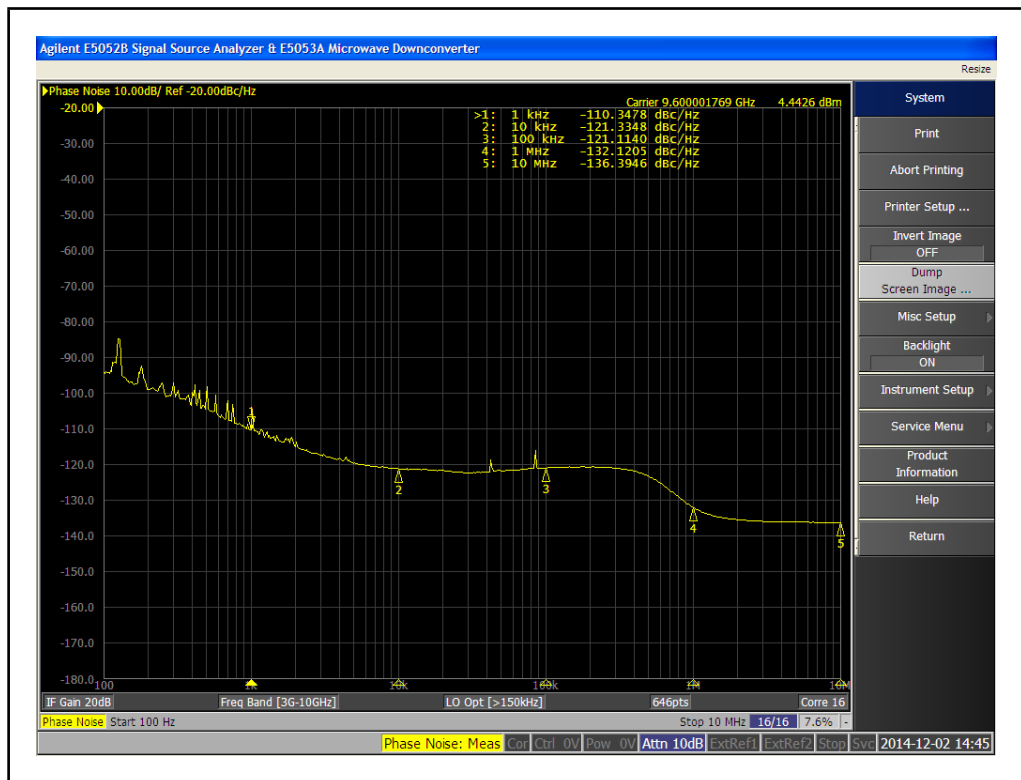
Figure 3.55: SSB phase noise measurement of M8X phase 2.
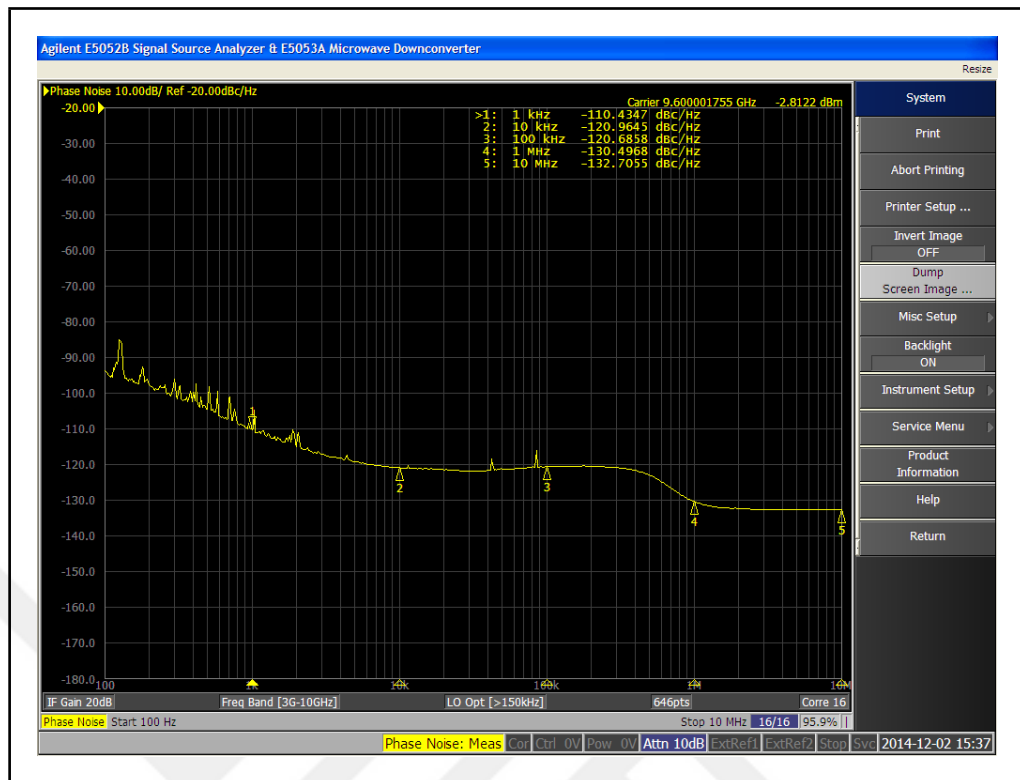
Figure 3.56: SSB phase noise measurement of Hittite HMC444.

3.8. RESULTS

M8X phase 2 tests indicate the following:

- Measured output power is almost 12 dB lower than simulation results. In order to isolate causes of low output power, first M8X phase 2 should be measured using RF probes. This will isolate the possibility that the problem is related to packaging, PCB, or design. If it is related to design, there are test points connected to biasing sections and various taps of blocks. With a new bonding plan and packaging, they will be available outside the chip. With the help of these test points, there will be enough information to debug the design. If the problem is due to the packaging and PCB, several iterations can be done on the PCB design. Bond wire and package parasitic model given in Fig. 3.47 contains approximate values of capacitance and inductance. Design of the stepped impedance transmission line used on PCB is highly sensitive to these elements. In order to design a more accurate output path on PCB, output return loss of PCB and M8X phase

2 should be characterized with network analyzer.

- Measured harmonic contents are inversely proportional to the input power. This behaviour has not been observed in simulations. Although observation points can give some information about the root of this behaviour, excessive simulations such as monte-carlo, post-layout simulations should be done on chip-level to recreate such behaviour on simulation environment.

- Due to signal source limitations, SSB phase noise characteristic of M8X phase 2 could not be measured accurately. On the other hand, measurement result of HMC444 also shows the similar performance with M8X phase 2.

4. CONCLUSIONS AND FUTURE WORK

4.1. CONCLUSIONS

In this thesis, a frequency multiplier, with a phase noise performance better than -130 dBc/Hz at 1 kHz offset, is designed and tested. Three test dies are designed and tested. First die is the balun which converts single ended input signal to differential. Its design and testing is given in Chapter 2. It is designed using passive components with the help of EM simulation. It tested using RF probes and close correlation between simulation and measurement has been observed. Second die consists of three frequency doublers and a variable gain amplifier. Its design and testing given in Chapter 2. Due to signal source limitations, phase noise could not be characterized precisely. However comparison with commercial product in terms of phase noise is satisfactory to realize next die. Other problem related to second die was the output power. Third die consists all the block required to fulfil system requirements. These blocks are the balun, frequency doublers, variable gain amplifier, differential to single ended converter, power amplifier, digital to analog converter, peak detector and on-chip reference generator. Its design and testing given in Chapter 3. In order to increase output power, modifications on previous blocks was made. During the design of second die, excessive corner analyses was done and results are given in Chapter 3. In order to sense output power, peak detector was realized. To set the output power, peak detector DC output was compared with DC output of on-chip reference generator. It was designed to compensate peak detector output variation between the different process corners, temperature variations. Digital to analog converter was designed to generate variable gain amplifier control voltages. Power amplifier was added at the end of frequency multiplier chain for 0 dBm output power. System level simulations show that designed system fulfil all the target specifications for three different process corners. Due to the limited time, only preliminary testing was conducted. Although simulated output power was about 0 dBm, the measured output power is about -12 dBm. Though necessary precautions was taken on chip to debug possible problems, the causes of low output power could not be determined at the time of writing this thesis. In terms of phase noise, third die

shows similar characteristic with previous design.

4.2. FUTURE WORK

Proposed future work is listed as follows:

- In order to isolate low output power problem, new bonding diagrams and related package and PCB configurations should be designed. There are unconnected pads on die to observe biasing of sub-blocks. The new bonding and testbench setups should make observing these bias points possible. The physical design at the output of frequency multiplier chain and power amplifier shall be designed to facilitate testing these points with GSGSG and GSG RF probes. Measuring the outputs with RF probes will eliminate the packaging and PCB related issues.

- Variable gain amplifier control loop was not realized on-chip. It should be first realized on PCB with discrete component and logic devices. After the verification on PCB, it will be realized on-chip by using standard digital cells and digital flow.

- On-chip bandgap reference should be designed.

- In order to characterize additive(residual) SSB phase noise of the designed frequency multiplier, phase noise measurement systems should be reviewed and appropriate one should be adopted. In [8], various residual phase noise measurement systems are reviewed. All of the systems are complicated and require excessive trial and design phases. Instead of designing such a complicated system, commercial products may be acquired to measure additive phase noise such as Agilent E5505A Phase Noise Measurement Solution

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