LEAKAGE CURRENT REDUCTION IN DYNAMIC ANALOG STORAGE

by

Erol Asığ

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APPROVED BY:

Prof. Dr. Uğur Çilingiroğlu .....
(Thesis Supervisor)

Assoc. Prof. Dr. Arda Deniz Yalçınkaya .....

Assoc. Prof. Dr. Serkan Topaloğlu .....

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Finally, I would like to dedicate this thesis to my beloved fiance Seçil Göncüoğlu. It was impossible to complete this work without her endless love, support and patience.

ABSTRACT

LEAKAGE CURRENT REDUCTION IN DYNAMIC ANALOG STORAGE

Analog data has to be sampled and held across a capacitor prior to processing by a discrete-time system. This requirement can be easily fulfilled as long as the sampling process is repeated at a sufficiently high frequency. In the case of low-frequency sampling or high-temperature operation the leakage currents associated with the sampling switch may deteriorate the data held across the storage capacitor. These leakage currents are particularly significant in the 0.18-μm or newer CMOS technology nodes.

We propose in this project a novel guarding technique that virtually eliminates the leakage current of an open switch by limiting port voltages to 100 μV at most. The data hold time offered by this technique is expected to be at least an order of magnitude longer than what the alternative techniques serving the same purpose can achieve. Featuring a short settling time and operating with only two unsynchronized clocks are two additional advantages offered by this technique. The only limitation on its application is the necessity of deep n-well NMOS devices.

ÖZET

CMOS ANALOG BELLEKTE KAÇAK AKIM AZALTIMI

Ayrık zamanlı sistemlerde analog verinin işlenebilmesi için önce örneklenmesi ve bir kondansatör üzerinde tutulması gerekir. Bu basit işlem, yeterince yüksek frekansta tekrarlanması koşuluyla, sorun yaratmadan yerine getirilebilir. Düşük frekans veya yüksek sıcaklık uygulamalarında ise kondansatör üstünde tutulan veride kayda değer kayıp ortaya çıkabilir. Bunun nedeni örnekleme anahtarına ilişkin kaçak akımlarıdır. Bu akımlar özellikle 0.18-µm ve daha yeni CMOS ailelerinde ihmal edilemez boyuttadır.

Bu projede, örnekleme ve tutma işlemi yapan bir anahtarın açık olduğu konumda terminalleri arasındaki gerilimleri en fazla 100 µV ile sınırlayarak kaçak akımlarını hemen hemen ortadan kaldıran özgün bir koruma tekniği önerilmektedir. Bu teknikle sağlanacak veri tutma süresinin aynı amaca hizmat eden diğer tekniklerin sağladığı süreden en az bir mertebe daha uzun olması beklenmektedir. Yerleşme süresinin kısalığı ve faz ilişkisi olmayan iki saatla çalışabilmesi gibi ek avantajlara da sahiptir. Üzerindeki yegane sınırlama derin n-kuyulu NMOS transistor kullanımıdır.

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LIST OF SYMBOLS/ABBREVIATIONS

A_d	Open Loop Gain of OTA
C_H	Hold Capacitor
C_L	Load Capacitance
C_{ox}	Oxide Capacitance
E_{gain}	Gain-error of DDA
f_d	Dominant Pole Frequency
g_m	Transconductance of Transistor
M_N	N_{th} MOSFET
I_C	Channel Leakage Current
I_D	Drain Current
I_G	Gate Leakage Current
I_J	Junction Leakage Current
I_L	Total Leakage Current
r_{ds}	Drain-Source Dynamic Resistance
r_o	Output Dynamic Resistance
R_N	R_{th} Resistor
S_N	N_{th} Switch
V_+	Non-Inverting Input of OTA
V_-	Inverting Auxiliary Input of OTA
V_{a+}	Non-inverting Auxiliary Input of OTA
V_{a-}	Inverting Input of OTA
V_B	Bias Voltage
V_C	Capacitor Voltage
V_{DD}	Supply Voltage
V_{GS}	Gate to Source Voltage
V_{GT}	Overdrive Voltage
V_i	Input Voltage
V_{inv}	Inverting Input of OTA
V_{os}	Offset Voltage

V_O	Output Voltage
$V_{O(max)}$	Upper Compilance Limit
$V_{O(min)}$	Lower Compilance Limit
V_{DSsat}	Drain Source Saturation Voltage
V_{th}	Threshold Voltage
μ_n	Electron Mobility of n-channel
φ	Sampling Clock
φ_d	1 Unit Delayed Sampling Clock
φ_{2d}	2 Unit Delayed Sampling Clock
AC	Alternating Current
DC	Direct Current
DDA	Differential Difference Amplifier
DIR	Differential Input Range
DNW	Deep n-well
GBW	Gain Bandwidth Product
PDK	Process Design Kit
PM	Phase Margin
RF	Radio Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor Field Effect Transistor
OTA	Operational Transconductance Amplifier
PMOS	P-type Metal Oxide Semiconductor Field Effect Transistor
SR	Slew Rate
S/H	Sample and Hold
SoC	System on a Chip
UMC	United Microelectronics Corporation

1. INTRODUCTION

In discrete-time systems, analog data needs to be sampled first and held on a capacitor. This simple process can be implemented without any problem with a sufficiently high switching frequency. However, data loss occurs remarkably in low frequency or high temperature applications. This loss is present because of leakage currents in switches. These switches implemented as NMOS M_1 and PMOS M_2 transistors are shown in Figure 1.1 as a part of conventional S/H circuit. C_H is the storage capacitor where data is stored as voltage. A unity-gain buffer is used to read data without interfering with the capacitor. Data is sampled in $\varphi = 1$ phase where M_1 and M_2 are in conduction. Data is stored on the capacitor as $V_c = V_i + V_B$,where V_i is the signal voltage and V_B is bias voltage. Transistors are in cut-off in $\varphi = 0$ phase where data is held. In the ideal case of zero leakage current I_L, the charge on the capacitor cannot find a way to discharge in this phase. Therefore V_C remains constant and buffer output V_O can be processed as its replica.

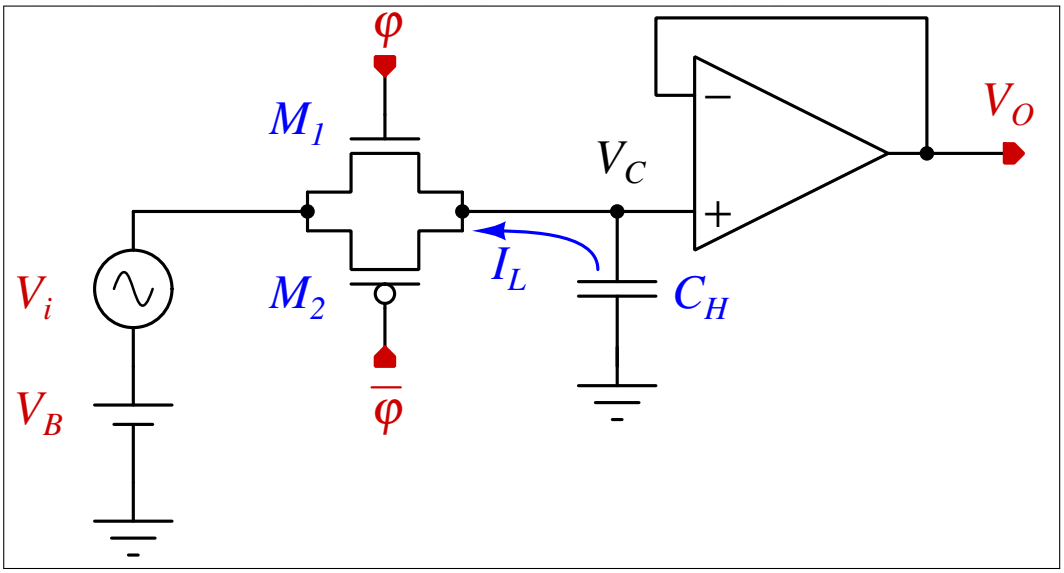

Figure 1.1. Conventional S/H circuit

Major leakage currents I_L, flows from V_C node to the bulk terminals of the two switching transistors by junction leakage and the input node by channel leakage. Gate leakage is also important for technologies newer than 0.18-µm process which do not use thick gate-oxide

transistors. Total leakage current is around 1-10 fA at room temperature in 0.18-μm technologies. Applicable integrated circuit capacitors is around pF, so the drop rate of the capacitor voltage will be around 1-10 mV/s. This drop rate is acceptable when holding period is below milliseconds and cannot exceed typical noise levels so there will be no problem in applications. However, especially in the biomedical applications where sampling frequency is too low, drop rate of the voltage becomes a serious problem.

Leakage currents are highly function of temperature except gate leakage. For example, between 20°C and 200°C leakage currents increases 4 orders of magnitude which we are going to discuss in Chapter 2 in detail. High temperature causes significant drop rate even with ms of hold time. Besides, leakage currents are very process and technology dependent and shows very poor yield. Because of above reasons, drop rate is nearly impossible to predict while designing.

The aim of the project is to make leakage currents technology and process independent and decrease at least an order of magnitude less than conventional circuit shown in Figure 1.1, thus we would have at least an order of magnitude longer hold time. Therefore, leakage currents will become 1-10 aA and drop rate will decrease to 1-10 μV/s.

In Chapter 2, we will describe basics of leakage currents and investigate techniques in the literature to prevent them.

2. BACKGROUND

Conventional topologies of S/H circuits are explained in details by R. Jacob Baker [1]. Related low frequency applications like neural networks are studied in [2–6]; but high temperature applications can exceed 200°C in those applications involving geophysical sensors used oil and natural gas research [7].

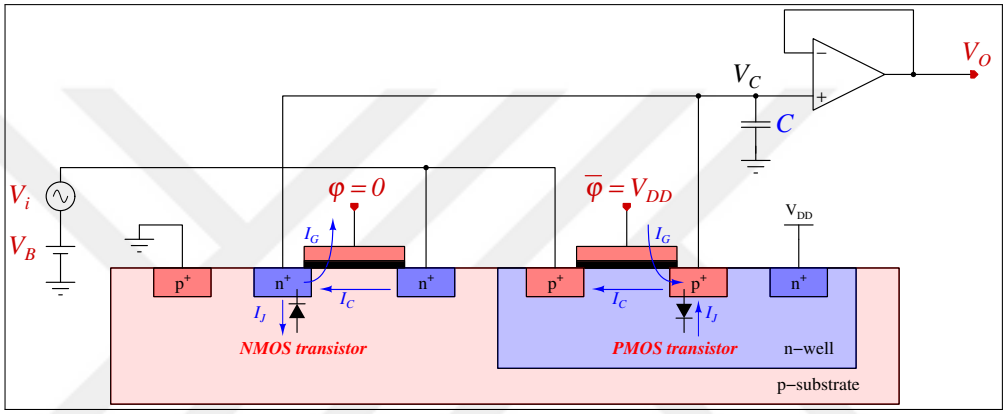

Figure 2.1. Leakage current components in a conventional S/H circuit

Leakage current components of a S/H circuit in holding phase of a conventional S/H circuit is shown by demonstrating cross section of the switching transistors in Figure 2.1. I_G, I_J and I_C refer to gate leakage, junction leakage and channel leakage, respectively. As mentioned in Chapter 1, I_G is significant remarkable in those CMOS technologies newer than 0.18-µm that don't use thick gate oxide transistors. This current in NMOS transistor flows to given direction where V_C has non-zero value. In the PMOS transistor, current flows in the direction indicated where V_C is different from V_{DD}. The root cause of I_J the reverse biasing of the junction. This current in NMOS arises when $V_C \neq 0$ and flows in the reference direction. In PMOS, it occurs when $V_C \neq V_{DD}$ and also flows in the reference direction. I_C occurs whenever MOSFET's drain-source voltage has non-zero value, that is $V_C \neq V_i + V_B$. This potential is usually non-zero because in holding phase V_i changes independently from V_C which stays at the sampled value. The common reason of all three leakage components is the potential difference between V_C and other nodes.

Temperature dependency and random mismatch of different samples of same circuit are investigated detailed in [8,9]. These negative properties which are expected to affect hold time of the S/H circuit are simulated with Cadence-Spectre with minimum dimensions by using *UMC L180 Mixed-Mode/RF* PDK shown in Figure 2.3 and Figure 2.2. First of Figures is related to temperature variation and it shows 1 fA leakage current at 27°C becomes 0.1 µA at 200°C by increasing 8 orders of magnitude.

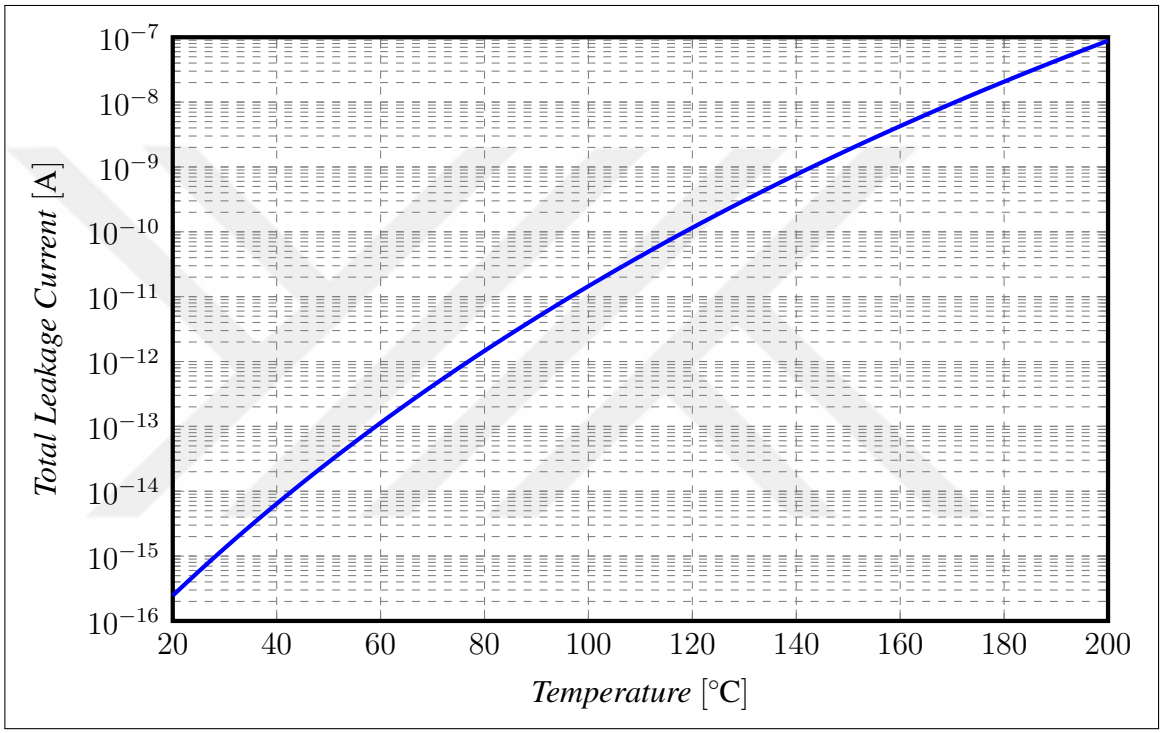

Figure 2.2. Temperature simulation of total leakage current

Monte Carlo simulations of the same circuit was implemented at 27°C as shown in Figure 2.3. Mean value of the total leakage current is 3.54 fA and standard deviation is 2.72 fA with respect to simulation results. Regarding to this simulation, total leakage current differs around 230 % for to 3-σ variation which is standard for semiconductor production.

Leakage reduction techniques in literature are commonly topological or physical. One of the simple solution is described in [4]. NMOS and PMOS leakage flows opposite direction to each other. Total leakage can be compensated by adjusting junction area but this solution is reasonable at constant, specific temperature and fixed junction potential. This technique has no effect on random distribution or channel and gate leakage.

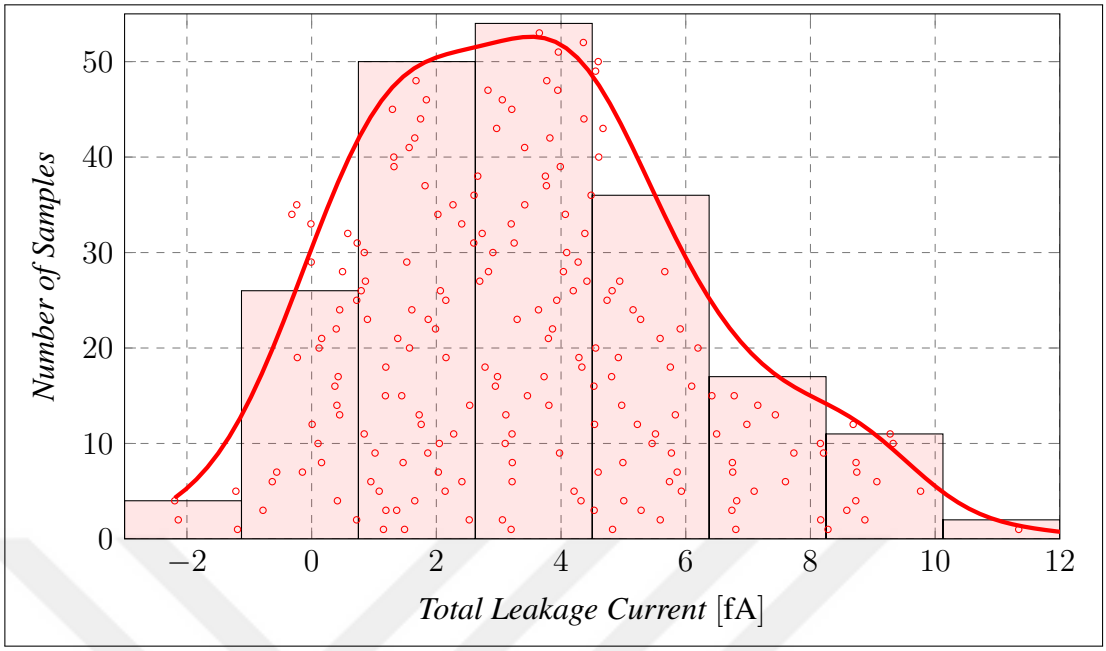

Figure 2.3. Monte Carlo simulation results of total leakage current

One technique used to reducing leakage currents is making a replica of leakage currents and injecting them in opposite direction. [10–14] are using this compensation method with different replication topologies. However, these methods don't use any kind of automatic control thus they become less effective because of random mismatch.

We have stated earlier leakage current components arise because of potential difference of holding node and other nodes of switching transistors. [15] proposed an topological solution which is based on zeroing drain-source potential to reduce critical channel and junction current. It is important to investigate this work in detail because our proposed circuit which will be explained in Chapter 3 is also based on zeroing the node potentials. Circuit schematic is given in Figure 2.4(a) and switch topology used in S_2 is given in Figure 2.4(a). φ represents the clock itself and φ_{2d} represents 2-unit delayed version of the clock so, that S_1 and S_2 is in conduction in sampling phase and S_3 is in cut-off. Circuit turns into holding phase with S_1 and S_2 forced into cut-off and S_3 into conduction. After ignoring charge injection, clock feedthrough and leakages, output voltage of operational transconductance amplifier (OTA) is given by

$$V_O = V_B + \frac{1}{1+A_d}V_i - \frac{A_d}{(1+A_d)^2}V_{os}, \tag{2.1}$$

and, node potential the of inverting input of OTA is

$$V_{inv} = V_B - \frac{1}{1+A_d}V_i - \frac{A_d(2+A_d)}{(1+A_d)^2}V_{os}, \tag{2.2}$$

where A_d and V_{os} represent OTA's open loop gain and offset voltage, respectively. It can be understand from (2.1) that if A_d is large enough, output voltage will be $V_O \approx V_B + V_i$, which is root cause. However, this potential changes with time because of the leakage currents of S_2. The root cause of the leakage currents is the voltage across switch S_2 in holding phase. From (2.1) and (2.2)

$$V_O - V_{inv} = V_i + \frac{1}{1+A_d}V_{os} \approx V_i + V_{os}, \tag{2.3}$$

we can find this potential, generally has large value due to V_i. It can create large leakage current, if no precaution is taken. This leakage flows to capacitor C and change $V_O - V_{inv}$ quickly in time. However, V_{inv} remains at V_B because of virtual ground at OTA. The only changing potential is V_O. In order to solve this problem, partially, [15] implemented the switch structure shown in Figure 2.4(b). φ_d is one unit delayed version of φ as shown. In the sampling phase, because clock signals are $\overline{\varphi} = 0$, $\varphi_d = 1$ and $\overline{\varphi_d} = 0$, M_B is in cut-off, M_A and M_C are in conduction so that T_1 and T_2 are shorted, on other words switch is closed. Holding phase starts with $\overline{\varphi} = 1$. First, M_A turns into cut-off and after one unit delay M_B follows it, so nodes T_1 and T_2 are disconnected. At the same time M_B starts to conduct and V_B is connected to the right terminal of M_A. T_1 is connected to V_{inv} which is expressed in (2.2). The voltage between the two terminals, which is the drain-source voltage is given by

$$V_{ds} = \frac{1}{1+A_d}V_i + \frac{A(2+A_d)}{(1+A_d)^2}V_{os} \approx V_{os}. \tag{2.4}$$

Bulk of M_A is connected to V_B so it has voltage expressed in (2.4) connected to T_1 terminal. Typical value of V_{os} is around 1-10 mV which is much lesser than potential expressed in (2.3), therefore current flows to T_1 terminal channel and junction leakage reduced.

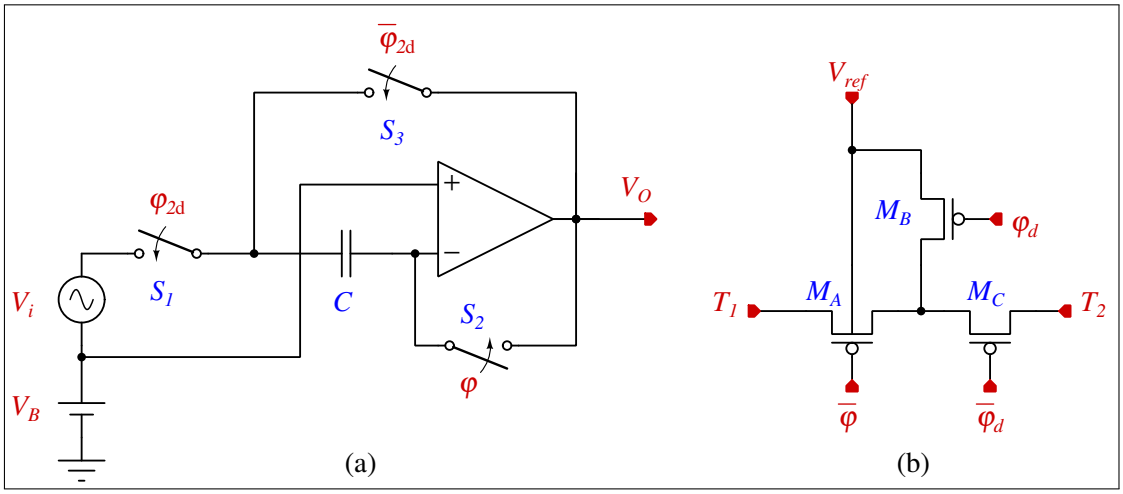

Figure 2.4. (a) A S/H circuit (b) S2 implemented in transistor level [15]

Another contribution to reduce leakage in M_A is that the PMOS is in accumulation mode. This condition occurs because in the holding phase substrate is tied to V_B and gate-bulk potential becomes positive. Operating MOSFET's in accumulation mode to reduce leakage currents is also proposed by [16].

There are three important problems in the topology shown in Figure 2.4. First problem, even with the offset level, there is still potential difference on S_2. Therefore, leakage currents have a significant minimum level because of random mismatch. Second problem is when $V_i < 0$ at the beginning of holding phase, after S_3 is closed, because the output voltage doesn't change immediately, T_1 node voltage goes higher than V_B for a short time. This event causes junction of M_A forward biased so leakage current occurs. Solution of this problem proposed by [15], is zeroing output voltage one time after S_2 opens, just before S_3 closes. This can be done by pulling down output node to ground with a NMOS transistor, however clock signals shown in Figure 2.4 and non-overlapping with shown clock signals needs to be generated. This clock generation circuit has a 28 μm^2 footprint which shows us the complexity of the design. Third problem is OTA is loaded with a much higher capacitance than the node capacitance, and this will reduce the settling time. This is really a problem in high frequency designs and the test chip's holding period is 10 ms.

3. PROPOSED TECHNIQUE OF LEAKAGE REDUCTION

We have stated that in Chapter 2 leakage currents occur because of potential difference between V_C node and other nodes in Figure 2.1 in holding phase. We propose '*shielding*' technique to reduce leakage currents which is based on zeroing potential difference between V_C, drain, source and bulk connection of transistors in holding phase. After zeroing node potentials, charge on the capacitor can be stored for a very long time because leakage currents are significantly reduced. This method includes offset compensation and can even cancel gate leakages and can reduce leakage an order of magnitude further than [15]. In addition, this method doesn't load the holding capacitor and can be implemented with much smaller capacitor. This will lead to a lesser settling time. Proposed technique requires two non-overlapping clock signals with no phase relation. All these advantages makes our proposed circuit much simpler than the technique described in [15].

3.1. OVERALL TOPOLOGY

In this section, we describe the overall topology of our proposed technique in detail. Figure 3.1 shows the top-level schematic.

S_N is the N_{th} switch, a transmission gate which is made of NMOS and PMOS transistors and they are triggered at logic-1. M_1 and M_2 are drawn to be investigated in detail because they are the source of leakage currents.A DNW(deep n-well) device is used for M_1 in order to access bulk connection. For buffering we use an OTA because only a capacitive load is to be driven. However, a rail-to-rail OTA is preferred for general purpose usage. Timing diagram of non-overlapping clock signals φ_1 and φ_2 are given in Figure 3.2.

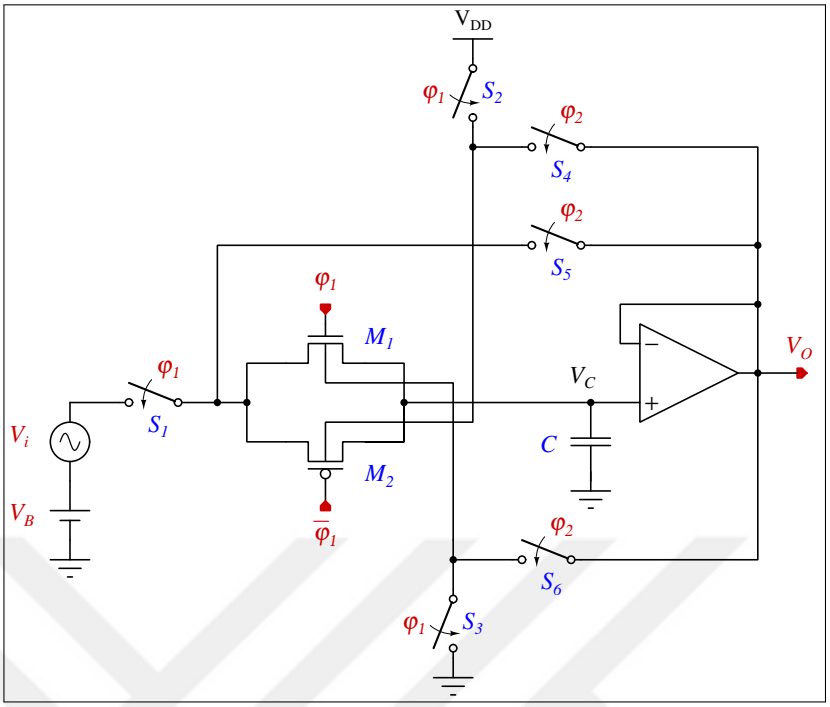

Figure 3.1. Circuit diagram of shielding technique

Generating non-overlapping clocks is much simpler than generating multiple phase clock systems. This non-overlapping clock generator circuit will be explained in Section 3.3.

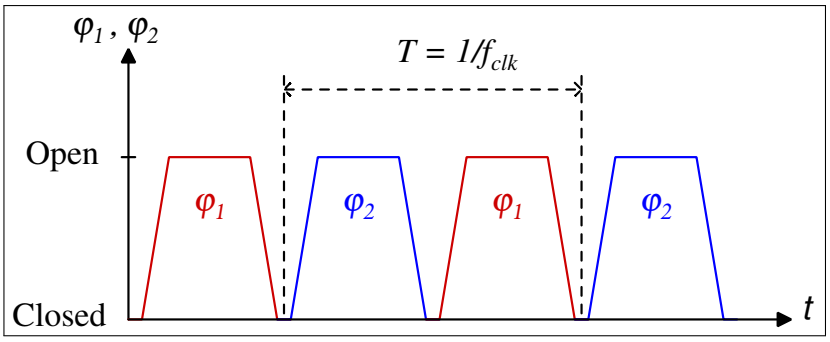

Figure 3.2. Timing diagram of non-overlapping clock signals

If gate leakage is also to be cancelled, generalized topology shown in Figure 3.3 is utilized.

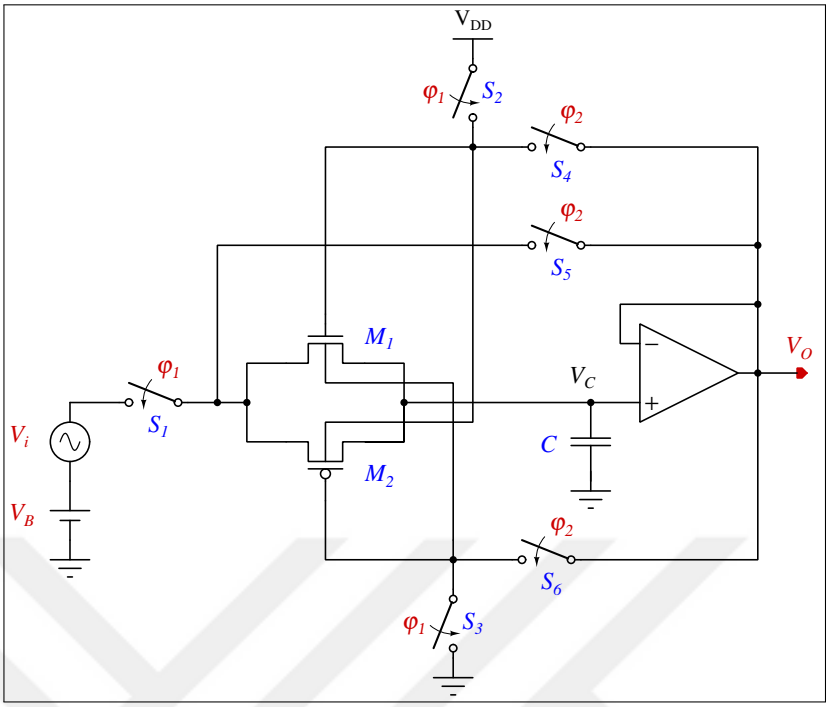

Figure 3.3. Proposed circuit diagram including shielding gate leakage

Gate leakage is negligible in the processes older than 0.18-µm. For newer processes they usually include thick gate-oxide devices in PDKs so gate is not a significant issue at all. That's why we only investigate and design circuit in Figure 3.1.

We need to investigate the circuit in different phases to understand its working principle. First phase prevails when $\varphi_1 = 1$, and second phase when $\varphi_2 = 1$.

After extracting closed switches from circuit diagram in Figure 3.1, simplified circuit becomes like in Figure 3.4. Only M_1 and M_2 are still shown in the circuit to investigate leakage currents.

In this sampling phase, M_1 and M_2 are closed and the data is stored on the capacitor. The capacitor voltage becomes

$$V_C = V_i + V_B, \tag{3.1}$$

and the output voltage is

$$V_O = \frac{A_d}{1 + A_d}(V_i + V_B) + \frac{A_d}{1 + A_d}V_{os}. \tag{3.2}$$

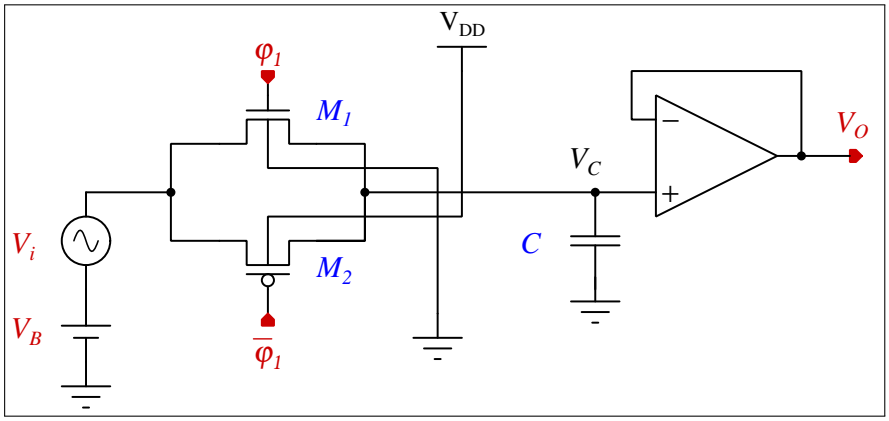

Figure 3.4. Simplified circuit in sampling phase

where V_{os} represents the input referred offset of OTA and A_d is open-loop gain of the OTA. If A_d is high enough, (3.2) becomes

$$V_O = V_i + V_B + V_{os}, \tag{3.3}$$

and data will be tracked until holding phase.

Proposed technique can be understand more clearly in holding phase. S_1 of Figure 3.1 is used to isolate input source from shielded transistors. This provides leakage currents will become independent from input voltage. The circuit can be redrawn after the extraction of closed switches as in Figure 3.5.

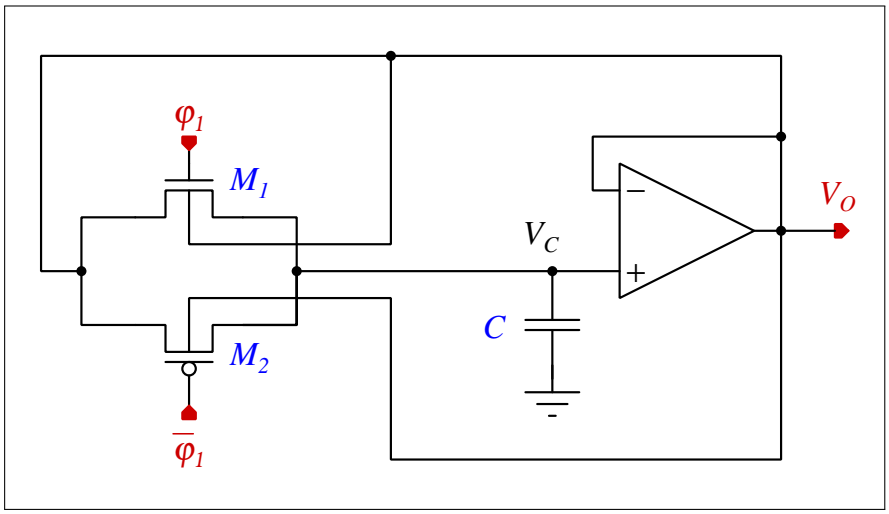

Figure 3.5. Simplified circuit in holding phase

In this phase, the buffer mirrors sampled V_C voltage to the output and applies it to the drain, source and bulk nodes of M_1 and M_2. V_O is described in (3.3). Potential difference between V_C and the other nodes becomes

$$V_O - V_C = (V_i + V_B + V_{os}) - (V_i + V_B) \approx V_{os}, \tag{3.4}$$

and this means potential difference between V_C and the other nodes becomes approximately zero. In ideal case, where input referred offset of OTA V_{OS} is neglected, leakage current becomes zero because there is no potential difference left to cause leakages. Clocks are $\varphi_1 = 0$ and $\overline{\varphi_1} = 1$ in this phase and both transistors operate in accumulation mode, so leakage currents become much less because gate leakage is negligible. However, because of random mismatch, V_{os} of a typical OTA is approximately between 1-5 mV and this causes a small leakage. Even with this potential difference our proposed technique provides extensive reduction of leakage currents.

The proposed circuit can be designed very easily because of the simplicity of its topology. It only requires a low-offset and high open-loop gain OTA. Bandwidth of OTA depends on the application so there is no significant limitation in design. We add only some extra switches and one simple non-overlapping clock generator circuit to design. Therefore it has not much difference from conventional design explained in Chapter 1.

The most outstanding problem in design is the input referred offset voltage of the OTA. There are several ways to deal with offset. We can categorise the available methods as automatic and non-automatic. The automatic methods can be found in literature as auto-zeroed amplifier. Let us examine one auto-zeroed amplifier proposed in [17] and shown in Figure 3.6. DDA stands for *differential difference amplifier* which has extra nulling inputs over an OTA. The circuit diagram is drawn differently from what is presented in [17] in order to explain the effect of amplifier. This circuit can be assumed as a sub-circuit to be used in Figure 3.1. C is represents a holding capacitor.

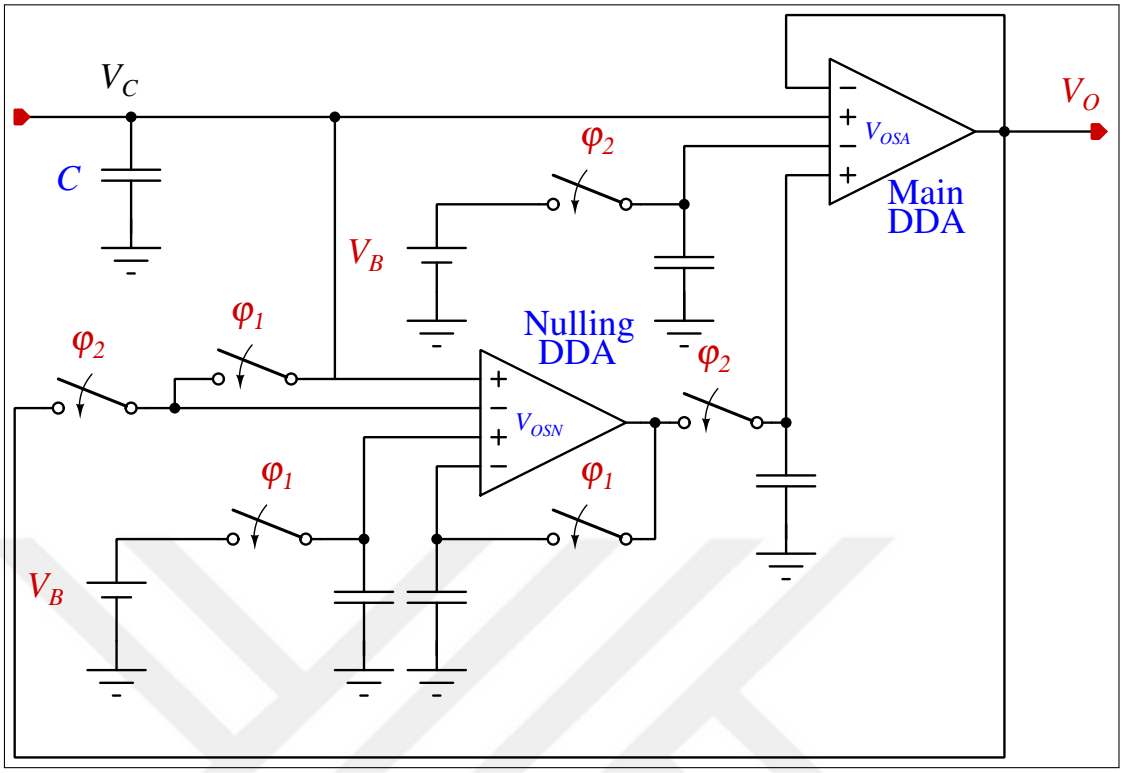

Figure 3.6. An auto-zeroed amplifier [17]

In order to understand how this amplifier operates, refer to corresponding article. Using this circuit brings extra problems to our proposed technique. As we can see there is a switch connected to holding capacitor which brings us extra leakage problems. Moreover, auto-zeroing requires storing offset voltage on capacitors and needs to be stored during every period. These switches need to operate at considerable high frequency much higher than main frequency because of the leakage currents of extra switches. Using high frequency clocks may not be be seem as a problem at all but let's consider the switch connected to holding capacitor. As our proposed technique is to be used at lower frequencies, data should be stored for a very long time. While this holding period, high frequency clocks causes clock feed-through and charge injection problems. Therefore, charge on the holding capacitor slowly altered during holding phase and the data suppose to be constant in this phase will not be constant anymore. That problems makes using this auto-zeroed amplifier impossible in our proposed technique.

All of the auto-zeroed amplifiers in literature, requires switched capacitor structure and none of them is suitable for our application.

Now let's consider another option for compensation of offset voltage. We can compensate offset voltage manually. This may not be best option but it is the most reliable one for our technique. Manual compensation can be done by deploying a DDA, instead of and OTA. Nulling inputs are actually another differential input stage. Figure 3.7 is a closed-loop application of DDA which can be used in offset compensation.

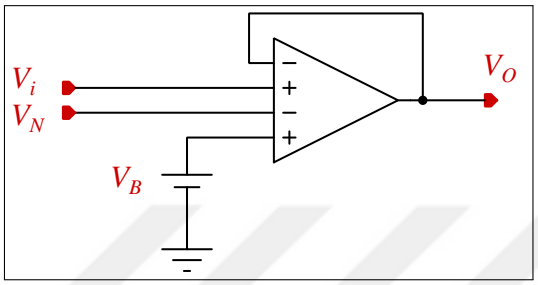

Figure 3.7. Closed loop unity gain configuration of differential difference amplifier

Shortly, we can write closed loop relation between input and output as

$$V_O = A_d(V_i - V_O + V_B - V_N + V_{os}). \tag{3.5}$$

Input signal will be applied to V_i. V_O and inverting input of the DDA are interconnected to get unity gain feedback. We can use two auxiliary inputs, V_N and V_B, making one connected to constant reference or preferably to common mode voltage and use the other one as variable DC source will allows us to compensate offset voltage. Mathematically we can express this as

$$V_O - V_{i-} = V_{os}, \tag{3.6}$$

and (3.5) becomes after compensation

$$V_O = A_d(V_O - V_i), \tag{3.7}$$

Therefore we can operate buffer without offset. V_N and V_B can be set either on-chip or externally. For example, can connect externally a potentiometer to calibrate system. More convenient usage will be on-chip controlling. Many SoC's use digital controller in its core today and this compensation voltages can be easily controlled digitally. Designing DDA will be explained in detail in Section 3.2. After inserting DDA to our circuit in Figure 3.1, the final schematic turns into the form shown in Figure 3.8.

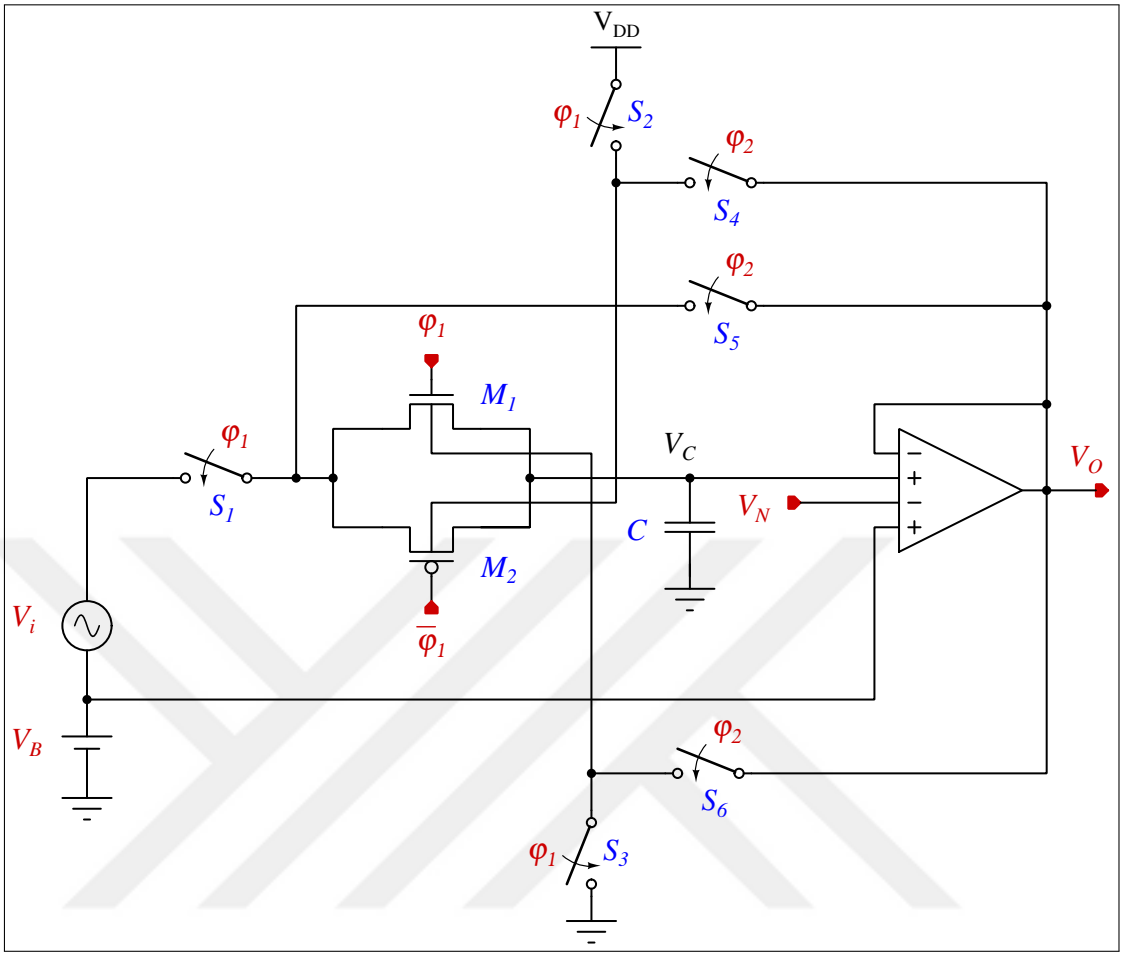

Figure 3.8. Shielding technique including offset compensation with DDA

This circuit shown in Figure 3.8 can be implemented in any CMOS technology which offering a deep n-well option. Leakage currents is reduced independent of the selected process, which implies a technique that is immune to random mismatch. Temperature dependency is also significantly reduced. Design of the circuit is very simple in comparison with the others in literature. Therefore we need only to design a high open-loop gain DDA and one simple non-overlapping clock generator circuit which as explained in Section 3.2 and 3.3, respectively.

3.2. DIFFERENTIAL DIFFERENCE AMPLIFIER

DDA design may be subject to specific constraints in any application-specific design scenario. Here, we target rather general features such as rail-to-rail operation with a reasonable bandwidth for, a typical 0.18 µm CMOS technology, and low power consumption. There are many of DDA topologies available in literature and text books. We will use folded cascode DDA based on NMOS drivers as shown in Figure 3.9. What makes this topology rail-to-rail despite absence of additional PMOS drivers is the availability of low-threshold NMOS devices in the PDK of the selected fabrication.

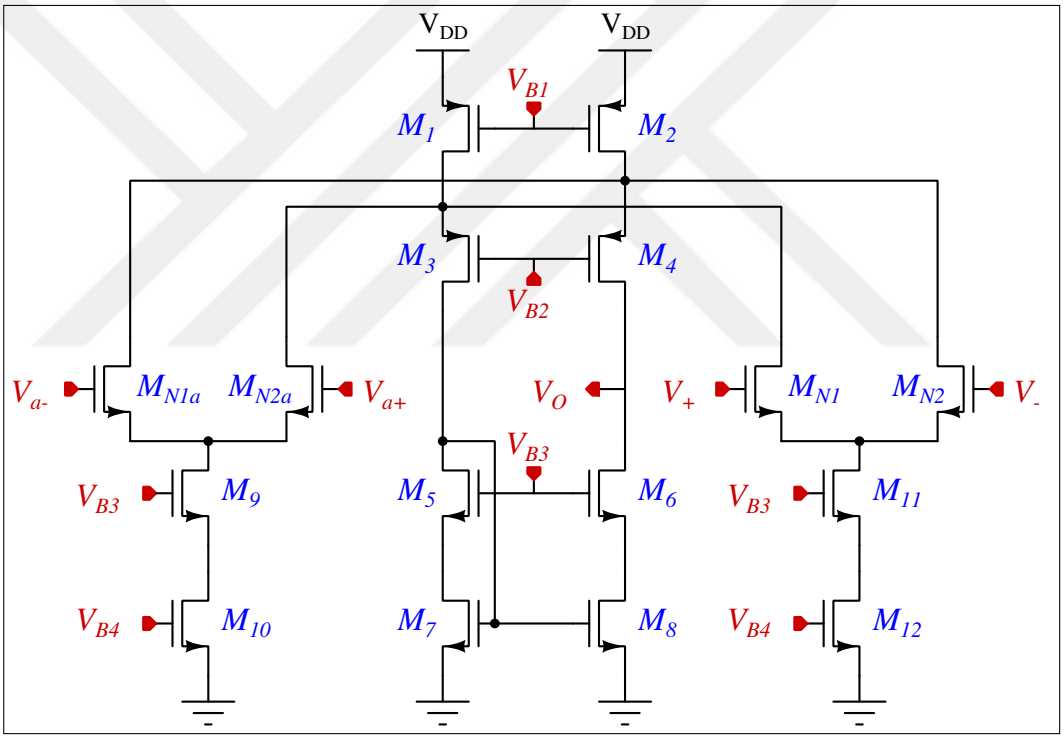

Figure 3.9. Circuit diagram of folded cascode DDA

M_{N1}, M_{N2}, M_{N1a} and M_{N2a} represent main NMOS and auxiliary NMOS drivers respectively. Main advantage of using folded cascode topology is that it is based on adding currents and this phenomena eases to add an auxiliary inputs. We now analyse the DDA topology with a view to model certain performance metrics. Note that M_{N1a} and M_{N2a} will be ignored in some calculations because of these two devices are not used as main drivers. Also note that bulk connections are made to ground in NMOS devices and to V_{DD} in PMOS devices.

Common-mode voltage(CMR) is only limited by threshold voltage of M_{N1}, M_{N2} and compliance limit of the current source below. We can define CMR as follows

$$V_{CM} \geq V_{GS(N1,N2)} + V_{DSsat(M9,M10)}, \tag{3.8}$$

where $V_{GS(N1,N2)}$ is the gate-source voltage of M_{N1} and M_{N2}, and $V_{DSsat(M9,M10)}$ is the drain-source saturation voltage of M_{N1} and M_{N2}. $V_{GS(N1,N2)}$ is directly related to the threshold voltage of the NMOS drivers here. Our design kit allows us to use low-threshold NMOS transistors in which threshold voltage is around 100 mV. Output range is related to M_2, M_4, M_6 and M_8. Its lower limit defined as follows

$$V_{O(min)} \geq V_{DSsat(8)} + V_{DSsat(6)}, \tag{3.9}$$

and the upper limit defined as

$$V_{O(max)} \geq V_{DD} - (V_{DSsat(2)} - V_{DSsat(4)}). \tag{3.10}$$

Open-loop gain equals to product of the transconductance of M_{N1}, M_{N2} and the output resistance which defined as follows

$$r_o = (A_{(6)} r_{ds(8)}) \parallel (A_{(4)} r_{ds(2)}) \parallel (A_{(4)} r_{ds(N1,N2)}) \parallel (A_{(4)} r_{ds(N1a,N2a)}), \tag{3.11}$$

$$A_d = g_{m(N1,N2)} r_o, \tag{3.12}$$

where

$$A_{(4)} = g_{m(4)} r_{ds(4)}, \tag{3.13}$$

$$A_{(6)} = g_{m(6)} r_{ds(6)}. \tag{3.14}$$

Dominant pole f_d frequency can be written as

$$f_d = \frac{1}{2\pi r_o C_L}, \tag{3.15}$$

where C_L is the load capacitance. Gain-bandwidth product GBW and the slew-rate SR of the amplifier are given by

$$GBW = A_d \times f_d, \tag{3.16}$$

$$SR = 2\pi \times GBW \times DIR, \tag{3.17}$$

where DIR is the differential input range and defined as follows

$$DIR = V_{GS(N1,N2)} - V_{th(N1,N2)}, \tag{3.18}$$

where $V_{th(N1,N2)}$ denotes the threshold voltage of M_{N1} and M_{N2}. Differential input range is not so important for our application so we can set it very low levels to get higher gain. GBW, as we discussed before, depends on the application. $V_{O(min)}$ and $V_{O(max)}$ can be set around to 200 mV for rail-to-rail applications. For practical and symmetrical layout we can design M_{N1}, M_{N2} and M_{N1a}, M_{N2a} identical.

Next thing to do is to design a proper current reference circuit. For this design we chose beta-multiplier current reference circuit. Advantages of this circuit is that it virtually eliminates supply and temperature sensitivity. It also features self-biasing. The circuit diagram is shown in Figure 3.10.

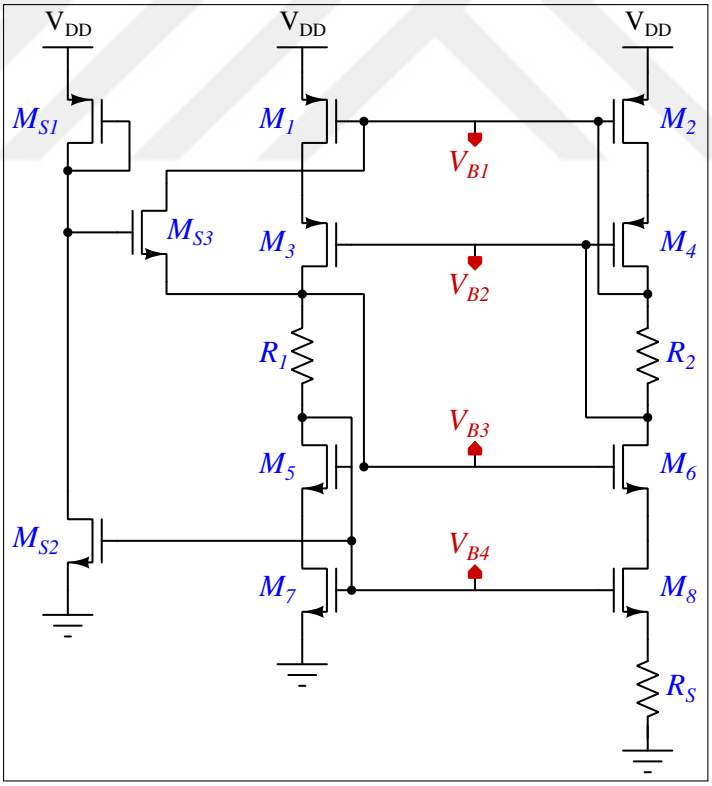

Figure 3.10. Beta-multiplier current reference circuit of the DDA

R_1 and R_2 are used to bias the related transistors so we can get desired drain-source saturation voltages. R_S is the resistor that controls the currents. Many designers choose $(W/L)_{(6,8)} = 4 \times (W/L)_{(5,7)}$ to get a stable circuit. By doing so, we end up with

$$R_S = \frac{1}{g_{m7}}, \tag{3.19}$$

and this is sometimes called *constant-g_m* biasing. We can set desired current by just setting proper R_S given in (3.19).

On the left hand side of the schematic shown in Figure 3.10, M_{S1}, M_{S2} and M_{S3} serve as a conventional start-up circuit. There is no mechanism in the topology by which circuit can start conducting current when first power-on. In order to avoid this circumstance, we add start-up circuit. This part of the reference circuit becomes active when the power supply is first turned on or somehow V_{B4} drops below threshold and should go to cut-off after serves its purpose. When no bias outputs are present, M_{S2} stays in cut-off and gate voltage of M_{S3} is just one $V_{DSsat(MS2)}$ below V_{DD} so M_{S3} starts to conduct current. With this conduction, gate capacitance of $M_{5,6}$ starts to charge and V_{B3} will slowly ramp up. After M_5 and M_7 start conducting, bias references reach to desired state and M_{S3} should go to cut-off. This can be ensured by setting drain voltage of M_{S2} and make gate-source voltage of M_{S3} below threshold. Thus, start-up circuit will not interfere with reference current generation.

3.3. NON-OVERLAPPING CLOCK GENERATOR

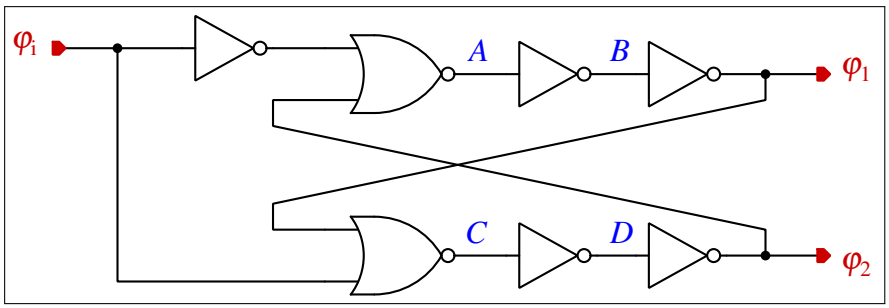

Figure 3.11. Non-overlapping clock generator circuit

Figure 3.11 shows the circuit diagram of two-phase clock generator circuit which is used in the topology of Figure 3.8 where φ_i is input clock signal. The main purpose of using this circuit is to prevent possible short circuit events between outputs and inputs while switching. Suppose that every high-to-low and low-to-high propagation delay through any gate equals one unit. With this simplification we can draw the timing diagram of the circuit as shown in Figure 3.12.

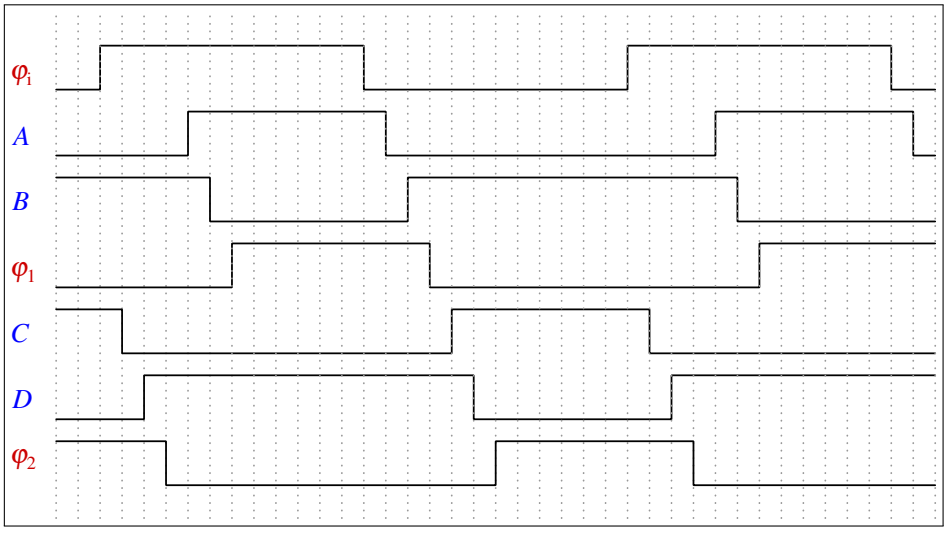

Figure 3.12. Timing diagram of non-overlapping clock generator

Note that, φ_1 in delayed with respect to φ_i by three units. We can extend this delay by adding more inverters to the inverter chain at the output depending on design requirements.

4. CIRCUIT DESIGN

In Chapter 3, we have described circuit topology and how our system works. Now, it is time to point out design specifications and size transistors properly regarding to requirements.

Specifications of each block is determined for general purpose usage. These specifications can be altered depending on system that our circuit will be used.

There are three blocks in our proposed circuit to be designed which are non-overlapping clock generator, differential difference amplifier and overall topology. In this Chapter, we will determine the specifications of each block and design circuits in transistor-level.

4.1. OVERALL TOPOLOGY DESIGN

There are two ways to design a system. Bottom-up strategy is designing lowest hierarchy level first then going higher levels. This design needs specification assumption of each block. In case of specifications doesn't meet overall system, designer needs to trim blocks iteratively until it meets design criteria. This method would take much time because we need to determine specifications of DDA and designing it requires lots of time. Therefore, top-down design is more convenient for our system. Design starts in the highest hierarchy of the system. This method needs adjustable models for each block to determine specifications. Then each individual block is to be designed separately according to specifications found in higher levels.

We have two blocks to be modelled in our system. Non-overlapping clock generator is easiest one to be modelled. Two clocks can be adjusted on testbench with ideal sources available on simulator. DDA needs to be modelled mathematically because we need to change its parameters such as, open-loop gain, output range, bandwidth etc. We choose Verilog-A language to model DDA. Verilog-A is analog counterpart of Verilog which allows us to use mathematical expressions more easily. The model that we used doesn't include auxiliary inputs which described in Section 3.2 because offset of amplifier can be changed externally

and it is given in Appendix A. Parameters shown in the model can be adjusted externally in simulator, thus we can determine best suitable parameter for our application. DDA is to be designed according to these parameters found in iterative simulations.

All the switching transistors in Figure 3.8 are sized in minimum dimensions to get reduce leakage as much as possible. Transistors M_1 and M_2 used as thick gate-oxide devices in out PDK to get even lesser leakage. Size of the transistors are given in Table 4.1.

Table 4.1. Transistor sizes of switching transistors

	Width	Length	(W/L)
M_1,M_2	240 nm	340 nm	0.7
Others	240 nm	180 nm	1.3

Note that, our purpose of using buffer is to mirror capacitor voltage to shielded nodes. Hence, output accuracy is important parameter to us. In closed loop configurations, gain-error defines output accuracy with offset voltage. Remember the input-output relation of the DDA given in Equation 3.5. Gain-error in closed-loop configurations is given by

$$E_{gain} = \frac{1}{A_d}, \tag{4.1}$$

where A_d is open-loop gain. According to simulations, 80 dB open-loop gain should be enough for our application. Gain-bandwidth product is not critical for us because we are using very low-speed clock. We also want a rail-to-rail operation so, output-range is chosen as 0.3 V-1.5 V. Other specifications is to be determined while designing the DDA in transistor level.

4.2. NON-OVERLAPPING CLOCK GENERATOR DESIGN

Let's start with the easiest block in our design. In Figure 3.11 we have shown that logic circuit diagram of the non-overlapping clock generator circuit. Transistor level design of NOT and NOR gates which are used in the circuit shown in Figure 4.1.

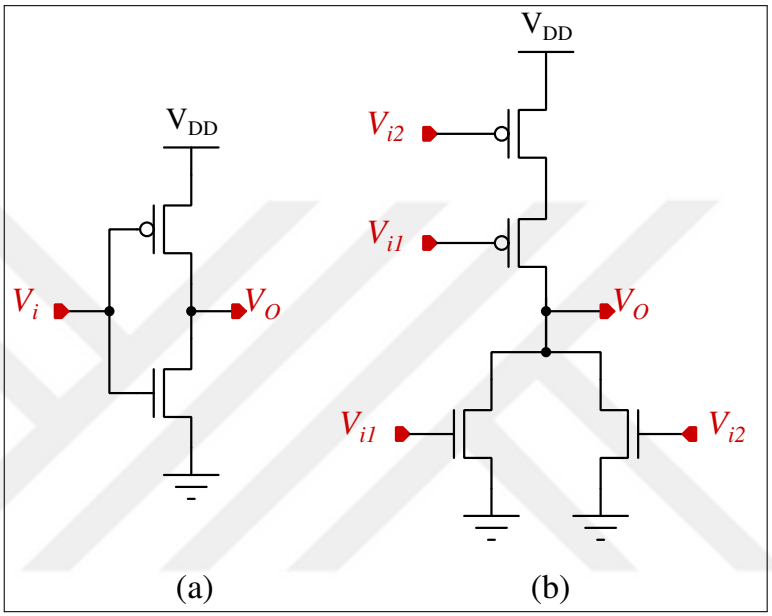

Figure 4.1. Transistor level of NOT and NOR gates

Designing non-overlapping clock generator is very simple. We don't have any speed limitation so we can size transistors at minimum dimensions. We size transistors to make high-to-low and low-to-high propagation delay to be equal and of course make as small as possible. This is done by equalizing PMOS and NMOS currents. Mobility of NMOS is roughly three times larger than PMOS so these transistors are three times wider. Table 4.2 shows the final size of transistors used in design.

Table 4.2. Transistor sizes of non-overlapping clock generator

	Width	Length	(W/L)
NMOS	240 nm	180 nm	1.3
PMOS	800 nm	180 nm	3.3

4.3. DIFFERENTIAL DIFFERENCE AMPLIFIER DESIGN

According to specifications found at top-level simulations, it is time to design DDA in transistor level. We are using folded-cascode topology so we don't need to concern about stability. Let's remember our specifications. Open-loop gain needs to be higher than 80 dB and output range is 0.3 V-1.5 V.

We will use well-known g_m/I_D methodology for sizing transistors. In this method, designer needs to know two of three constraints given which are g_m, V_{DSsat} and I_D. Our specifications gives us only V_{DSsat} of output transistors. g_m directly effects open-loop gain but it is not to be determined in the beginning of the design. I_D and g_m has more effect on bandwidth which doesn't our concern in design. Therefore we choose tail current as 2 µA to minimize power consumption and have considerable high bandwidth. Differential input range isn't critical also because we don't have speed limitation. Therefore DDA can slew in closed-loop application.

Next thing to determine is V_{DSsat} values of the output transistors. Note that Equation 3.9 and 3.10 gives us the lower and upper limits of the output. We choose maximum 100 mV V_{DSsat} for all the output transistors. With these selections, after setting 100 mV safety margin, output-range becomes

$$0.3\ \text{V} \leq V_O \leq 1.5\ \text{V}. \tag{4.2}$$

Remember the current-voltage relation of NMOS transistor

$$I_D = \frac{\mu_n C_{ox}}{2A_{bulk}} \frac{W}{L} (V_{GS} - V_{th})^2, \tag{4.3}$$

and drain-source saturation voltage is

$$V_{DSsat} = \frac{V_{GS} - V_{th}}{A_{bulk}}, \tag{4.4}$$

where I_D is drain-source current, C_{ox} is oxide capacitance per unit area, μ_n electron mobility of n-channel and A_{bulk} is process parameter. With given I_D and V_{DSsat} we can determine the W/L ratio of transistors. Note that given equations are simplified to ease design process and they are accurate enough only on long-channel processes. In our process, which can be considered as short-channel these equations are not applicable in design. Therefore these equations are only used to light our way to understand which parameter effects the other

ones. In the end, all parameters are determined by using simulator iteratively.

In order to ease design process, we choose all NMOS and PMOS transistors except drivers are chosen identical devices. We select 3.3 V devices for output devices and current reference because these transistors in our PDK has much more drain-source dynamic resistance for specified current so we could easily get larger gains with smaller devices. As for NMOS drivers, we select 1.8 V low-threshold transistors in order to obtain wider input range.

We have determined I_D and V_{DSsat} values so W/L ratios can be found for M_1, M_2 ... M_{12} given in Figure 3.9. It is time to size input drivers. We have decided identical devices for transistors M_{N1}, M_{N2}, M_{N1A} and M_{N2A}. As we have stated before, differential input range is not so critical for our application so we set device sizes are chosen to work close to threshold voltage to get higher g_m.

Before we continue design, we need to size beta-multiplier current reference circuit given in Figure 3.10. We have known that unit transistors should be identical to each other so W/L ratio of devices shall be same as mirrored ones. Start-up transistors and resistors are critical ones to be decided. M_{S1}, M_{S2} and M_{S3} are sized to ensure M_{S3} stays in cut-off state in normal operation of reference circuit. R_1 and R_2 are sized to meet 100 mV safety margin for output. R_S is found in Equation 3.19.

We have determined all W/L ratios for transistor with iterative DC operating point simulations to meet design criteria. All length of the transistors are set to 1 µm in the beginning of the iterative simulations. After verifying DC operating points of all devices, last thing to do is to get high open-loop gain. In g_m/I_D methodology, gain is set with keeping W/L constant while changing length of devices. We performed stability analysis iteratively to get high open-loop gain. We will give more details about these simulations in Chapter 5. Device sizes of DDA in Figure 3.9 shown in Table 4.3.

Table 4.3. Transistor sizes of the DDA

	Width	Length	(W/L)
M_{N1},M_{N2},M_{N1a},M_{N2a}	1 µm	0.8 µm	1.25
M_1,M_2	2×22.4 µm	1.4 µm	32
M_3,M_4	22.4 µm	1.4 µm	16
M_5,M_6,M_7,M_8,M_9,M_{10},M_{11},M_{12}	3 µm	0.8 µm	3.75

Sizes of the beta-multiplier current reference circuit in Figure 3.10 is given in Table 4.4.

Table 4.4. Transistor sizes of the beta-multiplier current reference circuit

	Width	Length	(W/L)
M_1,M_2,M_3,M_4	2×22.4 µm	1.4 µm	32
M_5,M_7	2×3 µm	0.8 µm	3.75
M_6,M_8	8×3 µm	0.8 µm	3.75
M_{S1},M_{S3}	340 nm	240 nm	1.25
M_{S2}	1 µm	180 nm	1.25

Note that, some transistors are fingered to make sure all unit devices have same current flow. The values of resistors are given in Table 4.5.

Table 4.5. Resistor values of the beta-multiplier current reference circuit

R_S	14.5 kΩ
R_1	64 kΩ
R_2	67 kΩ

5. VERIFICATION

In this Chapter we are going to verify the presented in Chapter 3. All of the verification has been performed at *Yeditepe Microelectronics Design and Characterization Laboratory* by using *Cadence Virtuoso and Cadence Spectre*. Recall that the design is based on a PDK provided by *Europractice* for *UMC L180 Mixed-Mode/RF* CMOS technology.

5.1. NON-OVERLAPPING CLOCK GENERATOR VERIFICATION

First of all we are going to verify the non-overlapping clock generator circuit. For input clock φ_i we applied signal with 800 ps pulse width to see non-overlapping clocks more clearly. Simulation runtime is 1.5 ns and the results are shown in Figure 5.1.

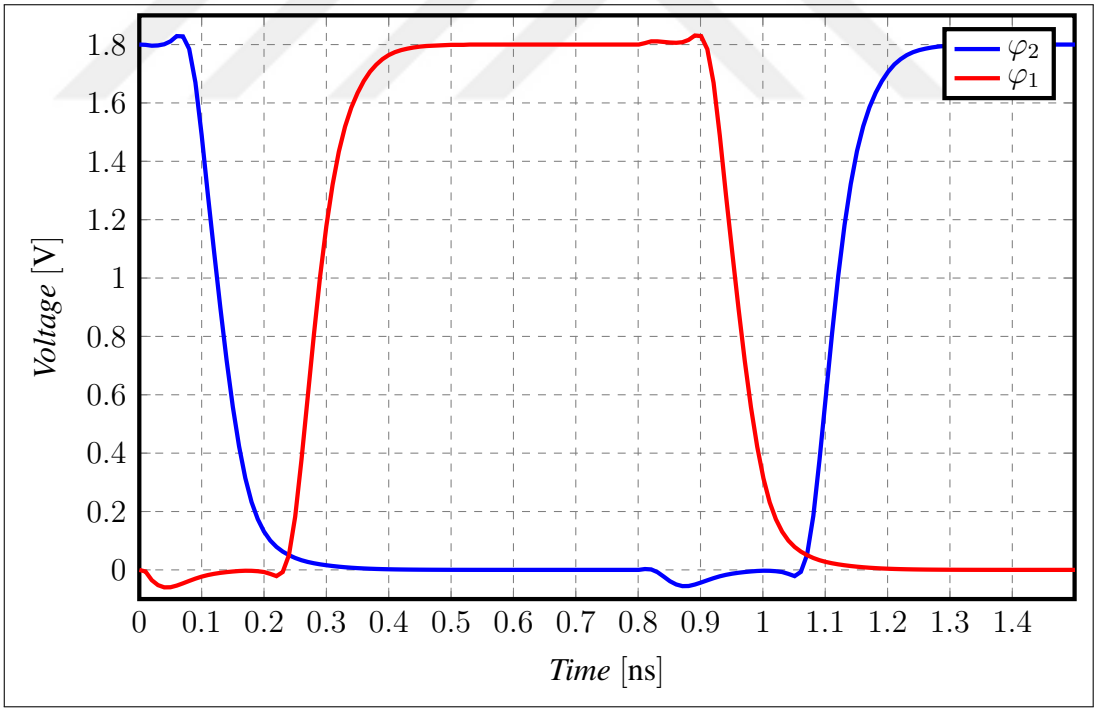

Figure 5.1. Simulation results of non-overlapping clock generator

Considering 0.9 V as logic threshold, the duration of dead time where both clocks are at logic 0 or 1, appear to be around 150 ps. Low-to-high and high-to-low propagation delays are approximately equal to each other.

5.2. DIFFERENTIAL DIFFERENCE AMPLIFIER VERIFICATION

First off all we are going to make DC analysis and find operating point of devices. After that, we are going to do AC analysis to get phase margin and open loop gain of the amplifier. Finally, we are going to do a large signal analysis with unity-gain configuration which is the most challenging configuration of DDA. Additionally, we are going to perform monte-carlo simulations to get worst corners which DDA has maximum offset and we are going to trim this parts with our nulling inputs.

The testbench used for this simulations shown in Figure 5.2 below. V_{DD} and V_B are set to 1.8 V and 0.9 V respectively, in all simulations. For the other sources we are going to talk about them in the relevant simulations. Also notice the instance I_{PROBE} connected to the feedback loop. This is an instance provided by *Cadence* and it is used to perform stability analysis. In DC and transient simulations it becomes short circuit so it will not affect simulation. The instance calculates loop-gain and stability parameters in stability analysis and it allows us to make AC simulations much more easier.

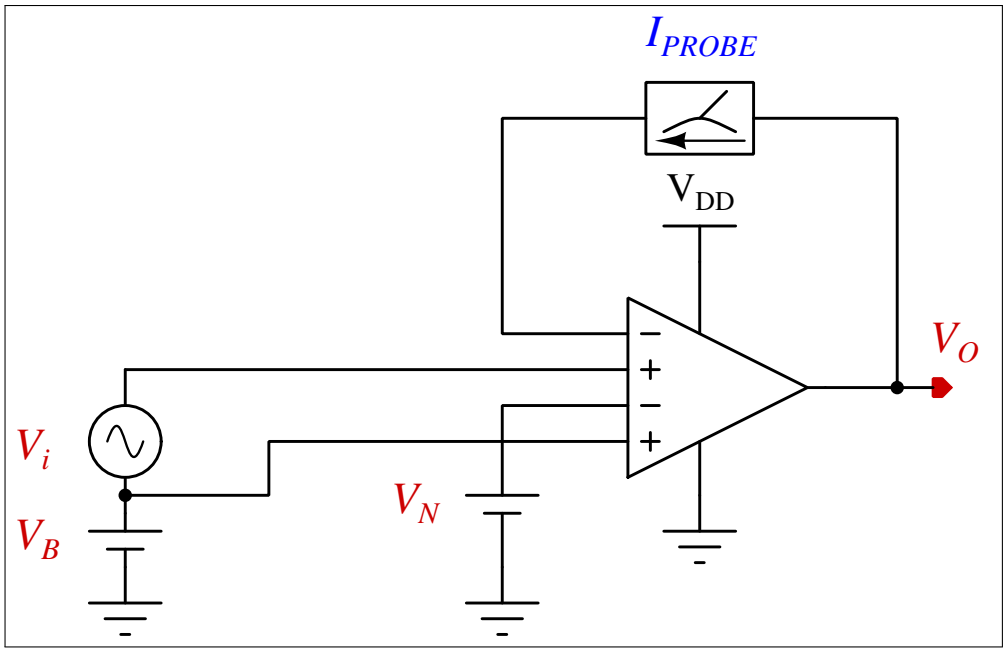

Figure 5.2. Testbench of DDA

5.2.1. DC Analysis

Operating point analysis is the very first step of designing and verifying analog circuits. We have already discussed designing and sizing of the transistors in Section 4.3. Design requires iterative simulations and they are already performed while sizing devices. In this Section, we will show final verification of the DDA.

Now, we will focus on operating point simulation results. For the simulation V_N is set 0.9 V thus auxiliary drivers will not affect the amplifier and AC input voltage is set to zero. We expect that output voltage stays at 0.9 V because of unity gain configuration so we can determine transistors' operating conditions. This is a DC simulation at one point that will show us scalar values. Results of the operating point of devices are given in Table 5.1. V_{GT} refers to overdrive voltage.

Table 5.1. DC operating point results of DDA

	I_{DS}	V_{DSsat}	V_{GT}
M_{N1},M_{N2},M_{N1a},M_{N2a}	1 µA	79.8 mV	26.2 mV
M_1	-4 µA	-87 mV	-47.1 mV
M_2	-4 µA	-87 mV	-47.1 mV
M_3	-2 µA	-88.3 mV	-44.3 mV
M_4	-2 µA	-88.4 mV	-44.5 mV
M_5	2 µA	87.2 mV	44.6 mV
M_6	2 µA	87 mV	44.2 mV
M_7	2 µA	86.4 mV	47.7 mV
M_8	2 µA	86.4 mV	47.7 mV
M_9,M_{11}	2 µA	87.2 mV	44.7 mV
M_{10},M_{12}	2 µA	86.4 mV	44.7 mV

Bias voltages are shown in Table 5.2 below.

Table 5.2. Bias voltages

V_{B1}	1.03 V
V_{B2}	0.76 V
V_{B3}	0.98 V
V_{B4}	0.73 V

Operating point results of the beta-multiplier devices are shown in Table 5.3.

Table 5.3. DC operating point results of beta-multiplier current reference circuit

	I_{DS}	V_{DSsat}	V_{GT}
M_1	-4 µA	-87.1 mV	-47.1 mV
M_2	-4 µA	-87.1 mV	-47.1 mV
M_3	-4 µA	-88.5 mV	-44.6 mV
M_4	-4 µA	-88.5 mV	-44.7 mV
M_5	4 µA	87.2 mV	44.6 mV
M_6	4 µA	57.5 mV	-31.62 mV
M_7	4 µA	86.4 mV	47.7 mV
M_8	4 µA	56.6 mV	-29.7 mV
M_{S1}	-1 µA	-227.3 mV	-266.7 mV
M_{S2}	274 aA	56.8 mV	-801.7 mV
M_{S3}	1 µA	112.3 mV	88.3 mV

DC operating values matches with the design shown in Section 4.3. V_{DSsat} values are better than expected. After verifying DC operating point of the amplifier, we will sweep input voltage to observe input and output range. This can be also verified by using operating point values of the transistors, but observing directly output gain will give more accurate results. For this simulation we will sweep V_i from 0 to 1.8 V and plot derivative of the output. We used the following expression for determining gain

$$Gain = \frac{dV_O}{dV_i}. \tag{5.1}$$

Simulation results of DC sweep can be observed in Figure 5.3

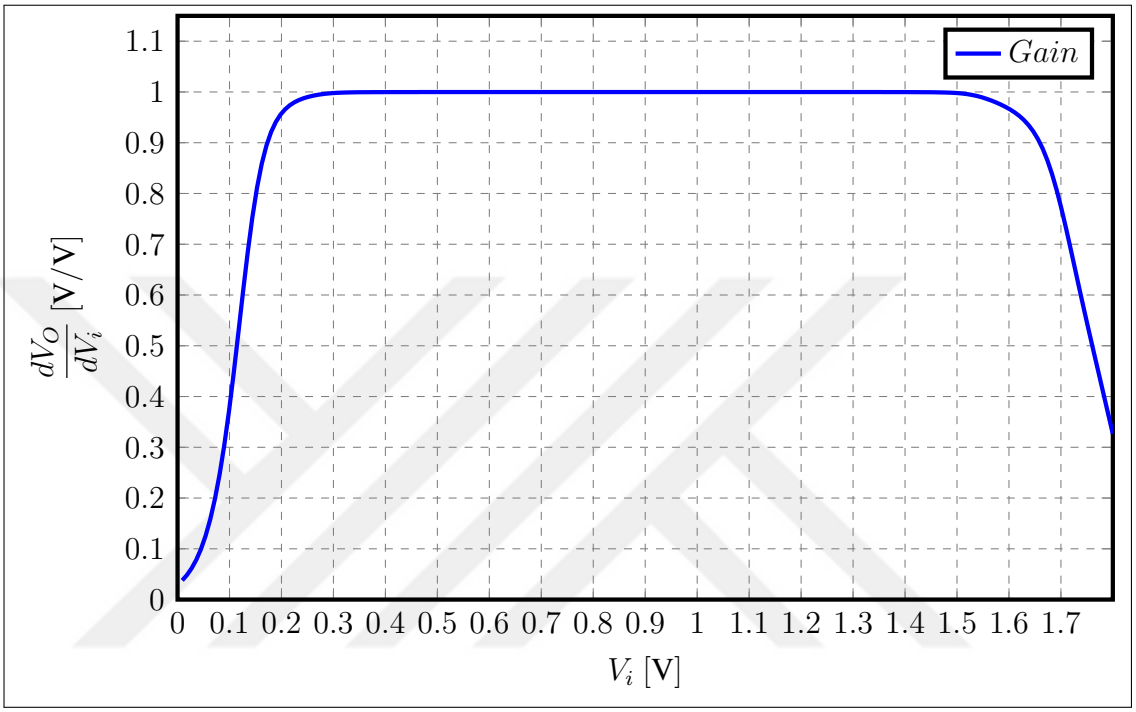

Figure 5.3. Closed-loop gain of the amplifier

In order to determine operating range, we need to focus on where $Gain \approx 1$. From results, we can say that DDA can be operate as unity-gain buffer within input and output range from 0.3 V to 1.5 V. Gain is lost when output devices is not operate in saturation mode anymore. We can see that output devices has approximately 90 mV V_{DSsat} and limited with two V_{DSsat}. Therefore, DC sweep results match with operating point analysis. Output limits can be written as follows

$$V_{O(min)} \approx 0.3 \text{ V}, \tag{5.2}$$

$$V_{O(max)} \approx 1.5 \text{ V}. \tag{5.3}$$

5.2.2. Stability Analysis

Now we will perform stability analysis to obtain open-loop gain and phase margin of the amplifier. In old fashioned way, we need to break feedback loop and make AC simulation. *Cadence* provides us stability analysis with $Iprobe$ shown in Figure 5.2. This instance breaks loop and make proper adjustments at load side so we would not need to do extra testbench change. V_N is set to 0.9 V for this simulation. Simulation results are shown in Figure 5.4.

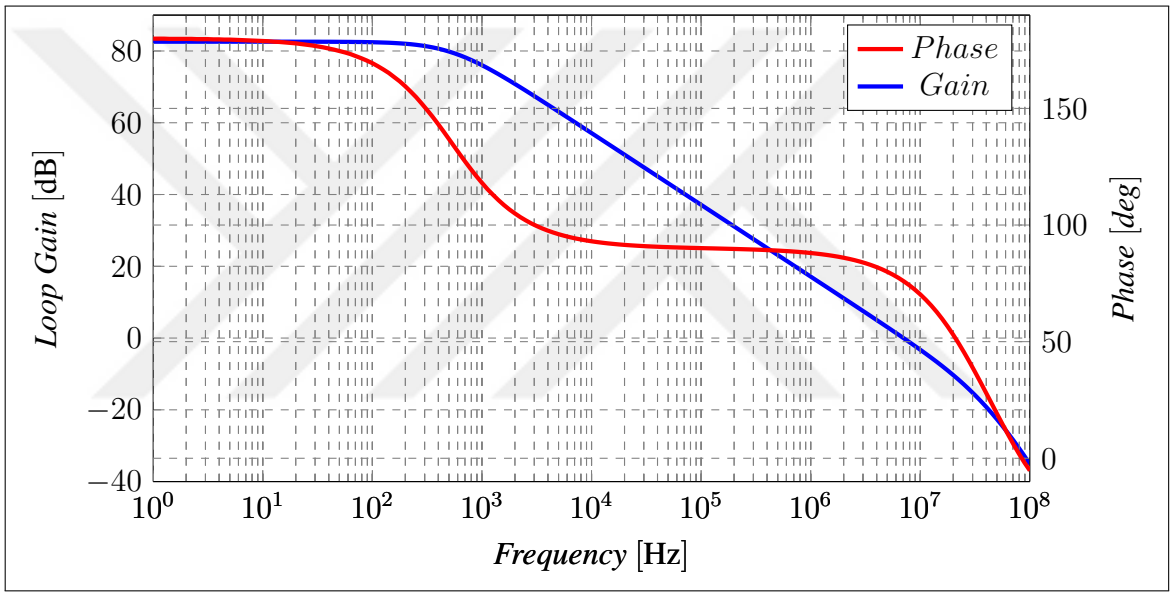

Figure 5.4. Open-loop gain of the amplifier

Loop-gain is drawn in dB and it is measured as 82.6 dB. Phase margin is defined as the phase difference to 180 ° when loop gain equals to 0 dB. This means output and input amplitude are identical at this particular frequency. This frequency is also defined as gain-bandwidth product. From the simulation results, stability summary is given in Table 5.4.

Table 5.4. Stability summary of the DDA

A_d	13.48k (V/V)
GBW	6.98 MHz
PM	75.36 °

5.2.3. Transient Analysis

In this section, we will describe the results of verification time-domain analysis. Firstly, we need to ensure that our start-up circuit in Figure 3.10 is working correctly. In order to implement this scenario, we ramp-up V_{DD} slowly to 1.8 V and determine whether the bias voltages and reference current settle properly or not. In this simulation V_N is set to 0.9 V and runtime is 1.1 ms.

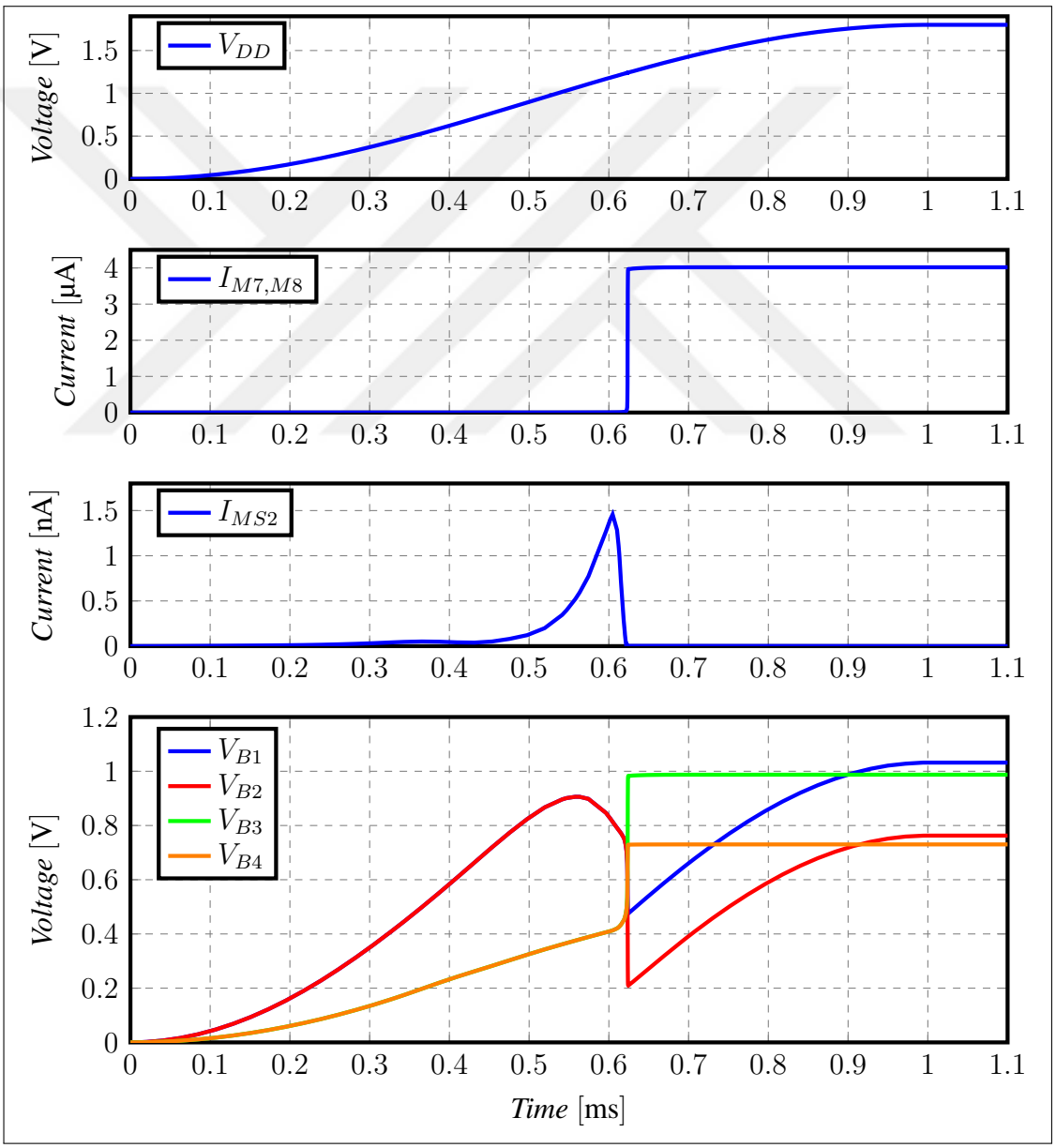

Figure 5.5. Beta-multiplier startup

From the results, we can observe that I_{MS2} flows only when node V_{B3} is below threshold. After M_{S2} serves its purpose, the transistor goes into cut-off region and all bias voltages settle once the power-supply voltage reaches V_{DD}.

Now, we need to confirm that unity-gain configuration works properly. To this end, we will apply a pulse signal to it's input and observe the output voltage. The simulation results are shown in Figure 5.6.

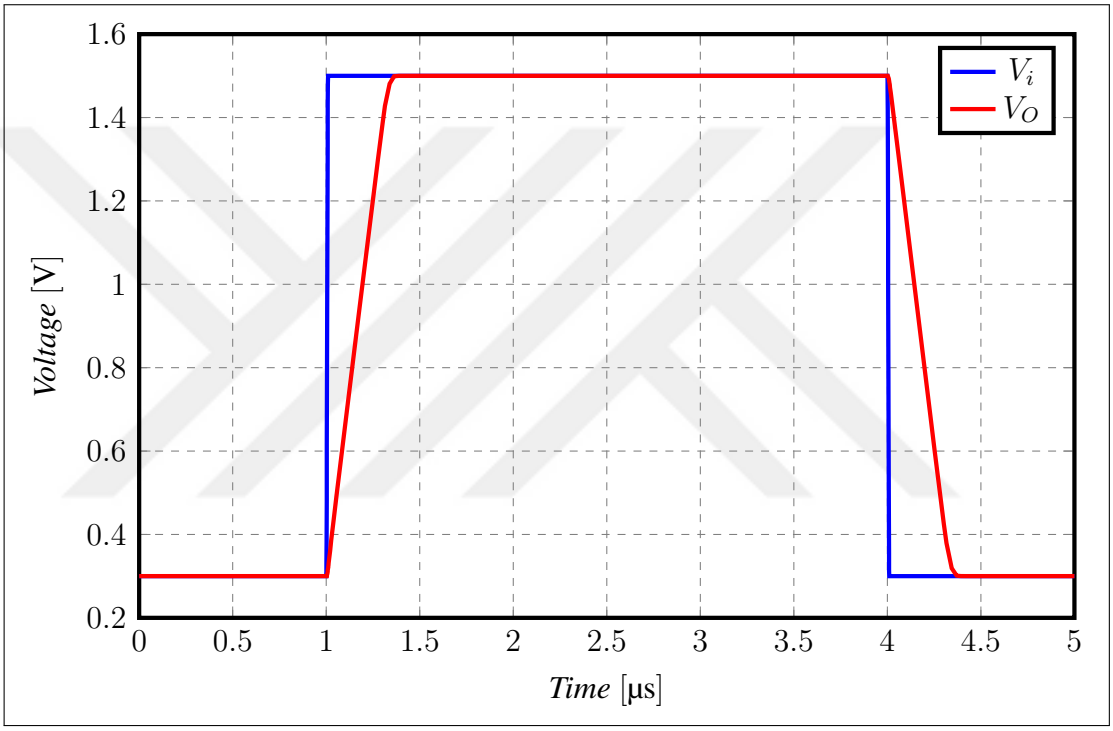

Figure 5.6. Pulse response of the DDA

The output voltage waveform obviously doesn't exhibit any overshoot. This is consistent with the 75.36 °-phase margin measured in stability simulation. Pulse signal applied between 0.3 V to 1.5 V is close to the DDA's range limits. It is obvious from output waveform that the circuit performs as intended even at the limits of its operating range. Slew rate is measured as 3.65 V/µs. These results are not to be compared with anything in the design because we didn't take slew-rate into account.

5.2.4. Monte-Carlo Analysis

Input referred offset is the most important performance metric of our proposed technique. Therefore, it is important to see statistical variation of the offset voltage. Monte-Carlo simulation results with 200 samples with 3-σ distribution are shown in Figure 5.7.

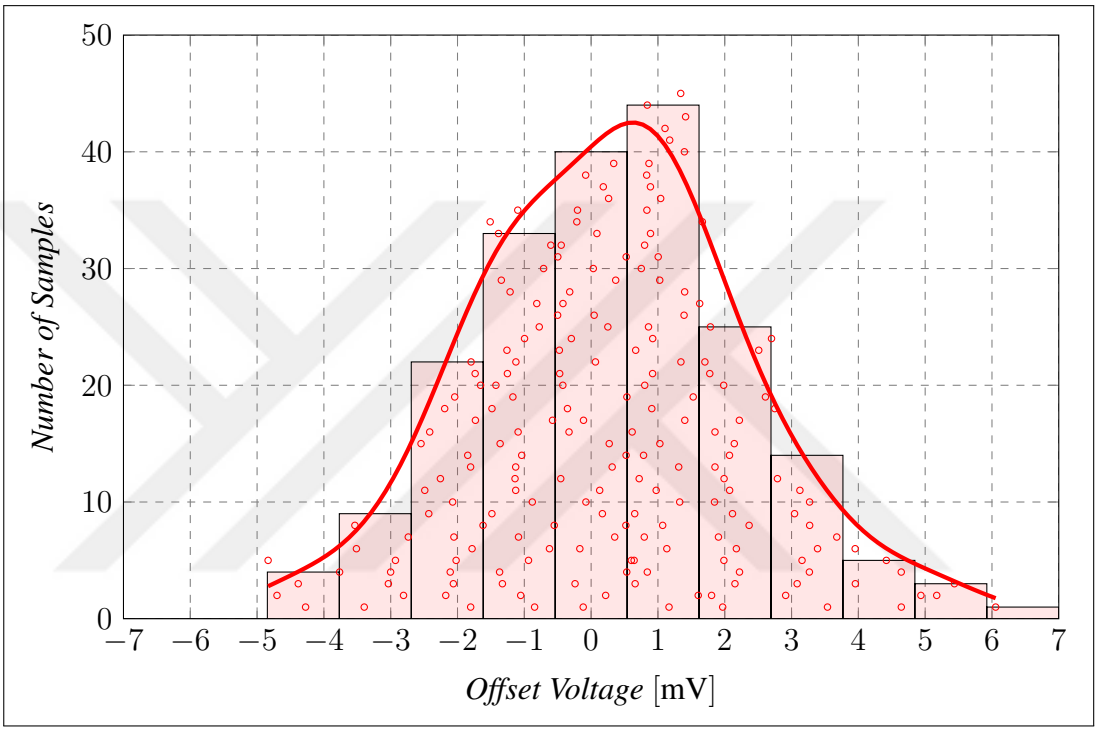

Figure 5.7. Monte-Carlo simulation results of the offset voltage

The statistical data is provided by foundry and we perform a DC operating point analysis as we did in Section 5.2.1 to observe offset voltage at common-mode. Please note that offset voltage corresponds to potential difference between the non-inverting input and inverting inputs. The offset voltage varies between -6 mV and 6 mV. Mean value of the offset is found as 270 µV and standard deviation is 2 mV. We will use this values while simulating auxiliary inputs.

Let's examine that our auxiliary inputs works properly given in Figure 3.9. To do that, we will perform DC sweep analysis to the input voltage V_N. Firstly, we will apply some input referred offset to non-inverting input, V_+, which are -5 mV and +5 mV. Then we will sweep V_N to cancel offset voltage. The simulation results are given in Figure 5.8 below.

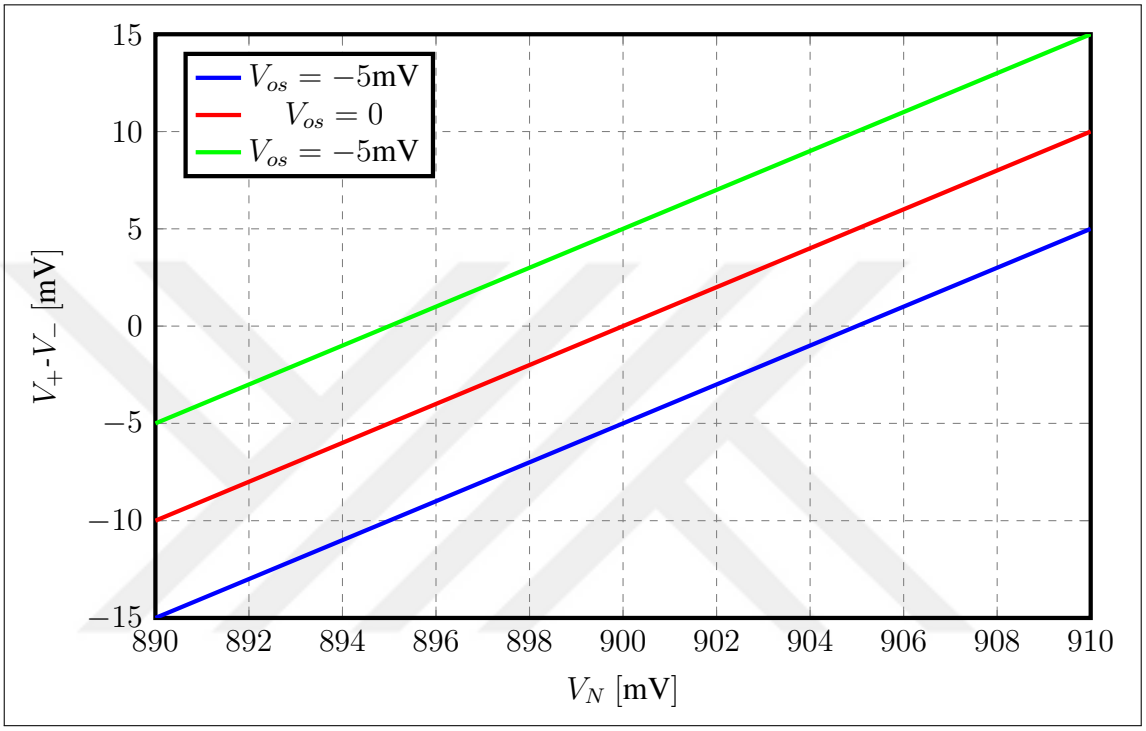

Figure 5.8. Trimming auxiliary inputs of the DDA

From the simulation results, we can say that offset trimming works properly. There is a linear relationship between offset and auxiliary input difference. We can change sensitivity of auxiliary inputs by changing aspect ratio of auxiliary drivers M_{N1a} and M_{N1a} given in Figure 3.9.

5.2.5. DDA Specification Summary

We have designed a DDA to match our design specifications. Firstly, we determined DC operating points and operating range. After that, we have verified AC behaviour of DDA and found stability parameters. Then, we have verified start-up behaviour of the beta-multiplier current reference and observe pulse response of the unity-gain configuration. Finally, we have performed Monte-Carlo simulation to see the statical distribution of the offset voltage and trim the DDA with auxiliary inputs to cancel worst case offset voltages. A summary of the verification result is given in Table 5.5 below.

Table 5.5. Specification summary of the DDA

$V_{O(min)}$	0.3 V
$V_{O(min)}$	1.5 V
Tail Current	4 µA
Power Dissipation	-30 µW
A_d	13.48k (V/V)
GBW	6.98 MHz
PM	75.36 °
Slew-Rate(low-to-high)	3.65 V/µs
Slew-Rate(high-to-low)	-3.65 V/µs

5.3. SHIELDING TECHNIQUE VERIFICATION

We finally simulate our proposed technique with the DDA designed in Section 5.2. and we first verify sinusoidal response of the circuit. This type of input waveform is used to verify correct S/H circuit working principle. After that we examine hold time of the circuit with three different input voltages 0.3 V, 0.9 V and 1.5 V. Finally we test the how temperature response. These simulations are performed with the non-overlapping clock generator circuit that we designed in Section 4.2 to supply clocks to the system.

5.3.1. Sinusoidal Response

We applied a sinusoidal input signal of 100 Hz frequency and a clock signal of 400 Hz frequency with 50 % duty cycle. Simulation results are given in Figure 5.9 below.

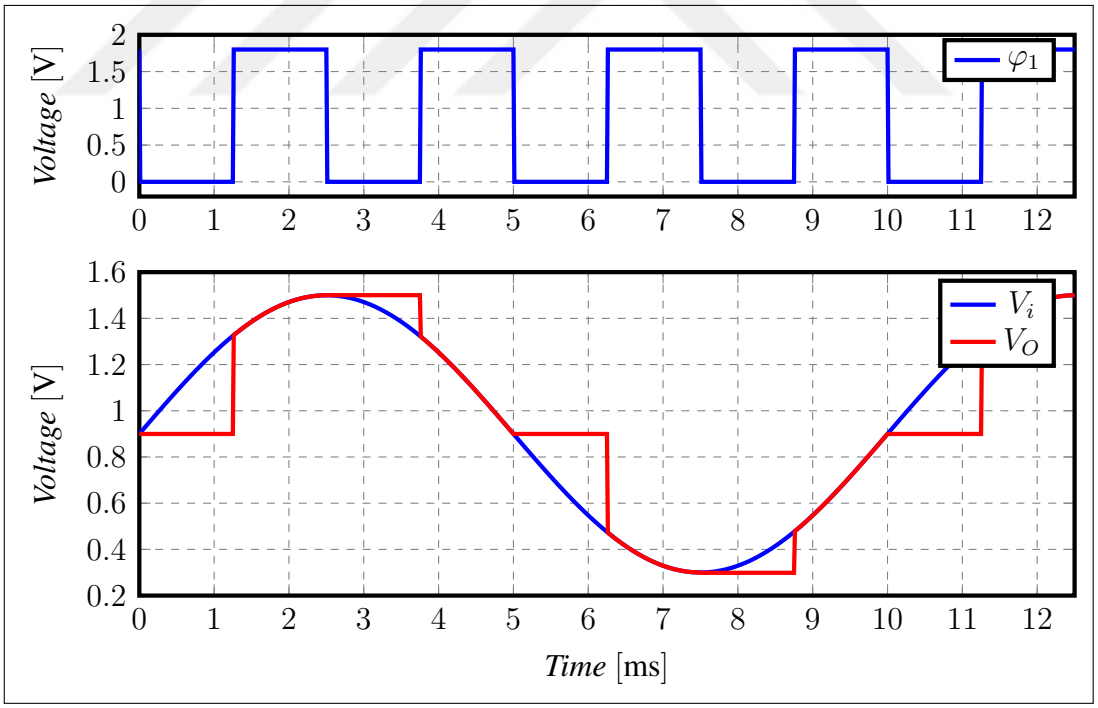

Figure 5.9. Sinusoidal response of the proposed S/H circuit

We can observe sampling phase where $\varphi_1 = 1$ and holding phase where $\varphi_1 = 0$. The sinusoidal signal is applied to operate at the borderline of saturation where the limits of DDA's output range are reached.

Output follows input at sampling phase as expected and the circuit holds sampled value along holding phase. This simulation verified normal operation of S/H circuit.

5.3.2. Maximum Hold Time Analysis

Another simulations is performed for observing how long the proposed S/H circuit with shielding technique can hold voltage. In order to observe maximum hold time at room temperature we perform transient analysis with three different input voltages as mentioned before. These voltages are constant along all the simulation. φ_1 is applied as logic-1 at the very beginning of the simulation and kept logic-0 rest of the simulation. We assume that no offset voltage present in this simulation. Figure 5.10 show the output voltage with different input voltages. Note that the simulator settings needs to be adjusted in low current simulations. These setting are *gmin* and *iabstol* that set to $10^{-}24$ and $10^{-}18$ respectively. They are available in most of the simulators. *Spectre* uses *gmin* for convergence by putting resistors to the ground for each node. We are dealing with very low leakages so we need to set these values very low to prevent false leakage values.

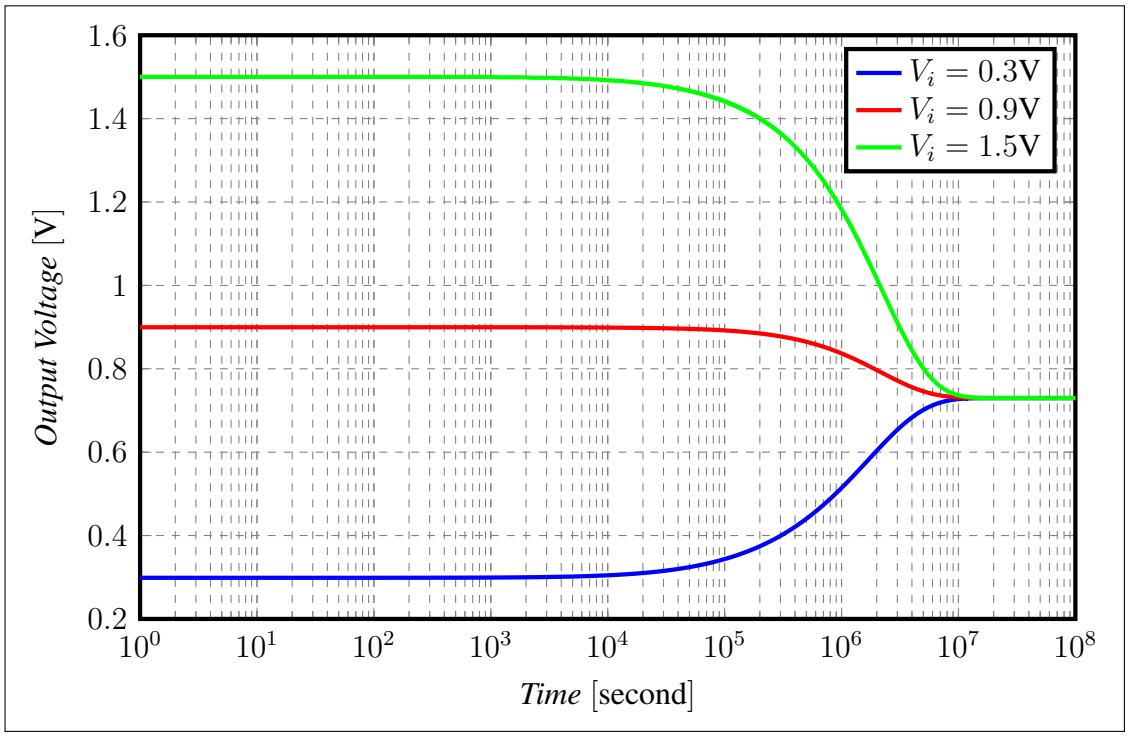

Figure 5.10. Hold time analysis of the proposed S/H circuit

From the results, we can see that voltage on capacitor is starting to decay around 2 ks which approximately equals 33 hours. Let's examine the total leakage current that flows through the capacitor in Figure 5.11.

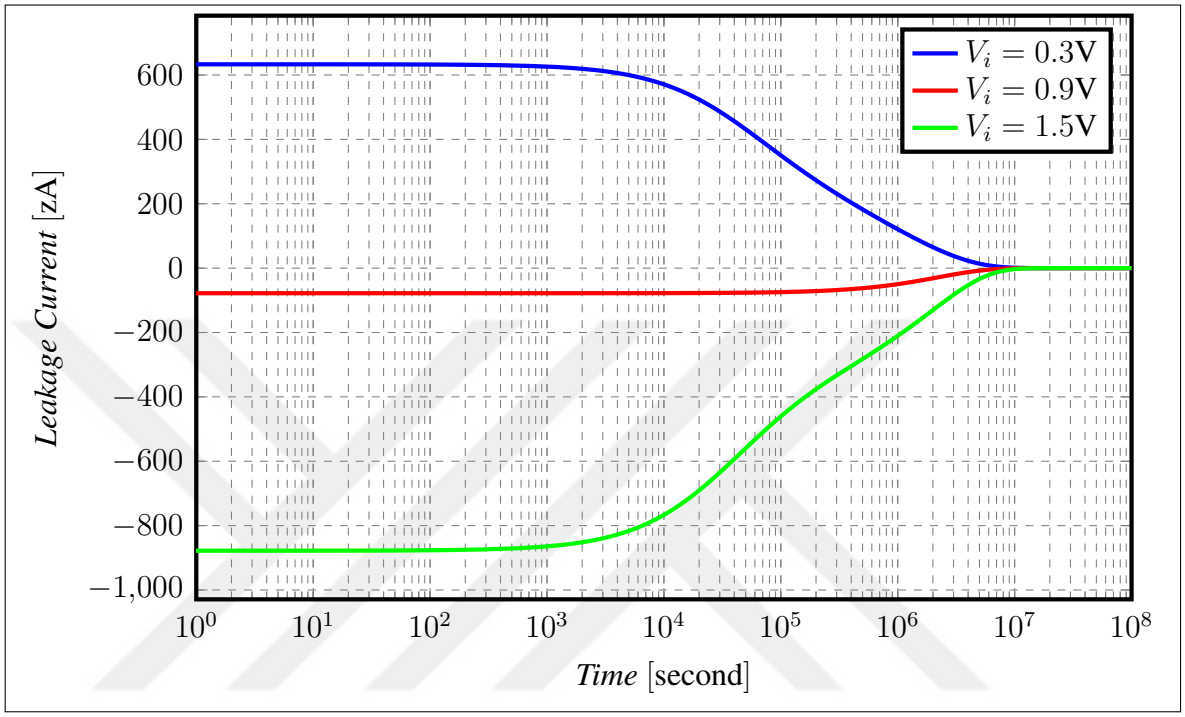

Figure 5.11. Leakage current analysis during hold time

The leakage current is measured at holding period where output voltage still not decayed. The measured values are given in Table 5.6.

Table 5.6. Leakage current results of the proposed S/H circuit

V_i	Leakage Current
0.3 V	633 zA
0.9 V	-78 zA
1.5 V	-877 zA

In order to ensure that we have that small of leakage, of course the proposed circuit needs to be fabricated and tested properly.

5.3.3. High Temperature Analysis

Let's examine our circuit's behaviour at different temperature. We perform same simulation at 100 °C to examine circuit's behaviour at high temperatures. Figure 5.12 shows the output voltages with different input voltages at 100 °C.

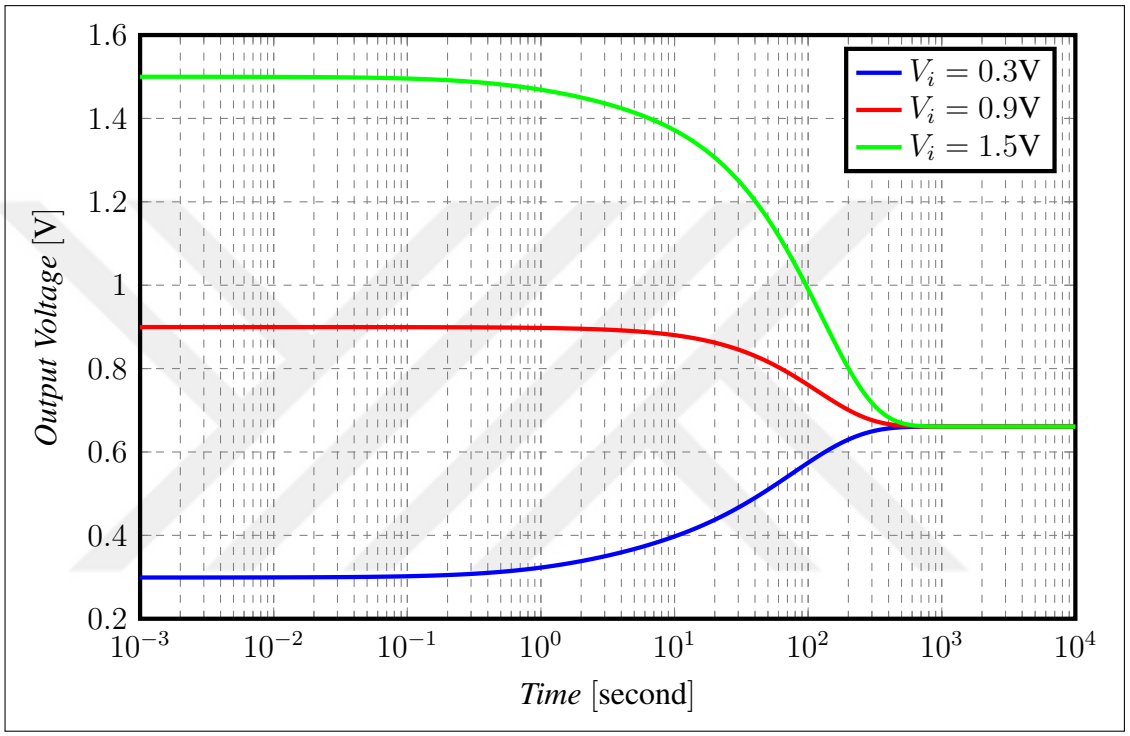

Figure 5.12. Hold time analysis of the proposed S/H circuit at 100 °C

It is obvious that even at high temperatures, circuit has approximately 1 s hold time. Therefore, the proposed circuit can be used at low frequencies at high temperatures where holding period is not higher than 1 s. Let's check the total leakage current presented in Figure 5.13.

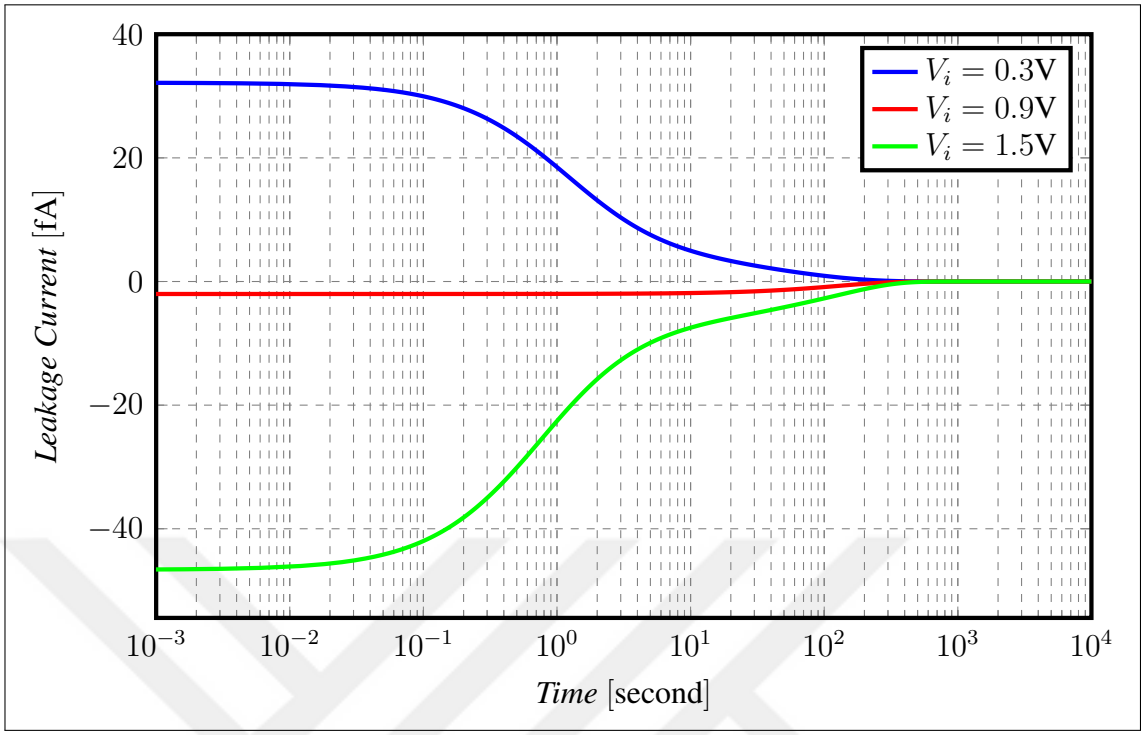

Figure 5.13. Leakage current analysis during hold time at 100 °C

The measured values are given in Table 5.6 below.

Table 5.7. Leakage current results at 100 °C

V_i	Leakage Current
0.3 V	32.1 fA
0.9 V	2 fA
1.5 V	-46.6 fA

As observed from simulations, output is merging at some voltage no matter what input voltage is. This is the point that theoretically gain error and systematic offset voltage of DDA cancels each other, which means V_O and V_C equals to each other. At that point, leakage current is zero. This is not important for our application but it is an interesting conclusion that we can actually mirror voltage at this point with 100 % accuracy.

6. CONCLUSION

In analog IC design, sampling and holding circuits is the very first step of analog to digital signal conversion. Sampling data at low frequencies and high temperatures becomes problem for designers because of leakage currents of switches. There are many techniques in the literature to deal with the leakage-current problem. Some of them are physical solutions but they are hard to implement in CMOS process. Topological solutions are explained in detail and yet they are also difficult to design. We proposed the *"shielding"* technique to reduce leakage currents. We have used *UMC L180 Mixed-Mode/RF* technology for design and *Cadence Spectre* for simulations.

The main idea is to equalize source, drain and bulk potentials of the switches to reduce leakage current. Proposed technique requires two non-overlapping clock signals with no phase relation and one simple DDA design. DDA is used to compensate for the offset voltage of the buffer in order to mirror capacitor voltage more accurately. Designing DDA and non-overlapping clock generator is much more simpler than the techniques proposed in the literature. Minimum 1 aA leakage current and 2 ks hold time achieved. We have managed to get 1 s hold time at 100 °C.

In summary, the *"shielding"* technique can be used in various applications. As we have mentioned, biological signals require long hold time during data conversion process. This problem can be solved with *"shielding"* technique. Moreover, leakage currents in high temperature applications lead to severe problems. Our technique reduces leakage currents significantly even at high temperatures.

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APPENDIX A: VERILOG-A OPAMP MODEL

```
`include "constants.vams"
`include "disciplines.vams"
module OPAMP(Vp,Vn,Vdd,Vss,Vo);

input Vp,Vn;
inout Vo,Vdd,Vss;
electrical Vp,Vn,Vo,Vdd,Vss;
electrical Vcd_in, Vcd, Vcnd_in, Vcnd, Vo1, gnd;
ground gnd;
branch (Vp,Vn) Vin; // ------------------------------ Differential Input Voltage
parameter real Rin = 10T;  // ------------------------ Input Resistance
parameter real Rout = 50; // ------------------------- Output Resistance
parameter real Ad0 = 10k; // ------------------------- Open-Loop Gain
parameter real GBW = 5M;  // ------------------------- Gain-Bandwidth Product
parameter real fnd = 20M; // ------------------------- Non-Dominant Pole Frequency
parameter real Offset = 0 from(-10m:10m); // --------- Input referred Offset Voltage;
parameter real Vcomp = 300m; // ---------------------- Output Complience Limit From Vss and Vdd
parameter real DIR = 200m from[0:inf); // ------------ Differential Input Range
localparam real fd = GBW/Ad0; //  -------------------- Dominant Pole Frequency
localparam real SR = `M_TWO_PI * GBW * DIR; // ------- Slew-Rate
localparam real wd = `M_TWO_PI*fd;  // --------------- Radial Frequency of Dominant Pole
localparam real wnd = `M_TWO_PI*fnd; // -------------- Radial Frequency of Non-dominant Pole
localparam real rd = 1;
localparam real cd = 1/(wd*rd);
localparam real rnd = 1;
localparam real cnd = 1/(wnd*rnd);
localparam real Imax = SR*cd*rd/Ad0; // -------------- Slewing Current
real qcd, qcnd; // ----------------------------------- Pole-Capacitor Charges
real Ad,w; // ---------------------------------------- Soft Open-Loop Gain

analog
  begin
    V(Vin) <+ I(Vin) * Rin; // ----------------------- Input Stage
    if(V(Vin) > DIR) V(Vcd_in) <+ Imax; // ----------- DIR Limited Slew-Rate
    else if(V(Vin) < -DIR) V(Vcd_in) <+ -Imax;
    else V(Vcd_in) <+ V(Vin)+Offset; // -------------- Buffer

    I(Vcd_in,Vcd) <+ V(Vcd_in,Vcd)/rd; // ------------ Dominant Pole
    qcd = V(Vcd)*cd;
    I(Vcd) <+ ddt(qcd);
    V(Vcnd_in) <+ V(Vcd); // ------------------------- Buffer
    I(Vcnd_in,Vcnd) <+ V(Vcnd_in,Vcnd)/rnd; // ------- Non-Dominant Pole
    qcnd = cnd*V(Vcnd);
    I(Vcnd) <+ ddt(qcnd);
    // ---------------------------------------------- Variable Open-Loop Gain Between Rails
    Ad = 0.5*Ad0*(tanh((V(Vo)-(V(Vss)+Vcomp))/(0.125*Vcomp))-tanh((V(Vo)-(V(Vdd)-Vcomp))/(0.125*Vcomp)))+1u;
    w = (V(Vdd)-V(Vss))/(4*Ad)+1n; // ---------------- Limitting Output Voltage with Slew-Rate
    V(Vo1) <+ 0.5*((V(Vdd)+V(Vss))+(V(Vdd)-V(Vss))*tanh(V(Vcnd)/(2*w)));
    I(Vo1,Vo) <+ V(Vo1,Vo)/Rout; // ------------------ Output Stage
  end
endmodule
```