

# DESIGN OF SELECTABLE GSM-BAND RFIC FILTER



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Submitted to Graduate School of Natural and Applied Sciences  
in Partial Fulfillment of the Requirements  
for the Degree of Master of Science in  
Electrical and Electronics Engineering

Yeditepe University

2019

## DESIGN OF SELECTABLE GSM-BAND RFIC FILTER

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DATE OF APPROVAL: ..../..../2019

## ACKNOWLEDGEMENT

First of all, I wanted to thank my supervisor Associate Professor Serkan Topalođlu for his help, guidance and support throughout my Master's and Bachelor's degrees. During my education, my main guide was his advice, lecture notes, and feedbacks. Also, I deeply appreciate Anil Özdemirli and Ömer Orberk for their assistance; they helped me to solve even the toughest problems with their technical experience and moral support. On a final note, I would like to sincerely thank my friends Ali Arda Yıldız, Aydın Köksal Ardal, İlsu Şeren, Okan Şen, Aslihan Genc, Utku Tuncel and Tugba Haykır for their continuous support.

Thank you,

Ali Baran

## ABSTRACT

### DESIGN OF SELECTABLE GSM-BAND RFIC FILTER

Nowadays, an increasing number of applications use radio frequency (RF) for communication and require various RFICs (Radio Frequency Integrated Circuits) to meet the relevant needs. Since electronic products have widespread use, the environment has led to an increase in electromagnetic radiation; this increases the need for RFICs that offer improved communication reliability. RFICs offer high performance with low noise, low cost and high mobility in high-frequency domain circuits.

RFICs generally use silicon-based technologies such as metal oxide semiconductors (MOS) and silicon-germanium for implementation (Si-Ge). However, RFICs should not be limited to silicon-based technologies; for example, Ga-As substrate which is a compound of Gallium and arsenic can also be classified as RFICs.

Typical RFICs typically work with in-chip circuit elements. However, because of the high-quality factor in the chip, on-chip circuit elements can also be used. These lumped elements are effective when high quality factor is needed. In addition, the use of lumped elements can withstand high voltages. Lumped elements also allow going beyond the inductor values that foundry has given to the user.

The integration technology has been reduced to millimeter range, this causes an obvious decrease in the designed circuit. The aim of the thesis is to create a novel design for filters on the market and reduce size in IC scale and make the bands are selectable.

According to the literature research, a filter that operates at GSM bands; GSM 900 and GSM 1800 with selectable center frequency was not found. However, there are various papers including GSM band filters with dual center frequencies. By making the center frequency selectable, the novelty factor is provided to the specifications of the design. Also, no IC sized filter that is operating in the GSM bands had been found in the literature research. Hence, reducing the dimensions of the filter to the IC scale is adding value to the thesis. Reducing the dimensions to the IC scale also decreases the weight of the prototype. Decreasing the weight of the prototype allows to be more portable and makes it possible for the filters to be used in designs where even the smallest weight changes are crucial.

## ÖZET

### GSM BANT RFIC BANT GEÇİREN FİLTRE TASARIMI

Günümüzde, artan iletişim uygulamaları için radyo frekansı (RF) kullanır ve ilgili ihtiyaçları karşılamak için çeşitli RFIC'leri (Radyo Frekansı Entegre Devreler) gerektirir. Elektronik ürünler artık her yerde olduğu için, çevrede elektromanyetik radyasyonun artmasına neden olurlar. Bu durum, gelişmiş iletişim güvenilirliği sunan RFIC'lere olan ihtiyacı artırır. RFIC'ler genellikle MOS ve Silikon Germanyum gibi silikon tabanlı teknolojileri kullanılmaktadır, fakat RFIC sadece silikon tabanlı teknolojilere sınırlandırılmamalıdır. Örneğin Galyum Arsenik (Ga-As) alt tabakalar da RFIC olarak sınıflandırılabilir. Bu bileşimler düşük gürültü, düşük maliyet ve yüksek mobilite ile yüksek performans sunarlar. Tipik RFIC'lerde, özellikle düşük frekanslarda genellikle ayırık devre elemanları kullanır. Bu ayırık elemanlar genellikle etkilidir ve hatta kullanılması gereklidir. Ayırık elemanların kullanılma nedenleri arasında kırılma gerilimlerinin yüksek olması vardır. Ayrıca ayırık eleman kullanmak üretim evinin tasarımcıya sağladığı bobin değerlerinin dışına çıkabilmesine olanak verir. En önemlisi ise ayırık eleman kullanmak bobinin kalite faktörünün yüksek tutulmamasına neden olur. Bu durum devrenin kalite faktörünü kırk içerisindedeki kullanılan bobin değerleri ile ulaşılamayacak seviyelere çıkartabilir.

Piyasada değişken isterlere sahip birçok ayırık elemanlı filtre bulunmaktadır. Tümleştirme teknolojisi ise milimetre seviyelerine inmiştir. Bu durum, tasarlanan devre alanında önemli bir azalmaya neden olur. Tezin temel amacı, piyasadaki filtrelerin özgün tasarımını yapmak, IC ölçeğinde büyüklüğü azaltmak ve bantları seçilebilir hale getirmektir.

Literatür taramasında GSM bantlarında çalışan ve merkez frekansı seçilebilen filtre bulunamamıştır. Bunun yanında, çeşitli makalelerde, çift merkez frekanslı, GSM bantlarında çalışan filtrelere rastlanmıştır. Merkez frekans seçilebilir hale getirilerek tasarıma özgünlük katmıştır. Literatür araştırmasında, GSM bantlarında çalışan ve IC boyutlarında filtrelere de rastlanmamıştır. Bu sayede, filtrenin boyutları IC ölçeğine küçültülerek teze bir değer takılması hedeflenmiştir. Prototipin boyutlarını IC ölçeğine küçültmek, aynı zamanda ağırlığının da azaltılmasını sağlamıştır. Böylelikle, prototipin kullanılabileceği alanlar çoğalmıştır.

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## LIST OF SYMBOLS/ABBREVIATIONS

EM:	Electromagnetic
$f_0$ :	Center frequency
GaAs:	Gallium- arsenide
GHZ:	Giga hertz
GSM:	Global system for mobile communication
GTF:	Gate transfer function
IL:	Insertion loss
IR:	Return loss
MHz:	Mega hertz
MSUB:	Microstrip substrate
pHEMT:	Pseudomorphic high electron mobility transistor
RFIC:	Radio frequency integrated circuit
Q:	Quality factor

## 1. INTRODUCTION

It is noteworthy that for the dual-band GSM operators in the world, the frequency range allocated from the 900 MHz band does not fall much below 5 MHz. In countries that are not included in the standard GSM band, frequency allocation can be made from the extended GSM band for dual-band networks [1].

It is crucial to filter these two GSM (900 MHz-1800 MHz) bands to operate. Literature research shows that many filters are designed in GSM bands. The most important and challenging part is the reduction in the length of this filter from the range of cm to the range of mm. Besides, the purpose of the designed filter is to reduce the bandwidth, because the low bandwidth increases the quality factor of the circuit. The designed filter will also operate in two frequency bands. One of them is 900 MHz and the other one is 1800 MHz [2]. The band to be used will be selected by the user.

The biggest problem of the RFICs is there are eight components common to two different frequency blocks. These circuit elements make it difficult to create matching circuits and add new losses. Besides, when the layout of the circuit is drawn, parasitic effects will also occur.

Another problem is the inductors which are added to the circuit when designing the circuits in the IC scale because the size of the spiral inductors made in the chip is very large in comparison to the size of the rest of the circuit. This adds an undesirable effect to the outcome of the electromagnetic simulation caused by parasitic capacitive effects that comes from the spiral shapes and losses from the length. Also, these inductors have a low-quality factor and cause a loss in the circuit [3].

As a solution to these problems, the number of components should be kept a minimum. With this method, extra parasitic effects which are the results of the extra components in the circuit will be avoided. Compared to discrete inductors, spiral inductors are bigger in size. The ideal way to reduce the size of the chip is to replace the spiral inductors with discrete ones. With the replacement of inductors, the designer should keep in mind, that the price of the chip will be increased. Replacement of the inductors will also cause the insertion loss to be reduced significantly because discrete inductors have much higher quality factors compared

to spiral inductors. Because of the parasitic capacitor effect of spiral inductors, the center frequency of the filter will shift unintentionally [4]. Since discrete inductors do not couple with the rest of the circuit components, the center frequency will not be affected and this is contrary to the spiral inductors [5].

According to the thesis, switches were used to shift between frequencies. The change in the gate voltage value of switch leads center frequency of the filter to change. This allows the filter to have a tunable center frequency. According to the designed filter, the center frequency of the filter is 900 MHz when the bias voltage is 5 V. When the bias voltage changes; the center frequency of the filter is shifted to 1800 MHz.

An RFIC bandpass filter with selectable center frequency operating in the GSM-Band could not be found in the literature review. Making the center frequency selectable and reducing the size of the filter to IC dimensions has added value to the filter. Furthermore, a comparison of the references and the presented thesis is mentioned. According to the comparison, insertion loss was improved by 1-3 dB and the bandwidth was significantly reduced. Rejections were improved between 10 and 15 dB. In this case the quality factor of the circuit has been developed by the comparator reference circuit quality factor. This reduction in the bandwidth makes the filter more selective. These improvements in specifications have added value to the design.

Microwave filters are the basic elements used in selection in the channel and separated signals in communication systems [7]. There are different filter types to do this. These are low pass, high pass, bandpass, and band-reject filters.

Electrical performance plays an important role in system-level designs. Insertion loss, return loss and slopes in the rejection zone are the three most important properties expected [8].

The band-pass filter is a type of filter that allows frequencies in the desired band range and rejects other frequencies. The design phase small size, low cost and availability of mass production should be considered by designers. In the designed prototype, the terms impedance and frequency are normalized [9]. The prototype design is then converted to the desired frequency range and impedance level [10]. In this section, what is the resonance in electronic circuits and types of resonance will be discussed. In addition, what the quality factor is and how to change the quality factor, will be discussed. Finally, what scattering parameters are and what they are used for will be mentioned.

## 1.1. RESONANCE in ELECTRONIC CIRCUITS

Connection of series and parallel resonant circuits between the source and the load is as shown in Figure 1.1. The series resonant circuit is used when the signal is to be transferred source to the load at the resonant frequency between output and input. The parallel resonant circuit is used when the sign is desired to be filtered.

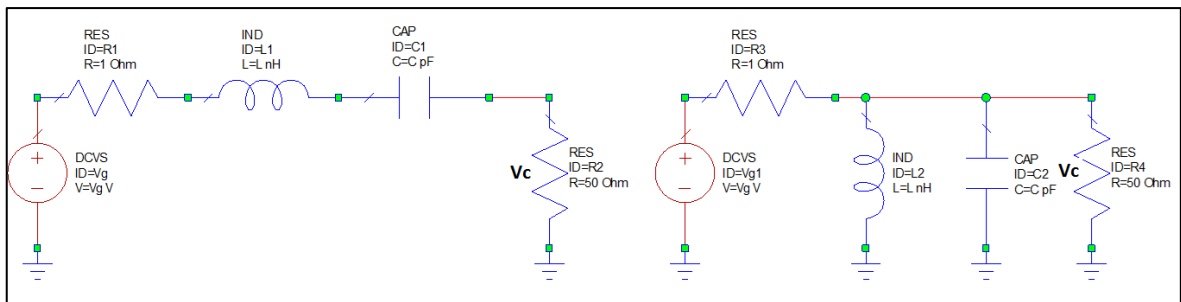


Figure 1.1. (a) Series and (b) parallel resonant circuits formed by LC elements

In a circuit voltage division can be done by a simple impedance addition to the circuit. Referring to the circuit Fig. 2.1, output voltage and input voltage ratio obtained by calculating the parallel-connected LC (X<sub>LC</sub> is considered to be the emplacement of the LC elements in the parallel arm) is expressed as:

$$\frac{V_c}{V_g} = \frac{X_{LC}}{R_g + X_{LC}} \quad (1.1)$$

This ratio, also called the voltage transfer function, can be written in decibels as follows:

$$\frac{V_c}{V_g} = 20 \log_{10} \frac{X_{LC}}{R_g + X_{LC}} \quad (1.2)$$

$\frac{V_c}{V_g}$ : GTF which is the gate transfer function

$R_s$ : Source resistance

$X_c$ : Impedance of the capacitor ( $X_c = \frac{1}{j\omega c}$ )

The GTF of the circuit consisting of the capacitor and resistor given in Figure 1.2 can be written in decibels according to the frequency.

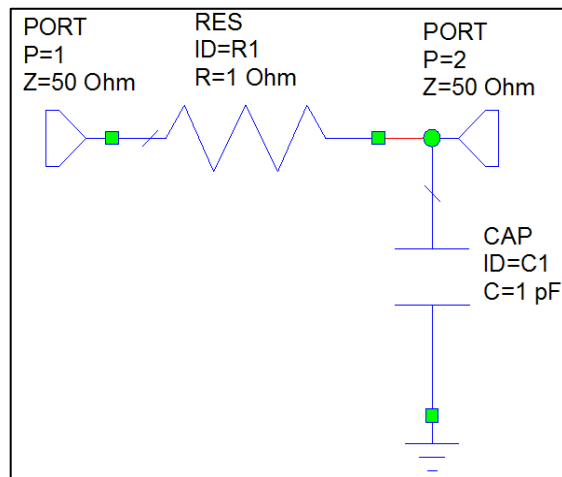


Figure 1.2. A simple RC low-pass filter

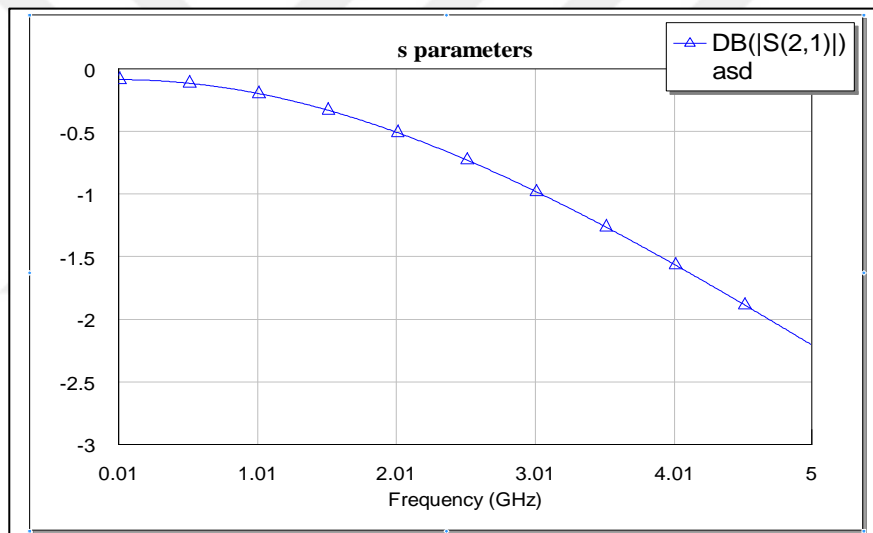


Figure 1.3 Frequency response of RC circuit given at Figure 1.2

From the frequency curve, the insertion loss of the circuit was observed as the frequency increased. So this circuit shows a simple low-pass filter features. If the inductor is replaced with the capacitor instead of the capacitor, the frequency response of this circuit can be found by the following formulas[13].

$$GTF = \log_{10} \frac{X_L}{R_S + X_L} \quad (1.3)$$

$R_S$ : Source resistance

$X_L$ : Inductance impedance

$$X_L = j\omega L$$

Figure 1.4 also shows a simple RL high-pass filter circuit with a load inductor.

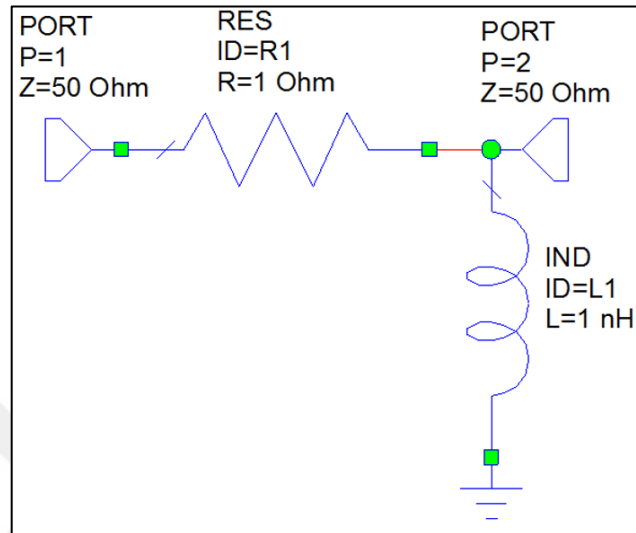


Figure 1.4. A simple RL high-pass filter

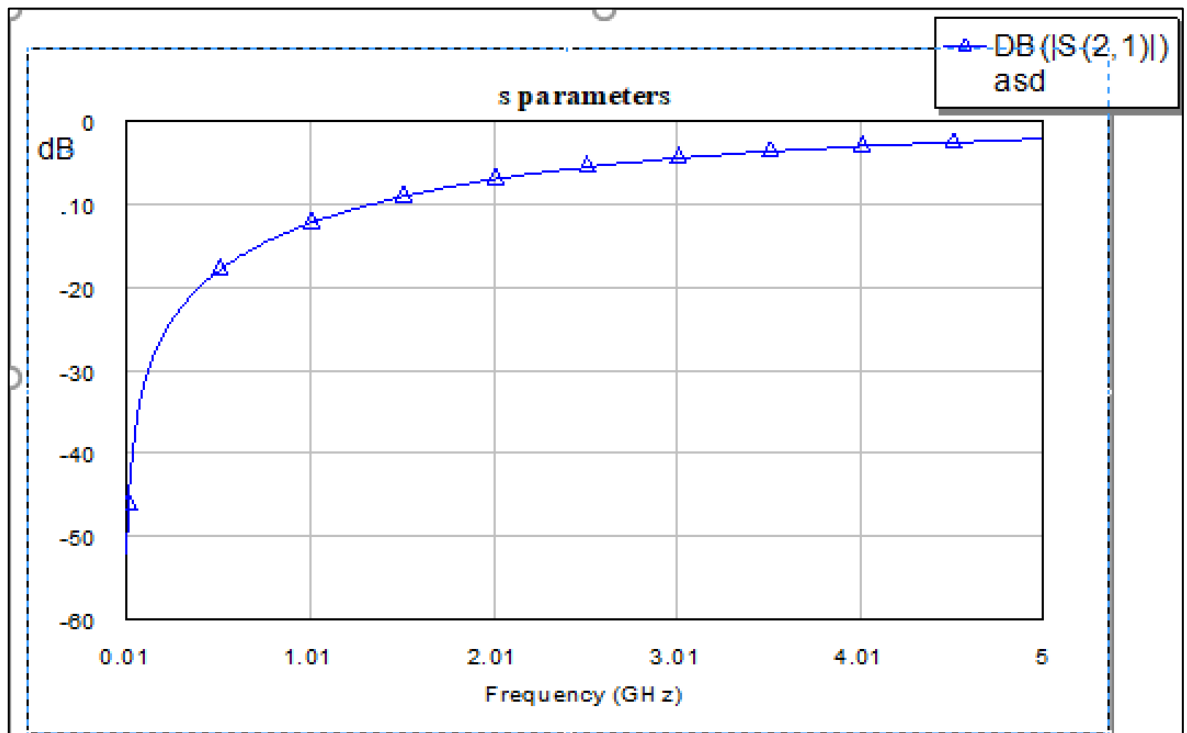


Figure 1.5. Frequency response of RL circuit given at Figure 1.4

This circuit, as shown in Figure 1.5 shows high pass filter feature. The frequency characteristic of the RLC circuit given in Figure 2.5 will be obtained. The equations given below will be used for this purpose [14].

$$V_{out} = \frac{X_{Total}}{R_{in} + X_{Total}} (V_{in}) \quad (1.4)$$

$$X_{Total} = \frac{X_C \cdot X_L}{X_C + X_L} \quad (1.5)$$

$$X_C = \frac{1}{j\omega C} \quad , \quad X_L = j\omega L \quad (1.6)$$

$$X_{Total} = \frac{\frac{1}{j\omega C} (j\omega L)}{\frac{1}{j\omega C} + (j\omega L)} = \frac{\frac{L}{C}}{\frac{1}{j\omega} + j\omega L} \quad , \quad j^2 = -1 \quad (1.7)$$

$$X_{Total} = \frac{j\omega L}{1 + (j\omega L)(j\omega C)} = \frac{j\omega L}{1 - \omega^2 LC} \quad (1.8)$$

If this is put in place in equation 2.4, result will be:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{j\omega L}{1 - \omega^2 LC}}{R_{in} + \frac{j\omega L}{1 - \omega^2 LC}} \quad (1.9)$$

$$\frac{V_{out}}{V_{in}} = \frac{j\omega L}{R_{in} + \frac{j\omega L}{1 - \omega^2 LC}} \quad (1.10)$$



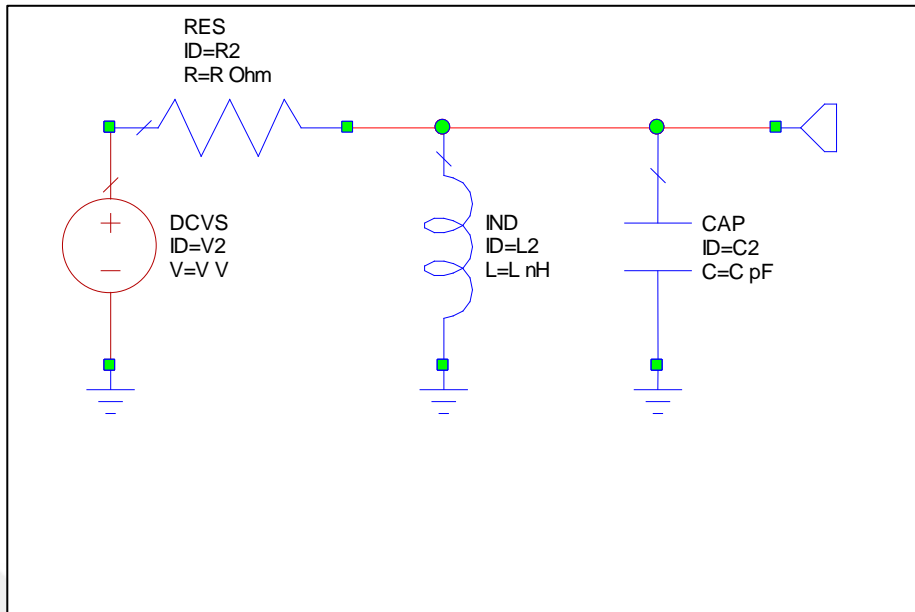


Figure 1.6. Parallel RLC resonant circuit

## 1.2. LOADED Q

In resonant circuits,  $Q$  is defined in different ways, with and without load. Since the definition given in Equation 1.11 belongs to the actual circuit, it is the  $Q$  definition. The loaded  $Q$  value of the resonant circuit depends on the source and load resistors and the qualities of the components. Inductor quality factor is determined as the ratio of the inductance value to the loss resistance in the series arm. The same situation is true for the capacitors. However, series loss resistance is used instead of capacitor equivalent series resistance. This is because the capacitor has the equivalent of both series and parallel loss resistors. The method for the practical design of the resonant circuit, which is given in Figure 1.7 and built in the loaded state but with lossless (ideal) LC elements, is as follows:

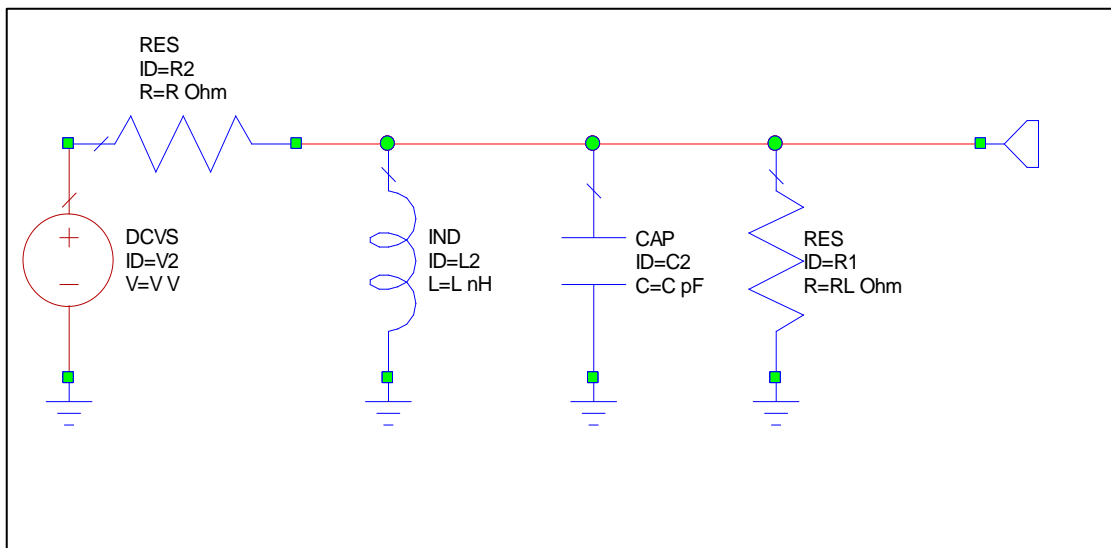


Figure 1.7. Resonance circuit with loaded Q

$$Q = \frac{f_H - f_L}{f_C} \quad (1.11)$$

Firstly, calculate the parallel equivalent ( $R_p$ ) of the source and load resistors of the circuit.

Secondly, calculate the reactance value of the inductance at the resonant frequency using  $R_p$  value and the desired Q value.

Finally, calculate the capacitor value using  $X_L = X_C$  at the resonant frequency.

If the element losses are also taken into account, the series resistors ( $R_s$ ) used in the element equivalents for the resonant circuit design and representing the losses are calculated as the equivalent parallel resistance of the losses of the elements by the series / parallel equivalence transformation.

$$R_p = (1 + Q_e^2)R_s \quad (1.12)$$

Here  $Q_e$  shows the element quality factor and, in the case of both (series and parallel) equivalence,  $Q_e$  is the same and the equivalent reactance value in parallel is calculated as  $X_p = R_p/Q_e$ . If the element quality factor  $Q_e$  is greater than 10,  $R_p = Q_e^2 R_s$  and  $X_p = X_s$  can be used [14].

### 1.3. SCATTERING PARAMETERS

The scattering parameters are defined while using transmitted and reflected waves on the transmission line connecting a high-frequency circuit to an external circuit. To make the definition understandable, consider a two-port circuit connected to the transmission line as shown in Figure 1.8. S-Parameters of the circuit will be defined by using the voltage waves at the connection points. (Transmission lines are not required to define S-parameters. However, in order to observe the waves, a piece of a transmission line is used on both ports.)

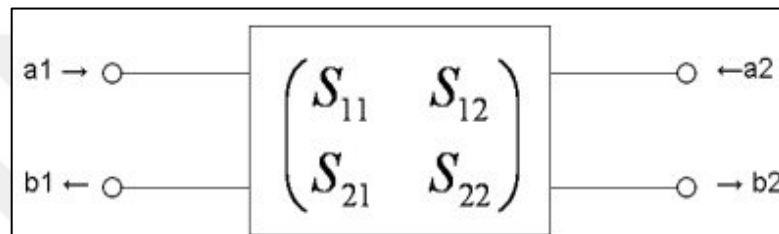


Figure 1.8. Linear two-port microwave circuit

Port voltage and current can be divided into two as transmitted and reflected.

$$V_1 = v_1^+ + v_1^- \quad (1.13)$$

$$I_1 = \frac{1}{Z_0} (V_1 = v_1^+ + v_1^-) \quad (1.14)$$

$$V_2 = v_2^+ + v_2^- \quad (1.15)$$

$$I_2 = \frac{1}{Z_0} (V_2 = v_2^+ + v_2^-) \quad (1.16)$$

$Z_0$  is the impedance of the transmission line characteristic. Microwave circuits are usually 50 ohms. The reflected and transmitted waves in the ports can be found by solving the above equations.

$$V_1^+ = \frac{V_1 + Z_0 I_1}{2} \quad (1.17)$$

$$V_1^- = \frac{V_1 - Z_0 I_1}{2} \quad (1.18)$$

$$V_2^+ = \frac{V_2 + Z_0 I_2}{2} \quad (1.19)$$

$$V_2^- = \frac{V_2 - Z_0 I_2}{2} \quad (1.20)$$

The voltages received from each port and reflected are normalized using the normalization impedance. This normalization impedance is usually selected the same as the characteristic impedance of the line [16].

$$a_{1,2} = \frac{V_{1,2}^+}{\sqrt{Z_0}} \quad (1.21)$$

$$b_{1,2} = \frac{V_{1,2}^-}{\sqrt{Z_0}} \quad (1.22)$$

The power received from each port and reflected (when current and voltage gets maximum values) can be formulated as:

$$P_1^+ = \frac{1}{2} |a_1|^2, \quad P_2^+ = \frac{1}{2} |a_2|^2 \quad (1.23)$$

$$P_1^- = \frac{1}{2} |b_1|^2, \quad P_2^- = \frac{1}{2} |b_2|^2 \quad (1.24)$$

Scattering parameters using normalized voltage waveforms can be defined as follows:

$$b_1 = s_{11} a_1 + s_{12} a_2 \quad (1.25)$$

$$b_2 = s_{21} a_1 + s_{22} a_2 \quad (1.26)$$

The above equations can be written in matrix form:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (1.27)$$

#### 1.4. ORGANIZATION OF THESIS

This thesis discusses the design procedure of on chip integrated band-pass filter design, including the characterization and design of RF BPF using PP10 technology on GaAs substrate. The simulations are executed by AWR.

The electrical properties of the targeted filter are given in Table 1.1.

Table 1.1 Targeted specifications of the thesis

	<b>@0.9 GHz</b>	<b>@1.8 GHz</b>
Center Frequency ( $f_c$ )	900 MHz	1800 MHz
Insertion Loss	7 dB	8 dB
Return Loss	18 dB	15 dB
3 dB Bandwidth	10%	10%
Frequency Control Voltage (channel on)	-1 V	-1 V
Frequency Control Voltage (channel off)	5 V	5 V
High Side Rejection (Rejection > 20 dB)	$1.25 * f_c$	$1.05 * f_c$
Low Side Rejection	$0.6 * f_c$	$0.85 * f_c$

As a result of literature review, the specifications of the projects [42, 44, 45] were utilized. In this way, the specifications presented in Table 1.1 were determined.

Chapter 2 is presents on filter topologies and filter design procedures. Chapter 3 focused fabrication technologies. Chapter 4 introduces RFIC bandpass filter design method. Chapter 5 presents the designs and simulations. Chapter 6 is conclusion.

## 2. MICROWAVE FILTER DESIGN

Filters are the selective structures that operate at a certain frequency where they allow the desired signals and reject the rest. Selected low or high cut-off frequencies determine the bandwidth of the filter. Four types of filter topologies exist which are low pass, high pass, bandpass, and band-reject (stop) filter topologies. Bandpass filters allow selected signals to pass and weaken the unwanted signals. The frequency response of an ideal bandpass filter should be rectangular. In this chapter, the three known filter topologies which are Butterworth filter type, Chebyshev filter type, and Cauer filter type will be explained.

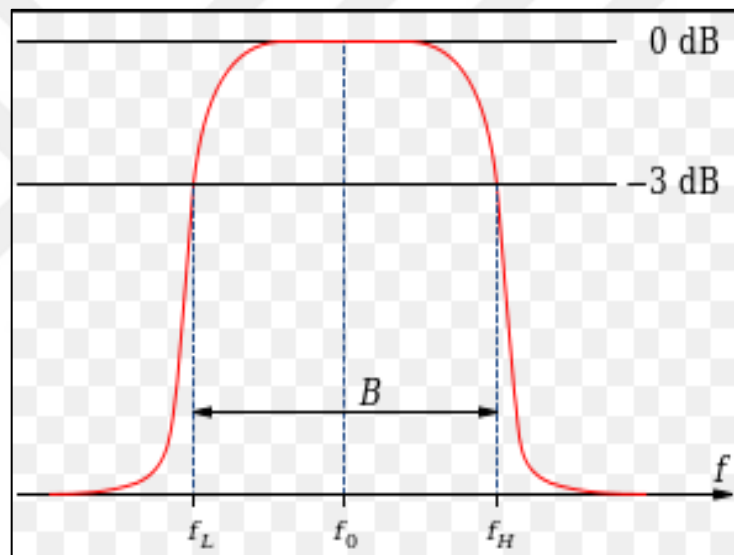


Figure 2.1. Bandpass filter [46]

$$BW = f_h - f_l \quad (2.1)$$

$$f_0 = \frac{f_h - f_l}{2} \quad (2.2)$$

### 2.1. BUTTERWORTH FILTER

Butterworth filter is described as the maximum flat magnitude filter. It was first published in 1930 by Stephen Butterworth in his article "On the Theory of Filter Amplifiers". There are no ripples in the stopband and the transition band [17]. It has a maximum flat frequency

response within the passband and approaches the zero within the stopband. In contrast to other filters, Butterworth maintains its shape in the frequency amplitude curve, except for the hard steep in the stopband when the order of the filter increases. Because the Butterworth filter has a wider transition band than the Chebyshev Filter and Elliptic Filters, it needs high order to ensure that the stopband properties are correctly applied. It has a more linear frequency response than the Chebyshev Filter and Elliptic Filter.

Table 2.1 Butterworth low-pass filter prototype

<b>n</b>	<b>C<sub>1</sub></b>	<b>L<sub>2</sub></b>	<b>C<sub>3</sub></b>	<b>L<sub>4</sub></b>	<b>C<sub>5</sub></b>	<b>L<sub>6</sub></b>	<b>C<sub>7</sub></b>
2	1.414	1.414					
3	1.000	2.000	1.000				
4	0.765	1.848	1.848	0.765			
5	0.618	1.618	2.000	1.618	0.618		
6	0.518	1.414	1.932	1.932	1.414	0.518	
7	0.445	1.247	1.802	2.000	1.802	1.247	0.445
<b>n</b>	<b>L<sub>1</sub></b>	<b>C<sub>2</sub></b>	<b>L<sub>3</sub></b>	<b>C<sub>4</sub></b>	<b>L<sub>5</sub></b>	<b>C<sub>6</sub></b>	<b>L<sub>7</sub></b>

The equation of the Butterworth Filter is equation (2.3):

$$A(dB) = 10 \log\left(1 + \left(\frac{\omega}{\omega_c}\right)^{2n}\right) \quad (2.3)$$

$\omega$ : desired bandwidth

$\omega_c$ : cut-off frequency of the filter

$n$ : number of elements of the filter

If equation (2.3) was developed in a certain frequency range for different grade filters, Figure 2.2 was revealed.

The 5th degree Butterworth filter reaches 30 dB attenuation at twice the cut frequency of the filter.

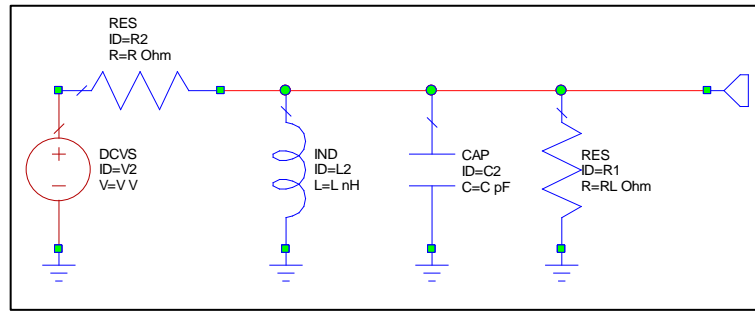


Figure 2.2. RLC resonant circuit starts with series capacitor

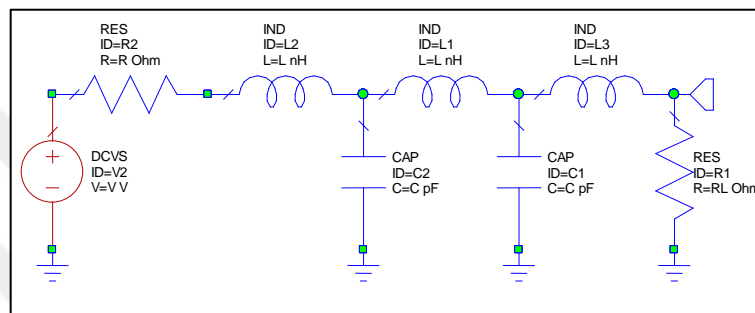


Figure 2.3. RLC resonant circuit starts with series inductor

## 2.2. CHEBYSHEV FILTER

Chebyshev filters are kind of high-Q filters. Due to the slope used in electronics, it is a type of filter that suppresses adjacent frequencies much better [18]. The Chebyshev filter draws a very steep slope at the upper and lower cut frequency and is, therefore, the reason for the preference for designers. However, it has a disadvantage that the gain is not flat in the passband frequencies. Due to the changing gain, the bode curve shows ripples in the passband. Attenuation of Chebyshev filters is given at equations (2.4), (2.5), (2.6) and (2.7).

$$A(dB) = 10 \log(1 + \varepsilon^2 C_n^2(X')) \quad (2.4)$$

$$X' = X \cosh\left(\frac{1}{n} \cosh^{-1}\left(\frac{1}{\varepsilon}\right)\right) \quad (2.5)$$

$$X = \frac{f}{f_c} \quad (2.6)$$

$$\varepsilon = \sqrt{10^{RdB/10} - 1} \quad (2.7)$$



$C_n^2(X')$  : Chebyshev polynomial,

$R_{dB}$  : Passband ripples in dB

$n$  : Order of filter

$\mathcal{E}$  : Parameter that defined at equation (2.7)

cosh : Hyperbolic cosine

$\frac{f}{f_c}$  : Desired frequency over cut-off frequency

Table 2.2. Chebyshev low-pass filter prototype with 0.1 db ripple

<b>n</b>	<b><math>R_g/R_y</math></b>	<b><math>C_1</math></b>	<b><math>L_2</math></b>	<b><math>C_3</math></b>	<b><math>L_4</math></b>
2	1.355	1.209	1.638	1.638	
	1.667	0.733	0.733	2.489	
	2.000	0.560	0.560	3.054	
3	1.000	1.433	1.594	1.433	
	0.600	1.648	1.017	2.603	
	0.200	3.942	0.317	7.850	
4	1.355	0.992	2.148	1.585	1.341
	1.667	0.576	2.730	1.185	2.243
	2.000	0.440	3.227	0.967	2.856
<b>n</b>	<b><math>R_y/R_g</math></b>	<b><math>L_1</math></b>	<b><math>C_2</math></b>	<b><math>L_3</math></b>	<b><math>C_4</math></b>

### 2.3. CAUER (ELLIPTIC) FILTER

Elliptic filters are also known as the Cauer Filter after Wilhelm Cauer. Elliptic filters are used in many applications that require a fast transition between the passband and the stopband. Elliptic filters have a significant disadvantage, even if they have the fastest transition, they cause ripples in the passband and stopband. Very fast transitions result in a sharper filter structure and a more selective filter within the band [19].

The elliptic filter is characterized by the ripple in both pass-band and stop-band. The height of the ripple can be changed by the designer during the design stage. When ripples at the rejection band selected as zero filters behave like a Chebyshev type. If the ripples in the stopband and the passband selected as zero, the filter look like a Butterworth filter [20].

## 2.4. FREQUENCY-IMPEDANCE SCALING

After calculating the low pass prototype values, the next step is used to convert prototype circuits into a designable circuit. The circuit is located between the 1-ohm source and load resistance. The transformation of the components is made according to the following formula:

$$C = \frac{C_n}{2\pi f_c R} \quad (3.8)$$

$$L = \frac{RL_n}{2\pi f_c} \quad (3.9)$$

$C$ : Last capacity value

$L$ : Last inductor value

$C_n$ : Low-pass prototype element value

$L_n$ : Low-pass prototype element value

$R$ : Load resistance

$f_c$ : Cut-off frequency

- It is realized by following the following steps for low pass filter design:
- Firstly, define how much attenuation is required for the desired frequency value.
- Normalize the desired frequency to its exact frequency  $f/f_c=1$ .
- Define how much ripple you will most likely allow in the traversing band.
- Find low-pass prototype values from the table.
- Finally, scale all elements to the desired frequency and impedance range.

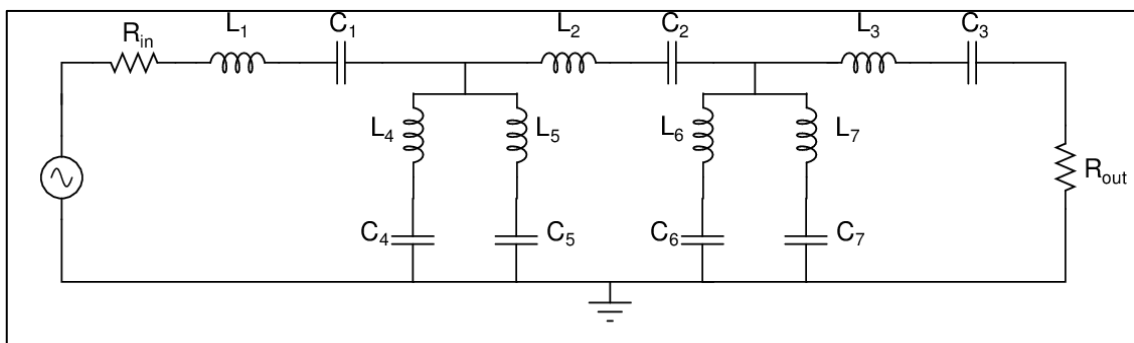


Figure 2.4. Elliptic (cauer) filter topology

When determining the structure of the filter, it was taken into consideration that the high

number of switchable circuit elements and the transition band is sharp. Due to a sharp filter transition band, the elliptic filter structure fits the desired specs. Due to narrow bandwidth is desired in the designed filter, ripples are less concerned. Because of the sharp transaction at cut-off frequency filter is designed according to the Chebyshev Filter values. Adding adjustable capacitors at parallel blocks makes the filter out of known topologies. As the resonant frequency of the blocks has changed, and because of the constant inductor values that can be used in the circuit, optimization is applied to the circuit.

## 2.5. HIGH-PASS AND LOW-PASS FILTER DESIGN

In the low-pass filter design, the transition is quite simple. For example, a Chebyshev low-pass filter with 4 elements and 0.5 dB ripple makes a 60 dB attenuation at  $f / f_c = 4$ . Instead of the low-pass filter.

Once the desired properties have been determined and the degree of the filter is found, a higher pass element value is obtained from the lower pass prototype element value. The next step is to obtain a high-pass element value than the low-pass prototype element value. Each component is equal to its opposing component. This is the exact opposite of the high-pass filter characteristic obtained by this transformation [21].

## 2.6. BAND-PASS FILTER DESIGN

Low pass prototype circuit and frequency response curve also be used in bandpass filter design. The same method is applied as in the case of a high pass. The attenuation bandwidths remain the same when converting from low pass design to bandpass design. That is, a 3-band low-pass filter with a bandwidth of 2 kHz is converted to a band-pass filter with a bandwidth of 2 KHz. If the low-pass circuit response is 30 dB attenuation at 4 kHz bandwidth ( $f / f_c$ ), the band-pass circuit response also makes 30 dB attenuation with 4 kHz bandwidth [22].

$$\frac{BW}{BW_c} = \frac{f}{f_c} \quad (2.10)$$

$BW$ : Bandwidth at desired attenuation value

$BW_c$ : 3 dB bandwidth of the band-pass filter

Sometimes the required attenuation values are given at the frequency value. In this case, equation 3.10 is converted to the properties that meet the requirements [6].

The center frequency of the bandpass filter is found according to the following formula:

$$f_0 = \sqrt{f_a f_b} \quad (2.11)$$

$f_a$  and  $f_b$  are any two frequency values, one of the transition band and one on the other. These two values have the same rejection value.

After finding the value of  $f_{\text{center}}$ , the ratio of the bandwidth is calculated in equation 2.12.

$$\frac{BW_{40 \text{ dB}}}{BW_{3 \text{ dB}}} \quad (2.12)$$

After this ratio is found,  $f / f_c$  value of 40 dB attenuation filter design is coming.

The low-pass prototype value of the filter that provides the desired properties is converted to the bandpass filter. Each parallel component in the low pass filter is converted to the series resonant circuit.

In the final stage of the design, the converted filter is frequency and impedance scaled.

For parallel resonant arms:

$$C = \frac{C_n}{2\pi RB} \quad (2.13)$$

$$L = \frac{RB}{2\pi f_0^2 L_n} \quad (2.14)$$

For series resonant arms:

$$C = \frac{B}{2\pi f_0^2 C_n R} \quad (2.15)$$

$$L = \frac{RL_n}{2\pi B} \quad (2.16)$$

$R$ : Load resistance

$B$ : 3 dB bandwidth

$f_0$ : Center frequency

$L_n$ : Normalized inductance value for bandpass filter

$C_n$ : Normalized capacitance value for the bandpass filter

In short, the band-pass filter design stages can be listed as follows:

- Using equation 2.11, the bandpass filter properties are converted to low pass properties.
- Find the type and degree of the filter using the low pass attenuation curve.
- Low-pass prototype values are found.
- The circuit is converted to a bandpass filter.
- Impedance and frequency scaling is performed [23].

### 3. FABRICATION TECHNOLOGIES

Semiconductors are crystal and amorphous solids with distinct electrical properties. Although they exhibit high resistance to typical resistance materials, their resistances are not as high as insulators. In contrast to metals, their resistance decreases as the temperature increases. Finally, if desired, the purity of the conductivity properties can be changed easily by disrupting the method called “doping”. The doping method reduces the resistance of the semiconductor. Semiconductor devices; It has useful features such as easier flow in one direction, changeable resistance, and sensitivity to light-temperature. Electrical properties of semiconductor materials; the devices produced from semiconductors can be used as amplifiers, switches or energy conversion elements as they can be changed by the use of doping method. Modern knowledge of the properties of semiconductors and the explanation of their movements in the crystal lattice structure are based on quantum physics [24].

Doping effectively increases the number of charge carriers in the crystal. A doped crystal; if it contains mostly free cavities, it is called the p-type crystal, and if it contains mostly free electrons it is called n-type crystal. The doping method is applied under strict conditions in order to control the density of the semiconductor materials, p and n-type dopants used in electronic devices. A single semiconductor crystal may have a plurality of n or p types of fields, and the p-n connections formed between these areas allow the useful electronic properties of the semiconductors. Although many compounds and pure elements exhibit semi-conductive properties, silicon, and germanium or gallium compounds are the most commonly used in electronic devices. The elements in the region called the semi-metals ladder of the periodic table are generally used as semiconductors. Many features of semiconductors were discovered in the mid-19th century and early 20th century. The first practical application of semiconductors is the Cat Whisker detector, which was developed in 1904 and is widely used in radio receivers. The developments in quantum physics led to the development of transistors in 1947 and integrated circuits in 1958, respectively. The global semiconductor market has been moving for a long time. The industrial facilities to be used for chip production require investments worth billions of dollars. Periodic fluctuations in supply and demand cause significant fluctuations in prices and dividends. Semiconductors can be elements such as germanium, silicon, selenium; copper oxide, gallium arsenide, indium phosphide, lead sulfide [25].

Since semiconductors are the most important building blocks of integrated circuits, almost all of today's technological instruments use semiconductors. Devices with integrated circuits; common examples such as laptops, scanners, mobile phones. Semiconductors for integrators are produced by mass production. To produce an ideal semiconductor, chemical purity is a priority. Considering the dimensions of the materials used, even the slightest defect can have a very destructive effect on how the material behaves. A high degree of crystal perfection is also important, as defects in the crystal structure can affect the semiconductor properties of the material. Crystal defects are the main causes of the defects of semiconductor material. As the crystal grows, it is also difficult to achieve the perfection that is desired. Today, mass production techniques are sliced into thin discs with 100-300 nm diameter wafers. For the production of semiconductors to be used in the integrals, a method is used which is the mixture of semiconductor manufacturing processes. The first method is the thermal oxidation method. A silicon dioxide layer is formed on the surface of silicon by the thermal oxidation method and the product is used as Gate Insulator silicon or Field Oxide Thermal. The sequence is called Photomask and Photolithography, which means that the shape of the circuit is created on the material. The drawing of the circuit is reflected using ultraviolet light to the surface of the photosensitive material which provides the shape to form on the material. The result is obtained after chemical changes in the light-sensitive substance. In the next process etching. In the previous step, the surface of the silicone, which is not coated with the light-sensitive material, can be etched at this stage using acid. Today, the method of scraping with plasma is preferred. The plasma scraping method uses an abrasive plasma gas under low pressure. Freon or chlorofluorocarbons are examples of corrosive plasma gases used. The high-frequency radio voltage generated between the cathode and the anode allows the gas to circulate in the medium. The silicon thin disk (wafer) is located on the cathode and the positively charged ions scattered from the gas passing through the plasma are hit by the disc. As a result, the silicon material is anisotropically referred to as step-by-step diffusion, and the stage at which the desired properties are imparted to the semiconductor material is progressed. Diffusion is also known as doping. At this step, impure atoms are added, which allow p-n junction points to form. The process is carried out in an environment of 1100 C to integrate these impure atoms with silicon thin disks. When this step is completed and the semiconductor is returned to room temperature, the production process is completed. Now the semiconductor material is ready to take its place in the integrated circuit [26].

### 3.1. PHEMT MANUFACTURING PROCESS

High electron mobility transistors are the group of devices which in their operation rely on heterojunctions. The heterojunctions are formed between semiconductors of different compositions and bandgaps, such as GaAs. In a HEMT free electrons are physically separated from the ionized donors due to a specially designed epitaxial layer structure, thus the electron mobility is increased. Conventionally, the epitaxial layers are grown employing molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) [26] and maybe doped or undoped depending on the requirements [29].

The foundry which is used in this work is a GaAs foundry that has developed numerous technologies employing HBTs, BiFETs, and pHEMTs [30]. It is worth describing the GaAs pHEMT manufacturing process, as this work leverages circuits manufactured by foundry's fabrication plant. The present 0.15  $\mu\text{m}$  pHEMT process utilizes molecular beam epitaxy (MBE) material growth and an i-line ( $\lambda_i = 365 \text{ nm}$ ) stepper for the formation of the gates. The epitaxial structure consists of a high concentration undoped in the GaAs channel layer and double  $\delta$ -doped layers, that provide the carriers to the channel. There are GaAs spacer layers grown between the channel layer and Si layers, and on top of the upper spacer layer, a GaAs Schottky layer is placed [30].

In many applications, the electrical behavior of materials is more important than their mechanical behavior. For example, the metal wire that conducts current over long distances must have a high electrical conductivity to reduce the power loss caused by heating. It is necessary to understand how concepts such as electrical conductivity are produced and controlled to select and use materials for electrical and electronic applications. It should also be noted that electrical behavior is influenced by the material structure, material handling and the environment in which the material is exposed. For this reason, the atomic structure and electronic devices of materials must be well known and basic electrical laws should be reminded [31].

### 3.2. ELECTROMAGNETIC SIMULATION

Electromagnetic simulation is a modern technology to simulate electromagnetic devices based on different simulation methods. Increasingly used to replace expensive prototyping.



The most popular methods for field simulations are finite elements, boundary elements, or finite differences [32].

Using these terms, AWR can be considered as an electromagnetic simulation software based on finite element analysis for field simulations at static, low and medium frequencies [20].

In the thesis prepared for the thesis, AWR Design Environment was used as a simulator. For electromagnetic simulation, AXIEM electromagnetic solver is used in AWR. The AXIEM engine which is provided by AWR, results close to actual measurements. The closeness of the AWR to the schematic results can be tested from a simple simulation. Two simple transmission lines were placed side by side and a capacitor was connected. This simple circuit was set up in a schematic and tested in an electromagnetic simulator. The results are presented in Figure 3.3.

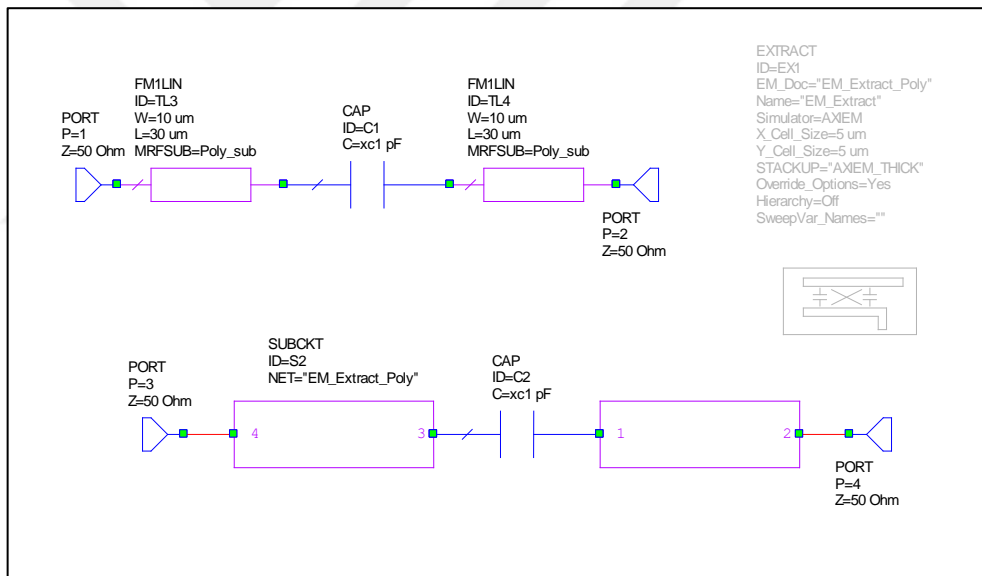


Figure 3.1. The capacitor connected between two fixed plates

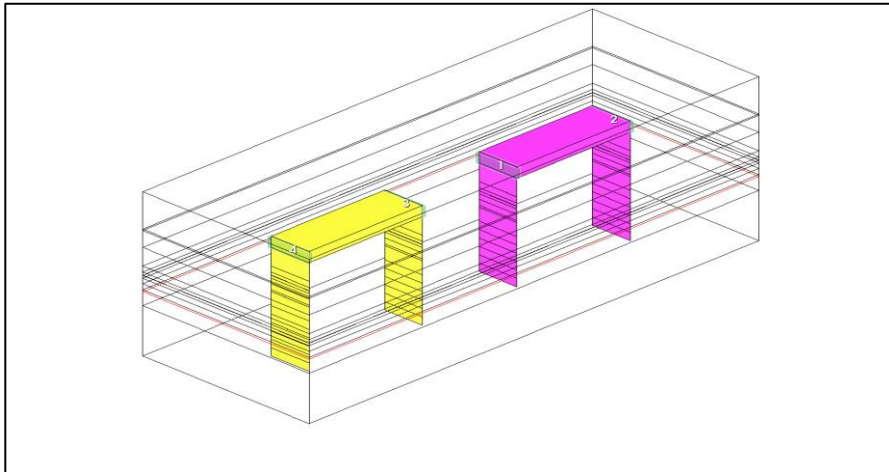


Figure 3.2. Electromagnetic simulation for schematic given in Figure 3.1

When simulating EM, the simulator divides the circuit into small pieces. The name of each piece is called the mesh. The higher the number of mesh in the circuit, in other words, the smaller the mesh in the circuit, the more precise the result of the circuit. Meshing, sometimes called sub sectioning or gridding, characterizes full-wave EM simulators and distinguishes them from closed-form, equation-based modeling found in circuit simulations [33].

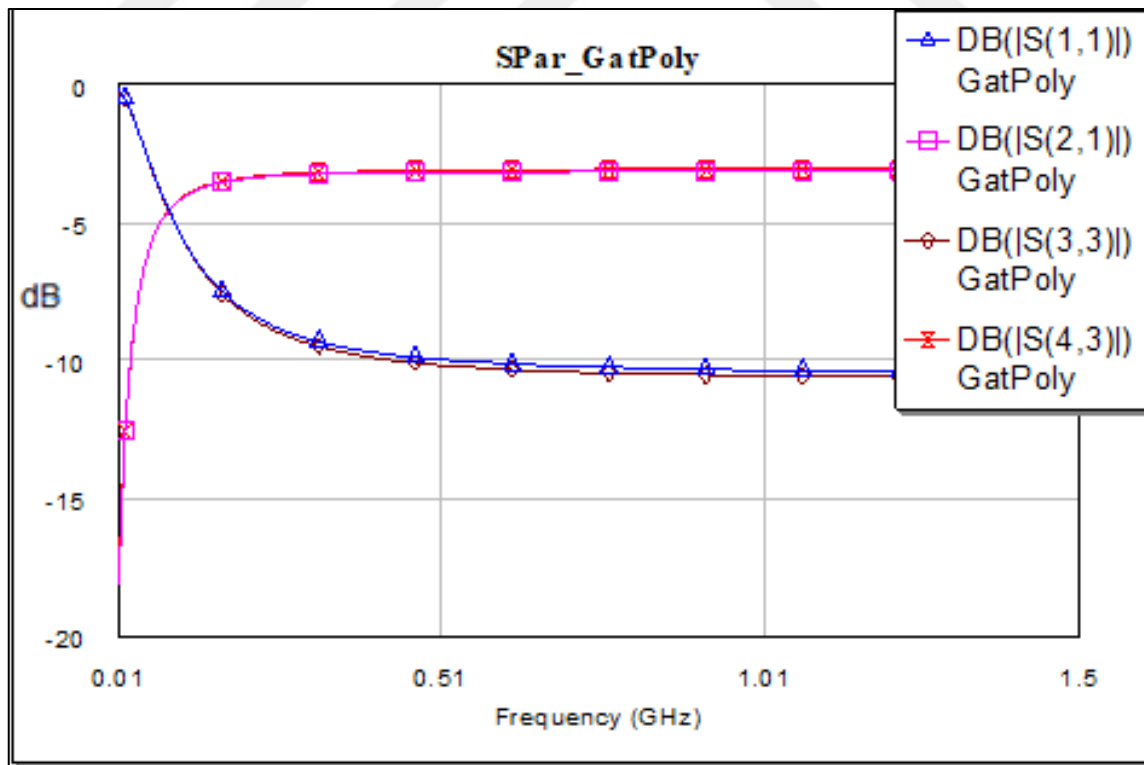


Figure 3.3. Simulation results vs EM extraction results of Figure 3.2

Two simple transmission lines were placed next to each other to test the reliability of EM

Solver. The results of EM Solver are given in Figure 3.3 as s33 and s43. s11 and s21 are the schematic simulation results.

As can be seen in Figure 3.3, AXIEM is very close to the schematic simulation results. This also gives confidence to the layout after the circuit is designed.



## 4. METHODOLOGY

Several factors were considered before the design of presented thesis. The first of these factors is to check if there are other works at the same frequency. When looking at researches, it is a prominent filter: 900 MHz and 1.8 GHz microwave thin-film bandpass filters on AZO3 substrates are designed, fabricated and characterized. Based on the high-Q values of passive components, spiral inductors, and MIM capacitors, for example, a low insertion loss of thin-film bandpass filter can be realized with a minimized chip area. The insertion loss was 3 dB for a 1.8 GHz filter and was 5 dB for a 900 MHz filter [10]. However, these aimed frequencies were realized one by one. There is no transition between the two frequencies. In addition, the insertion losses are lower than the designed filter, but the bandwidth is larger than the designed filter.

Another example is the dual-band 900 MHz 1800 MHz filter [42, 44,45]. In the paper, a dual-band filter using stepped impedance resonators with coupled-feed lines is proposed to develop the microstrip open-loop resonators dual-band filter. The dual-band filter is based upon the design of two filters independently; one of them is meeting the desired performance at 900 MHz and the other desired performance at 1800 MHz. The two filters can be combined using the coupled feed lines. The measured insertion losses are better than 3 dB for the two channels [27,28]. Unlike this filter, the bands of the designed filter are selectable. Insertion loss is not very different from the thesis. In addition, the size of the circuit to be reduced to the integrated circuit size is an original value for the designed circuit.

The second factor is to determine the specifications required in the circuit. To determine the specifications, there should be the midpoint of a filter made with non-chip components with single frequency filters designed at the integrated circuit level. The quality factor of a filter realized by discrete components is much better than the quality factor of a filter made on-chip. The reason for this is that the quality of an inductor, which is designed discrete, is much higher quality than an inductor designed on-chip and causes a lot of losses. In some cases, the quality factor of the inductors provided by the foundry is so low that the chip may need to be connected to the inductor circuit outside of the chip. In addition to this, a minimum rejection value is required for frequency applications set in the circuit. The aim is to improve the minimum rejection value. Acceptable minimum insertion loss is 10 dB. The higher the

quality factor of the circuit, the lower the loss of insertion.

The next step is to determine the topology of the circuit. The topology of the circuit was determined according to the rejection and ripple tolerance in the band. The topology of the circuit is the Cauer (Elliptic) Filter. The Cauer filter creates a little ripple in the band. Rejection out of the band is not high but 3 dB rejection slope is quite sharp. According to design is presented, the negative feature of the Cauer filter topology is that it contains a large number of inductors. The more inductor it contains, the greater the loss to be experienced in the circuit. External inductors were used to solve this problem. However, the use of external inductor increases the cost of the circuit while improving the quality of the circuit.

The quality factor of the circuit is intended to be as high as possible. For this, the circuit elements must be made of high-quality products. The general name of the manufacturing companies that provide these elements is called foundry. After determining the topology in the circuit, the material and foundry to be used in the circuit are determined before the design. The determination of foundry is the fourth factor to be determined before the design of the circuit.

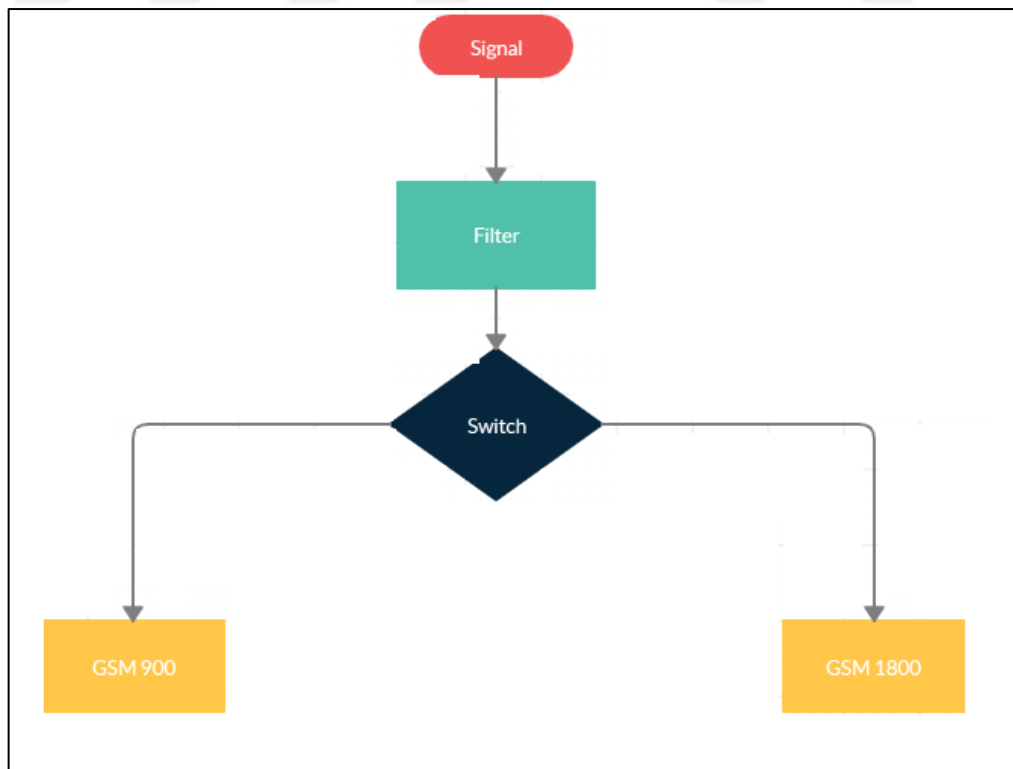


Figure 4.1. Block diagram of the thesis topology

GaAs is the substrate material that is used in the presented thesis. The selected technology

process is provided by WIN Semiconductor foundry. The reason for using this foundry is that it can withstand high voltages according to the experience obtained from previous designs.

The advantages of the GaAs substrate are that GaAs process technology continually provides improved power efficiency and higher linearity [48]. Also, GaAs has very high electron mobility, high thermal stability, low noise and wide temperature operating rate. In addition, GaAs foundries also have to provide solutions on the infrastructure side with cost-effective, ultra-high-performance technologies to enable high capacity backhaul networks operating at E-Band and above. These high data rate microwave radios will rely on production-ready advanced transistor technologies such as the WIN 0.1 $\mu$ m technology platform, PP10, which is the only production 0.1 $\mu$ m pHEMT available on 150mm substrates.

A primary difficulty in developing GaAs integrated circuits has been low integration levels, limited by yields and integration densities that are lower than silicon technologies. However, recent advances in GaAs EHFET (enhancement junction field-effect transistor) technology have allowed much greater integration levels.

Table 4.1 Comparison of silicon and GaAs[47]

<b>Property</b>	<b>Silicon</b>	<b>GaAs</b>
Low Field Mobility of Electron (cm <sup>2</sup> /V-s)	500-1200	4000-9000
Low Field Mobility of Hole (cm <sup>2</sup> /V-s)	480	400
Saturated Electron Velocity (cm/s)	9 x 10 <sup>6</sup>	1.3 x 10 <sup>7</sup>
Energy Gap (eV)	1.12 (indirect)	1.43 (direct)
Dielectric Constant	11.7	12.93

With the purpose of making the designing process easier, the thesis has started on the basis of 900 MHz. In this part, the design of 900 MHz bandpass filter is explained and in the next heading, the transition from 900 MHz to 1800 MHz bandpass filter is inspected.

The design of a single frequency circuit was examined before designing the 900 MHz - 1800 MHz selectable bandpass filter. The circuit component values were found numerically. After

that, scattering parameters of the circuit were examined with the help of the simulator (AWR). In the next step, the circuit was tuned. After the circuit design with the ideal components, the actual component was replaced with the ideal component.

The next stage was drawing of the layout. When the layout was drawn, the components were connected by microstrip lines. Because microstrip lines are much less expensive than the other waveguide technologies and microstrip lines are lighter and more compact. The characteristics of these microstrip lines are given by the manufacturer. Finally, EM simulation was performed. Schematic results and electromagnetic simulation results were compared.

The mathematical extraction of circuit component values is given in the following equations.

It is necessary to look at the Chebyshev filter coefficient table to see the prototype values of the components in the filter. The filter must be of seventh-degree to provide rejection values. Prototype values are given in Table 4.2

Table 4.2 Chebyshev filter coefficients

$N$	$g_0$	$g_1$	$g_2$	$g_3$	$g_4$	$g_5$	$g_6$	$g_7$	$g_8$
1	1	1.99	1.00						
2	1	3.10	0.53	5.80					
3	1	3.34	0.71	3.34	1.00				
4	1	3.43	0.74	4.34	0.59	5.80			
5	1	3.48	0.76	4.53	0.76	3.48	1.00		
6	1	3.50	0.76	4.60	0.79	4.46	0.60	5.80	
7	1	3.51	0.77	4.63	0.80	4.63	0.77	3.51	1.00

According to Table 4.2:

$$g_8 = g_0 = 1$$

$$g_7 = g_1 = 3.51$$

$$g_6 = g_2 = 0.77$$

$$g_5 = g_3 = 4.63$$

$$g_4 = 0.80$$

Since the filter is grade 7, the above constants are selected.  $g_1, g_2, g_3, g_4, g_5, g_6, g_7,$  and  $g_8$  are constants of inductor and capacitor values.  $g_0$  and  $g_8$  are input and output resistor values.

The table assumes that the input resistors are 1 ohm. The conversion equations 5.1, 5.2 and 5.3 will be used because the input and output of the designed circuit will be over 50 ohms.

$$R'_G = 1 R_G \quad (4.1)$$

$$L' = L R'_G \quad (4.2)$$

$$C' = \frac{C}{R'_G} \quad (4.3)$$

According to equation 4.1:

$$R'_G = 1 \cdot 50 = 50 \Omega$$

$$L_1 = L_4 = (50)(3.51) = 175 H$$

$$L_2 = L_3 = (50)(4.63) = 230 H$$

$$C_1 = C_3 = \frac{0.77}{50} = 15 mF$$

$$C_2 = \frac{0.80}{50} = 16 mF$$

In the next step, the low cut frequency ( $\omega_l$ ) and the high cut-off frequency ( $\omega_u$ ) are determined.

In this thesis,  $\omega_u$  is selected as 1.1 ( $k_1$ ) times of center frequency and  $\omega_l$  is selected as 0.9 ( $k_2$ ) times of center frequency.

$$\omega_{center} = \omega_c = \sqrt{\omega_l \times \omega_u} \quad (4.4)$$

$$\omega_u = k_1(2\pi f_c) \quad (4.5)$$

$$\omega_l = k_2(2\pi f_c) \quad (4.6)$$

According to equation 4.5 and 4.6:

$$\omega_u = (1.1)(2\pi \cdot 900 \times 10^6) = 6.21 GHz$$

$$\omega_l = (0.9)(2\pi \cdot 900 \times 10^6) = 5.08 GHz$$



$$\omega_u - \omega_l = 1.13 \text{ GHz}$$

$$\omega_c = \sqrt{\omega_l \times \omega_u} = 5.61 \text{ GHz}$$

The design for this part was for the low pass filter. In the next step, the low pass filter will be converted to the bandpass filter. A high pass filter is designed at the end of the low pass filter. The best way to do this is to use resonant components corresponding to each component. The formulas that convert the low pass filter into a bandpass filter are given below.

For series capacitors and inductors:

$$L'' = \frac{L'}{\omega_u - \omega_l} \quad (4.7)$$

$$C'' = \frac{\omega_u - \omega_l}{\omega_0^2 L'} \quad (4.8)$$

For shunt capacitors and inductors:

$$L'' = \frac{\omega_u - \omega_l}{\omega_0^2 C} \quad (4.9)$$

$$C'' = \frac{C}{\omega_u - \omega_l} \quad (4.10)$$

The final status of the circuit is given in Figure 4.2.

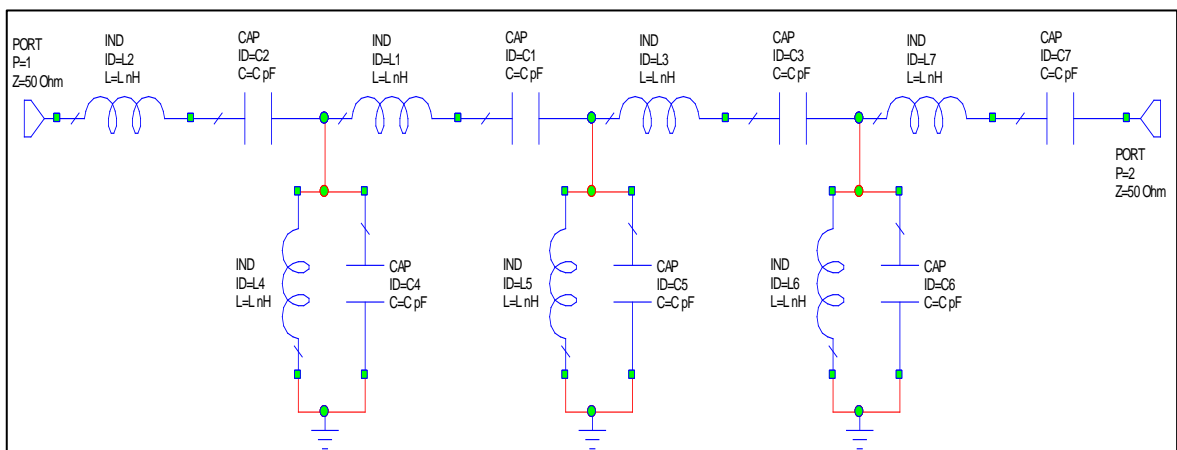


Figure 4.2. Transformation of low pass filter to the bandpass filter

$$L1'' = L4'' = \frac{175}{1.13 \times 10^9} = 154 \text{ nH}$$

$$L_{2''} = L_{3''} = \frac{175}{1.13 \times 10^9} = 203 \text{ nH}$$

$$C_{L1} = C_{L4} = \frac{1.13 \times 10^9}{(31.5 \times 10^{18})(175)} = 0.2 \text{ fF}$$

$$C_{L2} = C_{L3} = \frac{1.13 \times 10^9}{(31.5 \times 10^{18})(230)} = 0.15 \text{ fF}$$

$$C_{1''} = C_{3''} = \frac{15 \times 10^{-3}}{1.13 \times 10^9} = 13.2 \text{ fF}$$

$$C_{2''} = \frac{16 \times 10^{-3}}{1.13 \times 10^9} = 14.1 \text{ fF}$$

$$L_{C1} = L_{C3} = \frac{1.13 \times 10^9}{(31.5 \times 10^{18})(15 \times 10^{-3})} = 2.39 \text{ nH}$$

$$L_{C2} = \frac{1.13 \times 10^9}{(31.5 \times 10^{18})(16 \times 10^{-3})} = 2.24 \text{ nH}$$

After the component values have been added, the appearance of the circuit is given in Figure 4.3.

In the next step, optimization will be applied to the circuit. The values in the circuit are increased to 203 nH. 203 nH is not performed in IC circuits. The high-value inductor in the chip is also large in size. As an example, an inductor of 200 nH is 5 times larger than the rest of the chip. The circuit components will be replaced by the external components. Each added real circuit component will introduce a loss of insertion to the circuit. In addition, there will be changes in the center frequency of the circuit with the effect of parasitic capacitances.

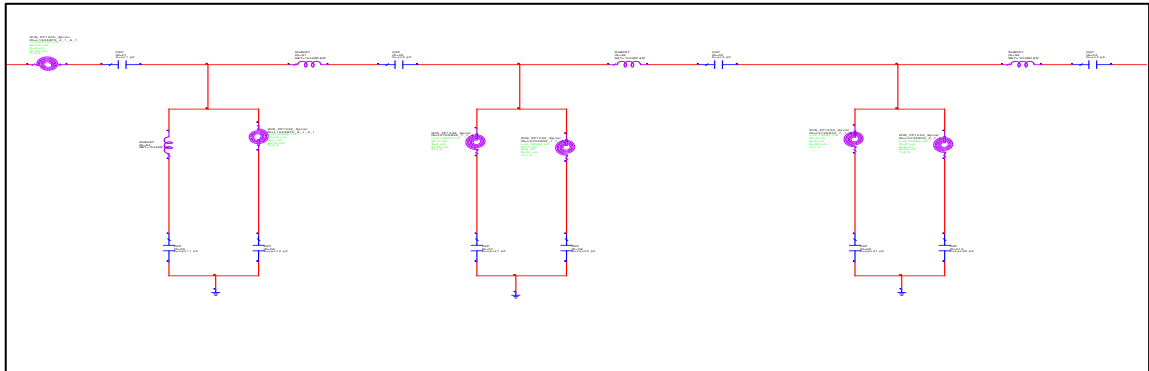


Figure 4.3. Real inductors added to the circuit after optimization.

The circuit components will be replaced by the actual components. Each added real circuit component will introduce a loss of insertion to the circuit. In addition, there will be changes in the center frequency of the circuit with the effect of parasitic capacities.

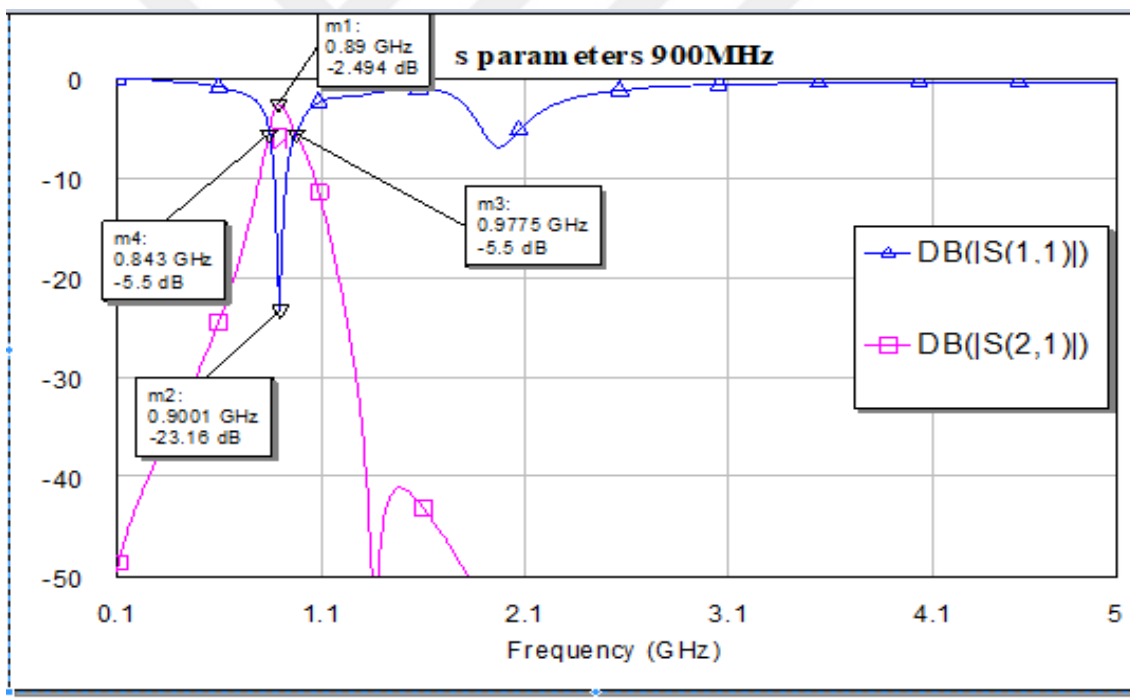


Figure 4.4. Simulation results of 900 MHz Bandpass Filter

According to the graph in Figure 4.5, the center frequency of the filter shifted by 10 MHz. Insertion loss is 2.49 dB, but this value will increase with the losses of microstrip lines.  $0.5 \cdot f_c$  and  $1.5 \cdot f_c$  rejections are 28 dB, and when the lines are connected to the circuit, these suppressions will increase with "insertion loss". The next step is to draw the layout of the circuit in Figure 4.3.

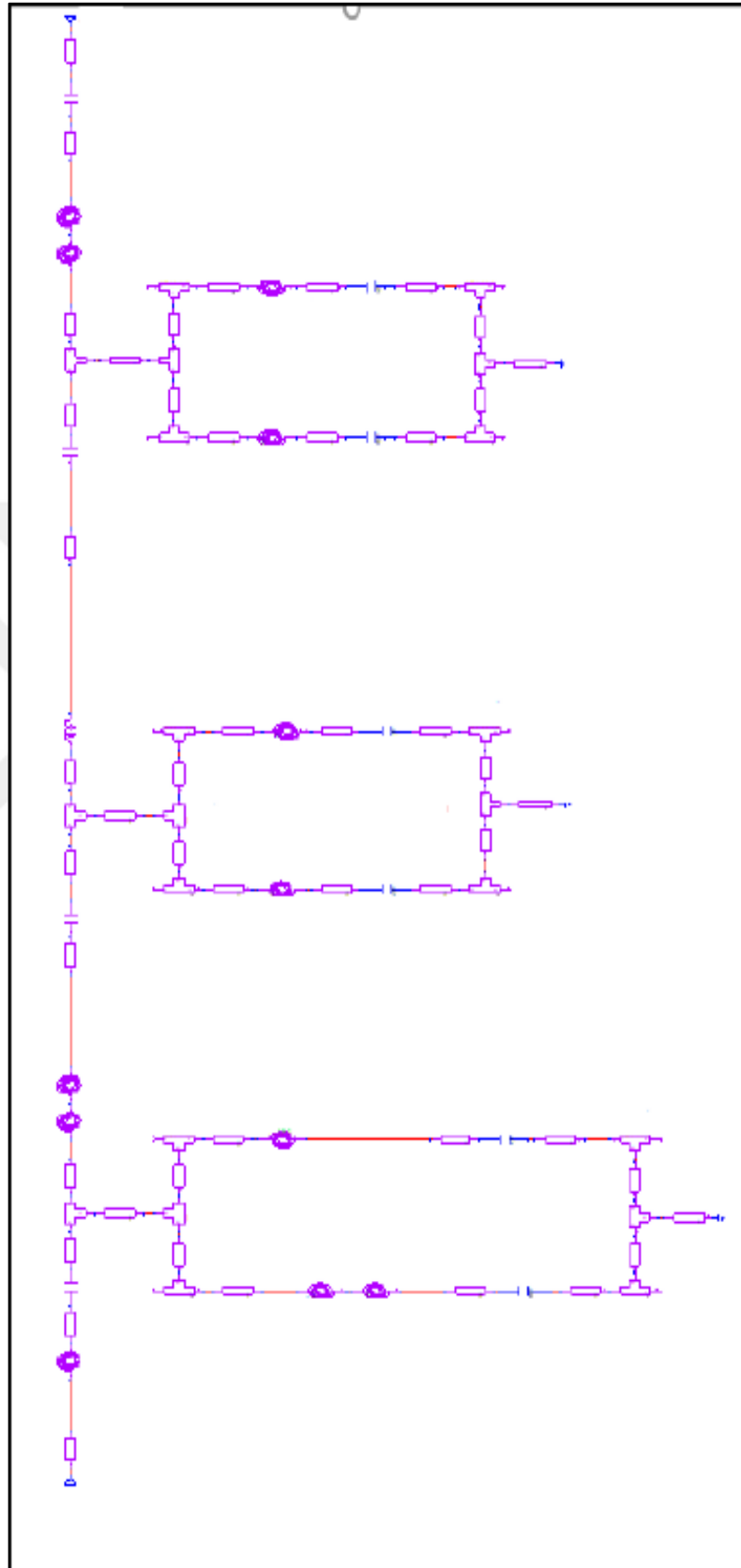


Figure 4.5. Microstrip lines connected to the circuit to create the layout

After adding microstrip to the circuit, the layout drawing is completed. When drawing the circuit layout, the length of the microstrip is important so that the components do not come close together. If the components on the layout are close to each other, parasitic capacitive effects may occur in the circuit. In addition, the components can induce each other, which induction current is parasitic for the designed circuit. After the distances are set, the layout of the circuit is given in Figure 4.6.

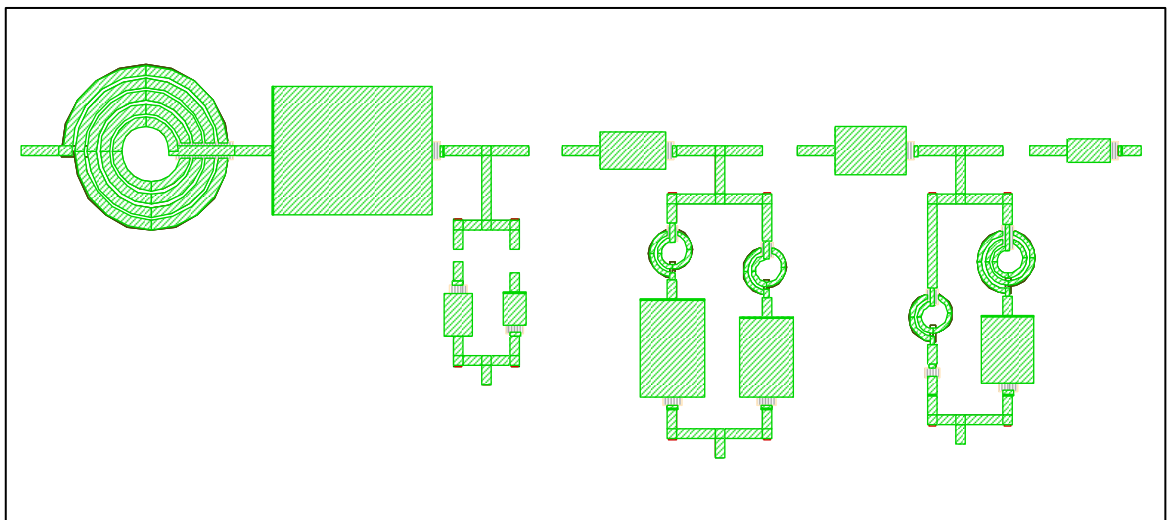


Figure 4.6. Layout of the 900 MHz filter

Some inductors in the circuit give an error in electromagnetic simulation. Because the inductors in the layout have too many layers to be solved by EM Solver. These inductors are deactivated and the remaining part is considered as a black box and EM Extraction results are taken from AXIEM. The results of the scattering parameters of this black box with pins on it are distinct. After adding the inductors schematically on this circuit, the result is very similar to the results of the electromagnetic simulation. If the results are too close, the inductors given by the manufacturer as the circuit on-chip are already associated with electromagnetic simulation results.

Before the electromagnetic simulation is performed, a final schematic simulation was performed to see the difference between the schematic simulation and electromagnetic simulation. Electromagnetic simulation and schematic simulation results are given in Figure 4.7 and Figure 4.8

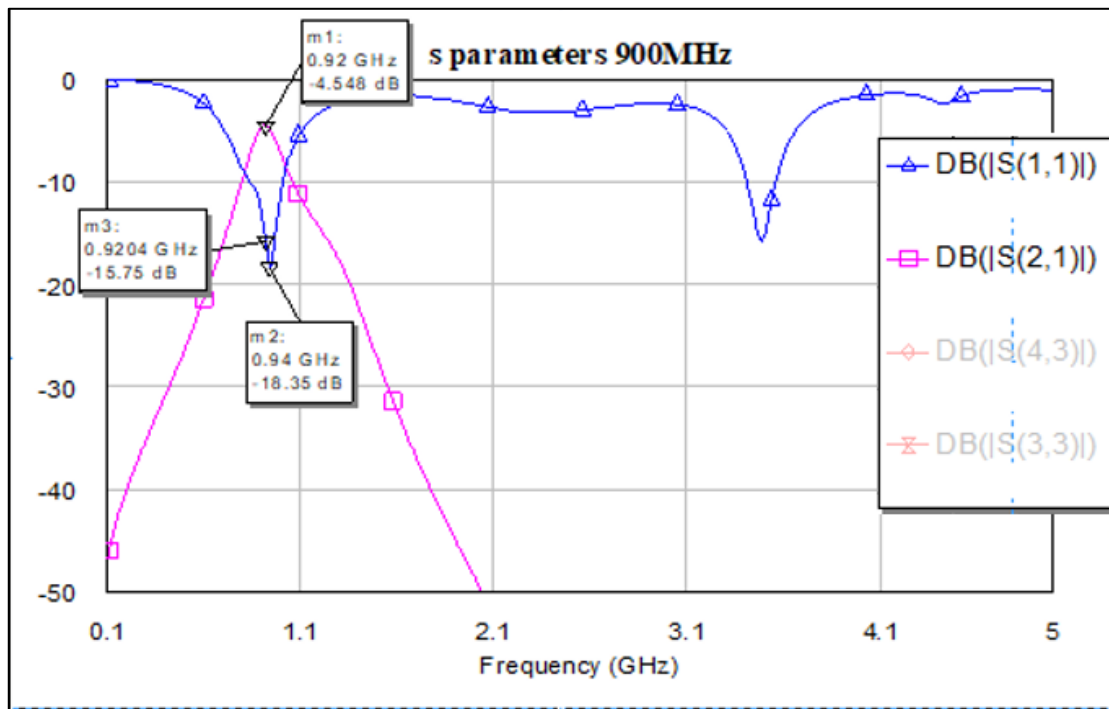


Figure 4.7. Schematic simulation of the final circuit

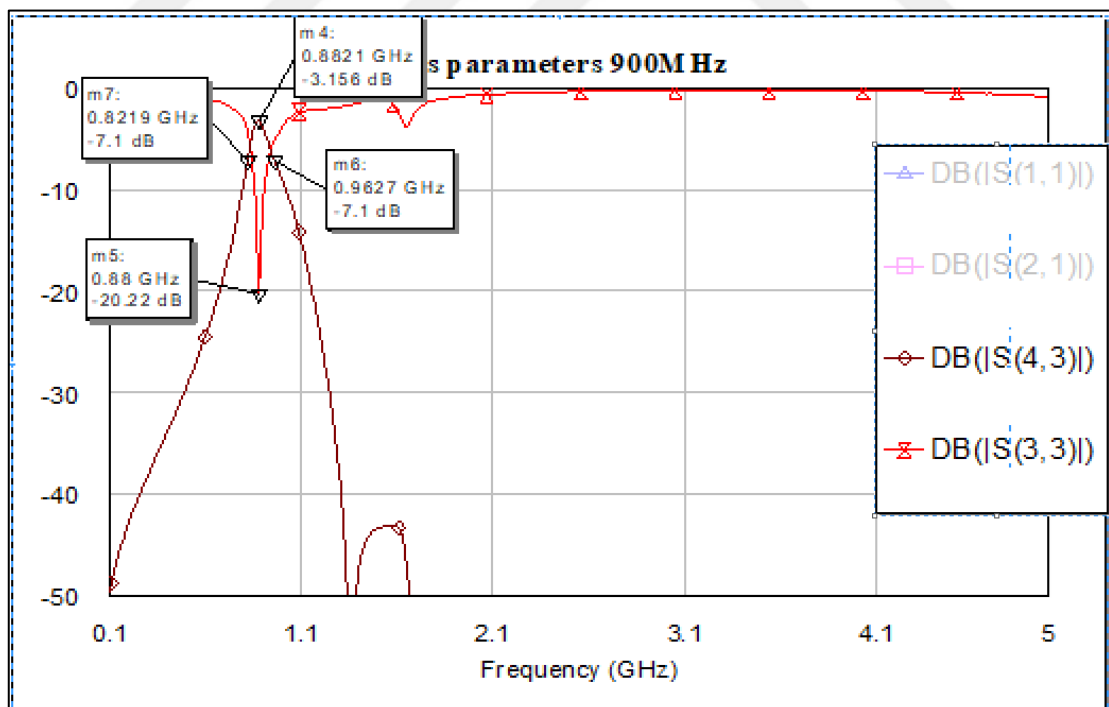


Figure 4.8. EM simulation of the final circuit

Figure 5.6 presents the schematic simulation of 900 MHz RFIC bandpass filter. Figure 5.7 is electromagnetic simulation of the 900 MHz RFIC bandpass filter. As shown in Figure 5.7, the center frequency of the circuit is shifted to the left as a result of electromagnetic

simulation. This is due to the parasitic effects in the circuit. However, the electromagnetic simulation results have shown that the insertion loss of the circuit has reduced and the matching of the circuit has improved.



## 5. GSM BAND SELECTABLE BAND PASS FILTER DESIGN

The works to achieve the targeted specs are described in this chapter. There is no numerical solution for the two frequencies. This is because there are two separate blocks for two different frequencies on the circuit. The common components to which these blocks are connected must also vary for two frequencies. The solution is formed by a circuit diagram for the center of two frequencies of 1.35 GHz. The next step was to use the optimization to find the values that the blocks should take. The shifting between the two frequencies is made using two switches.

In this case, since the layout size of the circuit is approximately known, microstrips are also connected to the circuit with the ideal components. The addition of microstrips to the circuit will make the optimization results closer to realization. To resolve the circuit at two frequencies, a different copy of the circuit was biased with a different DC value. Ideal circuit elements and circuits formed with microstrips are given in Figure 5.1. In Figure 5.2 and Figure 6.3, scattering parameter results of this circuit are given.

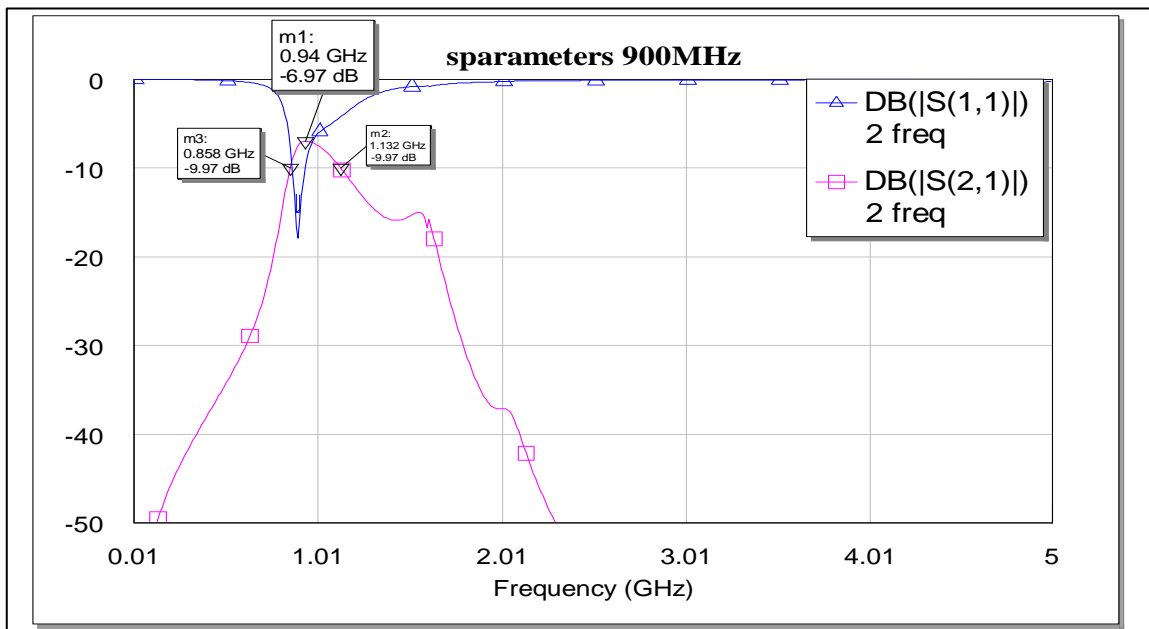


Figure 5.1. 940 MHz band pass filter



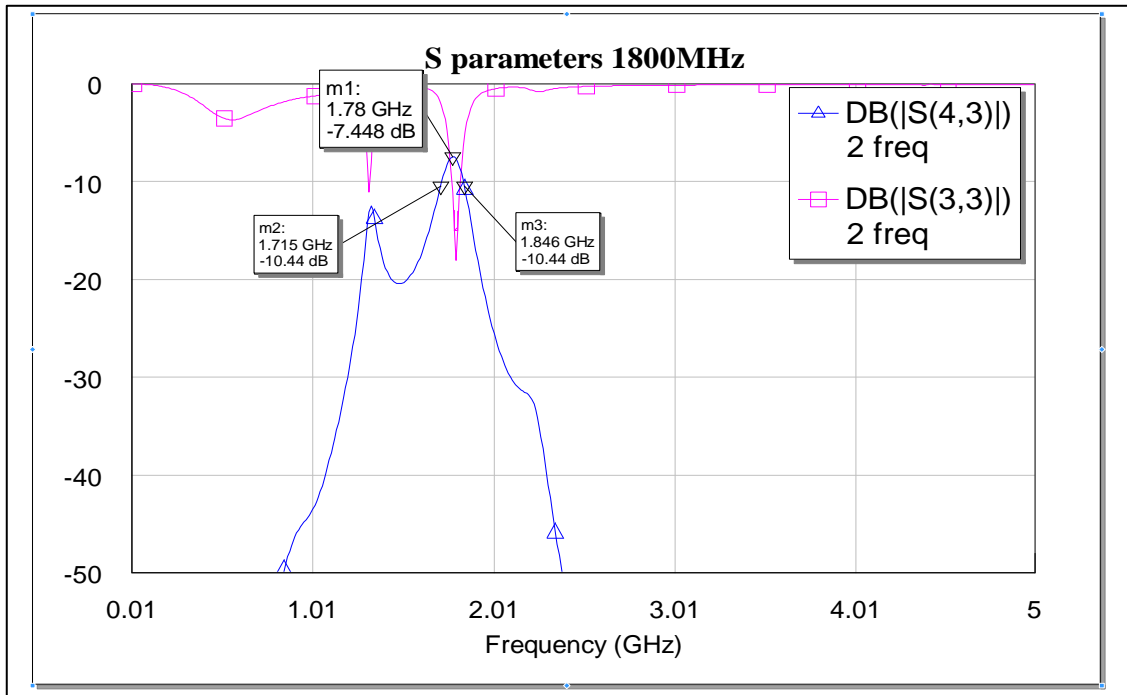


Figure 5.2. 1780 MHz band pass filter

Serial resistors have been added to the inductors to look at the quality factor of the actual components to be used in the circuits. If the change in these resistance values greatly increases the loss of the circuit, the use of high-quality inductors will be required.

The calculation of the quality factor of an inductor is given in equation 5.1. As the real impedance of an inductor increases, the resistor value is increased in the circuit. Losses occur in the circuit due to heating.

$$Q \text{ factor} = \frac{j\omega L}{R} = \frac{2\pi fL}{R} \quad (5.1)$$

The tolerable resistance value is 40 ohms for this inductor to make high losses in the circuit. The calculated quality factor value for the inductor with 40 ohms is:

$$Q \text{ factor} = \frac{2\pi(900 \times 10^6)(16.84)(10^9)}{40} = 1.58$$

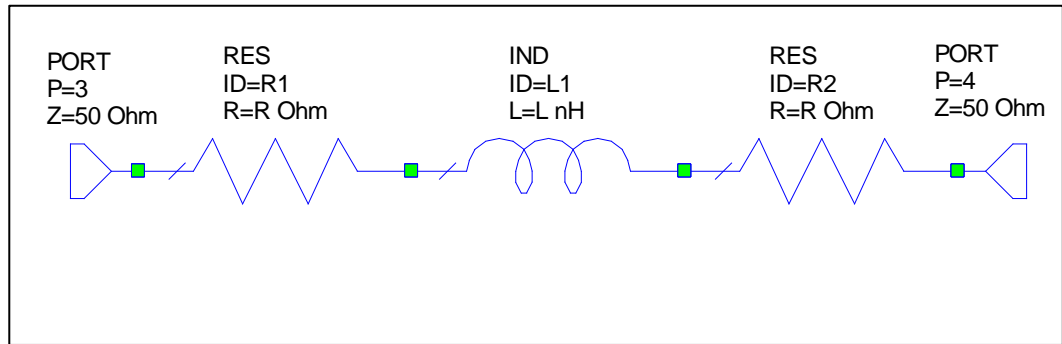


Figure 5.3. Series resistance connected to an ideal inductor

The quality factor is 1.58 is very low and is easy to obtain. For this reason, the inductors provided by foundry will be useful. But at some points of the circuit, low resistance values cause big losses. External components are used at these points as the high-quality factor is required.

There are several characteristics that determine the quality factor of the inductors. The first of these is Hysteresis losses. External inductors hysteresis loss is low and eddy current is less. Therefore they have a high-quality factor. These inductors are used at the points where the high-quality factor is desired. For these inductors, HQ (high quality) inductors from the 0805 series of the Coilcraft brand were used.

Due to the parasitic capacities caused by the switches in the circuit and due to the excess of the unchangeable common component in the circuit, the circuit built with the switches have high losses due to the matching problem at 900 MHz and 1800 MHz.

After the capacity and inductors in the circuit were realized and after the in-chip inductors were connected, the circuit was optimized and simulated. The result of this simulation before the layout is given in Figure 5.5 and Figure 5.6.

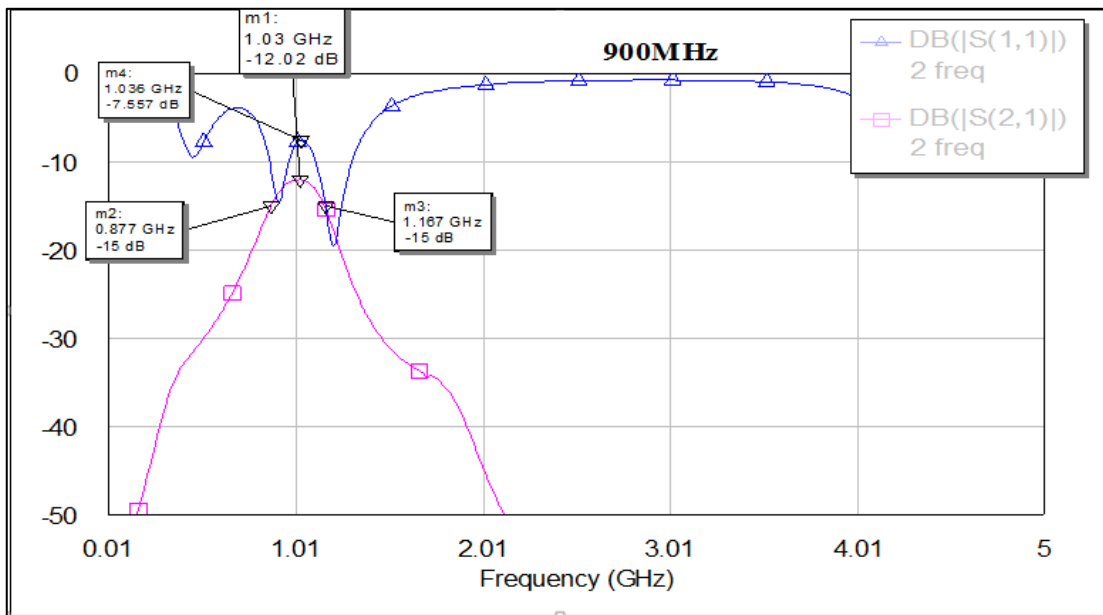


Figure 5.4. 900 MHz schematic simulation with on-chip switch

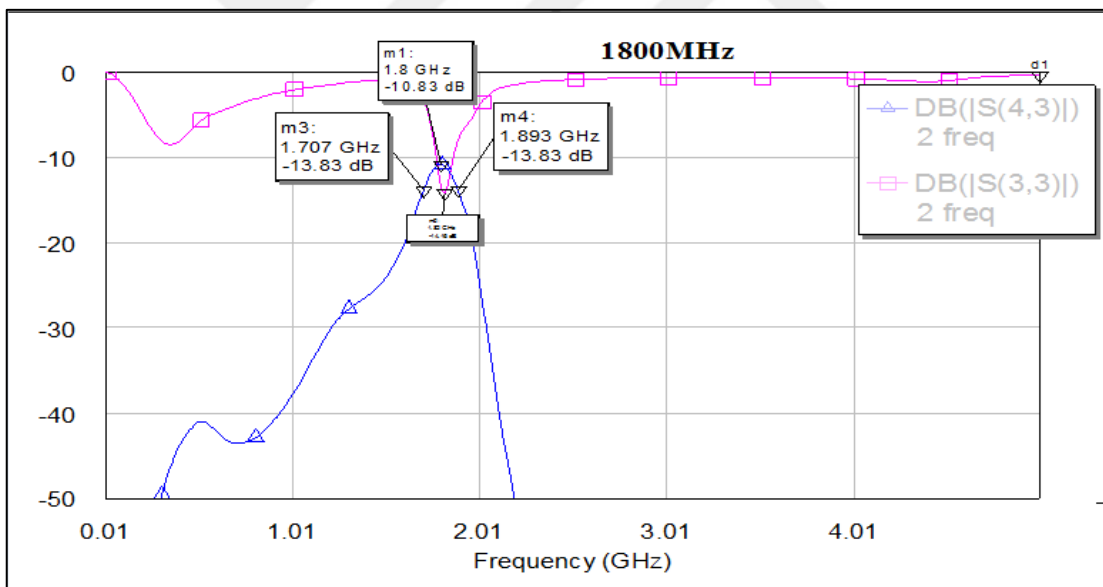


Figure 5.5. 1800 MHz schematic simulation with on-chip switch

According to the graph given in Figure 5.4 and Figure 5.5, insertion loss is 10.8 dB and 12 dB. These insertion loss values are high compared to the target value. As in the 900 MHz design, this problem is foreseen to be solved by shifting the center frequency to the left in the electromagnetic simulation results.

Center frequency shift and extra insertion loss to be observed after the EM simulation will worsen the specifications of the circuit. Therefore, a different method is required to correct

the circuit specifications.

In order to improve this situation, problem determination is required. In this case, when the current values passed through the switch are examined, the parasitic effect on the circuit is reduced to a minimum. To do this, the bias voltage of the switch was a sweep. It was seen that the minimum current was passed through the switch at the most suitable  $-5$  V bias voltage. But there is no way to eliminate the parasitic capacities from the switch because layout is already drawn. The number of switches provided by foundry is just one. In this case, the on-chip switch cannot be changed. To overcome this problem, it was decided to remove the switches out of the chip. This increase the chip's price and improved chip in specifications.

To find the bias voltage is where the switch is off, the gate voltage of the switches is swept.

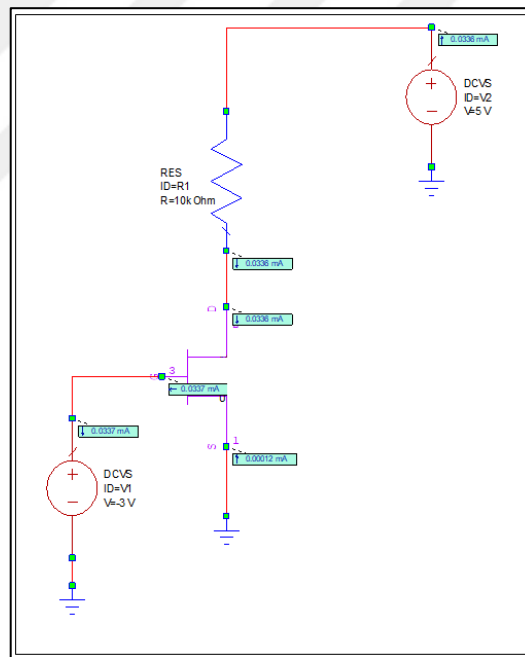


Figure 5.6. DC operating point analysis for the switch

When the bias voltage of the circuit is  $-3$  V according to the simulation given in Figure 5.7, the minimum current flows.

If the switch is connected to the circuit outside the chip, the  $s$ -parameters that can be obtained are given in Figure 5.8 and Figure 5.9.

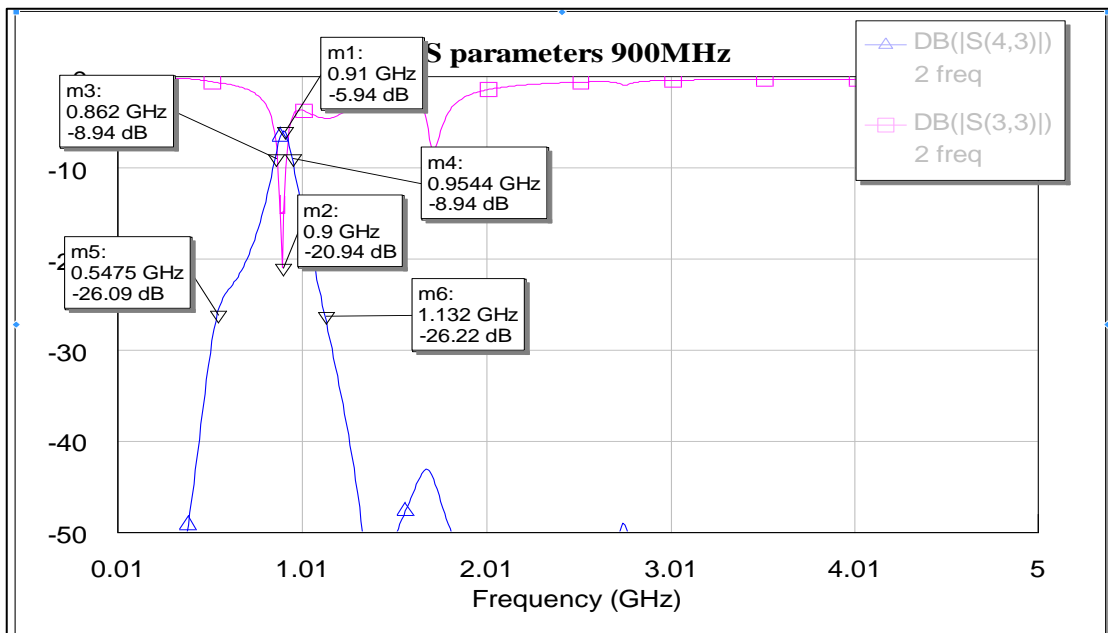


Figure 5.7. Schematic simulation of 900 MHz filter

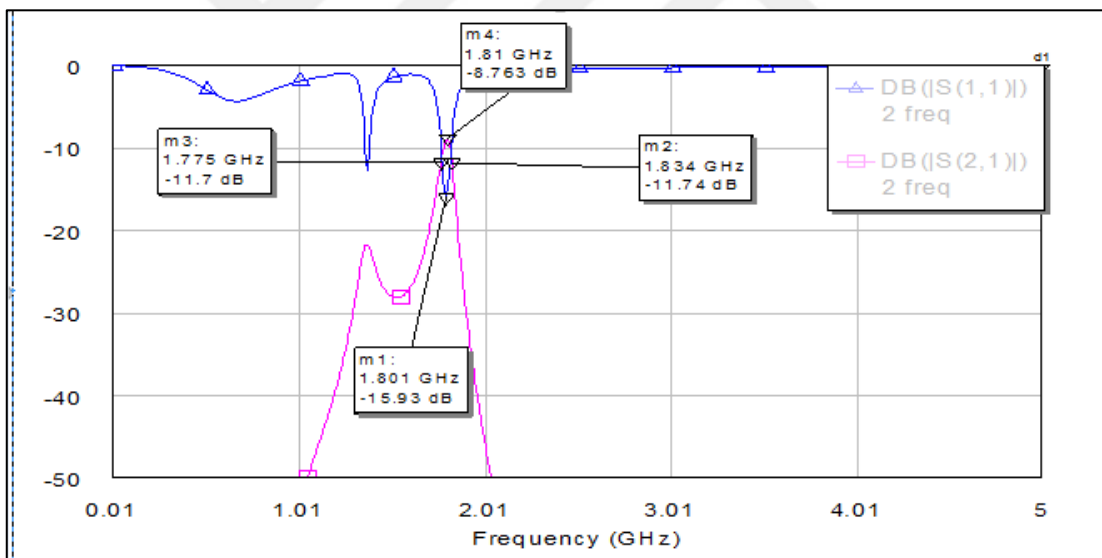


Figure 5.8. Schematic simulation of 1800 MHz filter

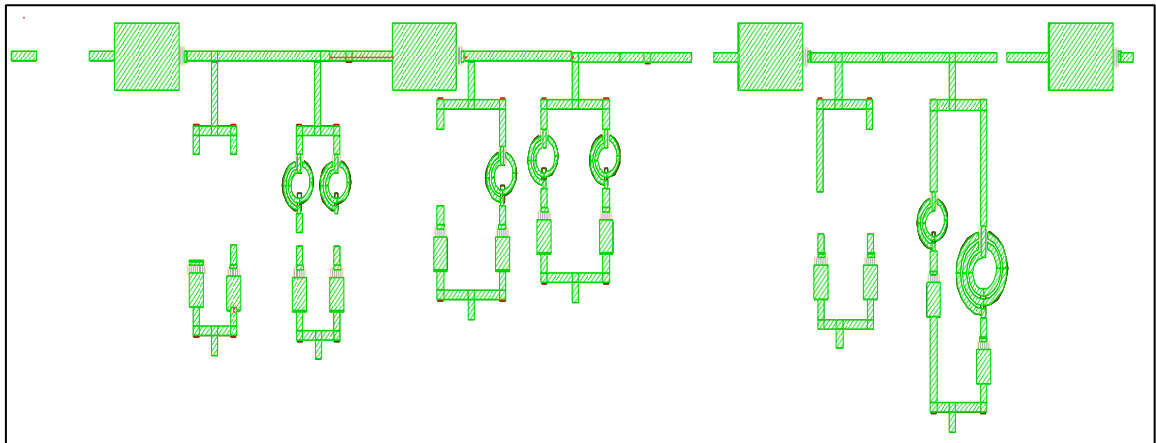


Figure 5.9. Layout and EM simulation of the 900 MHz-1800 MHz filter

The reason for the lack of inductors and capacities in the electromagnetic simulation is that the simulator cannot solve the multiplex structures because they are complex.

To complete the rest of the circuit, the structure after the electromagnetic simulation is considered a black box. It combines the s-parameters of the black box with the inductor and capacity to be added schematically and gives the result of the simulation closest to the reality.

The electromagnetic simulation for 900 MHz and 1800 MHz is given in Figure 5.10 and 5.11.

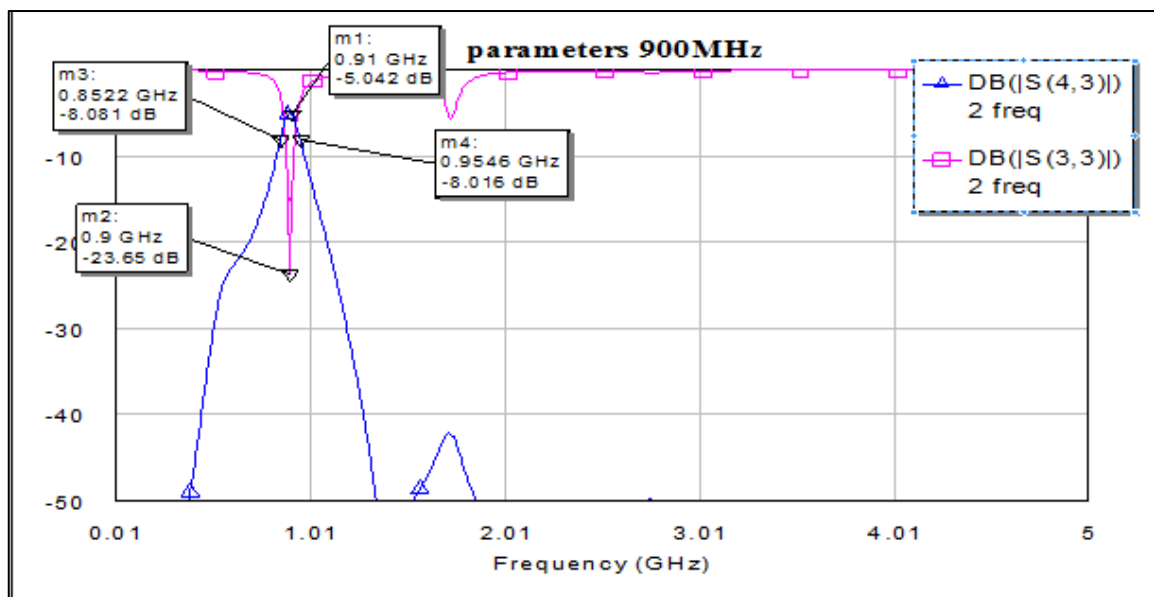


Figure 5.10. EM Simulation results for 900 MHz

According to the electromagnetic simulation results of the designed filter, for 900 MHz

insertion loss is decreased by 0.9 dB and return loss is improved by 3 dB.

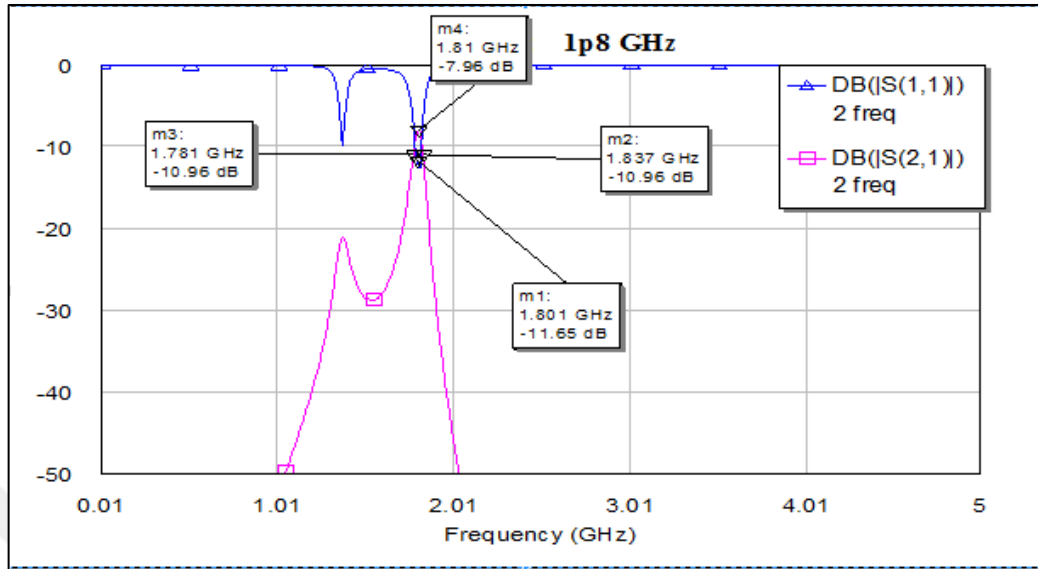


Figure 5.11. EM simulation results for 1800 MHz

For 1800 MHz, Insertion loss improved 0.8 dB and return loss is 11.65 dB which can be count as a matched circuit according to authorities [33].

## 6. CONCLUSION

In this thesis, a bandpass filter with 900 MHz-1800 MHz selectable center frequency is designed. To do the final design, designing a circuit with a frequency 900 MHz was first step to test if the design can be realized. Chebyshev low-pass filter constants were used for calculations. In the next step, the low pass filter was converted to a bandpass filter. The inductor and capacitance values in the circuit were calculated. Optimization was used because the inductor values were far from the realizable values. The desired inductor values were given during the optimization and future capacitances were determined depending on the inductor values. In the next stage, the inductor and capacitor with values found by optimization were replaced with actual inductors and capacitors. The nearest inductor values were chosen because the actual inductors were lack of variety. As the optimizer values were exceeded, a new optimization was required for the capacitors. After finding the optimal component values, the layout of the circuit is plotted. Microstrip lines were used to connect the circuit components. As the areas of the components were large, the length of the lines was determined so that the components did not overlap or approach each other. The longer the microstrip line is, the less induction caused by near components, however, as the length of the microstrip lines increases, the insertion loss in the circuit will also increase. In the last step, the electromagnetic simulation was applied for the layout of the circuit. There was an almost 1 dB difference between the results of the electromagnetic simulation and the schematic simulation. With reference to the insertion loss difference between Figure 4.6 and Figure 4.7, 1 dB was an expected difference. Therefore a second frequency could be added to the circuit.

When the band-pass filter design with the selectable center frequency of 900 MHz to 1800 MHz is performed, the calculation of frequencies cannot be made for the same circuit. Due to the calculation problem, the center frequency of the circuit was 1350 MHz, which is the average value and was calculated according to this value. As expected, the optimization was performed because the inductor values were well above the IC inductor values.

During the circuit design, the serial components were selected as common for 900 MHz and 1800 MHz. Parallel blocks to change the frequency are connected to the circuit by an external switch. Since the on-chip switch has a lot of parasitic capacity, the circuit does not operate



at 900 MHz and 1800 MHz. For this reason, the switches are connected externally. When the switches are connected outside the chip, the numerical results of the circuit are compatible with the specifications. In addition, since the quality factor of the inductors provided by the foundry was very low, the connection of some inductors was made out of the chip. Due to the low-quality inductors, 8 out of 32 circuit components have been implemented outside the chip and all the eight components are inductors and switches.

In the next step, the layout of the circuit is plotted. When drawing, the connection of the components is made with a microstrip. The electrical values of the microstrip were requested from the foundry. The electromagnetic simulation is provided for the circuit drawn. The reason for the layered layout, layout complexity and scale of components in the circuit, gives an error while running AWR electromagnetic simulation. As a result of the electromagnetic simulation, the resulting  $s$  parameters were considered as a black box. On the schematic, the inductors removed from the black box were added again and the schematic simulated. Electromagnetic simulation results were compared with the specifications that are aimed at the heading of the problem statement.

According to the electromagnetic simulation results of the designed filter, for 900 MHz insertion loss is decreased by 0.9 dB and return loss is improved by 3 dB. For 1800 MHz, Insertion loss improved 0.8 dB and return loss is 11.65 dB which can be count as a matched circuit according to authorities and the bandwidth of the circuit is almost unchanged for both frequencies.

Table 6.1. Comparison of designed filter and literature research

<b>Specs</b>	<b>[42]</b>	<b>[43]</b>	<b>[44]</b>	<b>[45]</b>	<b>Designed Filter</b>
Insertion Loss (s21)	1 dB	3 dB	5 dB	9 dB	5-8 dB
Return Loss (s11)	25 dB	50 dB	28 dB	12 dB	23-11 dB
3dB Bandwidth	25%	15%	%28	10%	11% - 2%
Tunable Center Freq(fc) Range	1.8 GHz- 3.2 GHz	2.9 GHz- 3.4 GHz	1.9 GHz- 3.0 GHz	6.8 GHz - 12.6 GHz	0.9 GHz – 1.8 GHz
Rejection@0.5*fc	30 dB	60 dB	20 dB	45 dB	38 dB - 55 dB
Rejection@1.5*fc	20 dB	40 dB	29 dB	46 dB	50 dB – 70 dB
Frequency Control Voltage	N/A	N/A	N/A	0-14 V	(-2 V) – (0 V)

During literature research an RFIC with selectable band band-pass filter operates at GSM band could not be found. Due to the high parasitic effects of the internal inductors in the circuit, 8 inductors were connected externally. This increases the dimensions and cost of the circuit but is the only selectable RFIC design on the GSM band. Improved circuit specifications that are insertion loss and rejection adds novelty to the circuit. The filter insertion loss is higher than the reference [42, 43, 44] but lower than article 45 according to the comparison of the designed filter specifications with the literature research. Return loss is lower in [42, 43, 44] articles that means these articles are better-matched circuits. 3 dB bandwidth percentage is the lowest bandwidth in the designed article which means the designed circuit has more selective bands compared to other articles given at table 6.1. Besides, 1.5\* fc rejection is also the highest in the designed circuit that means designed circuit makes better filtration on the high-frequency side.

To improve the circuit, inductors must be included inside of the chip, rather than being externally connected. A switch with a high  $f_0$  (center frequency) and inductors with high quality factors can be selected. For this, different foundry can be used. Because the inductors provided by the technology for the selected topology do not have a high quality factor. Besides, the inductor diversity is quite low. This makes designs with a large number of inductors difficult. In addition, the topology of the circuit can be changed, but the specs will be less challenging.

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