IMPROVEMENT OF IMAGE REJECTION FOR HARTLEY IMAGE REJECT RECEIVERS

by
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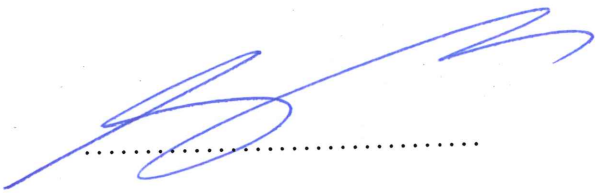
Assoc. Prof. Dr. Serkan Topaloğlu ..... 
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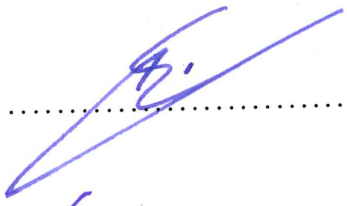
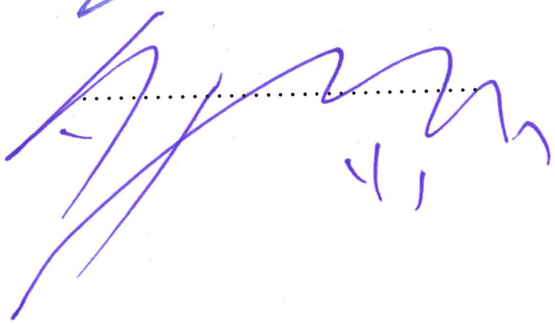
Prof. Dr. Ahmet Arif Ergin ..... 

Prof. Dr. Sıddık Yarman ..... 

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ABSTRACT

IMPROVEMENT OF IMAGE REJECTION FOR HARTLEY IMAGE REJECT RECEIVERS

In this thesis, a tunable amplitude compensation method is presented for Hartley image-reject topology which eliminates amplitude errors causing degradation in image rejection performances.

Firstly, different types of receiver topologies and solutions of these topologies for image signal problem are investigated as background knowledge. Especially, methods that need to be applied in these topologies to obtain sufficient image rejection ratios are studied for broadband systems. The presented solution of Hartley image reject topology for image signal problem is proven by mathematical expressions and supported by simulation results. The amplitude and phase errors of components used in the topology are identified. Also, the effects of these errors on image rejection ratios are investigated. In addition to the tunable amplitude compensation method for obtaining improvements of image rejection values, a non-tunable phase compensation method is also applied to the proposed design. The effects of the proposed tunable amplitude compensation method are measured on the designed receiver which covers 950-1450 MHz band. Improvement of image rejection values is presented. It is also shown that the necessity of filter banks could be eliminated by the proposed method.

Besides, the frequency synthesizer is another critical part of the receiver design. Tunable reference clock frequency method is presented as a spur reduction method for spurious signals which are caused by using fractional-PLL in frequency synthesizer design. It is shown that tunable reference clock frequency is applicable for frequency spread spectrum systems which have 200 us guard time. Up to 40 dB spur reduction is achieved for LO signals which are required for 950-1450 MHz receiver. Superior results are obtained when considering the communication standards requirements in terms of phase noise and spurious power response. Measurement performed using both proposed methods are evaluated by a comparison with the literature and similar commercial products.

ÖZET

HARTLEY GÖRÜNTÜ BASTIRMA ALICILARI İÇİN GÖRÜNTÜ BASTIRMADA İYİLEŞTİRME

Bu tez çalışmasında, geniş bantlı alıcılarda kullanılan Hartley görüntü bastıma topolojisinde görüntü bastırma performansının bozulmasına neden olan genlik hatalarını ortadan kaldırmayı amaçlayan ayarlanabilir genlik kompanzasyon metodu sunulmuştur.

Öncelikle farklı tipteki alıcı topolojileri incelenmiş ve görüntü problemine sunduğu çözümler incelenmiştir. Özellikle geniş bantlı sistemler için bu topolojilerin istenilen görüntü bastırma oranlarını elde edebilmek adına alıcı tasarımlarında izlenmesi gereken yöntemler irdelenmiştir. Hartley görüntü bastırma topolojisinin görüntü sinyali problemine getirdiği çözüm, ilgili denklemler ile gösterilmiş, sistem benzetimleri ile desteklenmiştir. Topolojide kullanılan komponentlerden kaynaklanan genlik ve faz hataları belirlenmiş, bu hataların görüntü bastırma oranlarını nasıl etkilediği gösterilmiştir. Görüntü bastırma seviyelerini iyileştirmek adına uygulanan ayarlanabilir genlik kompanzasyon metoduna ek olarak ayarlanamayan sabit faz kompanzasyon metodu tasarıma uygulanmıştır. Öne sürülen genlik kompanzasyon metodunun etkileri, geliştirilen ve 950-1450 MHz arasında çalışan alıcı tasarımı üzerinde ölçülmüş ve görüntü bastırma oranlarında iyileşmeler sağladığı sunulmuştur. Öne sürülen bu metot ile geniş bantlı sistemler için gerekli olan filtre bankası ihtiyacının ortadan kaldırılabileceği gösterilmiştir.

Ayrıca alıcı tasarımının bir parçası olan frekans sentezleyicilerde kesirli-faz kilitlemeli döngü kullanımında ortaya çıkan çıkıntı (spur) işaretleri, ayarlanabilir referans saat işareti metodu uygulanarak bastırılmıştır. Bu metodun 200 us koruma zamanı olan frekans atlamalı yayılı izge tekniği için de uygulanabilir olduğu, kilitleme süreleri ölçümleriyle gösterilmiştir. Bu yöntem uygulanarak 950-1450 MHz arasında çalışan alıcı tasarımı için gerekli olan LO sinyallerinde 40 dB'ye kadar çıkıntı sinyali bastırma oranları elde edilmiştir. Bu yöntemin uygulanmasıyla uydu haberleşme standartlarında belirlenmiş faz gürültüsü ve çıkıntı sinyal güç seviyelerinden daha üstün sonuçlar elde edilmiştir. Öne sürülen bu iki metodun uygulanmasıyla elde edilen ölçüm sonuçları, piyasada yer alan ürünler ve akademik çalışmalar ile karşılaştırılarak değerlendirilmiştir.

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LIST OF SYMBOLS/ABBREVIATIONS

α	Attenuation constant
ε	Dielectric constant
f	Frequency
I	In-phase
us	Microsecond
F	Noise factor
β	Phase constant
γ	Propagation constant
Q	Quadrature
c	Speed of light
v	Velocity
λ	Wave length

ADC	Analog to digital converter
AGC	Automatic gain control
AM	Amplitude modulation
CPW	Co-planar waveguide
DAC	Digital to analog converter
dB	Decibel
DC	Direct current
DSSS	Direct sequence spread spectrum
DRC	Design rule check
EA	Electronic attack
ENOB	Effective number of bits
EW	Electronic warfare
FHSS	Frequency hopping spread spectrum
FPGA	Field programmable gate array
GHz	Gigahertz
IESS	Intelsat earth station standards
IF	Intermediate frequency

ITU	International telecommunication union
MHz	Megahertz
MWO	Microwave office
kHz	Kilohertz
LNA	Low noise amplifier
LUT	Look-up table
LO	Local oscillator
P	Power
PCB	Printed circuit board
PFD	Phase frequency detector
PLL	Phase lock loop
RF	Radio frequency
SPI	Serial peripheral interface
SNR	Signal to noise ratio
TCXO	Temperature compensated crystal oscillator
THSS	Time hopping spread spectrum
V	Voltage
VCO	Voltage controlled oscillator
VCXO	Voltage controlled crystal oscillator

1. INTRODUCTION

Different systems are developing to ensure the continuity, the security of the communication and information security nowadays. Frequency hopping spread spectrum, which is a submethod of spread spectrum is one of the most popular methods. Spread spectrum methods have been developed against electronic attack (EA) and are used in not only military communication systems but also commercial communication systems for the continuity of communication and propagation [1].

Receivers are the critical sub-systems of both the EW and commercial wireless systems. There are several types of receiver topologies, and the most preferred ones are heterodyne, homodyne, image-reject and dual-IF heterodyne. These topologies have advantages and disadvantages due to the system configuration. Therefore, there are several research and projects on the receiver topologies and applications. Recently, wireless communication is on the rise, and many devices are sharing the same spectrum. Therefore, spectrum efficiency is one the crucial issue in wireless communication. The image signal is the main problem in the low IF-based receivers. If image signal effects are not mitigated, receiver systems performance is degraded due to the unpredictable image signal. That is the reason why image rejection is critical for receivers. Therefore, the receiver topologies are shaped by image signal interference problem [2-4].

Popularly, heterodyne topology is preferred by the receiver system due to ease of use and image rejection values. In this topology, a filter or filter bank is required to obtain sufficient image rejection values. For a narrow band system, a filter could solve the image problem. On the other hand, a filter bank is necessary for broadband systems whose passband bandwidth is specified according to IF frequency. Besides, Dual-IF heterodyne receiver topology is another solution for image signal problem in broadband systems. The image problem mitigation is guaranteed by selecting a second IF frequency whose center frequency is higher than the total bandwidth of the systems. While these approaches are providing the solution for image signal problem, they cause disadvantages in terms of complexity and form factor [5-7].

On the other hand, image rejection topology is guaranteed absolute image rejection in theory. Therefore, while creating a conceptual design, IF frequency and appropriate filter may be

disregarded upon on the application. However, there are some problems with this topology in the implementation phase due to the non-ideal response of the components. Image rejection efficiency is directly related to components' characteristics, especially regarding amplitude and phase response. In this topology, image rejection value degradation is caused by phase and amplitude errors. Even if image-reject receiver topology is implemented, a filter bank is preferred to use to achieve sufficient image rejection ratios [8].

Therefore, a lot of academic studies have been performed to eliminate implementation problems and therefore increase the image rejection efficiency of the topology. These studies are based on amplitude compensation, phase compensation or both. Besides, different approaches and methods are preferred to eliminate these errors.

In this study, improvement of image rejection is aimed by eliminating amplitude errors in Hartley image-reject topology. Both amplitude and phase errors also occur in the Hartley image reject topology due to non-ideal characteristics of the components. The aim of this thesis study is eliminating amplitude errors which exist between in-phase and quadrature section. The mixers, which are driven at optimum operating points by LO signal, are deteriorated due to applying DC voltage. The insertion loss of the mixer increases due to the deterioration. The DC voltage should be applied to the mixer according to the insertion loss comparison between in-phase and quadrature sections. So, the insertion loss which comes from in-phase and quadrature sections can be equalized at the output of both sections. Despite the thesis study is based on eliminating amplitude errors exists between in-phase and quadrature section, the phase errors also are investigated. The phase shift is performed by delayed trace method to optimize the phase errors. The complete phase compensation could not be provided by phase shift method due to the non-tunable characteristic. On the other hand, the phase shift has an improver impact on image rejection ratios also.

A similar method has been reported previously. However, details of the method have not been reported. Also, improvement of the image rejection values by using the same method and effects of this method on the desired signal has not been indicated. In the thesis study, the effect of applying the proper DC voltage and improvements are shown by simulations and measurement results [9].

The motivation of this thesis study is offering a tunable amplitude compensation method on Hartley image reject receiver topology. Moreover, this study aims to present an alternative

approach to the heterodyne receiver and dual-IF topologies for IF-based receivers and eliminating filter bank usage. Therefore, Hartley image-reject topology is built with discrete elements and the effects of components characteristics are investigated in the 950 MHz to 1450 MHz band. A remarkable improvement of image rejection by applying tunable amplitude compensation method is intended. Also, the effects of these methods are investigated both on the desired signal and the image signal.

In addition to image rejection improvement, use of frequency synthesizers in the receivers are investigated, too. The other critical part of the IF-based receivers is frequency synthesizers. The high accuracy is critical for the systems due to spectrum efficiency. The PLL based synthesizers are commonly preferred to generate local oscillator signal with high accuracy. There are two types of PLLs; integer type and fractional type. Both the fractional and integer type PLL provides the solution for receivers regarding small tuning step sizes. However, VCO tuning step sizes are equal to PFD frequency for integer type PLL. So, PFD frequency needs to be as small as frequency tuning size. However, smaller PFD frequencies cause phase noise degradation. On the other hand, the phase noise degradation phenomenon is not valid for the fractional type PLLs. Sub-Hz grade tuning step sizes could be obtained without any phase noise degradation by fractional type PLL — nevertheless, fractional PLLs cause spurious response due to its operation. Some of the spur products could be removed by the loop filter of the PLL, but spurs that locate in the pass-band of the loop-filter could not be eliminated. The spur location is specified by PFD frequency and fractional part of the PLL feedback divider value. Moreover, the desired frequency could be obtained by different PFD and feedback divider combination. If the PFD frequency is changed, spur location will move. Therefore, spur products could be shifted to the attenuation region of the loop-filter. Thus, spur products could be eliminated by changing PFD frequency. Changing PFD frequency could be achieved by changing reference clock frequency or changing reference clock dividers [10].

Therefore, many studies are conducted to analyze the effects of this spurious response and to eliminate these effects. Mitigation of these effects could be achieved by eliminating spurious response. The proposed tunable reference clock method offers a solution for the spurious response of the fractional PLLs [11,12].

The proposed tunable reference clock method is reported by both academic studies and commercial projects. However, only spur reduction is investigated in those studies. On the

other hand, the lock-up times are critical for receivers which use frequency hopping spread spectrum. This method should be investigated regarding locking speeds [10-12].

The motivation of this study about frequency synthesizers is the design of a spurious free synthesizer design for fast frequency hopping spread spectrum receivers by the proposed tunable reference clock method. Therefore, a frequency synthesizer was designed, and the proposed spur reduction method is applied to this design. Effect of the proposed method is investigated both regarding spur reduction and lock-up times.

Within the scope of this thesis study, the working principals of downconverter topologies will be explained in the second chapter. Moreover, the methods, which could be applied to mitigate image problem in receiver topologies for broadband FHSS receivers, will be investigated. Also, essential RF components which are commonly used in these topologies will be presented as a summary.

In the third chapter, receiver design parameters will be discussed. Also, the simulation-based result of effects of amplitude and phase error on Hartley image reject topologies will be included. Besides, components errors, the effect of these errors on the proposed structure, and compensation approaches will be investigated on the proposed Hartley image rejection receiver design. Proposed compensation method and implementation details will be expressed. How the spur problem occurs in PLL, spur effects, and how the proposed method works as a solution are also discussed in chapter 3.

The downconverter design details and implementation of the proposed method will be given in chapter 4 with the measurement results

The spurious-free synthesizer design details, implementation of the proposed spur reduction method will be presented in chapter 5. Moreover, measurement results will also take part in this section.

Chapter 6 belongs to the conclusion section, and the results of the thesis will be given in this chapter. Also, the outlook of the thesis study and comparison with previous studies and products will be discussed.

2. DOWNCONVERTER TOPOLOGIES AND DESIGN CONSIDERATIONS

2.1. DOWNCONVERTER TOPOLOGIES

There are several parameters that are specified for achieving an optimum downconverter topology. These are the modulation type, communication system configuration, signal noise levels and the existence of interferer or adjacent channels. The convenience of the topology can be varied from one application to another. Complexity, cost, power consumption and form factor are other parameters to care for an optimum topology. The detailed information regarding different topologies is given in this chapter.

2.1.1. Heterodyne Receiver

The heterodyne receiver topology is the most preferred topology in the systems for several years. Mixers, low-pass/bandpass filters, and low noise amplifiers are the main building blocks used in this topology. The basic block diagram is shown in Figure 2.1 below.

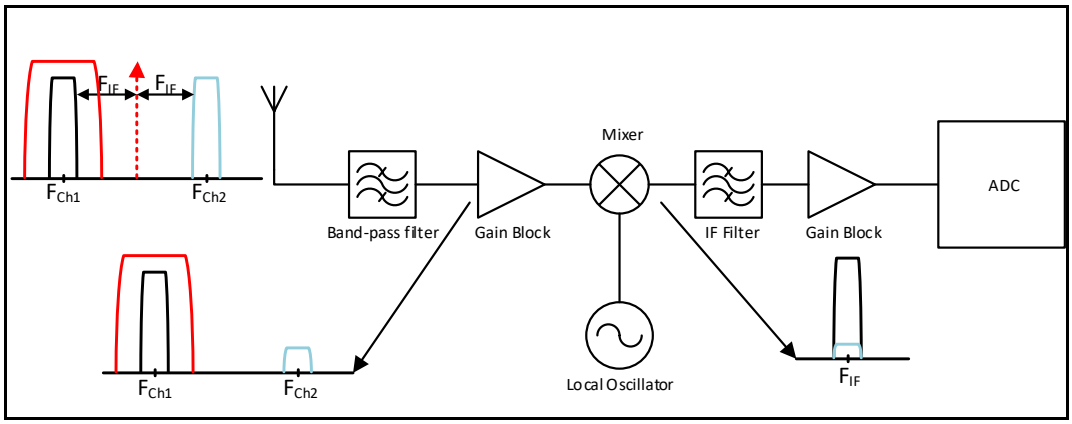


Figure 2.1. Block diagram of the heterodyne receiver

Low power signal that is received by the antenna or from the output of another system is applied to RF input port of the mixer. Also, the LO signal is applied to the LO port of the mixer whose frequency is arranged by the synthesizer according to the relevant channel frequency. After mixing operation, the high-frequency RF signal is down-converted to a

lower frequency that is suitable for sampling. Therefore, sampling could be conducted by analog to digital converter (ADC) efficiently. Achieved 'relatively lower' frequency is called Intermediate Frequency (IF). The performance of frequency conversion operation and the choice of parameters play a crucial role in the cumulative performance of the receiver.

After down-conversion, harmonics and leakage will occur due to the mixer's natural behavior. Unfortunately, mixer creates not only the desired IF signal but also other unwanted signals due to the multiplication of undesired signals which exist at the inputs of the mixer. In other words, other signal components and harmonics at the channel might affect the performance of the receiver. The output response of a mixer is shown in Figure 2.2.

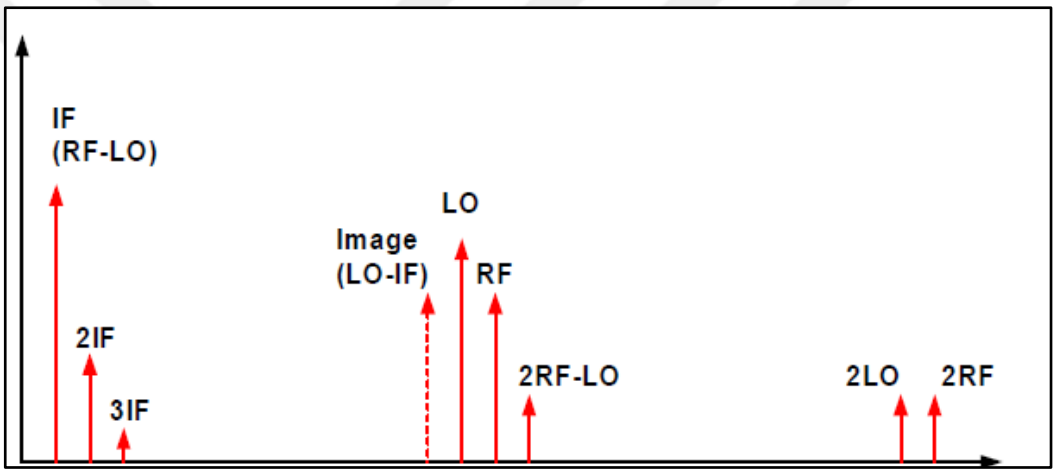


Figure 2.2. Frequency spectrum response of a mixer

One of the signals that are located symmetrically from LO is the desired signal, and the other one is an unwanted signal, which could be an interferer or an adjacent channel. The unwanted signal is also called the image signal. In heterodyne receiver topology, main RF signal and unwanted image signal will be down-converted to same IF frequency. The wanted, and the image signal is shown in Figure 2.3.

As a result, two signals interfere with each other. Moreover, necessary information in the desired signal may become inaccessible after sampling. It is possible that the image signal power may be higher than the desired signal power. In such a case, the image signal must be removed before the mixer to detect the desired signal. The system design needs to have a proper image rejection ratio to annihilate the effect of the image signal or decrease it at least.

On the other hand, IF & LO frequency selection and image rejection ratio have to be well calculated when considering image signal in system design. The general way to reject image

signal is placing an image reject filter before the mixer in a heterodyne receiver. Choosing a proper image reject filter is a trade-off in terms of the system performance. At very low IF frequencies, applying a channel selection filter will be relatively easy. The channel selection filter will have low insertion loss and a high-quality factor. However, when IF frequency gets smaller, rejection of the image signal at RF frequencies will decrease because a proper filter implementation will be hard due to the image will be located close to the desired signal. When IF frequency gets higher, image signal will be further away from the desired signal so rejection of image signal could be more relaxed.

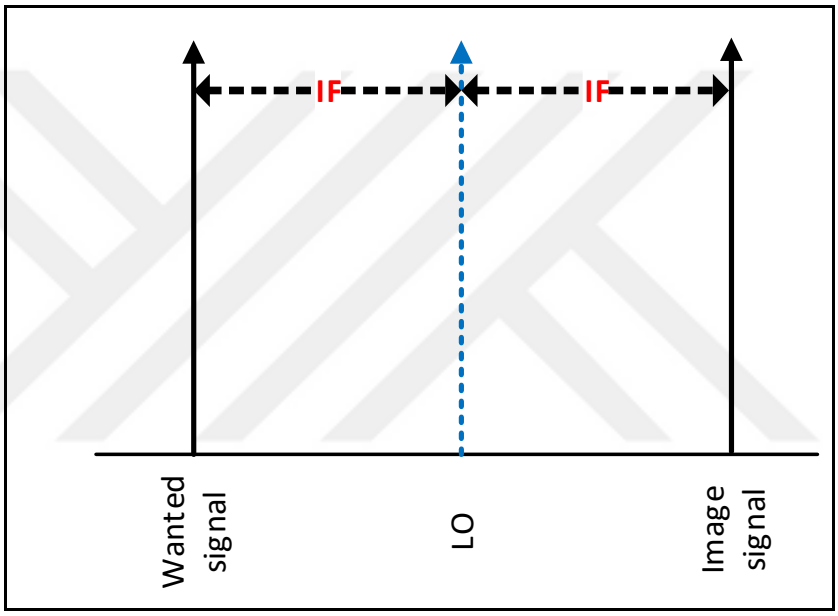


Figure 2.3. Wanted and the Image signal

On the other hand, at higher IF frequencies, channel selection filters have more insertion loss, and ADC has to be capable of high frequency IF signal. In brief, there is a trade-off between channel selection and image rejection in heterodyne receivers. The poor image signal rejection causes dramatically reducing receiver sensitivity performance so choosing image rejection is proper way in this trade-off. Besides the channel selection could be simple in a new generation of analog to digital converters and FPGA implementations. Also, the LO signal could be lower and higher than the desired signal. If the difference between the LO and the desired signal is equal to IF frequency, in both cases the desired signal will be down-converted to IF frequency. This situation called high-side injection or low-side injection. While choosing low side or high side injection, all frequency bands which include image signal must be taken into account and the frequency must be chosen which existence probability of the image signal is low [3,13-16].

2.1.2. Dual-IF Heterodyne Receiver

The trade-off between image rejection and channel selectivity which was described in the previous section could be optimized with the Dual-IF method. Nowadays, most receivers down-convert RF signal to IF frequencies with two stage. This method is called Dual-IF heterodyne architecture. Dual-IF heterodyne architecture is shown in Figure 2.4.

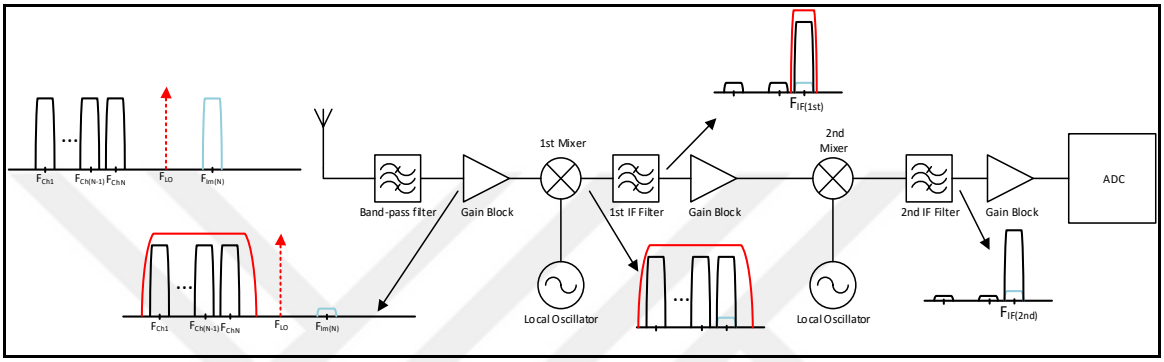


Figure 2.4. Block diagram of a dual-IF heterodyne receiver

In all stages, filtering and amplifying is applied to the signal while down-converting. At the first stage, the image signal problem is tried to be reduced. The desired signal is down-converted to a higher IF frequency. Because of the higher IF frequency, image signal will occur far-away from the desired signal due to IF frequency. This situation will allow filtering image signal easily. Moreover, the desired signal should be down-converted to a very low IF frequency which is easy to sample by ADC at the second stage. Before down-conversion at the second stage, channel selection is applied to high- IF signal with a proper high Q filter. On the other hand, the image problem is still valid for the second down-conversion stage. For example, very low IF frequency should be higher than half of the system bandwidth. However, there are different components more than a single heterodyne receiver, so these components cause an increase to the noise figure of the system and a decrease the receiver sensitivity. In this case, ADC cannot sample the signals correctly. The other disadvantage of Dual-IF receiver is the area due to including extra filters and amplifiers. Especially if low-resolution ADC is used in the system, extra amplifiers have to be used to sample at low power inputs. Power requirements of the system will increase due to this reason. Also, mixers cause extra harmonics and spurs, so frequency planning is the crucial subject in Dual-IF receiver design. Despite the disadvantages, Dual-IF receiver method is the most used method in receiver designs [3,13-17].

2.1.3. Homodyne Receiver

The other down-conversion topology is the homodyne receiver topology. The block diagram of the homodyne receiver is shown in Figure 2.5.

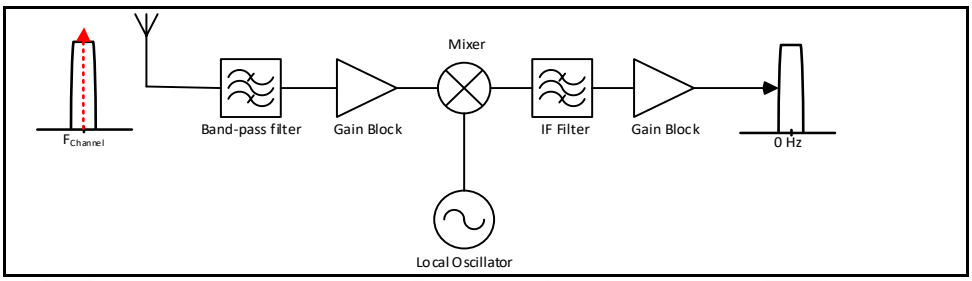


Figure 2.5. Block diagram of a homodyne receiver

In this topology, the modulated RF signal is down-converted to a modulated zero-IF signal by just one down-conversion stage. The image rejection problem does not exist in this topology. The desired signal center frequency is the same as LO frequency, and only high Q channel selection filter is enough for channel selection. This topology is called as direct conversion due to a single down conversion stage or zero-IF.

This method is only used in Double-Sideband AM systems because down-converted IF signal exist and overlap both negative and positive side of the spectrum. If the communication system uses a phase or frequency modulation techniques, the down-converted IF signal should have in-phase and quadrature components. Because, spectra of the frequency modulated or phase modulated signals have different information on both sides, the signal needs to separated quadrature phase to use this topology. Although the homodyne receiver is easy to implement compared with the heterodyne receiver, the homodyne receiver has a problem that does not exist in heterodyne receiver topology. Homodyne receiver topology that is for phase and frequency modulated systems is shown in Figure 2.6 [3, 13-17].

2.1.4. Image-Reject Receiver

This architecture achieves image rejection through phase cancellation. Therefore, while creating a conceptual design, IF frequency and appropriate filter may be disregard upon on the application. This topology ensures image rejection owing to the down-convert input

signal (both the desired and the image signal) and creating a 90-degree phase shift in other words creating Q and I and then adding them with 90 shift again, so image rejection achieved. Hartley image-reject architecture is shown in Figure 2.7 [18-20].

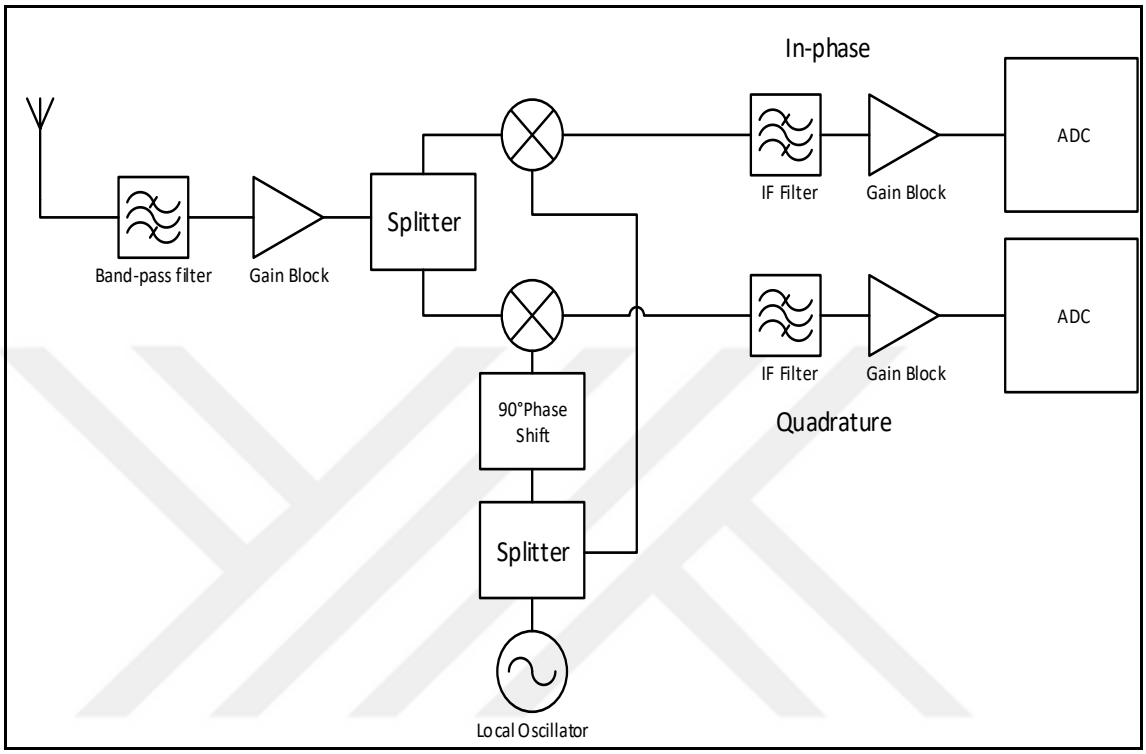


Figure 2.6. Block Diagram of homodyne receiver for phase or frequency modulated systems

Moreover, the mathematical proof is stated below [19]. Assume that,

$$w_{LO} = Local\ ossilator\ frequency$$

$$w_{RF1} = Desired\ RF\ signal\ frequency$$

$$w_{RF2} = Image\ RF\ signal\ frequency$$

$$\cos(w_{RF1}) = Desired\ RF\ signal$$

$$\cos(w_{RF2}) = Image\ RF\ signal$$

$$\cos(w_{LO}) = Local\ ossilator\ signal$$

$$\cos(w_{RF1}) + \cos(w_{RF2}) = Input\ RF\ signal$$

When the input signal is applied to the upper mixer, then the IF stage is obtained:

$$(\cos(w_{RF1}) + \cos(w_{RF2})).\cos(w_{LO}) = \cos(w_{RF1}).\cos(w_{LO}) + \cos(w_{RF2}).\cos(w_{LO}) \quad (2.1)$$

$$\frac{1}{2}.(\cos(w_{LO} - w_{RF1}) + \cos(w_{LO} + w_{RF1}) + \cos(w_{RF2} - w_{LO}) + \cos(w_{RF2} + w_{LO})) \quad (2.2)$$

After filtering is applied, Equation (2.3) is obtained and called in-phase part of the signal.

$$\frac{1}{2}.(\cos(w_{LO} - w_{RF1}) + \cos(w_{RF2} - w_{LO})) \quad (2.3)$$

When the input signal is applied to below mixer, then at IF stage:

$$(\cos(w_{RF1}) + \cos(w_{RF2})).\sin(w_{LO}) = \cos(w_{RF1}).\sin(w_{LO}) + \cos(w_{RF2}).\sin(w_{LO}) \quad (2.4)$$

$$\frac{1}{2}.(\sin(w_{LO} - w_{RF1}) + \sin(w_{LO} + w_{RF1}) + \sin(w_{LO} - w_{RF2}) + \sin(w_{RF2} + w_{LO})) \quad (2.5)$$

After applying a filter, Equation (2.6) is obtained and called quadrature part of the signal.

$$\frac{1}{2}.(\sin(w_{LO} - w_{RF1}) - \sin(w_{RF2} - w_{LO})) \quad (2.6)$$

When 90° phase shift is applied to Equation (2.6), Equation (2.7)is obtained.

$$\frac{1}{2}.(\sin(w_{LO} - w_{RF1} + 90) - \sin(w_{RF2} - w_{LO} + 90)) = \frac{1}{2}.(\cos(w_{LO} - w_{RF1}) - \cos(w_{RF2} - w_{LO})) \quad (2.7)$$

Equation (2.3) and Equation (2.7)are added, then image signal will be canceled out. Equation (2.8) is obtained without image signal.

$$\frac{1}{2}.(\cos(w_{LO} - w_{RF1}) + \cos(w_{RF2} - w_{LO})) + \frac{1}{2}.(\cos(w_{LO} - w_{RF1}) - \cos(w_{RF2} - w_{LO})) \quad (2.8)$$

$$= \frac{1}{2}.(\cos(w_{LO} - w_{RF1}) + (\cos(w_{LO} - w_{RF1})) \\ = \cos(w_{LO} - w_{RF1}) \tag{2.9}$$

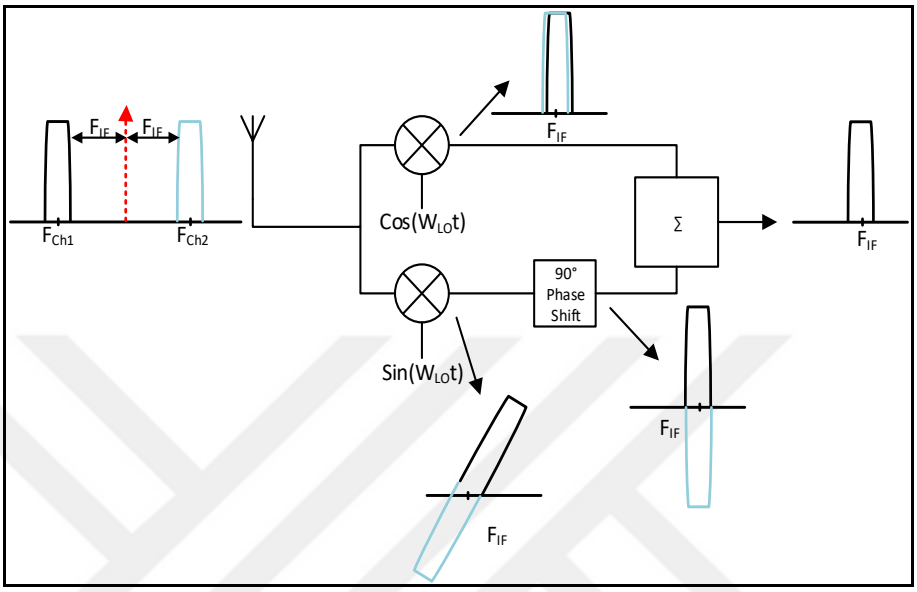


Figure 2.7. Hartley image-rejection topology

Image signals cancel each other, and only the desired signal will stay back without the existence of an image signal. Mathematically, the components in the architecture are assumed to be ideal components, and each of them is identical. As a result, the infinite image rejection is obtained. However, components in architecture are not ideal, and some parameters play an important role in image reject efficiency of architecture in a practical case. In an image-reject downconverter, image-rejection ratio depends on phase and amplitude errors between in-phase and quadrature signals. Image rejection ratio could be expressed with the following equation [19].

$$IR = -10\log(\frac{1+A^2-2A\cos\emptyset}{1+A^2+2A\cos\emptyset}) \tag{2.10}$$

A: $Amplitude\ Error$

$\emptyset$: $Phase\ Error$

The amplitude error includes cumulative amplitude and the phase errors between the in-phase and quadrature part, so any of the components in the design that causes amplitude and phase difference between ports causes degradation of the image-reject ratio. Achieving perfect image rejection is almost impossible for implementations of this architecture with

discrete components due to the amplitude and phase errors in components. In other words, these errors prevent to achieve absolute image rejection. Achieving necessary image-rejection is relatively easy for narrowband systems, but more challenging for wide-band systems [3,13-20].

2.2. RECEIVER DOWNCONVERTER TOPOLOGIES FOR WIDEBAND FHSS

Image signal creates significant problems in heterodyne receivers in terms of proper operation of the receiver. A filter with a high image rejection ratio is required to avoid image problem. However, this solution does not make much sense in broadband systems especially in a broadband frequency hopping systems. In general, systems that include only an image reject filter have a fix carrier frequency or a narrow bandwidth. Only one image reject filter provides a solution for narrowband systems but this solution is not sufficient for broadband systems. In FHSS systems, the center frequency of the carrier is continuously changed. The center frequency of the desired channel and the center frequencies of the other channels are changed at the same time. For this reason, another channel may be an image signal for the desired receiving channel.

For these systems, the two methods usually are applied. One of the methods is to place a filter bank before the mixer. At the input of the receiver, several narrow bandpass filters with different center frequencies are used. Heterodyne down-converter topology with filter bank is shown in Figure 2.8. Also, a switch must select the filter that will operate according to the carrier frequency. In this topology, there are some difficulties in practice. First of all, the bandwidth of the bandpass filters is tightly coupled to the IF frequency. Band-pass filter bandwidth should be narrower twice than the IF frequency. Considering the image rejection values of the band-pass filters, the bandwidth of filters should be up to %75 of twice than the IF frequency. Furthermore, it is necessary to arrange the bands without dead spots, which means that the filters will have to be overlapped. If the L band frequency hopping system is considered, the entire band from 950 MHz up to 1450 MHz should be covered with filters. Generally, the IF frequency of the downconverters is 70 MHz. For the image rejection value to be sufficient, the bandwidth of the filters must be 100 MHz. For this reason, for an L-band system, it must be used at least five band-pass filters to cover the entire band. For a particular design, these filters cannot be found easily on the market. Therefore, all these filters have to

be designed carefully. If these filters are designed by microstrip design method, filters will take up considerable space due to the wavelength. For these reasons, filter bank method brings difficulties in terms of form factor, time and cost. Especially form factor disadvantage limits the usage of applications.

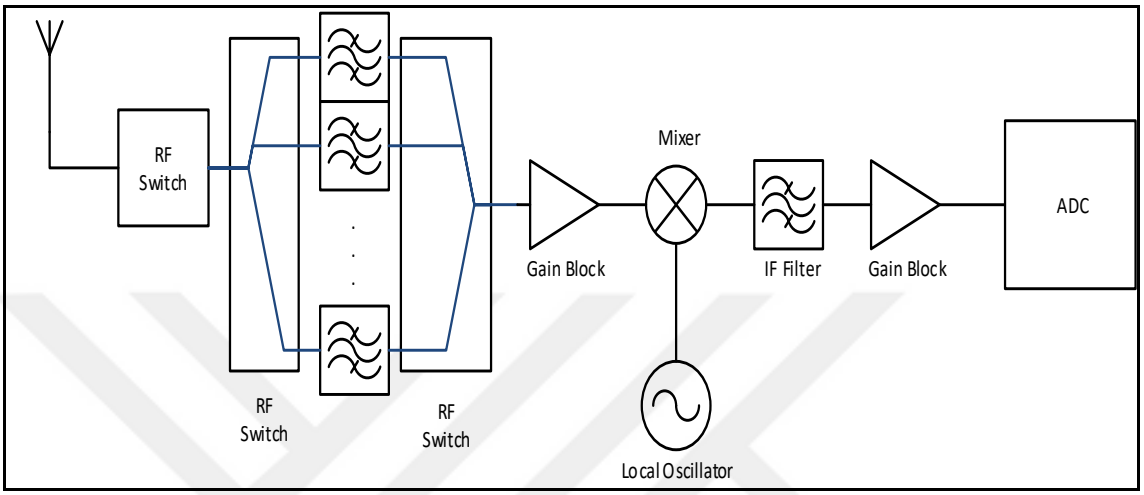


Figure 2.8. Heterodyne down-converter topology with the filter bank

Another topology is the Dual-IF Heterodyne Receiver architecture to achieve high image rejection. In this topology, the carrier signal is down-converted to IF frequency in two stages to prevent image signal distortion effect. There are two IF frequencies. One of these is the desired IF output frequency for ADC input, and the other one is higher than IF output frequency which is necessary for improving image rejection ratio**.** Due to the image signal that is outside of preselection filter, image signal power will be decreased. In general, due to out of band rejection characteristic of the preselection wide bandpass filters, image signal could not be absorbed completely. Depending on the RF input frequency, the second IF frequency must be adjusted meticulously.

Alternatively, there is an architecture which is called image reject architecture. Theoretical background of the image rejects architecture is given in chapter 2.1.4. As mentioned before, there are some limitations due to amplitude and phase mismatches. When these problems are solved, this topology is the optimal solution for several applications. This study focuses on the implementation of down-converter by using image rejection topology, and degradation of the image reject ratio due to amplitude difference and offer a solution to this serious problem [8, 21, 22].

3. SYSTEM DESIGN AND SIMULATIONS

This chapter focuses on the design considerations as mentioned in the previous sections. Simulations, design approaches and design steps, explanations and implementation of proposed design take part in this chapter.

3.1. SYSTEM DESIGN

Design approaches and simulations of these solutions have to be done before starting design. Based on these simulations and system needs, the design specifications also have to be defined therefore these details are examined in this chapter.

3.1.1. Receiver Design Parameters

A downconverter which supports Frequency Hopping Spread Spectrum satellite communication systems is investigated. The system performance is defined by some parameters such as bandwidth, gain, sensitivity and image signal rejection. Moreover, the goals of this study are defined by analyzing products performances which are in the market [23-25]. The main subject of the study is implementing downconverter and achieve at least these parameters. These parameters are given the next sections.

3.1.1.1. Bandwidth

Most of the satellite system uses 950-1450 MHz frequency band as downconverter input. Independently from the system frequency band, L band input and output exist for both transmitter and receivers. The reason for this situation is using different frequency bands used for different applications and purposes. Table 3.1. shows frequency bands of the different satellite systems.

Downconverter or receiver which operates at L band is used from all these systems as a common downconverter. In general, another downconverter is placed to down-convert the desired signal to L band which is located within 500 MHz bandwidth. That is enough to

down-convert the desired signal to IF frequency for L band downconverter. Also, frequency hopping is implemented in L band downconverter or up-converter because this is relatively easy with respect to an implementation in upper bands. For this reason, a downconverter that covers the 950-1450 MHz band is studied and implemented.

Table 3.1. Satellite frequency bands [26]

Band	**Down-link (MHz)**	**Up-link (MHz)**
C Band	3700-4200	5925-6425
X- Band (Military)	7250-7745	7900-8395
Ku	FSS:10700-11700	FSS:14000-14800
	DBS:11700-12500	DBS:17300-18100
	Telecom:12500-12750	Telecom:12500-12750
Ka-Band	26000-40000	26000-40000
L Band	800-2150	800-2150

3.1.1.2. Image Rejection

Image rejection ratio concept and importance for downconverter are mentioned in the previous sections. An optimum value for image rejection is difficult to define. On the other hand, several products ensure at least 40 dB image rejection. In this study, at least 40 dB image rejection is targeted [27,28].

3.1.1.3. Gain Control

Gain control is another critical parameter for the receiver. In runtime, the power of the desired signal could be changed dynamically, or signal is needed to be amplified to higher levels. Both these issues affect the system performance. Gain control usually is implemented by measuring the power level of the signal from the different point of the receiver. Also, the receiver is applied required parameters to a high-frequency path like attenuation or switching to the high gain path concerning measured power level. This operation called as Automatic Gain Control (AGC). This method is not implemented in this study, and the incoming signal

has to be monitored, and the required operation is applied manually. In some applications, the specified minimum signal may need to be amplified to ADC's full-scale input level that is located in the demodulator. That makes it possible to sample the desired signal with all effective number bits of ADC. The downconverter, which is designed for general purpose, have to provide high gain to provide this situation. Similar downconverters and receivers are investigated and gain control range should be about 70 dB. [23-25]

3.1.1.4. Sensitivity

Receivers processes and constitute meaningful words from shallow power signals. The signals have to be amplified. If the amplification value is lower then the added noise power or signal power is lower than the noise power, the signal could not be sampled by the demodulator. Therefore, defining the sensitivity of a receiver is so critical. Minimum detectable signal power or sensitivity depends upon several parameters. One of the most critical parameters is the noise figure. The noise figure of a receiver specifies how much noise power is added from receiver input to demodulator input. In general speaking, this value equals ratio between output SNR of the downconverter and input SNR of the downconverter. Amplifiers, filters and mixer work for a proper sampling of the desired signal. By the way, an extra noise power added to the signal after all these operations. Amplifier blocks increase the amplitude of the signal, and this increase is higher than the noise values that added after the amplification process. Thus added noise power after amplification is less effective in system noise figure, so the cascaded noise figure equation is given in Equation (3.1). As a result, this knowledge is used for proper component selection and creating block design.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 . G_2} + \cdots + \frac{F_{n-1} - 1}{G_1 . G_2 \ldots G_{n-1}} \tag{3.1}$$

The sensitivity of a receiver specifies minimum signal level which over a certain quality. In general, the quality of the signal determines from SNR for the analog system and bit error rate for digital systems. Therefore, sensitivity depends upon several parameters like required SNR, ADC number of bits, ADC sampling method, communication standards, the bandwidth of the channel, and so forth. In this study, the sensitivity of the downconverter could not be adequately defined, because designed downconverter is not related to any

communication standard then the SNR or bit error rate could not be specified. Moreover, downconverter does not contain demodulator block so ADC parameters also could not be specified so sensitivity [17].

3.1.2. System Design and Simulations

In this section, conceptual design and system modeling with the help of computer-aided design tools will be discussed before starting the receiver design. The simulations will cover the receiver topologies described in chapter 2.1. First, the image-reject receiver topology is examined. The Hartley image reject receiver topology is adapted to AWR Visual System Simulator program excluding other receiver components. Mathematical proof of the image reject receiver topology is checked by simulations. System diagram of the Hartley image reject receiver topology built in AWR design environment is shown in Figure 3.1.

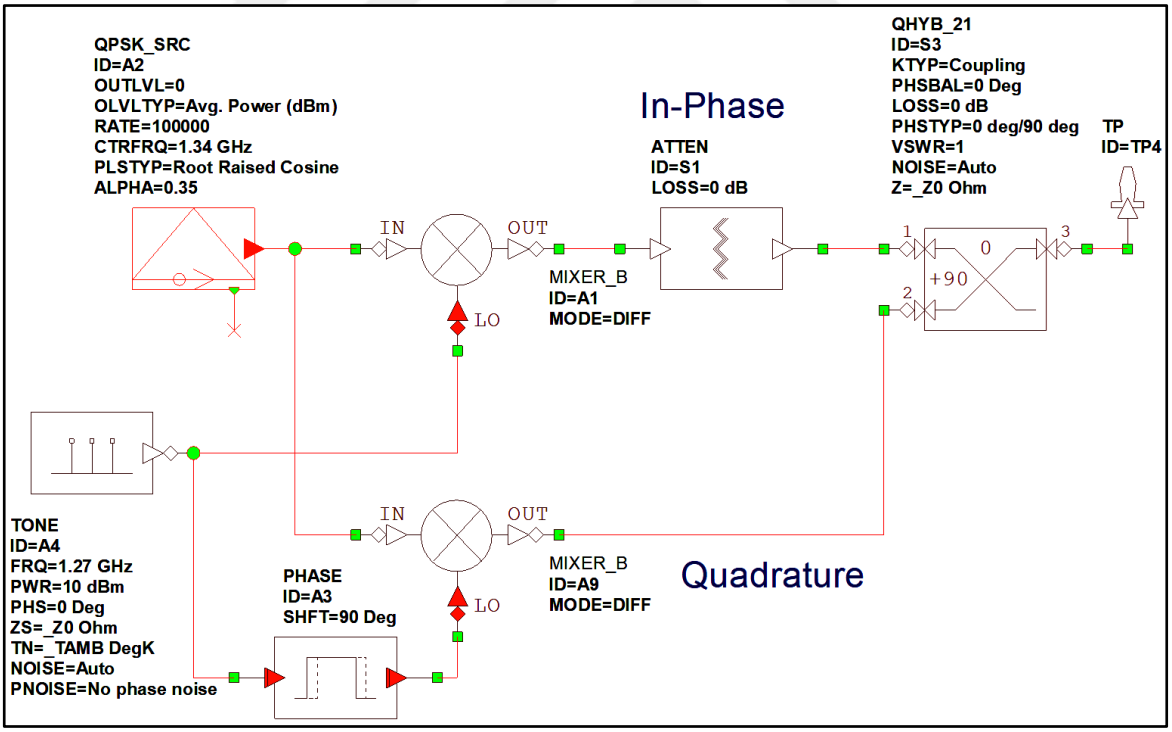


Figure 3.1. AWR model of Hartley image reject topology

Two identical mixers are placed. These mixers are used to down-convert RF signal to IF band. One of the mixers is used to generate in-phase component while the other creates the quadrature component of IF signal. Again, the same signals regarding phase and amplitude are applied to both mixers.

On the other hand, two different signals in term of phase are applied to LO ports such in Hartley Image Receiver topology. The source of the LO signals is the same, but a 90-degree phase shift is applied to one of the LO signals by using phase shifter before going into the mixer at the bottom. Outputs of these two mixers generate in-phase and quadrature parts of IF signals. In the ideal case, I (In-phase) and Q (Quadrature) parts are the same in terms of power level and center frequency. Then, I and Q signals are summed by using a quadrature coupler. Notice that there is again a 90-degree phase difference between input ports of quadrature coupler. As seen in Figure 3.1, the LO signal frequency is 1.27 GHz, and the desired modulated signal frequency is centered at 1.34 GHz. In such configuration, the desired signal is finally converted to 70 MHz which is the intended IF value. When IF signal is 70 MHz and the LO signal is 1.27, any arbitrary signal centered at 1.2 GHz is called the image signal of the desired 1.34 GHz signal. Therefore, the 1.2 GHz image signal should be removed from the system.

Ideally, there is no phase and amplitude mismatch between I and Q segments. Therefore, image rejection will be infinite, which is impossible to achieve in practice. Figure 3.2 shows the down-converted desired signal at the spectral view.

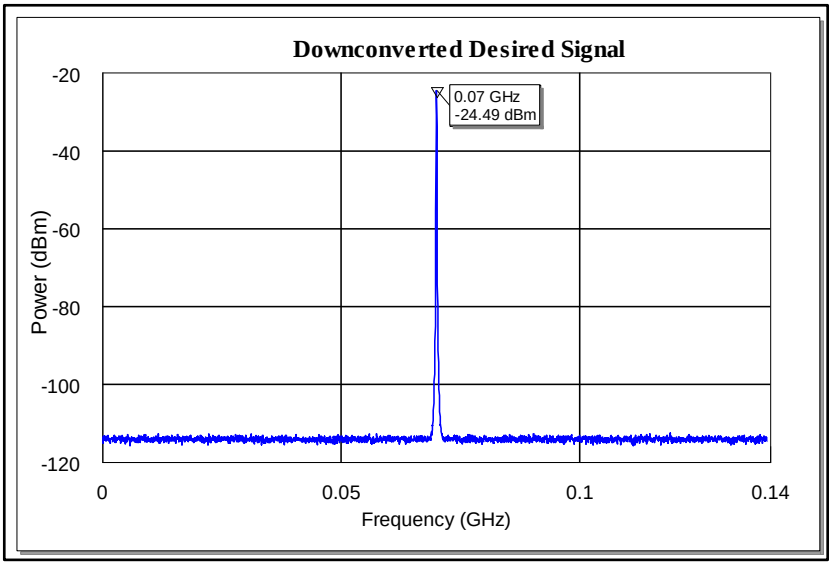


Figure 3.2. Spectral view of the down-converted desired signal

It is expected that if the frequency of the source is adjusted as the image signal frequency which is 1.2 GHz, down-converted image signal will not exist at 70 MHz. The image signal rejection will be infinite, and therefore the down-converted signal will be disappeared in the noise floor. Figure 3.3 proves this claim via a spectral view.

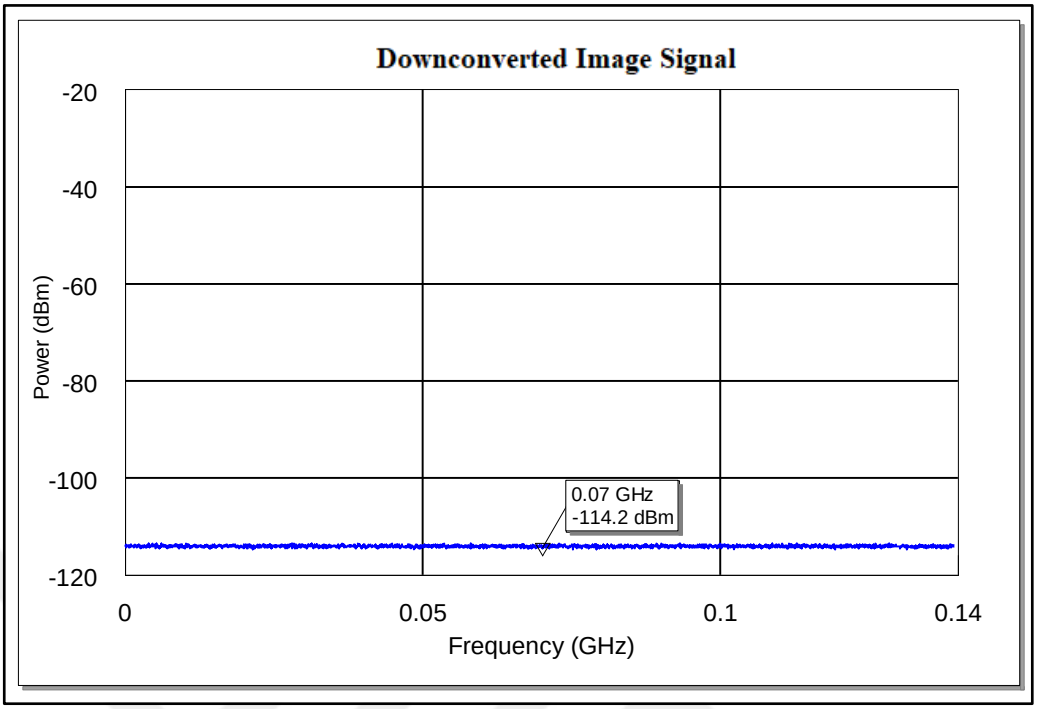


Figure 3.3. Spectral view of down-converted image Signal

If input port connections of quadrature coupler are switched; in other words, 90-degree phase shift is applied to I component instead of Q components, the desired signal is going to occur at lower sideband, which is 1.2 GHz. The modified system diagram is shown in Figure 3.4.

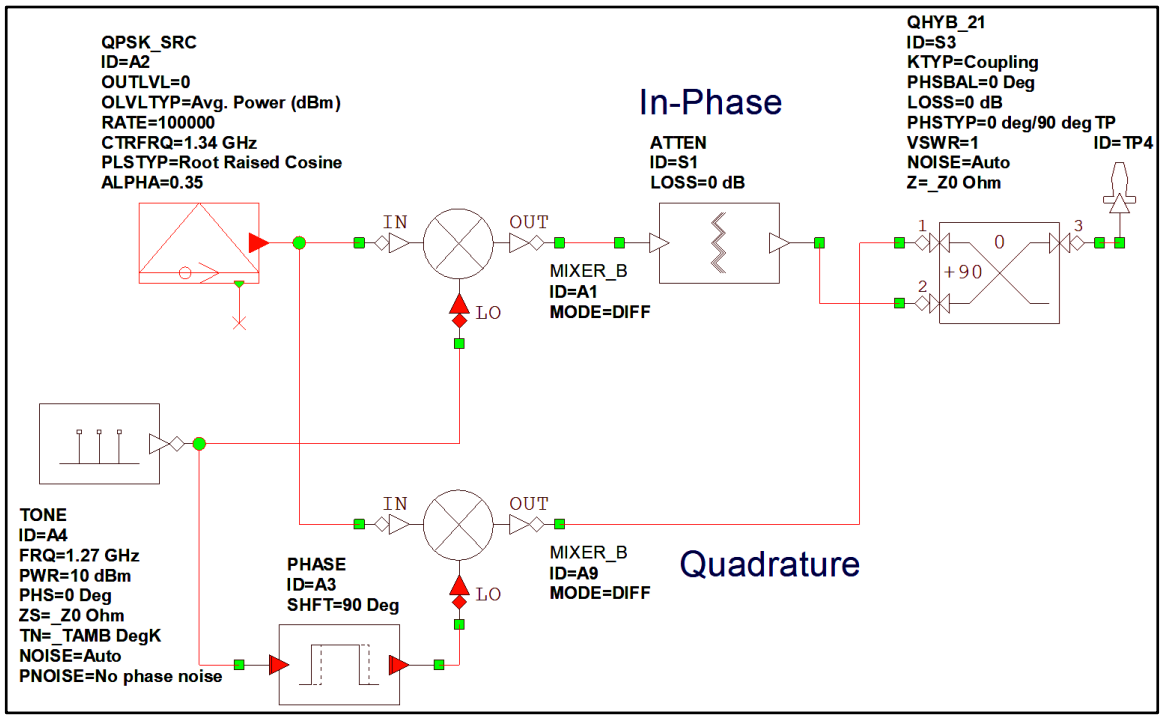


Figure 3.4. AWR model of modified Hartley image reject topology

Then, 1.2 GHz will become the desired signal, and 1.34 GHz becomes image signal for this case. Spectral view of the down-converted lower-sideband desired signal and the undesired image signal is respectively shown in Figure 3.5 and Figure 3.6.

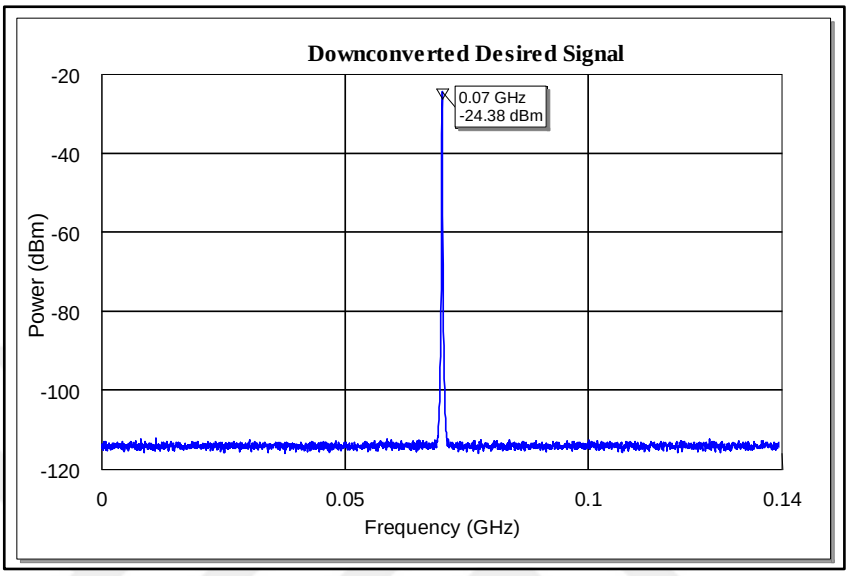


Figure 3.5. Spectral view of the down-converted desired lower-sideband signal

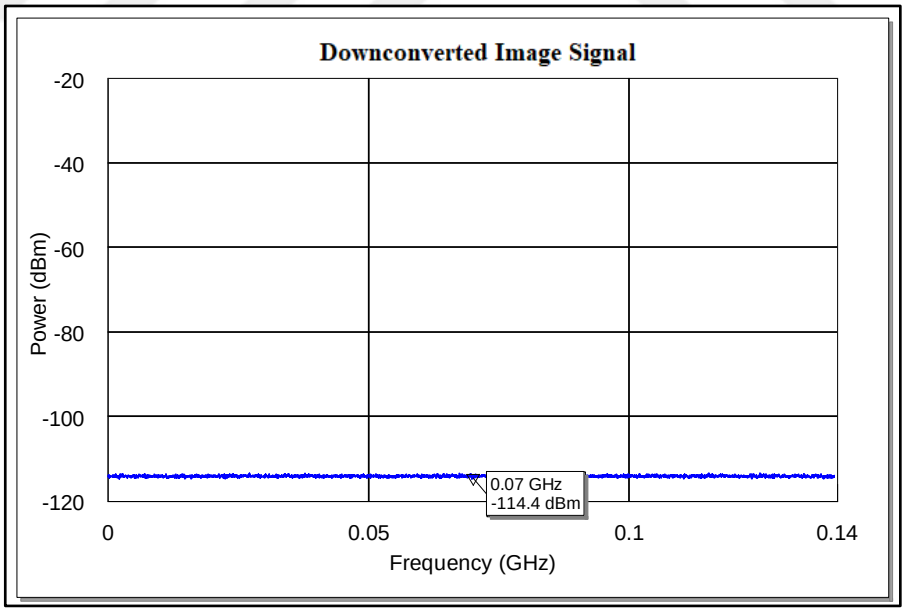


Figure 3.6. Spectral view of down-converted 1.34 GHz signal as an image

However, as stated before topology is not going to be realized ideally, and it is going have phase and amplitude mismatches. In simulations, to see the effect of this non-ideal behavior, 91-degree phase shift is applied to the LO signal instead of 90 degrees. It turns out that the image signal power appears as -65 dBm, so the image rejection ratio is around 40 dB.

Simulation result related to the power of the down-converted image signal is shown in Figure 3.7. This effect occurs at any difference of 1-degree phase mismatch between I and Q part of IF signal. In other words, the 89-degree phase shift is going to create the same effect as the 91-degree phase shift.

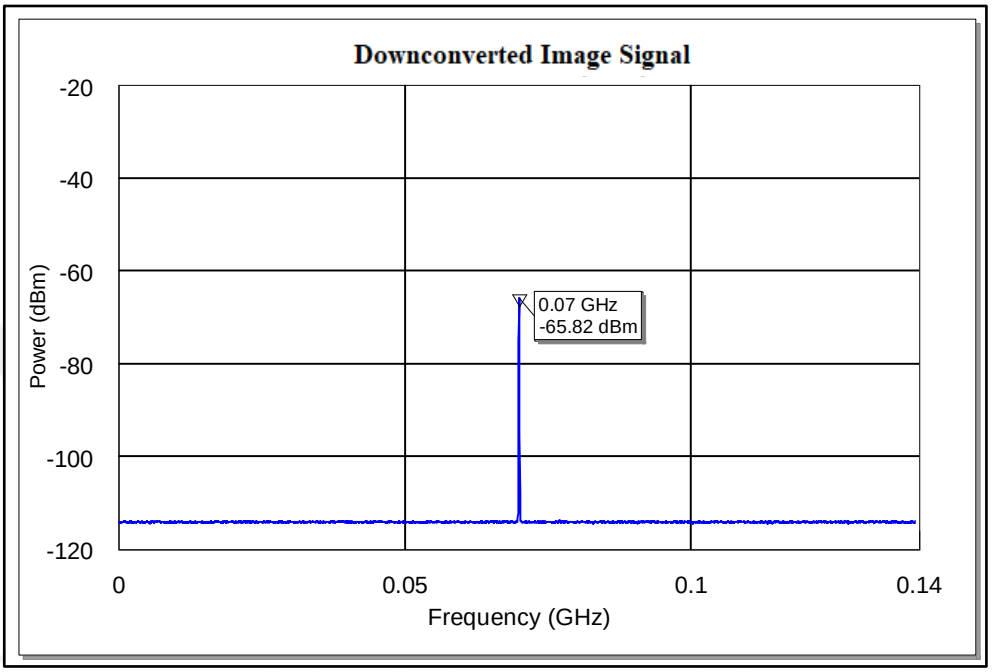


Figure 3.7. Down-converted image signal when 1-degree phase mismatch occurs

The same problem may occur for amplitude mismatch between I and Q no matter what causes that amplitude difference. When amplitude mismatch exists between the I and Q parts, the image rejection ratio will be decreased. If 1 dB amplitude mismatch is applied to I part by using an attenuator, the down-converted image signal power will be about -50 dBm. So the image rejection ratio will be about 25 dB. The simulation result of the down-converted image signal which 1 dB amplitude mismatch occurs is shown in Figure 3.8. Any amplitude mismatch will decrease the image rejection dramatically. Moreover, in practice, both phase and amplitude mismatches more likely exist at the same time which results in a dramatical degradation on total performance. These mismatches need to be minimized to achieve an optimal image rejection.

According to the obtained graphs, simulation results show a good fitting with the theory. Furthermore, AWR system simulations were executed to investigate and compare the performance issues between topologies that is suitable for FHSS systems. With this regard, dual-IF heterodyne topology and image-reject topology are adapted in AWR. Also, proper

components were chosen and simulated for both topologies. 850 MHz is selected for center frequency of first IF-frequency in dual-IF heterodyne receiver topology. As described in chapter 2.1.2, the frequency planning is one of the most critical issues in this topology. The frequency is selected after several simulations and iterations. When iterations are performed, filters in the market are investigated for a realistic approach. The spurious response is also investigated to find proper first IF value. The simulation results are given in Table 3.2. to clarify the chosen values. However, achieving an outstanding image-rejection ratio, by the only usage of the image reject topology, is difficult; so dual-IF heterodyne topology is generally preferred. If the difficulty can be eliminated somehow by the proposed image-rejection approach, the image-rejection topology may be preferred.

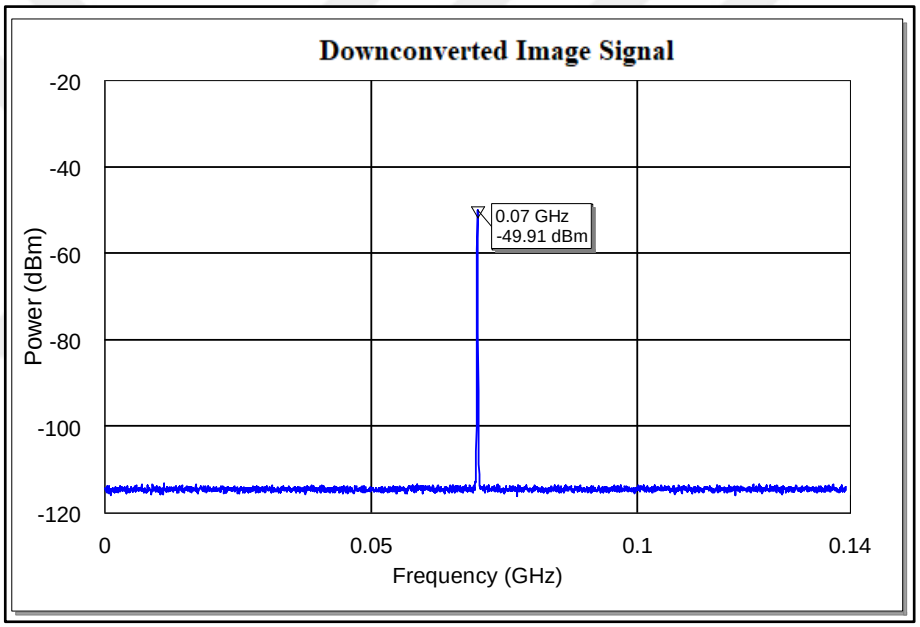


Figure 3.8. Down-converted image signal when 1 dB amplitude mismatch occurs

3.1.2.1. Image Rejection Simulations

The most challenging part of designing image reject downconverters are I and Q mismatches of IF signals and an effort to minimize these mismatches to obtain the appropriate image rejection ratio. Even if other parameters such as noise figure, sensitivity are well-tuned, the image rejection ratio could be decreased due to the amplitude and phase errors. Especially in broadband FHSS systems, the carrier and the image are continuously being changed. For these reasons, component selection is the most crucial point in the image-reject receiver topology than anything else.

Table 3.2. Simulation results of appropriate topologies

Parameter	**Dual-IF Heterodyne Receiver**	**Image-Reject Receiver**
Frequency Range (MHz)	950-1450	950-1450
Output Frequency (MHz)	70 ±15	70 ±20
Gain (dB)	40	40
In-Band Ripple (dB)	<1.5	<0.5
Variable-Gain Range (dB)	63	63
1 dB Compression (dBm)	1.7	3.4
Noise Figure (dB)	<10	<12
Image Rejection (dB)	>50	>40

In the discrete implementation of Hartley image reject receiver, the first component is power splitter that could cause amplitude and phase mismatches between I and Q sections. The first issue is frequency-band to consider for a splitter. The frequency band of the splitter has to be between 950-1450 MHz. The second important parameter is phase and amplitude unbalance between two output port of the splitter. In the ideal case, there is no amplitude and phase difference between output ports. Both amplitude and phase parameter should be same between ports. However, these parameters could be different with respect to frequency due to design and production tolerances of components. While choosing a proper component, products of several manufacturers are investigated, and "PD0922J5050S2HF" Wilkinson power divider is selected to use as a zero-degree splitter. "PD0922J5050S2HF" is a product of Anaren from Xinger product family. In datasheets, the unbalanced term refers to amplitude or phase difference between ports. Unbalance is specified typically about 0.1 dB for amplitude and 1 degree for phase between output ports for the splitter working in-band. The s-parameter of the splitter is transferred to AWR Microwave Office (MWO) simulation tool. In AWR MWO, s-parameter magnitude delta and s-parameter phase delta measurements are performed to specify amplitude and phase unbalance. Figure 3.9 shows the simulation setting of the phase and amplitude unbalanced simulations in AWR [29].

In the simulation, the maximum amplitude difference between output ports is 0.024 dB at 1.3825 GHz, and minimum amplitude difference is 0.0078 dB at 1.1026 GHz between the 950-1450 MHz band. The simulation result is shown in Figure 3.10. The maximum phase difference between output ports is 0.2139 degree at 1.1026 GHz, and the minimum phase difference is 0.0307 degree at 1.4225 GHz between 950-1450 MHz band. The simulation result is shown in Figure 3.11. According to s-parameter simulations, this splitter will cause small effects due to unbalanced values.

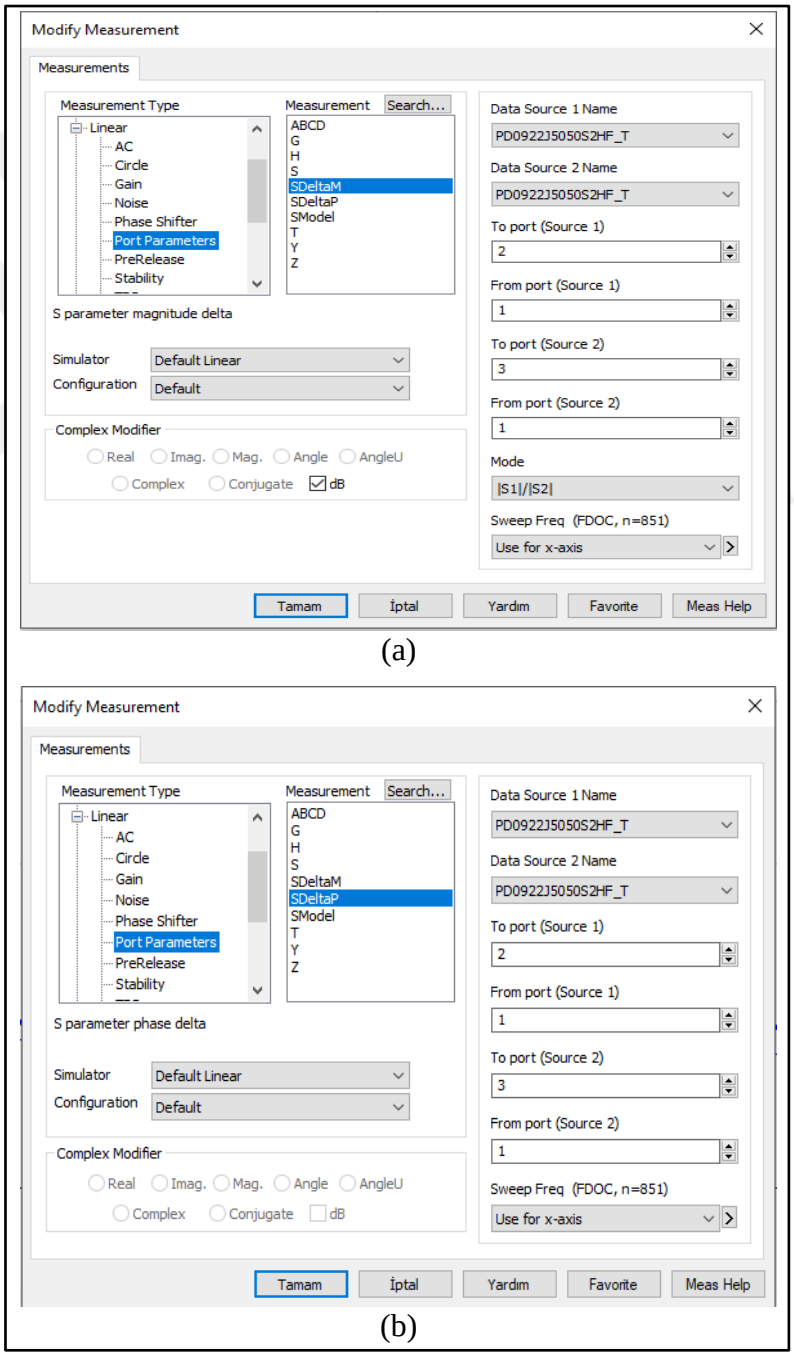


Figure 3.9. Error simulations view in AWR. (a) Amplitude error, (b) Phase error.

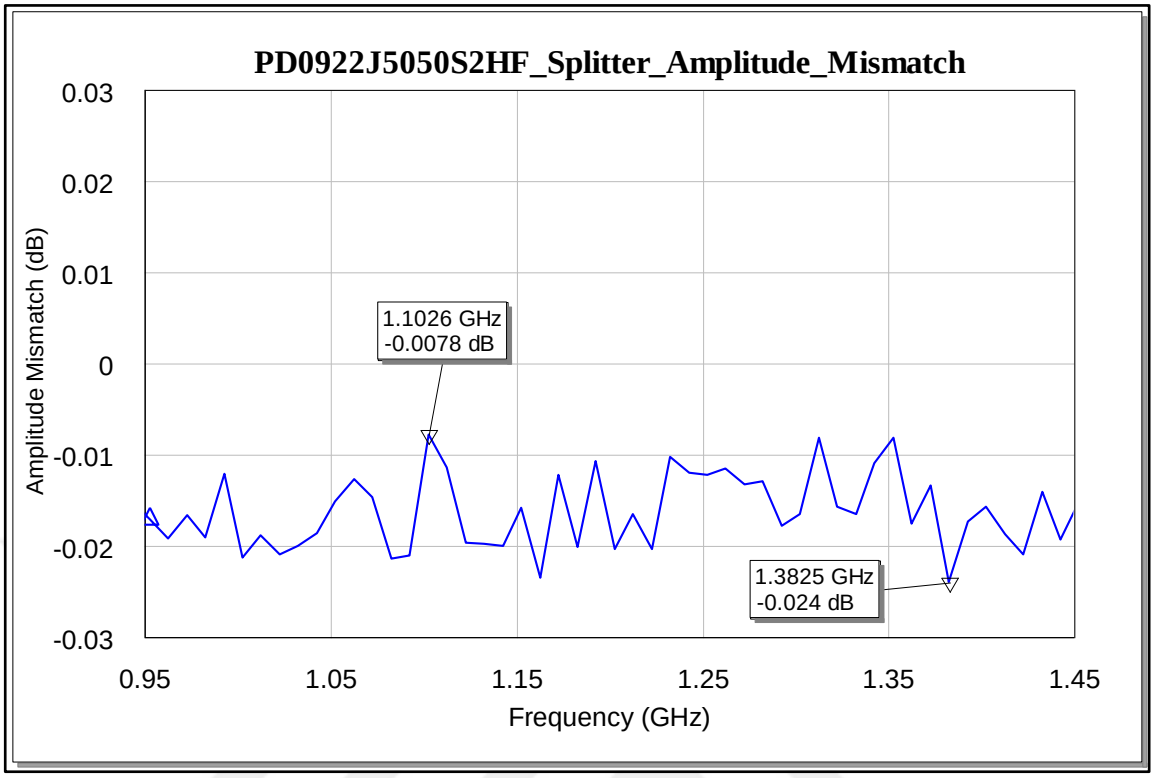


Figure 3.10. Amplitude mismatch simulation of the splitter

In this topology, the other component that causes image-rejection ratio degradation is the 90-degree phase shifter. For this operation, a 2-way 90-degree power splitter could be used. This component splits the LO signal into two outputs but applies 90-degree phase shift with respect to 0-degree port. However, these exact 90-degree phase shift is expected in the ideal case, and it is hard to achieve 90-degree phase shift over a broad-band. While this operation, the difference in magnitude occurs between ports. QCS-152+ is selected for this operation from Mini-Circuits Company. Simulations are performed from 880 MHz to 1380 MHz. Because Input frequency is specified from 950-1450 MHz and IF frequency is 70 MHz. So LO signal frequency is placed from 880 MHz to 1380 MHz. According to simulation, this 90-degree splitter could not achieve an exact 90-degree shift at anywhere from 880 MHz to 1380 MHz. The maximum phase-unbalance occurs at 880 MHz, and the phase difference value is 86.027-degree instead of 90-degree. Moreover, also minimum phase-unbalance occurs at 1380 MHz. Figure 3.12 shows the phase relations between the output ports of QCS-152+ [30].

Additionally, there is amplitude mismatch between ports according to simulations. At 1.0444 GHz, there is no amplitude mismatch, and amplitude difference between ports is 0 dB. However, maximum amplitude error occurs at 880 MHz, and this value is 0.05dB.

Amplitude mismatch simulation result of 90-degree splitter is shown in Figure 3.13. The phase unbalance is relatively high and causes a reduction in image rejection ratio to about 20 dB. Therefore, the amplitude-unbalance could be negligible for this component.

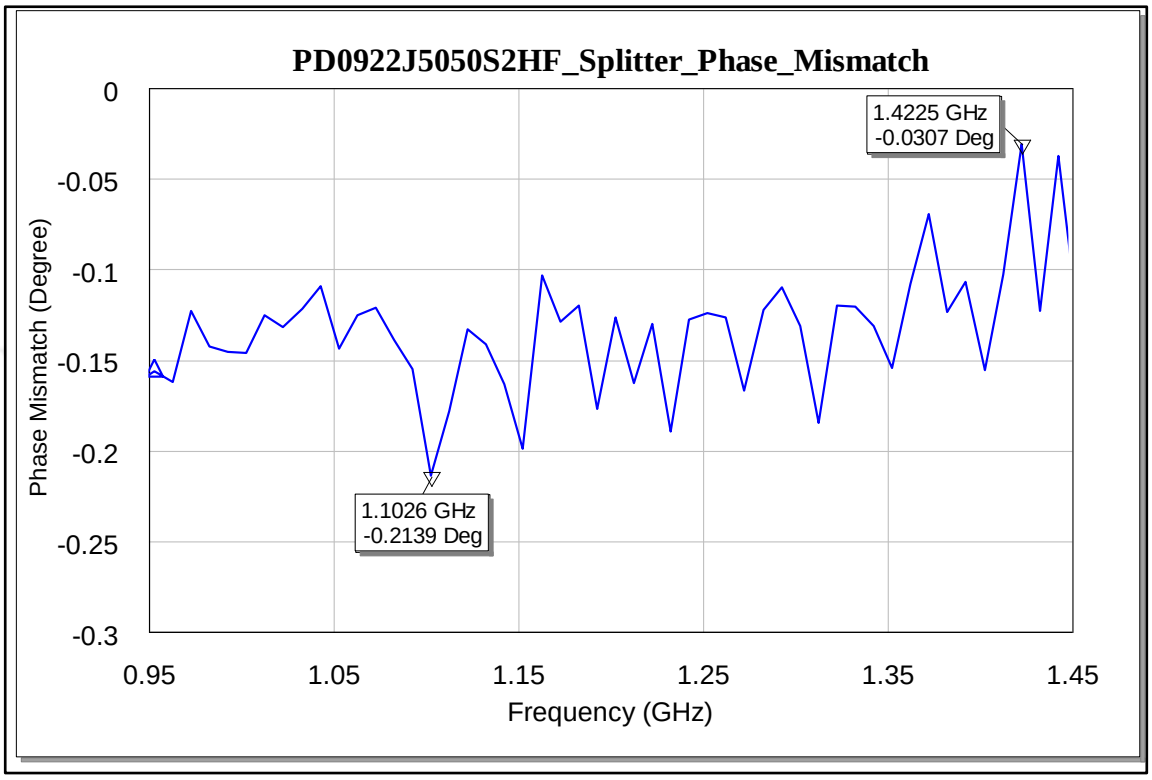


Figure 3.11. Phase mismatch simulation of the splitter

In Hartley image reject receiver topology, the last component which provides image rejection is a 90-degree combiner. Combining I and Q parts with 90-degree phase shift are produced by "JSPQW-100A+" from Mini-Circuits. This product is a two way 90-degree combiner and its working frequency is between 30-100 MHz. Amplitude error is stated as about 0.5 dB, and phase error is stated as about 1.8-degree in the product datasheet. In other words, there is no exact 90-degree phase shift again. For this component, only 70 MHz is taken into account because all carriers and also image signals are down-converted to 70 MHz IF frequency. So phase error is 0.65-degree, and amplitude error is 0.1 dB at 70 MHz according to s-parameter simulation results. Phase relation simulation of 90-degree combiner is shown in Figure 3.14, and amplitude relation simulation of 90-degree combiner is shown in Figure 3.15 [31].

The double balanced mixers are used for mixing operations which are located at both in-phase and quadrature section. These mixers are assumed as identical. As discussed, these

parts critical for image-rejection topology and image-rejection ratio. Because of that reason, choosing components was made carefully.

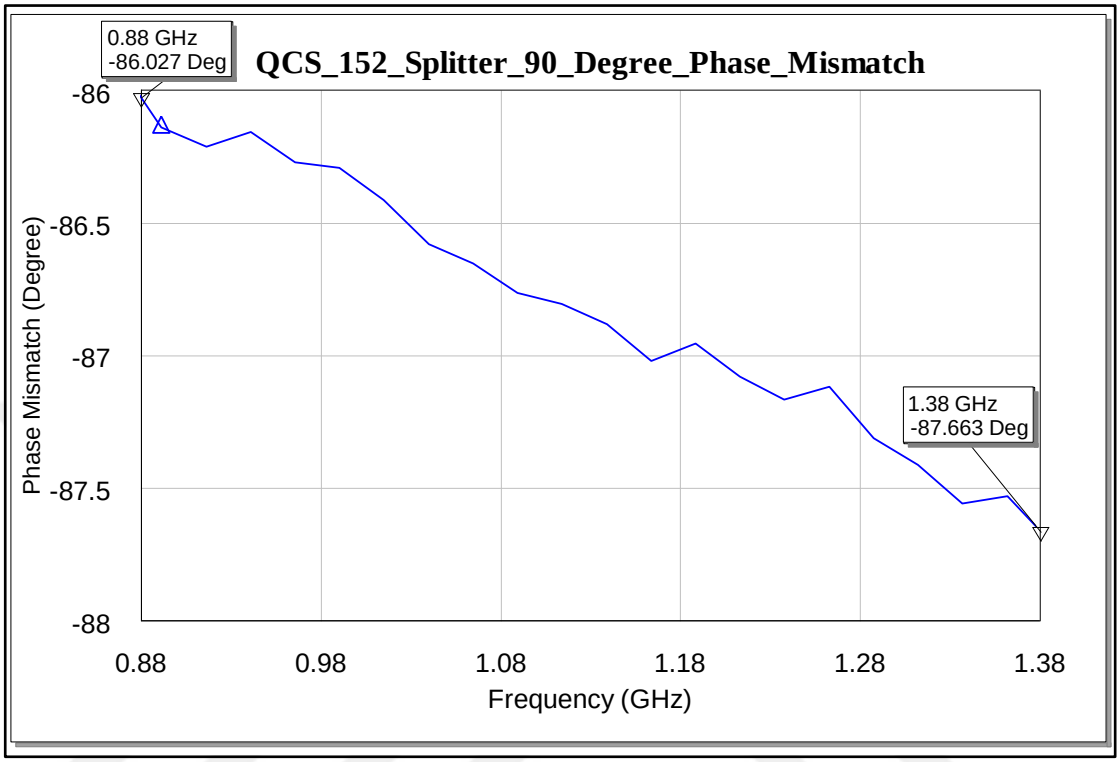


Figure 3.12. Phase mismatch simulation of 90-degree splitter

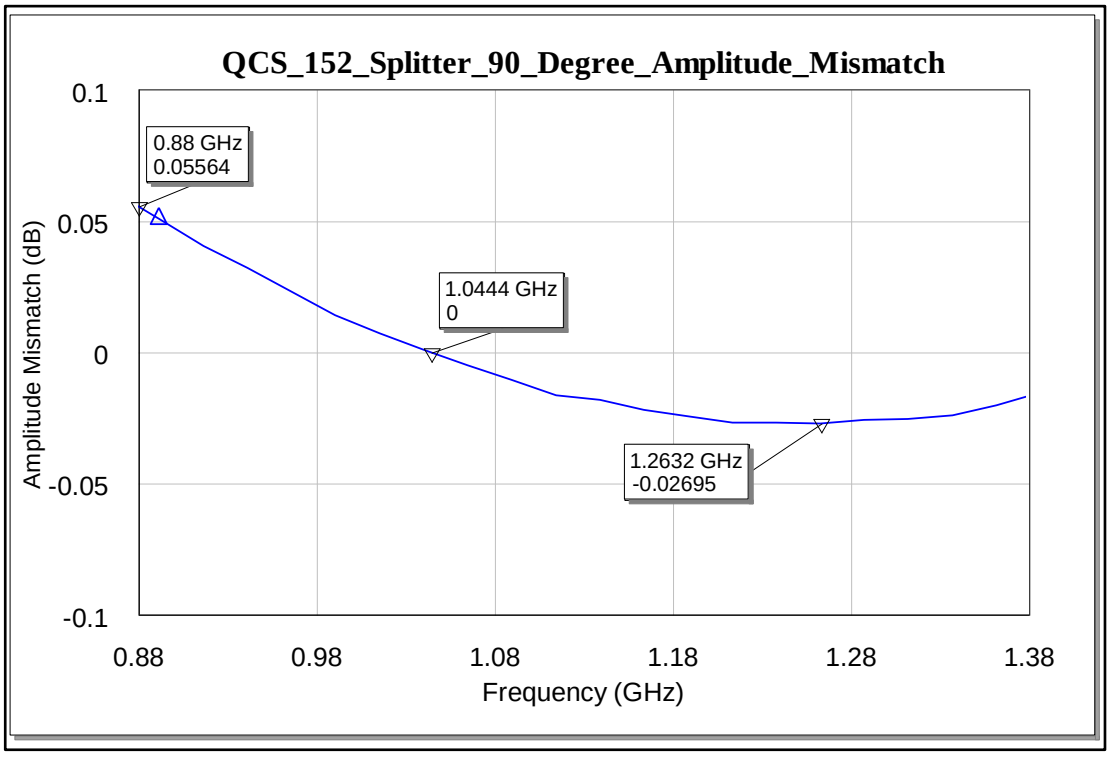


Figure 3.13. Amplitude mismatch simulation of 90-degree splitter

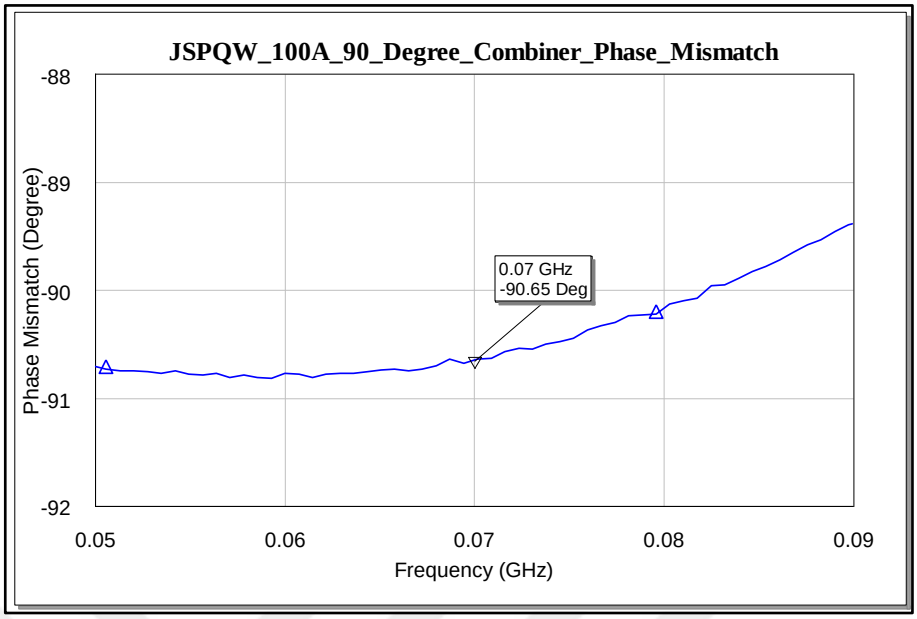


Figure 3.14. Phase mismatch simulation of 90-degree combiner

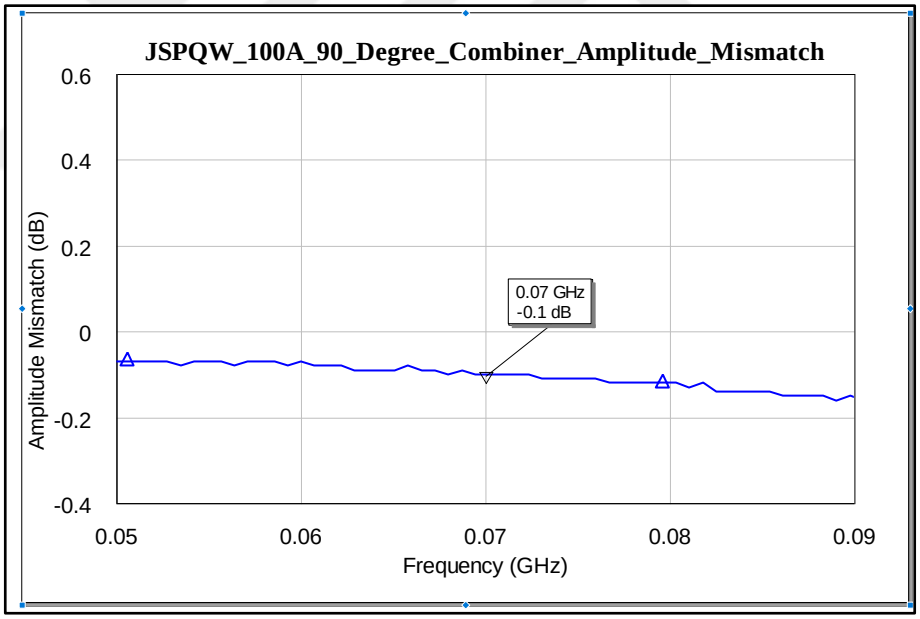


Figure 3.15. Amplitude mismatch simulation of 90-degree combiner

All these components show these behaviors at different frequencies. However, all effects on the signal path could be taken into account. For example, the desired signal is present at 1000 MHz, and LO will be 930 MHz. IF frequency is 70 MHz. The power splitter "PD0922J5050S2HF" has +0.1458 degree phase error and 90-degree splitter "QCS-152+" present - 3.82-degree phase error and at 70 MHz 90-degree combiner has +0.65 degree phase error. So totally 3.02-degree phase error on an entire chain for desired 1000 MHz. In other words, expected image rejection could be calculated using with this approximation.

All amplitude and phase errors from each component are summed, and phase and amplitude values are adopted in Equation (2.10). This equation will give the expected image rejection ratio. All data is calculated in excel and result of the equation for each frequency are transferred to AWR MWO as a data file and plotted. Figure 3.16. shows expected image rejection.

Expected image rejection values with respect to image signal frequency when If any amplitude or phase correction methods are not applied. In this case, best image rejection value occurs at 965 MHz, and its value is 32,786 dB.

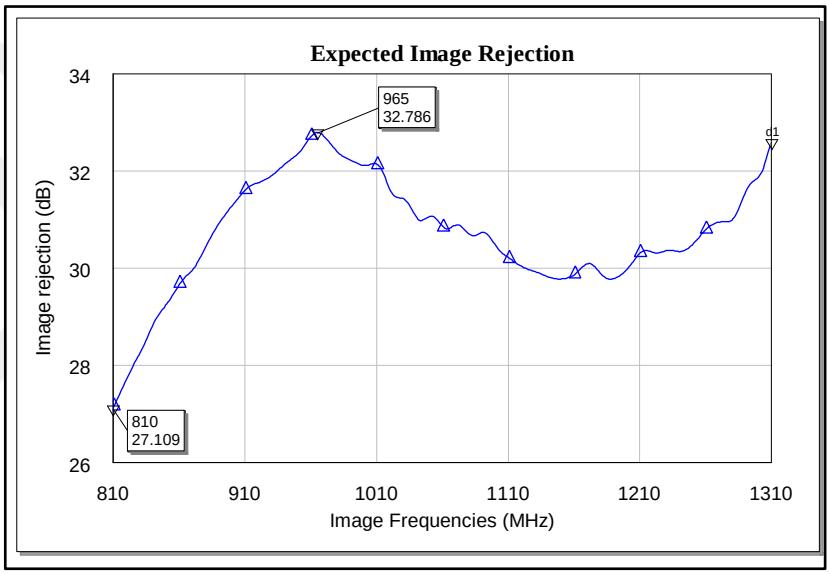


Figure 3.16. Expected image rejection based on s-parameter simulations

On the other hand, worst image rejection occurs at 810 MHz with 27 dB. These results are not enough for most of the communications system, and so image rejection of the design should be improved. Methods of image rejection are described in the next chapter.

3.1.2.2. Adaptive Image Reject Downconverter

As described in the previous section, the image rejection values without any compensation are not sufficient. Therefore improvement methods on the image rejection are based on amplitude and phase. Total phase errors of the architecture are shown in Figure 3.17.

Assume that, above values, the compensation method is applied to eliminate only the phase mismatches which create zero phase mismatch at all image frequencies. So if new image

rejection ratio is calculated according to Equation (2.10), image rejection ration will be like Figure 3.18.

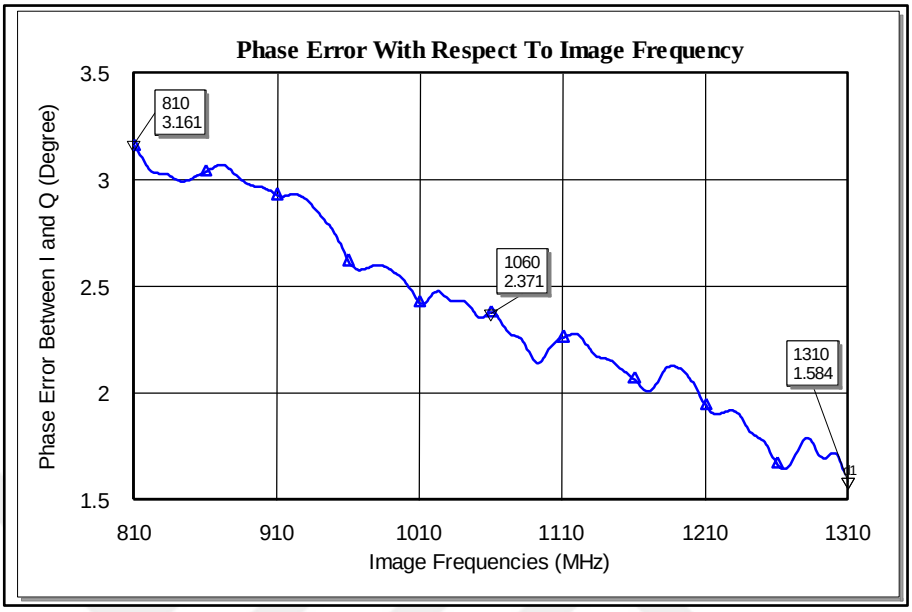


Figure 3.17. Total phase error in architecture

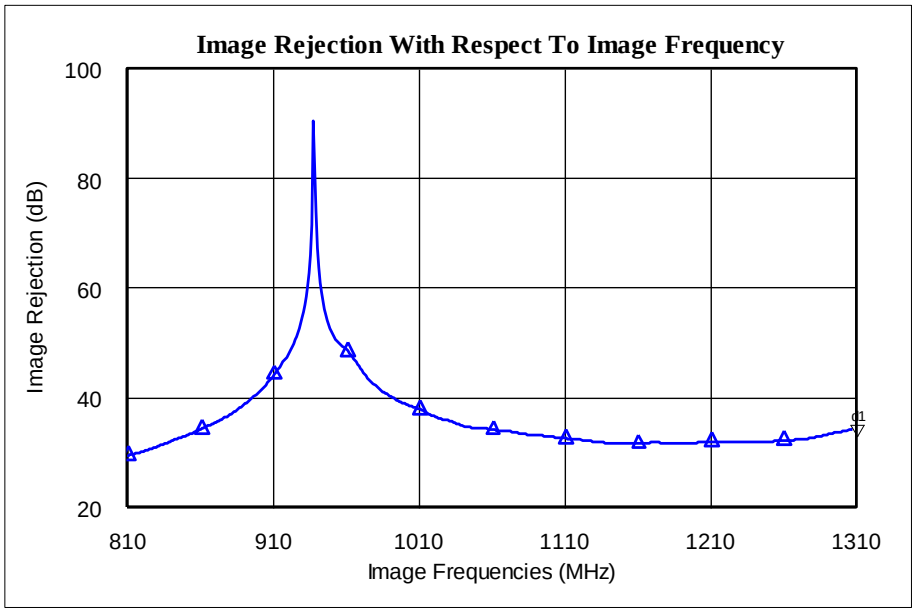


Figure 3.18. Image rejection ratio when all phase errors minimized

Also, architecture's total amplitude errors are shown in Figure 3.19. Furthermore, If the same approach is applied for the amplitude errors, amplitude errors will be zero at all frequencies, but phase errors will be still the same. In this regard, calculated image rejection will be like Figure 3.20.

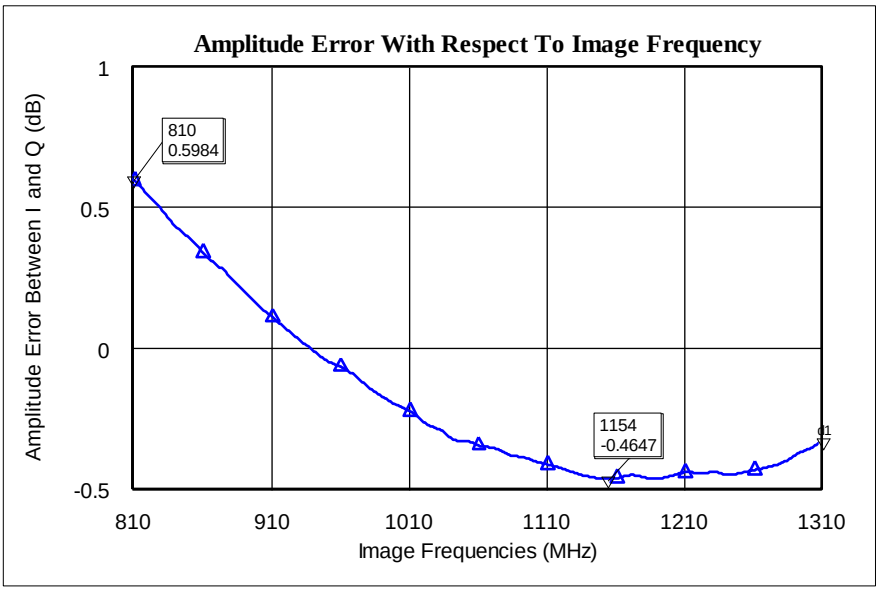


Figure 3.19. Total amplitude error in architecture

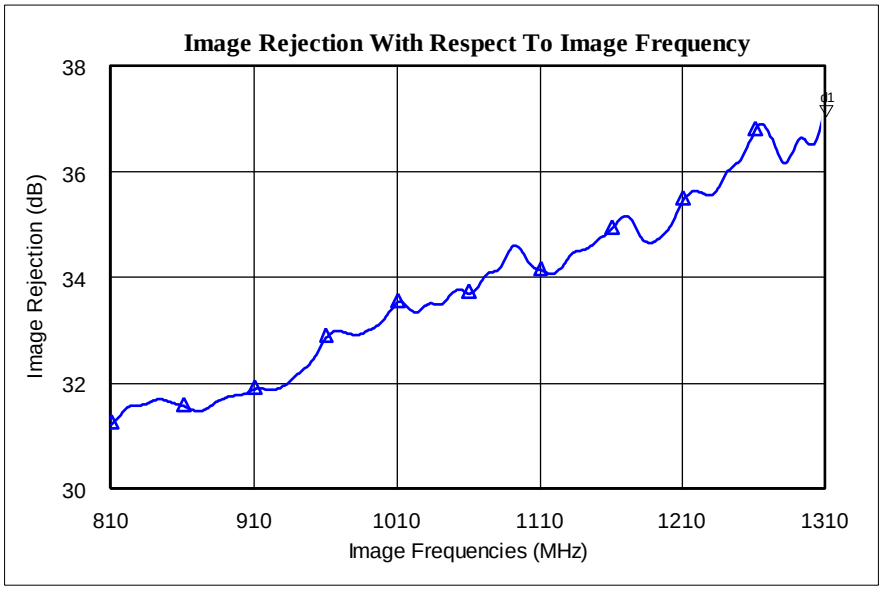


Figure 3.20. Image rejection ratio in case of all amplitude errors minimized

In the light of these results, phase error compensation and amplitude error compensation are caused by different effects on image rejection in the proposed design. Compensating phase errors makes image rejection ratio sufficient in a narrow band in the spectrum. Besides, compensation on amplitude errors enhances image rejection all over the entire band. The best way to achieve perfect image rejection is applying both amplitude and phase compensations, but this study focuses only on the amplitude compensation. Besides, the image-rejection ratio improvement is proven by previous works by eliminating amplitude

and phase mismatches [32,33]. There are some widely-used methods to compensate for phase errors. This study is about a novel-approach about adaptive amplitude mismatch compensation by applying DC voltage to the mixer.

On the other hand, only insertion loss of the mixer will be affected by applying DC voltage to the mixer , not phase response. Therefore, phase errors are still the same and will cause degradation in the image rejection ratio. Despite the thesis study aims to eliminate amplitude errors for improving the image rejection ratio, the phase error optimization is also considered. According to Figure 3.17, the phase error is not zero anywhere in the band and changes almost linearly from 810 MHz to 1310 MHz. If the phase shift is applied until phase error is zero at the center of the band, the phase mismatch will be zero at the center of the band and will be distributed almost symmetrically below and above the center of the band. Moreover, this operation will reduce maximum phase error. According to the s-parameters, in-phase part is ahead from the quadrature part. So phase shift should be applied to the quadrature part. Total phase errors of components are about 2,371 degrees at the center of the image frequencies at 1060 MHz. Based on this information, if 2,371-degree phase shift is applied to the quadrature part, new phase mismatch graph will be like Figure 3.21.

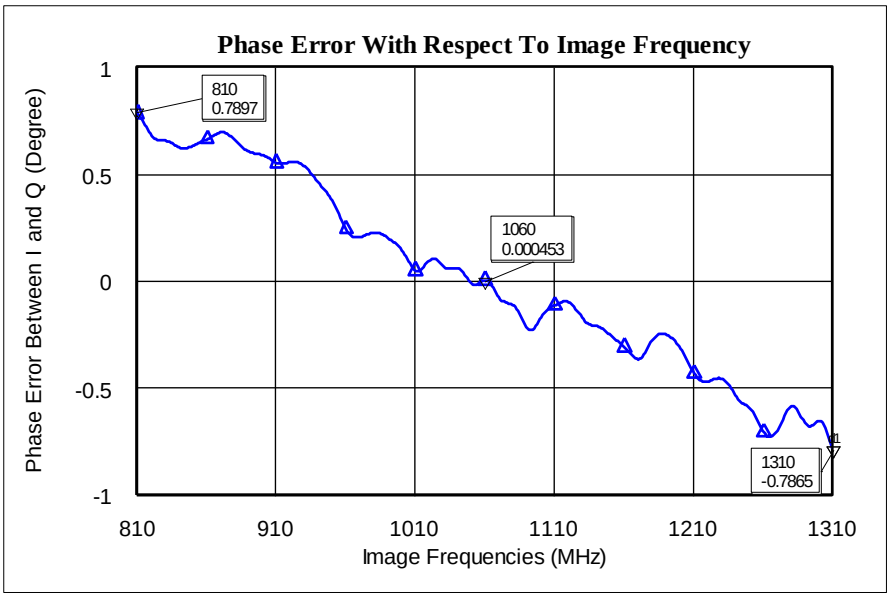


Figure 3.21. Total phase error after compensation in architecture

Phase error at 1060 MHz is nearly zero as shown in Figure 3.21 after 2,731-degree phase shift is applied. The maximum phase error is 3.161-degree at 810 MHz image frequency if any phase correction is not applied. After the proposed method is applied for phase errors,

the maximum phase error will be 0.78-degree and distributed symmetrically. This operation will increase image rejection ratio owing to the reduction of phase error. New image rejection data could be found in Figure 3.22 when the amplitude errors are still the same, and the necessary 2,731-degree phase shift is applied to the quadrature part.

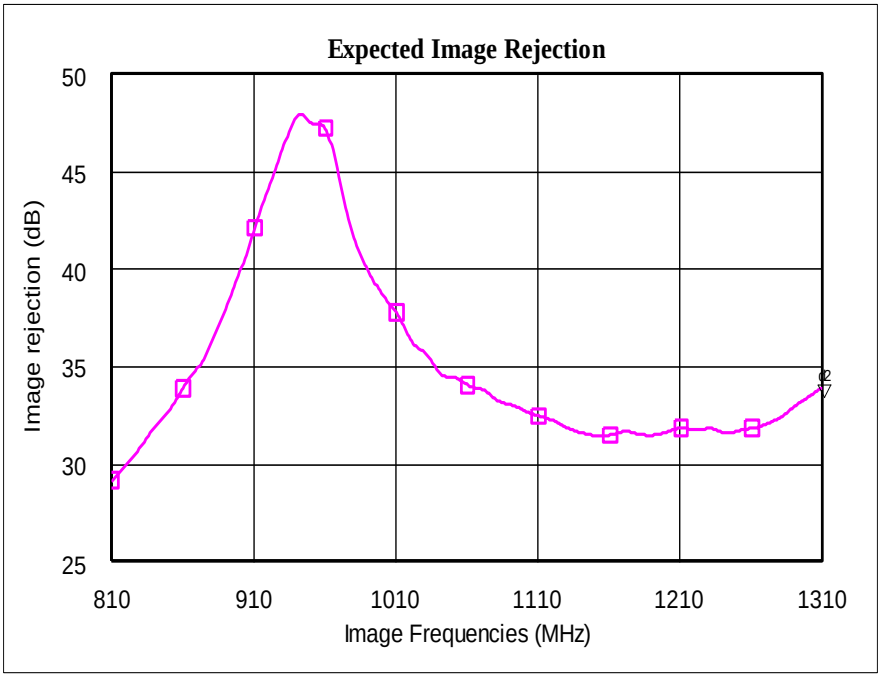


Figure 3.22. Expected image rejection ratio after phase compensation is applied

On the other hand, this method is a non-adaptive approach because it is not tunable. So the phase shift will not change depending on the input image frequency.

As discussed before, all mismatches could be examined cumulatively. Therefore, it does not matter where the phase shift is to be applied theoretically. Detailed information about phase shift is given at 4.2.

Nevertheless, this compensation method will not cause any change in amplitude errors. Also, the amplitude mismatch is tightly bound with the image frequency like the phase mismatch. The phase compensation that is applied is a non-adaptive approach. However, the amplitude compensation will be depended on the image frequency and minimized at each image frequency.

A double balanced mixer that is used in the image-reject converter design contains diode rings. If DC voltage is applied to the diodes of the mixer, the diodes operation condition will

change, and also insertion will be affected since the diodes' bias conditions will be changed. Notably, two of the diodes will be opened at higher voltages, and the others will be closed at higher voltages. So mixer's normal operation degenerates, and in that case, insertion loss of this mixer will also degenerate when DC voltage is applied. The output power of the mixer could be expressed in the following equations;

$$P_{out} = \frac{V_0}{R_L} \tag{3.2}$$

Or

$$P_{out} = \frac{{V_0}^2 R_L}{[\frac{\pi^2}{4}(R_g + R_{SW}) + R_L + R_{SW}]^2} \tag{3.3}$$

Where;

$$P_{out} = Output\ power\ of\ the\ mixer$$

$$P_{out} = Output\ power\ of\ the\ mixer$$

$$V_o = Output\ voltage$$

$$R_L = Load\ impedance$$

$$R_g = internal\ loss$$

$$R_{SW} = Device\ loss\ (\text{Diode Junction})$$

Conversion or insertion loss of the mixer could be expressed as;

$$L_{conv} = \frac{[\frac{\pi^2}{4}(R_g + R_{SW}) + R_L + R_{SW}]^2}{\pi^2 R_L R_g} \tag{3.4}$$

According to the Equation (3.3) and Equation (3.4), increasing device loss will cause increasing in mixer insertion loss. Thereby, increasing insertion loss of mixer is obtained by applying DC voltage to the mixer. Therefore, tuning of insertion loss of the mixer and error compensation of the amplitude errors are allowed. In the image reject receiver topology, DC voltage is applied to one of the I and Q part mixers IF port whose insertion loss value is lower than the other. In the case of applying DC voltage to IF port,

this section insertion loss will also be increased and the amplitude mismatch will be decreased between I and Q ports. However, while applying DC voltage, more attention should be given not to damage the diode permanently in the mixer due to the over-voltage. [9, 34].

Applying a constant voltage value could not offer a solution over wideband due to a variable characteristic of the amplitude mismatch. The DC voltage values need to be changed according to amplitude mismatch depend on the image frequency to overcome this problem. Applying DC voltage provide a solution for the amplitude mismatch, on the other hand, there will be no change in the phase.

This method presents a significant solution to the amplitude mismatch. At the conceptual design stage, the amplitude changes according to the value to be applied should be simulated, and DC voltage values should be predicted by using the spice model of mixer.

Unfortunately, the spice model of the mixer that is used in this study is not supplied by the manufacturer. For this reason, predicted DC voltage values could not be obtained from simulations. Therefore the values that are obtained from measurements will be discussed in the next chapters. In real time applications, the measured DC voltage values that provide best image rejection will be stored on a controller in tabular form and will be applied with regard to the image frequency values.

According to Figure 3.21, insertion loss of In-phase section is surplus than the quadrature section from 810 MHz to 939 MHz. DC voltage needs to be applied to the Quadrature section's mixer to increase insertion loss thereby reduce amplitude mismatch. From 939 MHz to 1330 MHz, insertion loss of the quadrature section is surplus than the in-phase section, so DC voltage is needed to be applied to the In-phase section's mixer to increase insertion loss of the In-phase section. Detailed information about applying the DC voltage to IF port the mixer is discussed in chapter 4.1.

Especially in commercial applications, DC voltage values that are stored in tabular form with respect to the image frequency is applied by a DAC. A controller communicates over SPI buses with DACs, and necessary DC voltages are applied to the mixer's port by DACs. The adaptive image rejection is ensured over broadband by applying that method.

3.1.3. Spurious-Free Synthesizer Design Approach

The phase noise or jitter response of a clock or an LO signal defines the quality of the signal. The Phase noise is the frequency domain representation of the clock signal noise. The jitter is the time domain representation of the clock signal instability. Jitter shows random variations of the clock signal in the time domain that should not be present in an ideal clock signal. The phase noise is indicated in terms of dBc/Hz, and the jitter is indicated in terms of ps. The low phase noise property of clock signals are required for RF systems especially for ADC, DAC, and downconverter. In ADCs, poor phase noise response causes a reduction in SNR and Effective Number of Bit (ENOB) of ADC. The desired signal and LO signals are impulses in the ideal case. Therefore the down-converted signal is an impulse with no change in shape. In real, the LO signal has phase noise, and a high power interferer or adjacent channel could exist. After down-conversion, the both desired and interferer are down-converted.

Moreover, the down-converted desired signal is swallowed from the tail of the down-converted interfere signal. This situation is called reciprocal mixing. Figure 3.23 shows the reciprocal mixing situation. Also, the information that is the carried in the phase of the carrier could be distorted by phase noise of the LO source. Therefore, sharper phase noise response should be represented by the LO signal in RF systems. That is the reason; the phase noise response limitations are well specified from standards.

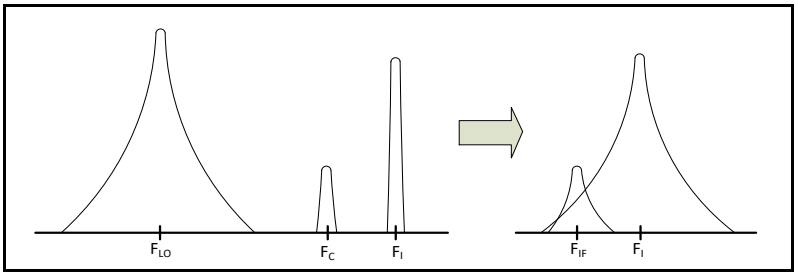


Figure 3.23. Reciprocal mixing

PLL is a feedback topology which is used for composing constant phase desired clock or RF frequency by using VCO and phase comparator. The basic PLL topology includes a comparator, a loop filter, VCO and frequency dividers. The comparator is fed by the reference signal and a clock signal. The clock signal is obtained by division of the VCO frequency by the feedback divider which is existed at comparator. The reference signal and

the clock signal are needed to be equal in terms of frequency. The signals are compared in the comparator, and a phase error is obtained. According to this error value, the charge pump current is composed and feeds VCO tuning port. When these two clocks are equal to each other in terms of phase and frequency, the lock condition is ensured. In a word, the phase error zero will be zero. Therefore, the VCO is set to desired frequency with constant phase. Basic PLL structure is given in Figure 3.24.

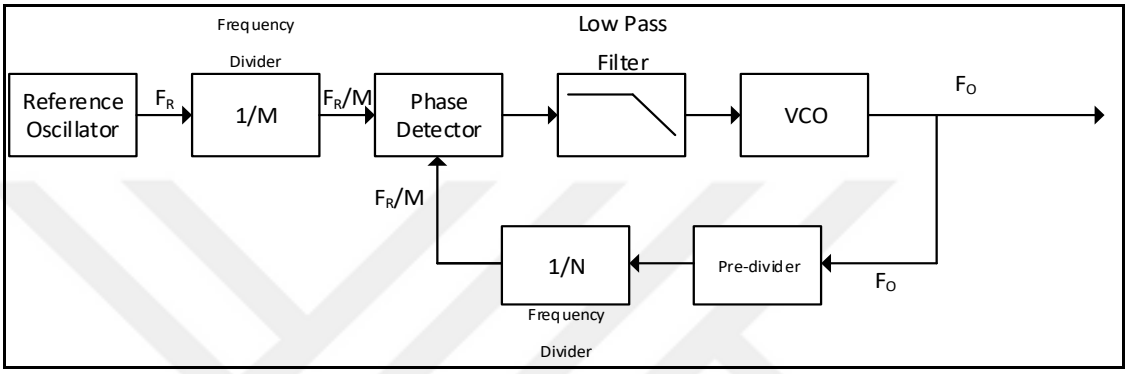


Figure 3.24. Basic PLL structure

The Phase Frequency Detector (PFD) is the section which phase and frequency comparison come true. Comparison frequency is the PFD frequency. The VCO tuning step size is defined by the PFD frequency in the integer-N PLL. Reference divider and VCO pre-scalar could also exist in the PLL structure. By using the dividers, smaller PFD frequencies could be possible. For instance, 10 MHz is applied to the PLL reference input from system and PFD frequency will be 10 MHz in the absence of reference divider. On the other hand, in the case of using reference divider, smaller PFD frequency will be obtained. If its value is arranged as 10, the PFD frequency will be 1 MHz, and VCO tuning resolution will be 1 MHz. Thus, VCO tuning resolution is increased as well as output frequency resolution. Illustration of an integer-N PLL parameter detail is given in Figure 3.25. The output frequency of an integer PLL could be expressed in the following equations.

$$f_{Output} = \frac{F_{VCO}}{k} \tag{3.5}$$

Where;

$$f_{Output} = Output\ frequency$$

$$f_{VCO} = VCO\ frequency$$

$$k = \ Output\ divider$$

Output VCO frequency could be expressed as;

$$f_{VCO} = \frac{f_{Ref}}{R} \cdot N \cdot N_{pre} \tag{3.6}$$

Where;

$$F_{Ref} = \ Reference\ frequency$$

$$R = \ Reference\ divider$$

$$N = \ Feedback\ divider$$

$$N_{pre} = Pre - divider$$

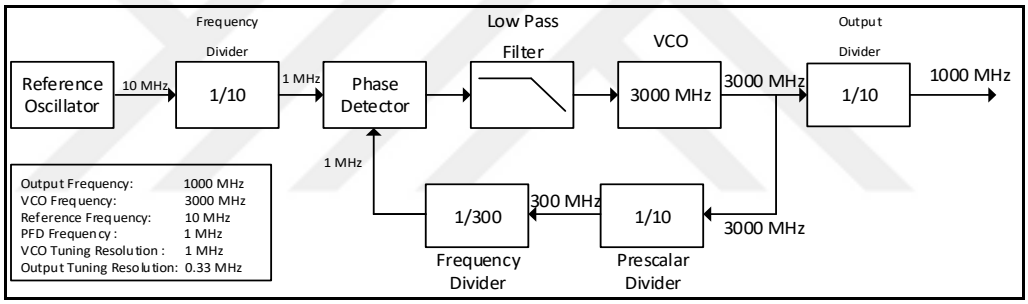


Figure 3.25. Application of an integer-N PLL

The smaller VCO tuning step size is ensured by the smaller PFD frequencies. On the other hand, this method causes increment in-band phase noise. The PFD noise levels of the manufactured PLLs in the market are adequate for analog systems even if the small step size is ensured. However, digital modulation systems are sensitive for phase noise response and also need small step sizes. Besides, the PFD frequency has limited by the manufacturer due to its comparator circuit. That is to say; the integer-N PLLs are not satisfactory for some digital modulation systems. In the circumstances, Fractional-N PLL's must be preferred.

The smaller tuning step sizes are obtained by the Fractional-N PLLs in terms of Hz. VCO tuning step size can be tiny fractions of PFD frequency. In this manner, the PFD frequency can be higher, and the feedback divider can be lower. Thereby, the in-band phase noise will be reduced. The mathematical expression of the output VCO frequency for a fractional-PLL system is given in the following equations.

$$f_{VCO} = f_{int} + f_{frac} \tag{3.7}$$

$$f_{VCO} = \frac{f_{Ref}}{R} \cdot (N_{int} + N_{frac}) \tag{3.8}$$

$$f_{PFD} = \frac{f_{Ref}}{R} \tag{3.9}$$

$$N = (N_{int} + N_{frac}) \tag{3.10}$$

Where;

$$F_{int} = Integer\ part\ of\ \ the\ VCO\ frequency$$

$$F_{Frac} = Fractional\ part\ of\ \ the\ VCO\ frequency$$

$$N_{int} = Integer\ division\ ratio$$

$$N_{Frac} = Fractional\ division\ ratio$$

$$N = Division\ ratio$$

$$f_{PFD} = PFD\ frequency$$

Fractional division ratio could be between 0 and 0.999999 according to fractional modulator specifications. The operation of the fractional-N PLLs is similar with the integer-N PLLs'. The only difference is that the fractional-N PLL includes a modulator. The modulator changes feedback divider ratio between N and N+1 to attain fractional part of the frequency. When modulator's full cycle is completed, the fractional part is obtained on an average of the feedback divider ratio. Feedback divider ratio calculation could be expressed as the following equation.

$$N = \frac{(C - C_{frac}) \cdot N_{int} + C_{frac} \cdot (N_{int} + 1)}{C} \tag{3.11}$$

$$C_{frac} = F_{PFD} \cdot N_{Frac} \tag{3.12}$$

Where;

$$C = Total\ cycle\ number\ of\ modulator$$

$$C_{frac} = Number\ of\ fractional\ cycle$$

For instance, suppose that the PFD frequency is 50 MHz, the VCO frequency 3 GHz and feedback divider ratio is 60. In integer-N PLL topology, PFD frequency should be 1 MHz which is 50 times smaller than the PFD frequency in fractional PLL to obtain VCO tuning size is 50 MHz. The modulator is needed to set the feedback divider value to 60 for 49 cycles in 50 cycles. For the last cycle, the accumulator is needed to set feedback divider value to 61. The feedback divider ratio is calculated according to Equation (3.11).

$$C = 50$$

$$f = 50\ MHz$$

Equation (3.11) is arranged as in Equation (3.13).

$$3001\ MHz = 50.(N_{int} + N_{frac}) \tag{3.13}$$

$$N_{int} = 60$$

$$N_{int} = 0.02$$

According to the Equation (3.11) and Equation (3.12), the number of the fractional cycles could be found as;

$$C_{frac} = 50 \cdot 0.02 = 1 \tag{3.14}$$

$$C - C_{frac} = 49 \tag{3.15}$$

Therefore;

$$N = \frac{49 * 60 + 1 * 61}{50} = 60{,}02 \tag{3.16}$$

So output frequency is;

$$60{,}02 * 50\ MHz = 3001\ MHz \tag{3.17}$$

The desired 3.001 GHz value is obtained by this operation in fractional PLL. Besides, PFD remains as 50 MHz, and 1 MHz is tuning step size is attained. On the other hand, the PFD should be 1 MHz to obtain 1 MHz tuning step frequency for the integer-N PLL. This value is 50 times smaller than fractional PLL's PFD frequency. The theoretical noise reduction by using fractional PLL is expressed in Equation (3.18).

$$Phase\ Noise\ Reduction = 20\log(\frac{PFD_{Fractional}}{PFD_{Integer}}) \quad (3.18)$$

Thereby, the phase noise reduction by using fractional PLL is calculated and about 34 dB compared to integer-N PLL. The calculation is given in Equation (3.19).

$$PFD_{Fractional} = 50\ MHz$$

$$PFD_{Integer} = 1\ MHz$$

$$Phase\ Noise\ Reduction = 20\log\left(\frac{50\ MHz}{1\ MHz}\right) = 33{,}97\ dB \quad (3.19)$$

Due to this reason, the fractional PLLs are used to obtain smaller step sizes and reduce phase noise response at the output frequency.

On the other hand, speed changes in feedback divider value cause a spurious response at the VCO output. These spurs are called fractional spurs or integer-n boundary spurs. The fractional spurs occur at an offset from the carrier. This offset value is equal to the multiplication of the PFD frequency and difference between feedback divider value's decimal part and its closest integer value. Fractional spur location could be specified by using the following Equation (3.20).

$$f_{VCO} - f_{spur} = \begin{cases} (N - \lfloor N \rfloor) \cdot f_{PFD}, & N - \lfloor N \rfloor < 0{,}5 \\ (N - \lceil N \rceil) \cdot f_{PFD}, & N - \lfloor N \rfloor \geq 0{,}5 \end{cases} \quad (3.20)$$

where;

$$f_{spur} = Frequency\ of\ spurious\ product$$

The same example is discussed; the feedback divider value is 60.02. The difference between feedback divider value's decimal part and its closest integer value is 0.02. Besides, the PFD value is 50 MHz. Thus, the fractional spur occurs at 1 MHz away from 3001 MHz on both sides. Calculations of the example are given in the following equations;

$$N = 60{,}02$$

$$N - \lfloor N \rfloor = 60{,}02 - \lfloor 60{,}02 \rfloor = 0{,}02 \quad (3.21)$$

$$N - \lfloor N \rfloor = 0{,}02 < 0{,}5 \tag{3.22}$$

Therefore;

$$f_{VCO} - f_{spur} = (N - \lfloor N \rfloor) \cdot F_{PFD} = 0{,}02 \cdot 50\ MHz = 1\ MHz \tag{3.23}$$

Indeed, the spurious products can be filtered away by the loop filter. For smaller values, spurs occur in loop filter passband region. In the circumstances, the spurs cannot be filtered. On the other hand, the spurious products could be filtered by reducing loop filter band-pass region. However, this method causes poor lock times.

In epitome, the fractional-N PLLs are widely used in designs because of the frequency tuning and other requirements. On the other hand, this topology also has disadvantages such as spurs. In this regard, the proposed design propounds a solution for the fractional spurious response and reference spurious response. Therewithal, the proposed architecture is providing an opportunity for FHSS systems in terms of locking times [10-12].

4. IMAGE REJECT DOWNCONVERTER DESIGN

Logical design of downconverter needs to be done to create a product whose specifications are investigated in previous sections. So the logical design of downconverter details takes part in the schematic design chapter. Then the design details of down-converter which is necessary for production are going to be studied in layout design chapter.

4.1. SCHEMATIC DESIGN

The proposed hardware is conducted on the computer-aided design tool “Altium Designer.” Before stating schematic design, libraries of the components are created to be used. Not only schematic or layout libraries but also 3D libraries are created to better mechanical understanding issues.

Also, the schematic design is conducted in order, and the order provides convenience in terms of tracing in the design. Therefore, the design is divided into several parts. The detailed schematic design is located at Annex-A.

The components that are decided to be used in RF design are usually internally matched. ADL5610 is also internally matched which is used for amplifying signals. On the other hand, ADL5610 is an active device, so necessary voltage needs to be applied to work correctly. The amplifier has no extra bias pin to apply voltage. The “RF OUT” pin is a shared pin to use for RF OUT and bias. Because of this reason, 5V DC is applied to RFOUT pin. Therefore, both DC voltage and RF signal will exist at RFOUT pin. A bias tee needs to be applied to this port to prevent interferer from RF to DC and leakage from DC to other components. The suggested RF choke inductor in the datasheet is 43 nH is applied to this port for biasing.

The amplitude compensation method is discussed in the previous chapter to achieve both adaptive and optimum image rejection. The proper DC voltage needs to applied to IF ports of the mixer. The bias tee circuit is applied to IF ports to apply this method. The appropriate inductor and capacitor selection for bias tee is conducted by AWR simulations. The simulation result is shown in Figure 4.1. The optimum inductor value is 1.1 uH and DC blocking capacitor value is 3.3nF concerning 70 MHz IF output.

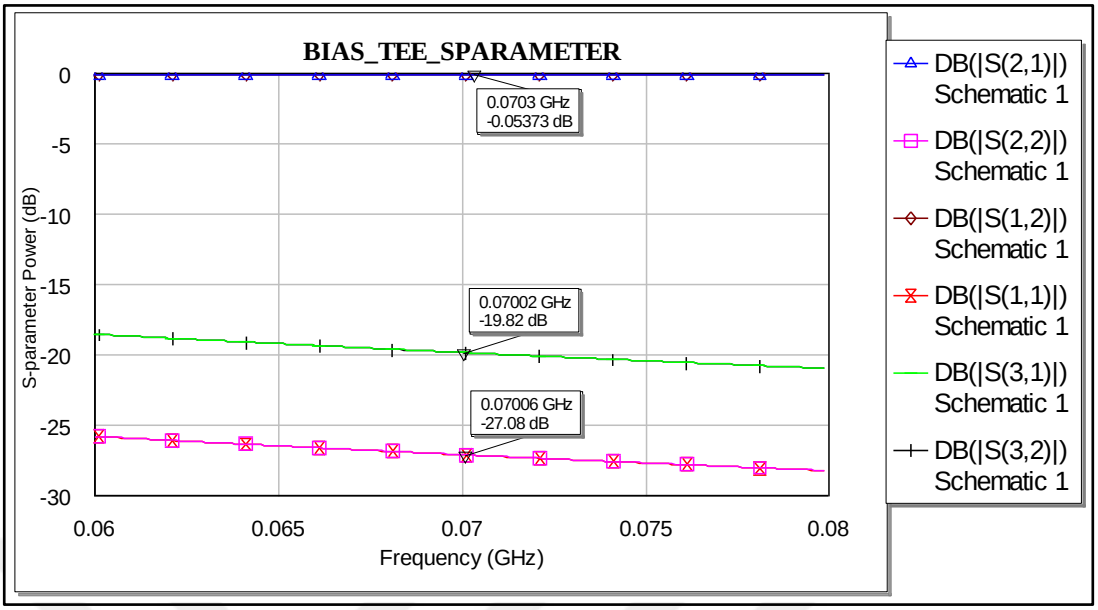


Figure 4.1. Bias tee s-parameter simulation

The DC bias values for compensation differ from carrier frequency to carrier frequency. Therefore, DACs are placed to apply different DC bias values and controlled via software. Resolution of the DACs is 12-bit, and their processing speed is 500MSps. They are controlled via SPI bus. The voltage values can be generated with 1.2mV step size. Therefore, the high precision is obtained. Also, DACs have eight us settling time, so this speed is adequate for frequency hopping applications. This approach is applied to both I and Q sections in the topology.

Some of the components have to be programmed to work correctly. The programming interfaces of the components are listed in Table 4.1.

Table 4.1. Communication interface details of components

Component Function	**Interface**	**Quantity**
DAC	SPI(3 Wire)	2
RF Attenuator	Parallel (6 wire)	1
IF Attenuator	SPI(3 wire)	1

Evaluation board of Texas Instruments is used for programming these components. Pinout diagram of TIVA evaluation board is shown in Figure 4.2.

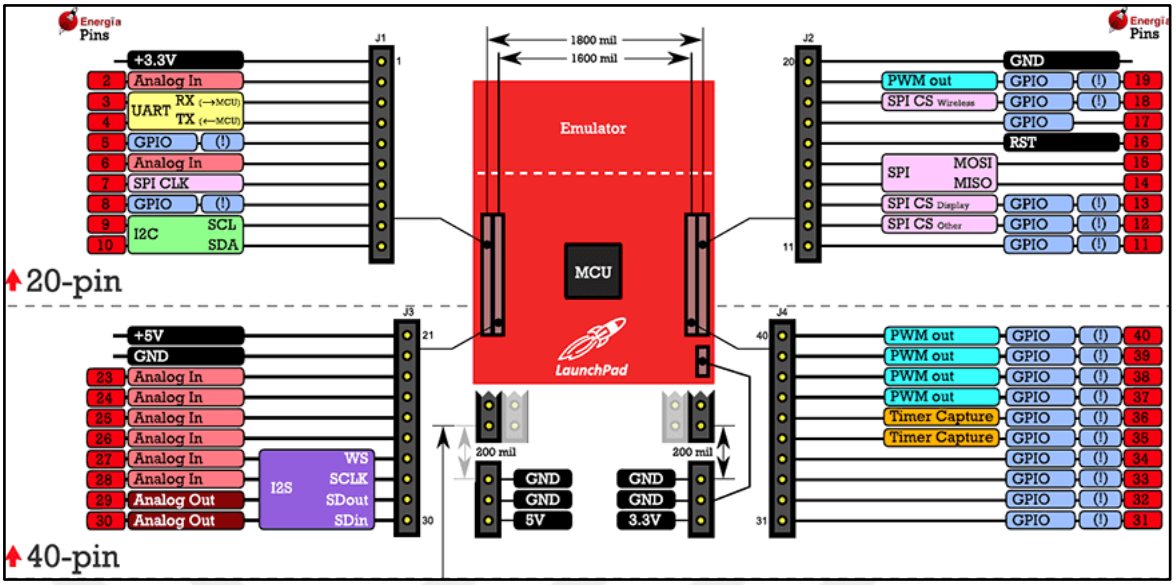


Figure 4.2. Pinout of TM4C123G Launchpad [35]

TIVA owns dedicated pins for 3 SPI bus, and 6 GPIO pins are used for parallel bus programming. TIVA board is placed on downconverter design as a daughter board. Proper connections between the down-converter and TIVA are realized in the schematic design. All schematic design details are given in APPENDIX A.

4.2. LAYOUT DESIGN

In general, RF circuits or high-speed circuit designs also this design include impedance-controlled traces. At first, stack-up planning needs to be composed before starting the layout design. According to design, the impedance controlled RF signals are going to be taken place at the top layer and the second layer will be ground plane as a reference plane for the top layer. Non-fast signals that control active components will take place in the third layer. Also, the ground plane at the second layer is a reference also for preventing interferences from signals at the third layer to the top layer. Lastly, power traces will exist at the bottom layer. When the design is discussed in this manner, 4-layer PCB will be adequate and appropriate.

After predicting the required number of layers, the laminate material of PCB needs to be decided according to the design requirements. The selection of the laminate material is made according to the following characteristics.

- The frequency of operation, bandwidth, and power

- System loss requirements
- Temperature range of system

In generally, laminates with lower loss properties are preferable. The choice has two reasons. One of them is that RF signals have very low power property and consequently insertion loss and noisy elements are undesired. The other one is that losses convert to heat at high power applications.

The insertion losses of the most used laminates depending on the frequencies are shown in Figure 4.3. In many applications, the FR-4 laminate is preferred for using as long as loss and noise budgets are in the safe margin.

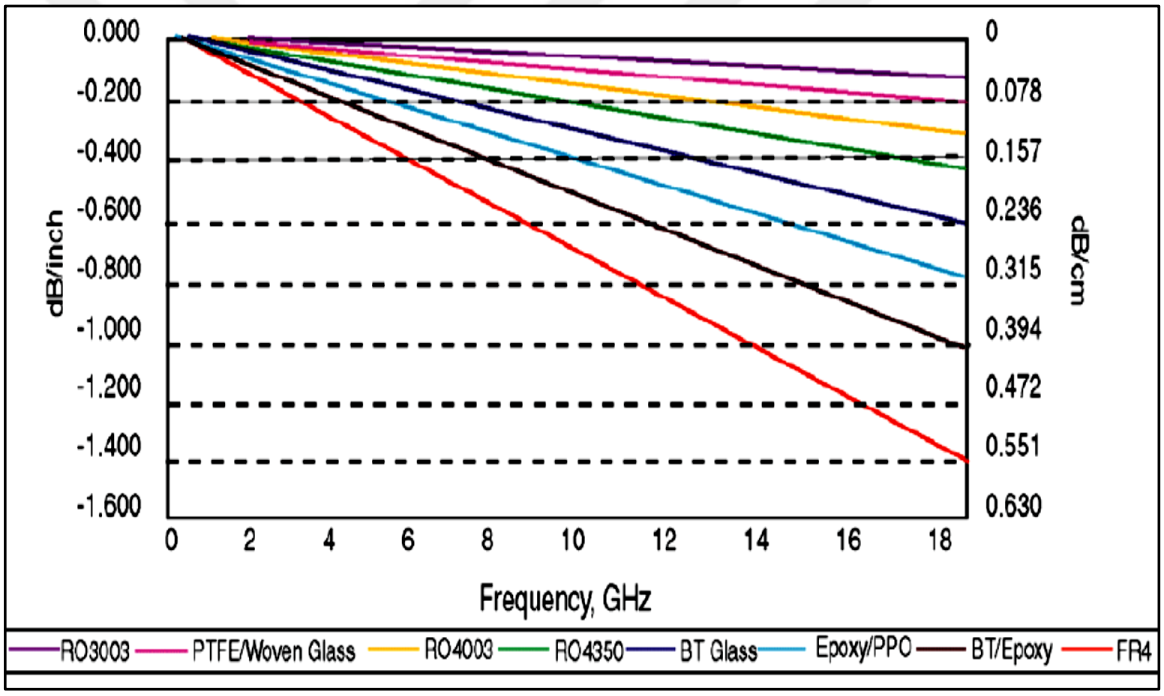


Figure 4.3. Microstrip insertion loss data [36]

Within this design, FR-4 is used due to its cost-effectiveness, and it offers acceptable performance at L-band operations. 4-layer FR-4 stack-up is requested by the manufacturer, to clarify some PCB design specifications and the 4-layer FR-4 stack-up details that the manufacturer can manufacture is given in Figure 4.4.

The stack-up includes copper foil and laminates thicknesses and also dielectric constant information. This information is critical for impedance controlled trace calculations. Apart from the known information, specifications of the solder mask are also crucial for impedance calculations because of covering traces.

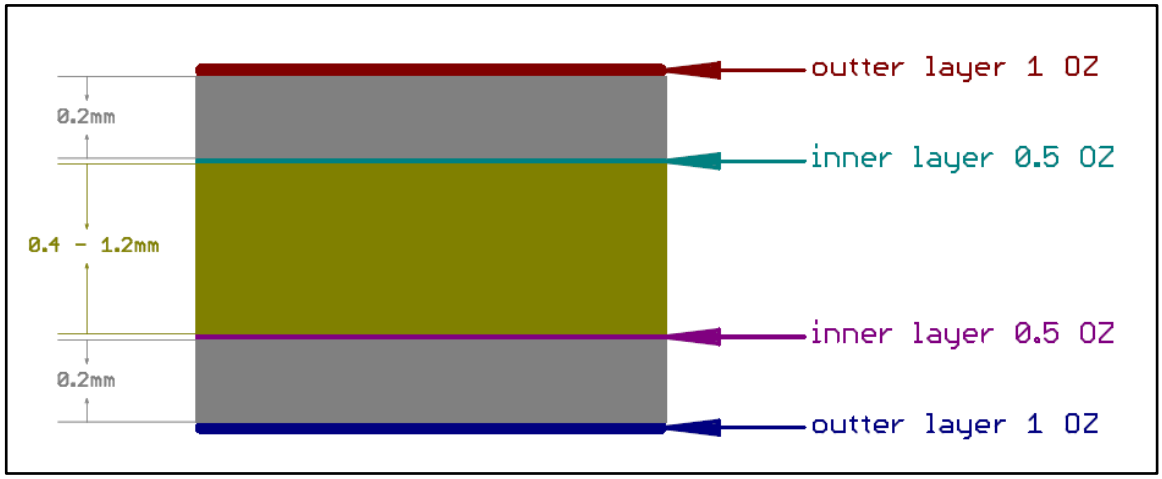


Figure 4.4. Stack-up information provided by the manufacturer

Traces at the outer layer are wrapped by solder mask in the form of a thin membrane. This coating material acts as a dielectric material, so solder mask needs to be taken into account especially high-frequency applications. That is the reason, solder-mask information is requested from the manufacturer and taken into account while calculating impedances. So all information is added to layer stack-up section in Altium Designer. Figure 4.5 shows stack-up information in Altium designer.

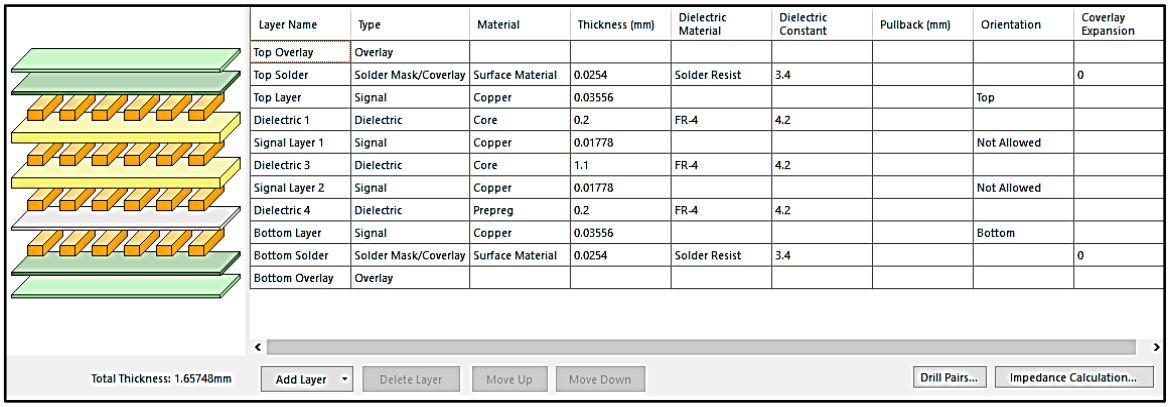


Figure 4.5. Imported stack-up information in Altium Designer

Trace width calculations are made according to stack-up parameters. Grounded Coplanar Waveguide is applied for high-frequency signal traces.

For the calculations, Polar Si8000 Controlled Impedance Quick Solver has used whose products of Polar Instruments. Different types of microstrip, strip-line, and differential traces calculations can be made easily through this software. At the same time, TXLINE tool also can be used for this purpose which includes AWR. However, Si8000 solver allows

entering much more information about PCB properties. Therefore, Si8000 is more convenient for manufactured PCBs. For PCBs that is made from PCB prototyping machines, TXLINE gives enough information.

To calculating traces characteristics, “Coated Coplanar Waveguide with Ground” type is selected on Si8000. In this 4-layer design, top layer carries impedance-controlled traces and second layer act as a reference layer as mentioned before. So the top layer and second layer copper foil’s information and laminate information between these two copper foil are adequate for calculations. As shown in Figure 4.6., necessary information is adapted into software and iterated on trace width and ground separation to obtain 50-Ohm impedance.

While iterating, manufacturer capacities should take into account because there are some limits on manufacturing. These limits are generally minimum trace width, minimum gap separation between traces so the calculated values which are obtained by iterations must not be out of the limitations. Thereby,Minimum trace width and minimum gap between traces is four mil for top layer according to the manufacturer. Trace width simulation is shown in Figure 4.6. Trace width needs to be 13 mils and trace ground separation need to be 15 mils according to the solver.

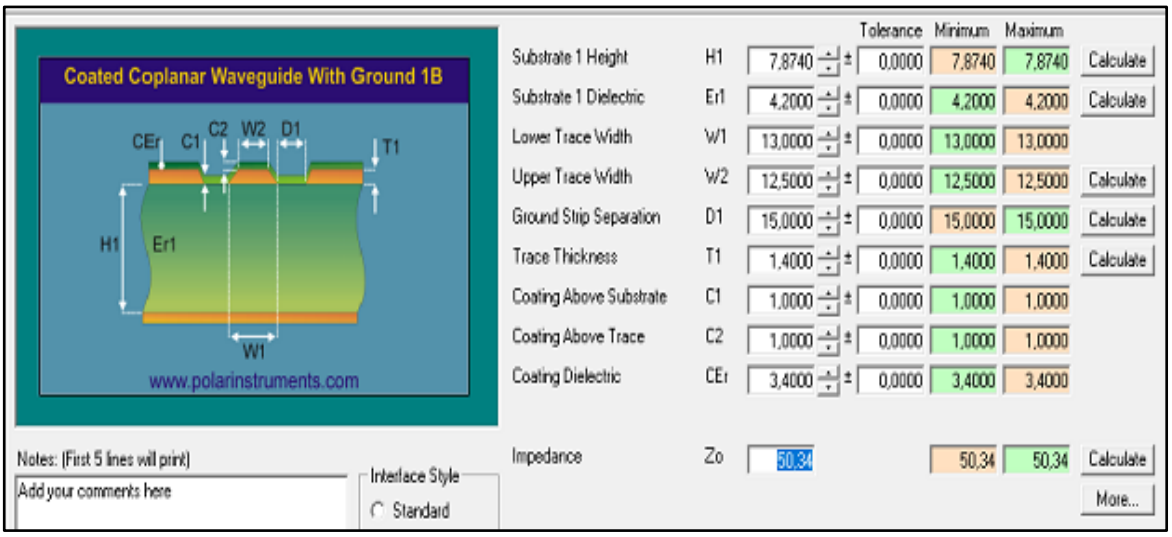


Figure 4.6. The result of the impedance calculation

In order to prevent design faults while designing layout, this information is added to Altium Designer as a rule. Figure 4.7 shows gap rule between coplanar waveguide trace and its ground plane. This rule prevents mistakes such as lower or higher gap between trace and ground plane in Altium designer.

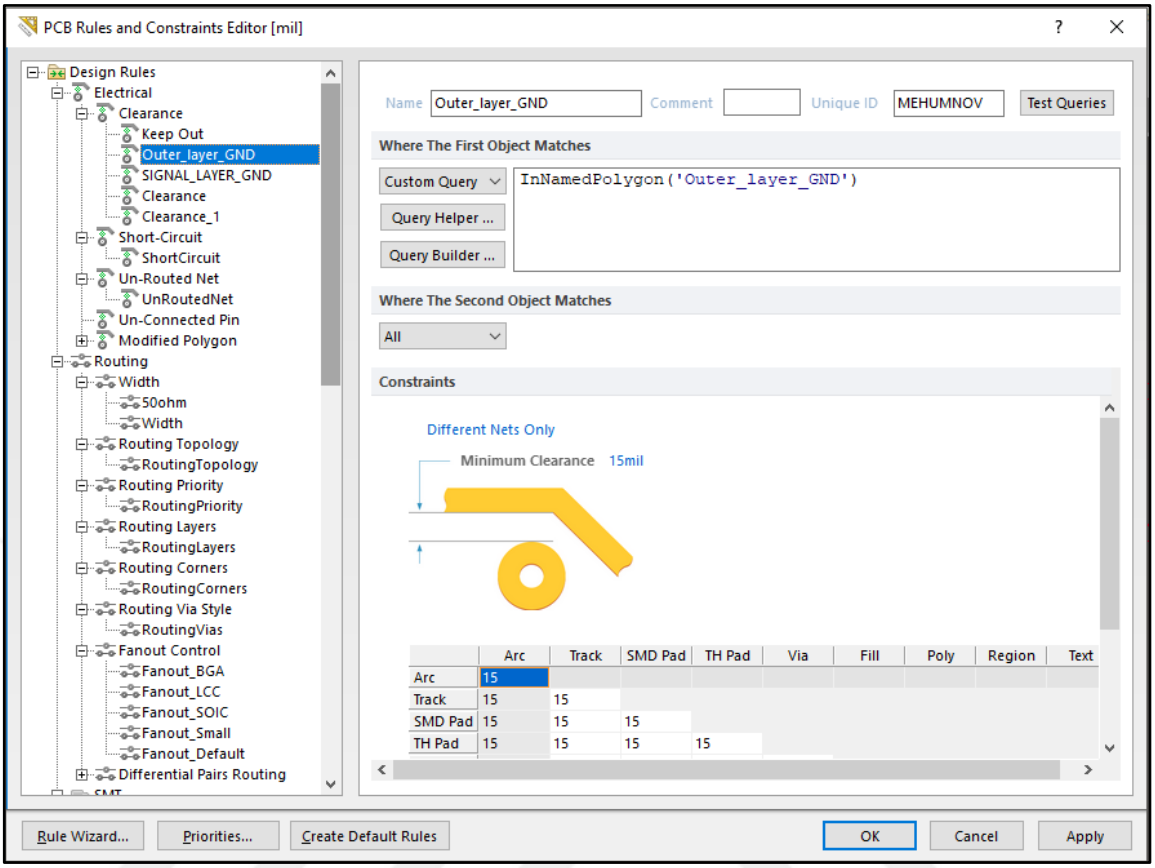


Figure 4.7. Rule definition window in Altium Designer

Also, other manufacturing specifications that came from the manufacturer are added as a rule in Altium Designer to guarantee the production of PCB.

First of all, components in the design are placed roughly and make a prediction about board dimensions. Both this prediction and mechanical needs considered and decide dimensions of boards. After this approach, board dimensions are 150mm x 81 mm. Then precise component placement is conducted. As previously stated, in order not to add extra phase and amplitude errors, In-phase and quadrature sections have to have same trace lengths in some regions and so In-phase, and quadrature sections' parts are placed symmetrically. Firstly, single-ended RF input is divided into in-phase and quadrature parts after 0-degree splitter. After then these traces enter mixers' RF inputs. Traces that have different trace lengths create different electrical length so phase shift. These phase errors also create additional phase errors. Therefore, the image rejection ratio will decrease. Therefore, to keep constant phase errors due to components phase errors, in-phase and quadrature traces lengths are the same in this section. Moreover, this requirement is added to Altium Designer as a ruleset, and Figure 4.8 shows this section traces and trace length details.

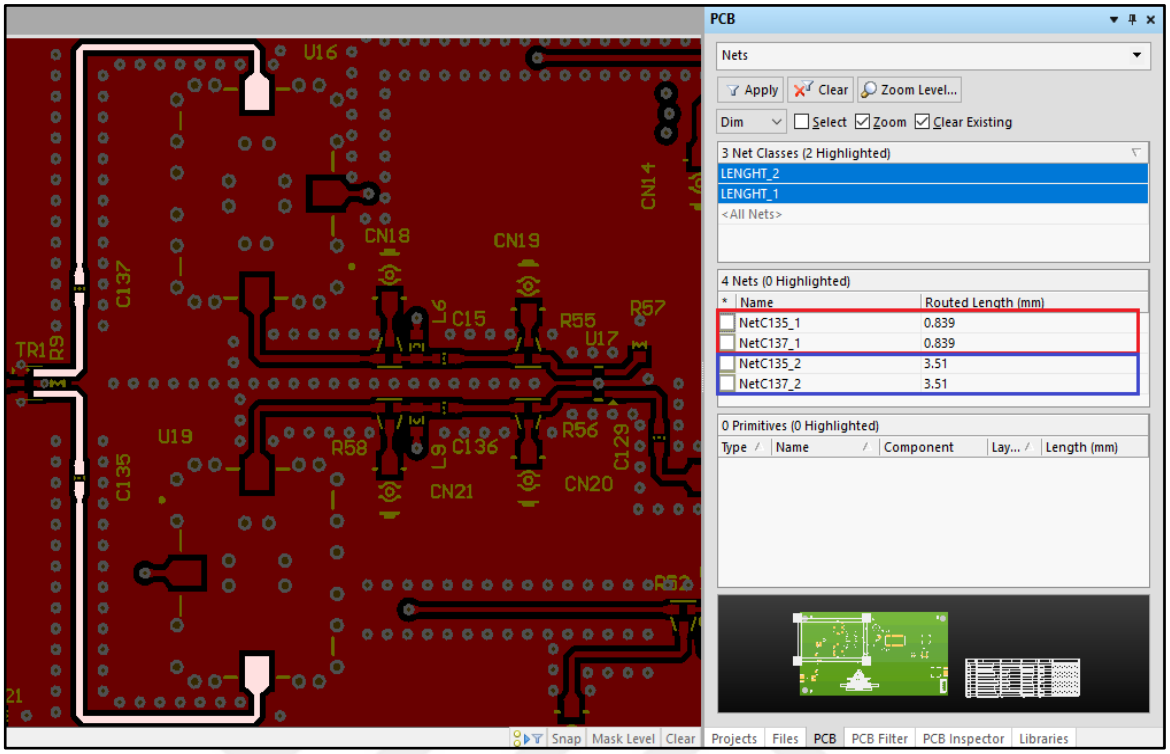


Figure 4.8. Symmetrical traces from the splitter to mixers and length details

In the layout view, highlighted traces come from splitter outputs to mixers RF inputs. After the splitter before the inputs of the mixers, there is a DC blocking capacitor. So both traces after the splitter output to the DC blocking capacitor is same length 0.839 mm. This data is shown in the red box on the right side of Figure 4.8. Also, traces after the DC blocking capacitor until the mixer input have the same length, 3.51 mm length as stated in the blue box on the right side of Figure 4.8. The same case is valid for traces that carry LO signals to mixers. In other words, the in-phase mixer LO trace and the quadrature mixer LO trace have equal lengths. The in-phase mixer's IF output port and the quadrature mixer's IF output port are located in the opposite side of the board. The IF output ports and traces of both in-phase and quadrature mixers are shown in Figure 4.9. As is seen, the trace of the quadrature part needs to be carried in another layer to reach other components of the IF section. The same case can occur for RF or LO inputs of the mixers. This situation is directly related to the mixer's layout orientation and how they are placed. A via needs to used for carrying the signal to another layer and then again another via the need to be used for carrying back the same signal to the top layer.

The vias are commonly used in PCBs which has high-density connections. However, the vias also have inductance and capacitance like PCB traces. That inductance and capacitance

generally are ignored because vias have smaller lengths relative to the trace. Discontinuities and open stubs are come into existence by the vias. That situation causes impedance mismatches also. Therefore all these effects become important whether the traces carry signals which higher than a few hundreds MHz. The following equations show via inductance effect related to frequency. That is the reason, the usage of vias are preferred at IF stages at 70 MHz.

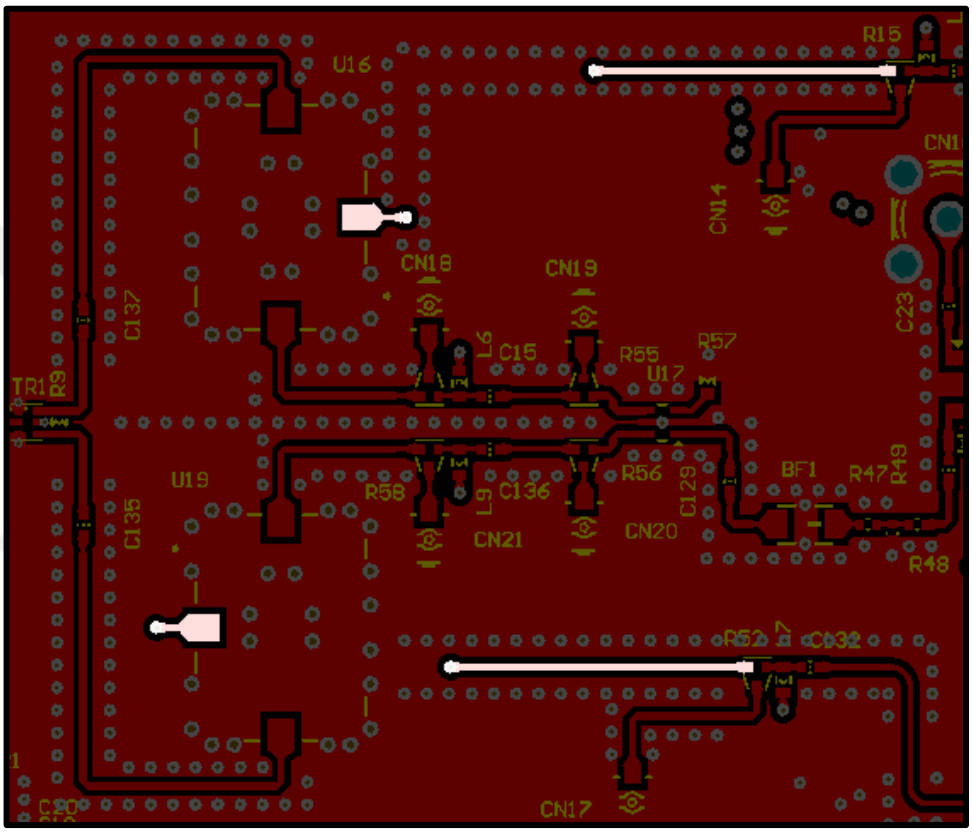


Figure 4.9. The I and Q IF section traces at the output of the mixers

$$L_{Via} = 5.08 * h * (\ln(\frac{4 * h}{d}) + 1) \quad (4.1)$$

$$L_{Via} = 5.08 * 63 * (\ln(\frac{4 * 63}{11.8}) + 1) \quad (4.2)$$

$$L_{Via} \sim 1.3\ nH$$

$$X_L = 2 * \pi * f * L \quad (4.3)$$

$$X_L = 11.8\ ohm\ @\ 1450\ MHz$$

$$X_L = 0.57 ohm\ @\ 70\ MHz$$

Another critical issue in this design is constant phase shift to be applied independently from input RF frequency. The electrical length of the trace with the same trace length will change with frequency because the wavelength varies depending on the frequency. The relation between frequency and phase response of a trace is expressed in the following equations. The propagation constant of a wave along a transmission line could be expressed as;

$$\gamma = \alpha + j\beta \tag{4.4}$$

Where;

$$\alpha = attenuation\ constant$$

$$\beta = phase\ constant$$

$$\beta = \frac{2\pi}{\lambda}\ (radian/meter) \tag{4.5}$$

Where;

$$\lambda = Wave\ lenght$$

The wavelength could be expressed as;

$$\lambda = \frac{c}{f\sqrt{\epsilon_R}}\ (meters) \tag{4.6}$$

Where;

$$f = Frequency$$

$$c = Speed\ of\ light$$

$$\epsilon_{Reff} = Effective\ dielectric\ constant$$

The phase velocity is;

$$v_p = \lambda f = \frac{2\pi}{\beta} f\ (meters/second) \tag{4.7}$$

The time delay is;

$$Time\ delay = \frac{l}{v_p} = \frac{\beta l}{2\pi f}\ (seconds) \tag{4.8}$$

Where;

$$l = Lenght$$

Therefore, the electrical length of a trace could be expressed as:

$$Electrical\ Lenght = \beta l\ (radians) \tag{4.9}$$

$$Electrical\ Lenght = \frac{2\pi}{\lambda} l\ = \frac{2\pi}{\frac{c}{f\sqrt{\epsilon_{Reff}}}} l\ (radian) \tag{4.10}$$

$$Electrical\ Lenght = \beta l\ x\ \frac{360}{2\pi}\ (degree) \tag{4.11}$$

The phase response of a CPW trace with 3 mm length from 1 GHz to 2 GHz is simulated and given in Figure 4.10

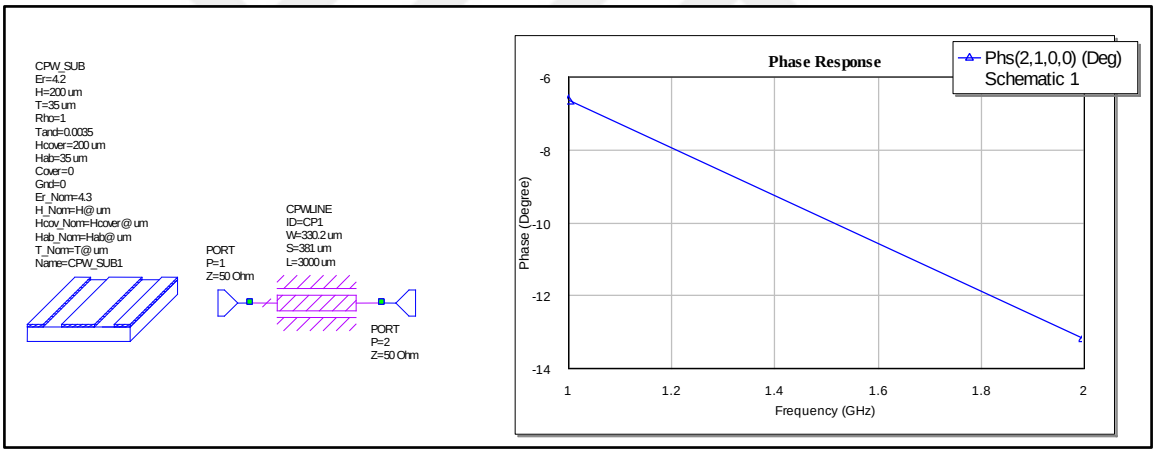


Figure 4.10. The phase response of a co-planar waveguide trace

That is the reason why phase shift needs to be applied at IF stages 70 MHz because of all the received signals is downconverter to 70 MHz. Also, all phase errors will be appeared in cumulatively at If stage. As stated in section 3.1.2.2, the necessary phase shift value is 2.371 degree at 70 MHz. Electrical length calculation is conducted by TXLINE tool. Figure 4.11 shows the calculated trace length value. Also, electrical length is calculated according to Equation (4.10) and Equation (4.11) and given the following equations.

$$f = 70\ MHz$$

$$c = 3\ \cdot 10^{8}\ m/s$$

$$\epsilon_{Reff} = 3.0638$$

$$Electrical\ Lenght = 2{,}371 - degree$$

$$2{,}371 = \frac{\frac{2\pi}{3 \cdot 10^8}}{70 \cdot 10^6\sqrt{3{,}0638}} lx \frac{360}{2\pi} \tag{4.12}$$

$$l = 0{,}01612\ m = 16{,}12\ mm$$

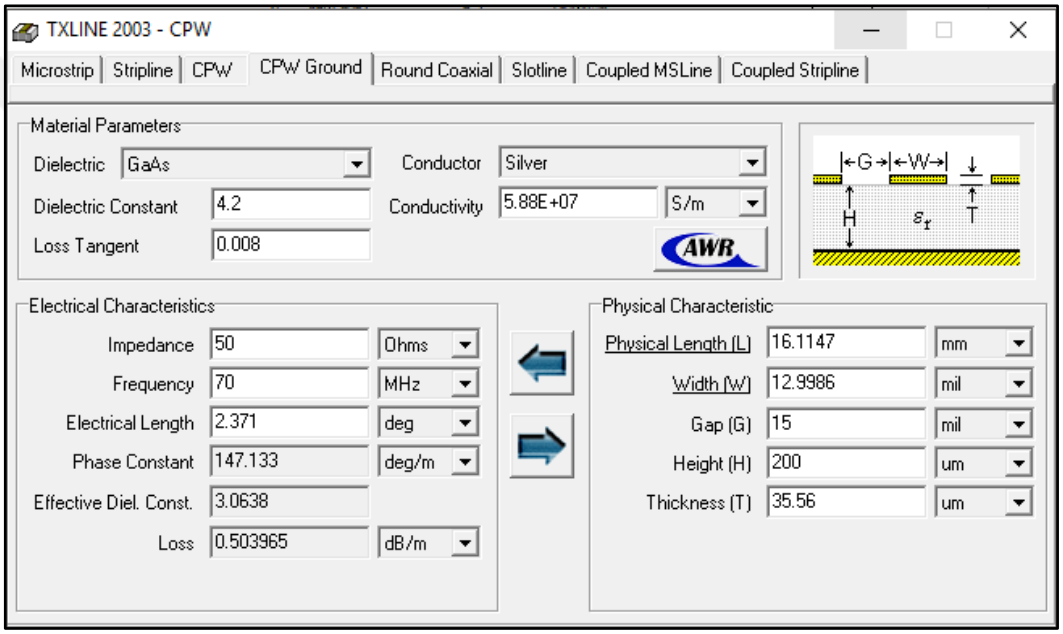


Figure 4.11. Electrical length calculation

While composing these two critical traces, differences of the routed lengths are checked on Altium Designer. The trace name that takes part in the in-phase section is “NETC82_2,” and the trace name that takes part in the quadrature section is “NETC132_2”. There are also another traces in both in-phase and quadrature section which come from mixers to the DC blocking capacitors. However, these traces are drawn completely equal. So to ensure 2.371-degree phase difference between “NETC82_2” and “NETC132_2”, 16.11 mm difference is sufficient. The phase of the quadrature section values is behind the in-phase section as stated before. Therefore the quadrate section trace need to be 16.11mm longer than the in-phase section. At first, in-phase section trace “NETC82_2” is drawn and then quadrature section is drawn. Figure 4.12 shows detailed data about this method. The highlighted upper trace is “NETC82_2,” and the highlighted bottom trace is “NETC132_2” in Figure 4.12.

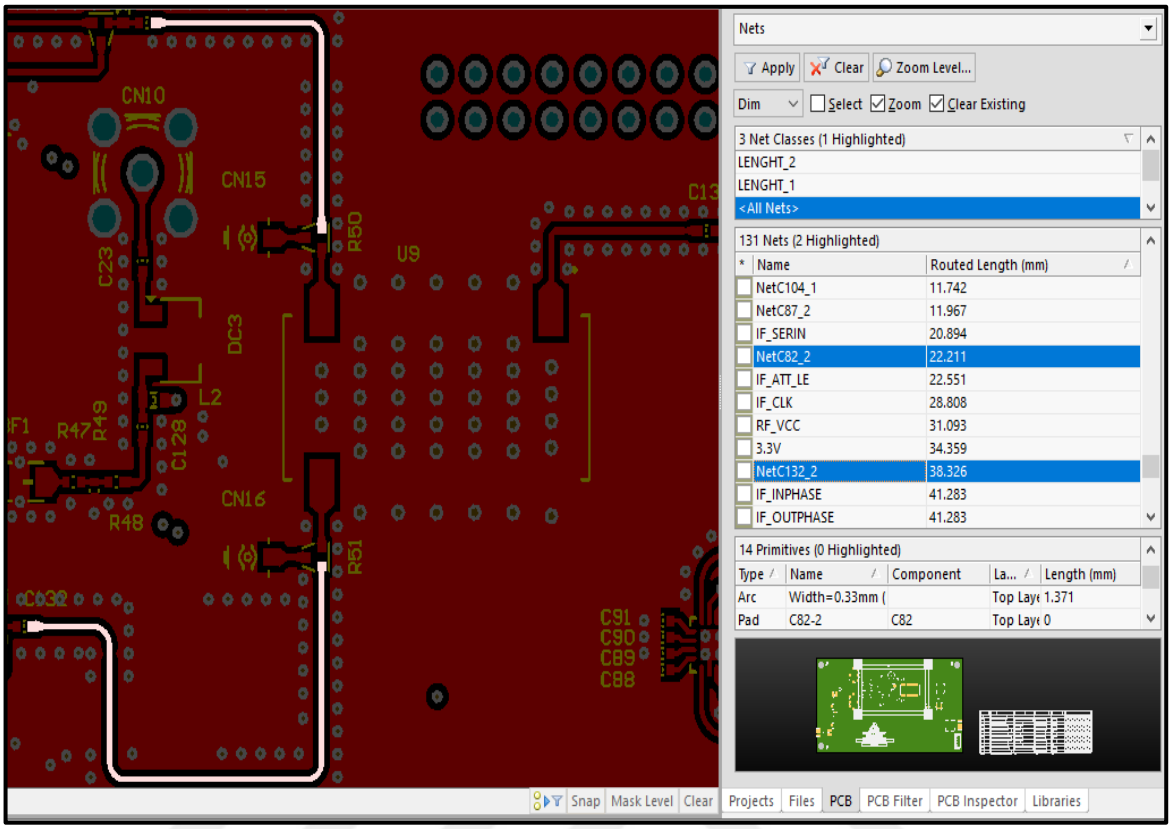


Figure 4.12. In-phase and quadrature parts' traces

The trace of the in-phase section “NETC82_2” length is 22.211 mm, and the quadrature section trace “NETC132_2” length is 38.326 mm. The difference between these two traces is 16.115 mm. Therefore, the quadrature section trace is longer than the in-phase section’s. The 2,371-degree phase shift is composed by the length difference at 70 MHz.

Tiva evaluation board is used as a controller and is assembled as a daughter board to the design. The Tiva’s control pins are gone out from the board with two pieces 2x20 pin header. The pin headers are male type at the top side and are female type at the bottom side of the Tiva Evaluation board. Both two types could be used. Furthermore, principal components and critical traces exist on the top side. Because of that reason, The Tiva is placed at the bottom of the design, and the female header type side is used. This kind of placement also provides convenience during measurements and tests.

After composing the design, Design Rule Check(DRC) is run in Altium Designer. DRC is a powerful automated feature that checks both the logical and physical integrity of a design. This feature should be used on every routed board to confirm that rules are maintained, and there are no other design violations. It is particularly recommended that a batch mode DRC

always be performed before generating final artwork. Moreover, general rules are mentioned previously. DRC errors according to rules are eliminated. The views of all signal layers are shown in 0., and the 3D view of the design is shown in Figure 4.13. and Figure 4.14.

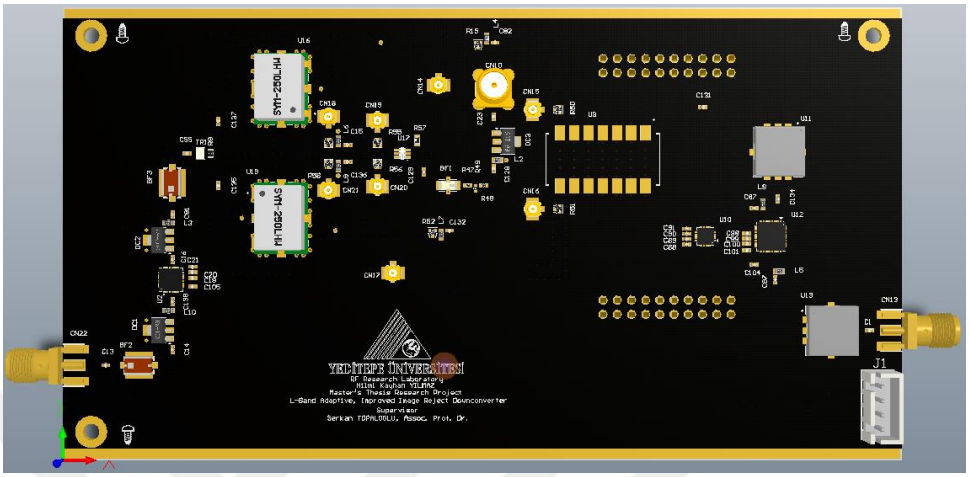


Figure 4.13. 3D view of design from the top

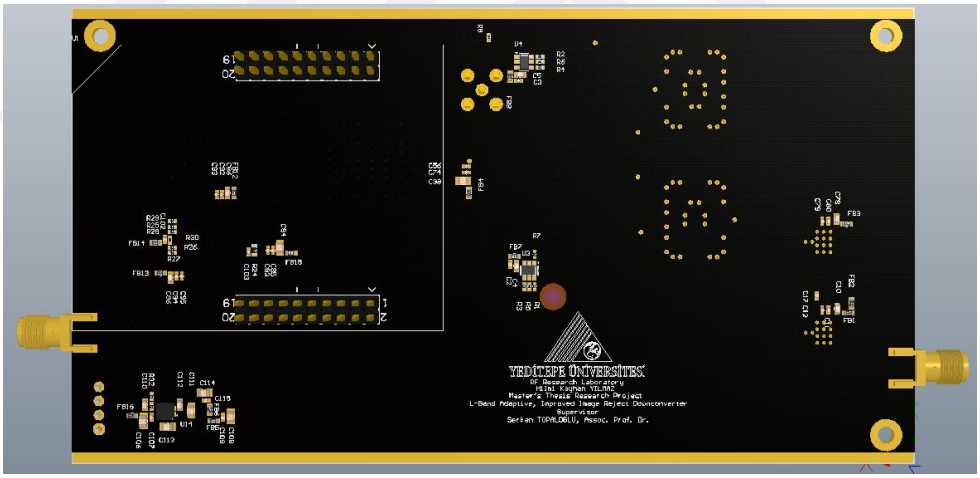


Figure 4.14. 3D view of design from bottom side

After that, manufacturing files which are necessary for production, are exported in "Gerber File Format" for each layer of PCB. Vias and mechanical hole coordinates and sizes are exported in "NC Drill File Format." Later these files are sent to the manufacturer.

4.3. IMPLEMENTATION AND TESTS

The post-production image of the design described in the previous section design stages is in Figure 4.15. Manuel placement of the components is soldered in proper order. After

placement of the components, TIVA board is used for programming of the components which are necessary. To obtain about -10 dBm signal power at IF port, -20 dBm input signal power is applied at RF port. -20 dBm signal power needs to be attenuated because the signal path has high gain resulting in the saturation of components that are placed in the signal path. The higher tuning power range of the receiver is given by this amplifying stages. Therefore, attenuators are placed with proper attenuating values for convenient operation. The LO power of the mixer is the other critical issue. Effects of different LO power stages is represented in the datasheet. For proper mixer operation, LO power needs to be about 10 dBm. When considering LO path gain, -4 dBm signal needs to be applied to LO signal to obtain 10 dBm power.

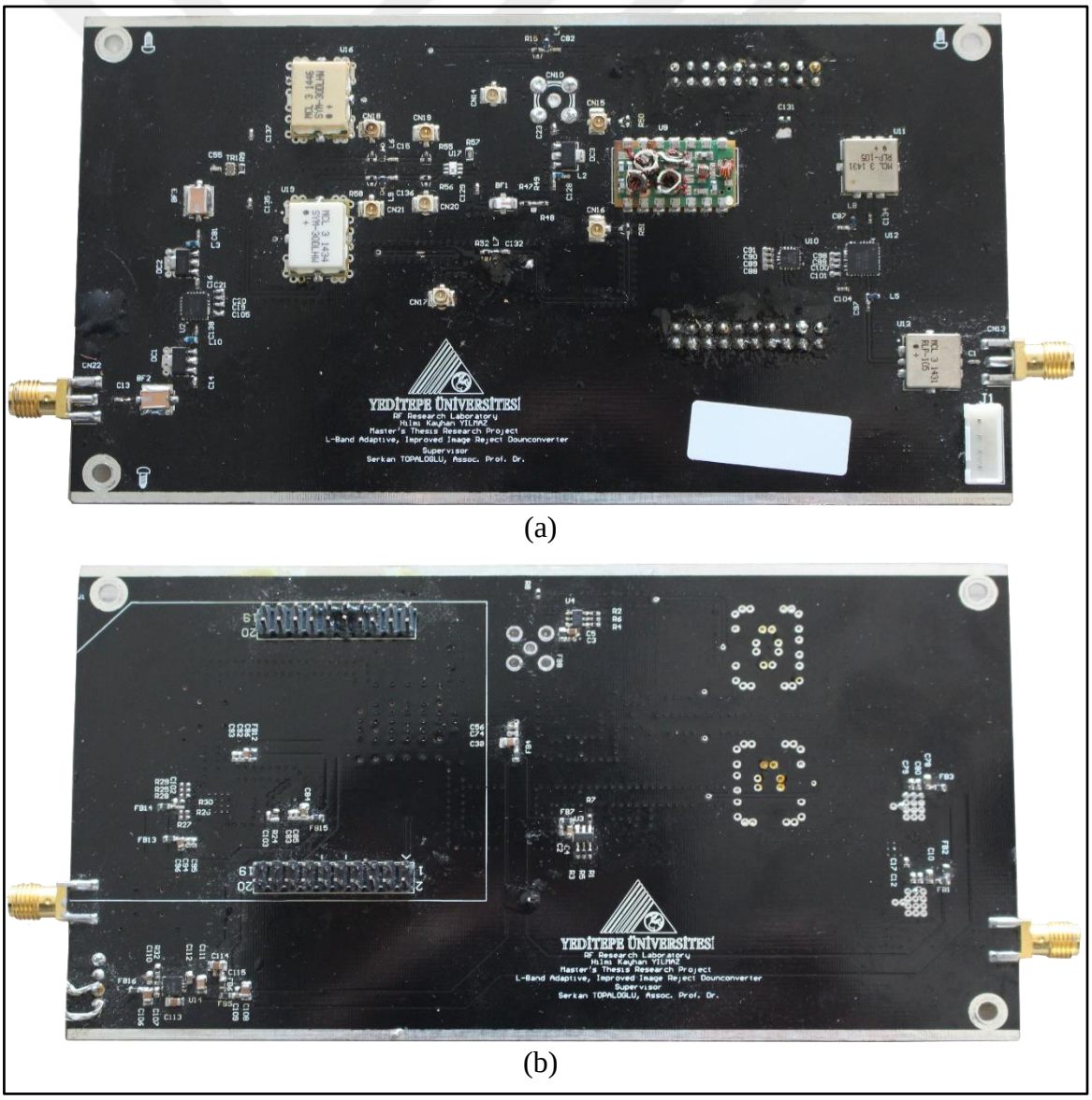


Figure 4.15. Post-production image of the design. (a) Top view, (b) Bottom view

TIVA board is used for programming of the components which are necessary. To obtain about -10 dBm signal power at IF port, -20 dBm input signal power is applied at RF port. -20 dBm signal power needs to be attenuated because the signal path has too much amplifying which causes saturating components that are placed in the signal path. The higher tuning power range of the receiver is given by this amplifying stages. Therefore, attenuators are arranged proper attenuating values for convenient operation. The LO power of the mixer is the other critical issue. Effects of different LO power stages is represented in the datasheet. For proper mixer operation, LO power needs to be about 10 dBm. When considering LO path gain, -4 dBm signal needs to be applied to LO signal to obtain 10 dBm power.

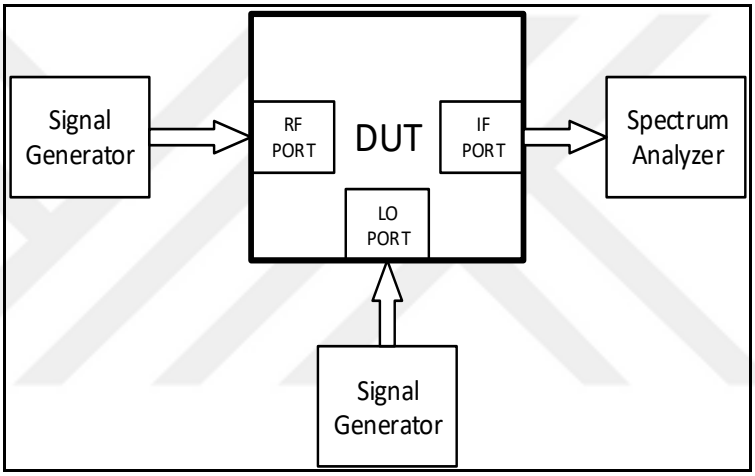


Figure 4.16. Block diagram of the test setup

Signals which are located in 950-1450 MHz are applied to RF port by using test set-up in Figure 4.16. LO frequency is also applied LO connector with respect to RF frequency and LO is changed to maintain constant IF signal at 70 MHz when RF signal frequency is changed. An example of measured IF signal with a spectrum analyzer is represented in Figure 4.17.

The down-converted fundamental signal is represented above. Same way, the image signal is applied which has a 140 MHz difference between the fundamental. An example of the down-converted image signal is shown in Figure 4.17. Both down-converted fundamental signal power and image signal power are measured with the same method.

As discussed before, The DC voltage is being applied to IF port to improve image rejection ratio, but first, any DC voltage is not applied to get unmodified signal powers. Band-pass filters on the RF path is useful within 950-1450 MHz. So the image rejection ratio

measurement is applied between 960 MHz and 1310 MHz to measure pure image rejection value without RF band-pass filter effect. In that case, RF fundamental frequency is applied from 1090 MHz to 1450 MHz due to applied image frequencies. Thus DC biasing effect could be distinguished on both fundamental and image signal easily.

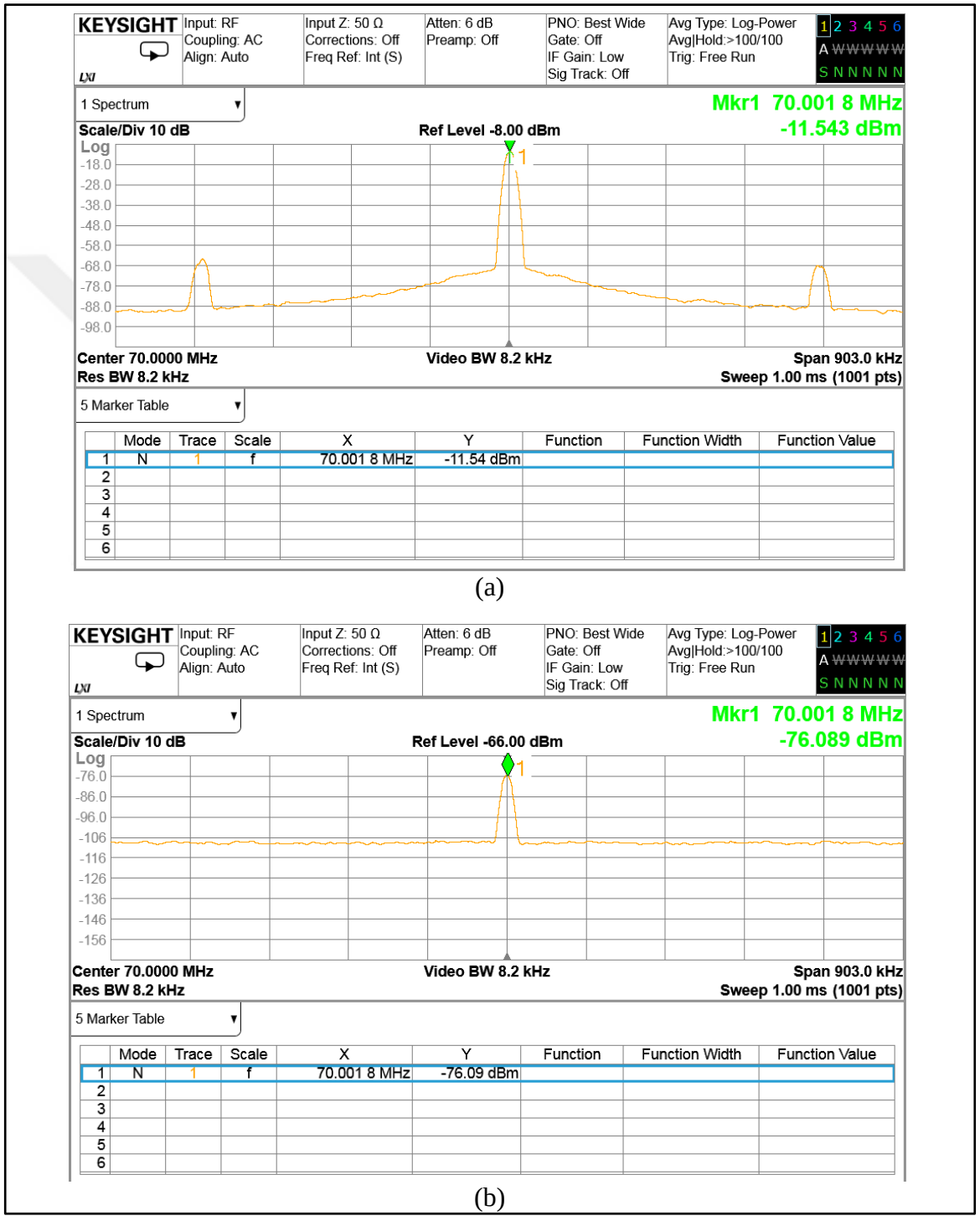


Figure 4.17. Measurement results. (a) Down-converted fundamental signal, (b) Down-converted image signal

In a word, the fundamental signal is applied from 1090 to 1450, and the image signal is applied from 960 to 1380 MHz. At first, down-converted fundamental signals are measured over the band and data is saved from the spectrum analyzer. Also, the data is imported to AWR MWO to draw characteristic on over the band. The down-converted fundamental signal power is shown in Figure 4.18. from 1100 MHz to 1450 MHz.

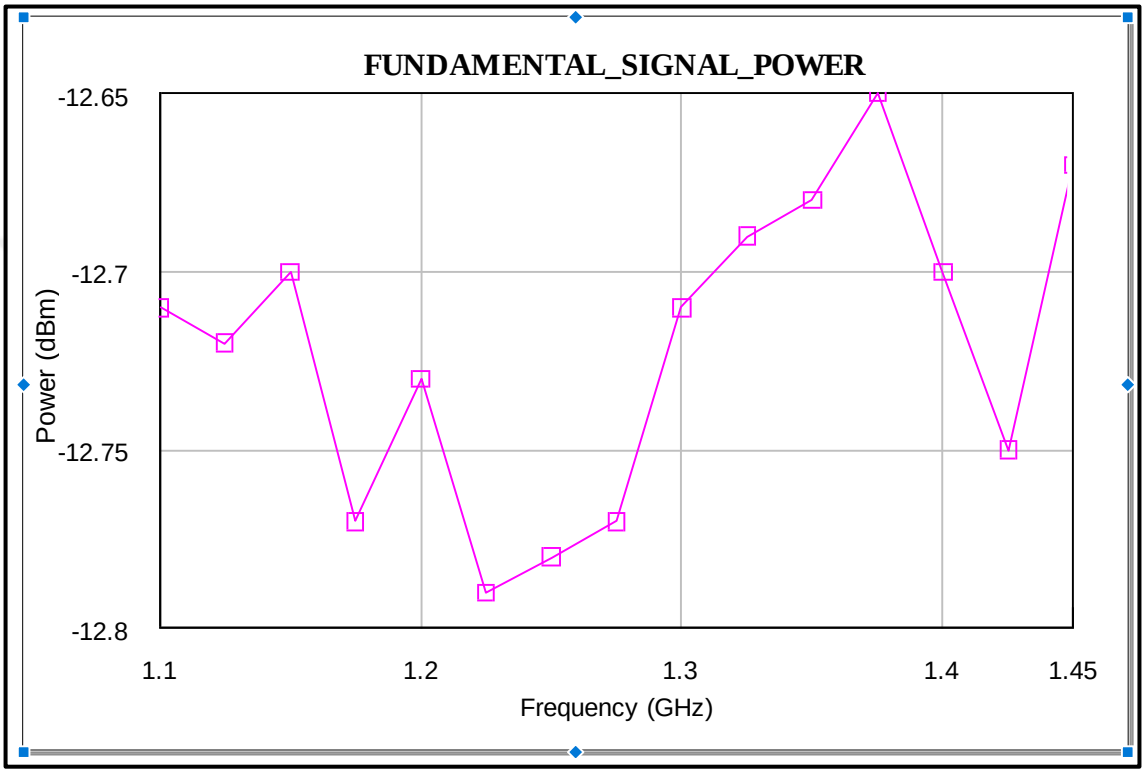


Figure 4.18. The down-converted fundamental signal power

In the same way, the down-converted image signal power is measured without any bias. The down-converted image signal power is shown in Figure 4.19. In normal operation of double balanced, the down-converted image signal power must be the same with the down-converted fundamental signal power. For instance, the fundamental is located at 1450 and image signal is located at 1310 MHz. Moreover, their down-converted signal power should be same and about -12.6 dBm at IF port. However, down-converted image signal power is about -53 dBm. Therefore, the image signal rejection is attained by that method, and the image rejection ratio is about 36 dB.

The image rejection ratio is defined by the difference between the down-converted image signal and down-converted fundamental signal powers in terms of dB. Figure 4.20 shows the image rejection ratio without any bias to the mixer.

The best image rejection ratio is obtained at 1.185 GHz, and the worst is at 0.96 GHz. As mentioned before, the best image rejection performance is expected close to the center of the band. There is an offset between simulation and measurement on the best point of the image rejection ratio. The comparison image rejection ratio between simulation and measurement results is shown in Figure 4.21.

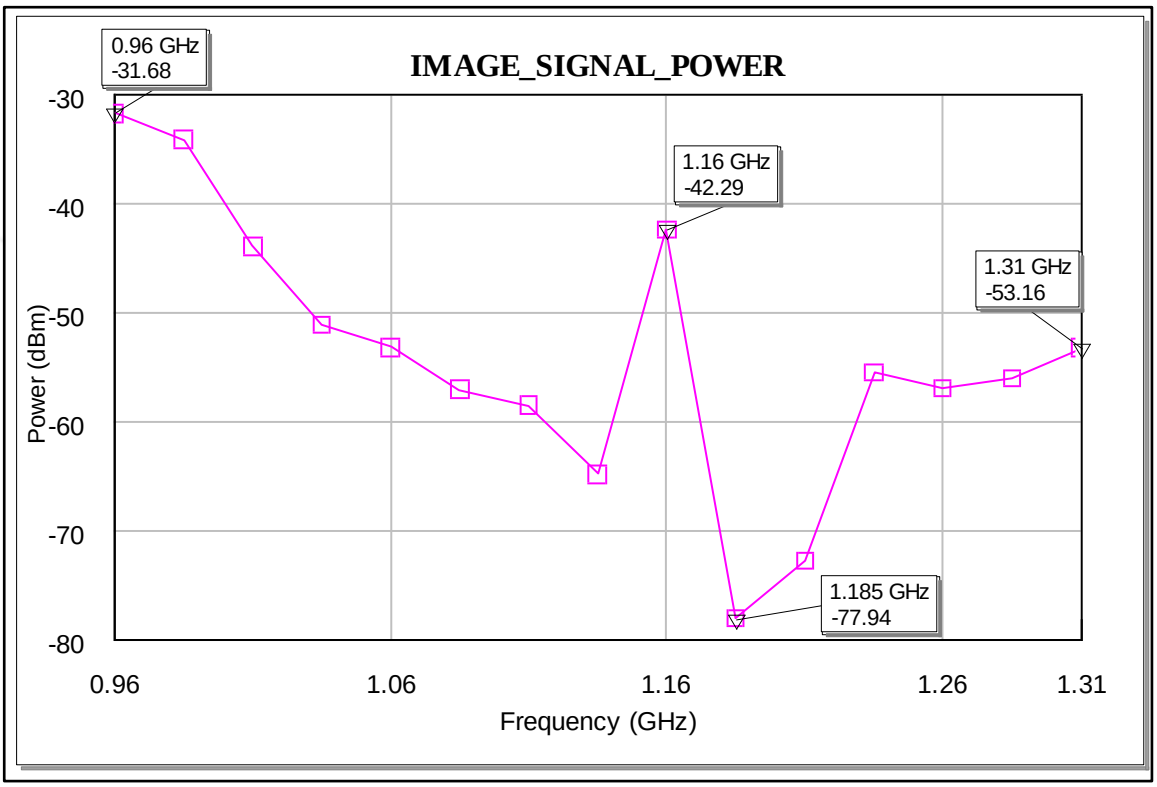


Figure 4.19. Down-converted image signal power with w.r.t. image signal frequency

Measured data demonstrate that best amplitude and phase match is provided at 1.185 GHz. The simulation best image rejection ratio result is obtained from s-parameters. On the other hand, these simulation values and measured data do not match. Minor change in amplitude and phase relation between in-phase and quadrature parts due to component characteristic cause significant changes in image rejection values. Likewise, Mixer's insertion loss and phase relation are taken into account as identical in simulations. Moreover, also mixer which is used in the design is a discrete design that causes minor characteristic changes. In brief, there are differences in simulation and measured data, and so these measured values are not enough for high-performance products. The proposed method to improve amplitude mismatch between in-phase and quadrature part is applied as mentioned before. Test setup for the proposed method is shown in Figure 4.22.

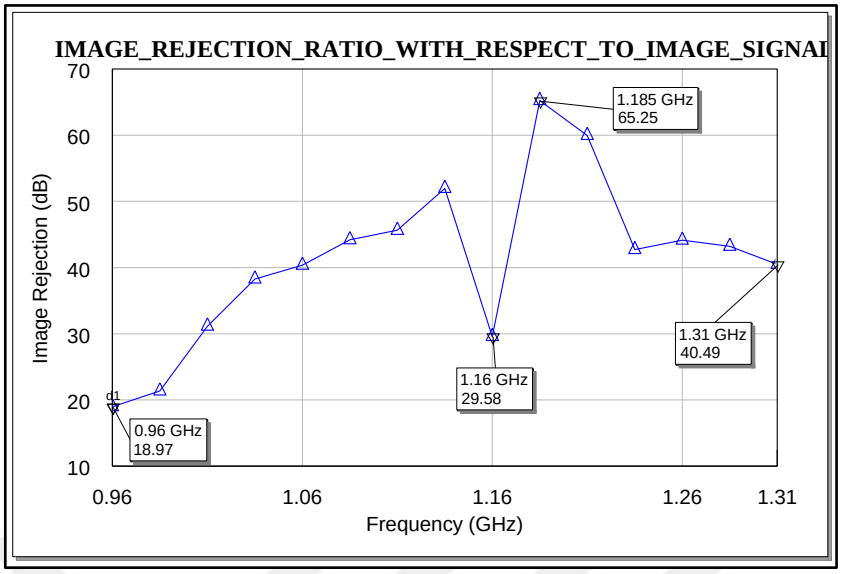


Figure 4.20. Image rejection ratio w.r.t. image signal frequency

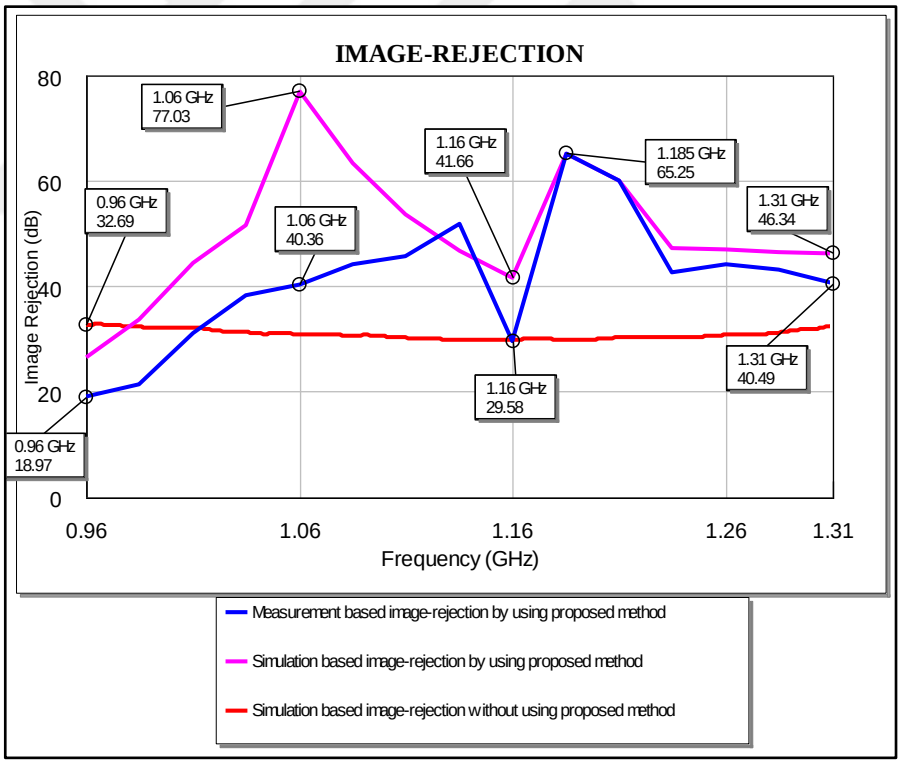


Figure 4.21.Simulation and measurement results of image rejection ratio

DAC is placed both I and Q parts of the downconverter to apply required DC biased point. DACs are needed to be programmed via SPI bus to get required DC voltage point. On the other hand, instead of using DAC in the test setup, I and Q parts are biased directly with a DC power supply to provide convenience in tests. In Figure 3.19, insertion loss of the in-phase side is higher than the quadrature side from 810 MHz to 940 MHz, and the insertion

loss of the quadrature side is higher than the in-phase section from 940 MHz to 1310 MHz according to the simulations. As proposed before, If the DC bias voltage is applied to the in-phase section from 940 MHz to 1310 MHz, insertion loss of that section will be increased and reached to same insertion loss point of quadrature section. Therefore, the amplitude imbalance effect on image rejection is eliminated. By using the same method, If DC bias voltage is applied to quadrature side from 810 MHz to 940 MHz, insertion loss of the quadrature side will be increased, and the same amount of insertion loss of in-phase side will be achieved. On the other hand, the image signal is suppressed by usage of bandpass filter till 950 MHz. The proposed method is evaluated from 950 MHz to 1310 MHz to see the individual effect on image rejection improvement. That is the reason for DC bias voltage is applied at IF port of the in-phase section mixer. Table 4.2 demonstrates the best image rejection performance with respect to DC bias values.

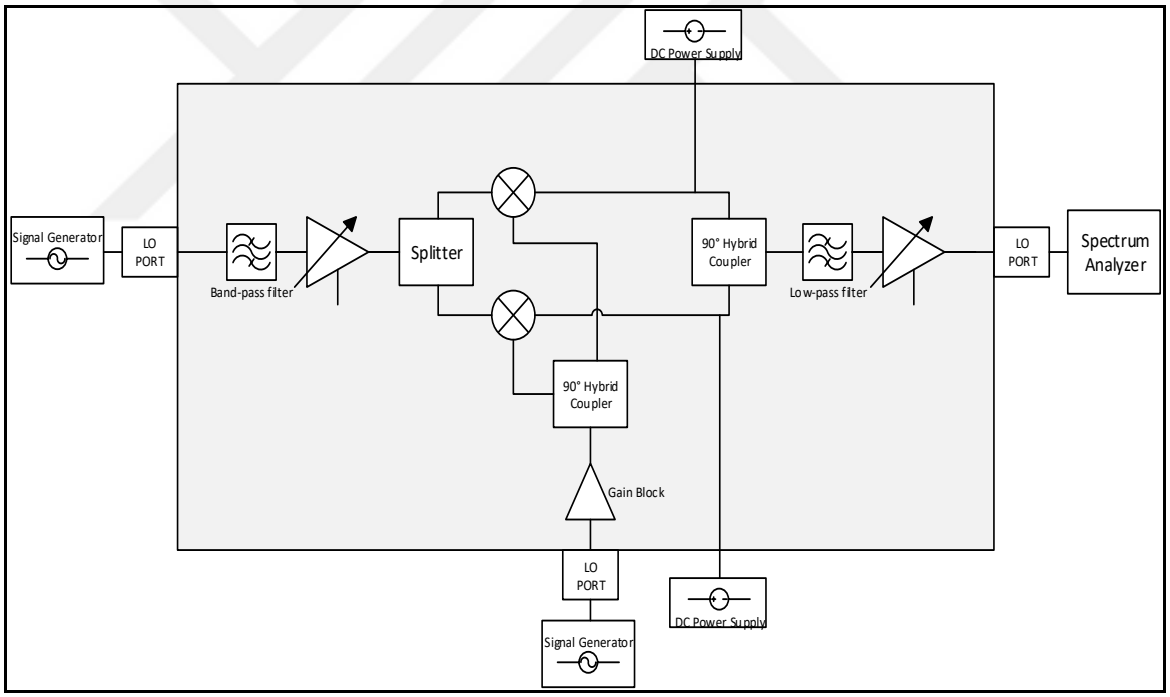


Figure 4.22. Measurement setup of the adaptive image reject topology

DC biased points are an optimum point where best image rejection points are obtained. Above and below these points, worse image rejection values are obtained. Insomuch as, image rejection values get worse at some points if any DC voltage is applied. On the other hand, while image rejection ratio is improved by applying DC biasing, the down-converted fundamental signal is also affected. Figure 4.23 shows the DC bias effect on fundamental signal power.

Table 4.2. Adaptive image-rejection ratio measurement results

Fundamental Signal Frequency (MHz)	Down-converted Fundamental Signal power (dBm)	Down-converted Fundamental Signal Power After Optimum DC Bias Applied (dBm)	Image Signal Frequency (MHz)	Down-converted Image Signal power (dBm)	Down-converted Image Signal Power After Optimum DC Bias Applied (dBm)	Image Rejection Improvement (dB)	Optimum DC biased point (VDC)
1100	-12.67	-12.51	960	-31.68	-39.22	7.54	0.28
1125	-12.75	-12.65	985	-34.07	-46.25	12.18	0.28
1150	-12.70	-12.58	1010	-43.85	-57.10	13.25	0.29
1175	-12.65	-12.59	1035	-51.05	-64.36	13.31	0.28
1200	-12.68	-12.68	1060	-53.09	-89.72	36.63	0.27
1225	-12.69	-12.69	1085	-56.99	-76.12	19.13	0.21
1250	-12.71	-12.69	1110	-58.42	-66.32	7.9	0.18
1275	-12.77	-12.74	1135	-64.73	-64.73	0	0
1300	-12.78	-12.75	1160	-42.29	-54.35	12.06	0.06
1325	-12.79	-12.75	1185	-77.94	-77.94	0	0
1350	-12.73	-12.69	1210	-72.65	-72.65	0	0
1375	-12.77	-12.72	1235	-55.37	-59.74	4.37	0.2
1400	-12.70	-12.65	1260	-56.84	-59.61	2.77	0.3
1425	-12.72	-12.67	1285	-55.96	-59.05	3.09	0.31
1450	-12.71	-12.65	1310	-53.16	-58.85	5.69	0.3

When the fundamental signal power is compared under biased and unbiased conditions, the most significant change is about 0.1 dB. In a typical receiver, 0.1 dB change in amplitude is not a remarkable change. Therefore, the receiver or downconverter system performance will not be affected.

After applying DC voltages, measured and expected image rejection values should be the same.Nevertheless, there are differences between expected and measured data. DC bias

effect on image signal power is shown in Figure 4.24. As mentioned before, there are several reasons for dissimilarities.

On the other hand, there are also phase mismatch, unlike simulation data files. Therefore this difference creates extra degradation in image rejection ratio. In this study, only amplitude mismatch correction is focused on, and observations prove that the proposed method works fine as expected.

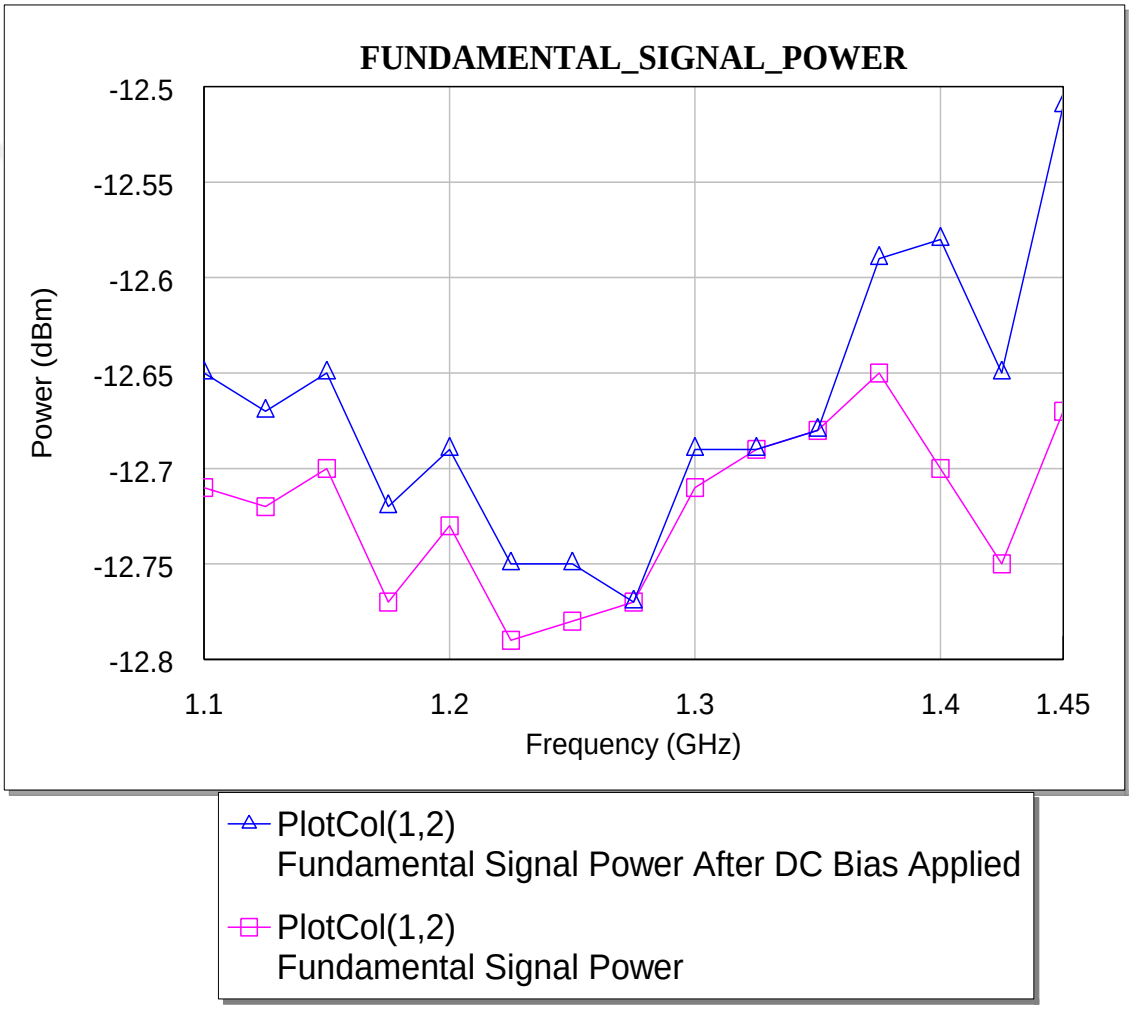


Figure 4.23. Bias effect on fundamental signal

Finally, DC bias values should be applied via DACs when downconverter is working. Especially for FHSS, this method should be applied fast and orderly. There should be a LUT, and it should contain DC values with respect to image frequency of fundamental frequency. As an example, if the communication channel is arranged at 1200 MHz, then the image signal will be located at 1060 MHz. Therefore significant bias voltage value 0.27 VDC is

obtained from the controller with the aid of LUT for 1060 MHz and the necessary information is written to DAC's register map by SPI bus. So instead of obtaining 40 dB image rejection, 77 dB image rejection will be obtained using this method.

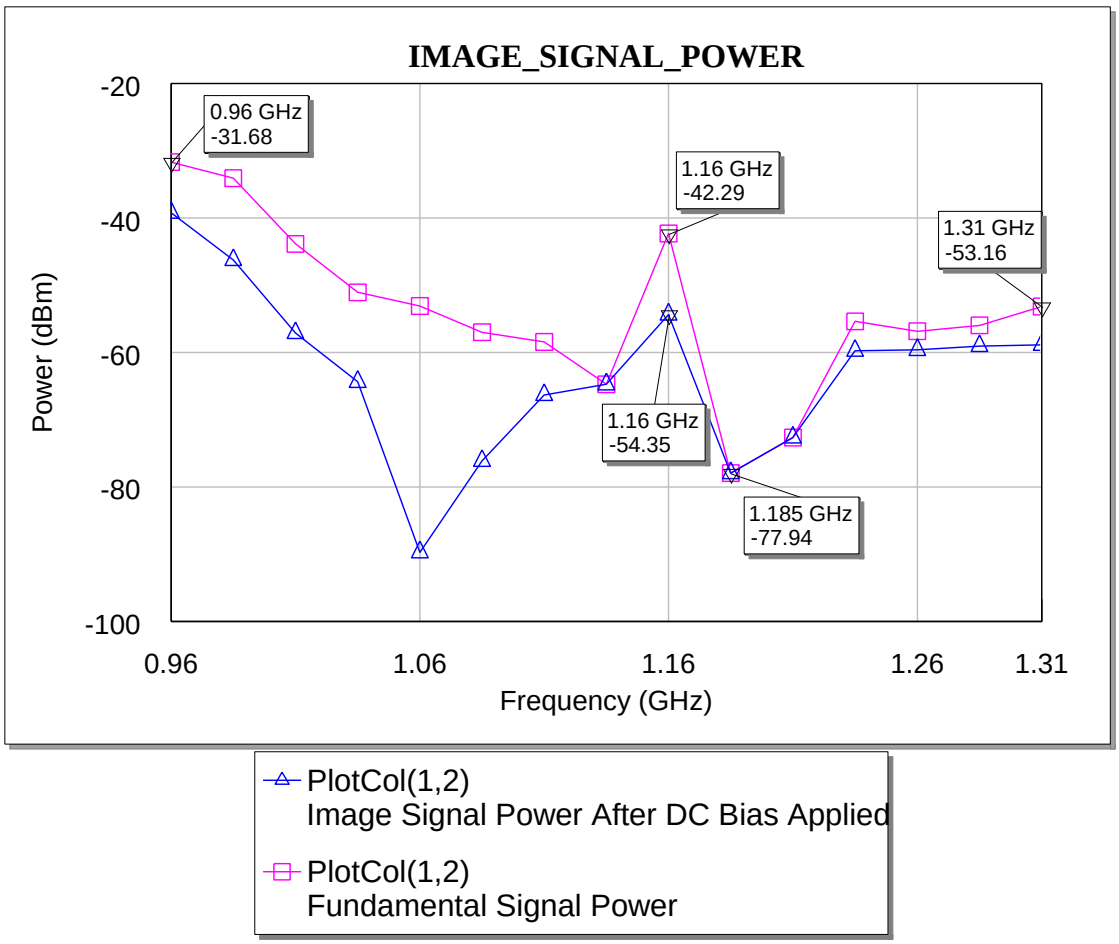


Figure 4.24. Bias effect on the image signal

5. SPURIOUS-FREE SIGNAL GENERATOR DESIGN

5.1. SYNTHESIZER HARDWARE DESIGN

The proposed design offers a solution for the fractional spurious response. The spurious response in fractional PLLs is directly related with the PFD frequency and the feedback divider's fractional part. If the PFD frequency is changed, both integer and fractional part of the feedback divider will be changed. Besides, multiplication of the PFD frequency and fractional part of the feedback divider will be changed. Thus, the fractional spurs location can send away from the carrier and can be removed by the loop filter. For instance, the PDF is arranged as 50 MHz, and the desired frequency is set to 3000.01 MHz. In this present case, the feedback divider ratio will be 60.0002, and fractional spur will exist at 10 kHz away from 3000.01 MHz. The spurious signal cannot be filtered by the loop filter.

On the other hand, the PFD is set to 48 MHz, and feedback divider ratio is arranged as 62.5 to obtain 3000.01 MHz. Thus spurious will exist at 24 MHz away from the carrier. The new spurious response could be easily removed by the loop filter. The spurious reduction is obtained by this method.

On the other hand, this method requires changing in the PFD frequency. The PFD frequency could be changed by the reference clock divider which is located in RF PLL. Degradation in phase noise will be caused due to the PFD frequency decreasing. Indeed, the method could not be the solution. Assume that, the reference divider ratio 2, the PFD frequency is 25 MHz and feedback divider ratio is 120.0004. Thus, the spurious signal will exist at 10 kHz away again. To proper operation, intermediate PFD values required and these values should be obtained from the tunable reference source. The different reference clock signals are needed for proper spurious reduction for tiny tuning sizes. Thereby, a PLL based clock distribution devices should be suitable for this operation.

Nevertheless, changing reference clock frequency speed is critical for FHSS. While this operation, PLL lock condition of the clock distribution device needs not to be corrupted. In a word, lock time of the clock distribution device should not be added to RF PLL lock time. Both spur reduction ratio and lock time issues are discussed because this study focuses on

spur reduction and effects for FHSS systems.

Benchmarking is conducted on clock distribution devices in the market. AD9524 clock generator from Analog Devices is selected as a clock source for the RF PLL in the proposed design. The lock time is not taken into consideration because the locking condition will be occurred after the power-up and remained unchanged. Therefore, locking time is not a critical issue when benchmarking. The phase of the RF PLL is directly related with phase noise of the clock source. The phase noise characteristic comes into prominence. The AD9524 is not just an ordinary clock distribution device. Besides, AD9524 has jitter cleaner feature. In other words, even if the clock source of the AD9524 has noisy clock response, the noisy response is eliminated by the AD9524. Besides, AD9524 has six output port which could be programmed to different frequencies. So the proposed design will not be just a solution for spur reduction also it will be a clock distribution unit. These are the reasons why AD9524 is chosen.

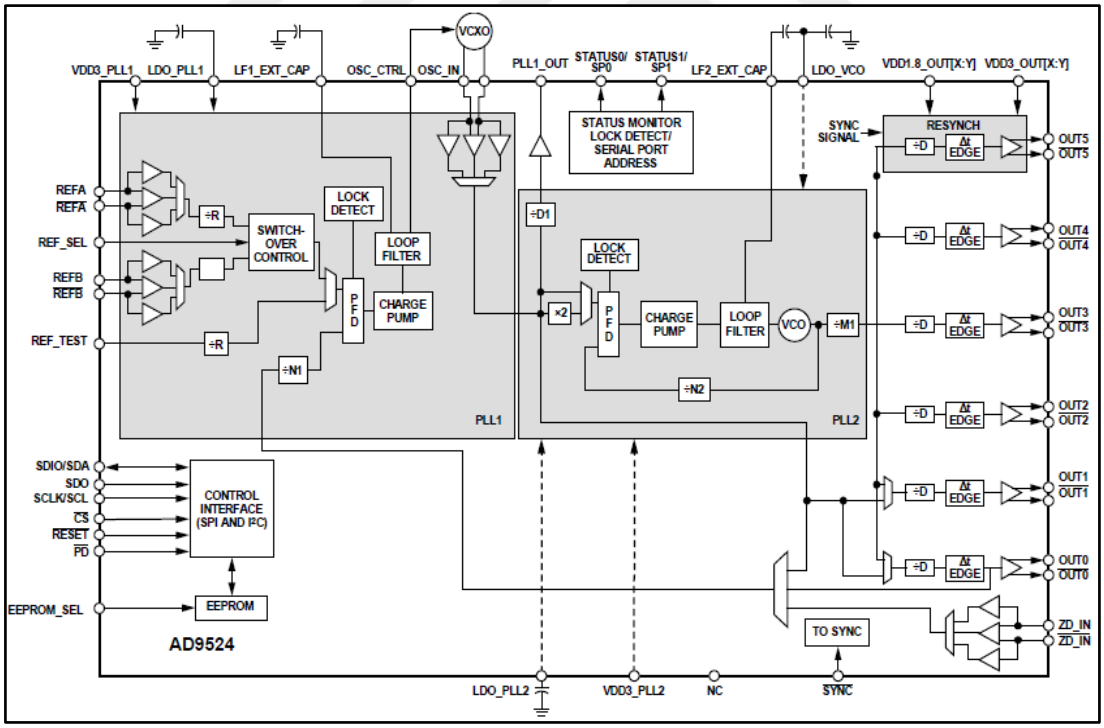


Figure 5.1. The Top-level diagram of AD9524 [37]

The device is included AD9524 is an integer-PLL device, which contains two PLL and internal VCO for second the PLL. A top-level diagram of AD9524 is given in Figure 5.1. PLL-1 is driven with an external clock source and lock to external Voltage-Controlled Crystal Oscillator (VCXO). In the proposed design, Temperature-Compensated Crystal

Oscillator (TCXO) is used for getting clean clock source at the output of AD9524. This first PLL has a very narrow loop filter for jitter clean. Therefore, AD9524 is called jitter-cleaner clock distribution device. The output of the PLL-1 in AD9524 is a clock source for PLL-2. Second PLL will be locked to internal VCO whose tuning range is between 3600-4000 MHz. Moreover, the output of the locked VCO is a source for AD9524 output channels.

The function of the first PLL output frequency could be expressed as the following equations according to Figure 5.1;

$$f_{VCXO} = \frac{f_{REF}}{R} \cdot N1 \tag{5.1}$$

Where;

$$f_{VCXO} = Voltage\ controlled\ crystal\ ossilator\ frequency$$

$$f_{REF} = Reference\ clock\ frequency$$

$$R = Reference\ divider$$

$$N1 = Feedback\ divider\ of\ PLL1$$

Moreover, the frequency of the PLL2 with integrated VCO is expressed as;

$$f_{VCO} = f_{VCXO} \cdot DX \cdot N2 \tag{5.2}$$

Where;

$$f_{VCO} = Internal\ voltage\ controlled\ ossilator\ frequency$$

$$DX = Doubler\ Value\ , 1\ or\ 2$$

$$N2 = Output\ divider\ of\ PLL2$$

Output channel frequency is given by,

$$f_{Channel} = \frac{f_{VCO}}{M1 \cdot D} \tag{5.3}$$

Where;

$$f_{Channel} = Output\ channel\ frequency$$

$$M1 = Output\ divider\ of\ PLL2$$

$$D = Channel\ divider$$

Owing to this internal VCO, AD9524 could supply necessary clocks for high-speed ADC and DAC's. In proposed, there is no ADC, but ADC has to be taken place in system design so clock necessity will occur. By taking into consideration this necessity, auxiliary outputs are included in the proposed design. Thus, all system is driven from the same source. In a sense, all clocks are synchronized. Also, there are two reference clock input ports. AD9524 can sense the presence of the clocks at inputs and switch to other input in the case of getting lost one of the clocks. The clock redundancy is provided to the proposed design by this feature. The proposed design block diagram is shown in Figure 5.2

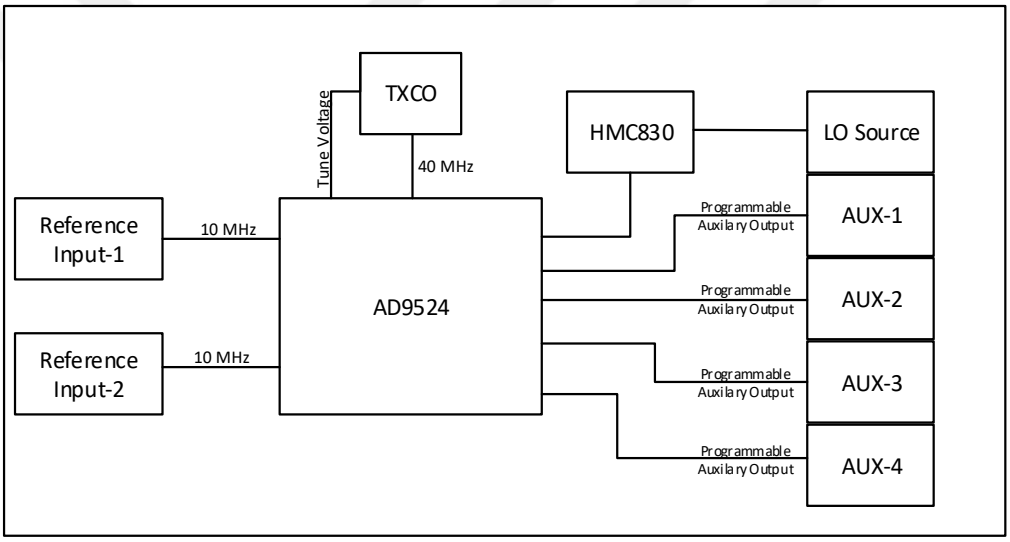


Figure 5.2. Block diagram of the synthesizer

10 MHz clock output is supplied to other equipment in most of the systems or test equipment. That is the reason why the reference clock input is assumed as 10 MHz, and all design is arranged based on this assumption however it is possible to be changed via software. TCXO's output frequency is 40 MHz, and 40 MHz clock frequency is a reference input for the second PLL. The parameters of the PLL-1 is specified according to the Equation (5.1).

$$40\ MHz = \frac{10\ MHz}{1} \cdot 4 \tag{5.4}$$

Thereby;

$$f_{VCXO} = 40\ MHz$$

$$f_{REF} = 10\ MHz$$

$$R = 1$$

$$N1 = 4$$

The locking frequency of the second PLL is chosen as 3720 MHz. So;

$$3720\ MHz = \ 40\ MHz \cdot 1 \cdot 93 \tag{5.5}$$

Thereby;

$$f_{VCO} = 3720\ MHz$$

$$f_{VCXO} = 40\ MHz$$

$$DX = 1$$

$$N2 = 93$$

The locking process only occurs at power-up. Herein, the locking times of the clock distributor are insignificant. ADISimClk is a simulation tool for Analog Devices clock distribution products. Thereby, it is used for specifying required parameters such as loop filter parameters, locking times. All proper parameters of the AD9524 are given in Table 5.1.

Table 5.1. AD9524 PLL parameters

PLL-1 Parameters		**PLL-2 Parameters**	
Reference Frequency (MHz)	10	**Reference Frequency (MHz)**	40
TCXO Frequency (MHz)	40	**VCO Frequency (MHz)**	3720
Reference (R) Divider	1	**Frequency Doubler**	Off
Feedback(N1) Divider	4	**Feedback(N2) Divider**	93
Loop filter (Hz)	30	**Loop Filter (kHz)**	450

All registers and loop parameters of the clock distributor are specified according to simulations. Required loop filters for PLL-1 and PLL-2 are located in AD9524 and

controlled via registers. Only one external component is required for the loop filter. This component is placed in the schematic design. Also, the VCO frequency is set to 3720 MHz and the channel output arranged as 50 MHz. The phase noise characteristics of the VCO and output port are given in Figure 5.3.

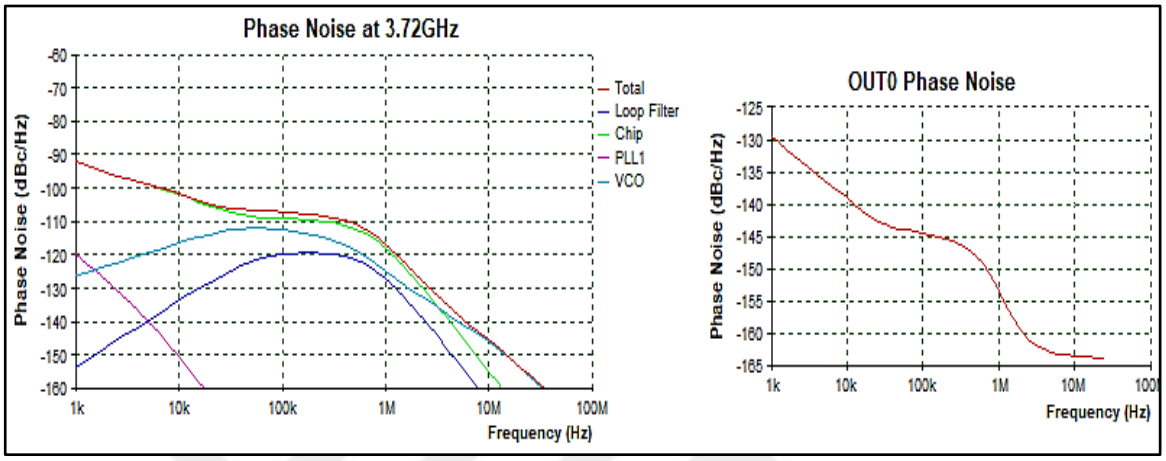


Figure 5.3. Phase noise response simulation of AD9524

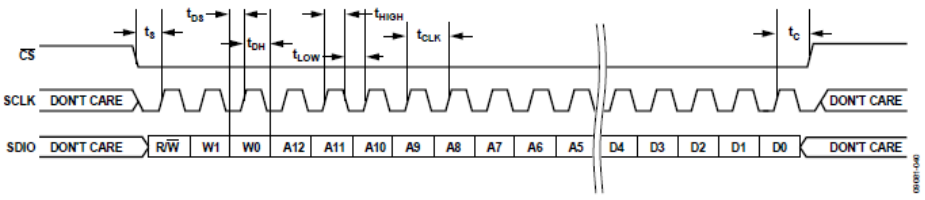
Besides common M1 divider and individual D divider for each channel have to be arranged required value for each output. Therefore, AD9524 output frequency, which is a source for HMC830, is arranged and changed for required clock frequency. M divider and D divider values are determined to approach 50 MHz. M and D values for obtaining the required frequency are given in Table 5.2 according to Equation (5.3).

The division operation is being occurred in the output section, not in PLL sections. Therefore, lock state of the PLL-1 and PLL-2 are still preserved. The elapsed time for this operation will be register update time and time for applying the changes. As mentioned before, the register data is written via the SPI interface. Therefore, SPI characteristic becomes important in Figure 5.4 shows the timing characteristic of the SPI interface.

Table 5.2. Required clock frequencies for spur reduction

Output Frequency (MHz)	**M1 (Common divider)**	**D (Channel Divider)**	**Total Divide Ratio**
58.125	4	16	64
57.23	5	13	65
53.14	5	14	70
51.666	4	18	72

SPI clock supports up to 25 MHz. However, SPI clock frequency is arranged as 10 MHz. M1 and D divider registers must be changed to attain proper divider value. 0x0F4 register. All 24 bits data, which includes data, address, and control bits, needs to be written in the register. The data is captured when the clock is rising and the period of SPI clock is 100 ns for 10 MHz. Therefore, this operation takes 2.4 us for getting access to just one register.



TIMING			
Clock Rate (SCLK, $1/t_{SCLK}$)		25	MHz
Pulse Width High, t_{HIGH}	8		ns
Pulse Width Low, t_{LOW}	12		ns
SDIO to SCLK Setup, t_{DS}	3.3		ns
SCLK to SDIO Hold, t_{DH}	0		ns
SCLK to Valid SDIO and SDO, t_{DV}		14	ns
$\overline{CS}$ to SCLK Setup, t_S	10		ns
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_C	0		ns
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	6		ns

Figure 5.4. AD9524 SPI timing details [37]

On the other hand, two different registers are reserved for the D-divider value. However, according to D-divider values in Table 5.2, the max D-divider value is 18, and it is represented by 5 bits in binary format. Registers are 8 bits so updating only one register will be sufficient. Thereby, changing D-divider register also will be taken 2.4 us. After this process, frequency changing takes only one clock cycle. However, It is negligible and total operation takes 6 us with guard time. This duration will occur at every clock frequency changes and each RF LO frequency changes. Therefore, that operation is added extra time concerning the operation that is implemented with a constant clock source. Whereas RF PLL lock duration is taken into account, duration of the clock source settling could be negligible.

Besides, the spur reduction by this method is examined via simulations. ADISim Frequency Planner software is utilized for these simulations. The design parameters of the proposed hardware are adapted to the simulation tool for getting reasonable results. Simulation parameters are shown in Figure 5.5.

In the simulation, the channel spacing is set to 100 kHz. The spurious response and phase noise simulations are conducted at each frequency from 880 MHz to 1380 MHz with 100 kHz resolution. All possible input clock frequencies, which is defined at clock generation section, is tested and compared regarding spur performance at each RF frequency. Thus, the input clock frequency, which performs best spur response at each output frequency, is obtained. The simulation result is given in Figure 5.6.

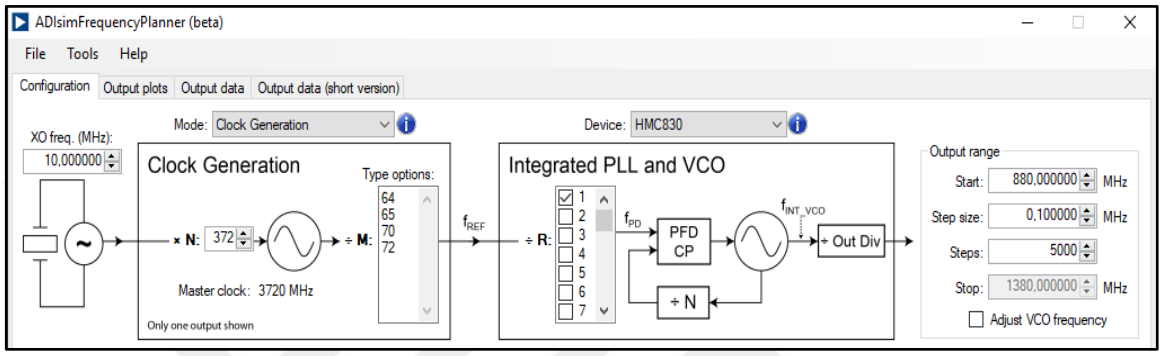


Figure 5.5. Fractional spur reduction simulation configuration

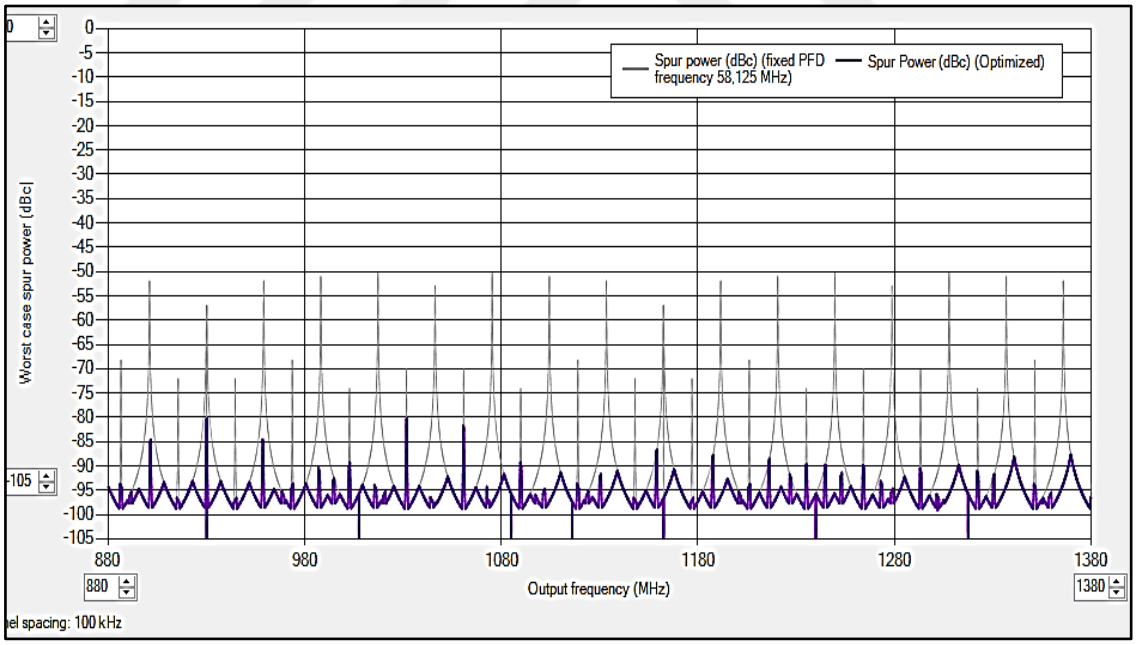


Figure 5.6. Fractional spur reduction simulation result

In simulations, the reference frequency is assumed constant as 58.125 MHz. The worst-spur response will occur at 929.9 MHz according to the simulation. The power response of the spurious signal is about -57 dBc when the reference clock frequency is 58.125 MHz. However, it will be about -80 dBc in the case of the reference clock frequency is 54.231 MHz. In other words, 23 dB spur reduction is obtained by changing reference clock

frequency. Besides, the best spur reduction will occur at 1017.2 MHz. The power response of the spur is -50.3 dBc when input reference is 58.125 MHz.

On the other hand, it will be -98.3 dBc when reference is changed to 57.231 MHz. The N-boundary spur will occur 12.5 kHz away from 1017.2 MHz when the reference clock frequency is 58.125 MHz. Thereby, it could not be filtered out by the loop filter. However, If 57.231 MHz is applied as a reference, the spur will occur 12,95 MHz away from 1017.2 MHz. Moreover, that spur is out of the pass-band region of the loop filter and filtered out. Hence, spur reduction is obtained. Mathematical proof of the operation is given in the following equations.

$$F_{Output} = 1017{,}2\ MHz$$

$$k = 2$$

VCO frequency could be found according to Equation (3.5);

$$1017{,}2 = \frac{F_{VCO}}{2} \tag{5.6}$$

$$F_{VCO} = 2034{,}4\ MHz$$

$$F_{Reference} = 58.125\ MHz$$

$$R = 1$$

According to the Equation (3.9), PFD frequency will be;

$$F_{PFD} = \frac{58{,}125}{1} = 58{,}125\ MHz \tag{5.7}$$

According to the Equation (3.8), feedback divider can be found;

$$2034{,}4 = 58{,}125 \cdot (N_{int} + N_{frac}) \tag{5.8}$$

Therefore;

$$N = 35{,}00043$$

$$N - \lfloor N \rfloor = 35{,}00043 - 35 = 0{,}00043 \tag{5.9}$$

As mentioned before, spur location could be specified according to Equation (3.20). Therefore;

$$F_{VCO} - F_{spur} = 0{,}00043 \cdot 58{,}125 = 0{,}02499375\ MHz \tag{5.10}$$

The spur will exist 24,99 kHz away from the carrier at the VCO output. But output divider (k) of the PLL is 2, so;

$$\frac{F_{VCO} - F_{spur}}{k} = \frac{0{,}02499375}{2} = 0{,}01249\ MHz \tag{5.11}$$

On the other hand, when reference frequency is changed to 57,231 MHz, then;

$$F_{PFD} = 57{,}231\ MHz$$

$$2034{,}4 = 57{,}231 \cdot (N_{int} + N_{frac}) \tag{5.12}$$

Therefore;

$$N = 35{,}5471$$

$$N - \lfloor N \rfloor = 35{,}5471 - 35 = 0{,}5471 > 0{,}5 \tag{5.13}$$

$$F_{VCO} - F_{spur} = (\lceil N \rceil - N) \cdot F_{PFD} = (36 - 35{,}5471) \cdot 57{,}231 \tag{5.14}$$

$$F_{VCO} - F_{spur} = 0{,}4529 \cdot 57{,}231 = 25{,}9199\ MHz \tag{5.15}$$

The spur will exist 25,9199 MHz away from the carrier at the VCO output. But output divider (k) of the PLL is 2, then;

$$\frac{F_{VCO} - F_{spur}}{k} = \frac{25{,}9199\ MHz}{2} = 12{,}95\ MHz \tag{5.16}$$

Spur location is moved from about 12 kHz to 13 MHz. Therefore, loop-filter will remove the spurious response of the PLL.

HMC830 is used for feeding mixers LO port as a synthesizer and simulation of HMC830 is realized with ADISIMPLL simulation tool for Analog Devices PLLs. The internal PLL of HMC830 is locked by using internal VCO. The internal VCO could be set between 1500-3000 MHz. Also, the output frequency of HMC830 could be between 25-3000 MHz due to output clock divider. So in this application, LO source needs to be between 880 MHz and

1380 MHz. That is the reason why VCO of HMC830 needs to be arranged from 1760 MHz to 2760 MHz. Also, the output clock divider ratio needs to be two. Thus, intended frequencies could be obtained by this methodology.

2000 MHz is analyzed in simulations because of the applied VCO frequency range. Locking time is investigated in simulations. Frequency changing speed is defined by lock duration of the PLL. Indeed, System speed is also defined. The locking duration at 2 GHz is approximately 150 us when absolute frequency error is under 1 Hz. Hence, sub-Hz grade accuracy is attained. The time simulation result is given in Figure 5.7.

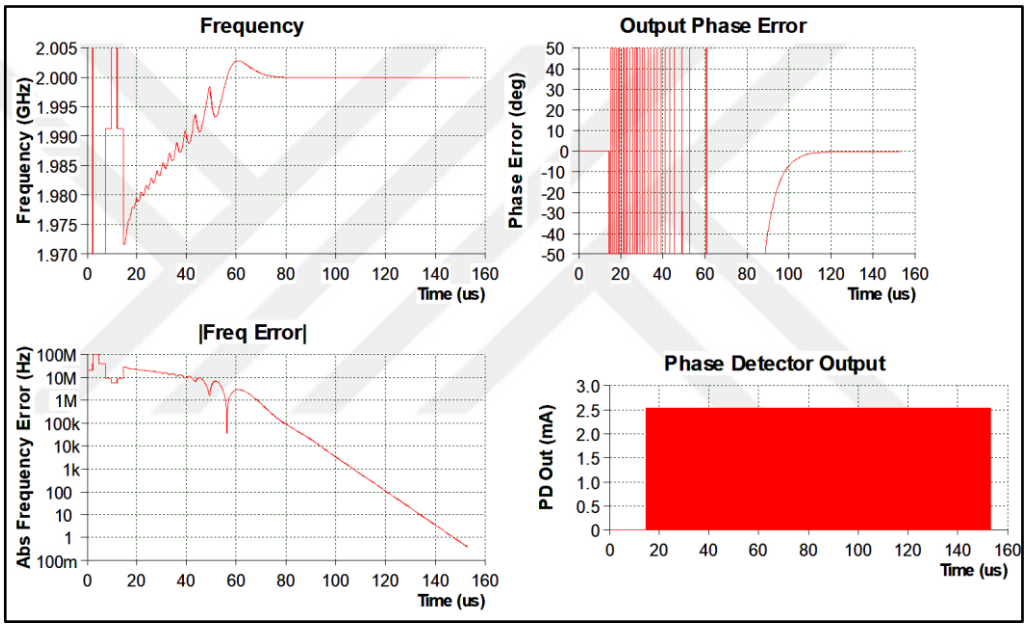


Figure 5.7. PLL time simulations

Moreover, locking duration directly related with loop filter bandwidth. Shortly this relation represents in Equation (5.1).

$$\text{Traditional Analog Lock time} \sim = \ 4 \ / \ \text{LBW} \tag{5.17}$$

Where;

$$\text{LBW} = \text{Loop} - \text{filter Bandwidth}$$

The loop filter is arranged as 45 kHz in the proposed design simulations. According to Equation (5.1), it will be taken approximately 90 us. On the other hand, HMC830 includes a step tuned VCO. Thus, the wide-band frequency response is obtained. A step tuned VCO includes a digitally selectable capacitor bank allowing the nominal center frequency of the

VCO to be adjusted or stepped by switching in and out of the VCO tank capacitors. Therefore, The auto-calibration feature is involved in finding the optimum capacitor in VCO with respect to the output frequency. This process also takes extra time because of the auto-calibration process. As a result, the locking duration takes much longer time than calculated in Equation (5.1). On the other hand, the auto-calibration feature could be deactivated. If auto-calibration is deactivated, all frequencies must be measured previously. The measurement must be conducted in auto-calibration mode and identified which VCO tank is used with respect to the output frequency. The VCO tank information is saved in a LUT. In the real-time application, the auto-calibration process is deactivated, and proper VCO tank capacitor information needs to be written to relevant register at every frequency change. Thus, the auto-calibration process time is eliminated, and locking duration will be shortened. Furthermore, increasing loop filter bandwidth could be shortened lock durations. More integer-boundary spurs will exist in loop filter passband region in the case of increasing loop filter bandwidth. However, the proposed integer-boundary spur rejection method will be canceled out the spurs. The VCO output phase noise characteristic will be affected by increasing loop filter bandwidth. There is a trade-off between phase noise and locking speed. Therefore, this topic needs to be taken into account. 45 kHz loop bandwidth will be sufficient for most systems. Thus, the configuration of the loop filter for 45 kHz is given in Figure 5.8.

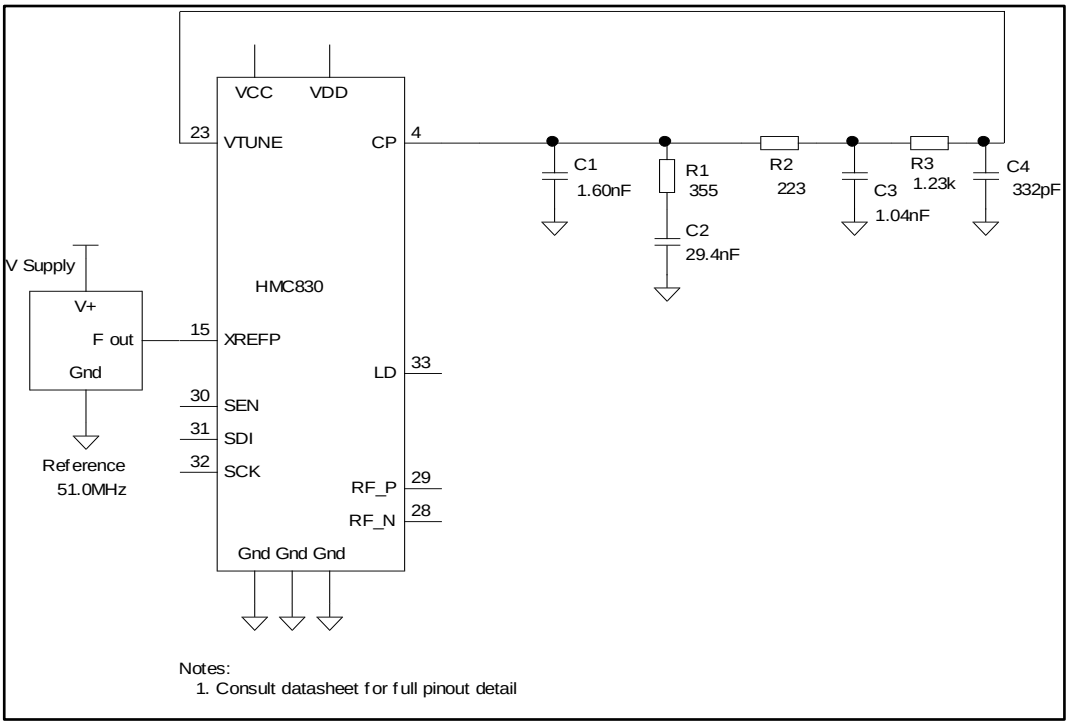


Figure 5.8. Loop filter parameters according to simulation

Parameters that are obtained from simulations are transferred to schematic design. After the schematic design, layout design is completed by specifications that mentioned in 4.2. Stack-up is same as down-converter design's stack-up. Hardware schematic and layout design details are given in APPENDIX C, and APPENDIX D. 3D view of designed hardware is given in Figure 5.9 [37-41].

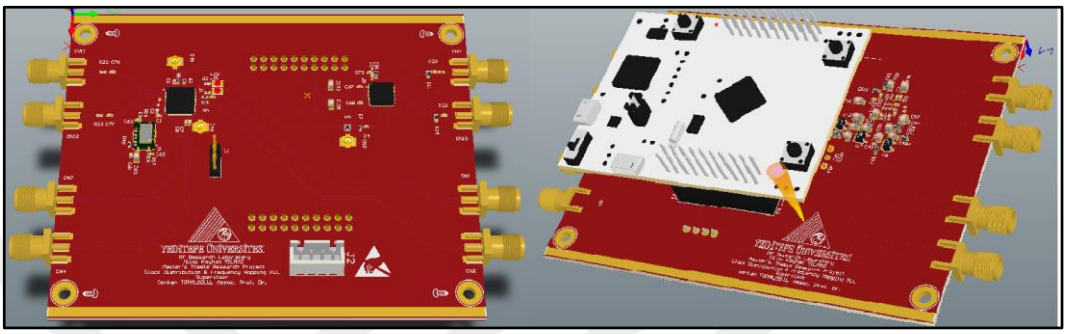


Figure 5.9. 3D view of designed hardware

5.2. IMPLEMENTATION AND TESTS

The post-production images of the proposed design are in Figure 5.10 and Figure 5.11. After evaluating necessary board bring-up tests, both AD9524 and HMC830 is programmed via SPI buses.

In order to evaluate simulation results, the output frequency of AD9524 is set to 50 MHz because the simulations are conducted at 50 MHz. Measurement of the spectrum and phase noise results at 50 MHz is given in Figure 5.12.

After this test, HMC830 output response is investigated. The simulations of HMC830 are conducted at 2000 MHz. That is the reason why HMC830 output response is investigated at 2000 MHz. Figure 5.13 shows the spectral and phase response of HMC830. When simulation and test results are compared in terms of phase noise, measurement results are corroborated by the simulation results.

The comparison of measurement and simulation results in terms of phase noise is given in Table 5.3. Simulation and measurement results are nearly the same. The phase noise response of a receiver is defined by some of the telecommunication standards such as International Telecommunication Union standards (ITU) and Intelsat Earth Station

Standards (IESS) IESS-309. Furthermore, when these results are compared with these standards, minimum requirements are met by the proposed design bountifully. In other words, the proposed design is compatible with ITU and IESS standards.

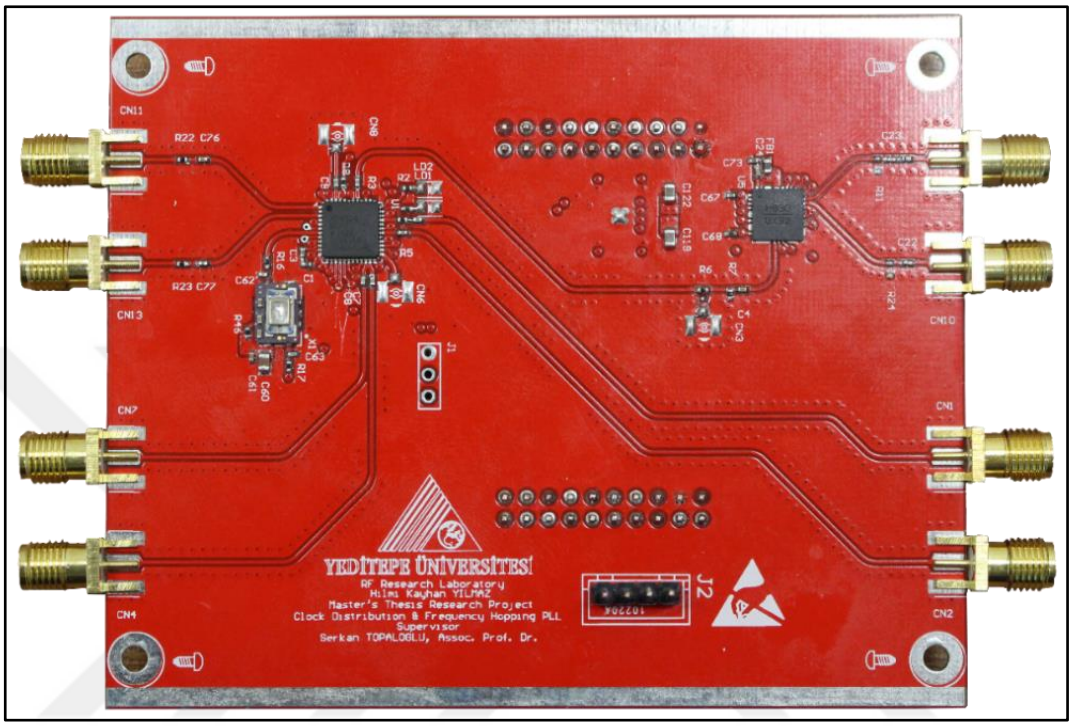


Figure 5.10. Top view of the manufactured synthesizer

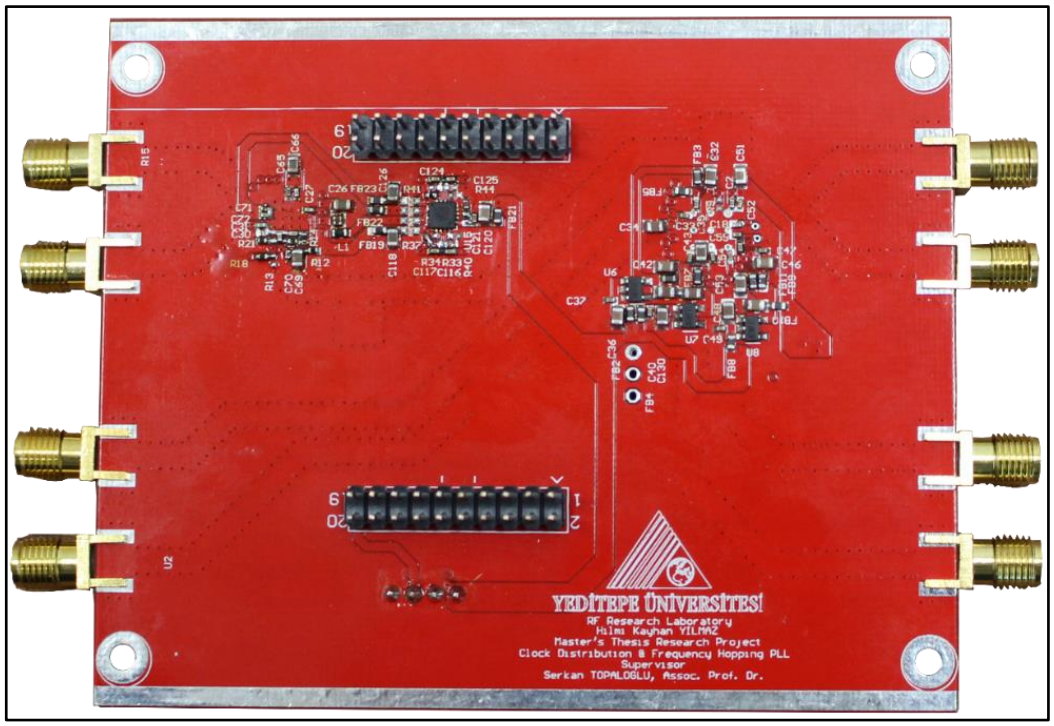


Figure 5.11. Bottom view of the manufactured synthesizer

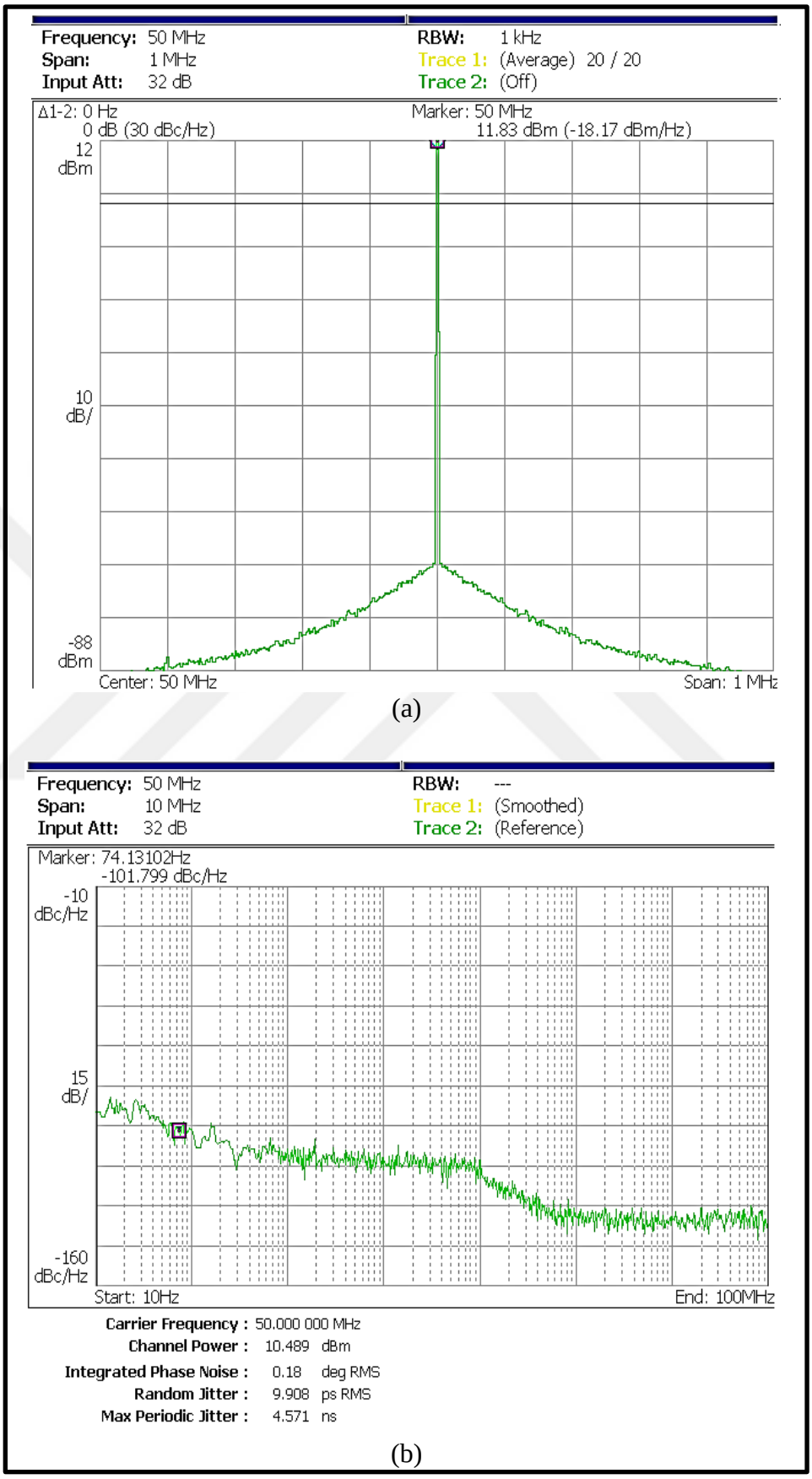


Figure 5.12. AD9524 measurements at 50 MHz. (a) Spectral view, (b) Phase noise

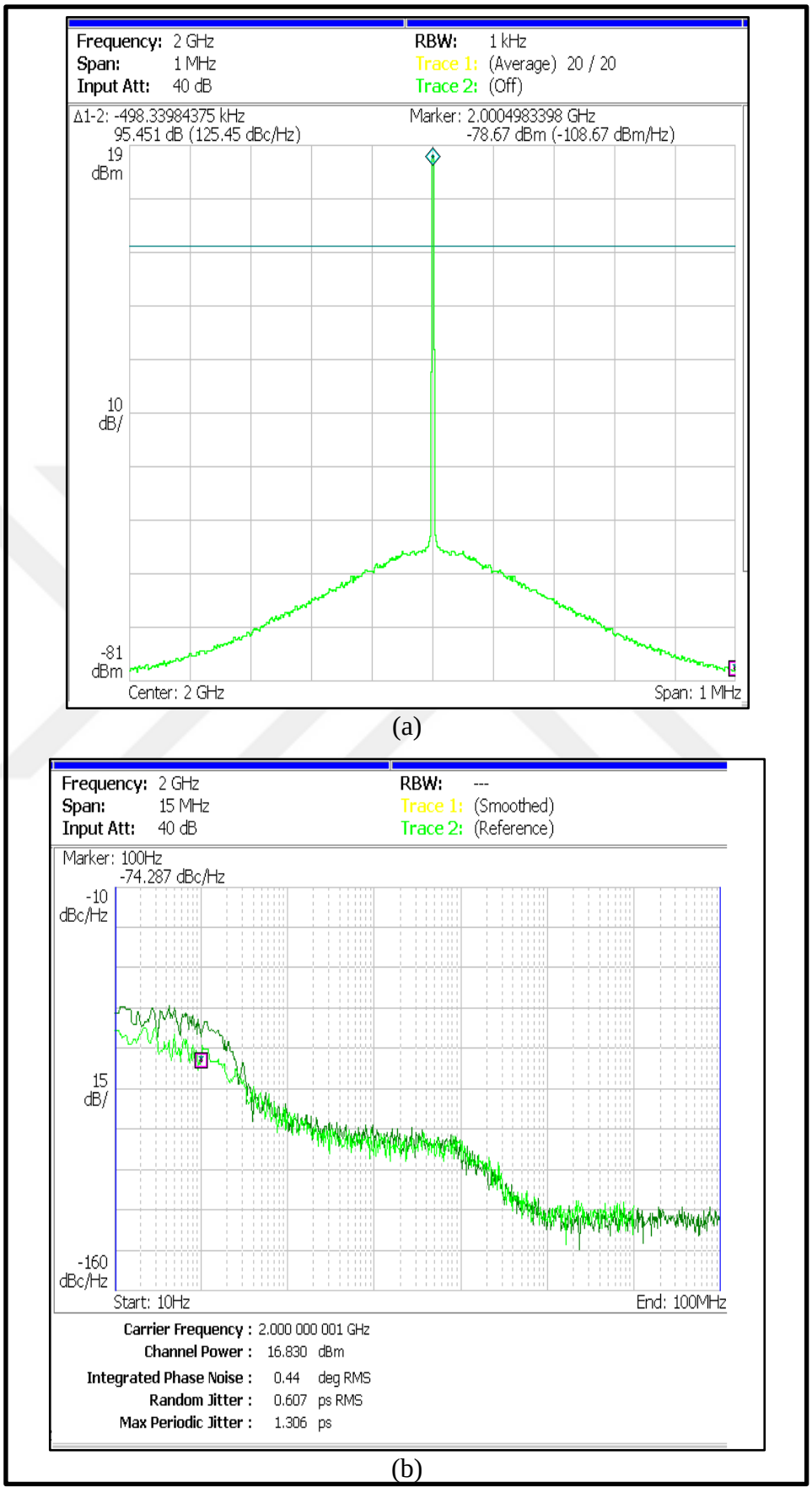


Figure 5.13. HMC830 measurements at 2 GHz. (a) Spectral view, (b) Phase noise

Table 5.3. Phase noise comparison with simulation and telecommunication standards

Offset from the carrier (kHz)	**Simulation (dBc/Hz)**	**Measurement (dBc/Hz)**	**International Telecommunication Union Standards(ITU) (dBc/Hz)**	**Intelsat Earth Station Standards (IESS) IESS-309 (dBc/Hz)**
0.1	-78	-74	-	<-60
1	-97	-95	-	-
10	-104.4	-102	<-90	-
100	-112.0	-111	-	<-90
1000	-141.2	-132	-	-

Furthermore, the lock duration of HMC830, which is vital for FHSS, is measured by signal source analyzer feature of the spectrum analyzer. The bandwidth capability of the spectrum analyzer is limited thereby frequency locking length is observed under 10 kHz frequency change condition. The frequency locking duration measurement is shown in Figure 5.14. the locking duration is measured as 180 us. In the simulation, this value is declared as 150 us. The measured data is very close to the simulation results. In other respect, the implementation period of the spur reduction method takes 6 us as stated before. 6 us extra time must be added to the locking duration of RF PLL. Hence, the total locking duration takes 186 us. This duration is assumed as 200 us to be on the safe side. In brief, the proposed design is suitable for FHSS systems which is tolerant to at least 200 us guard time between frequency changes.

According to the simulations, the best performance of the spurious reduction method occurs at 1017.2 MHz.The spurious reduction method is applied and measured at 1017.2 MHz to investigate this case. The power response of the spurious product is about -57 dBc when 57.125 MHz is applied to the clock input of the HMC830 as a source. In the measurement, the same conditions are applied to the proposed design. The power response of the spurious signals is also about -57 dBc. RF PLL output response at test conditions is shown in Figure 5.15.

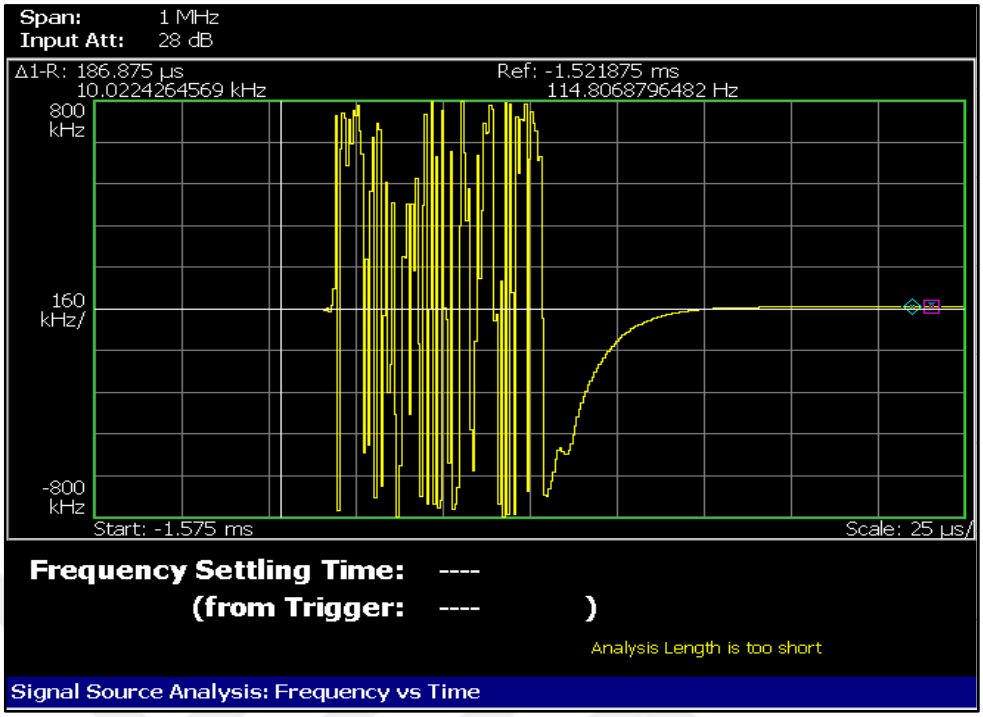


Figure 5.14. Locking time measurement of HMC830

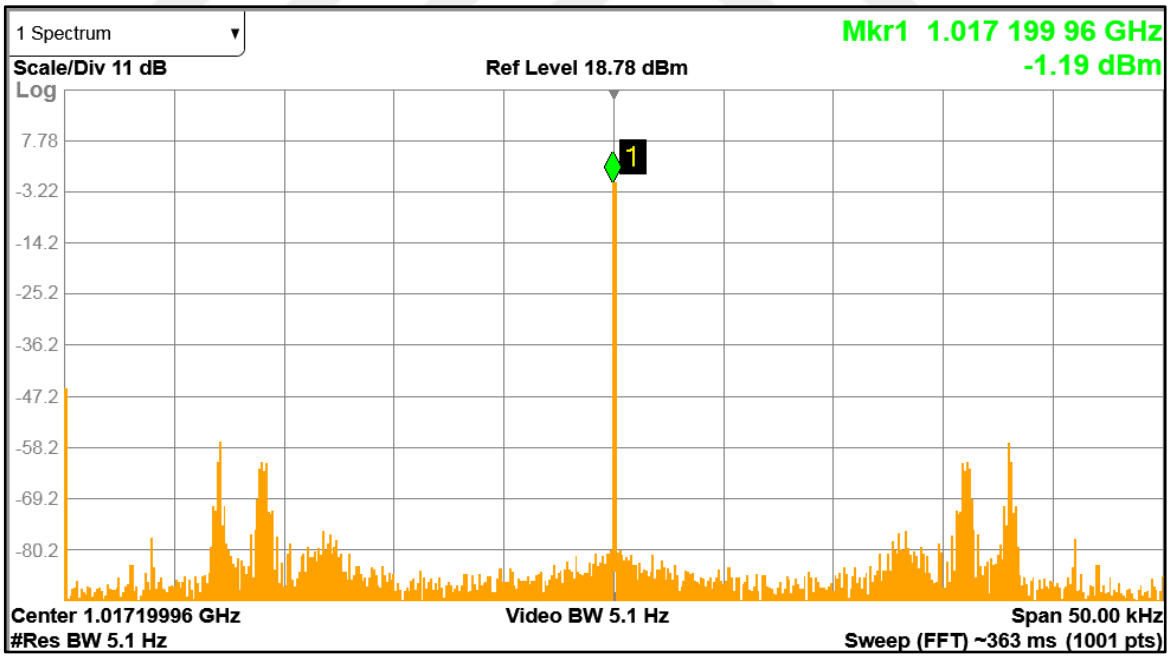


Figure 5.15. Spectral view of RF PLL output with the spurious response

As mentioned before, fractional will be changed therefore the location of the spurious signal in the spectrum will be shifted. This situation will happen when the reference clock frequency is changed from 57.125 MHz to 58.125 MHz. RF PLL output response is shown in Figure 5.16 if the reference clock frequency is 58.125 MHz.

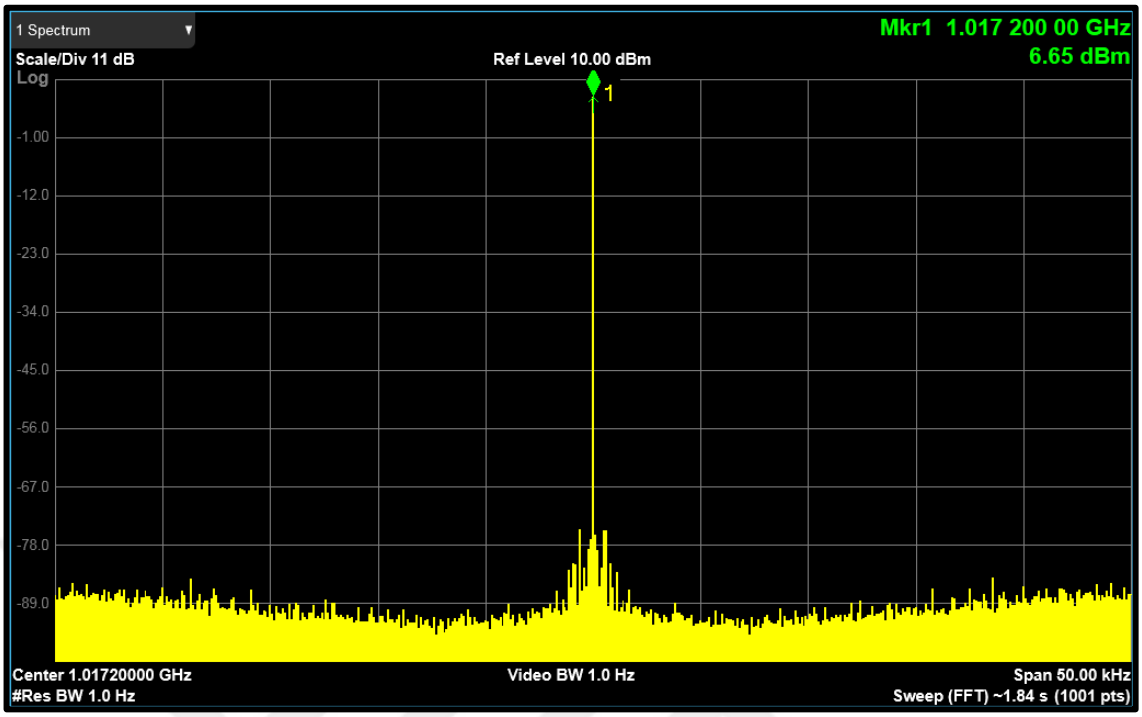


Figure 5.16. The spurious-free response of RF PLL's output

There are no spurious products in the spectrum within the same span. Besides, the noise level is around 97 dB below the carrier. A 40 dB spur reduction is obtained at 1017.2 MHz by using the tunable frequency method. In a real application, optimum clock reference frequency in terms of spurious response need to be applied for each RF Frequency. Therefore, the spurious-free response of the synthesizer will be obtained at each desired RF frequency. Thus, performance degradation of both receiver and transmitter will be eliminated.

6. CONCLUSION

In this thesis study, a tunable compensation method was presented for amplitude errors on Hartley image rejection topology. Amplitude errors, which exist between in-phase and quadrature section of the Hartley image reject topology, were eliminated. The insertion loss of the both in-phase and quadrature path was specified by simulations. The DC voltage was applied to the mixer located in the section that has less insertion loss characteristic. Therefore, insertion loss of the mixer and the section that the mixer located was increased. Thus insertion loss of the in-phase and quadrature section approached, and amplitude error was eliminated by applying DC voltage to the mixer. The improvement of image rejection ratio was achieved for Hartley image rejection receivers. The tunable amplitude compensation method was proven by measurement results. Improvement of image rejection ratios was obtained up to 36 dB by applying proposed tunable amplitude compensation method. In addition to this method, a non-tunable phase compensation method was applied to the proposed design by delayed trace method. Best image rejection ratio was measured as 77 dB, and this value was achieved by both the amplitude and phase compensation method. The most of the receivers use double-IF super-heterodyne topology, heterodyne topology with filter bank or image reject topology with filter bank to achieve these image rejection values. Enhanced results of the proposed design lead on previous studies about image reject mixer even if most of these studies have narrow-band response [42-45] Moreover, also there are some image-reject mixers in the market. These mixers work at different frequencies but use the same Hartley image rejection topology as proposed in this thesis study. However, these images reject mixers have poor image rejection values that are not enough to use in a receiver design without a proper filter bank. Table 6.1 shows a comparison between Mini-circuits image-reject mixer (JCIR-152H+) and thesis study which proposed method is applied [46,47].

In addition to the proposed method for improvement of image rejection ratios, spur reduction method was presented for fractional-PLL based frequency synthesizers. The proposed spur reduction method was based on tuning reference clock frequencies. The spur locations were specified by PFD frequency and feedback divider value. The same output LO frequencies were formed by different PFD frequency and different feedback divider. Therefore, PFD frequency was changed, and spur locations were shifted to the out-of-band region of the

loop-filter. In the proposed method, different PFD frequencies and feedback divider ratios were achieved by changing reference clock frequencies which were supplied by PLL based clock generator. The proposed method was proved by both simulations and measurement results. Up to 40 dB spur reduction is obtained by using the proposed method. Besides, the proposed design performs outstanding performance was compared with previous works and products in terms of spur reduction and phase noise. Comparison tables are given in Table 6.3 and Table 6.2. Besides, the convenience of proposed spur reduction method was proved by lock-up times measurements for Fast Frequency Hopping Spread Spectrum. The proposed synthesizer design is suitable for FHSS which has 200 us guard time.

Table 6.1. Comparison between the proposed design and JCIR-152H+

Proposed Design			**JCIR-152H+ [46] [47]**		
Fundamental Frequency (MHz)	**LO Frequency (MHz)**	**Image rejection (dB)**	**Fundamental Frequency (MHz)**	**LO Frequency (MHz)**	**Image rejection (dB)**
1100	1030	26,71	1000	1080	31,63
1125	1055	33,6	1040	1120	43,89
1150	1080	44,52	1080	1160	32,63
1175	1105	51,77	1120	1200	38,31
1200	1130	77,04	1160	1240	40,17
1225	1155	63,43	1200	1280	38,31
1250	1180	53,63	1240	1320	31,82
1275	1205	51,99	1280	1360	34,28
1300	1230	41,6	1320	1400	41,52
1325	1255	65,19	1360	1440	50,03
1350	1280	59,96	1400	1480	32,64
1375	1305	47,02	1420	1500	30,99
1400	1330	46,96	1430	1510	29,60
1425	1355	46,38	1440	1520	28,66
1450	1450	46,2	1450	1530,00	27,42

This study offers solutions for both downconverter image signal problem and spurious response of synthesizer. The proposed methods are asserted regarding simulations and are

proven by implementations and measurements.

Table 6.2. Comparison with some receivers

		This work	NewTech FRC0720 [23]	ComTech LBC-4000 [24]	Novella Satcoms D350 [25]
Input Frequency (MHz)		950 to 1450	950 to 2150	950 to 2000	950 to 1750
IF Frequency (MHz)		70	70	70	70
Phase Noise (dBc/Hz)	**10 Hz**	-65	<-50	-	-60
	100 Hz	-74	<-70	-78	-75
	1 kHz	-95	<-80	-79	-80
	10 kHz	-102	<-85	-90	-85
	100 kHz	-111	<-95	-113	-95
	1 MHz	-132	-	-129	-110

Table 6.3. Comparison with prior works

	[48]	[49]	[50]	This work
Type	IC	IC	IC	Discrete
Supply (VDC)	1.8	2.5	2.5	3.3
Power (mW)	20	18	13.5	1500
Freq. (GHz)	2.5- 2.7	4.8/2.4	5.14-5.7	0.025 -3
Phase Noise @1MHz	-105	-104 / -110	-116	-132
Spur Reduction (dB)	20	10	20	40

On the other hand, phase and amplitude response of the components will be affected by some other effects such as temperature. Especially, non-tunable phase compensation method will be dummy and ineffective. Therefore, the image rejection values will change according to the temperature. Eliminating temperature effect on Hartley image reject receiver, non-tunable phase compensation method should be replaced with tunable phase compensation method. Phase tunability could be achieved by varactor diodes. Independently from

temperature effects, the obtained results by applying tunable amplitude compensation methods could be enhanced by adding tunable phase compensation. Filter bank necessity will be removed entirely by both applying tunable amplitude and phase compensation. On the other hand, there are differences in the characterization of the downconverter due to components manufacturing. The calibration requirement of the downconverter was not taken into account within the thesis scope. A self-calibration part should be incorporated into the proposed design [51, 52].

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APPENDIX A: SCHEMATIC DESIGN OF THE RECEIVER

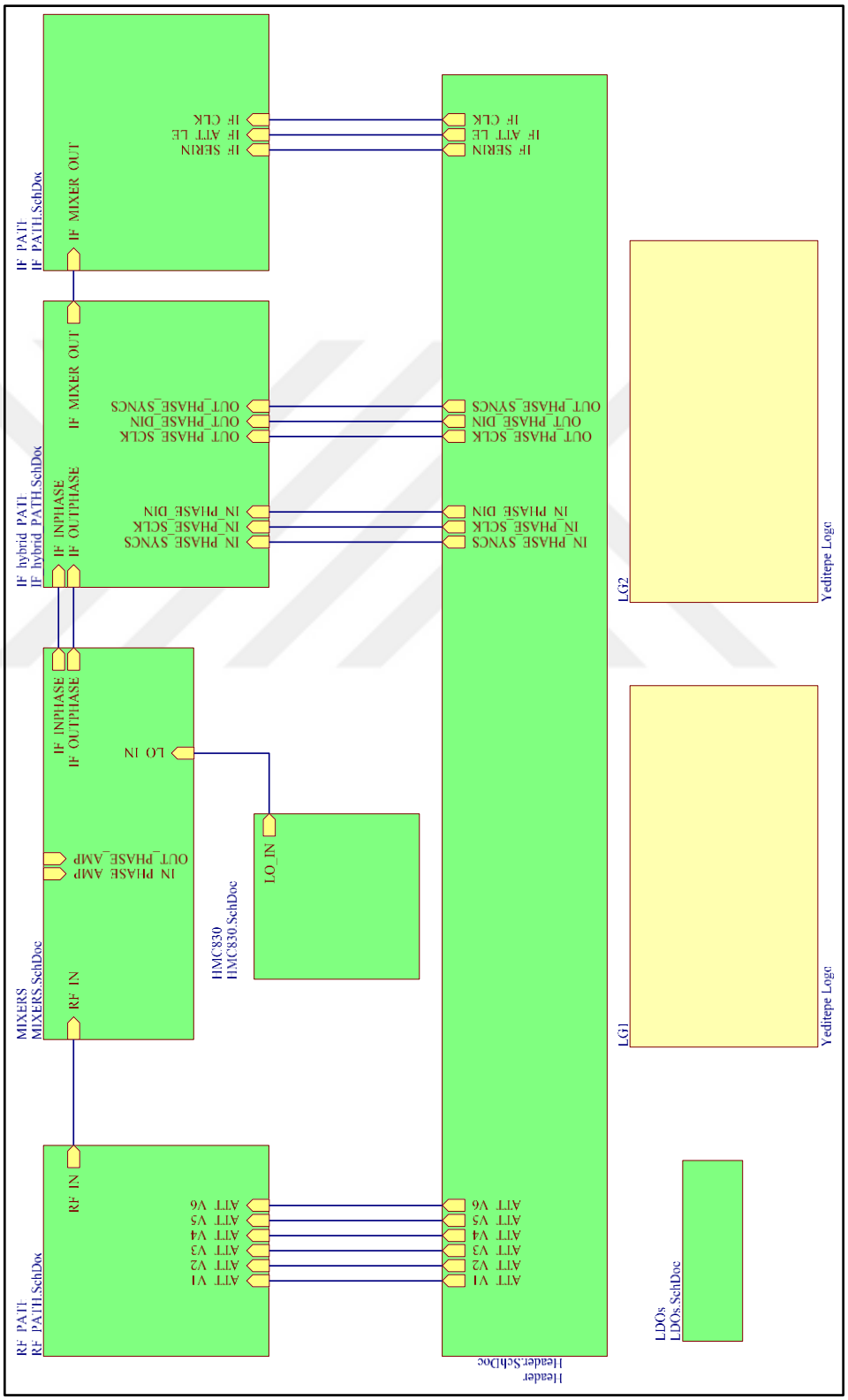

Figure A.1. Top level schematic of the receiver design

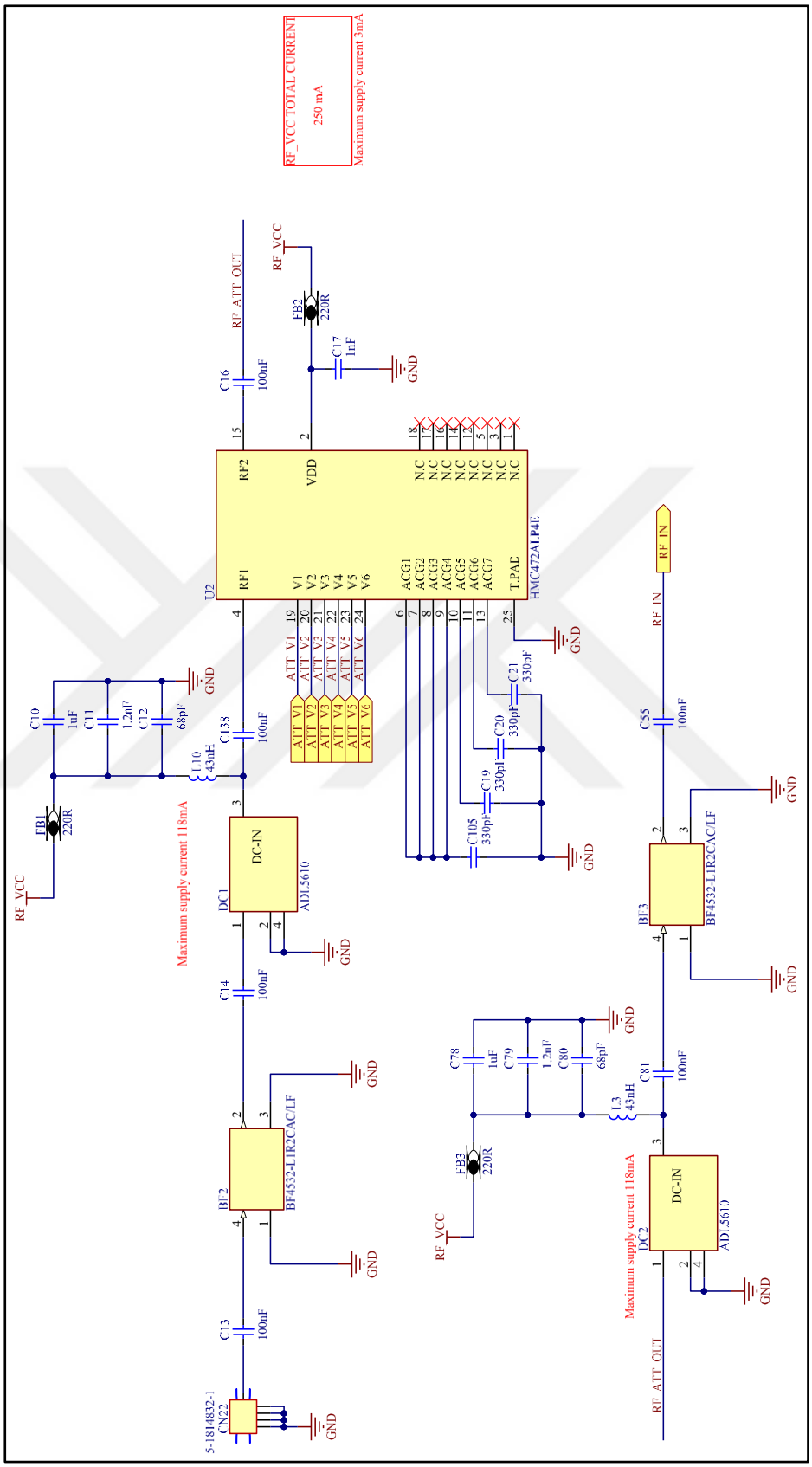

Figure A.2. RF front-end schematic of the receiver design

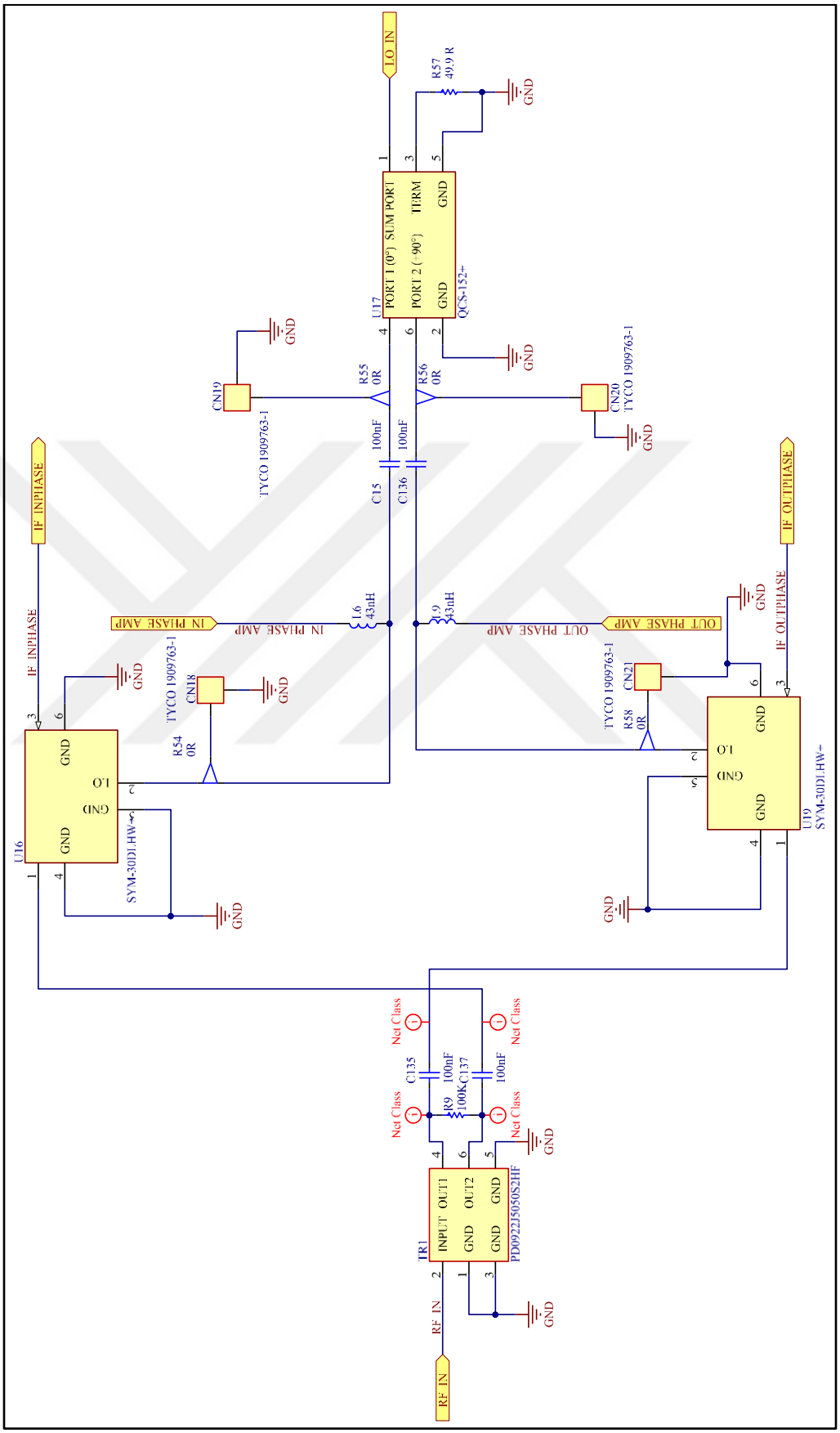

Figure A.3. Mixer block of the receiver design

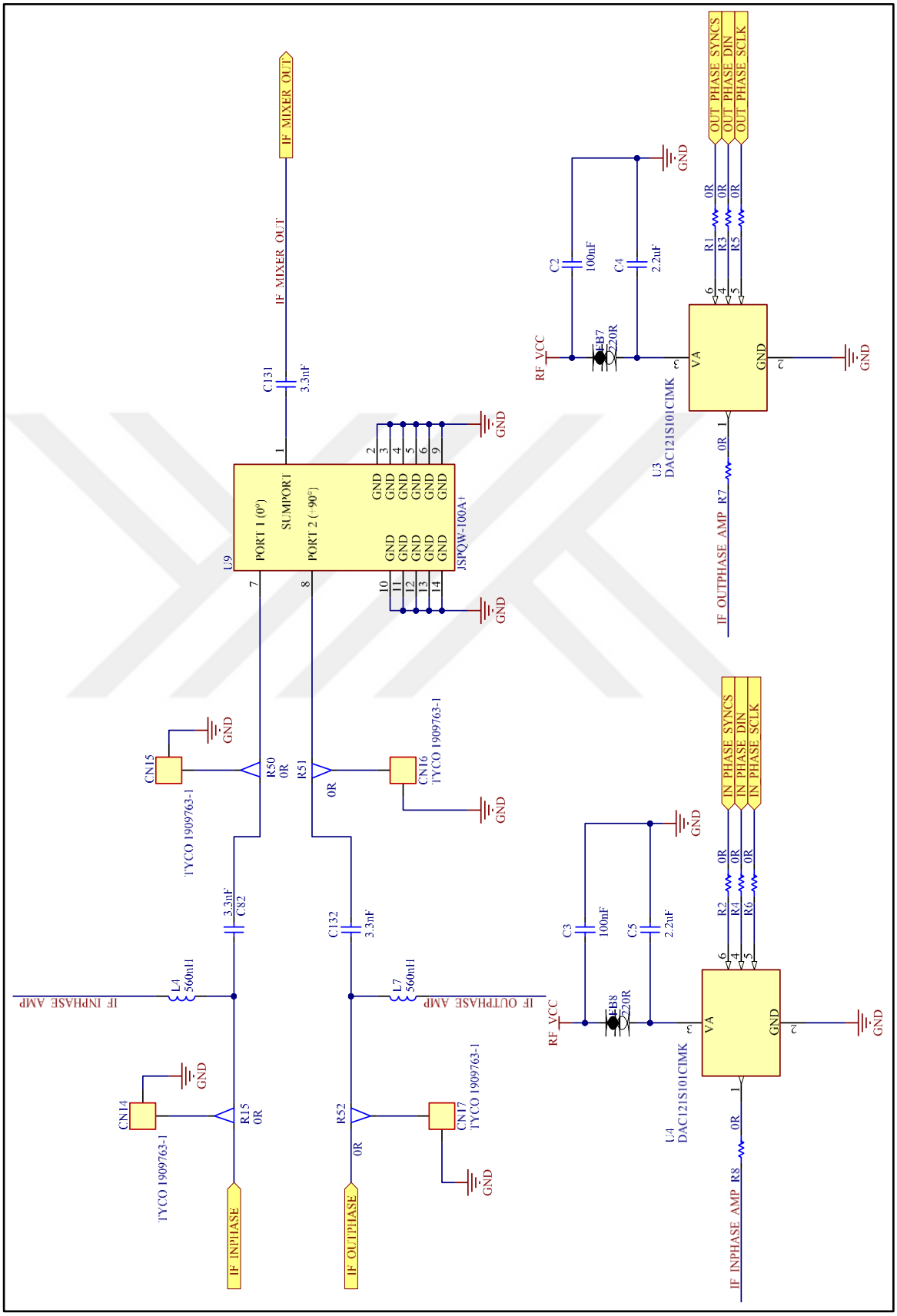

Figure A.4. Amplitude control stage of the receiver design

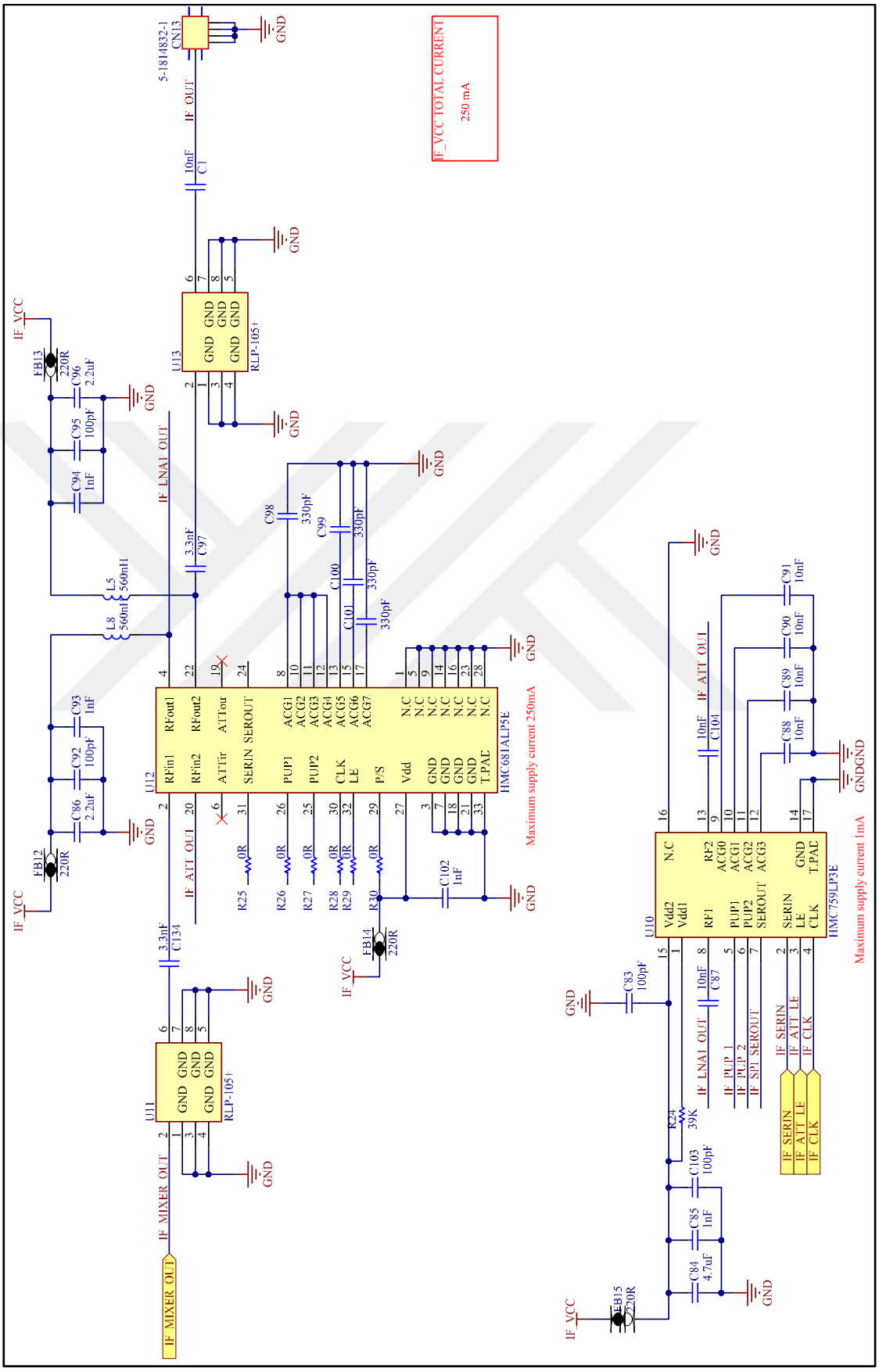

Figure A.5. IF stage of the receiver design

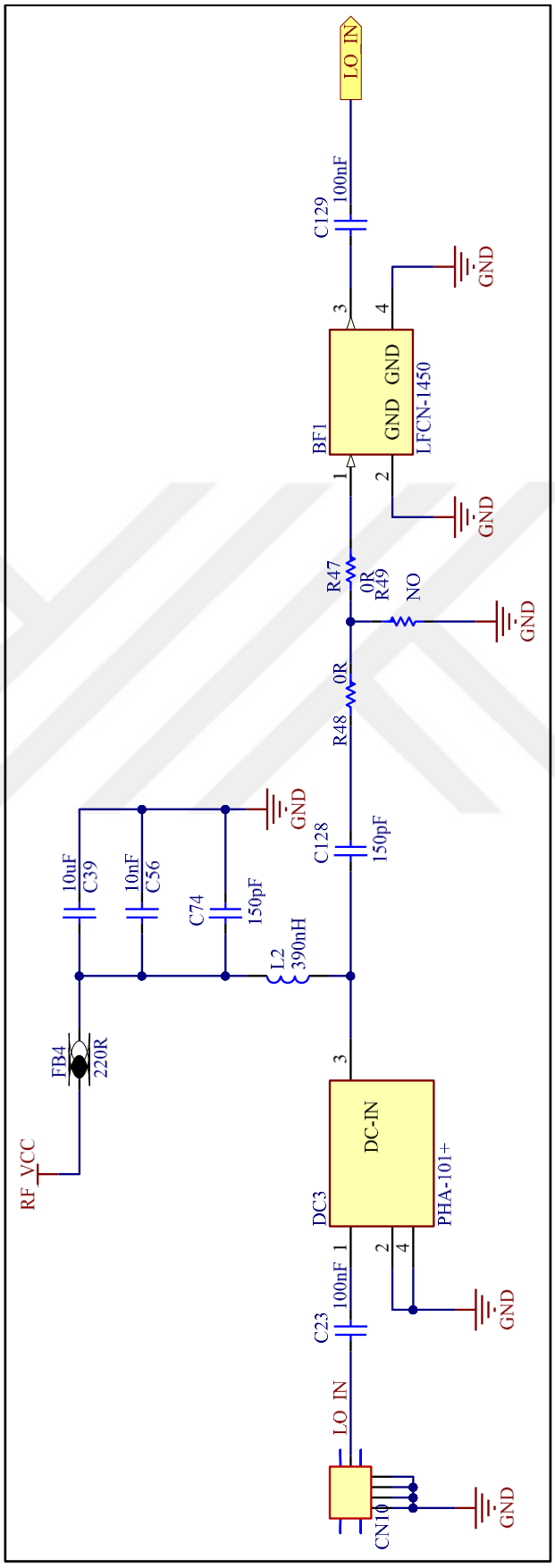

Figure A.6. LO block of the receiver design

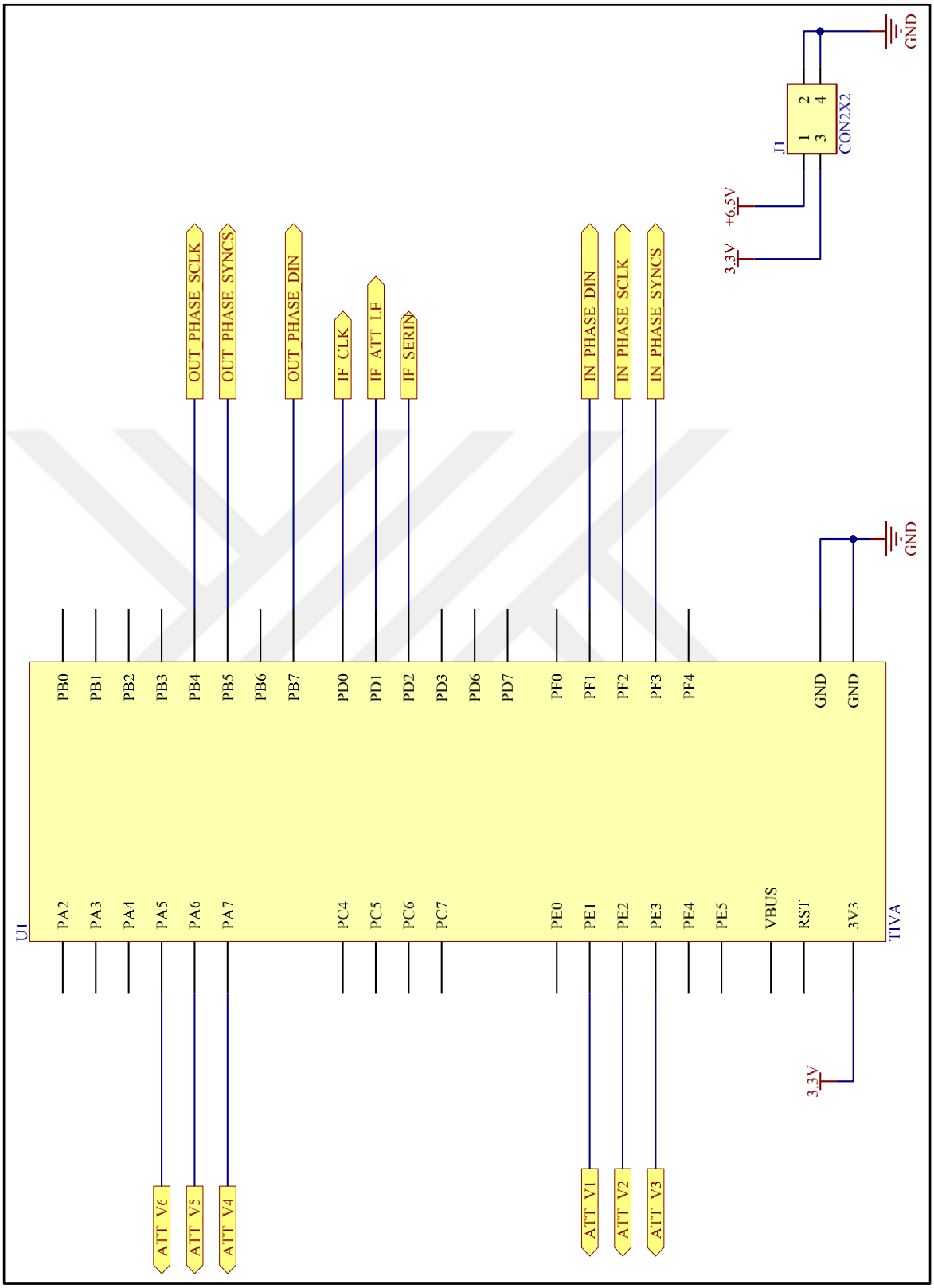

Figure A.7. TIVA connection schematic

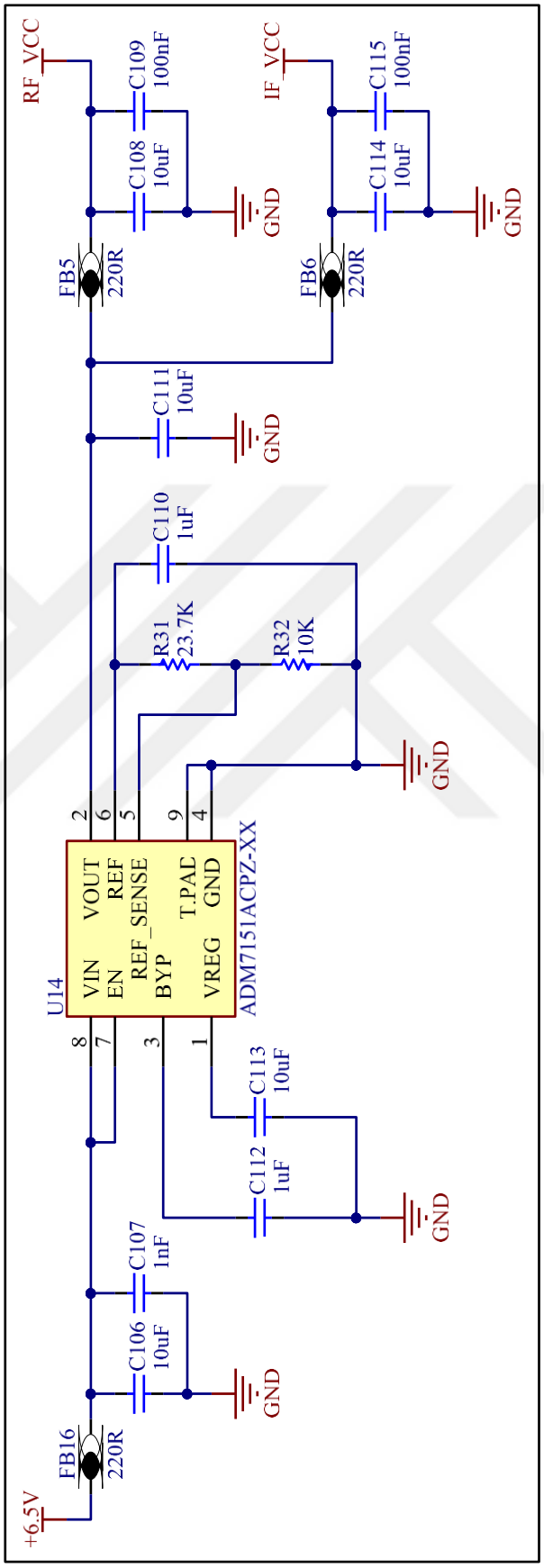

Figure A.8. LDO block of the receiver

APPENDIX B: LAYOUT DESIGN OF THE RECEIVER

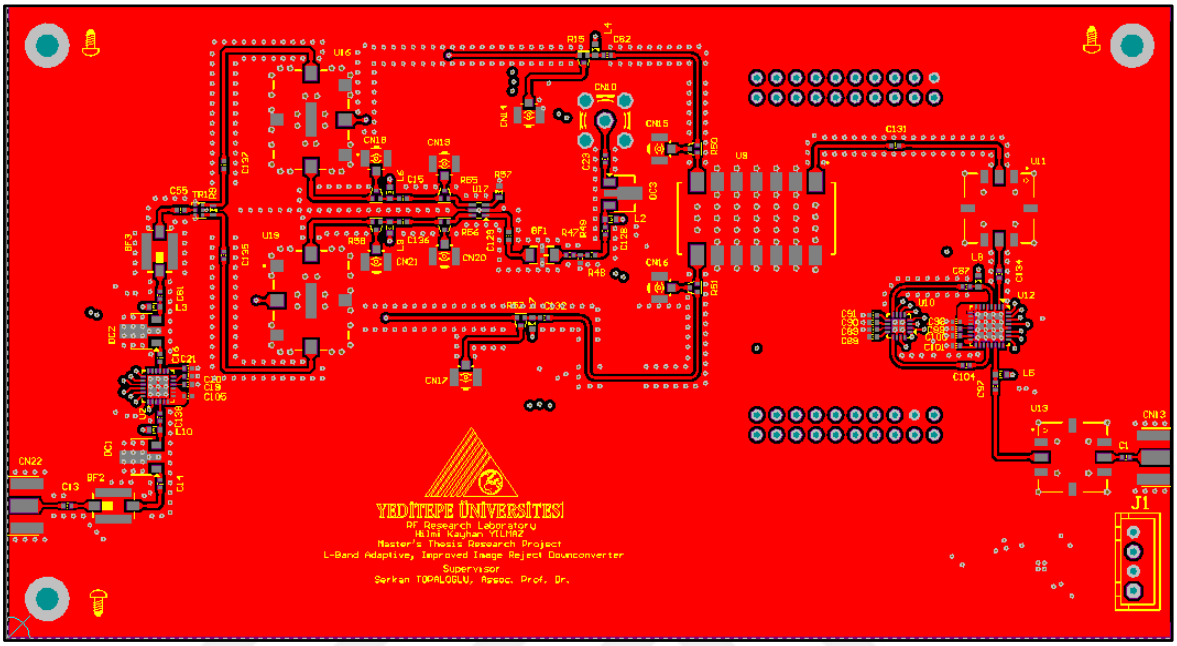

Figure B.1. The top layer of the receiver design

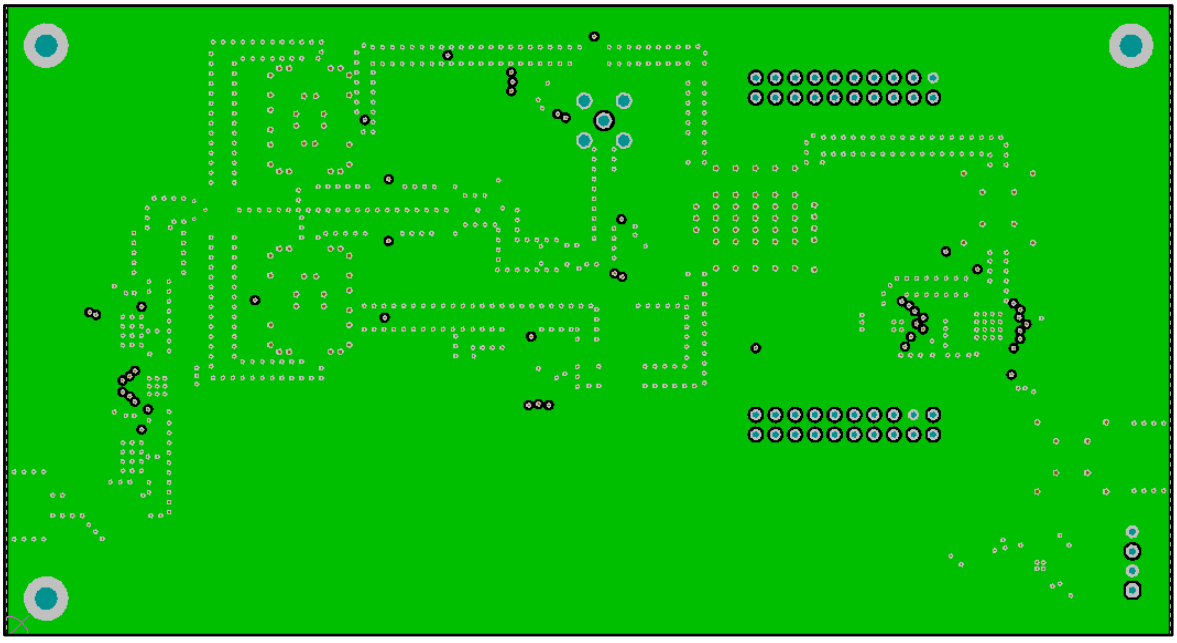

Figure B.2. The second layer (Ground layer) of the receiver design

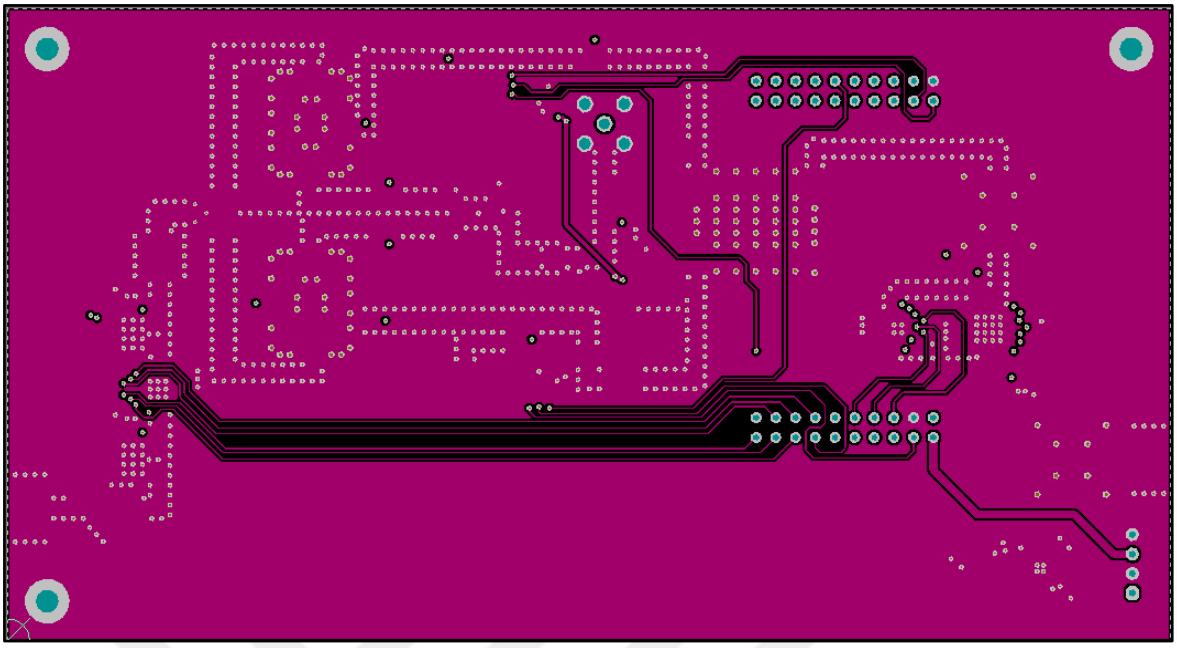

Figure B.3. The third layer (Signal Layer) of the receiver design

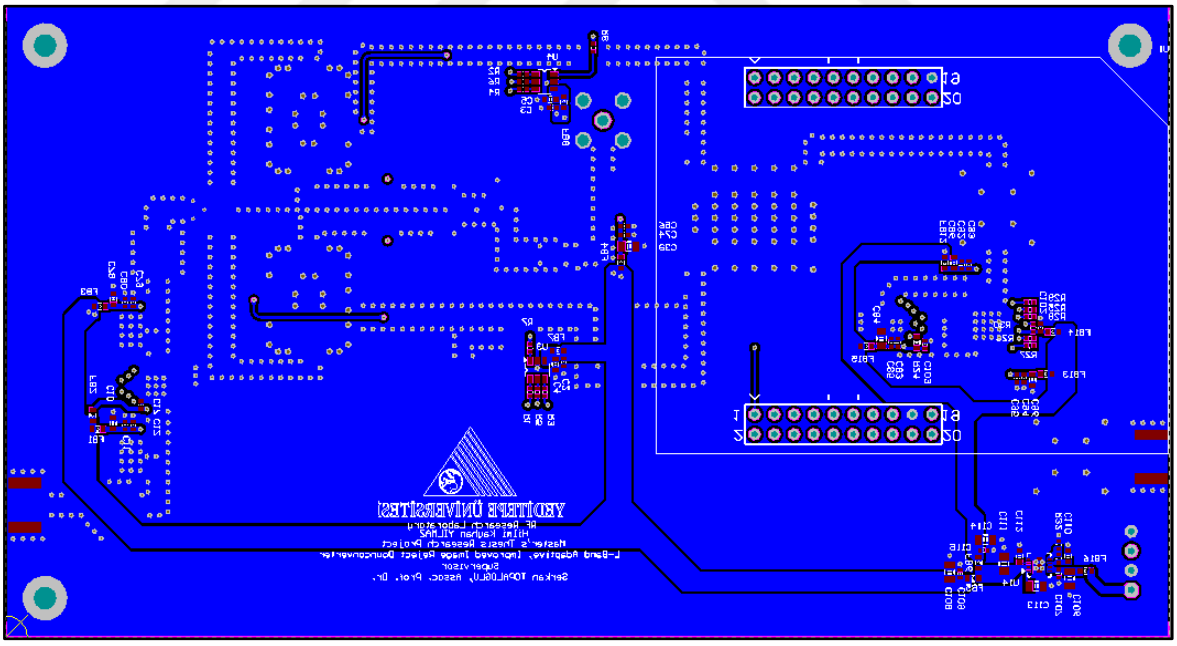

Figure B.4. The bottom layer of the receiver design

APPENDIX C: SCHEMATIC DESIGN OF THE SYNTHESIZER

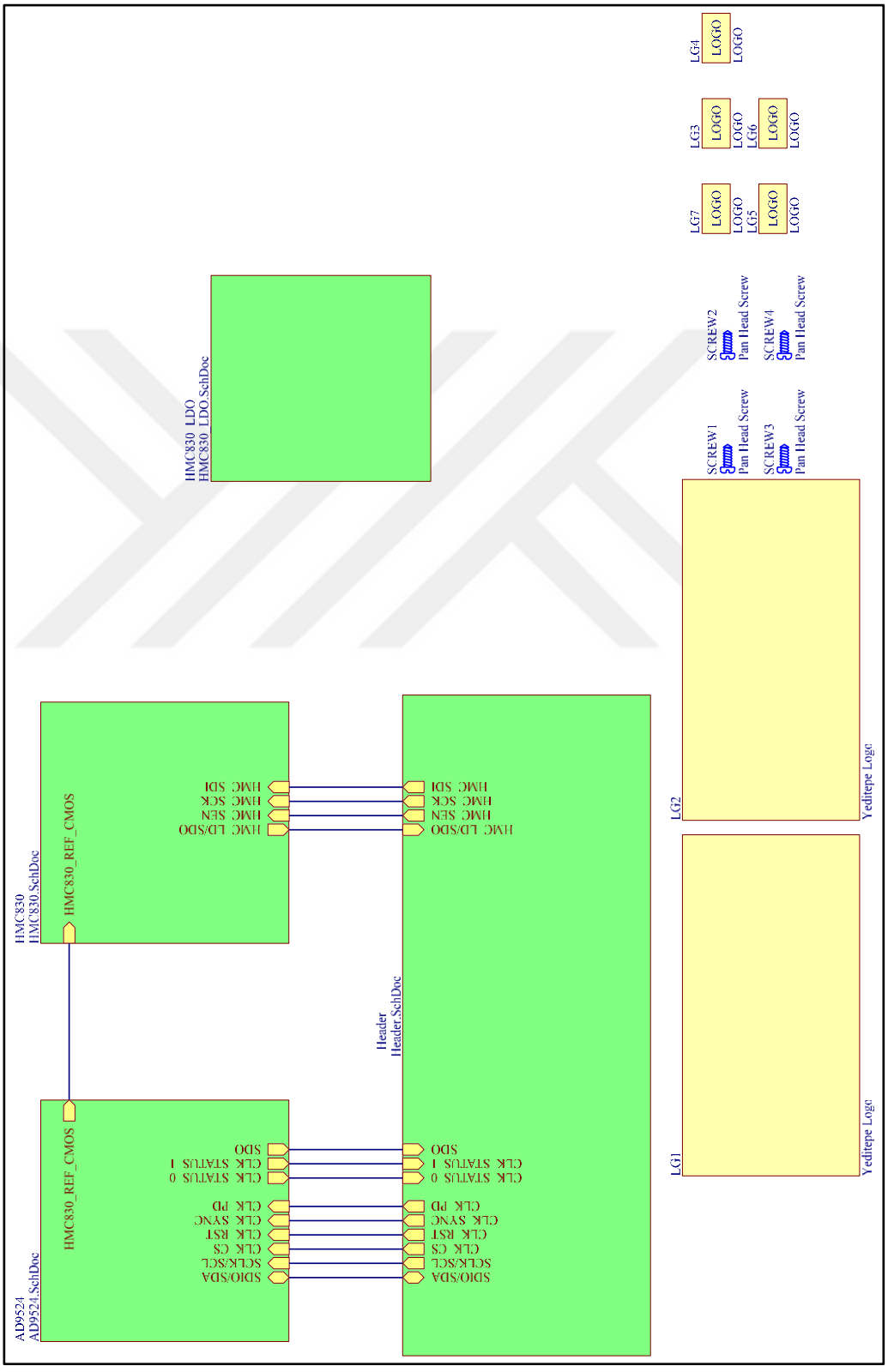

Figure C.1. Top level schematic of the synthesizer design

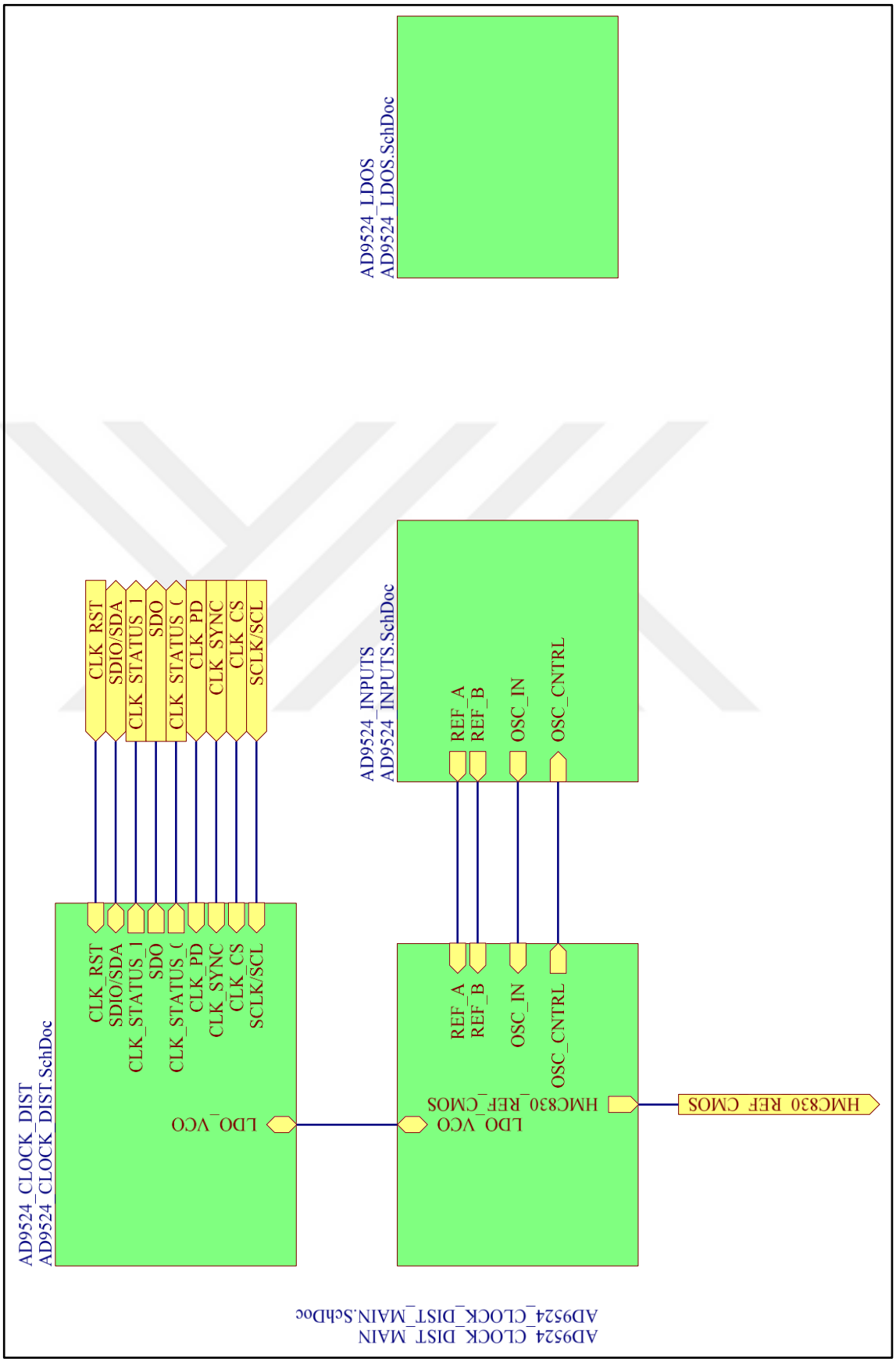

Figure C.2. Clock distribution schematic of the synthesizer design

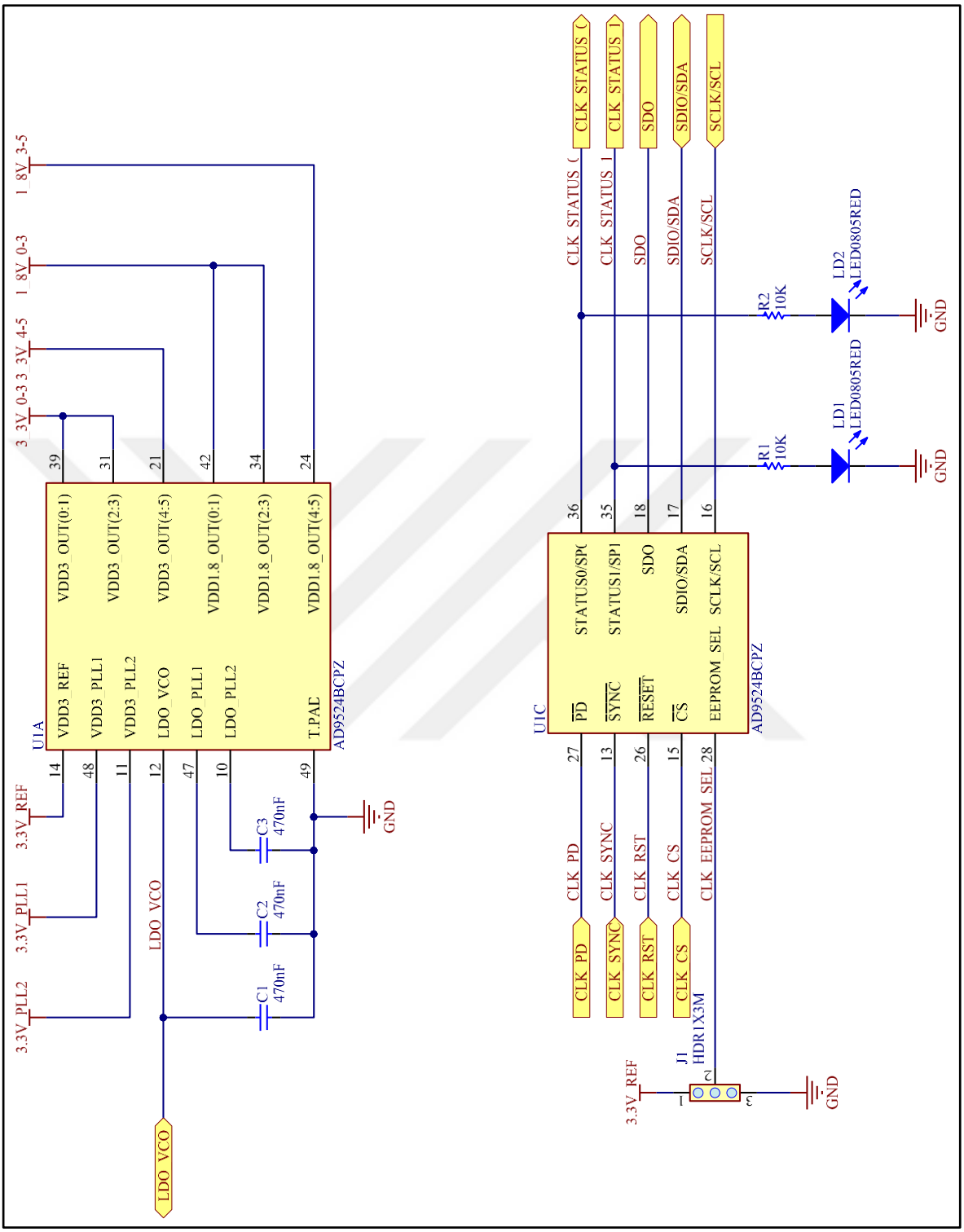

Figure C.3. Interface schematic of AD9524

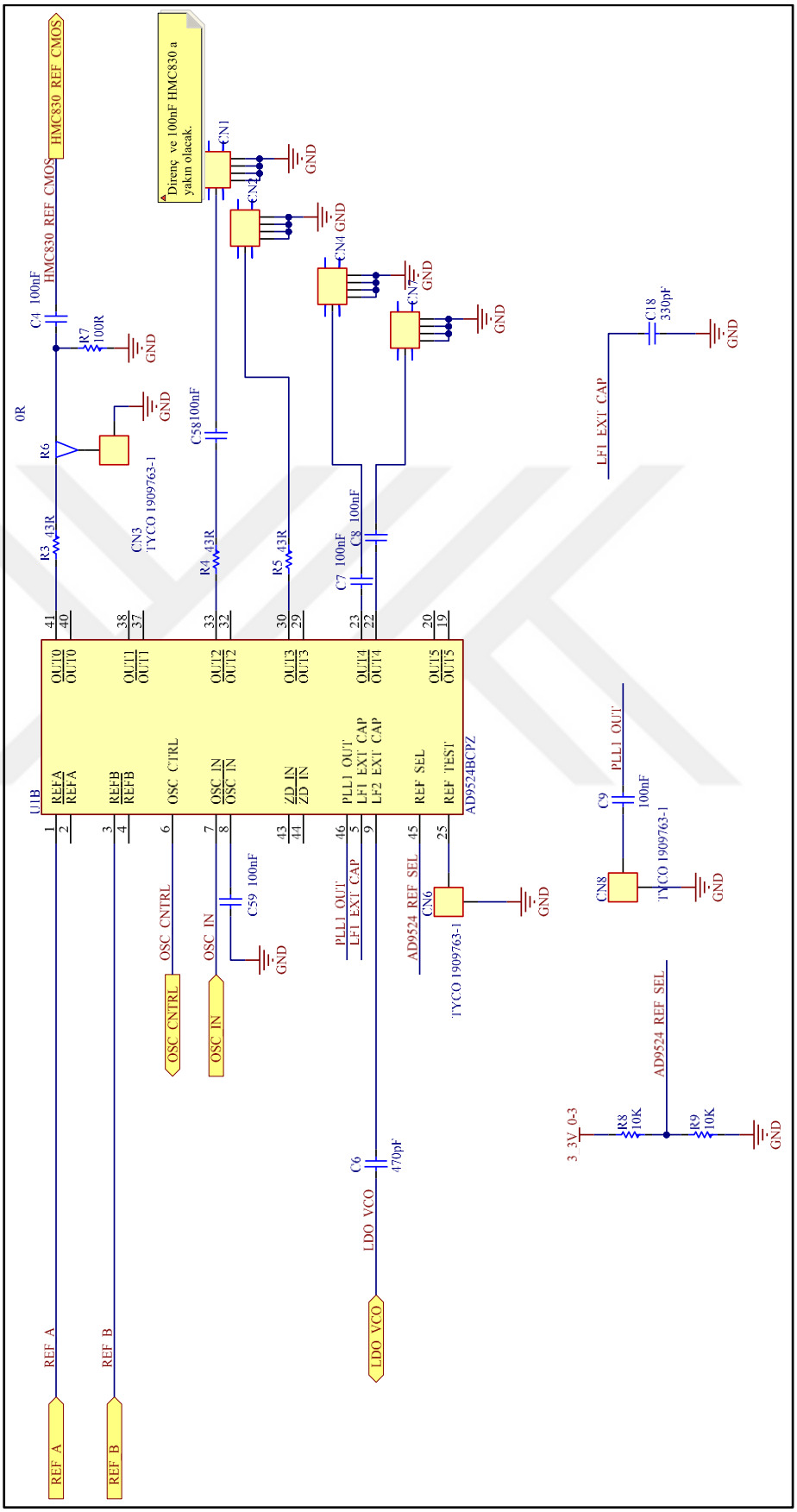

Figure C.4. Clock distribution schematic of the AD9524

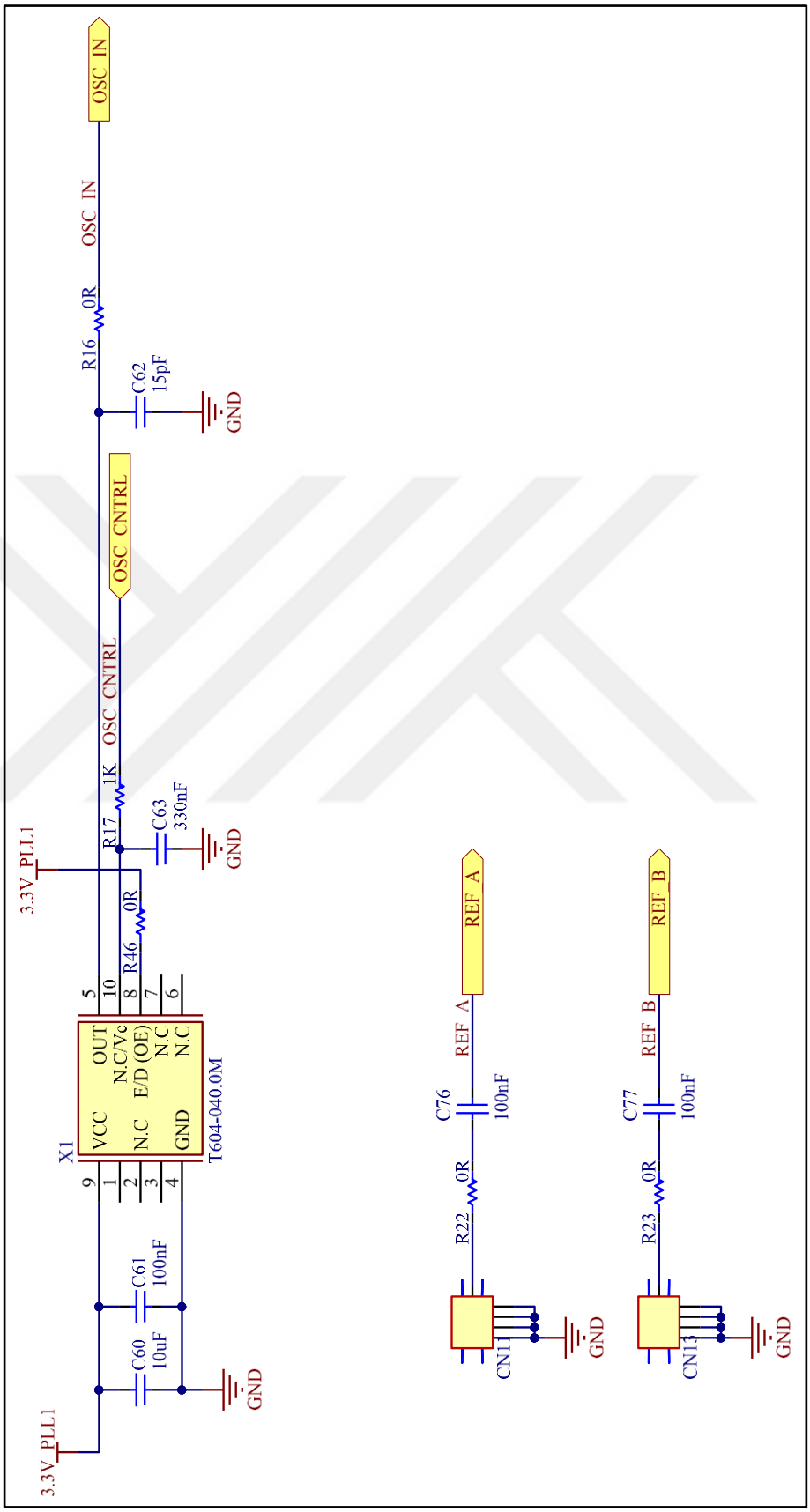

Figure C.5. Reference input schematic of the design

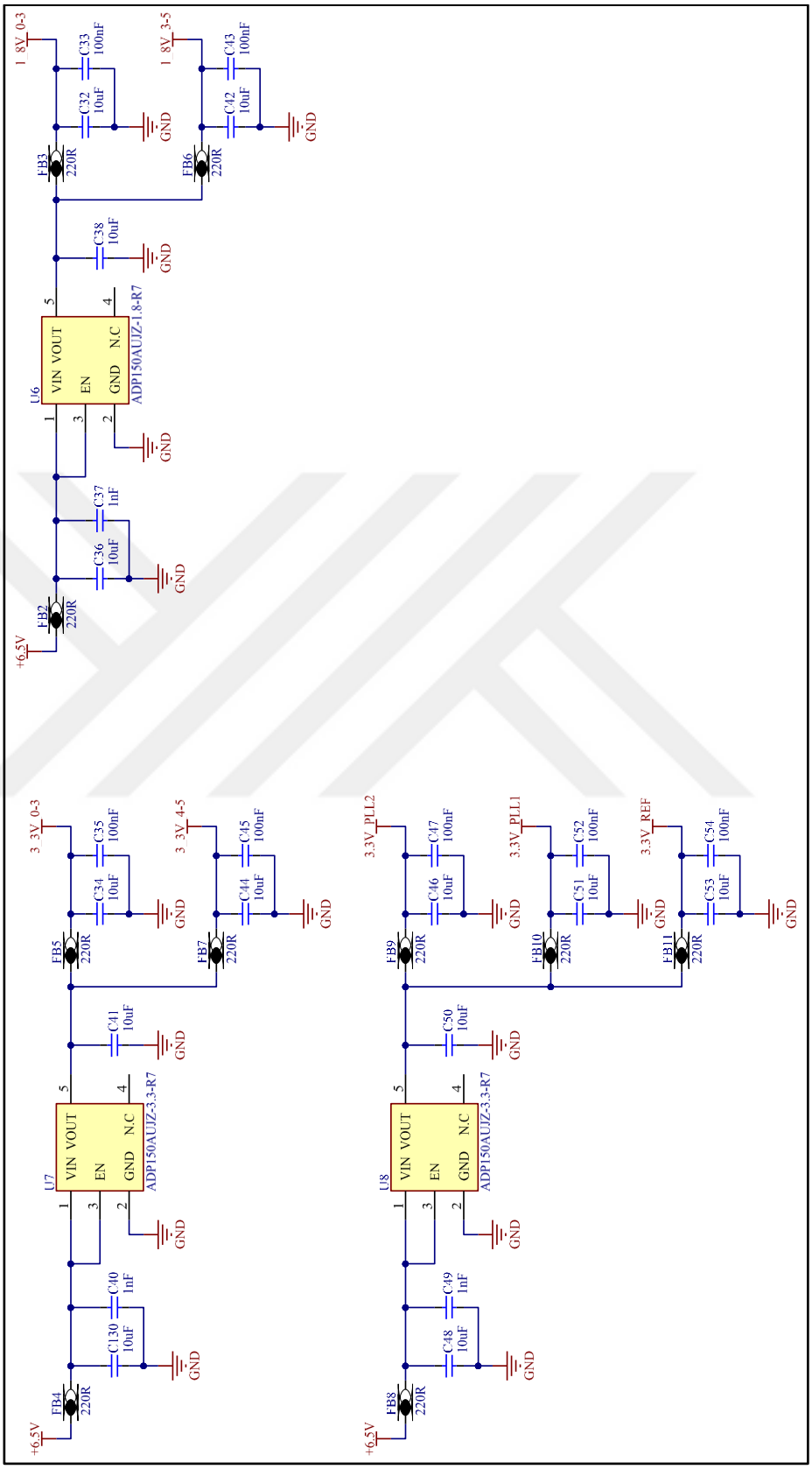

Figure C.6. LDO block of the AD9524

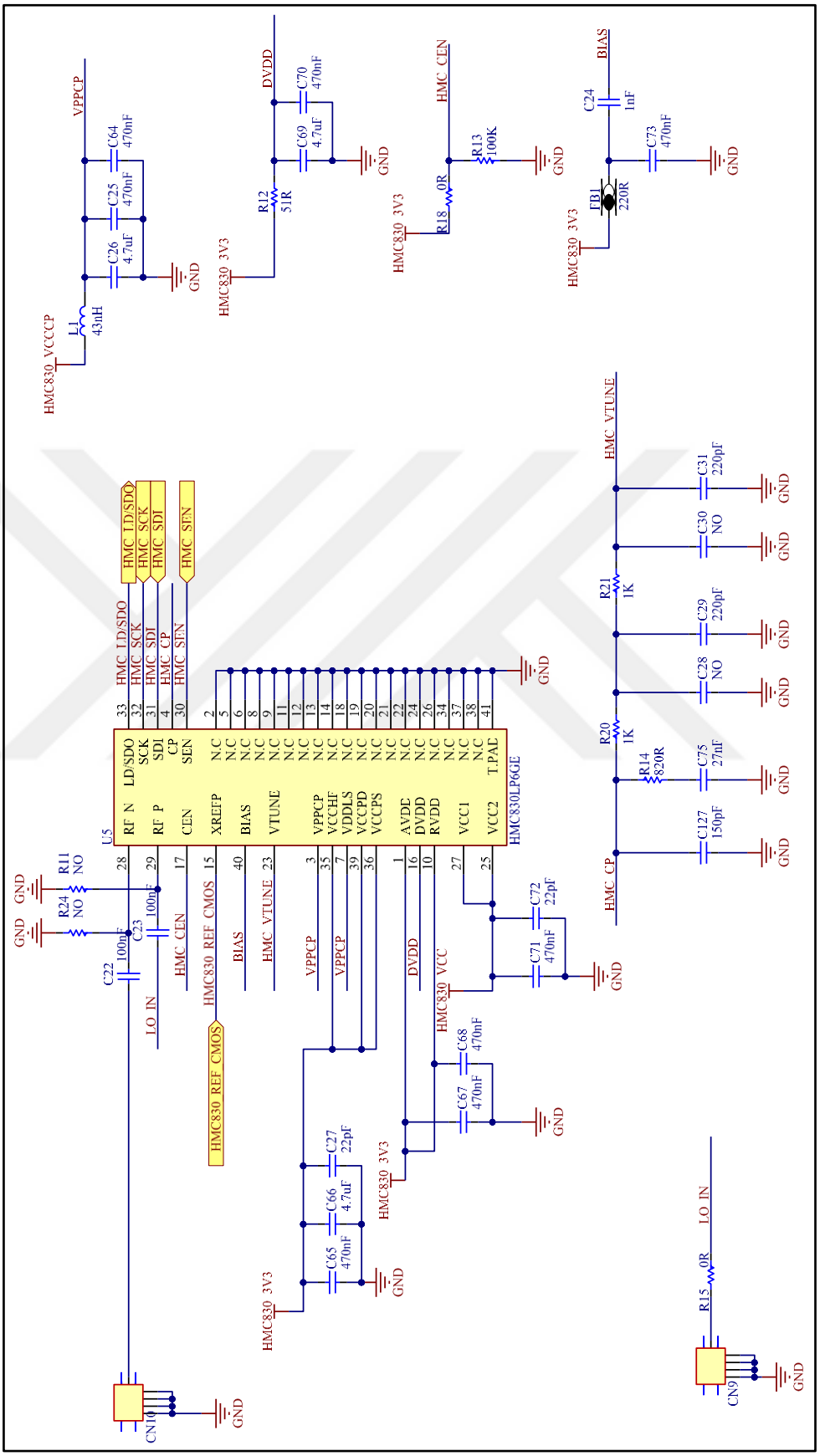

Figure C.7. RF PLL block of the design

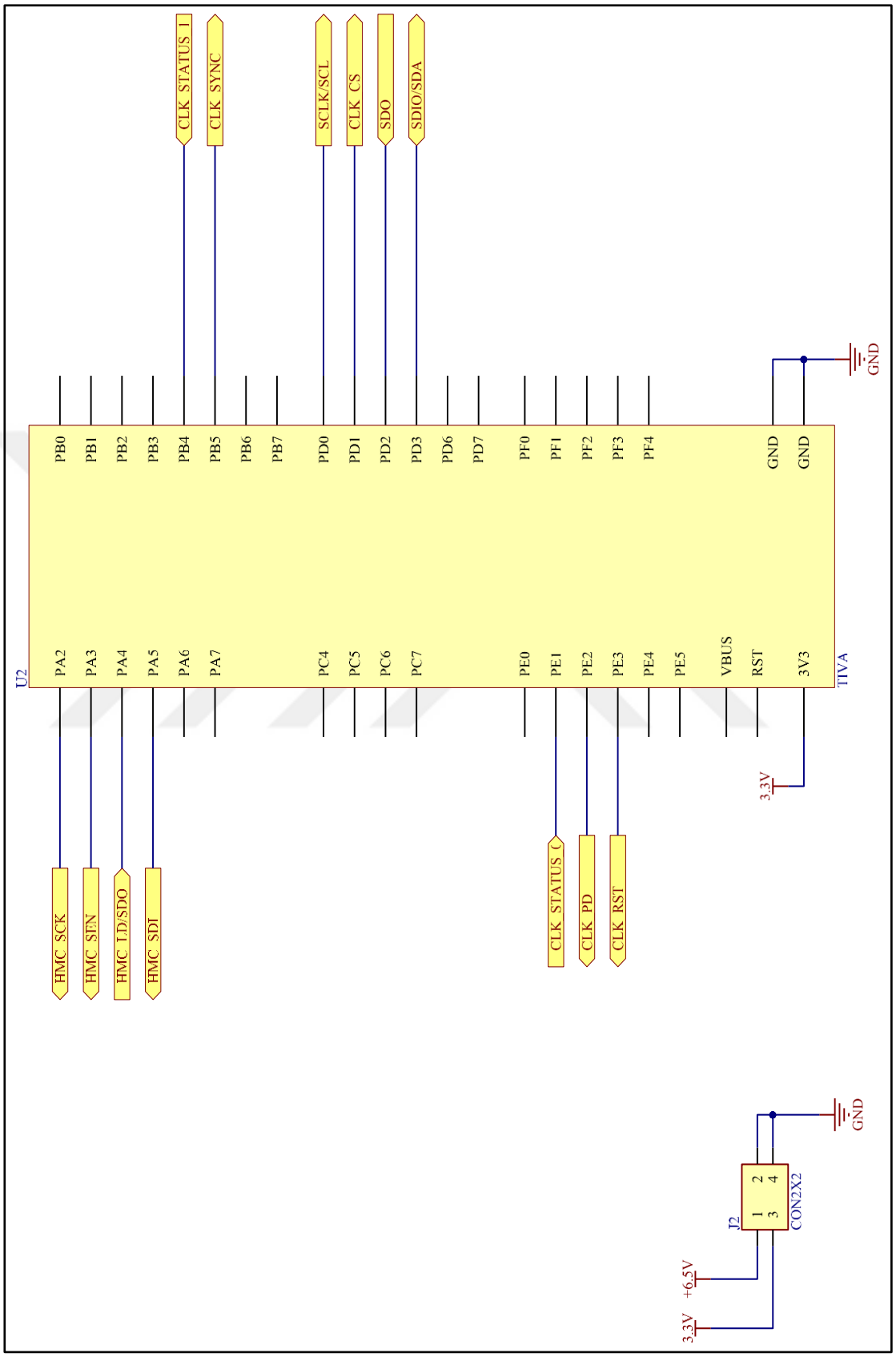

Figure C.8. TIVA connection schematic

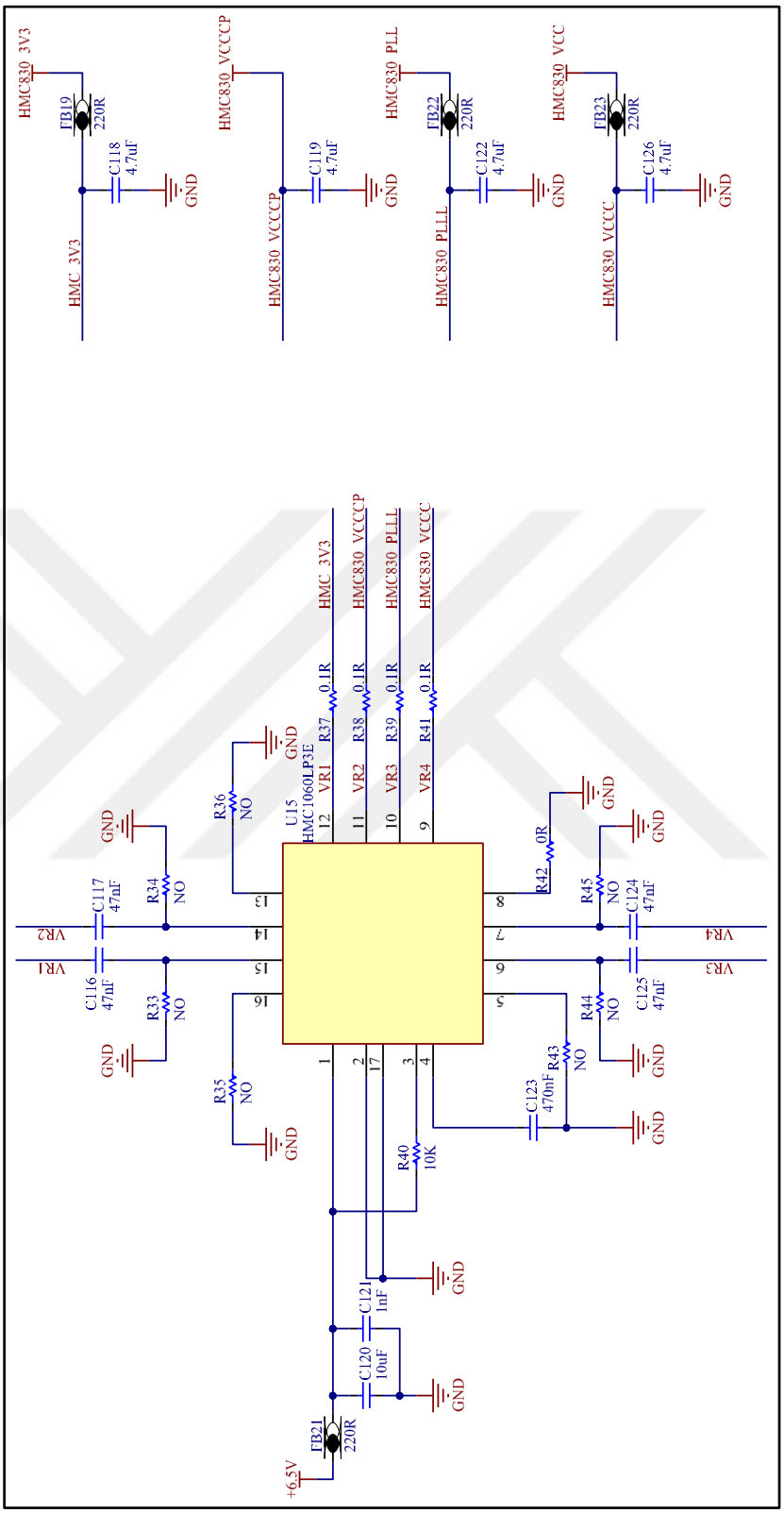

Figure C.9. LDO block schematic of RF PLL

APPENDIX D: LAYOUT DESIGN OF THE SPURIOUS-FREE SYNTHESIZER

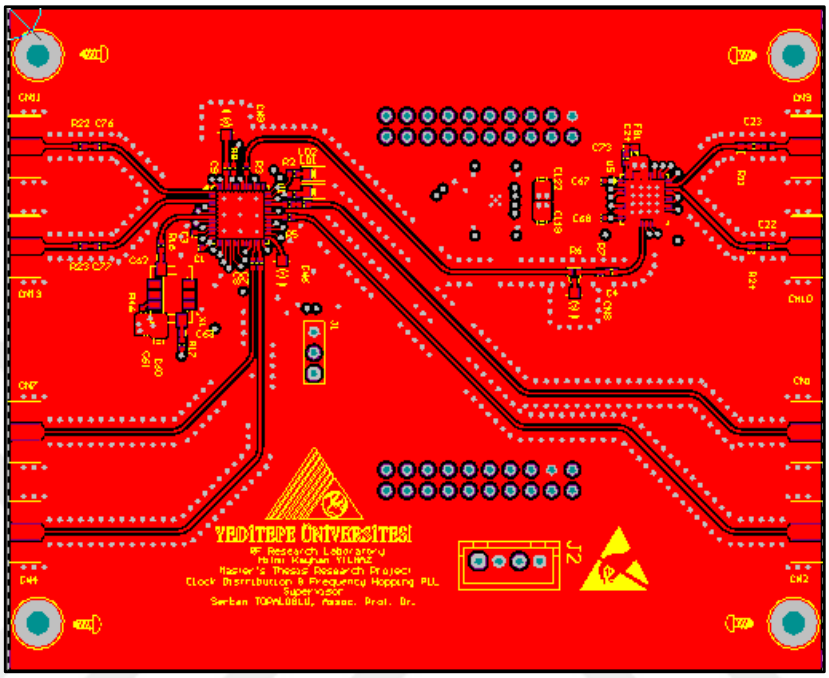

Figure D.1. The top layer of the synthesizer design

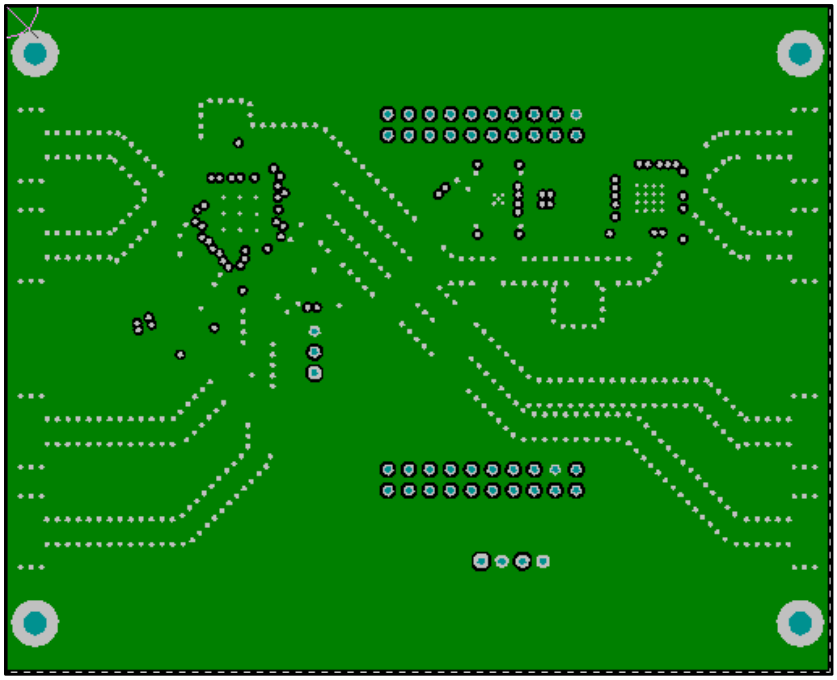

Figure D.2. The second layer (Ground layer) of the synthesizer design

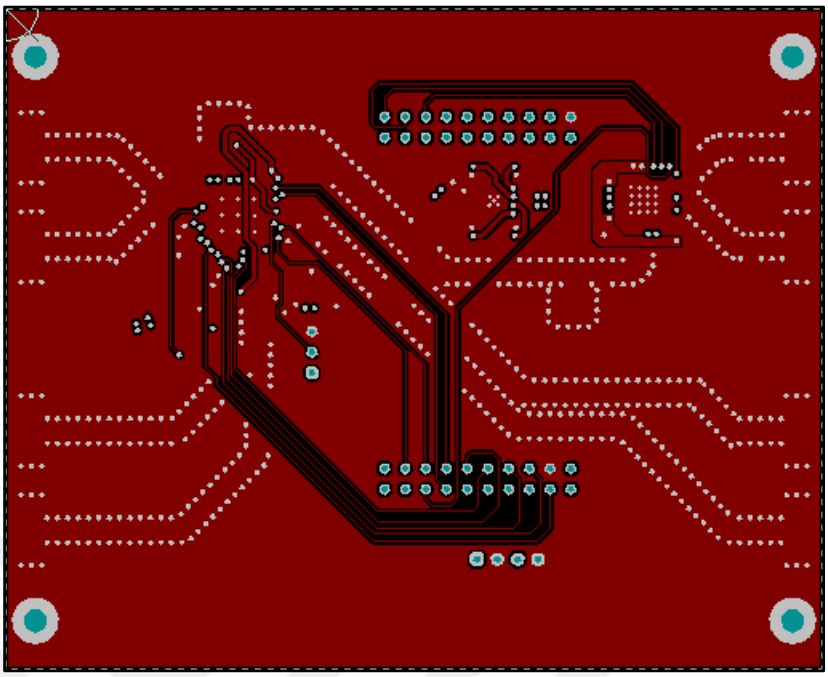

Figure D.3. The third layer (Signal layer) of the synthesizer design

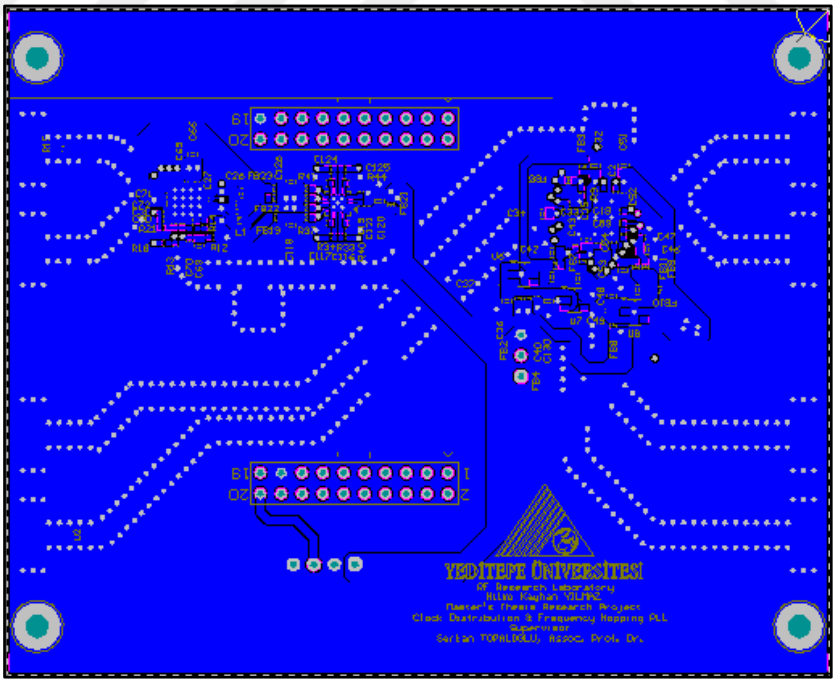

Figure D.4. The bottom layer of the synthesizer design