FREQUENCY-LOCKED INTEGRATED CMOS OSCILLATOR DESIGN WITH RESISTIVE REFERENCE

by

Taner Barışık

Submitted to Graduate School of Natural and Applied Science
in Partial Fulfilment of the Requirements
for the Degree of Master of Science in
Electrical and Electronics Engineering

Yeditepe University

2019

FREQUENCY-LOCKED INTEGRATED CMOS OSCILLATOR DESIGN WITH RESISTIVE REFERENCE

APPROVED BY:

Prof. Dr. Uğur Çilingiroğlu .....
(Thesis Supervisor)
(Yeditepe University)

Prof. Dr. Arda Deniz Yalçınkaya .....
(Boğaziçi University)

Assoc. Prof. Dr. Serkan Topaloğlu .....
(Yeditepe University)

DATE OF APPROVAL: ..../..../2019

ACKNOWLEDGEMENTS

I would like to express my most sincere appreciation and thanks to Prof. Dr. Uğur Çilingiroğlu, you have been a great mentor for me. I would like to thank you for inspiring and encouraging me.

I would especially like to thank Dr. Anıl Özdemirli for his never ending support in every possible way. I would also like to thank to my friends Erol Asığ, Ali Arda Yıldız and Ali Baran Dursun, your friendship is very dear to me.

I would also thank my colleague Ömer Orberk for his support. I can't thank you enough for your help and guidance. I have learned so much from your brilliant comments and suggestions.

A special thanks to my girlfriend Esra Vural. Your patience and love made all this possible.

Finally, I would like to show my gratitude to my mother Ayten Barışık, father Ahmet Barışık and my sister Pinar Karataş. Words can not express how grateful I am for your endless love and sacrifices that you've made in my whole life.

ABSTRACT

FREQUENCY-LOCKED INTEGRATED CMOS OSCILLATOR DESIGN WITH RESISTIVE REFERENCE

The purpose of this thesis is to introduce a design for a CMOS oscillator, that is practically insensitive to temperature and line voltages and conservative in power consumption.Also presented are the details of a band-gap reference voltage reference and a beta-multiplier current reference as needed for the proper operation of the oscillator.

Design and characterization of the proposed oscillator has been performed for XFAB XH018, 0.18 μm CMOS technology. The output of the oscillator provides a square wave of 545.5 kHz at room temperature with typical conditions. Oscillator output has achieved stable frequency within the temperature range -40 $^{\circ}\mathrm{C} \sim 85\ ^{\circ}\mathrm{C}$ and for $\pm$ 5 percent line voltage variation. The circuit satisfies the specifications by consuming only 5 $\mu\mathrm{W}$ and not more than $\pm$ 0.65 percent frequency variation. The design has also been verified in all process corners and distribution in process and matching for 3 σ.

ÖZET

DİRENÇ REFERANSLI FREKANSI KİLİTLENMİŞ ENTEGRE CMOS OSİLATÖR

Bu tezin amacı, sıcaklık ve kaynak gerilimlerindeki değişimlere karşı yüksek tolerans gösteren, ayrıca düşük güç tüketimine sahip CMOS teknolojisiyle tasarlanmış bir osilatörü tanıtmaktır. Ayrıca devrenin operasyonlarını gerçekleştirebilmesi için gerekli olan Bant-aralığı gerilim kaynağı ve beta çarpanı akım referansı devreleri de tanıtılmıştır.

Bu tezde tanıtılan osilatör XFAB XH018, 0.18 μm CMOS teknolojisi ile tasarlanmış ve karakterize edilmiştir. Osilatör devresi oda sıcakığında ve ideal koşullarda 545.5 kHz frekansında kare dalga üretmektedir. Osilatörün cıkışı -40 °C $\sim$ 85 °C sıcaklıklarında ve yüzde $\pm$ 5 kaynak gerilimi değişimlerine karşı sabit bir frekans üretmektedir. Devre, istenen özellikleri yüzde $\pm$ 0.65'den fazla frekans değişimi göstermeyerek ve 5 µW'dan daha düşük güç tüketerek karşılamaktadır. Tasarım ayrıca tüm teknoloji köşelerinde ve Monte Carlo simulasyonunda 3 σ dağılımıyla doğrulanmıştır.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS/ABBREVIATIONS

A_d	Open-loop gain of OTA
C_{SW}	Switch capacitor
C_{IN+}	Capacitor on the non-inverting input
C_{IN-}	Capacitor on the inverting input
C_{ox}	Oxide capacitance
f_d	Dominant pole frequency
f_{nd}	Non-dominant pole frequency
F_{OUT}	Output frequency of oscillator
g_m	Transconductance of transistor
I_{REF}	Reference current
K_{VCO}	Frequency sensitivity of VCO to the input voltage
k	Boltzmann constant
L	Length of MOSFET
M_N	N_{th} MOSFET
ppm	Parts per million
Q_N	N_{th} BJT
q	Elementary charge
r_{ds}	Drain-source dynamic resistance
r_o	Output dynamic resistance
R_{REF}	Reference resistor
R_{OUT}	Output resistance of OTA
V_{GS}	Gate to source voltage
V_{IN+}	Non-inverting input of OTA
V_{IN-}	Inverting input of OTA
V_{BG}	Band-gap voltage
V_C	Capacitor voltage
V_{DD}	Supply voltage
V_O	Output voltage
V_{DSsat}	Drain source saturation voltage

V_T	Threshold voltage
T	Temperature
W	Width of MOSFET
μ_n	Electron mobility of n-channel

AC	Alternating current
BJT	Bipolar junction transistor
DC	Direct durrent
IoT	Internet of things
LC	Inductor-capacitor
PDK	Process design kit
PM	Phase margin
MIM	Metal-insulator metal capacitor
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	N-type metal oxide semiconductor field effect transistor
NAND	Not-and logic gate
OTA	Operational transconductance amplifier
PMOS	P-type metal oxide semiconductor field effect transistor
RC	Resistor-capacitor
RFLO	Resistive frequency-locked-oscillator
SoC	System on a chip
VCO	Voltage controlled oscillator
VLSI	Very large scale integration

1. INTRODUCTION

1.1. PERFORMANCE METRICS OF OSCILLATORS

An oscillator is an electronic circuit block that provides a repetitive AC signal. Oscillators are one of the most common circuits in electronics, because generation of a clock signal is required in a large variety of circuitry ranging from basic sensors or energy harvesting circuits to complex VLSI circuits. Oscillators usually consist of an amplifier with positive feedback or regenerative feedback [1]. Shape and amplitude of the clock signal may vary depending on the topologies and components. Shape of the signal can be sinusoidal, square, triangle, sawtooth or any other periodic wave. Figure 1.1 depicts most common oscillator signal shapes.

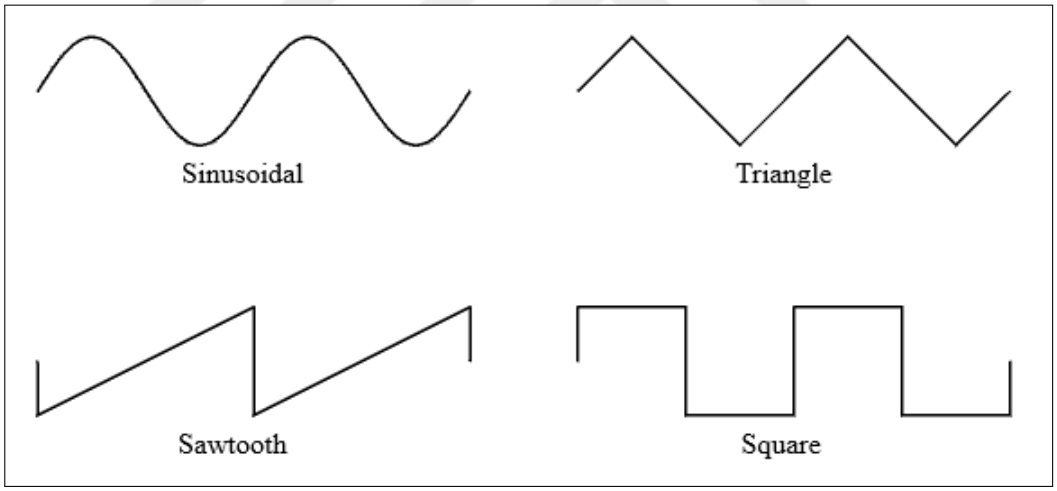

Figure 1.1. Most common oscillator waveform types

The elementary metric of an oscillator is frequency. It is the repeating rate of the output signal from the oscillator block. It is measured in hertz. Oscillator frequencies may vary from sub-hertz to terahertz [2] depending on the application. Some of the oscillators are designed with a programmability features by which, their frequency can be varied as needed [3].

The main property expected from an oscillator is to have a stable frequency. It is typically defined as the change of frequency in parts per million (ppm). It is the variation of

frequency that caused by external conditions. Conditions that impact on frequency stability of oscillators may differ by oscillator types.

Temperature stability and temperature range are usually the most common design specification for the oscillators. Since most of the oscillators are expected to work in uncontrolled environments, temperature sensitivity of the oscillators designs are usually concern of most of the designs. Temperature specification is usually defined for a typical condition and a range across nominal value. Even though the typical conditions for the temperature is usually 27 °C, operating range may vary across industries and applications. Examples of temperature ranges are shown in Table 1.1.

Table 1.1. Operating temperature range examples

Commercial	0 °C to 70 °C
Industrial	-40 °C to 85 °C
Military	-55 °C to 125 °C

Supply voltage sensitivity metric is defines voltage required to operate the oscillator. Supply voltage may drop down to 0.4 V [4] depending on the supply of the system. Supply voltage sensitivity has an impact on frequency instability of an oscillator. Since variation of supply could directly impact frequency stability, often linear regulators are used for supplying oscillators.

For most of the applications in electronics, power consumption and power efficiency is very important performance metrics in design. This metric is also competing point for oscillator designs. Specifications of oscillators are usually defines a maximum power consumption limit. Power efficiency of an oscillator may be measured as generated frequency per consumed power. Which is energy consumption per cycle of the oscillator.

In applications like switching converters, clocks that settles in few clock period [5] increase the efficiency of the converters. Since they are able to start up and shut down very fast, converters are able to follow the fast paced load transient. Other than specific applications like mentioned, oscillators start-up time is still expected to be fast and should not be the bottleneck of the system to start-up.

Table 1.2. Specifications

Technology	XFAB XH018, 0.18 μm
Maximum Start-Up Time After Power-Up	4 ms
Maximum Power Consumption	20 μW
Static Line Voltage	1.8 V
Line Voltage Variation	± 5 %
Operating Temperature Range	-40 °C to 85 °C
Maximum Frequency Variation Across All Corners Within 3σ Range	± 0.65 %

Given in Table 1.2 are the specifications defined for the oscillator designed in this thesis. Specification of the fabrication technology, narrows down the viable oscillator topologies to on-chip oscillators. Operating temperature range of 85 °C and ± 5 percent line voltage variations are the most effective on frequency instability. Therefore in order to maintain the maximum ± 0.65 percent frequency variation, topology of an oscillator should focus on temperature and line voltage insensitivity. There are two more limiting specifications in Table 1.2. Oscillator must have an stable output within 4 ms after start-up. The other is that the overall power consumption is limited by 20 μW. With an 1.8 V supply, maximum average current consumption of the system turns out to be approximately 11 μA.

1.2. ON-CHIP OSCILLATOR APPLICATIONS

In recent years, with increasing demand of IoT devices operating with ultra-low power, fundamental circuits like clock generators for analog and digital blocks had to evolve for this purpose, meanwhile increasing their performance [6]. Although crystal oscillators can provide very high frequencies, their power dissipation is significantly high, compared to their frequency outputs. Which makes them inefficient in cycle per energy performance metric. Also, crystal oscillators require longer start-up time which will result in extra power consumption. IoT devices have to be operated in wide thermal ranges, low and unstable line voltages. In order to satisfy these constraints, the design of the IoT devices has to be performed while maintaining related qualifications. The most desired property of these

devices to have stable operation which is practically insensitive to temperature and line voltage changes.

On-chip oscillators are able to provide low power consumption and stable frequency output over a wide temperature ranges. It is obvious that low power consumption is crucially important in wireless sensor applications. To maintain frequency stability is also crucial at low power levels. Since these devices have to operate with a limited power supply, on-chip oscillators must have an extended life time by means of their charged batteries.

In order to satisfy the conditions mentioned above, several topologies have been introduced. The most common topologies to maintain the specifications are LC oscillators, relaxation oscillators and RC harmonic oscillators.

1.3. CONVENTIONAL OSCILLATOR TOPOLOGIES

Probably the most popular among the oscillators mentioned above is the RC Relaxation Oscillator. Electrical schematic of a relaxation oscillator is shown in Figure 1.2.

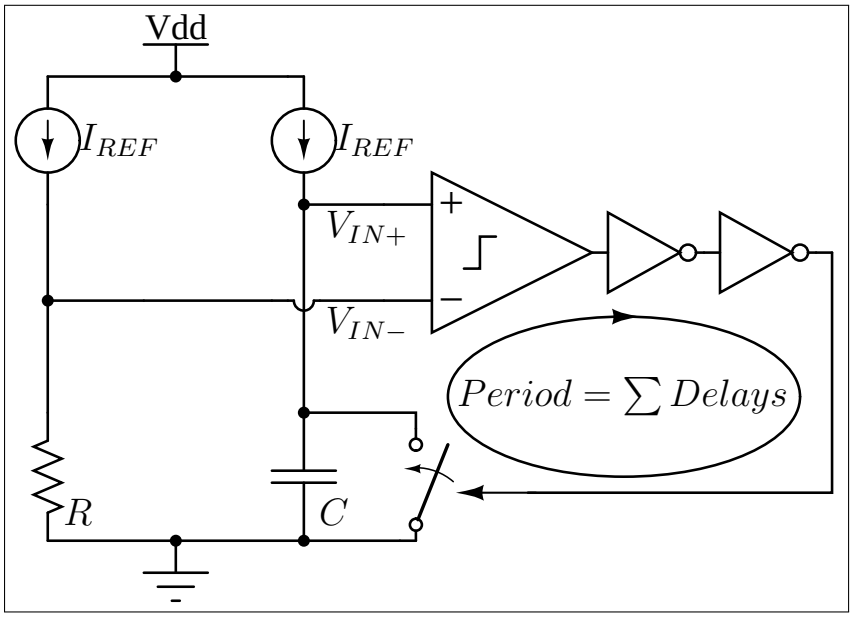

Figure 1.2. Relaxation oscillator

Relaxation oscillators consist of two identical current sources, capacitor with a switch, a resistor and a comparator with buffers. The voltage at the inverting input of the comparator

is created by the product of I_{REF} and the reference resistor R. Other reference current flowing through the capacitor, charges the reference capacitor C until V_{IN+} surpasses V_{IN-}. Then, the reset signal created by comparator and V_{IN+} is set to 0 V via switch.

In this topology, oscillation is generated by sum of RC delay, comparator delay and buffer delays. In Figure 1.3, impact of difference in total delay on frequency output is depicted. Delays of the cells may vary in many ways such as temperature and ripples in line voltage. Since there is no compensation mechanism in this topology, variation of delay directly changes frequency of the oscillator.

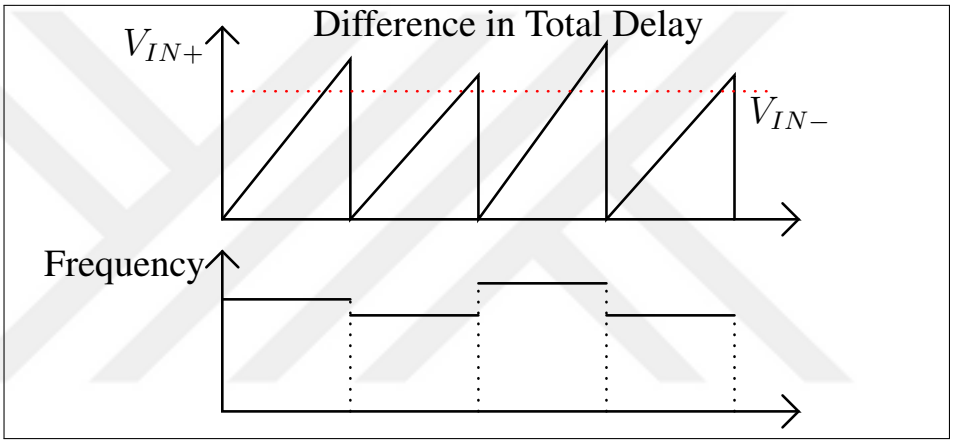

Figure 1.3. Relaxation oscillator delay representation

On the RC delay side, temperature compensation can easily be maintained. Consolidating resistors with negative and positive temperature coefficients can provide temperature insensitive resistor. Alternatively external resistors can be used in designs to get rid of trimming. MIM capacitors which are widely used in on-chip designs have almost zero temperature coefficient. Therefore RC delay is almost temperature independent. On the other hand, comparator delay and buffer delays can not be discarded easily. Even though temperature dependence of these blocks can be reduced, this requires complex design methods and also costs for more power or area on the chip.

Another commonly used on-chip oscillator topology is LC oscillators. There are many versions of LC oscillators like described in [7] or [8]. But due to the efficiency, complementary LC structure is usually preferred. Simplified schematic of complementary LC oscillator is shown in Figure 1.4.

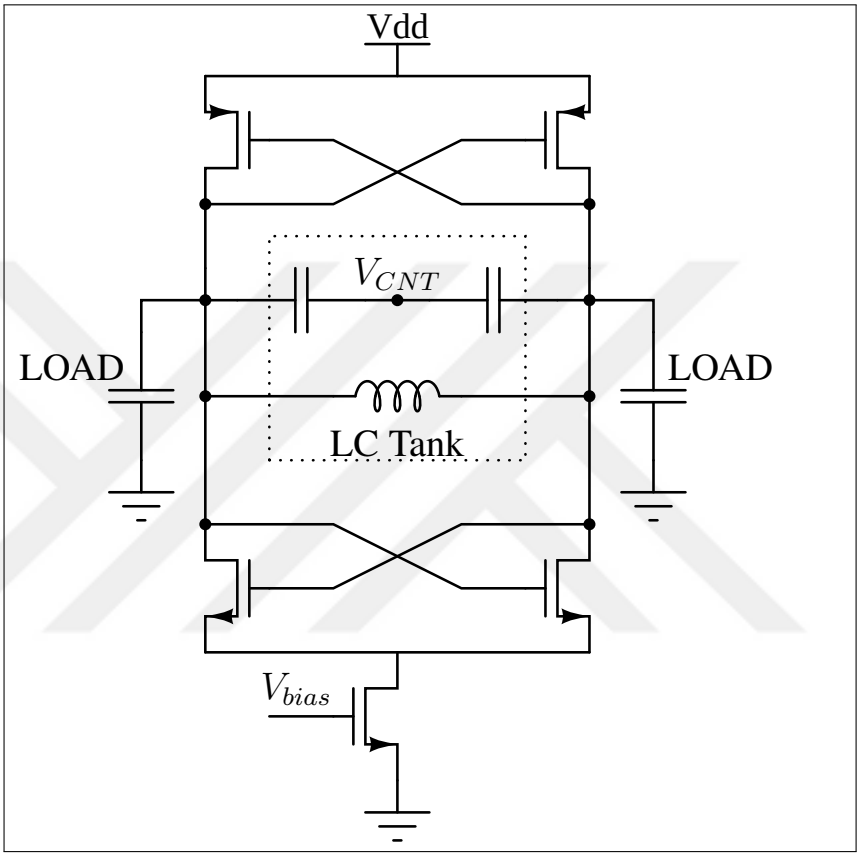

Figure 1.4. Complementary LC oscillator

LC oscillators are generate positive feedback from their LC tanks. Frequency of the oscillator is the resonant frequency of the tank as given in (1.1) [9].

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{1.1}$$

One disadvantage of the LC oscillator is that it is more suitable for high frequency applications. High frequency, comes with a high power consumption. Power consumption limited applications may suffer from this. As it can be seen in (1.1), even though frequency can be reduced by increasing the inductance, this comes at a price. While increasing L,

parasitic capacitances and increasing resistive losses decreases the frequency stability. Also this big inductor causes very large footprint. Therefore costs more area on the chip.

An LC oscillator with an stable frequency is usually provides an oscillation rate in the range of radio frequencies. [10] This yields around mW of power consumption even in a low power design. [11] This doesn't fit power consumption specification on Table 1.2.

1.4. PROPOSED OSCILLATOR DESIGN

Design of the oscillator specified in Table 1.2 requires high level of frequency stabilization. In order to achieve this, design should have immunity to both environmental and process variations. Conventional designs like the RC Relaxation Oscillator topology represented in Section 1.3, is very sensitive to process variations due to its frequency being mostly dependent on delays of comparator and buffers. Therefore conventional relaxation oscillator topology can't fit to the specifications.

This design does not have a specification for frequency. However, frequency of oscillator is correlated with consumed power, and therefore with a total power consumption. Taking base of low power works like [11], this design achieved 2.45 GHz oscillation with 1 mW. For a 20 $\mu\mathrm{W}$ limited power, including increasing percentage of power consumption of references, frequency is estimated over high frequency band. Which is between 3 to 30 MHz.

As mentioned earlier, LC oscillators provide RF band frequencies with high accuracy and power efficiently. However, LC topologies are not suitable for lower frequencies. In order to achieve low frequency outputs on LC oscillators, inductor value must be increased. Increasing size of the inductor increases its resistance and therefore it causes the decrease of quality factor. Due to decreased quality factor of inductor, LC oscillator topology looses its frequency accuracy. Therefore with low power application like this, LC oscillators are not suitable.

The general purpose of this thesis is to achieve better temperature coefficient at higher frequencies than their predecessors while preserving basic oscillator performance metrics like the energy consumption per cycle and line voltage insensitivity.

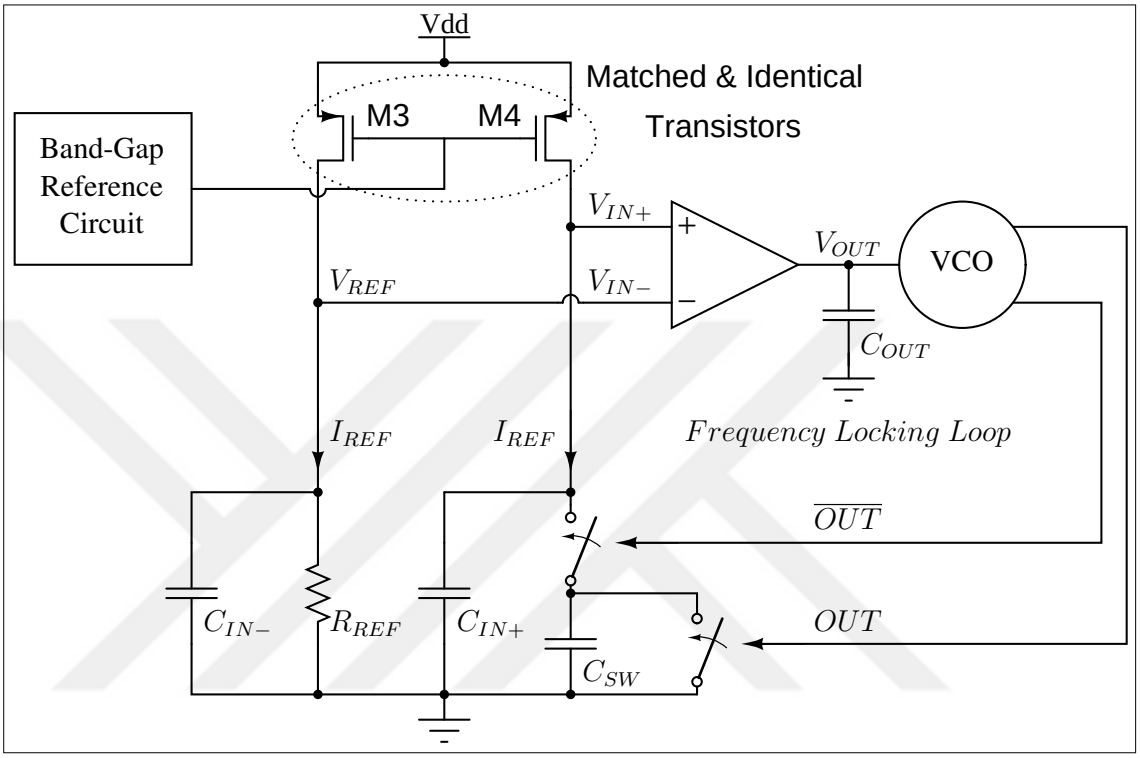

Figure 1.5. Switched-capacitor frequency-locking-loop

Proposed oscillator topology is illustrated in Figure 1.5 is based on works [12]. This topology aims at minimizing frequency dependent components and nullifying their dependency to the process, temperature and line voltage variations. In order to realize this, several changes are adapted to design shown in [12].

Frequency generation is controlled by two passive components in this topology. Main idea is to equalize impedance's of R_{REF} and C_{SW} via frequency feedback from oscillator. Current references on [12] is realized with technique represented in [13]. Even it is a resistorless and low area design, due to its high process and temperature dependency, in proposed design V_{REF} voltage generated by a band-gap circuit.

Amplifier equalizes voltages of V_{IN-} and V_{IN+}. Equating both node voltages yields first order frequency response of the system. V_{IN+} and V_{IN-} node voltages are represented in

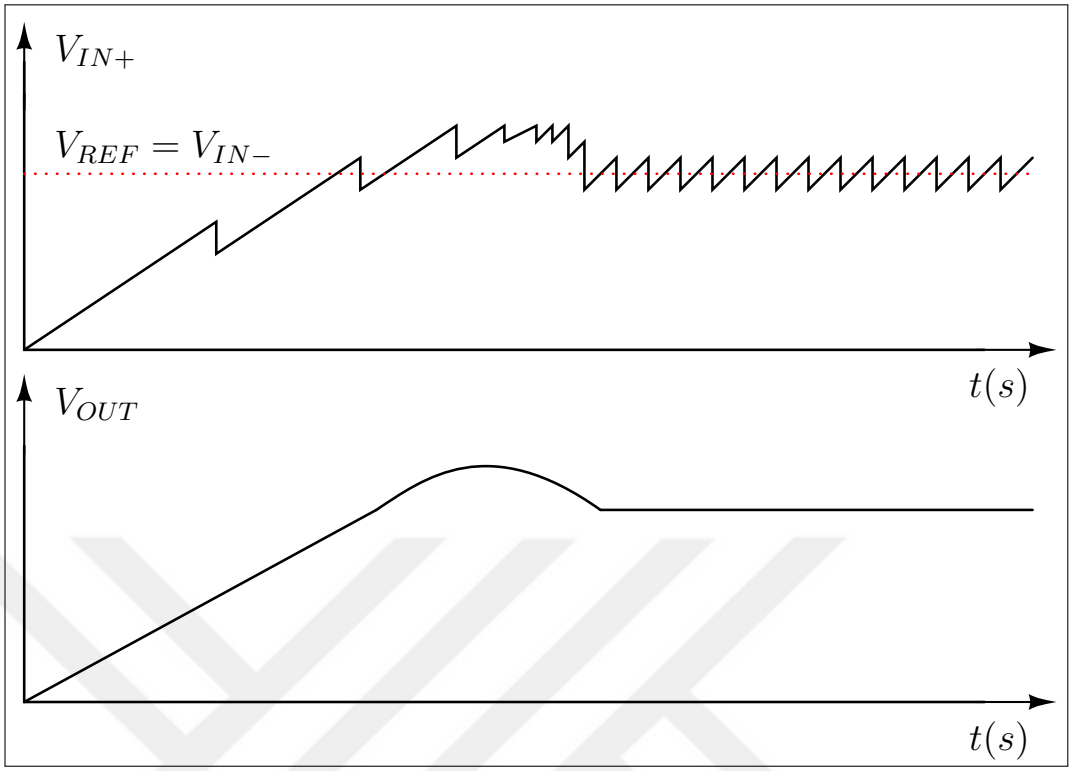

Figure 1.6. Illustration of start-up and settling behavior

Figure 1.6.

$$F_{OUT} = \frac{1}{R_{REF}C_{SW}} \tag{1.2}$$

Since frequency of the oscillator is function of R_{REF} and C_{SW}, line voltage, temperature and process variations on these passive components are main concerns of the designs. In [12], negative temperature coefficient poly resistor without and positive temperature coefficient diffusion resistor is serially connected to decrease temperature dependency of R_{REF}. However even with 2 point trimming of these resistors, temperature dependency decreased as much as 0.18 percent .Considering specified maximum variation across all corner cases, this design required better resistor solution.

In order to nullify these effects on the R_{REF} on proposed design, $1\mathrm{M}\Omega$ external resistor is chosen. According to the data sheet [14] of the resistor, its temperature coefficient is only 10 ppm/$^{\circ}$C. On the capacitor side, an internal MIM capacitor is used. Even though MIM capacitors are more expensive than MOM capacitors, they are known for better temperature and voltage coefficient. Also they have better immunity to process variations [15].

2. SWITCHED-CAPACITOR FREQUENCY LOCKED LOOP

2.1. FUNDAMENTALS

Stable frequency generation in Switched-Capacitor Frequency Locked Loop depends on equalization of 2 impedances; namely switched-capacitor and reference resistance. As it is in relaxation oscillator case the resistance can be on-chip temperature compensated resistances or external resistors. Since the frequency of an oscillator mostly depends on the temperature coefficients of these circuit elements, devices with low temperature coefficients must be chosen.

Reference current that is flowing through R_{REF} could be created by various methods. In this project, a band-gap based voltage reference is designed for better temperature compensation. A stable reference current I_{REF} is therefore established for low power amplifier with a temperature insensitive R_{REF} and V_{REF}.

$$I_{REF} = \frac{V_{REF}}{R_{REF}} = \frac{V_{IN-}}{R_{REF}} \tag{2.1}$$

V_{REF} is attached to the inverting input of the amplifier. Amplifier equalizes its non-inverting input to inverting input which is equal to V_{REF}. Since both current references are matched and equal in size, they conduct identical current of I_{REF}. This equality only be possible by equalized impedance of both R_{REF} and C_{SW}. F_{OUT} is the output frequency of the oscillator. According to the outputs of the voltage controlled oscillator, C_{SW} charges or discharges. Current flowing through the C_{SW} is also I_{REF}. Therefore current flowing through the C_{SW} is function of the oscillator frequency which is given in (2.2).

$$I_{REF} = \frac{V_{IN+}}{C_{SW} F_{OUT}} \tag{2.2}$$

On steady state, V_{IN+} and V_{IN-} are equal. Therefore both inputs of the amplifier voltages are cancel each other when equating both 2.1 and 2.2. This yields,

$$F_{OUT} = \frac{1}{R_{REF}C_{SW}} \tag{2.3}$$

In (2.3), reference currents, V_{IN+} and V_{IN-} cancel each other. Therefore generated frequency is insensitive to I_{REF}. Also output frequency is insensitive to the supply voltage because it is not shown in the (2.3). However these are only valid when current source transistors are matched and equal to each other.

In the first order analysis, frequency is only dependent in temperature coefficients of R_{REF} and C_{SW} as described by (2.3). R_{REF} may be chosen as on-chip temperature compensated or external component with a very low temperature coefficient. C_{SW} is an MIM capacitor. Due to MIM capacitors low temperature sensitivity, output frequency becomes almost immune to the temperature.

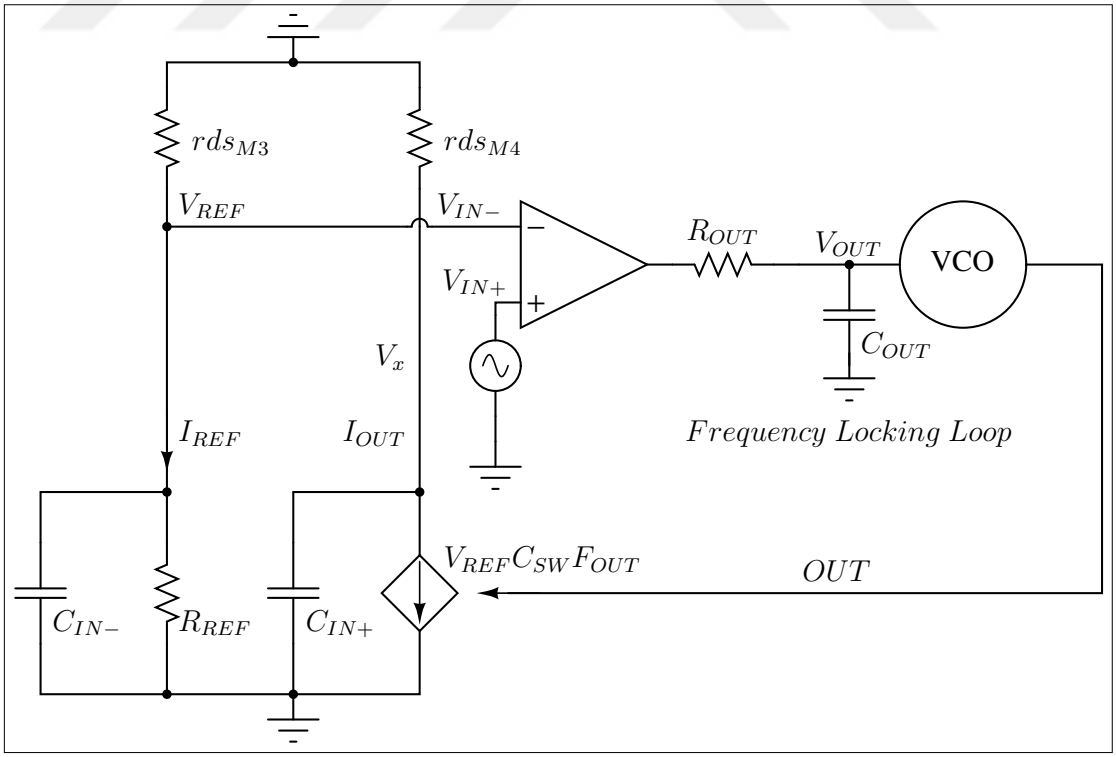

Figure 2.1. Small signal equivalent of switched-capacitor frequency-locking-loop

In determination of the dominant and non-dominant poles of the loop, Figure 1.5 turned into

the equivalent circuit shown in Figure 2.1 by shutting all supplies and breaking the loop on V_{IN+} node. If we would approximate the small-signal current of the C_{SW} from (2.2),

$$I_{REF} = V_{REF} C_{SW} F_{OUT} \tag{2.4}$$

From 2.4, s-domain relationship between V_x and F_{OUT} found as,

$$V_x = \frac{C_{SW} V_{REF} rds_{M4}}{1 + sC_{IN+} rds_{M4}} F_{OUT} \tag{2.5}$$

Frequency of the loop can be represented as a function of V_{IN+} as follows,

$$F_{OUT} = \frac{A_0 K_{VCO}}{1 + sR_{OUT} C_{OUT}} V_{IN+} \tag{2.6}$$

where, A_0 is the differential gain of the amplifier, K_{VCO} is linear approximate frequency gain with a given input voltage and R_{OUT} is the output resistance of the operational transconductance amplifier.

From (2.5) and (2.6), loop gain of the frequency locked loop is,

$$\frac{V_x}{V_{IN+}} = \frac{C_{SW} V_{REF} rds_{M4} A_0 K_{VCO}}{(1 + sC_{IN+} rds_{M4})(1 + sR_{OUT} C_{OUT})} \tag{2.7}$$

Even though there are additional poles coming from OTA, they are not represented in (2.7). From (2.7), frequencies of the poles can be written as,

$$f_{pole1} = -\frac{1}{C_{OUT} R_{OUT}} \tag{2.8}$$

$$f_{pole2} = -\frac{1}{C_{IN+} rds_{M4}} \tag{2.9}$$

Although the amplifier equalizes the voltages at V_{IN-} and V_{IN+}, there is a ripple at V_{IN+} due to switching behavior of capacitors. But the amplitude of these ripples can be minimized by choosing C_{IN+} significantly larger than C_{SW}. From (2.8), low-power amplifier and output

capacitance C_{OUT} act as a low pass filter. This filter also reduces the ripple on input voltage of the voltage controlled oscillator. Therefore, more stable frequency output can be achieved. Clock signal generated by voltage controlled oscillator and its non-overlapping complement, control the switches. Since the amplifier has low power with a high differential gain, it works with a narrow bandwidth. Therefore changes in nodes V_{IN-} and V_{IN+} are reflected to output of the amplifier with a delay. But, once the output frequency has settled, bandwidth of the low power amplifier will not disrupt the generated frequency.

2.2. VOLTAGE CONTROLLED OSCILLATOR

In order to create oscillation with an inverter chain, at least 3 stages with feedback is required. Number of inverters must be increased for increasing the total propagation delay. Yet, number of inverters must be an odd number otherwise it won't oscillate and output will settle at supply voltage or ground. Voltage controlled oscillator used in this topology must achieve the following requirements to satisfy the specifications.

- Low power consumption
- Wide frequency range
- Rail-to-rail operation

Design specifications restrict the power consumption of the oscillator to 20 $\mu\mathrm{W}$. Considering the power consumption of side blocks like amplifiers, reference circuits etc., voltage controlled oscillator's maximum power budged in this design is 15 $\mu\mathrm{W}$. In addition to this power, voltage controlled oscillator is should be able to supply up to 10-20 MHz.

Voltage controlled oscillator topology selected in this design is a ring oscillator which is shown in Figure 2.2. In order to increase frequency sensitivity with a given input voltage and reduce the average current consumption the voltage controlled oscillator, delay of each inverter is increased in a stacked inverter chain.

This thesis aims is to generate fairly high frequencies sensitivity with low amplifier output voltage. Therefore frequency generation per power consumption will be higher.

Voltage controlled oscillator block shown in Figure 2.2 has high input voltage sensitivity. In

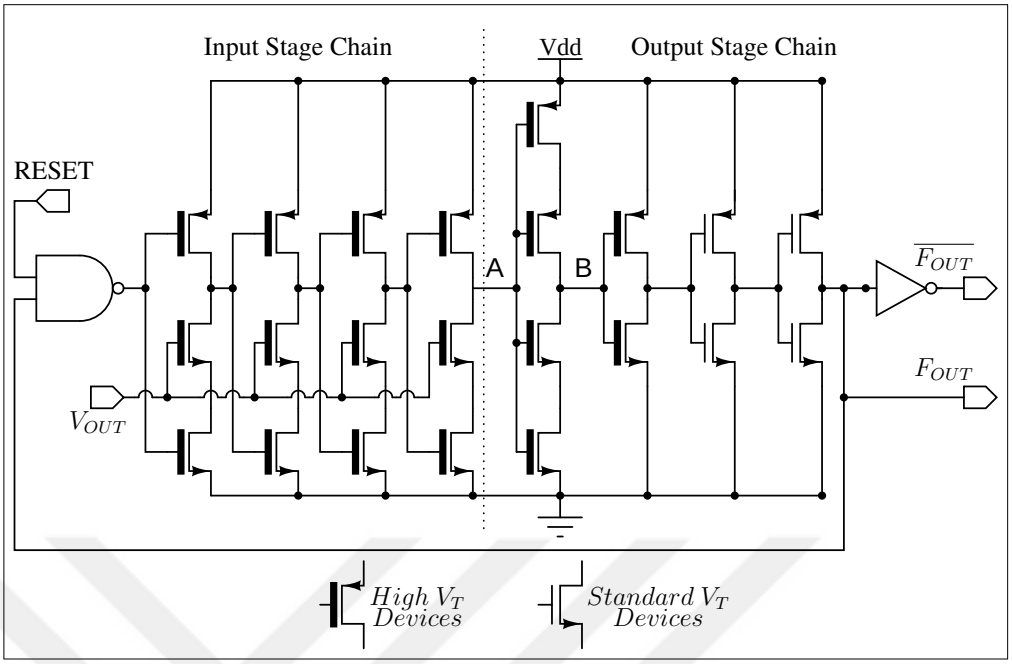

Figure 2.2. Voltage controlled oscillator

order to achieve high K_{VCO}, input stage transistors are forced to operate in sub-threshold region. This configuration increases their delay and yields high input sensitivity for K_{VCO} of voltage controlled oscillator due to their drain currents being exponentially dependent on V_{OUT}. This enables us to drive voltage controlled oscillator with a lower voltage level.

Illustration of output voltage at the end of the input stage chain, is given in Figure 2.3. Waveforms are qualitatively depicted in Figure 2.3. Simulated waveforms will be discussed in Section 4.2, and presented in Figure 4.5.

Rest of the inverters are used for increasing the slew rate with a low power consumption. For this purpose, beginning of the output stage chain is a stacked inverter configuration with high V_T devices. These devices reduce power consumption dramatically while increasing the slew rate. 6^{th} stages uses also high V_T devices. 7^{th} and 8^{th} stage use standard V_T devices, to fully restore the slew rate of the signal. Setup yields high delay between inverters while decreasing the average current consumption of the voltage controlled oscillator.

The final stage of inverters output chain is NAND gate. Purpose of choosing last one as NAND gate is to control the VCO. If RESET input is set to V_{DD}, then the NAND operates as the last stage of the inverter chain. If it is set to the 0 V, then output of this stage blocks the chain and stops the oscillation.

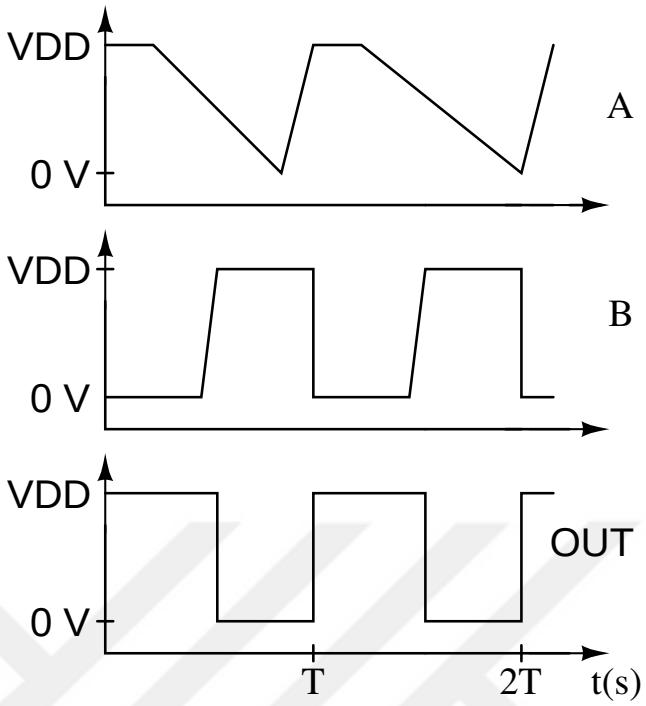

Figure 2.3. Expected behaviors of internal nodes of VCO

Frequency locking loop requires output clock and its non-overlapping complement. Apart from the inverters in the chain, there is one more inverter in the VCO. Last inverter designed with similar width and length as the 8^{th} stage has identical rise and low time as the generated clock signal. However, internal capacitance of devices must be sufficiently low enough to ensure non-overlapping of the generated signal with its reciprocal.

2.3. LOW POWER AMPLIFIER

The frequency generated in a frequency locked loop is only a function of the values of switched-capacitor C_{SW} and the reference resistor R_{REF} as shown in (2.3). Also in this topology the comparator block is replaced with a low power amplifier shown in Figure 2.4. The reason for this replacement is to amplify the corresponding difference between voltages of V_{IN-} and V_{IN+} nodes and to provide the VCO with a voltage that can generate the frequency calculated in (2.3).

Note that V_{IN-} has ripples due to the switching of the capacitance. The output resistance of the amplifier filters these ripples with the capacitance located in at its output.

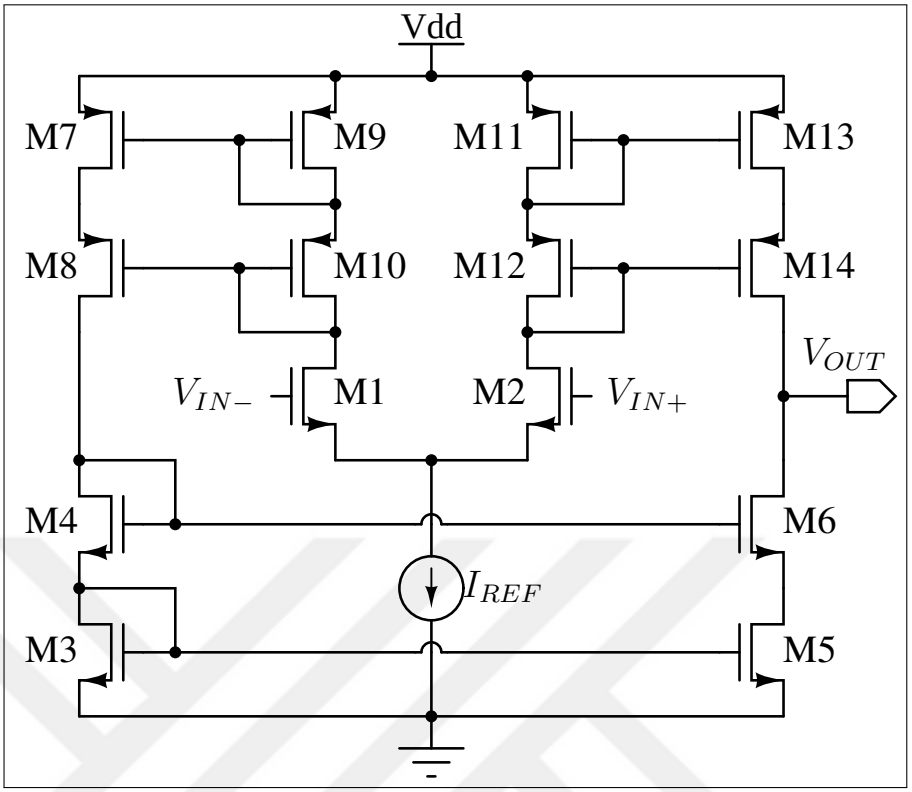

Figure 2.4. Operational transconductance amplifier

Output resistance of amplifier and C_{OUT} are act as a low-pass filter in this topology. Cut off frequency of the filter is also is also its pole location which is derived in loop gain analysis and shown in (2.8). Output resistance of the amplifier and C_{OUT} should be large enough to filter the signal. Therefore, output stage of the amplifier is cascoded. Reason for choosing it as a basic cascode over low voltage cascode is to avoid a bias circuit. Even though this choice reduces headroom of the output, this design doesn't require large output range.

Even in uncontrolled environments, temperature doesn't change much instantaneously. Therefore, amplifier does not have to respond to any high frequency variation. This enables the topology to have low bandwidth with a very low power consumption. Designing an amplifier with low-power consumption also has one more benefit in this work. Since large output resistance is required to decrease the cut-off frequency in low-pass filter, low currents on the output stage of the amplifier enables to achieve high output resistance value without increasing the channel lengths.

3. REFERENCE CIRCUITS

3.1. BAND-GAP VOLTAGE REFERENCE

In Chapter 2, need of a stable reference voltage that is insensitive to the line voltage, device parameters and temperature is mentioned. From (2.1), stable I_{REF} is possible only with a stable V_{IN-} and R_{REF}. Since R_{REF}'s temperature dependency can be minimized, insensitive V_{IN-} is critical for this application.

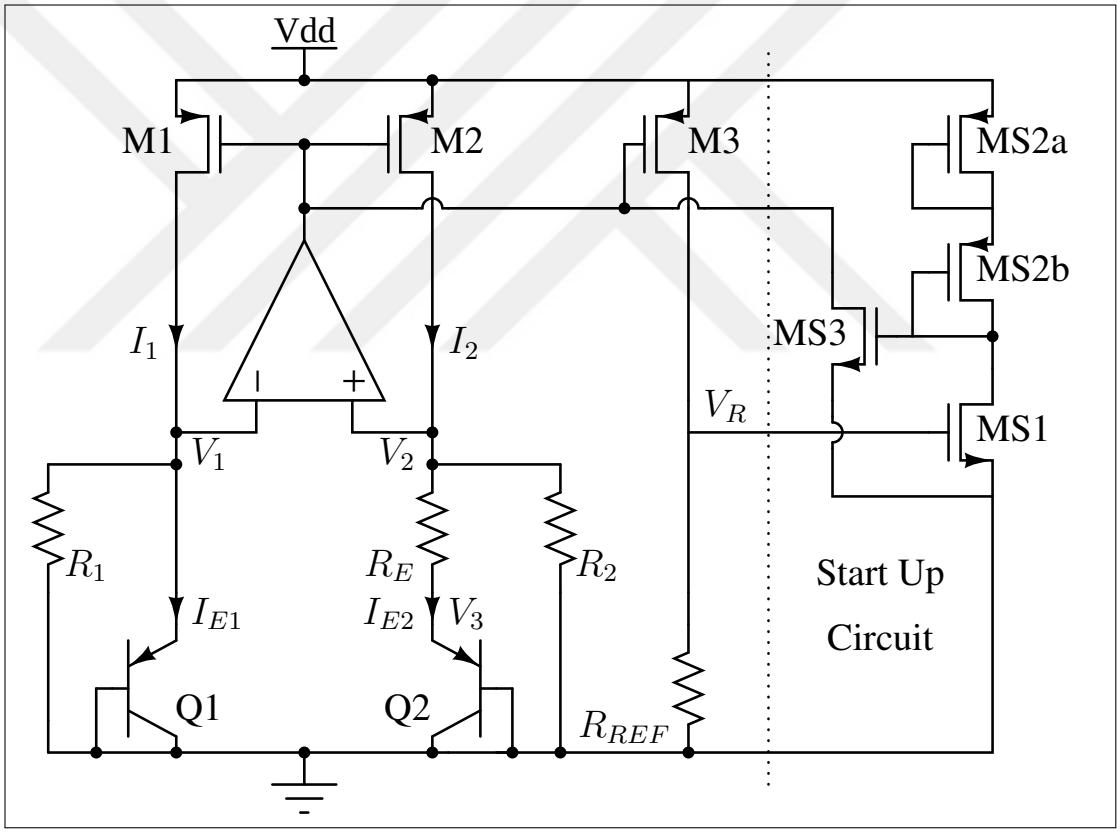

Figure 3.1. Band-gap voltage reference

For this application, a band-gap voltage reference circuit is suitable. Due to BGR circuit is self-biased, its supply sensitivity is minimized. However, BGR circuits require start-up circuit as shown in Figure 3.1 [16] to initiate voltage generation when V_{DD} applied.

There is no systematic mismatch since the reference devices (M1-M2-M3) are matched.

Accuracy of the output voltage therefore has been maintained. For temperature insensitivity BGR relies on silicons band-gap. Band-gap reference topology for generating V_{IN-} is demonstrated in Figure 3.1. BGR has a self-biasing feedback loop which equalizes I_1 and I_2 via matched M1 and M2 devices. Therefore, the high differential gain of the amplifier equalizes V_1 to V_2. BJT depicted in Figure 3.1 as Q1 and Q2 are act as a diode due to their base node being connected to the ground. Q2 has N parallel replicas of Q1. Emitter currents are described by

$$I_{E1} = \frac{I_S}{\alpha_F} e\Big(\frac{q}{kT} V_1\Big) \tag{3.1}$$

and

$$I_{E2} = \frac{N I_S}{\alpha_F} e\Big(\frac{q}{kT} V_3\Big) \tag{3.2}$$

where I_S is the intercept-current and α_F is the forward alpha. Since $V_1 = V_2$ is maintained by the amplifier, and R_1 and R_2 are matched resistors, I_1 and I_2 are equalized. Equating (3.1) and (3.2) results in

$$V_1 - V_3 = \left(\frac{kT}{q}\right) \ln N \tag{3.3}$$

Since $V_1 = V_2$, $V_1 - V_3$ also equals to $V_2 - V_3$. Dividing both by R_E results,

$$I_{E1} = I_{E2} = \frac{kT}{q} \frac{1}{R_E} \ln N \tag{3.4}$$

Adding V_1/R_1 to the emitter currents results in

$$I_1 = I_2 = \frac{V_1}{R_1} + \frac{kT}{q} \frac{1}{R_E} \ln N \tag{3.5}$$

I_1 and I_2 will be mirrored to M_3 with scale of S. Therefore, $I_3 = SI_1$. The reference voltage V_R defined as $V_R = R_{REF} I_3$. This yields,

$$V_R = S\left(\frac{R_{REF}}{R_2}V_1 + \frac{kT}{q}\frac{R_{REF}}{R_E}\ln N\right) \tag{3.6}$$

In (3.6), only emitter-base voltage V_1 and thermal voltage kT/q are temperature dependent variables. Temperature sensitivity of V_1 is negative. However, kT/q has positive temperature sensitivity. Therefore, these effects can be nullified by setting resistance values and BJT scaling factor N. Differentiating (3.6) with respect to T and equating it to zero results in

$$\frac{kT}{q}\frac{R_2}{R_E}\ln N = -\frac{dV_1}{dT}T \tag{3.7}$$

If this condition can be realized by the design, (3.6) turns into,

$$V_R = s\frac{R_{REF}}{R_2}\left(V_1 - \frac{dV_1}{dT}T\right) \tag{3.8}$$

Thermal sensitivity of the emitter-base voltage of BJT results in

$$\frac{dV_1}{dT}T = V_1 - V_{BG} - 3\frac{kT}{q} \tag{3.9}$$

where V_{BG} is band-gap voltage of the silicon, which is 1.12 V at room temperature $(T = 300°K)$. Combining all three equations above results in the following the condition of temperature insensitive V_R shown in 3.10 [17].

$$V_R = S\frac{R_{REF}}{R_2}\left(V_{BG} + 3\frac{kT}{q}\right) \tag{3.10}$$

3.2. BETA-MULTIPLIER CURRENT REFERENCE

In Section 2.3, low power amplifier topology is described. To achieve stable R_O, current flowing through the output of the amplifier should also be stable. Although it doesn't have a huge impact on the frequency, a need of a current reference in this topology is realized by a beta multiplier current reference. Since this topology is build around a self-biased loop, referenced current shows immunity to the line voltage variation.

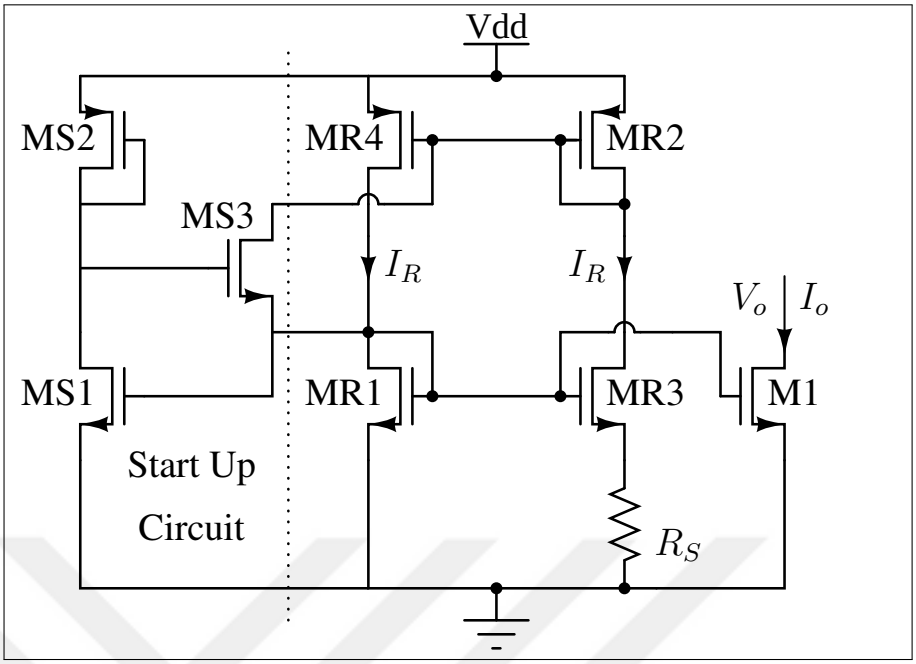

Figure 3.2. Beta-multiplier current reference

Circuit schematic shown in Figure 3.2 [18] is a single-device (non-cascoded) beta multiplier circuit topology. MR1, MR2, MR3, MR4 and R_S constitute the core of the beta multiplier circuit. Referenced current is mirrored through M1. MR2 and MR4 are matched device; MR2 mirrors current to MR4. This equates current flowing through the MR1 and MR3. Even though MR1 and MR3 operate in a with the same gate voltage level, gate-source voltage level of MR1 is greater than MR3 because the aspect ratio of MR3 is greater than MR1. Assuming these devices are operating in saturation, their gate-source voltages of these devices are,

$$V_{GS1} = \sqrt{\frac{2A_N I_R}{\mu_N C_{ox}(W/L)_{MR1}}} + V_{TN} \tag{3.11}$$

$$V_{GS3} = \sqrt{\frac{2A_N I_R}{\mu_N C_{ox}(W/L)_{MR3}}} + V_{TN} \tag{3.12}$$

Their threshold voltages are assumed equal even though existence of body effect in realization. From the Figure 3.2 voltage level of V_{GS1} is $I_R R_S$ higher than the V_{GS3}. Therefore,

$$V_{GS1} = V_{GS3} + I_R R_S \tag{3.13}$$

Solving this equation, I_R can be obtained as a function of aspect ratios and R_S as follows

$$I_R = \frac{2A_N}{\mu_N C_{ox} R_S^2} \left(\frac{1}{\sqrt{(W/L)_{MR1}}} - \frac{1}{\sqrt{(W/L)_{MR3}}} \right)^2 \tag{3.14}$$

Note that V_{DD} doesn't appear in (3.14). Therefore I_R's first order dependency on V_{DD} is zero. If M_1 stays in saturation region, current conducted through M_1 is,

$$I_o = \frac{(W/L)_{M2}}{(W/L)_{MR1}} \tag{3.15}$$

In a beta multiplier circuit, any device that conducts I_R has the same transconductance. Transconductances of such devices are mainly a function of R_S and aspect ratios. For example, if an NMOS devices that conducting $I_D = SI_R$ has a transconductance of:

$$g_m = \sqrt{2 \frac{W}{L} \frac{\mu_N C_{ox}}{A_N} S I_R} \tag{3.16}$$

Substituting (3.14) for I_R turns into,

$$g_m = \frac{2}{R_S} \sqrt{S \frac{W}{L}} \left(\frac{1}{\sqrt{(W/L)_{MR1}}} - \frac{1}{\sqrt{(W/L)_{MR3}}} \right) \tag{3.17}$$

As it can be seen from 3.17 [17], g_m is only function of R_S and aspect ratios.

4. DESIGN AND SIMULATIONS

4.1. BAND-GAP VOLTAGE REFERENCE CIRCUIT

4.1.1. Design Considerations

The design of the oscillator started with the generation of the reference voltage. From Chapter 2, because of generated frequency is mostly dependent on the current flowing through the R_{REF} and C_{SW}, generation of this voltage is important for this design. Selection of a voltage level is determined by 2 restrictions.

- Amplifier's compliance limit
- Low power consumption

Even though these are the main concerns, as it can be seen in (3.10), decreasing voltage level also requires larger resistors to be used in BGR block. By using this information, V_{REF} is chosen as 500 mV. This relaxes the input compliance of the amplifier's limit and with a 1 $\mathrm{M}\Omega$ R_{REF}, reference nodes conducts only 500 nA.

BGR block depicted in Figure 3.1 creates the V_{IN+} shown in Figure 1.5. Even tough it is not shown in Figure 3.1, M4 is other mirrored transistor that conducts current through C_{SW}.

4.1.2. Circuit Implementation

Device dimensions and area for BGR circuit and its start up circuit are given in Table 4.1. Initial start-up of the band-gap circuit limits the start-up time of the oscillator. In order to reduce the impact of the band-gap voltage generators impact to the start-up, aspect ratios of the $M_{1-2-3-4}$ are chosen as 3. Reason for choosing devices with huge width and lengths is to satisfy the 3σ specification in Monte Carlo simulations. In order to satisfy matching, these devices are placed as a common centroid form in layout.

Resistors used in BGR are chosen as internal components except R_{REF}. As mentioned in

Table 4.1. Band-gap voltage reference transistor sizes

Transistor Name	**Width** (μm)	**Length** (μm)	**Area** (μm^2)
$M_{1-2-3-4}$	60	20	1200
M_{S1}	2	0.18	0.36
$M_{S2A-S2B}$	0.22	3	0.66
M_{S3}	0.5	1.8	0.9

previous sections, R_{REF} is an external component with $\pm$ 10 ppm temperature coefficient and $\pm$ 0.05 percent resistance tolerance [14]. R_1, R_2 and R_E are chosen as P+ Poly resistors with a -110 ppm temperature coefficient and 290 $\Omega/\square$ sheet resistance. Resistor dimensions and area of BGR are shown in Table 4.2.

Table 4.2. Band-gap voltage reference's resistor sizes

Resistor Name	**Width**	**Length**	**Area**	**Value**
R_1-R_2	420 nm	2.98 mm	1251.6 μm^2	2.34 MΩ
R_E	420 nm	355.5 μm	149.3 μm^2	279 kΩ
R_{REF} [14]	2 mm	2 (5) mm	4 mm^2	1 MΩ

These transistor sizes and resistor values yield temperature compensated V_{REF} as shown in Figure 4.1. Under nominal conditions, V_{REF} value changes only up to 1.7 mV.

Voltage reference must also be immune for supply voltage variations. Even though temperature variation doesn't happen instantaneously, ripples on supply voltage may occur with very fast transients. Also noisy environments can cause supply voltage variation. Figure 4.2 shows the variation of reference voltage for line voltege sweep.

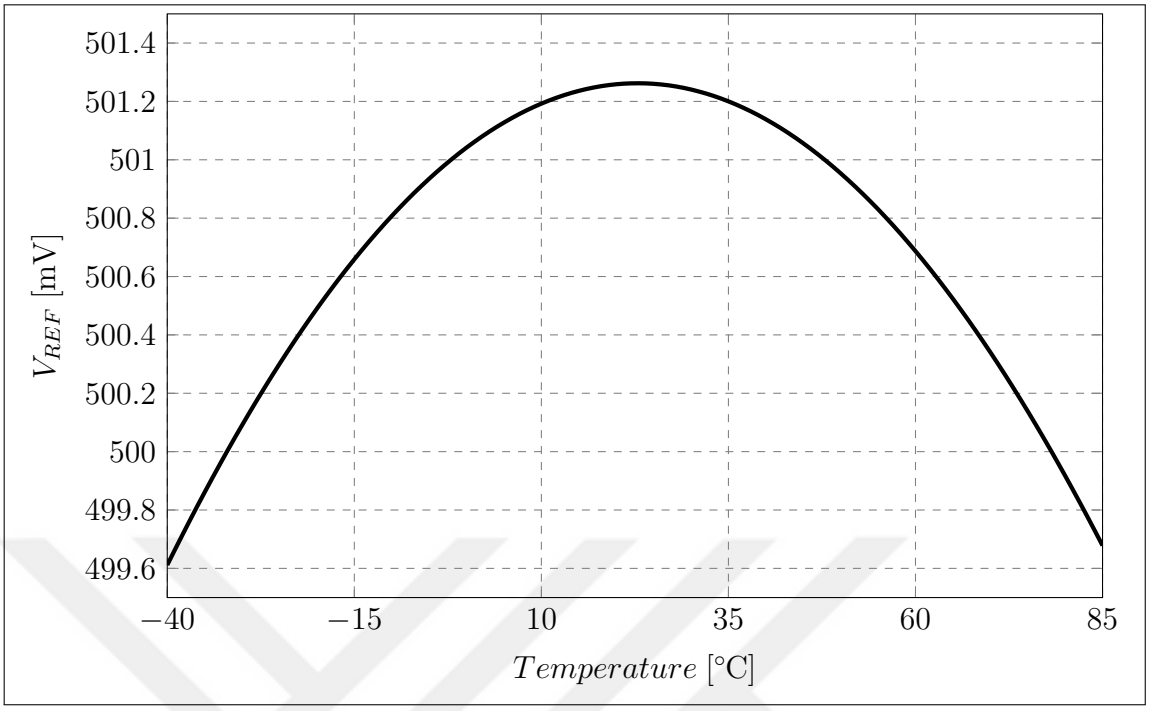

Figure 4.1. BGR's output voltage response across temperature range

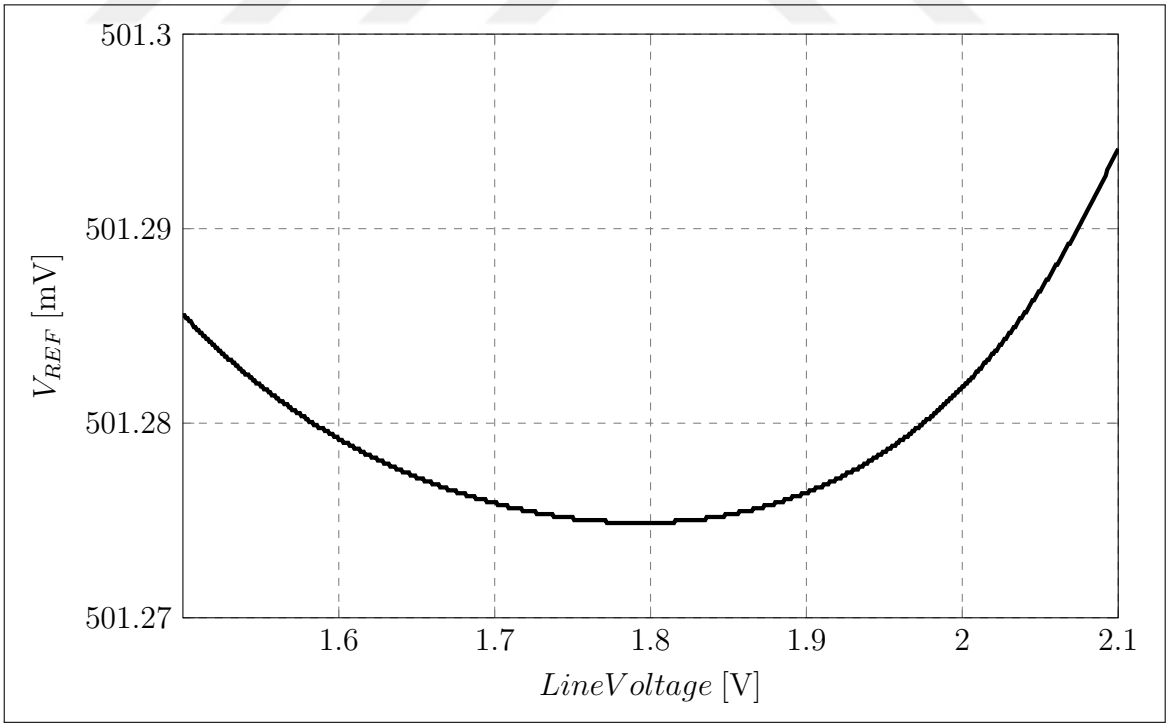

Figure 4.2. BGR's output voltage response for line voltage variation

Band-gap reference circuit is a self biased circuit. Therefore stability of the loop after start-up must be verified.

In stability analysis, loop is broken at the output of the amplifier and an AC small signal applied. Therefore both inverting and non-inverting nodes are added. Figure 4.3 illustrates the results of the loop gain. Stability analysis of the band gap reference yield 74 ° phase margin. For more accurate results, start-up simulation of band-gap circuit is simulated with the complete loop. Therefore it is mentioned in Section 4.4.

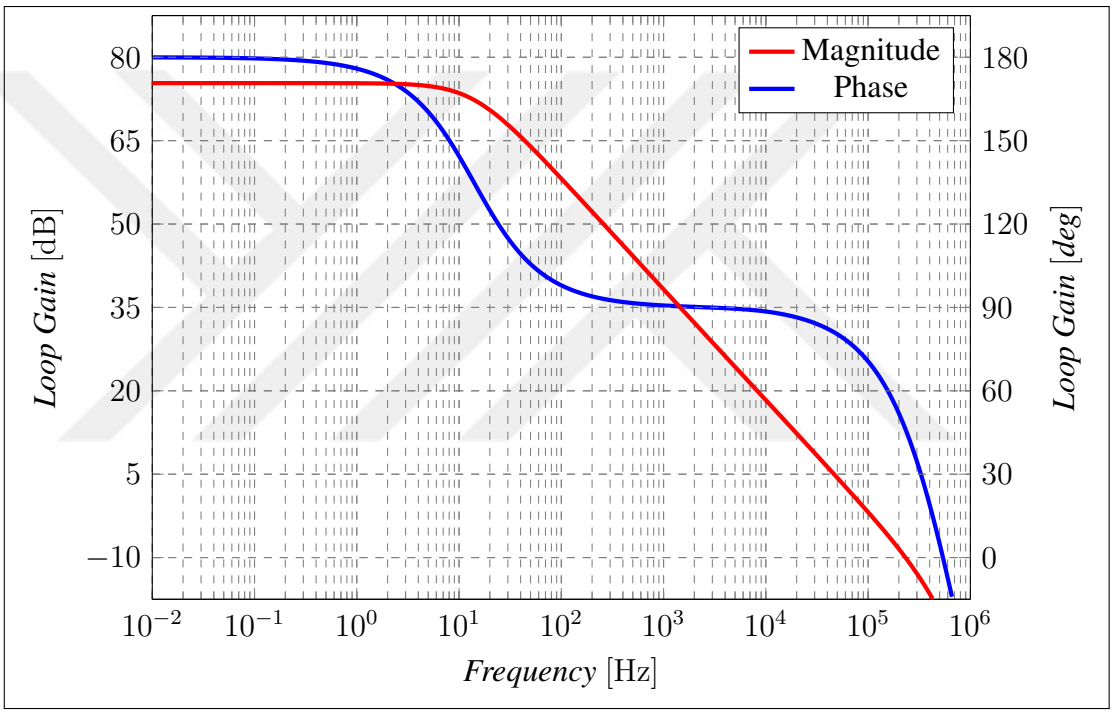

Figure 4.3. Stability simulation of band-gap reference circuit

In Figure 1.5, mirror devices must be identical and matched to generate same voltage on both inputs of the amplifier. However in production phase, mismatches may be seen between these devices. Monte Carlo simulation is set-up for both process and mismatch for band-gap circuit. Variation is chosen as 3 σ. Low-discrepancy sequence algorithm is used achieve best results with a 500 sample. Figure 4.4 illustrates the variation of V_{REF} for Monte Carlo mismatch simulation.

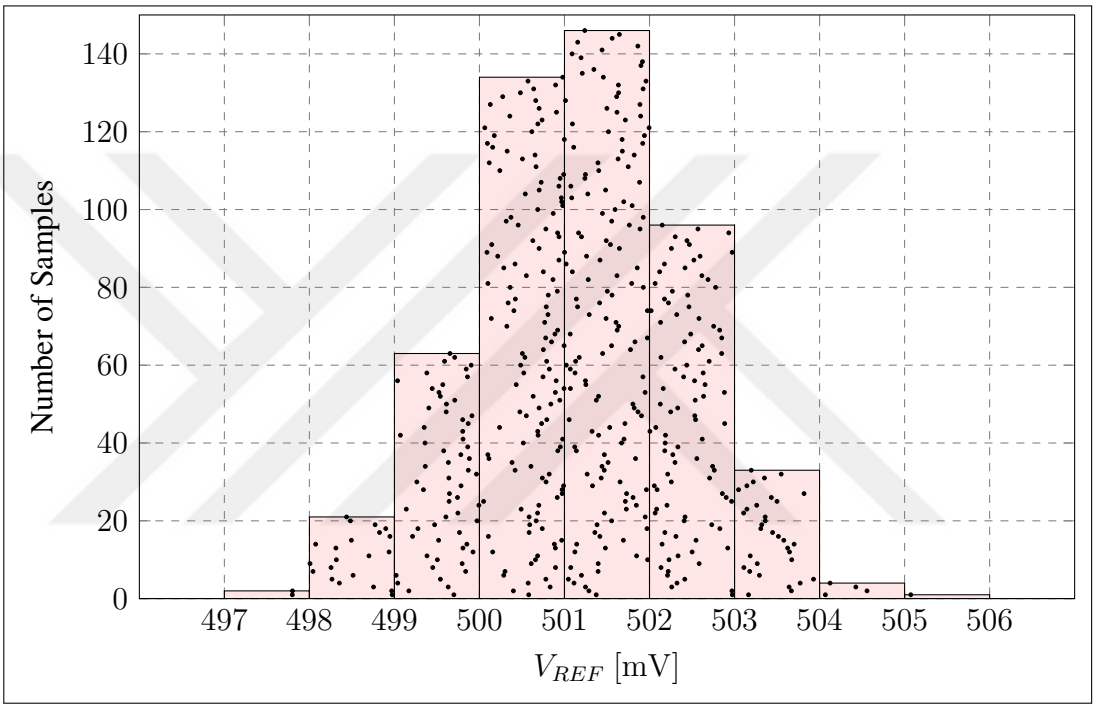

Figure 4.4. Reference voltage distribution of 500 samples in Monte Carlo simulation

As it can be seen from (3.10), V_{REF} is directly function of R_1 and R_2. Therefore, corners of resistors are the most effective circuit elements in BGR design. Because of V_{REF} generated in BGR is mostly dependent in resistor corners, due to V_{REF} distributions for corners with different resistor corners are given in Table 4.3.

Table 4.3. Band-gap reference output range across external resistor corners

Corner Condition	**Minimum Value** (mV)	**Maximum Value** (mV)
Typical	496	505
Worst Speed	404	412
Worst Power	610	620

4.2. VOLTAGE CONTROLLED OSCILLATOR CIRCUIT

4.2.1. Design Considerations

Voltage controlled oscillator design is driven by specification that stated in Table 1.2. Apart from specifications high slew rate of the output of the oscillator was one of the main consideration. In order to minimize the power consumption and shorten simulation time, frequency of the oscillator is set to minimum as possible while maintaining minimal frequency variation across all specified corners.

VCO depicted in Figure 2.2, is designed with 2 different type of devices with different V_T values.

4.2.2. Circuit Implementation

In this VCO design, current consumption of the transistors are aimed for a minimum while increasing the overall K_{VCO}.

With these specifications for the design in topology depicted in Figure 2.2 yields transistor sizes in Table 4.4.

Table 4.4. Voltage controlled oscillator's transistor sizes

Transistor Type	**Width** ($\mu\mathrm{m}$)	**Length** ($\mu\mathrm{m}$)	**Area** ($\mu\mathrm{m}^2$)
High V_T Devices	220	1.8	0.396
Standard V_T Devices	220	0.18	0.0396

Simulation results of nodes marked in Figure 2.2 are shown in Figure 4.5. As expected from Figure 2.3 in Section 2.2, slew rate of the signal increases with stages.

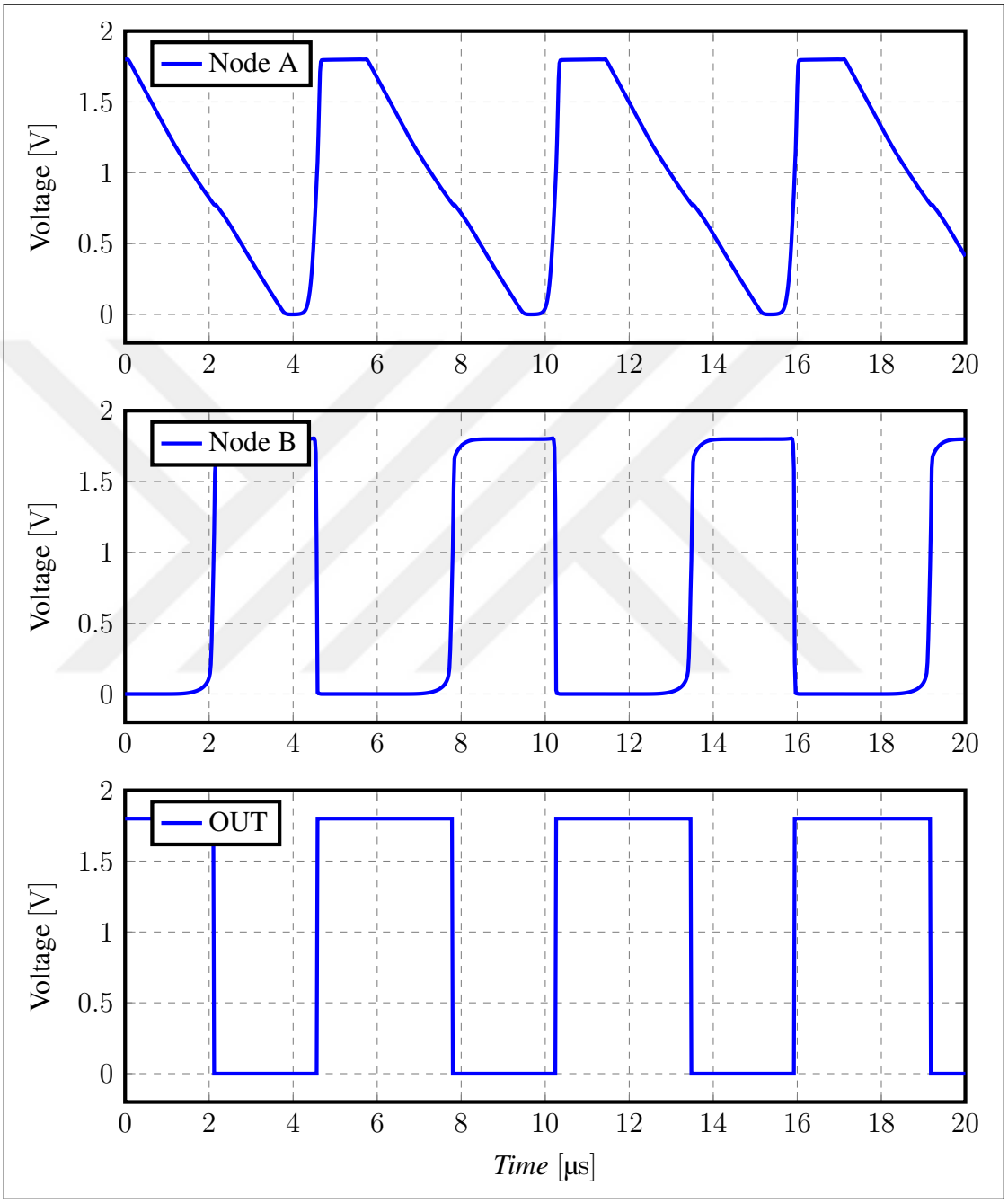

Figure 4.5. VCO's response within supply range

Length values given in Table 4.4 yields sufficiently high K_{VCO} shown in Figure 4.6. This allows us to operate low input voltages for VCO which yields low current consumption for the overall design.

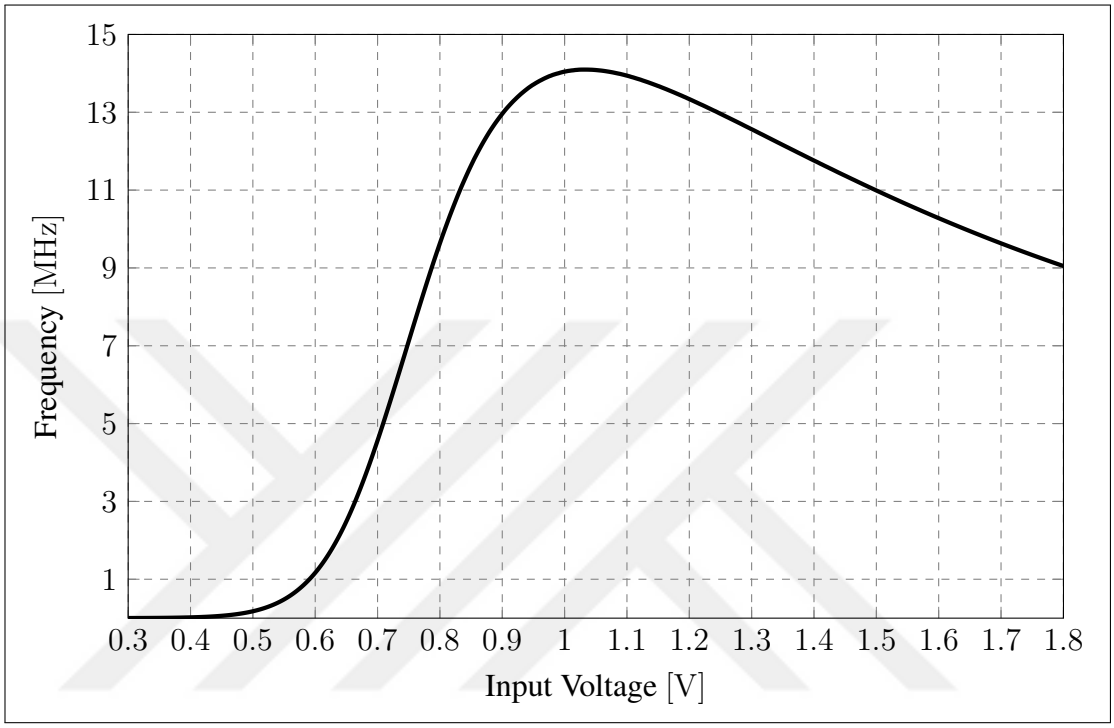

Figure 4.6. VCO's frequency response within supply range

VCO's measured frequency response with a given supply is shown in Figure 4.6. Reason for non-monotonicity of K_{VCO} is the result of the decreasing current consumption of the VCO. Increasing width of the transistors in the VCO would increase the monotonicity. However this would also increase the short-circuit current and increase the power consumption. Therefore design of VCO shaped around these concerns. Even though operation region is around 400 mV and 600 mV, design must care for the input voltage of the VCO should not suppress 1V.

For further investigation of voltage controlled oscillator, percentage of frequency change for supply sweep is shown in Figure 4.7. In specifications, supply variation is defined as ± 5 percent. With 1.8 V supply voltage, VCO's frequency variation for this variation is derived as ± 2.1 percent.

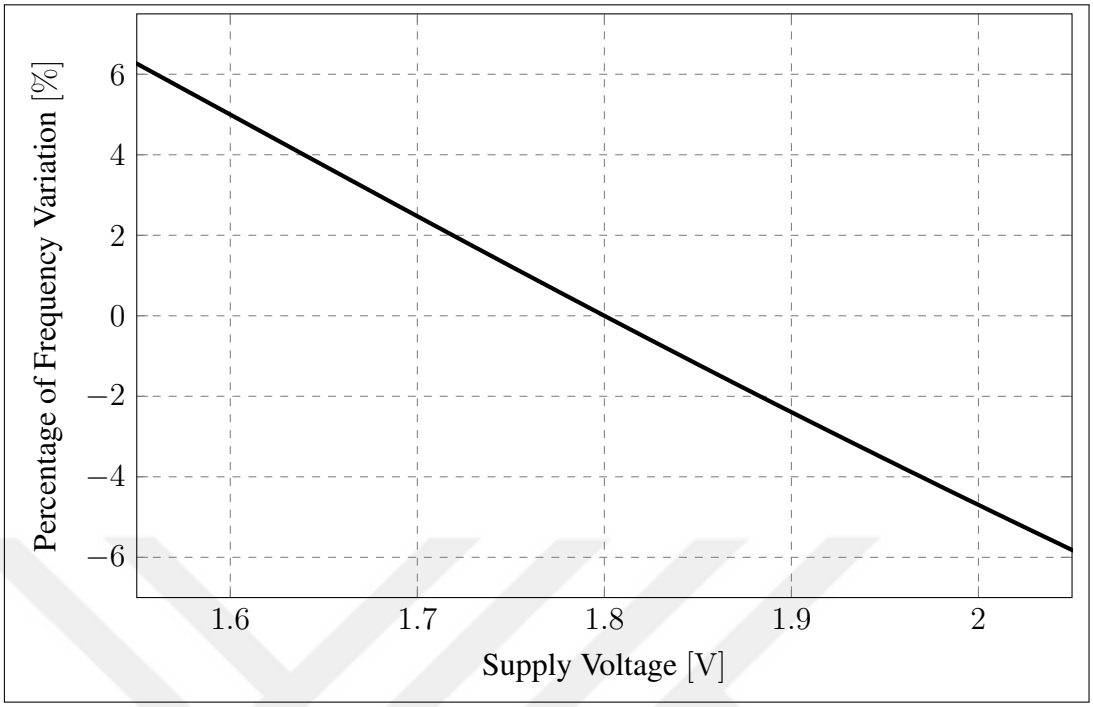

Figure 4.7. VCO's frequency variation with supply variation

4.3. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

4.3.1. Design Considerations

With a stable input voltage received from BGR, design continued with amplifier of the frequency-locked loop. Compared to the relaxation oscillator, this design replaces comparator with a low bandwidth amplifier. In this topology amplifier acts as a low pass filter as well. OTA needs to have high output resistance. But also should not put weight on overall design's power budget.

Symmetrical OTA topology depicted in Figure 2.4 is used in this design. At the output of the amplifier, cascoded devices are used in order to maximize the output resistance. In order to avoid additional bias generation, cascoded devices are not connected as low-voltage cascode. Due to expected output voltage is around 550 mV, even with basic cascode we have enough headroom on the output stage.

4.3.2. Circuit Implementation

Design of OTA is aimed high R_{OUT} with low power consumption. With these considerations, transistor sizes for this amplifier is given in Table 4.5.

Table 4.5. Operational transconductance amplifier's transistor sizes

Transistor Name	**Width** (µm)	**Length** (µm)	**Area** (μm^2)
M_{1-2}	4	1	4
$M_{3-4-5-6}$	4.4	5	22
$M_{7...14}$	10	5	50

Even though design aims for high gain and output resistance, simulation results are not always reliable for accurate measurements. In order to protect design from simulator's miscalculations and corner conditions, gain of amplifier is ramped up as much as it can be. From Figure 4.8, open loop DC gain of the OTA is measured as 104 dB.

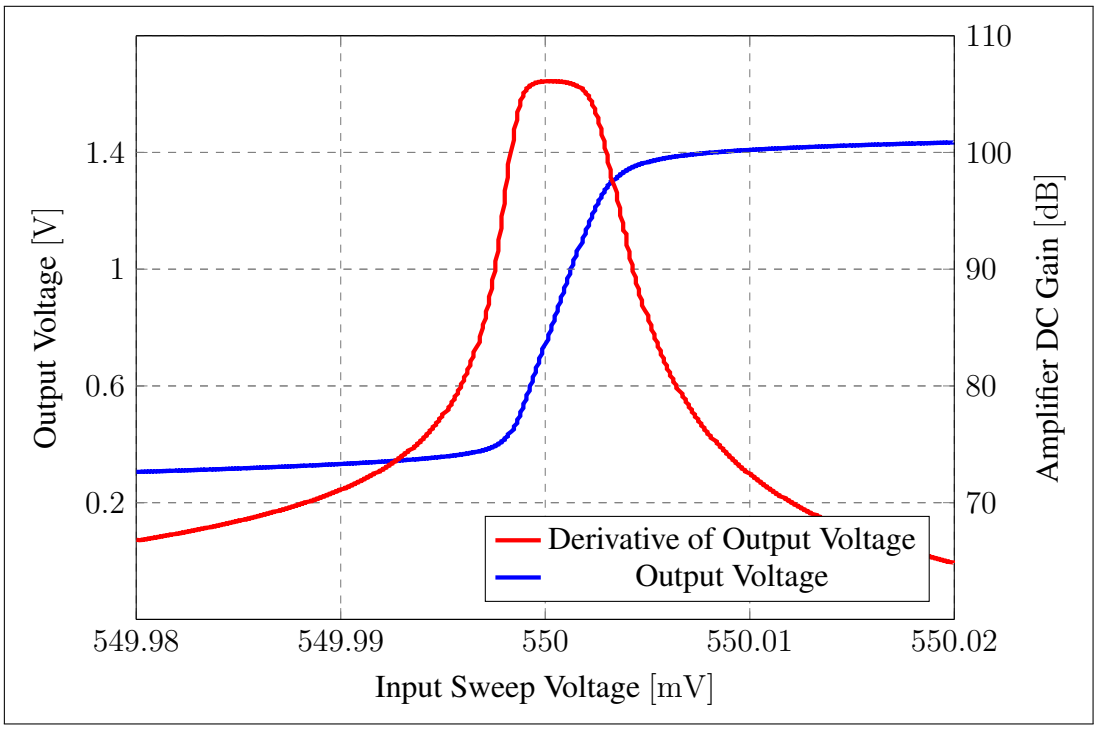

Figure 4.8. Open-loop DC transfer characteristic of amplifier

After achieving high gain, stability and start-up behavior of the OTA is verified. From Figure 4.9, phase margin of the OTA is found as 87 °. Also magnitude of the loop gain is measured as 104 dB as found as open loop simulation.

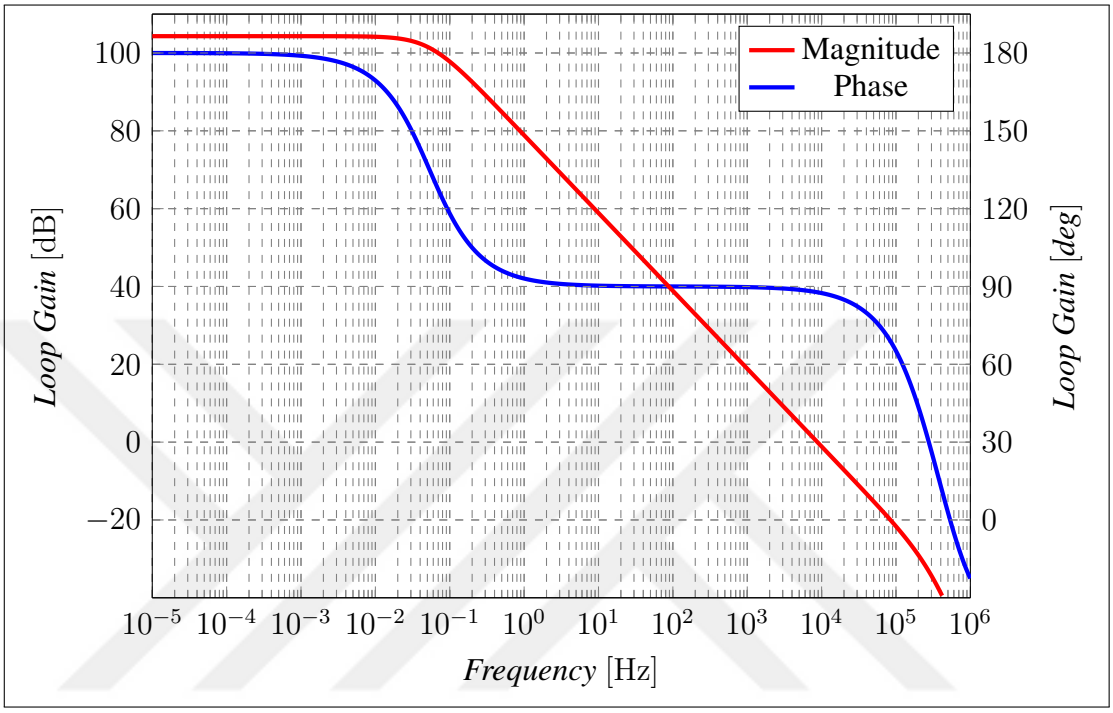

Figure 4.9. Stability simulation of operational transconductance amplifier

Start-up simulation is held with increasing the supply voltage to 1.8 V with 10 µs rise time. From Figure 4.10, around 20 µs beta-multiplier current reference settles to 100 nA. Total current consumption of the OTA after the output voltage rises and settles to desired voltage level is around 200 µs.

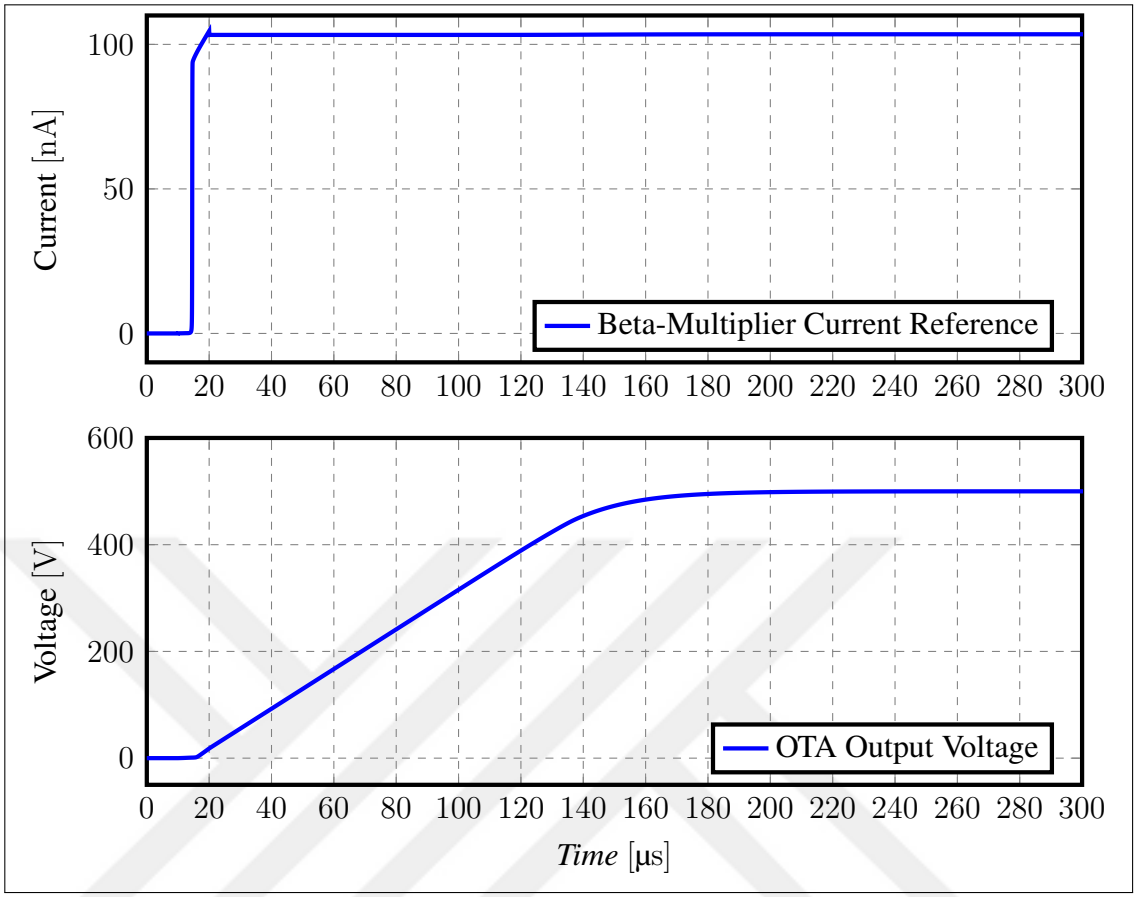

Figure 4.10. Starting behavior of beta-multiplier and OTA

4.4. SWITCHED-CAPACITOR FREQUENCY LOCKED LOOP

4.4.1. Design Considerations

In Chapter 2, overall frequency of the oscillator is derived as a function of R_{REF} and C_{SW} in (1.2). R_{REF} is an external resistor therefore its resistor value can be protected by well adjusted on chip power distribution network parasitic. Adjusting the C_{SW} capacitance and protecting it is defines the frequency integrity of the oscillator. Therefore, switches on the C_{SW} are need to be well adjusted. They need to be small sized in order to decrease charge injection and intrinsic capacitance. However, need to be large enough to eliminate leakage current. With these considerations device sizes of the switches shown in Figure 1.5 are chosen as follows:

Main principle of this design is to equalize the impedance of the switched capacitor to the resistor's with a clock input from the VCO. But, due to the switching activity ripple occurs

Table 4.6. Switch transistor sizes

Switch Name	**Width** (nm)	**Length** (μm)	**Area** (μm^2)
Upper Switch	220	1.8	0.396
Lower Switch	220	0.5	0.11

on the positive input side of the amplifier. The ripples can be damped down by choosing C_{IN+} significantly larger than C_{SW}.

4.4.2. Circuit Implementation

Frequency locked loop has 2 poles. Pole locations are defined in Section 2.1. (2.8) and (2.9) show the location of dominant and non-dominant poles. In order to separate these poles to achieve better stability results, a high R_{OUT} is needed. For the non-dominant pole side, since R_{REF} is already chosen as 1M Ω only C_{IN+} can be changed. C_{SW} is chosen as maximum capacitance value that PDK allows. Which yield 1.84 pF. From (1.2), frequency output of the loop can be calculated around 540 kHz.

Reason for choosing large capacitor is to make it more insensitive to the production processes. Since there is no frequency is specified, this independence have been used in choosing bigger capacitors. Yet, bigger capacitors come with a dramatically increased total area. With a R_{REF} and C_{SW} in hand, for this design ratio of C_{SW}/C_{IN+} is chosen as,

$$C_{SW}/C_{IN+} = 0.1 \tag{4.1}$$

In order to verify the stability of this loop, we need AC small signal analysis. However since this circuit is an oscillator and controlled by a switched capacitor circuitry, 1.5 need to be converted from discreet time system to continuous time domain.

In order to turn the system in to continuous time domain, switching parts must be changed in to their corresponding counterparts. Therefore switching capacitor and switches around it are replaced with a voltage controlled current source. In addition, VCO block is removed. Transfer function of the loop is already derived in (2.7). In order to emulate switch capacitor

and VCO, voltage controlled current source is defined as follows:

$$I = C_{SW} V_{REF} K_{VCO} V_{OUT} \tag{4.2}$$

As a result, Figure 1.5 turns into Figure 4.11.

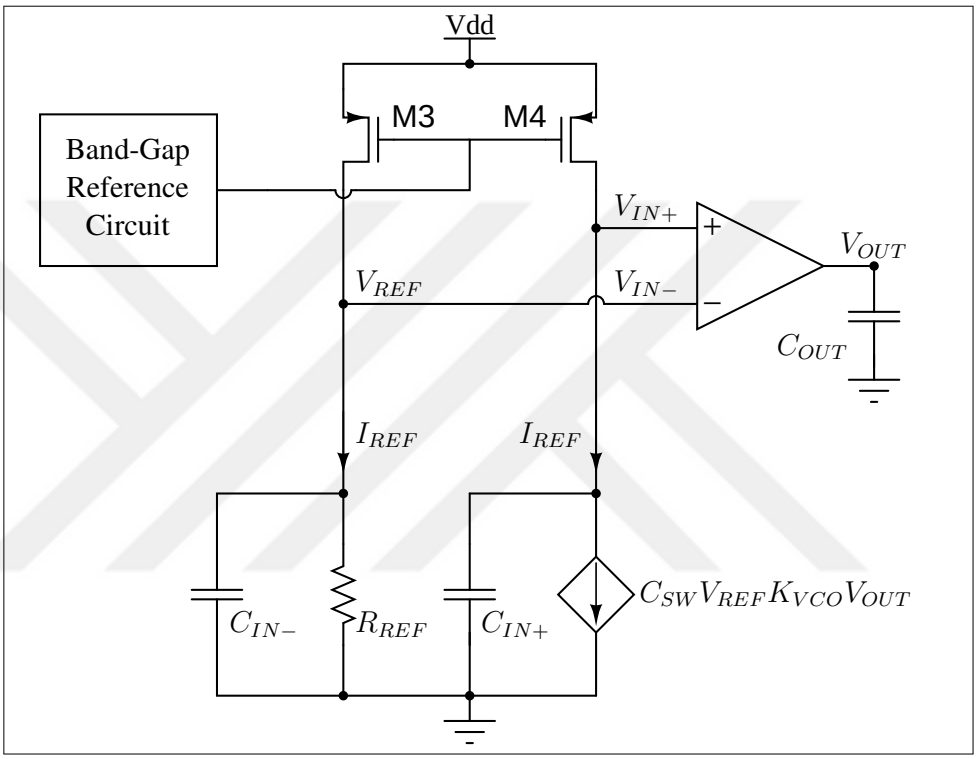

Figure 4.11. Continuous time equivalent of the frequency-locked-loop

In (4.2), $C_S W$ and V_{REF} already known. K_{VCO} is derived from 4.6 and V_{OUT} is generated by the OTA. Stability of the system is shown in Figure 4.12. Even though Figure 4.12 gives us

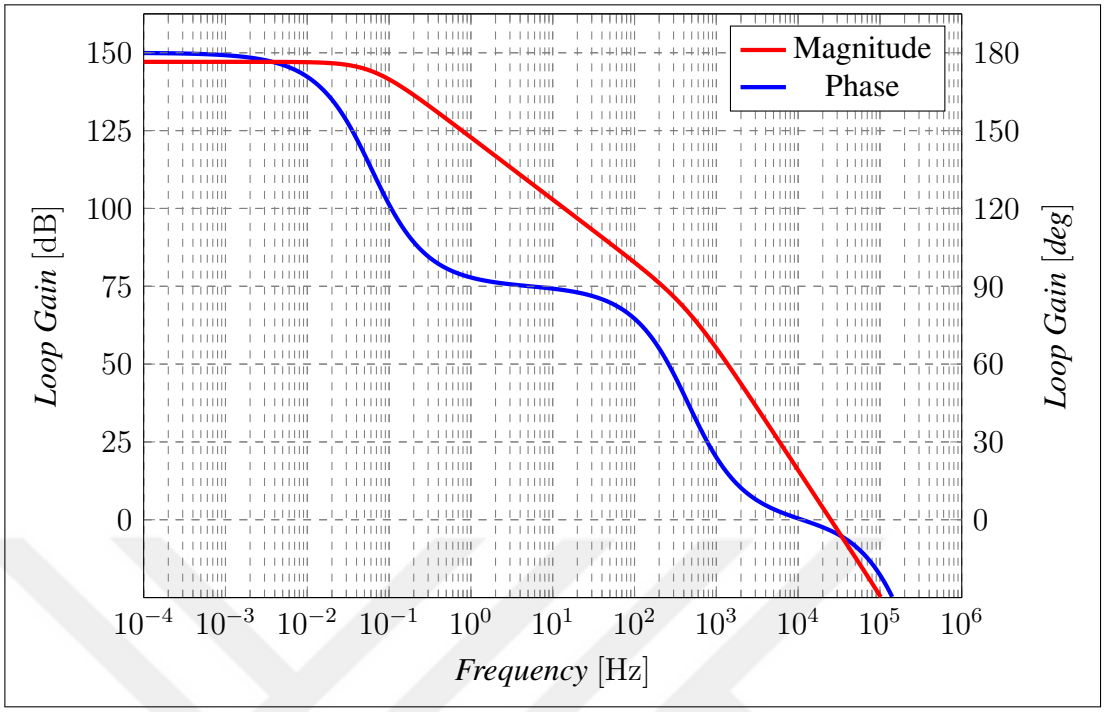

Figure 4.12. Stability simulation of frequency-locked-loop

initial stability results of the system, stability is verified with a start-up simulation. Supply voltage is applied with 10 µs rise time. Transient response of the loop is given in Figure 4.13

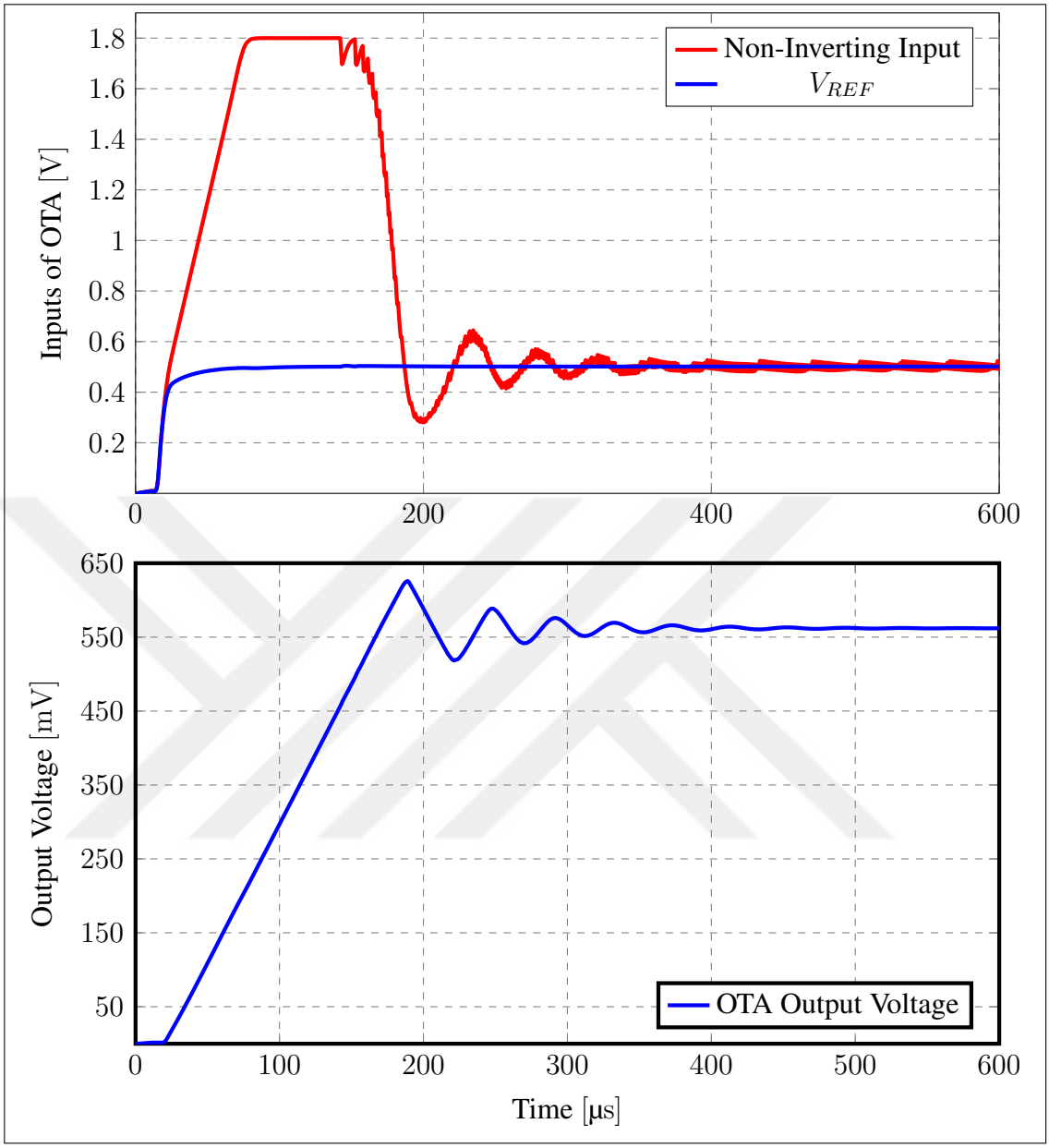

Figure 4.13. Starting behavior of frequency-locking-loop

After V_{REF} is generated, OTA is starting to react. However due to its bandwidth is limited, frequency searching can't start until 200 µs. Then, frequency starts to settle. Total settling time is measured as 600 µs. Main reason for slow response of the system start-up is caused by low-power amplifier. As it can be seen in Figure 4.13, almost 150 µs is required to reach around 500 mV output voltage. When output voltage reaches a certain level, frequency settles down around 600 µs in typical conditions. Maximum over corner settling time is measured as 1.1 ms.

4.4.3. Corner Simulation

In order to simulate the effect of device characteristics distribution in the process, this design is tested under all design, temperature and static line voltage corners shown in Table 4.7. For PDK parameters, 3 σ variation is selected.

Table 4.7. Overall design corner simulation setup

Temperature (°C)		-40	27	85	
Line Voltage (V)		1.71	1.8	1.89	
R_{REF} (Ω)		999500	1000000	1000500	
BJT		Typical	Worst Power	Worst Speed	
MOSFET	Typical	Worst Power	Worst Speed	Worst One	Worst Zero
Resistor		Typical	Worst Power	Worst Speed	
Total Corner Count = 1215					

From the corner simulation results, temperature coefficient is measured only in typical design corners with only temperature variant. Frequency measurements are given in Table 4.8.

Table 4.8. Frequency variation across temperature corners

Temperature (°C)	Frequency (kHz)
-40	546.251
27	545.496
85	544.846

Temperature coefficient for overall specified temperature range is measured as 20.6 ppm/°C.

After temperature coefficient measurement, oscillators line voltage sensitivity is measured. Frequency results in specified line voltage values are shown in Table 4.9.

Table 4.9. Frequency variation across line voltage corners

VDD (V)	Frequency (kHz)
1.71	546.019
1.8	545.496
1.89	545.039

From Table 4.9, line voltage sensitivity for overall specified voltage range is calculated as 1 percent/V.

Afterwards frequency sensitivity of the design has to be verified under all corners shown in Table 4.7 to verify frequency variation specification defined in Table 1.2. According to the specifications, frequency of the oscillator should not change more than $\pm$ 0.65 percent from the nominal frequency. For 545.496 kHz nominal frequency, maximum allowed frequency variation should not suppress 3.545 kHz.

Table 4.10. Frequency variation across all design corners

	Frequency (kHz)	Percentage of Change (%)
Maximum Value	548.760	0.598
Nominal Value	545.496	0
Minimum Value	542.007	-0.639

Table 4.10 verifies that maximum frequency variation doesn't surpass $\pm$ 0.65 percent.

Another important specification to verify in this design is power consumption. Design specifications stated in Table 1.2 is limits the total power consumption of the all blocks in the design. Furthermore, in order to illustrate design performance, only core blocks of the oscillator is calculated. Chosen core blocks in this design are following:

- Voltage controlled oscillator
- Low power amplifier
- External resistor and switch capacitor

Across all temperature range, total power consumption and core blocks power consumption is illustrated in Table 4.11. In specifications, total power consumption is limited by 20 µW. Therefore in worst case, 12 µW surplus in the power specification.

Table 4.11. Power consumption of the system across temperature points

	Total Power Consumption (µW)	Core Power Consumption (µW)
Maximum	8.05	3.50
Nominal	5.40	2.42
Minimum	3.13	1.17

In addition to the power consumption of the system, another performance metric is energy consumption of the system per clock cycle. This performance metric enables us to compare power consumption specification of the system with other designs independent of the frequency.

Across all temperature range, total energy per cycle consumption of the system and the core blocks are given in Table 4.12.

Table 4.12. Energy consumption per cycle of the system across temperature points

	Total Energy Consumption per Cycle (pJ/Cycle)	Core Energy Consumption per Cycle (pJ)
Maximum	14.8	6.46
Nominal	9.90	4.43
Minimum	5.72	2.14

4.4.4. Monte Carlo Simulation

The last part of the verification of the switched-capacitor frequency locked oscillator was Monte Carlo simulation for both process and mismatch. Corners that are defined in Table 4.7 are also defined for the Monte Carlo simulations.

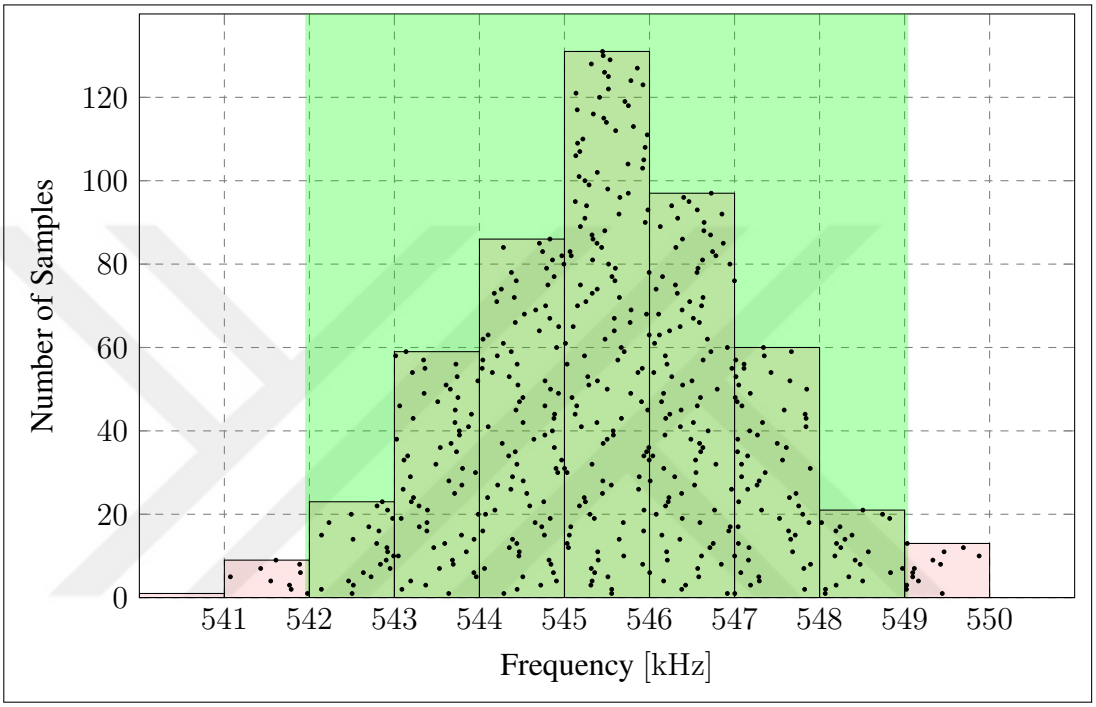

Figure 4.14. Frequency distribution of 500 samples in Monte Carlo simulation

Monte Carlo simulation is held with pseudo-random distributed 500 samples. Green area shown in Figure 4.14 indicates the specified $\pm$ 0.65 percent frequency band specified in Table 1.2.

In this design 96.2 percent yield is achieved.

5. LAYOUT

A layout of an analog block is as important as the design of it. Even though design looks great on the simulator, a bad layout configuration may cause the design go out of specifications.

Because of frequency of the oscillator is function of the C_{SW}, it is important to eliminate any semiconductor manufacturing process variations with proper layout techniques. Another factor that has impact on the C_{SW} is routing between switches and capacitor. In order to reduce the routing capacitance between C_{SW} and switches, both of the switches are placed nearby to the C_{SW}. Also routing is done by minimum width and 6th metal layer. Therefore capacitance between substrate and routing metal decreased as much as possible.

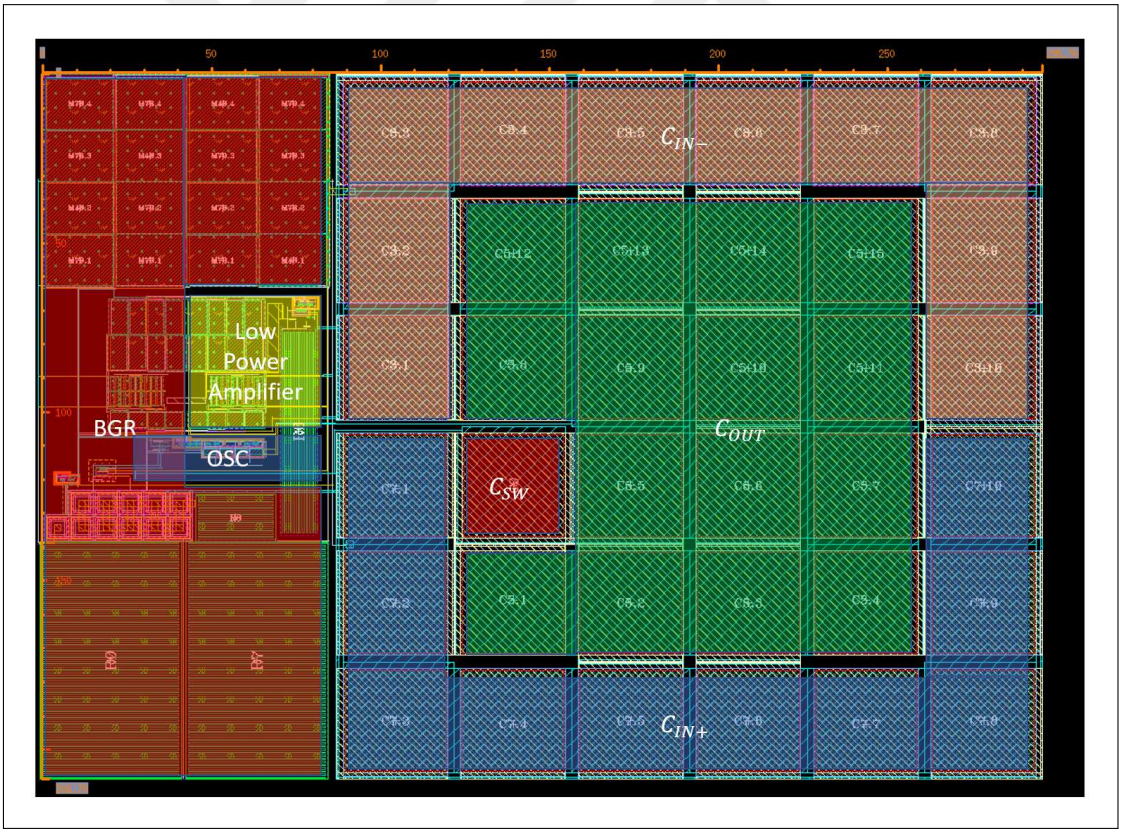

Figure 5.1. Layout

Apart from the manufacturing process variations, there is no ESD protection on the external resistor. In order to prevent leakage current to the reference node, ESD protection is removed.

Dimensions of the oscillator design shown in Figure 5.1 are 295.76 μm x 208.75 μm. Therefore total area is calculated as 0.0617 mm^2.

6. CONCLUSION

A switched-capacitor frequency locked loop oscillator has been presented. It has very low temperature coefficient, wide temperature range and marginally higher frequency. Besides, its small area and competitive energy consumption per cycle enables the design to be find use in block designs like phase locked-loop. Moreover in system level internet of things communication systems like Bluetooth or real time clock applications of mobile systems.

Table 6.1. Comparison of performance summary

	This Work	[12]	[19]	[20]
Process (nm)	180	180	180	90
Frequency (kHz)	545.5	70.4	122	100
Temperature Coefficient (ppm/°C)	20.59	34.3	327	104.6
Temperature Range (°C)	-40 85	-40 80	-20 100	-40 90
Line Sensitivity (%/V)	1	0.75	0.09	9.4
Power Consumption (W)	5.40 µ / 2.42 µ	110 n	190 n	280 n
Energy/Cycle (pJ/Cycle)	9.90 / 4.43	1.56	5.76	2.80
Start-up Time (s)	600 µ	2.5 m	N/A	10 µ
Area (mm^2)	0.06	0.26	0.03	0.12

As mentioned in Chapter 1.4 this work is based on topology represented on [12]. Improvements to decrease tempereture dependency of this design yield 14 ppm/°C improvement on temperature coefficient. This also allowed this design to comply with the specified maximum frequency variation of 0.65 percent.

This design also have huge improvement on start-up time compared to its predecessor. Even though 600 µs start-up time satisfies specifications, proposed architecture doesn't fit for systems require fast start-up options. In the system level this issue could be solved by adding an extra fast but inaccurate oscillator. Therefore 600 µs idle time could be decreased to few cycles.

This design is also has significant small die area compared to the predecessor design [12]. Moreover, with a competitive energy consumption per cycle could be decreased by increased frequency without sacrificing temperature coefficient.

REFERENCES

1. Schubert Jr TF, Kim EM. *Fundamentals of electronics: Book 4 oscillators and advanced electonics topics*. London: Morgan and Claypool Publishers; 2016.

2. Shu G, He W, Zhang L, Yin H, Zhao J, Cross AW, et al. Design of a sub-terahertz oscillator with high output power. *2016 IEEE 9th UK-Europe-China Workshop on Millimetre Waves and Terahertz Technologies (UCMMT) on*; 2016: 126–127.

3. Prasad D, Singh S, Kumari A, Srivastava M. A novel digitally programmable quadrature oscillator using DCVDGA. *2017 International Conference on Applied System Innovation (ICASI)*; 2017: 1391–1394.

4. Reddy N, Pattanaik M, Rajput S. 0.4V CMOS based low power voltage controlled ring oscillator for medical applications. *TENCON 2008 - 2008 IEEE Region 10 Conference*; 2008: 1–5.

5. Asano H, Hirose T, Miyoshi T, Tsubaki K, Ozaki T, Kuroki N, et al. A fully integrated, 1-μs start-up time, 32-MHz relaxation oscillator for low-power intermittent systems. *2016 14th IEEE International New Circuits and Systems Conference (NEWCAS)*; 2016: 1–4.

6. Martinez B, Monton M, Vilajosana I, Prades JD. The power of models: Modeling power consumption for IoT devices. *IEEE Sensors Journal*. 2015;15(10):5777–5789.

7. Craninckx J, Steyaert M. Low-noise voltage-controlled oscillators using enhanced LC-tanks. *IEEE Transactions on Circuits and Systems II: Analog and Digital SignalProcessing*. 1995; 42(12):794–804.

8. Hershenson MDM, Hajimiri A, Mohan SS, Boyd SP, Lee TH. Design and optimization of LC oscillators. *1999 IEE/ACM International Conference on Computer-Aided Design. Digest of Technical Papers (Cat. No.99CH37051)*; 1999: 65-69.

9. Razavi B. *RF Microelectronics*. New Jersey: Prentice Hall; 2012.

10. Tiebout M. Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS. *IEEE Journal of Solid-State Circuits*. 200; 36(7):1018–1024.

11. Agarwal D, Singh YK. Low power, low phase noise current reuse 2.45 GHz LC oscillator with MOS resistor. *2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE)*; 2017: 444–448.

12. Choi M, Jang T, Bang S, Shi Y, Blaauw D, Sylvester D. A 110 nW resistive frequency locked on-chip oscillator with 34.3 ppm/°C temperature stability for system-on-chip designs. *IEEE Journal of Solid-State Circuits*. 2016;51(9): 2106–2118.

13. Choi M, Lee I, Jang TK, Blaauw D, Sylvester D. A 23pW, 780ppm/°C resistor-less current reference using subthreshold MOSFETs. *ESSCIRC 2014-40th European Solid State Circuits Conference (ESSCIRC).* IEEE; 2014: 119–122.

14. Susumu Co L. Metal Thin Film Chip Resistors; 2019 [cited 2019 28 June]. Available from: https://www.mouser.com.tr/datasheet/2/392/n catalog partition01 en-1140338.pdf.

15. Lim QSI, Kordesch AV, Keating RA. Performance comparison of MIM capacitors and metal finger capacitors for analog and RF applications. *2004 RF and Microwave Conference (IEEE Cat. No.04EX924)*; 2004: 85–89.

16. Banba H, Shiga H, Umezawa A, Miyaba T, Tanzawa T, Atsumi S, et al. A CMOS bandgap reference circuit with sub-1-V operation. *IEEE Journal of Solid-State Circuits.* 1999; 34(5):670–674.

17. Cilingiroglu U. *Analog integrated circuit design by simulation: Techniques, tools, and methods.* Columbus: McGraw-Hill Education; 2019.

18. Razavi B. *Design of analog CMOS integrated circuits*. Columbus: McGraw-Hill Education; 2016.

19. Dai S, Rosenstein JK. A 14.4 nW 122 KHz dual-phase current-mode relaxation oscillator for near-zero-power sensors. *Custom Integrated Circuits Conference (CICC)*; 2015: 1–4.

20. Tokairin T, Nose K, Takeda K, Noguchi K, Maeda T, Kawai K, et al. A 280 nW, 100 kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme. *2012 Symposium on VLSI Circuits (VLSIC)*; 2012: 16–17.