

CMOS INTEGRATED SELECTOR WITH OPTICAL RECEIVER AND
PHOTOVOLTAIC SUPPLY



by
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CMOS INTEGRATED SELECTOR WITH OPTICAL RECEIVER AND
PHOTOVOLTAIC SUPPLY

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ABSTRACT

CMOS INTEGRATED SELECTOR WITH OPTICAL RECEIVER AND PHOTOVOLTAIC SUPPLY

Fabricated silicon wafers are subjected to a parametric test for identifying the ones qualified for the subsequent sort test. Also known as “scribe test”, this test is performed by measuring a few basic MOSFET parameters such as threshold voltage, saturation drive current and/or channel leakage current on monitor devices placed inside scribe lines or dedicated dies. Electrical access to these devices is established by mechanical means involving stepping, micrometric alignment and contacting, which necessitate not only an expensive stepper/aligner but also a customized probe card. To overcome this expensive problem, a wireless channel-leakage monitor is proposed and got funded by TUBITAK. In this thesis, a sub-circuit for this channel-leakage monitor is designed. The integrated selector supplied by photovoltaic cells enables the communication between the silicon and the antenna and selects either PMOS or NMOS version of the monitor to be used. To this end, a compact transimpedance amplifier followed by a peak detector and a switch is designed. The circuit has no external power supply since it harvests its energy from photovoltaic cells. By enabling/disabling the flickering light source with a certain illuminance and frequency besides the ambient room light, the switch creates a 1-bit signal for the following channel-leakage monitor. With the funding from TUBITAK and using UMC 0.18 μm design kit, 2 test chips have been taped out and measured. This thesis covers all the design procedures, simulation and measurement results of this integrated selector.

ÖZET

OPTİK ALICI VE FOTOVOLTAYİK BESLEMeye SAHİP BİR CMOS ENTEĞRE SEÇİCİ

Üretilen silikon pullar, ayırma testine girebilecek olanların belirlenmesi için bir parametrik teste tabi tutulurlar. “Çizik testi” olarak da bilinen bu test, silikon pul üzerinde özel belirlenmiş yerlere yerleştirilmiş monitör yapılarının eşik gerilimi, doymada sürücü akım ve/veya kanal kaçak akımı gibi MOSFET parametrelerinin ölçülmesi ile gerçekleşir. Bu yapılara elektriksel erişimin öteleme, mikrometrik temas ve hizalama gibi yöntemler gerektirmesi, pahalı bir öteleyici/hizalayıcı ihtiyacının yanı sıra özelleştirilmiş bir prob kart ihtiyacı doğurmaktadır. Bu sorunu aşmak için bir mekanik erişimsiz kanal kaçak monitörü TÜBİTAK projesi olarak önerildi ve kabul gördü. Bu tezde, bu kanal kaçak monitör sisteminin bir alt bloğu tasarlanmıştır. Tasarlanan fotovoltayik beslemeye sahip entegre seçici devre, silikon pul ve alıcı anten arasında iletişimin başlamasını ve test yapılacak yapılardan PMOS veya NMOS olanın seçimini sağlar. Bu amaçla kompakt bir transempedans kuvvetlendiricisi, diyotlu tepe detektörü ve anahtar devresi tasarlanmıştır. Devre herhangi bir harici güç kaynağına ihtiyaç duymaksızın, gücünü fotovoltayik hücrelerden üretir. Ortam aydınlatmasının dışında, kırmık üzerinde belirli bir aydınlanma ve frekansa sahip bir çakar ışık kaynağının açık veya kapalı duruma getirilmesiyle, sistemin sonunda bulunan anahtar ikil-1 veya ikil-0 işareti oluşturarak, kanal kaçak monitörüne iletir. TÜBİTAK desteği ve UMC 0.18 µm tasarım teknolojisi kullanılarak 2 test kırmığı üretilmiş ve ölçümleri yapılmıştır. Bu tezde, bahsedilen entegre seçici yapının tüm tasarım aşamaları ve ölçüm sonuçlarına yer verilmiştir.

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Table 1.1. Fault detection costs at different levels of silicon manufacturing 1



LIST OF SYMBOLS/ABBREVIATIONS

g_m	Transconductance
Hz	Hertz
I	Current
KHz	Kilo hertz
nm	Nanometer
pA	Pico ampers
pF	Pico farads
$\mu\text{W}/\text{cm}^2$	Microwatts per centimeter square
μm	Micrometers
V	Volt
AC	Alternative current
CMOS	Complementary metal-oxide semiconductor
DC	Direct current
DNW	Deep n-well
GND	Ground
LED	Light emitting diode
NMOS	n-Channel MOSFET
OPAMP	Operational amplifier
P-SUB	p-type substrate
PCB	Printed circuit board
PMOS	p-channel MOSFET
TIA	Transimpedance amplifier
TUBITAK	Türkiye Bilimsel ve Teknik Araştırma Kurumu
UMC	United Microelectronics Corporation
VDD	Positive power supply
VSS	Negative power supply

1. INTRODUCTION

As the world keeps spinning, speed of development increases everyday. Vast improvements in technology pushes the limits of both engineers and customers. Nearly every single day a new breakthrough is achieved and the amount of information created is just enormous. Improvements made for integrated circuit manufacturing have a big role in these achievements. As the Moore's Law commands to get smaller and smaller every two years, it gets harder and harder to do so.

Nowadays, silicon processes are at 9 nm level and with every step, it brings all kinds of difficulties. Controlling the process variations at this level is getting more challenging. To increase yield and reliability of the manufactured integrated circuits is the main topic for many foundries. It is really important for a foundry to detect a malfunctioning chip as early as possible. The approximate cost to a company of detecting a fault at various levels in manufacturing is given in Table 1.1.

Table 1.1 Fault detection costs at different levels of silicon manufacturing [1]

Wafer	\$0.01 - \$0.10
Packaged Chip	\$0.10 - \$1
Board	\$1 - \$10
System	\$10 - \$100
Field	\$100 - \$1000

To analyze and model these process variations, companies came up with different solutions. The most common one is scribe line testing (parametric testing). On silicon wafers, there must be fixed a distance between every single chip. This distance is approximately 200 μm . This distance is important because it protects the chips while the wafer gets diced and also foundries put their specially designed test structures in these areas. Visualization of these scribe lines are can be seen in Figure 1.1.

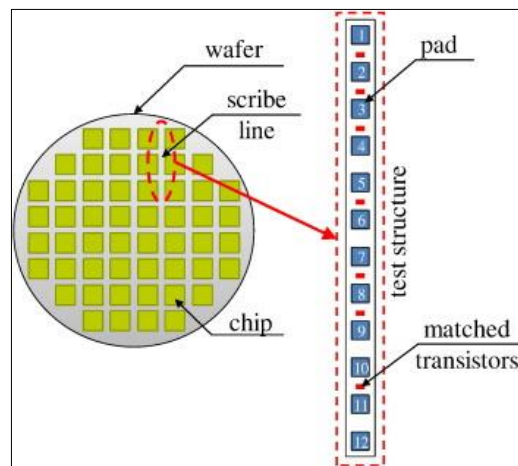


Figure 1.1 Scribe lines and test structures on a silicon wafer

1.1. PROBLEM STATEMENT

Controlling every single chip on a wafer is a huge waste of time since there are thousands of chips on it. Instead of that, a smarter solution has been found. When the wafers are being manufactured, chips on the wafer must be separated by a distance which is called a scribe line. Foundries put their specially designed test structures inside some of these scribe lines with a pattern of their own. After the production is completed, wafers are put into a special testbench and with probes, mechanical access to these test structures is performed. This process requires high precision for aligning and this causes a waste of time. To this end, a novel structure that can realize these measurements without mechanical access but wireless has been proposed to TUBITAK 1001 - Scientific and Technological Research Projects Funding Program. The funding has been granted so that the system can be taped out and realized. In this thesis, a sub-block for this channel-leakage monitor is designed.

Since the whole idea for this system is having the ability to work without mechanical access, the chip would not have supply voltages. Wireless powering is an option but since the scribe test environment has sufficient indoor irradiance, photodiodes can be used to harvest power which is readily available by the indoor light. Photovoltaic energy conversion creates the necessary supply voltages and this will be covered later in this thesis. As the system includes two different channel-leakage monitors and since the selection between them could not be made with external sources, this created a necessity of

another wireless solution. The chip needed to be activated by an external signal source. The solution is to use a flickering light source besides the indoor irradiance and by that, the circuit could select either to use NMOS or PMOS version of the channel-leakage monitor. Detailed design procedure is explained in the further chapters.

Photovoltaic cells are used frequently for optical receiving operations in literature. Lots of different papers have been published and lots of research has been made. The legacy of the previous work done in our laboratory has been a great guide for this thesis [2]. The common sense on this topic is to convert the current supplied from the photodiodes to voltage and use them for further operations. To do so, the most common way is to use a transimpedance amplifier. A wide literature review for using transimpedance amplifiers with photovoltaic supply has been made but a little to no papers have been found. This required a new topology for the current circumstances. Two tapeouts to this end had been made and measured. A novel photodetector/transimpedance amplifier with photovoltaic supply design process and its results are explained in detailed in this thesis.

1.2. TRANSIMPEDANCE AMPLIFIERS

The term “amplifier” generally recalls for a voltage amplifier in the first place. However there are different types of amplifiers such that uses or produces current at its input or output. Transimpedance amplifiers belong to this category. They are basically current to voltage converters. “Transimpedance” comes from the term “transfer impedance” which implies that the defined impedance is measured from two separate ports. Simplified schematic and idealized model of a TIA are shown in the Figure 1.2 and Figure 1.3.

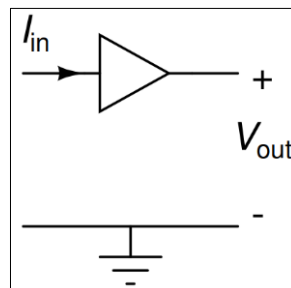


Figure 1.2. Transimpedance amplifier

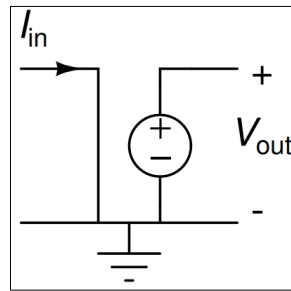


Figure 1.3. Idealized model of a transimpedance amplifier

The simplest transimpedance amplifier is a common-gate circuit which converts current at its source to a drain voltage as it can be seen in Figure 1.4.

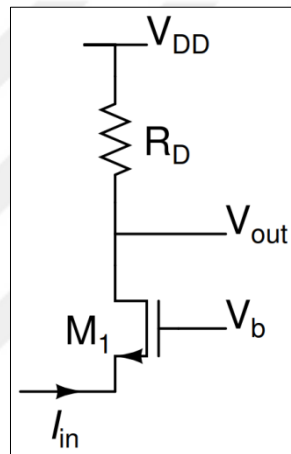


Figure 1.4. A common-gate transimpedance amplifier

Not much as their counterparts, transimpedance amplifiers do find usage in the industry. Common applications for TIAs include optical receivers. These types of circuits must sense the current produced by a photodiode to create a voltage to be used for subsequent system blocks [3]. This frequent usage became a starting point for this thesis since the whole system needs a optical communication for starting and selecting operations.

TIA – photodiode pairs are mainly used as photodetectors. In figure 1.5, the reader can see the basic topology of a TIA and a photodetector. It consists an Op-Amp in inverting configuration with a feedback resistor. Reverse biased photodiode creates a current flowing through the feedback resistor and creates an output voltage according to that. Photodiode sees low impedance at the input of the TIA and becomes isolated from the output of the amplifier [4]. Feedback resistor R_f sets the low frequency gain of the TIA and the relationship between them is;

$$-R_f = \frac{V_{out}}{I_{in}} \quad (1.1)$$

From the (1.1), it is clear that, with the increase of feedback resistor R_f , transimpedance gain increases.

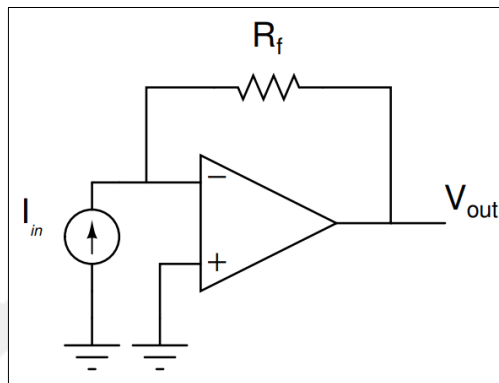


Figure 1.5. A transimpedance amplifier with a feedback resistor

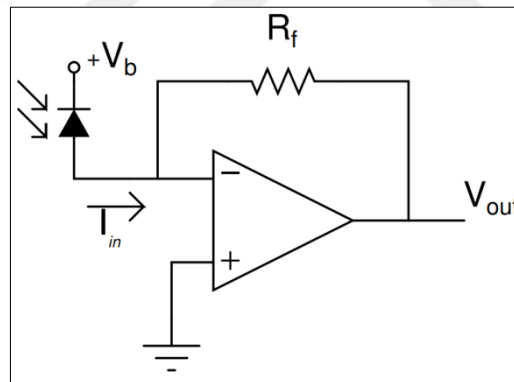


Figure 1.6. A transimpedance amplifier in a photodetector configuration

1.3. PHOTODIODES

Photodiodes are standard p-n junction diodes that are designed for capturing photogenerated carriers by an external light source. They have a history about 50 years in research as the first experiments for creating signals from the visible light started around 1960s. With the developments in silicon manufacturing technologies, p-n junction structures started to include an intrinsic region between p and n type regions for performance improvement.

When a photodiode gets struck by a photon with enough energy, it causes an excitation for the electrons from the valence band to the conduction band. This event generates an electron-hole pair. Photodiode operation relies on these pairs' separation inside the depletion region. With the effect of the built-in electrical field inside this region, electrons will be pulled to the n-side and holes will be pulled to the p-side, thus creating a photocurrent. Visualization of this effect is shown in Figure 1.7.

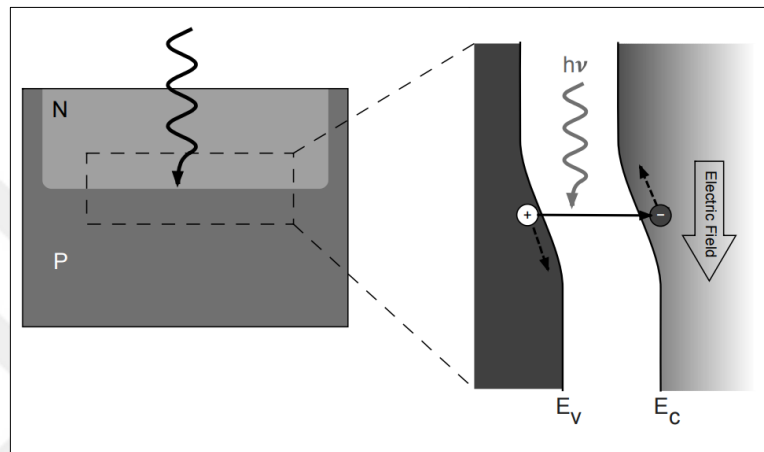


Figure 1.7. Electron movements in a photodiode [5]

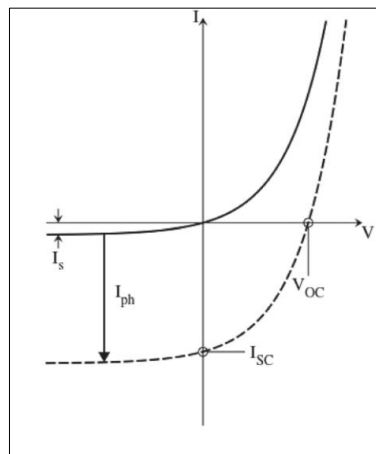


Figure 1.8. I/V characteristics of a photodiode [5]

Due to the generated photocurrent, in Figure 1.8, shifted I-V characteristics can be seen. This current is almost linearly proportional to the exposed light sources irradiance level. I-V relationship of this photocurrent I_L can be expressed as [5];

$$I_L = I_s \left[\exp\left(\frac{qV}{\eta kT}\right) - 1 \right] - I_{ph} \quad (1.2)$$

Where I_s is the saturation current, η is the ideality factor, k is the Boltzmann constant, T is the operating temperature and the I_{ph} is the generated photocurrent. The first term is the familiar Schottky Equation.

There are two main operating modes for a photodiode which are photovoltaic (short circuit) and photoconductive (reverse-bias) mode. If it is in the photovoltaic mode, the current flows through a short circuit between anode and the cathode of the photodiode as can be seen in the figure. This current is actually the I-V curve crossing the y-axis of the figure b above and it is called as short circuit current. These types of photodiodes can be used as supply voltages to the circuit.

In photoconductive mode, a reverse bias is applied to the photodiode. It corresponds to the right hand side of the Figure 1.9. Working under these circumstances increases depletion region width of the photodiode. This increment also leads to an increment in electrical field in the depletion region because change of width isn't as much as change of potential difference. Widened photogeneration region and bigger electrical field leads to an increase in drift velocity of photogenerated carriers. As a result, transit time of the carriers are reduced and signal loss is reduced too. This benefit tempts the designers to use the photodiode in photoconductive mode.

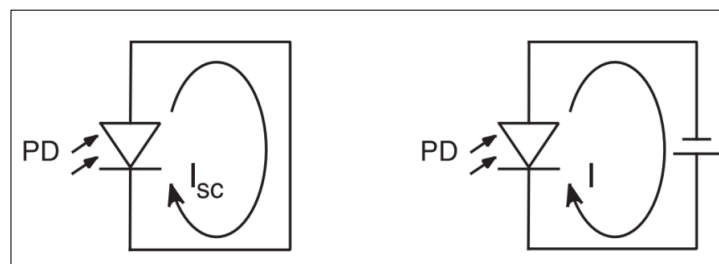


Figure 1.9. Photocurrent (left) and photoconductive (right) operation modes

As mentioned earlier, a previous work is done before including a great research about photodiodes and photovoltaic energy harvesting in our Microelectronic Design and Characterization Laboratory at Yeditepe University. This work has been a perfect guide for this thesis since all the photodiodes used in the system has the same architecture of the taped out and characterized photodiodes before. They were designed and prototyped in the same design kit this thesis has been designed and prototyped which is UMC 0.18- μm bulk-CMOS technology. Positive and negative photodiodes schematic symbols and cross sectional views are given in Figure 1.10 and Figure 1.11, respectively.

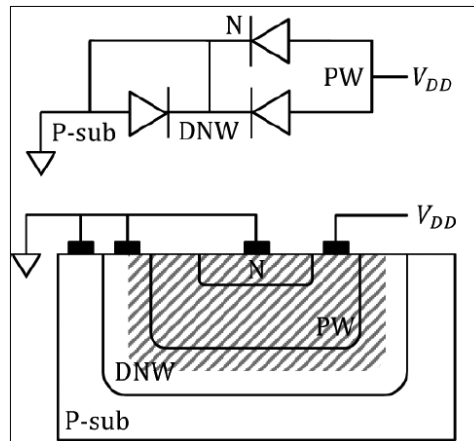


Figure 1.10. Symbol and cross sectional views of the positive photodiode [2]

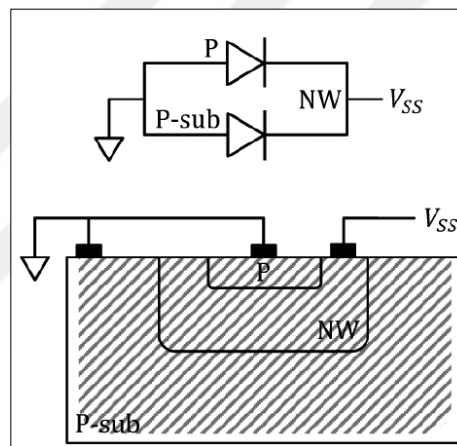


Figure 1.11. Symbol and cross sectional views of the negative photodiode [2]

In Figure 1.10 a positive photodiode, in Figure 1.11 a negative photodiode can be seen. Positive photodiodes are realized with a DNW rather than using a single N-well/P+ junction. As can be seen in Figure 1.10, the P-sub and DNW junctions are shorted. This is due to protect the N/PW. If they were not shorted, there would be a negative voltage formed and this will reduce the overall VDD voltage. The crossed areas are the photon collection areas. Negative photodiodes are more efficient in this term than their positive companions because the P-sub – DNW area is shorted and cannot produce photocurrent. Positive photodiodes are capable of generating positive voltage with respect to p-type substrate. The p-well/n-active and p-well/DNW junctions are in parallel and p-substrate/DNW junctions are short circuited, which leads to a photon collection area shown in gray cross lines [2]. Negative photodiodes could not be produced until the triple-well bulk technology has been developed. P-well and p-substrate are short circuited and this configuration leads to generating negative voltage with respect to the p-type substrate. As

can be seen in Figure 1.11, photon collection area is bigger than the positive photodiode, leading to a more efficient supply.

A $60 \times 100 \mu\text{m}$ positive photodiode creates an open-circuit voltage of 410 mV while a negative photodiode creates an open-circuit voltage of 300 mV under $1 \text{ mW}/\text{cm}^2$ irradiance. Since the negative photodiode is more efficient in photon collection, its current supply capability is bigger than the positive photodiode, as they can supply $0.312 \text{ A}/\text{W}$ and $0.176 \text{ A}/\text{W}$, respectively.

1.4. INITIALLY PROPOSED DESIGN

The designed circuit needs to be triggered by an external flickering light source besides the ambient room irradiance and should create a 1-bit signal to express if there is a flickering light or not. Ambient room irradiance should be $1 \text{ mW}/\text{cm}^2$ and the flickering light source should create a 10 percent irradiance level, which is $1.1 \text{ mW}/\text{cm}^2$. All system should be fitted into a $200 \mu\text{m}$ vertical space, representing the scribe line width.

With the needs of the system taken into account, an initial system level design has been proposed. In order to convert the current produced by the flickering light source a TIA, to boost the voltage levels into a higher level for switching, a voltage multiplier and to switch the multiplexer which is going to be used by the whole system as mentioned before, a switch is needed. In Figure 1.12, the reader may find the initial system level design of this thesis.

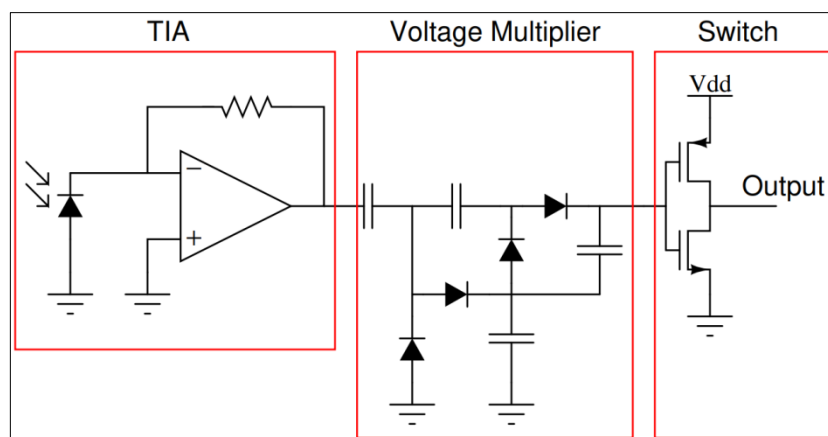


Figure 1.12. Initial system level topology of the proposed selector

2. LITERATURE REVIEW

As mentioned before, use of a TIA is inevitable. To do so, a massive literature review had been done. There are many examples of TIA-photodiode pairs in the literature. Most of them are focused on fast optical communication applications. In order to design a reliable optical receiver, the impedance seen by the photodiode needs to be low as mentioned in section 1.1.2. If the photodiode sees low impedance, the TIA will isolate its capacitance and strong part of determining the bandwidth will no longer be the photodiode's capacitance.

For starting point, the most basic TIA is a common gate structure. These configurations has the capability of isolating the photodiode capacitance because of the input transistor's g_m . Increasing the bias current of the circuit is also a solution to this but this leads to an increase in transistor sizes which will create large parasitic capacitances. In literature, regulated cascode TIAs are used to prevent this [6] [7].

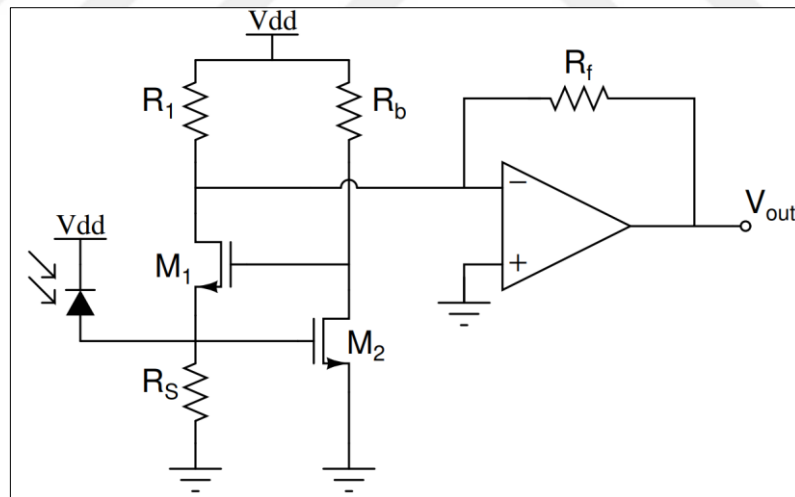


Figure 2.1. A regulated cascode transimpedance amplifier

In Figure 2.1, a regulated cascode schematic is shown. The current flowing from the photodiode gets converted into voltage via M_1 and R_1 . Transistor M_2 and R_b creates a feedback network in order to lower the input impedance. Recalling to section 1.1.2, the input impedance of the common gate topology can be calculated as;

$$R_{in} = \frac{r_o + R_D}{1 + (g_m + g_{mb})r_o}. \quad (2.1)$$

Considering $(g_m + g_{mb})r_o$ is much bigger than 1 and r_o is also much bigger than R_D , the equation converges into

$$R_{in} \approx \frac{1}{g_m + g_{mb}}. \quad (2.2)$$

Looking back into regulated cascode, the input impedance of the circuit can be written as;

$$R_{in} \approx \frac{1}{g_{m1}(1 + g_{m2}R_b)}. \quad (2.3)$$

is lower than the common gate circuit, so it is reasonable to use a regulated cascode TIA structure in this system. This low input impedance will have a better performance by lowering the photodiode's parasitic capacitance.

There are also common source [8] and cascode [9] TIA structures in the literature. A common source TIA can be seen in Figure 2.2;

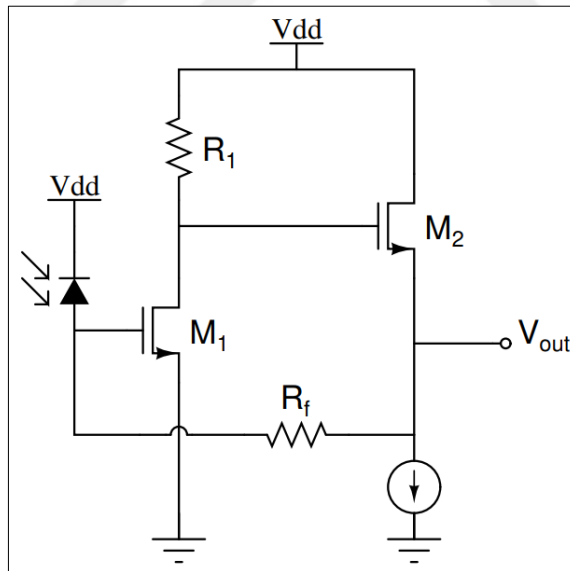


Figure 2.2. A common source transimpedance amplifier

For converting the input current supplied from the photodiode into voltage using a common source structure, a load resistance R_1 is connected to the drain of M_1 . To isolate this resistance from the feedback resistance R_f , a source follower structure is added.

A cascoded TIA structure can be seen in Figure 2.3;

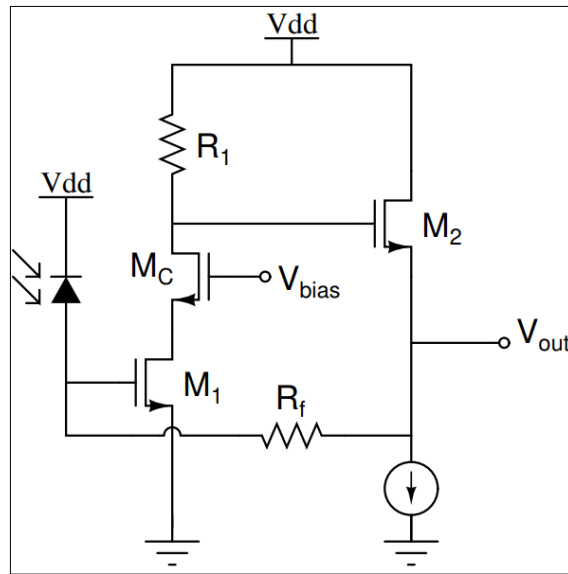


Figure 2.3. A cascoded transimpedance amplifier

Cascoded TIA is fairly similar to the common source TIA with only a difference of using a cascode gain stage. Gain of a common source stage is given as;

$$\frac{V_{out}}{I_{in}} = -g_m(R_L // r_o). \quad (2.4)$$

Considering r_o is much bigger than R_L , equation becomes;

$$\frac{V_{out}}{I_{in}} = -g_m R_L, \quad (2.5)$$

where R_L is the load resistance. Clearly, gain is directly proportional to R_L shown in Figure 2.2 and Figure 2.3. Using a cascode structure changes the input impedance to a common gate input impedance and this will drastically decrease the Miller effect.

Both of these topologies offer high gain and wide bandwidths. A disadvantage of cascode topology is that it requires higher supply in order to preserve the same gain as common source.

Despite a massive literature review, there were no similar designs made for the proposed system of this thesis. Nearly all of the TIAs in the literature are supplied by an ideal voltage source and this is the biggest difference from the proposed thesis content. Necessity of designing an OpAmp in current conditions also leads to bigger design challenges since the photodiodes can deliver considerably low voltage and current. Even if

the OpAmp should have been designed, because of the low input current supplied by the photodiode requires a huge resistor in order to convert this current to a high voltage swing, which is nearly impossible considering the narrow scribe line area.

Because of the reasons explained above, a novel TIA design had to be made. In the 3rd chapter, design of this novel topology has been explained in detail.



3. CMOS INTEGRATED SELECTOR DESIGN

3.1. FIRST TAPEOUT

It is understood that the use of the classic TIA's (OpAMPs with feedback resistor) was impossible to design in the given specs in Section 1.4. This is purely because of the maximum current supplied by the photodiodes into the OpAMP is way too low, and would require a massive feedback resistor, both in size and magnitude, to operate as necessary. As mentioned before, having no similar topologies according to our needs, led to a novel design for the photodetector. The basic principal for the proposed system stayed the same as given in section 1.1.4, the TIA is different from the standard TIA topologies. Schematic of the new TIA can be seen in Figure 3.1.

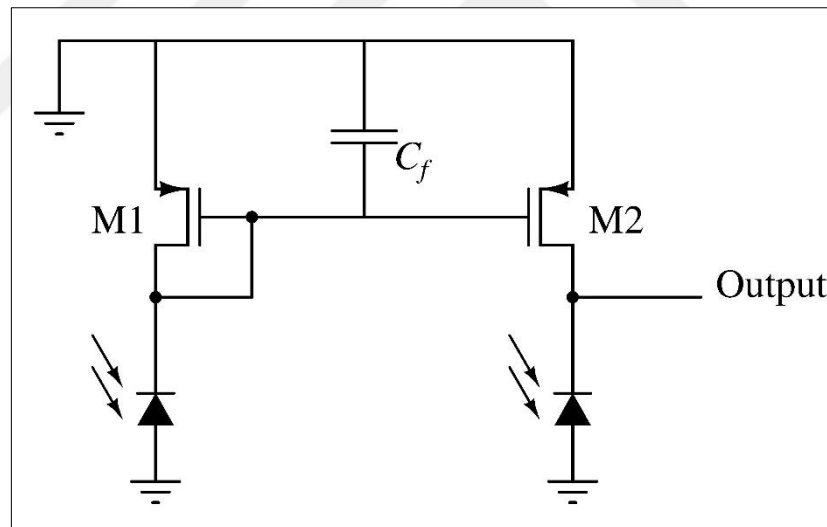


Figure 3.1. Schematic of the proposed transimpedance amplifier

3.1.1. Analysis of the Proposed Circuit

There are two small negative photodiodes with a size of $6 \times 10 \mu\text{m}$ behaving as optical receivers. A flickering light source above these two photodiodes besides the ambient light will trigger the circuit. This flickering light source has an irradiance of 10 percent of the rooms irradiance which has been targeted as 1 mW/cm^2 . The small signal equivalent circuit of the system is given in Figure 3.2.

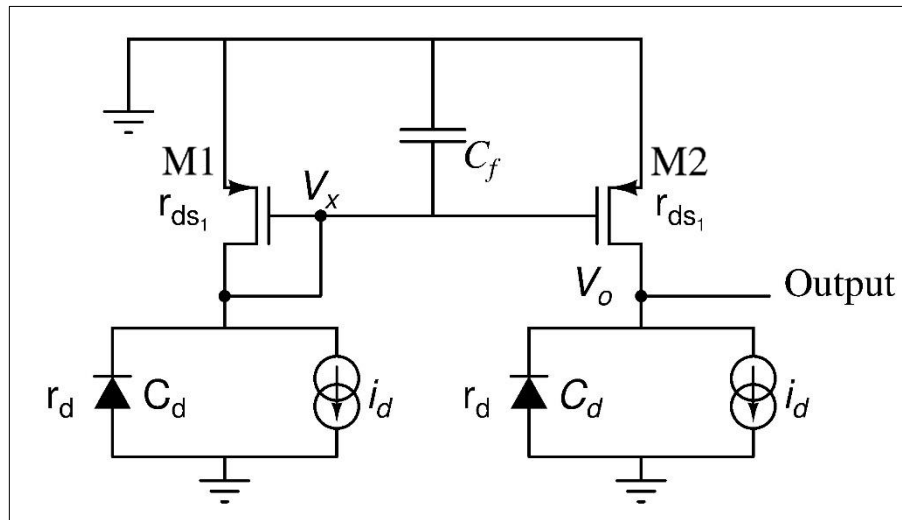


Figure 3.2. Small signal equivalent circuit of the proposed transimpedance amplifier

Analyzing the right hand of the circuit, it is kind of a PMOS common-source, with a difference that it is not driven from its gate but from its source with a current source, equivalent of the photodiode. Left hand side devices of the circuit are identical to its right hand side pairs. Only with a difference of transistor M_1 is a diode connected MOSFET. M_1 creates a gate voltage by the nature of the diode connected MOSFET. This gate voltage applies to the M_2 transistor and creates the necessary bias voltage. Since the photodiodes create negative bias voltage, there is no harm for connecting the sources of the PMOS transistors to the highest available potential, which is ground. This is very much in our favour since it eliminates the need of a positive supply.

Both of the transistors are affected by the external flickering light source, which creates fluctuations in their current as a result. Capacitor C_f prevents the V_x node from fluctuations by charging with every cycle of the sinusoidal signal and holding it still, since it does not discharge until the next period of this signal charges it again. Since the fluctuation in gate voltage is suppressed by C_f , and the current drawn from the drain is changing with time, M_2 increases its drain voltage to conduct the current drawn by the photodiode. This provides high transimpedance gain in contrast of the fluctuating current provided by the external light source and also becomes a self-biased circuit.

The circuit's main feature is that it provides a bandpass filter behaviour. To analyze this, the small signal model of the circuit is given in Figure 3.3.

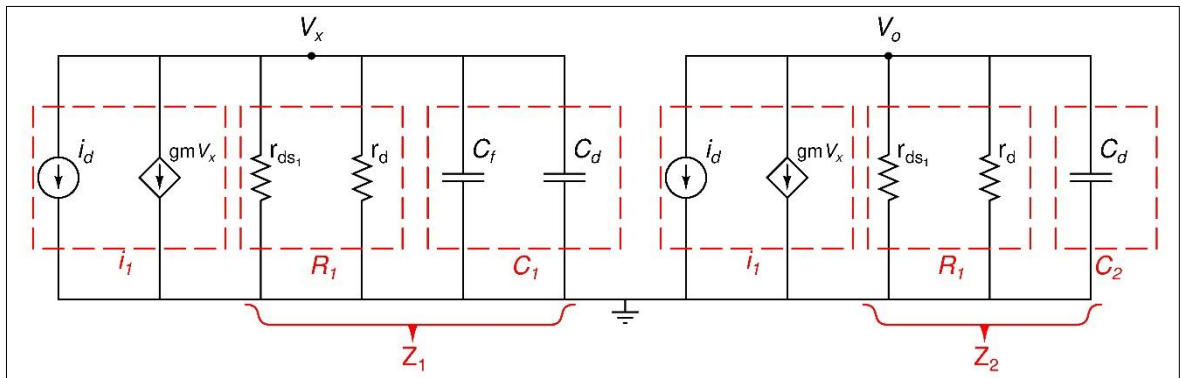


Figure 3.3. Detailed small signal equivalent circuit of the proposed TIA

Since the both transistors and the photodiodes are the same, i_d , gmV_x , r_{ds} , r_d and C_d are all the same too. Analyzing the left hand side;

$$Z_1 = R_1 \parallel \frac{1}{sC_1} = \frac{R_1}{R_1 + \frac{1}{sC_1}} = \frac{R_1}{1 + sR_1C_1} \quad (3.1)$$

$$V_x = -\frac{i_1 R_1}{1 + sR_1C_1} \quad (3.2)$$

$$V_x = -\frac{(i_d + gmV_x)R_1}{1 + sR_1C_1} \quad (3.3)$$

As a matter of simplification, C_l is replaced with the C_f itself since C_f is much more bigger than the parasitic capacitance of the photodiode by a magnitude of 10^6 .

$$\frac{V_x}{i_d} = -\frac{\frac{1}{g_m}}{1 + \frac{s}{(g_m/C_f)}} \quad (3.4)$$

Denominator of this equation recalls as a low-pass filter behaviour and the cutoff frequency of this low pass filter can be expressed as;

$$f_L = -\frac{1}{2\pi C_f(1/g_m)} \quad (3.5)$$

Analyzing the right hand of the circuit gives;

$$Z_2 = R_1 \parallel \frac{1}{sC_2} = \frac{\frac{R_1}{sC_2}}{R_1 + \frac{1}{sC_2}} = \frac{R_1}{1 + sR_1C_2} \quad (3.6)$$

$$V_o = -\frac{i_1 R_1}{1 + sR_1C_2} \quad (3.7)$$

$$\frac{V_o}{i_d} = -\frac{R_1}{\left(1 + \frac{1}{s}\right) + \left(1 + \frac{s}{R_1C_2}\right)} \quad (3.8)$$

The denominator of the equation now offers two cutoff frequencies which results in a bandpass behaviour with a low and high cutoff frequencies. These frequencies can be expressed as;

$$f_L = \frac{g_m}{2\pi C_f} \quad (3.9)$$

$$f_H = \frac{1}{2\pi R_1 C_2} \quad (3.10)$$

These low-pass and bandpass filters lead to a bandpass filter with a narrower band than the one coming from the right hand side of the circuit. Visualization of these two filters merging can be seen in figure;

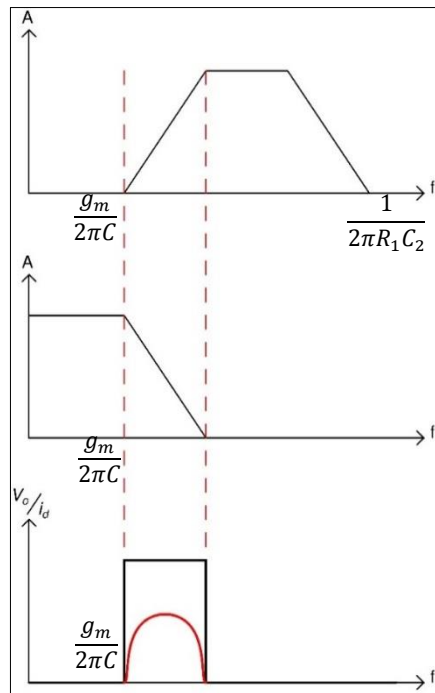


Figure 3.4. Bandpass filter visualization of the system

3.1.2. Design Procedure and Simulations

The low cutoff frequency target is selected to be greater than 500 Hz. This is simply done because, some types of indoor lighting systems are run directly via mains supply which has a frequency of 50 Hz and could interfere with the flickering light. To give a safety margin, low cutoff frequency has been selected as 500 Hz. Bandwidth is not so much of a concern as one can control the flickering light sources frequency to match the photodetectors working region.

This leads to device selection as UMC 0.18 μ m technology offers 4 different NMOS and 4 different PMOS types. These are 1.8V, 3.3V, 1.8V Low Threshold and 3.3V Low Threshold devices. To get the most out of the circuit, device sizes should be chosen correctly. Main performance metric to be focused is transconductance. It should be high enough to fulfill the lower frequency cutoff target as can be seen in equation.

Negative photodiodes are more efficient than the positive photodiodes, as mentioned earlier. Because of this, negative photodiodes are selected and this leads to elimination of NMOS devices since they need to be driven with a positive photodiode. After this, 4 different type of PMOS devices are sized with a channel width and length of 2 μ m and AC magnitude simulations has been made under 1 mW/cm² constant irradiance with a change of 10 percent in irradiance at 500 Hz, imitating the flickering light source. The outcome of this simulation can be seen in Figure 3.5;

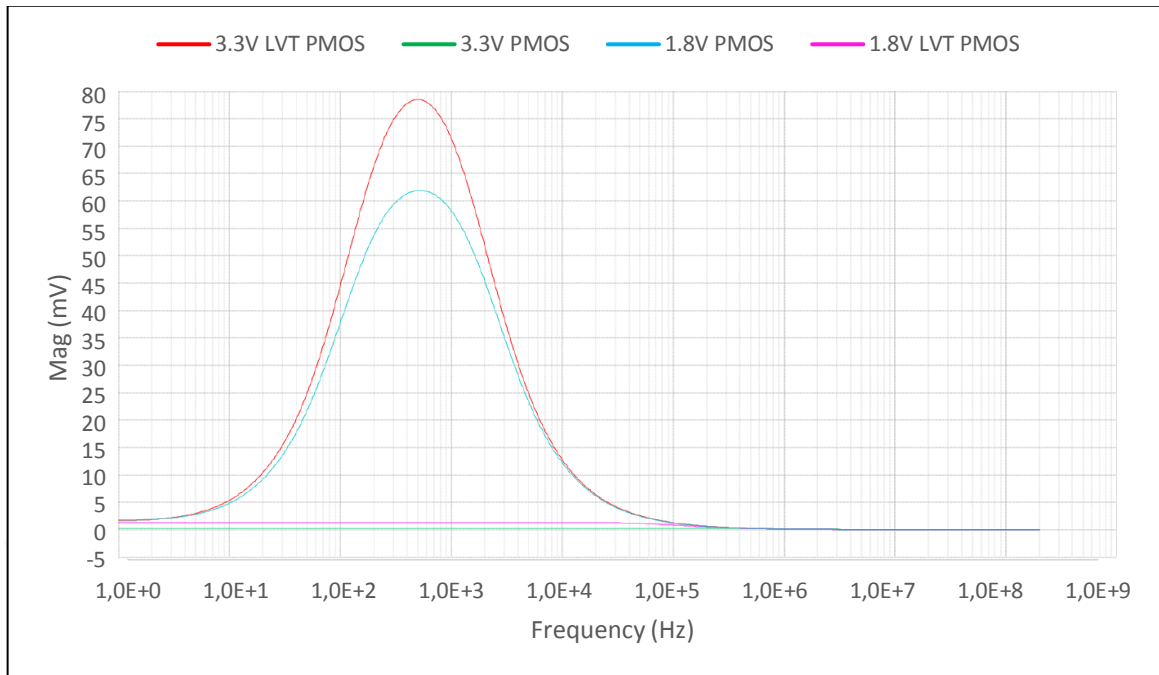


Figure 3.5. AC gain comparisons of the 4 devices

It is clear that the low threshold 3.3V PMOS transistor gives the most AC gain with this topology. Transconductance of this device is simulated as 5.93×10^{-9} S and it has a r_{ds} of 57.8 G Ω . To match the target frequency, capacitor C_f has been selected as 1 pF. Using these values with the equations, f_L of this topology has been calculated as 429 Hz. and f_H can be calculated as 2.3 KHz, which satisfies the target bandwidth.

The 60 x 100 μm photodiodes mentioned in Section 1.1.3. were meant to be used in this new photodetector topology. Fortunately, smaller they are, lower the shunt resistance (represented as r_d in Figure 3.3) they will have and this will lead to a higher cutoff frequency. Smaller photodiodes are selected to have a dimension of 6 x 10 μm . With a rough estimation, under an indoor irradiance of 1 mW/cm² a small negative photodiode will have a short circuit current of 190 pA. With the flickering light source, its short circuit current will rise up to 210 pA periodically. Flickering light sources frequency is selected as 750 Hz, satisfying the calculated photodetector receiver bandwidth.

From the previous work [2], a photodiode instance was created in our laboratory. As seen in the small signal equivalent circuit of the photodetector in Figure 3.2, photodiodes are modeled as a diode/current source parallel pair. For the smaller diode, the mentioned instance file has been modified roughly to satisfy the small photodiode behaviour. The

flickering light source has been modelled as a periodic current change in the photodiode. In the off state of the flickering light, the output of the photodetector is given in Figure 3.6.

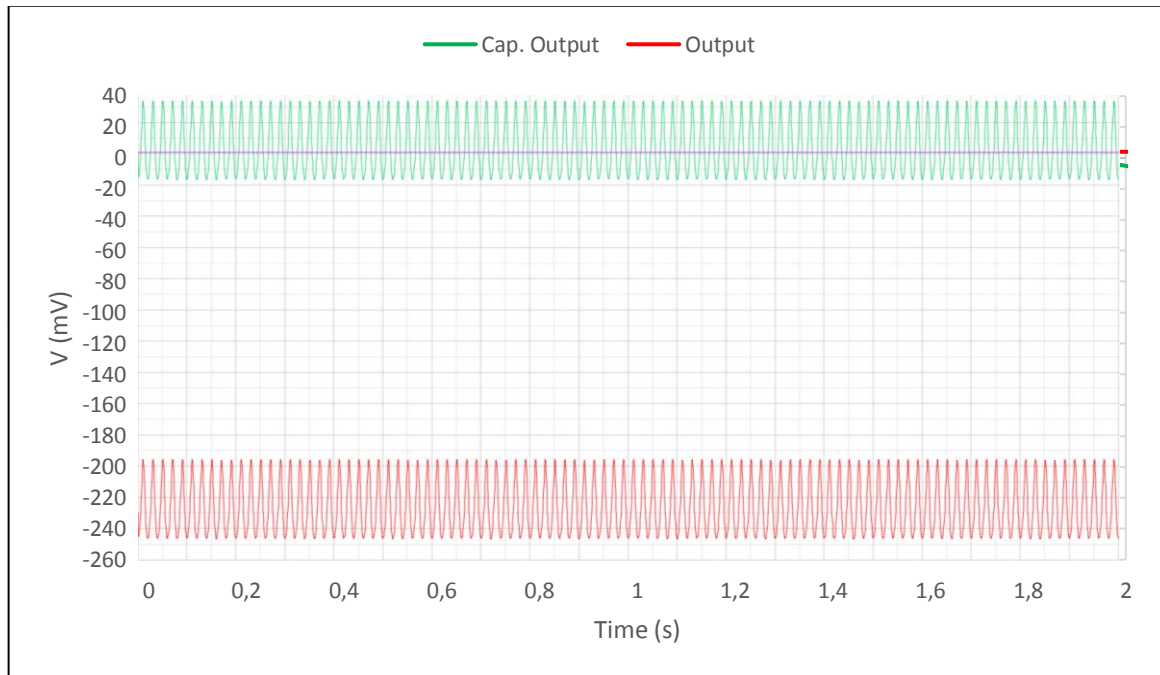


Figure 3.6. Off state simulation result of the system

The red waveform represents the photodetectors output and the green waveform represents this waveform after filtering the dc offset level with a capacitor. After applying the flickering light besides the indoor irradiance, the output waveform becomes as it is in Figure 3.7.

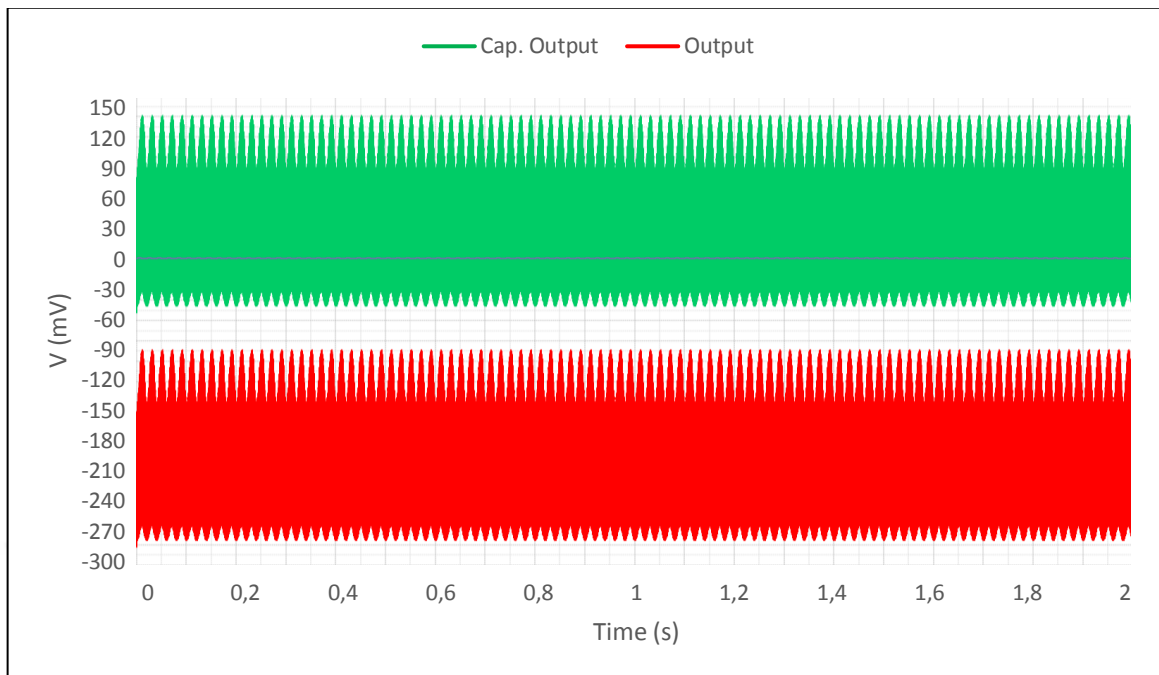


Figure 3.7. On state simulation result of the system

With only a 10 percent periodic irradiance change leads to a 180 mV voltage swing at the output of the photodetector. This proves that the new topology is working well. Close up to the waveforms can be seen in Figure 3.8.

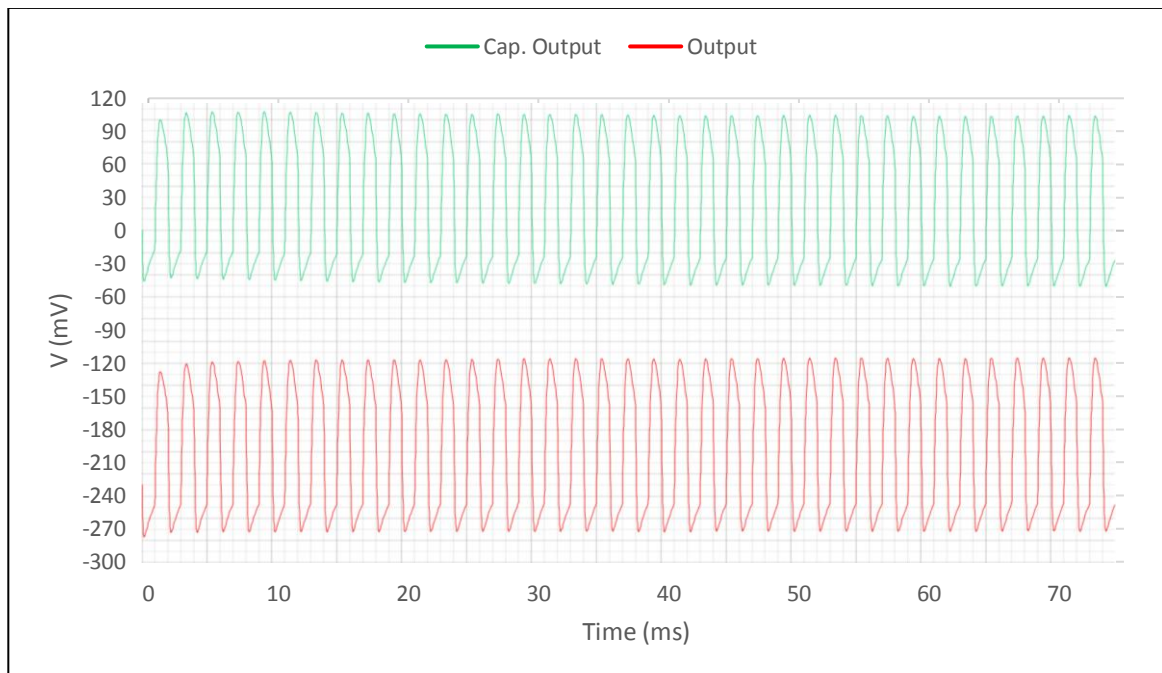


Figure 3.8. Close up view to the output waveforms of the photodetector

The second part of the system consists a voltage multiplier or to be more specific, a voltage quadrupler circuit. Voltage quadrupler is built by cascading two voltage doubler circuits. Voltage doublers consist two diodes and two capacitors only. A voltage doubler circuit can be seen in Figure 3.9. If a sinusoidal wave is applied to its input, during waves negative cycle, diode D_1 becomes forward biased. This means it will start conducting and this leads to charging of the capacitor C_1 to the peak voltage of input. Since there is no route for C_1 to discharge, it stays charged, acting as a battery. When the positive cycle of the input comes, D_1 becomes reverse biased and blocks the C_1 from discharging while D_2 is now forward biased and charges C_2 capacitor up. Since the C_1 is still charged to a positive peak voltage of the input signal, C_2 gets charged to twice of this peak voltage. By this way, there will be two times the input voltage peak at the output.

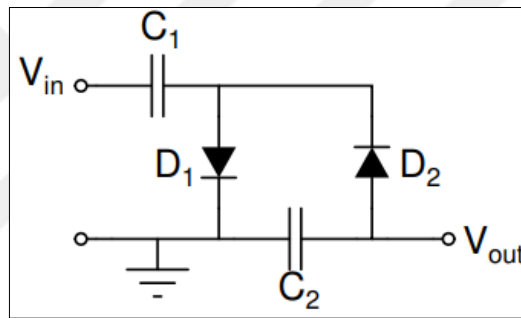


Figure 3.9. A voltage doubler structure

To boost the voltage even more, voltage quadrupler topology has been intended to use in this thesis. After building the circuit, the flickering light simulation at 500 Hz. has been made and its results are given in Figure 3.10.

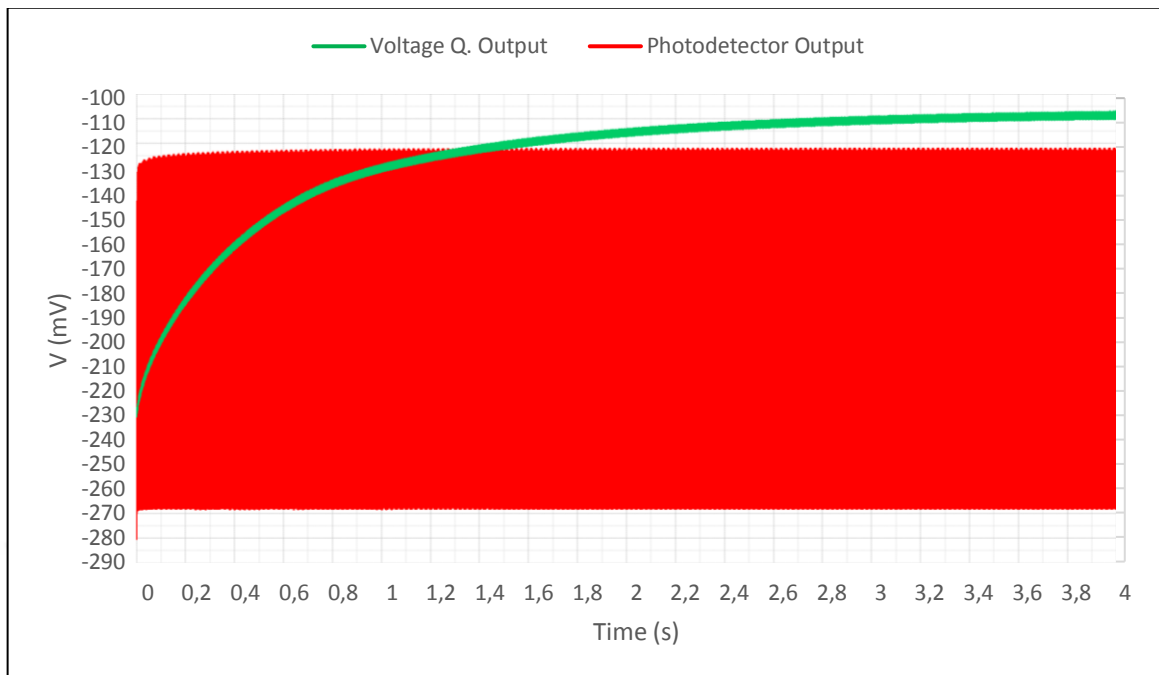


Figure 3.10. Output waveform of the voltage quadrupler at 500 Hz.

As can be seen, after 4 seconds, sinusoidal signal at the input of the voltage quadrupler has become a dc voltage at its output with a value of -110 mV. The starting DC offset level is also a critical value, since the switch that comes afterwards needs to handle these levels as logic 1 and logic 0. In other words, if there is no flickering light, the output of the voltage quadrupler will stay at -230 mV and will not trigger the subsequent switch, but in case there is flickering light, then the circuit will do its work and the switch will be triggered to logic 1.

The diodes in the voltage quadrupler has been designed by using 3 specially connected MOSFETs. This has been used by a former colleague in our laboratory and proven to be working [10]. Its schematic is given in Figure 3.11.

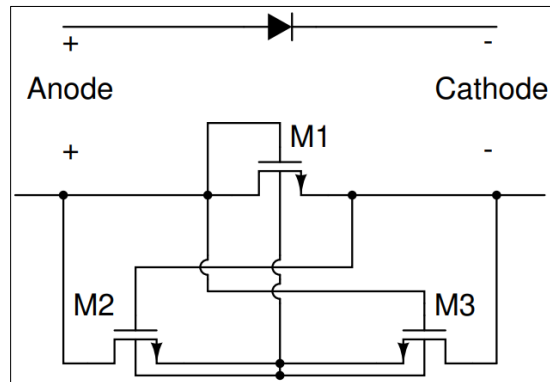


Figure 3.11. Used diode topology

M1 is intended to use as a diode by configuring it as a simple diode connected MOSFET. Since the anode or cathode of this structure can be at different voltage levels, to hold the bulk of this M1 transistor at lowest voltage level between drain and source, two cross coupled transistors M2 and M3 were added to the structure. In other words, M2 and M3 are here to keep the bulk of M1 to stay at the same voltage with its source. This topology is selected purely due to having lower leakage than the library diode of the foundry.

At last, a simple inverter has been designed to complete the system. In general, inverters are supplied with VDD and VSS or VDD and GND. Since the DC level of the voltage quadruplers output is negative, it was sensible to use GND and VSS supplies in the inverter, as given in Figure 3.12. By sizing the devices, switching voltage of the inverter has been selected as -150 mV. The total system simulation results are given in Figure 3.13.

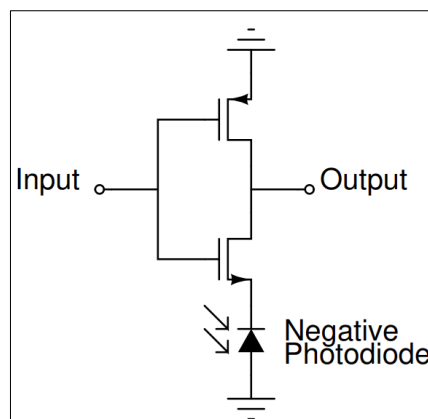


Figure 3.12. Used inverter with photovoltaic supply

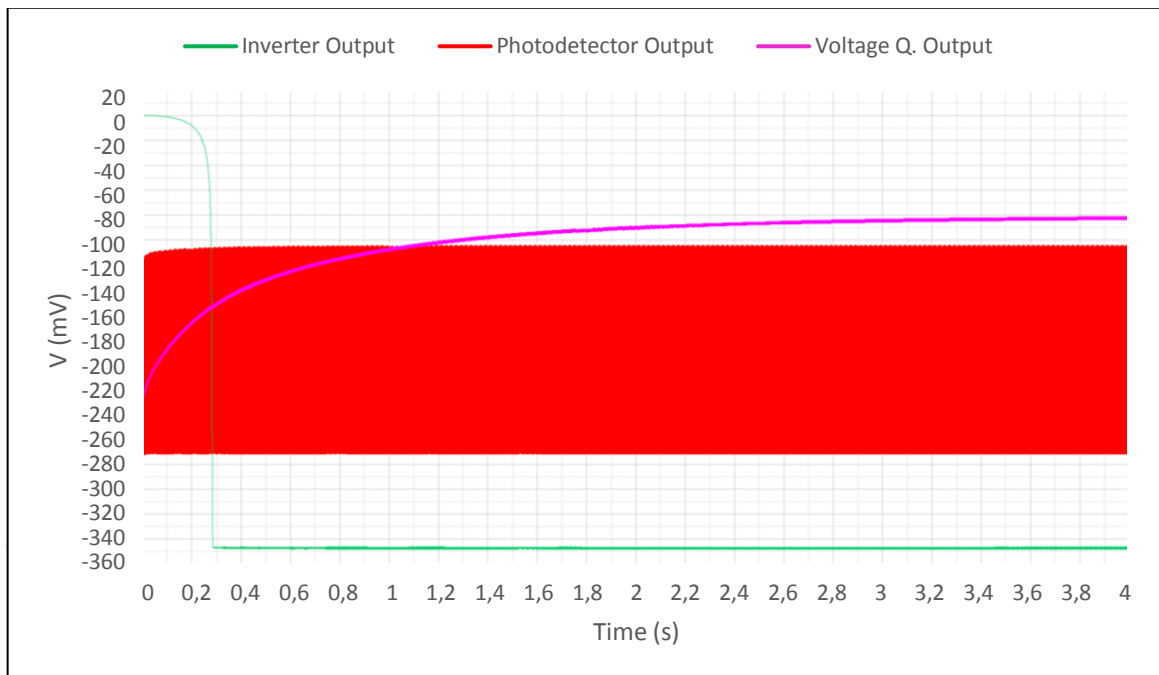


Figure 3.13. Output waveform of the total system

This simulation proves that the system is up and running with a 0.3 second response time to the flickering light source. This delay is completely acceptable since the time is not a concern for this system, unless it is at minute level.

As simulations proven the system is working as it should be, layout and tapeout phase begun. Below, layout screenshots of the system can be found.

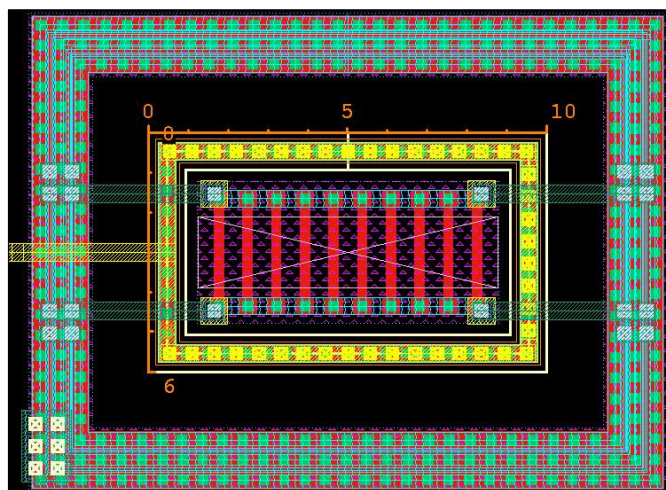


Figure 3.14. Layout of a small photodiode

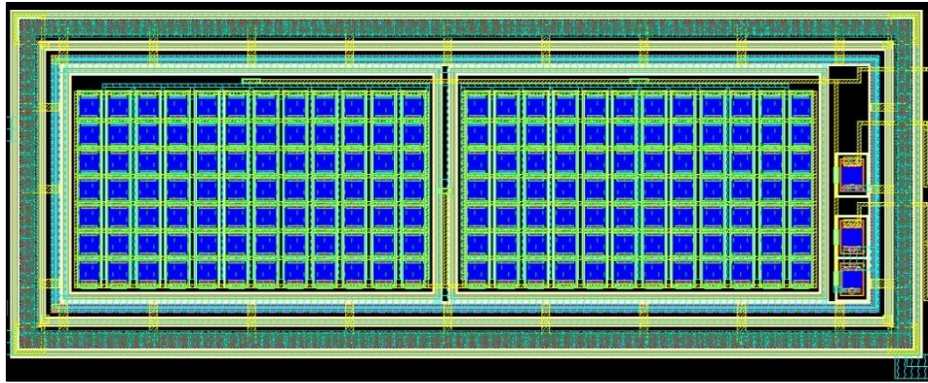


Figure 3.15. Layout of the novel transimpedance amplifier

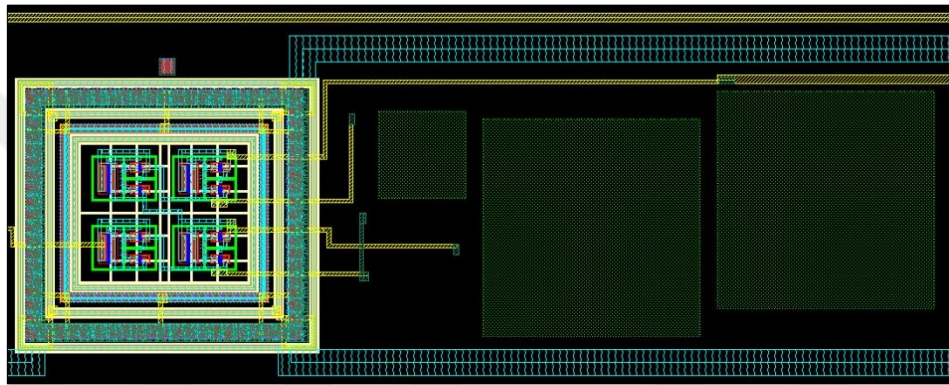


Figure 3.16. Layout of the voltage quadrupler and switch

Post layout simulations have been conducted before sending the chip to the foundry. On state simulation results of the system at 500 and 750 Hz are given in the figures below.

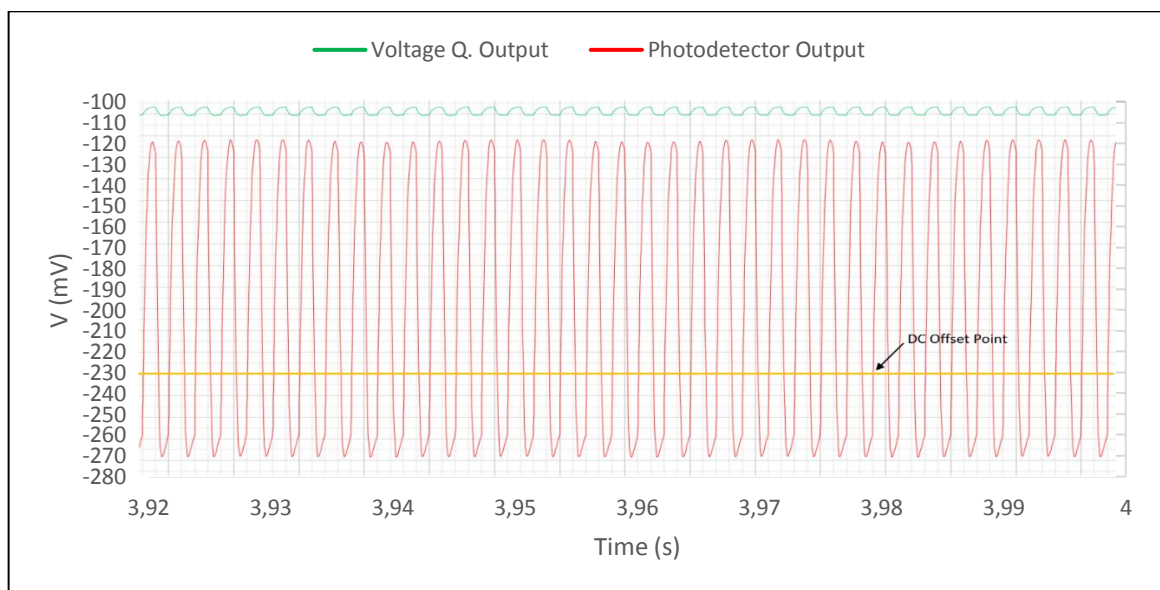


Figure 3.17. Post layout simulation results at 500 Hz.

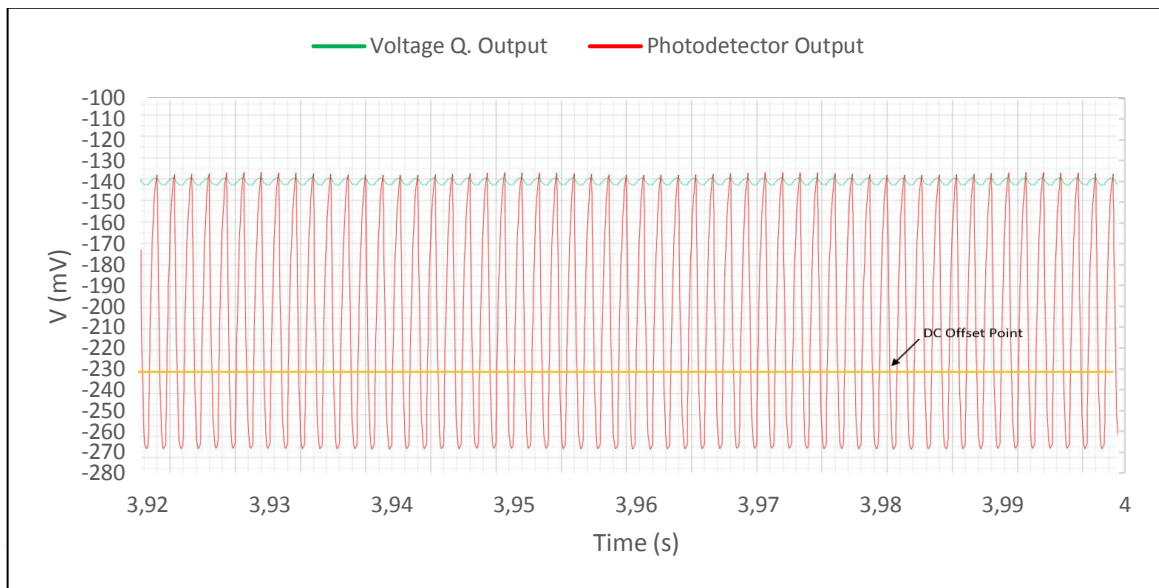


Figure 3.18. Post layout simulation results at 750 Hz.

3.1.3. Measurement Results

The tapeout has been made via Europractice IC and the procedure took about 4 months. The photomicrograph of the chip can be found in Figure 3.19. White rectangles marked with J, K, and L are representing the photodetector, voltage quadrupler and the inverter, respectively.

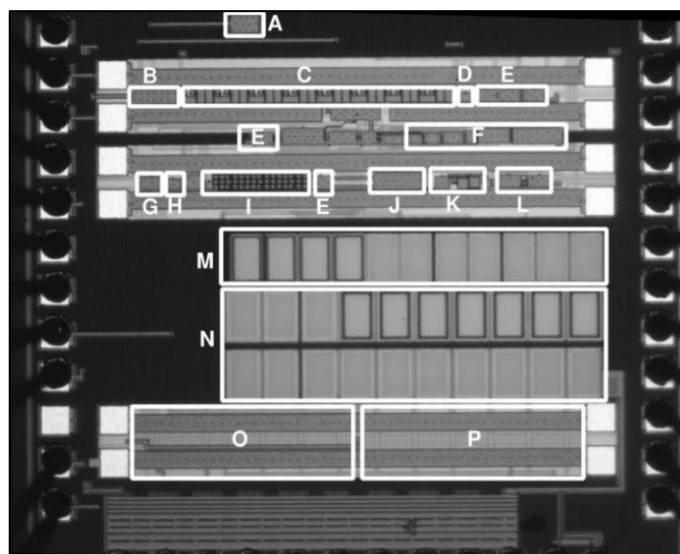


Figure 3.19. Photomicrograph of the taped out IC

It is indeed a compact structure with dimensions of only $50 \times 250 \mu\text{m}$.

After receiving the chip, a measurement plan has been made. The chip consists spare small photodiodes to be characterized, since this size of a photodiode has never been taped out from our laboratory. This also enables to model the photodiode in Virtuoso environment for the future tapeouts to be made.

First test has been made for the small photodiode characterization. This test has been conducted with a Gamma Scientific Eigenlite RS-5B Calibrated Light Source and Keithley 4200 SCS Semiconductor Characterization System devices in our laboratory. This light source is programmable and has an irradiance range of $16 \mu\text{W}/\text{cm}^2$ to $2 \text{mW}/\text{cm}^2$.

Under $1 \text{mW}/\text{cm}^2$ condition, characterization has been made. Surprisingly, its open circuit voltage and short circuit current turned out to be different then the estimated values. A $6 \times 10 \mu\text{m}$. photodiode has a short circuit current of 360pA and a open circuit voltage of 345mV . In the simulation models, it was roughly estimated that the small photodiode would have a current of a direct proportion scaled by its bigger companion. However it was later acknowledged that, when the photodiode becomes smaller, its efficiency increases. After the characterization, this new data had been used for creating a new model for this small photodiode with an intend to use in the following tapeouts. In Figure 3.20, simulated and measured voltage/current results are given.

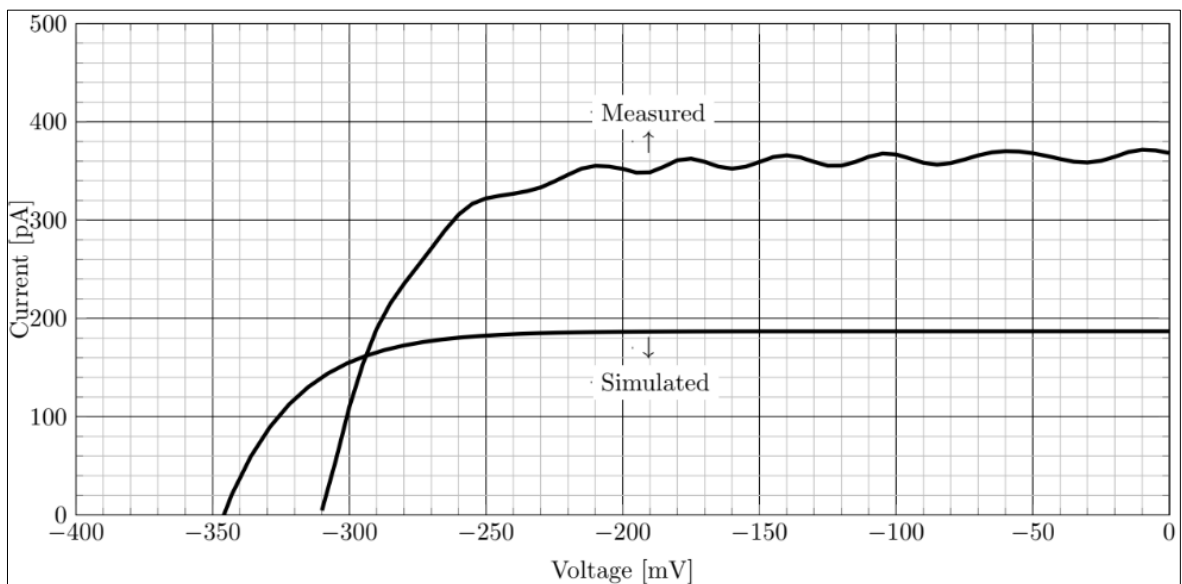


Figure 3.20. Voltage – current characterization of the small photodiode

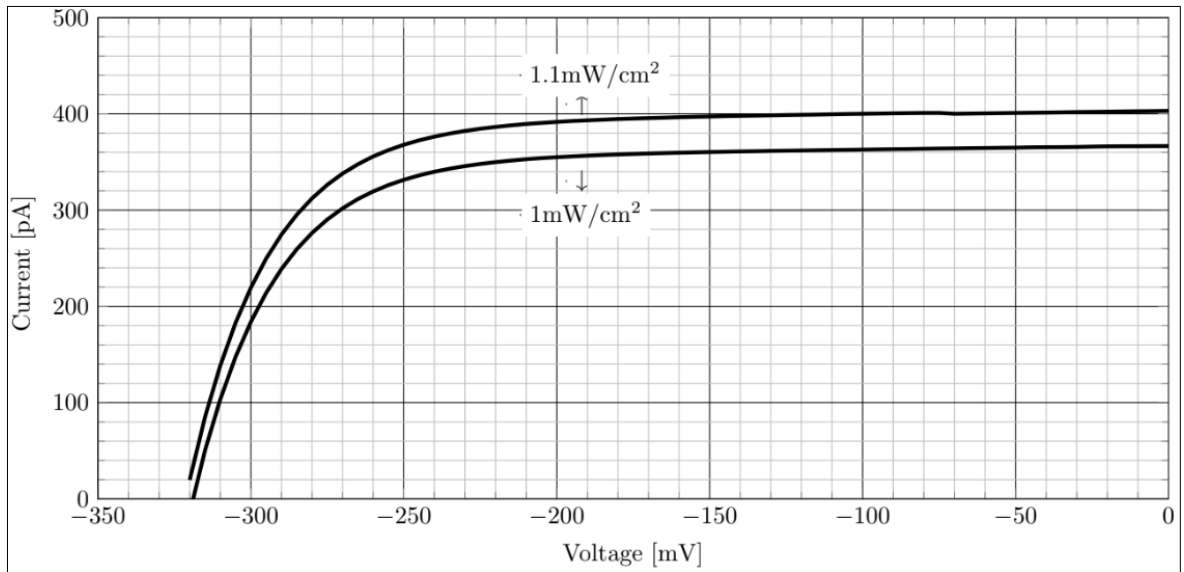


Figure 3.21. Voltage – current characterization under 1 and 1.1 mW/cm² conditions

The calibrated light source is not applicable to conduct the flickering light measurements since it could not be programmed as a flickering light source. To do so, a so called “Arda-box” has been created. Its main purpose is to have a controllable and constant LED light with an option of flickering. With a 3D printer, a small and portable box has been printed.

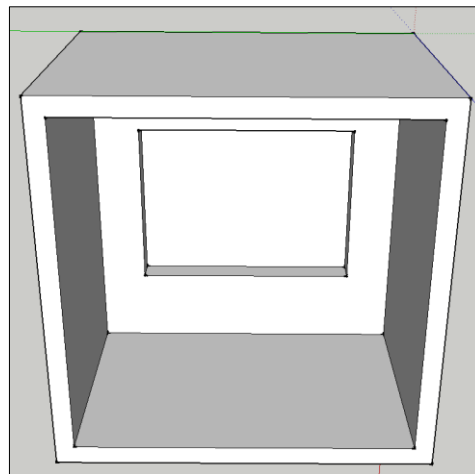


Figure 3.21. View from the bottom of the “Arda-box”

Inside this box, a simple constant current source circuit with the LM317T linear voltage regulator has been designed and its PCB has been manufactured. 6 separate LEDs have been placed inside the box with this PCB and the small photodiode characterized once more to adjust the current flowing through the LEDs by changing the resistor value at the output of LM317T to illuminate at 1 and 1.1 mW/cm².

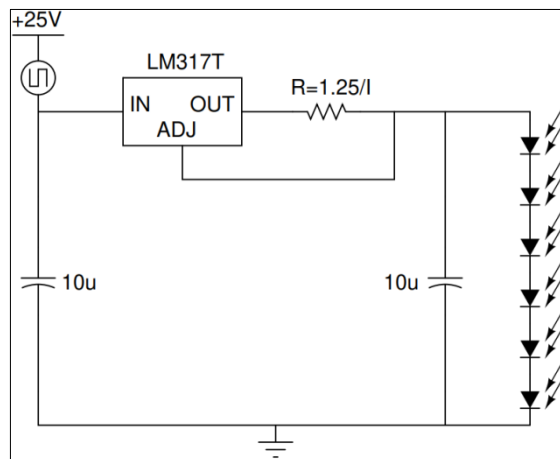


Figure 3.22. Schematic of the constant current light source

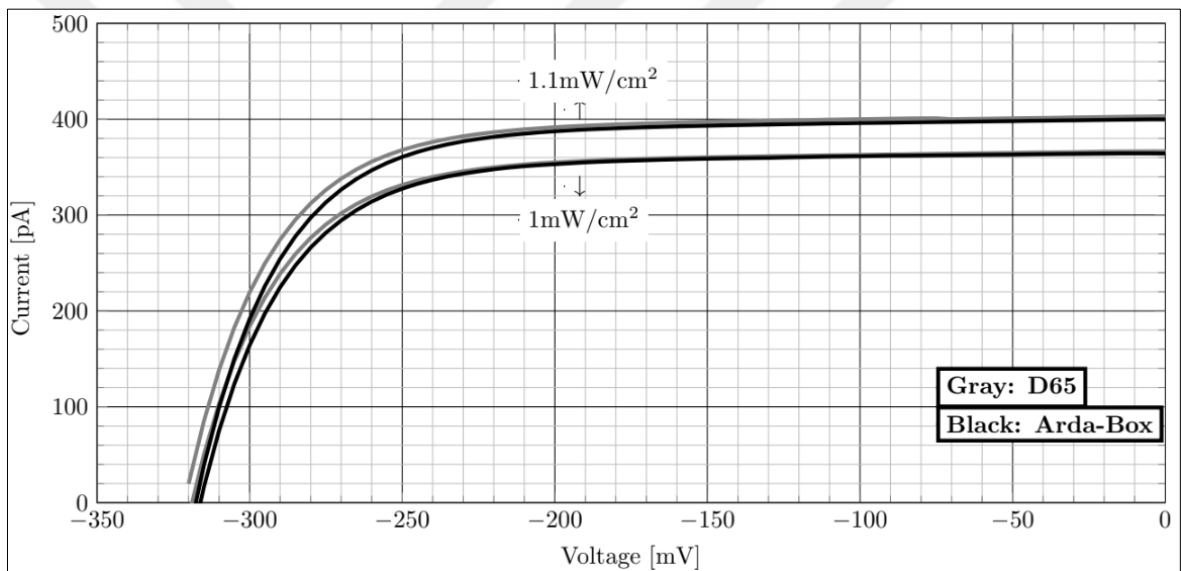


Figure 3.23. Characterization of the “Arda-box”

After the adjustments of the box has been done, flickering light measurements can be made to see if the chip is working properly. To capture the output waveforms, Tektronix DPO70804B oscilloscope has been used.

Unfortunately, not all of the chips worked properly. This is purely a design flow flaw due to being inexperienced. No corner simulations had been done during the design process. Also, subthreshold condition currents were not modeled properly by the foundry. This conclusion has been made through the testing of spare devices put into the chip. There were 5 to 6 times difference in currents between measurement and simulation results. The on and off state waveforms at the outputs of photodetector and voltage quadrupler under 500 Hz flickering light condition is given in Figure 3.23 and Figure 3.24, respectively.

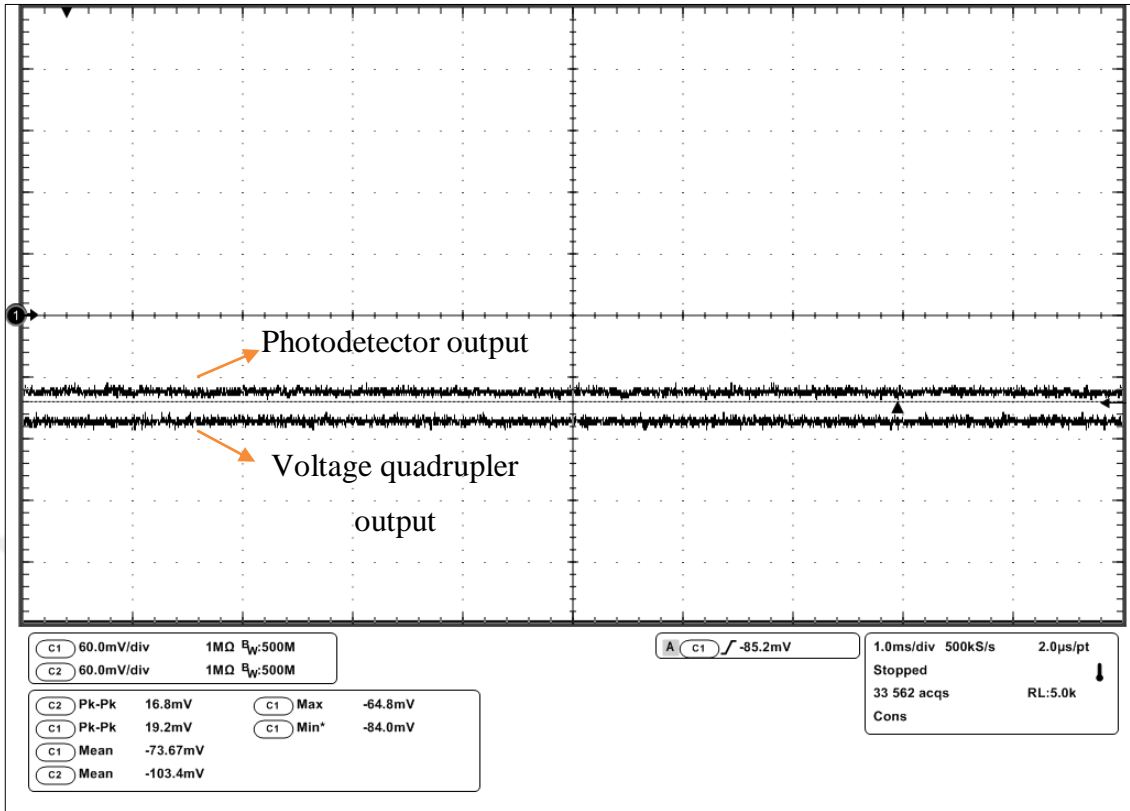


Figure 3.24. Off state output waveforms at 500 Hz.

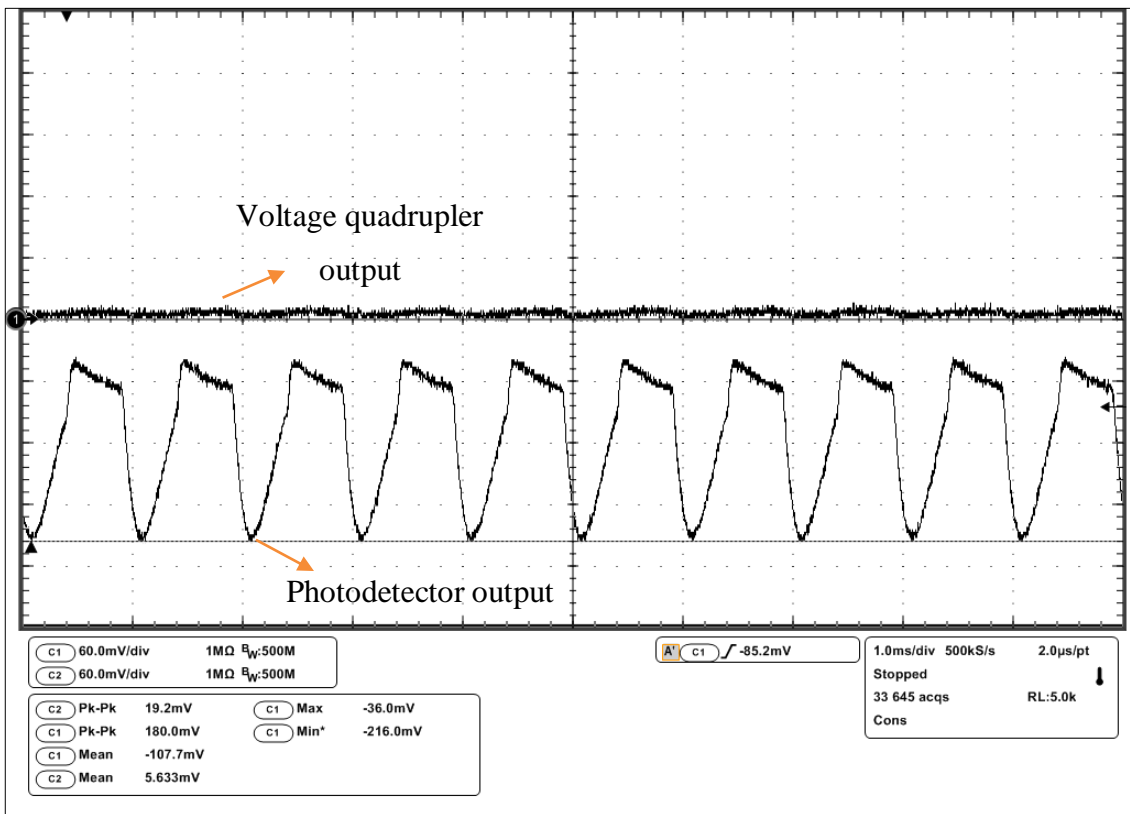


Figure 3.25. On state output waveforms at 500 Hz.

As can be seen in the results, the photodetector topology is clearly working. In simulations, peak to peak voltage of the output waveform was about 200 mV. From the measurements, it is read 180 mV peak to peak. Also the output of the voltage quadrupler arises from -100 mV to 5 mV which is acceptable. However the DC negative offset of the system was around -230 mV in the simulations. In the measurements it is around -100 mV and this prevented the switch at the output to work properly.

Still, the general idea of the system was realized and there was time to solve these problems until the next tapeout. In the next section, solutions for the problems above are explained and the results are given.

3.2. SECOND TAPEOUT

3.2.1. Design Procedure and Simulations

To prevent the problems caused by the process variations and increase reliability, it was a necessity to simplify the system even more and use fewer devices in the system. In the second tapeout plan, the system given in the Figure 3.26 has been proposed and designed.

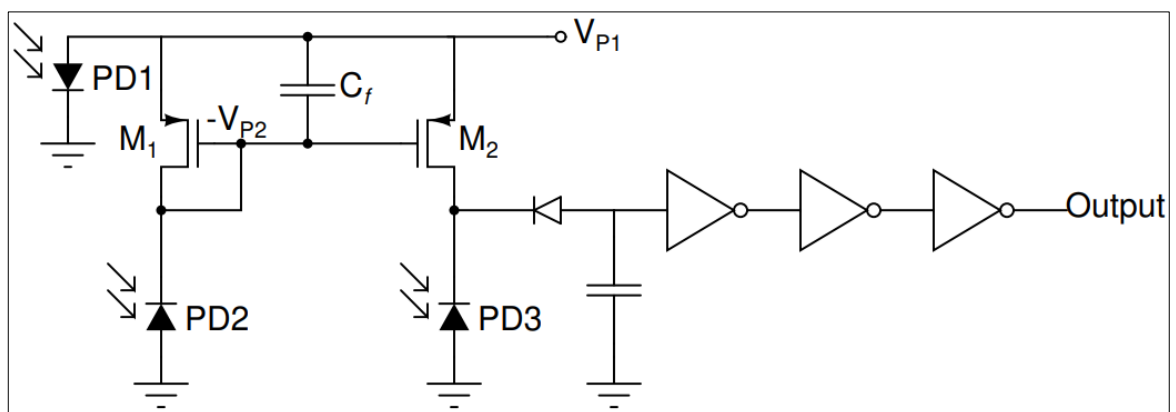


Figure 3.26. Final design of the selector

One of the main differences is to use double supply for the system. This is purely for increasing the rail to rail voltage of the system and thus increasing the peak to peak voltage of the output swing.

Also, use of the voltage quadrupler is abandoned. Voltage quadrupler structure has a lot of devices in it and from the first tapeout, their chip to chip variation were massive. While the output swing is boosted to a higher level, a simple peak detector structure is meant to use for converting the sinusoidal wave into a DC level by charging the capacitor.

Output of this peak detector is followed by a series of switches. Multiple switch usage is for having a sharp and vertical switching characteristic.

Once the design plan has been completed and the device sizing is done, a series of simulations are done to verify the performance of the system. In Figure 3.27, output waveforms of the each sub-block is shown.

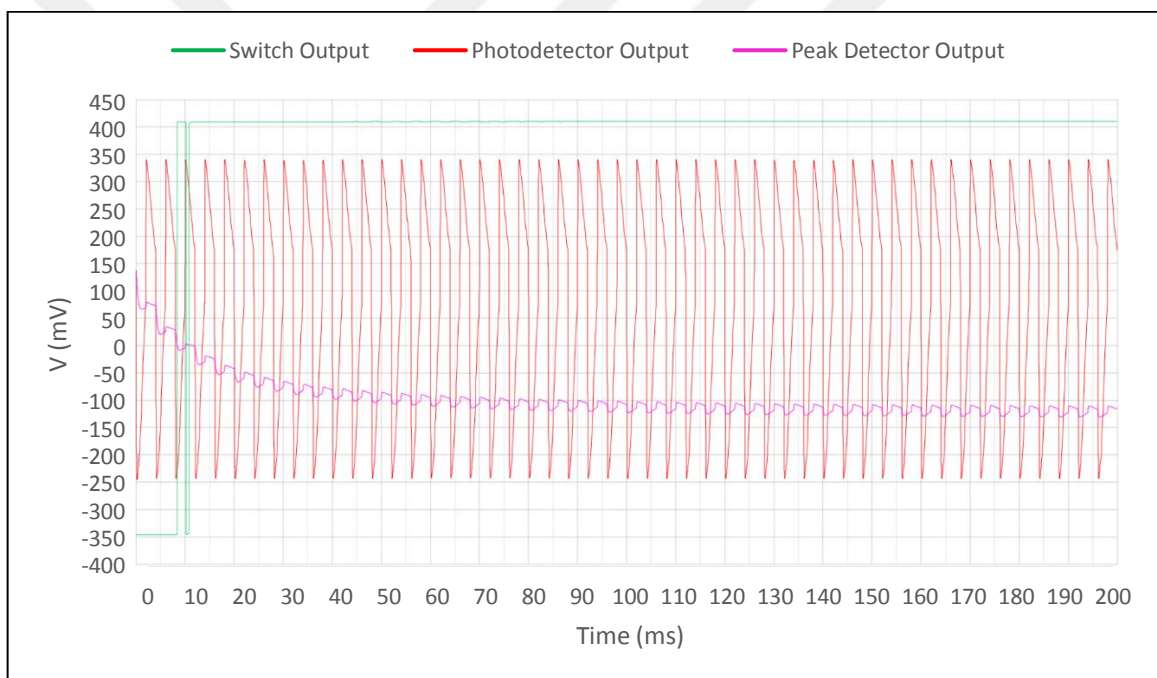


Figure 3.27. Output waveform simulations of the second tapeout

One thing to notice about this new topology is that the swing is bigger, as mentioned and aimed earlier. However, the DC offset point and starting point of the system is at 150 mV. Peak voltage is around 350 mV and level difference between these two points is 200 mV. The negative peak, nevertheless, is around -250 mV and the difference to the DC offset point is 400 mV. This created the necessity to work the peak detector in the negative side. As can be seen in the Figure 3.27, the peak detector charges the capacitor to a level of -100 mV. The switches following this block is designed to have a switching voltage of 0 V and

again as can be seen from the Figure 3.27, at 10 ms, the output switches from -350 mV to 400 mV, logic-0 to logic-1.

To extend the safety of the system and learning from the past tapeout mistakes, corner simulations has been made for this peak detector. In the Figure 3.28, outcome of the corner simulations is given.

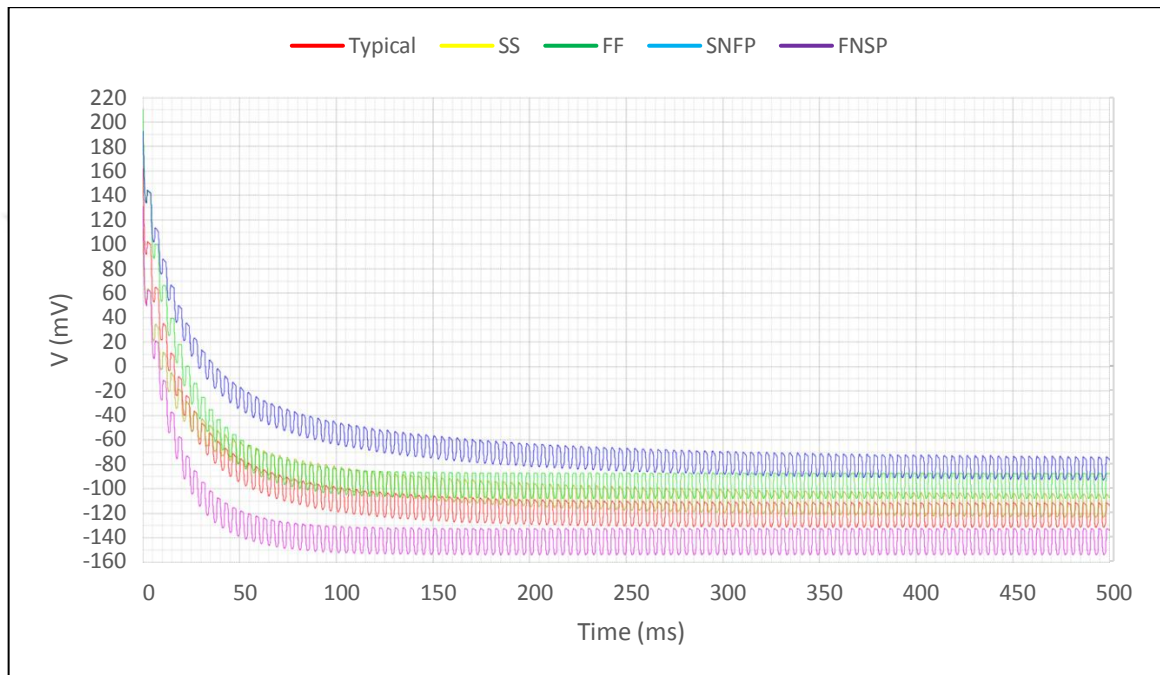


Figure 3.28. Corner simulation results of the peak detector

It is clear that the settling voltage level of all the corners are below 0 V which marks the safety of this structure at different process variations and the layouts can be drawn for tapeout.

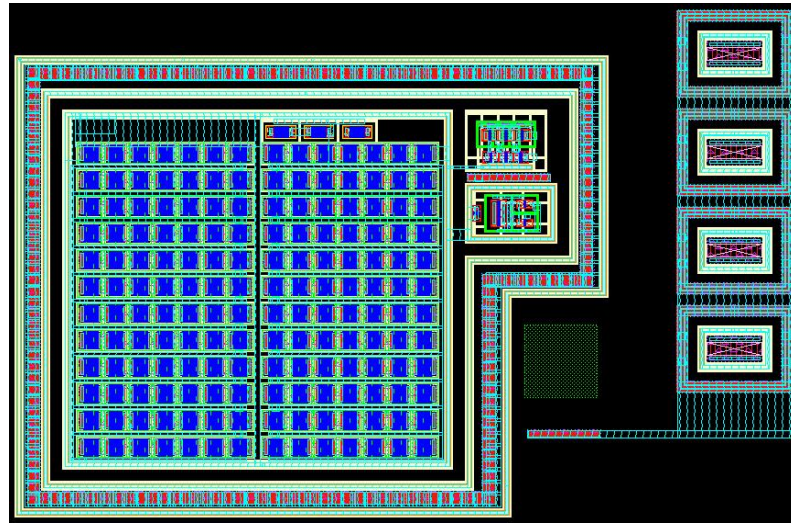


Figure 3.30. Layout of the second tapeout

3.2.2. Measurement Results

The chips have been received from Europractice IC in about 4 months time and measurements have begun. The same light box that is used for the first tapeout has been used for flickering light again. Measurements are conducted in 1 mW/cm^2 conditions and with a 500 Hz. flickering light source. The measurement setup picture and measurement results are given below.

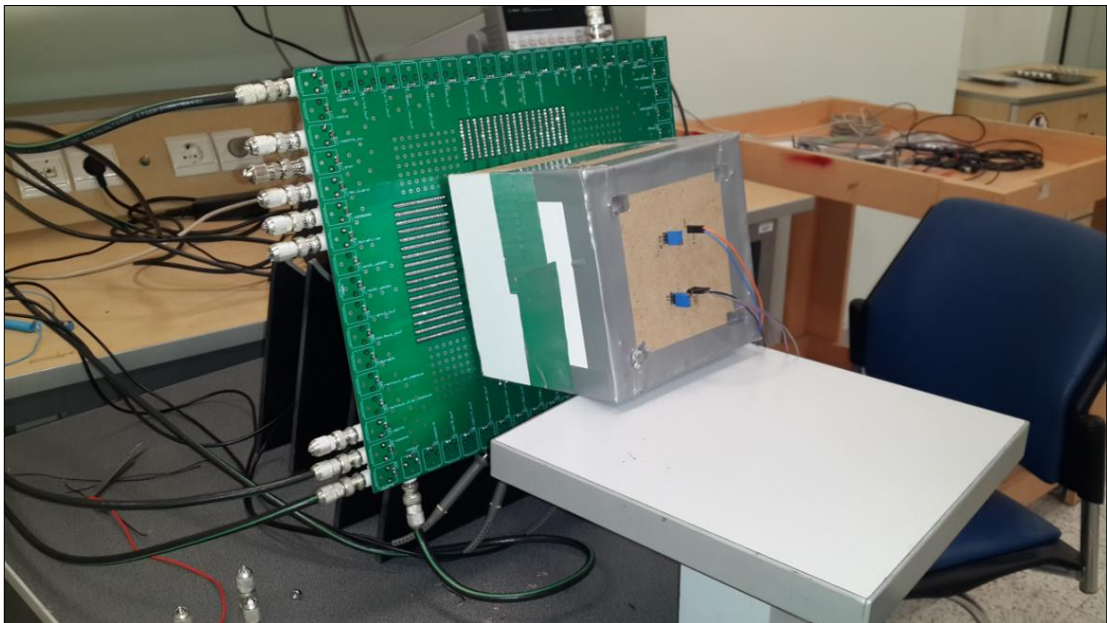


Figure 3.31. Measurement setup of the second tapeout



Figure 3.32. Photomicrograph of the second chip

Photodetector structure designed in this thesis can be seen in the whole system in Figure 3.32. Scribe line dimension specs are met and a compact, novel topology has been realized.

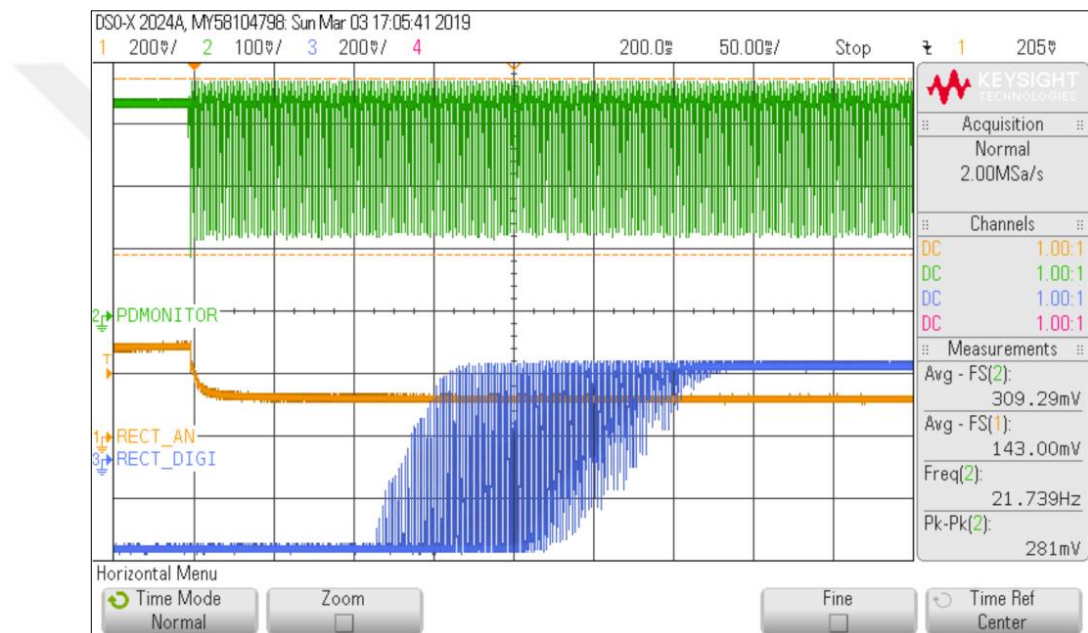


Figure 3.33. On-state measurements of the chip

Green waveform represents the output of photodetector, orange waveform is the output of the peak detector and the blue waveform is the output of the switch. As can be seen in Figure 3.33, after a while from the photodetector starts operating, the peak detector charges the capacitor to a negative level and after a while from that, the switch turns on to logic-1. A close up view to the waveforms are given in Figure 3.34.

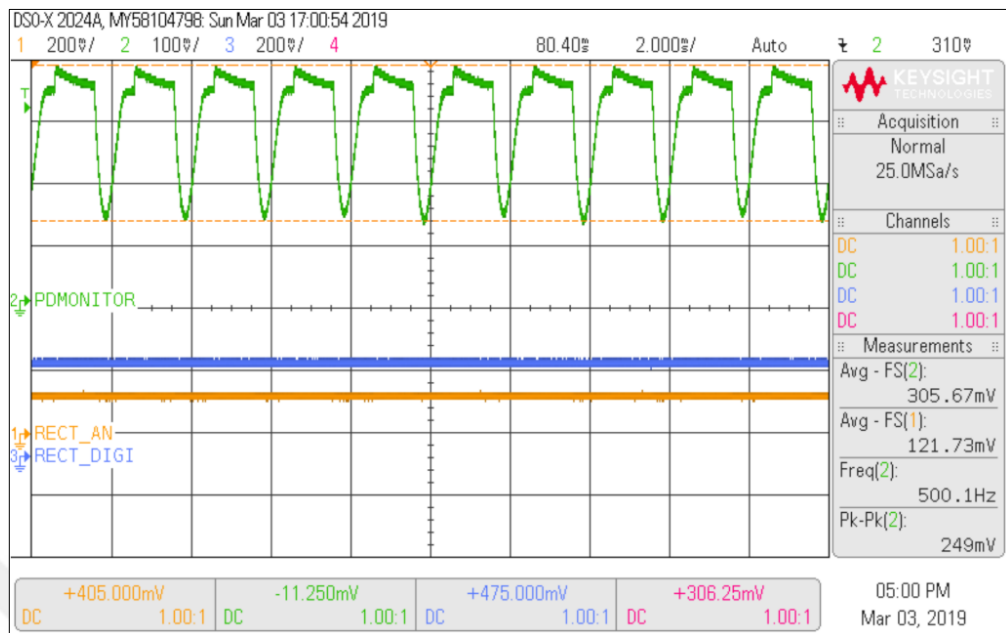


Figure 3.34. Close-up view to the output waveforms

Recalling the simulation results, the realization of the design can be called as a success. Measurement results prove that the integrated selector is working under the 1 mW/cm^2 irradiance and detects a flickering light having the frequency of 500 Hz. And an irradiance 10 percent of the 1 mW/cm^2 , which is 1.1 mW/cm^2 .

4. CONCLUSION

Expensive and time consuming aspects of the scribe line tests are discussed. To this end, a contactless channel-leakage monitor is proposed and applied for a funding. In order to start and select the specific channel leakage monitor, an integrated selector system was needed. The main goal of this thesis was to develop an integrated selector supplied through photovoltaic cells and with an optical receiver. It was necessary to do an intense literature review but little to no papers have been found with the given specs and working conditions. This created a requirement for a novel structure to be designed.

With the funding from TUBITAK, two test chips have been taped out via Europractice with UMC 0.18 μm bulk-CMOS technology.

In the first tapeout, the novel structure for the photodetector has been tested for the first time. It is proven to be working by the measurements, however the subcircuits following this structure were not working properly. This required a design review and a second tapeout.

With the second tapeout, some precautions have been made with the lessons learned from the first tapeout. Rail to rail voltage of the photodetector increased with a positive photodiode addition to the circuit. Also, voltage quadrupler topology has been given up since it is affected highly by the process variations due to high amount of devices working in subthreshold region. Instead of this, a negative peak detector has been designed and used. Single switch topology is also replaced with a ring of three switches to ensure the performance of the switching.

Measurement results from the second tapeout prove that the system is working as it should be. Under 1 mW/cm^2 indoor irradiance, a CMOS integrated selector has been designed, taped out and measured with success.

REFERENCES

1. Weste N, *CMOS VLSI Design: A Circuits and Systems Perspective*. Boston: Pearson; 2010.
2. Çilingiroğlu U, Tar B, Özmen Ç. On-chip photovoltaic energy conversion in bulk-CMOS for indoor applications, *IEEE Transactions on Circuits and Systems I: Regular Papers*. 2014;61(8):2491-2504.
3. Razavi B, *Design of Analog CMOS Integrated Circuits*. Los Angeles: McGraw-Hill; 2016.
4. Transimpedance Amplifier: Wikipedia; [cited 2019 29 April]. Available from: https://en.wikipedia.org/wiki/Transimpedance_amplifier.
5. Albert TH, Cheung MCK, Chodavarapu VP. CMOS Photodetectors. 2011.
6. Park SM, Yoo HJ. 1.25-Gb/s regulated cascode CMOS transimpedance amplifier for gigabit ethernet applications. *IEEE Journal of Solid-State Circuits*. 2004;39(1):112-121.
7. Goswami S, Silver J, Copani T, Chen W, Barnaby HJ, Vermeire B, Kiaei S. A 14mW 5Gb/s CMOS TIA with gain-reuse regulated cascode compensation for parallel optical interconnects. *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*; 2009: IEEE.
8. Tanabe YNA, Soda M. A single-chip 2.4 Gb/s CMOS optical receiver IC with low substrate cross talk preamplifier. *IEEE Journal of Solid State Circuits*. 1998;33(12):2148-2153.
9. Beaudoin F, El-Gamal MN. A 5-Gbit/s CMOS optical receiver frontend. *Circuits and Systems, The 2002 45th Midwest Symposium on*; 2002: IEEE.
10. Çilingiroğlu U, İpek S. A zero-voltage switching technique for minimizing the current-source power of implanted stimulators. *IEEE Transactions on Biomedical*

Circuits and Systems. 2013;7(4):469-479.

