X – BAND 7 BIT MMIC PHASE SHIFTER DESIGN

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

ERDİNÇ ERÇİL

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2006

Approval of the Graduate School of Natural and Applied Sciences

_____

Prof. Dr. Canan ÖZGEN

Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

_____

Prof. Dr. İsmet ERKMEN

Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

_____

Assoc. Prof. Şimşek DEMİR

Supervisor

Examining Committee Members

Prof. Dr. Canan TOKER (METU, EE) _____

Assoc. Prof. Şimşek DEMİR (METU, EE) _____

Prof. Dr. Altunkan HIZAL (METU, EE) _____

Prof. Dr.Nilgün GÜNALP (METU, EE) _____

Mehmet Altuntaş (M.S.) (ASELSAN A.Ş.) _____

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Erdinç ERÇİL

ABSTRACT

X – BAND 7 BIT MMIC PHASE SHIFTER DESIGN

ERÇİL, Erdinç
M.S., Department of Electrical and Electronics Engineering
Supervisor: Assoc. Prof. Dr. Şimşek DEMİR

September 2006, 130 pages

Modern phased array radars require large numbers of electronically controlled phase shifters to steer their beams to the desired direction. The amount of beam steering error depends on the phase resolution of the phase shifters as well as the performance of other parts of the antenna system. The size of the phase shifter in such systems is most of the time needed to be small, which necessitates the MMIC implementation. In the context of this thesis, an X band 7 bit MMIC phase shifter of 2.8125 degree phase resolution, including its layout, is designed using the design kit of OMMIC® Foundry. All bits of the phase shifter are designed to have low return loss so as to minimize the performance degradation due to loading effects upon cascading. Also some structures studied using the design kit of WIN® Foundry are presented. Both designs were performed using ADS®. For the optimum cascading of 7 bits, a MATLAB code was written and used.

Keywords: Digital phase shifter, MMIC, MMIC foundry, pHEMT.

ÖZ

X – BANT 7 BİT MMIC FAZ KAYDIRICI TASARIMI

ERÇİL, Erdinç
Yüksek Lisans, Elektrik Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Doç. Dr. Şimşek DEMİR

Eylül 2006, 130 sayfa

Modern faz dizili anten radarlarında hüzmenin istenen tarafa yönlendirilmesi için çok miktarda elektronik denetimli faz kaydırıcıya gereksinim duyulmaktadır. Bu sistemlerde huzme açısı hatası sistemin diğer elemanlarının performansına olduğu kadar, kullanılan faz kaydırıcıların faz çözünürlüğüne de bağlıdır. Söz konusu sistemlerde kullanılacak faz kaydırıcı boyutlarının küçüklüğü MMIC teknolojisini gerektirmektedir. Bu tez kapsamında OMMIC Firmasının ADS için hazırladığı tasarım kiti kullanılarak X bantta çalışan 7 bit sayısal bir faz kaydırıcı serimi ile beraber tasarlanmıştır. Tüm bitlerin tasarımında, art arda bağlanma sonucu ortaya çıkacak yükleme etkilerini azaltmak amacıyla, her iki porttan geriye dönüş kayıplarının iyi olmasına özen gösterilmiştir Ayrıca WIN Firmasının tasarım kiti ile tasarlanan bazı yapılar da sunulmaktadır. Her iki tasarım da ADS® programında yapılan benzetimler ile gerçekleştirilmiştir. Bitlerin performans açısından en uygun dizilimini tespit etme amacıyla bir MATLAB programı yazılmış ve kullanılmıştır.

Anahtar kelimeler: Sayısal faz kaydırıcı, MMIC, MMIC Firması, pHEMT.

To my beloved family

ACKNOWLEDGEMENTS

I would like to express my sincere appreciation to my supervisor, Assoc. Prof. Şimşek Demir for his support, valuable recommendations and friendly encouragement.

I also wish to present my special thanks to Mehmet Erim İnal and Eralp Atmaca. Their experience and insights enlightened me throughout this work. Also, my thanks go to ASELSAN A.Ş. for all facilities provided.

I would like to acknowledge my gratitude to my friends and colleagues Can Barış Top, Nizam Ayyıldız, Burak Alişan, Bülent Alıcıoğlu and Necip Şahan and my flatmate Ali Haydar Akçay for their morale support and trust.

Finally, I feel grateful to my family, for their patience and understanding.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

ADS ®	:Advanced Design System
AM-PM	:Amplitude Modulation - Phase Modulation
BST	:Barium Strontium Titanate
CMOS	:Complementary MOS
CPW	:Coplanar Waveguide
D/A	:Digital to Analog
DC	:Direct Current
ECM	:Electronic Counter Measures
FET	:Field Effect Transistor
GaAs	:Gallium Arsenide
GSM	:Global System for Mobile Communications
HBT	:Hetero-junction Bipolar Transistor
HP/LP	:High Pass / Low Pass
IC	:Integrated Circuit
IL	:Insertion Loss
LHTL	:Left Handed Transmission Line
LSB	:Least Significant Bit
LVDS	:Low Voltage Differential Signaling
MESFET	:Metal- Semiconductor Field Effect Transistor
MIM	:Metal - Insulator - Metal
MMIC	:Monolithic Microwave Integrated Circuit
MOSFET	:Metal - Oxide - Semiconductor Field Effect Transistor
PCB	:Printed Circuit Board
pHEMT	:Pseudomorphic High Electron Mobility Transistor
PIN	:Positive - Intrinsic - Negative
RF MEMS	:Radio Frequency Micro Electro Mechanical System

RHTL	:Right Handed Transmission Line
SPST	:Single Pole Single Throw
SPDT	:Single Pole Double Throw
TTL	:Transistor - Transistor Logic
TWTA	:Traveling Wave Tube Amplifier

CHAPTER 1

INTRODUCTION

Phase shifters are devices that change the phase of the signals at their output by some means of outside intervention. Most extensive usage area of phase shifters is phased array antennas, where they are most often used together with attenuators so as to obtain the desired complex excitation distribution along the antenna elements. Phased arrays with low sidelobes and low steering errors require digital phase shifters with large number of bits. The number of antenna elements and multi-beam requirements of modern phased array antennas call for small and lightweight phase shifters relying on the MMIC technology. In this study, a seven bit mid X- band MMIC phase shifter to be manufactured by OMMIC foundry of France is designed. Along with the design of this phase shifter, some extra work made with the design kit of another foundry, WIN, is presented.

Digital MMIC phase shifters have been studied extensively in the literature. The studies focus on design while trying to keep the performance of the phase shifter above some specified merit. The domain of studies is generally composed of different topologies and processes. Towards the recent years, the current trend of researchers is to get some MMIC foundry implement the design rather than merely work on theoretical models. Most often, element models or measurements that are obtained from foundries are used in the designs. However, in the early years of MMIC history, the studies used to remain on the theoretical phase. As a matter of fact, while the technology was shifting to MMIC, there was a continuity of circuit topologies that were designed for hybrid circuits.

The first examples of IC phase shifters utilize PIN diodes as switching elements. Work on semiconductor phase shifters using PIN diodes as control elements began in the late 1950's [1]. In the often referred paper [2], along with switched line, loaded line, and reflection types, broadband high pass/low pass filter topologies are

described and evaluated for their performance. Although not specifically meant for MMIC, these topologies have been examined and used very often in MMIC designs. The switching elements are assumed to be diodes and simple analyses on their switching performance was carried out. Equations yielding element values of loaded line and switched three pole HP/LP topologies were derived. It is reported that over almost octave bandwidth ±2° error is achieved with these topologies. The bandwidth performance of large bits is postulated to enhance by increasing the order of filter sections.

Another design in [3] with pin diode switching elements used again HP/LP networks as an alternative to distributed type phase shifters (loaded line, hybrid coupled, switched line). Three pin diodes in TEE configuration are utilized and their on and off state models are included in the design. Low loss was achieved together with 20 % bandwidth within which VSWR remains below 1.5 and phase variation remains within 10 % of nominal.

A monolithic integration example with PIN diodes exists in [4]. In this study, the low loss of the circuit is due to the novel topology proposed. Instead of cascading five bits using SPDTs, SP4Ts are used to divert the signal along 4 different phase paths. By this method the signal is subject to less switching elements and thus the insertion loss as low as 3 dB is accomplished.

While PIN diodes are possible alternatives as control elements in phase shifters, FET phase shifters were studied widely. [5] - [16] are only a few of the FET phase shifter examples. These studies exhibit a variety of bit numbers, topologies, and performances, but common property of all of them is the utilization of FET switches, be they active or passive; GaAs or SiGe; MESFET, pHEMT, or mHEMT transistors.

One of the hottest points in phase shifter studies is the selection or invention of different circuit topologies. Among these topologies, the reflective hybrid coupler, switched line, loaded line and high pass/low pass filter topologies are designed for digital phase shifters. These topologies all depend on switching between networks of different insertion phases. Due to its lumped implementation, high-pass/low-pass

topology is regarded as a good remedy below X band. For the sake of increasing bandwidth performance, the switching elements are sometimes considered as part of filters in [8], [10], [15], [17], [18], [19] and [21] . [15] is also attention taking for its demonstrating usage of silicon MOSFETs as switching elements rather than classical III-V compound semiconductor FETs.

Apart from above topologies which are all transmission type, varactor loaded hybrid couplers are often utilized as reflection type phase shifters (RTPS). At sufficiently high frequencies where the quarter wavelength lines become feasibly short, usually Lange couplers come into help for wideband requirements. As a matter of fact, distributed type phase shifters are most of the time not preferred at relatively low frequencies (below 10 GHz) due to size and cost considerations. Generally variable reflective loads are required for lossless phase shifting and 3 dB couplers are employed for routing the reflected signal. In [20] the topologies of the 90°, 45°, and 22.5° and 11.25° degree sections utilized interdigitated quadrature couplers terminated with FET switched reflective loads. The problem of too much chip area for hybrid couplers is tried to be circumvented by replacing the coupler with a lumped element equivalent of 3 dB 90 degree coupler in [22] where MESFET varactors are used as variable loads. 0.5 mm^2 chip area is reported together with 210 degree continuous phase control and 4.9 dB ±0.9 dB insertion loss.

In [23], the lossless phase shifting advantage and intrinsic match property of passive all pass networks are exploited to have octave bandwidth. It is claimed that the bandwidth could be easily increased using more all pass networks in cascade. Measurements of MIC implementation are reported for the 4 bit prototype: 5 dB insertion loss, with less than ±6° error for each bit is obtained. Also in [24] and [25] active phase shifters with all pass networks switched by HEMTs and HBTs are proposed and designed.

Some of the recent studies on MMIC phase shifters concentrate on the utilization of metamaterials. Metamaterials are the materials having negative permittivity (ε) and/or negative permeability (μ) [26]. The negativeness of these parameters result in the so called “Left Handed Transmission Line” in whose lumped model inductors are

shunt and the capacitors are in series as opposed to the normal “Right Handed Transmission Line”. For LHTL, the phase velocity and the group velocity are not co-directional, which is the usual case for a conventional (right-handed) transmission line. This results in negative electrical length. Switching between a LHTL and RHTL of are same amount but opposite sign electrical lengths, ±3 % error in one octave is reported [27].

In this thesis, the switching elements are the (pseudomorphic high electron mobility transistor) pHEMTs. The famous high pass – low pass switched filter structures are chosen for the 180 and 90 degree bits of the 7 bit phase shifter. For 45 and 22.5 degree bits, the embedded filter approach devised in [10], [14], [15], and [19] are examined and used. As for the smallest three bits, namely 11.25, 5.625 and 2.8125 degrees the amount of phase shift and the required bandwidth of operation allows usage of low pass/low pass filter switching, where the transistors are again embedded in the design of filters as filter elements. The details of the design will be given in Chapter 5.

In Chapter 2, the concept and general operation principles of phase shifters are introduced. Available technology types for production of phase shifters and applications of phase shifters are also given. Digital phase shifter requirements are also defined and clarified for they matter in the design practice.

Chapter 3 focuses on the preliminaries of designing a MMIC phase shifter. Common phase shifter topologies are presented with theoretical examples in the first part, critical component for a phase shifter, FET switch, is introduced in the second part and MMIC foundry issues are mentioned in the third part of this chapter.

Next, in Chapter 4, some practical work done with the design kit of WIN foundry is exhibited. These include the design of necessary SPDT for switched filter topologies and the 180 and 90 degree bits realized with this SPDT.

The backbone of the study within the context of this thesis is given in Chapter 5 & 6. In Chapter 5 the detailed design of the bits of the 7 bit X band phase shifter with the

OMMIC foundry design kit takes place. Individual design, optimization and performance of each bit and finally the entire phase shifter are given in this chapter. The evaluation of different bit arrangement alternatives for the finalized chip takes place in Chapter 6.

Eventually in Chapter 7, comments on the designed phase shifter are presented and possibilities of enhancing its performance are investigated.

CHAPTER 2

A CLOSE LOOK AT PHASE SHIFTERS

2.1. General Considerations

2.1.1. Definition of Phase Shifter

A phase shifter is a two port device that changes the insertion phase between its ports by some means of intervention. As a matter of fact, any network with modifiable phase characteristic could be regarded as a phase shifter, although it may not be a good one.

An ideal phase shifter only modifies the phase of the injected signal, without disturbing the amplitude. A phase shifter has different scattering matrices corresponding to its different states. The phase shift appears in the insertion phase of the signal, and therefore in the phase of S_{21} of the phase shifter. This phase shift is called the **differential phase shift**, because it is the difference of the phases of insertion phases of the two states. The terms phase shift and differential phase shift will be used interchangeably throughout this thesis.

The scattering matrices of an ideal phase shifter with a nominal phase shift setting of $\alpha_2 - \alpha_1$, before and after commanding the phase shift are the following:

State 1:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} 0 & e^{j\beta_1(\omega)} \\ e^{j\alpha_1(\omega)} & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2\text{-}1)$$

State 2 (Upon commanding the phase shift):

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} 0 & e^{j\beta_2(\omega)} \\ e^{j\alpha_2(\omega)} & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2\text{-}2)$$

From the matrices, it is apparent that the phase shift observed in the signal is equal to $\alpha_2 - \alpha_1$. The phase shift in the other direction is equal to $\beta_2 - \beta_1$, which may or may not be equal to $\alpha_2 - \alpha_1$. If they are equal, the phase shifter is said to be reciprocal; and if they are not, the phase shifter is said to be non-reciprocal.

The phase shift, $\alpha_2 - \alpha_1$, is not a function of frequency for an ideal phase shifter; that is, it is constant over the entire bandwidth of the phase shifter. It must be noted that, this does not necessitate α_1 and α_2 to be constant individually over that bandwidth.

As seen, the ideal phase shifter does not change the amplitude by definition. Also it is perfectly matched at its two ports.

On the other hand, the S matrices of a non-ideal phase shifter adjusted to shift the phase by $\alpha_2 - \alpha_1$ are given below:

State 1:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11}{}^1(\omega) & \left|S_{12}{}^1(\omega)\right| e^{j\beta_1(\omega)} \\ \left|S_{21}{}^1(\omega)\right| e^{j\alpha_1(\omega)} & S_{22}{}^1(\omega) \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2\text{-}3)$$

State 2:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11}{}^2(\omega) & \left|S_{12}{}^2(\omega)\right| e^{j\beta_2(\omega)} \\ \left|S_{21}{}^2(\omega)\right| e^{j\alpha_2(\omega)} & S_{22}{}^2(\omega) \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2\text{-}4)$$

Referring to parameters in (2-3) and (2-4) , following could be said:

- $|S_{21}^1(\omega)|$, $|S_{21}^2(\omega)|$, $|S_{12}^1(\omega)|$, and $|S_{12}^2(\omega)|$. are not necessarily equal and are not equal to one.
- $S_{11}^1(\omega)$, $S_{22}^1(\omega)$, $S_{11}^2(\omega)$, and $S_{22}^2(\omega)$ are not equal to 0.
- $\alpha_2(\omega) - \alpha_1(\omega)$ might not be exactly equal to the desired phase shift $\alpha_2 - \alpha_1$ at any frequency.
- $\alpha_2(\omega) - \alpha_1(\omega)$ and $\beta_2(\omega) - \beta_1(\omega)$ are not constant with frequency.

These facts imply the following about a practical phase shifter:

- Amplitude imbalance exists between two states of a phase shifter.
- A finite return loss is suffered by the phase shifter.
- The commanded phase shift and the resultant phase shift may not be exactly equal.
- Phase shift is not perfectly frequency independent.

2.1.2. Phase Shifter and Time Shifter

A time shifter is a type of phase shifter with linear phase shift characteristic w.r.t frequency. The amount of differential phase shift of the time shifter is proportional to the frequency. This fact results in constant differential group delay; that is, no matter what the frequency of the signal is, the difference of delays between the two states of the time shifter is constant. For this reason, a time shifter is usually called as a true time delay network. A time shifter is not a good phase shifter, considering the definition of ideal phase shifter; but its constant time delay property is the heart of wideband squintless beam steering of a phased array antenna. The reason of this requirement will be explained later in this thesis.

2.1.3. Phase Shifter Applications

Phase shifters are the critical elements of electronically scanned array antennas. These antennas are also called phased array antennas, which imply the role of phase shifter in the system. Used together with attenuators, they suffice to determine the distribution of the excitation of the antenna elements and thus the instantaneous pattern of the antenna. They could be used as a part of both the transmit and receive

antennas. Apart from the phased arrays, they are used in both analog and digital phase modulation. As an electronic warfare application, serrodyning or frequency translation is accomplished by continuously varying the phase of the phase shifter and obtaining the desired Doppler profile to deceive the engaged system [30]. Another application area is the power amplifiers, where phase shifting feedback networks are used to compensate for AM-PM distortion and other nonlinearities [29]. Phase shifters are also used in various microwave measurements.

2.1.4. Phase Shifter Classification

Phase shifters can be classified according to their various properties. Most basic classification would be on the basis of adjustability: A phase shifter is either a fixed phase shifter or an adjustable one. It is obvious that an adjustable phase shifter can always be used instead of a fixed one, but cost and design complexity would certainly favor a fixed phase shifter. Fixed phase shifters find their application area in Butler matrices and single channel monopulse converters[28]. Adjustable phase shifters are, on the other hand, one of the most critical elements in a scanned phased array antenna system.

Phase shifters are also divided into two parts according to the type of effort during adjustment: They are either mechanical or electronic. Electronic phase shifters are superior over their mechanical counterparts due to their inertialess phase shifting capability. In mechanical phase shifters, the phase shift is provided via some means of mechanical movement, such as rotating a knob; while it is usually of voltage controlled nature in electronic phase shifters. This difference of nature of phase change mechanisms between two types result in different state-change times as well. Electronic phase shifters are certainly much faster in operation than mechanical ones.

Another classification of phase shifters is according to the reciprocity of these devices. A reciprocal phase shifter could be utilized in both directions, but a non-reciprocal one usually offers haphazard phase and amplitude characteristics in the non-nominal usage direction.

An important category is the type of operation, being analog or digital. Digital phase shifters, as the name implies, have finite number of phase states and can not be operated to provide an arbitrary phase shift. On the other hand, analog phase shifters permit continuous insertion phase variation or in other words analog phase shifters have infinite phase resolution. Digital phase shifters are more compatible with the computerized systems, but an analog phase shifter can always be operated as if it is a digital one with the proper D/A and possibly a voltage leveling interface circuitry. A digital phase shifter has a truth table composed of some bits for reference to its different phase states. For an analog phase shifter, however, there exists some "control voltage to insertion phase transfer curve" used for correctly having the desired phase shift. A digital phase shifter is named after its number of bits, implying its angle resolution, while an analog phase shifter is addressed with its sensitivity. An obvious disadvantage of an analog phase shifter is the susceptibility of the phase shift due to slight variations in the control voltage. A digital phase shifter however, is insensitive to such small variations because the transistors are usually well-pinched off below their pinch-off voltage, keeping their insertion phase almost indifferent to the poorly regulated control voltages.

Hybrid approaches exist in the literature, where most of the phase shift is of digital nature but an analog bit of 11.25° is allocated fine tuning [31].

According to the transmission media employed to implement the phase shifter, a further classification can be done. Phase shifters can be realized in various media such as waveguide, planar transmission line, fin line and dielectric guide [28].

Finally, the technology of fabrication is an important discriminative property of phase shifters. Among these technology types are mainly ferrite, hybrid IC and MMIC. Also in the recent years, although not so mature as the classical IC's, RF MEMS takes its place among IC phase shifters. Ferrite phase shifters are bulky but they dominate over hybrid IC and MMIC in terms of loss and power handling capability. MMIC or in general IC phase shifters are superior to ferrite phase shifters with respect to size, weight and cost. They are incomparably smaller than ferrite phase shifters and once design is fixed, MMIC processes offer low cost phase

shifters in mass production. The logic behind phase shifting mechanisms in ferrite and IC phase shifters are quite different. Phase shifting with ferrites is usually accomplished by the change in magnetic permeability which occurs with application of a magnetic biasing field [32]. On the other hand, analog or digital voltages provide variation of the equivalent circuits represented by semiconductor circuit elements in IC type phase shifters.

In the context of this study, digital MMIC phase shifters are focused on, investigated and designed. Other types of phase shifters are mentioned shortly, wherever they are necessary for the sake of completeness.

2.2. Integrated Circuit Phase Shifters

The advent of IC technologies influenced the destiny of phase shifters profoundly as well as all other electronic circuits. Like all other microwave circuits, phase shifters enjoyed the benefits offered by IC approach. The principal advantage of IC phase shifters over waveguide phase shifters is the size of the circuit. Today's two dimensional phased arrays of thousands of elements would be impractical without IC phase shifters. Waveguide phase shifters are still not abandoned completely, they are critical in high power applications. They also have smaller insertion losses, which make them indispensable in certain transmit antenna applications. However, the common trend is to use IC phase shifters wherever possible. The term IC is a general term and could be separated into these parts:

- Hybrid IC (MIC)
- MMIC
    - Silicon
    - Compound Semiconductor (GaAs, InP, SiGe…)
- RF MEMS
- BST (Barium Strontium Titanate)

2.2.1. Hybrid IC (MIC)

Hybrid IC phase shifters are a blend of different technologies, as the name implies. The switching elements are chip diodes or transistors, but together with the passive elements and lines they are in PCB form. With hybrid IC's post-production tuning is possible. Furthermore, failures can usually be easily detected and fixed. However, unit to unit repeatability of hybrid IC's is low and their high frequency performance is poor. On the other hand, the cost of unit area of chip is quite low, which is an advantage of hybrid production in favor of design flexibility.

2.2.2. MMIC

The term MMIC stands for Monolithic Microwave Integrated Circuit. All passive and active elements are on the same substrate and thus no soldering is necessary in this technology. Indeed, the sizes of MMICs are so small that soldering is not possible. MMIC approach is suitable for mass production due to nature of the process that yields the chips. For MMICs post-production tuning is impossible and failure diagnosis is extremely difficult. Nevertheless, if the design is successful, the yield of a run is quite satisfactory as compared to hybrid IC's. As for the high frequency behavior, the choice of substrate material matters, although in any case MMIC dominates over hybrid circuits. Thanks to five times higher electron mobility of GaAs w.r.t Silicon, GaAs offers quite larger f_t's than Silicon. MMIC phase shifters with III-V compound semiconductor substrates are the most common ones among all types of IC phase shifters.

2.2.3. RF MEMS

RF MEMS is a newly emerging technology, but due to low-loss switching and fine capacitance variation capability, it is a suitable technology for producing digital and analog phase shifters. RF MEMS is quite cheaper than MMIC and bear similar advantages of MMIC over hybrid approach. The undesired point of RF MEMS is the restriction of switching life time, switching speed, power handling capability, reliability, etc due to various modes of failures including metal failure and dielectric

charging. However, RF MEMS appears to be promising in terms of cost per chip, due to less number of process steps as compared to MMIC production.

2.2.4. BST (Barium Strontium Titanate)

BST is also a new technology used for producing phase shifters. BST is a type of ferroelectric material whose dielectric constant changes with value of the electric field applied. With this property, the capacitance per unit length of a microstrip transmission line can be varied. This results in the modification of the phase velocity along the line, which can be exploited to shift the phase by moderate amounts. Also varactors and therefore analog phase shifters can be created with the same idea [29].

2.3. Digital Phase Shifters

The insertion phase of digital phase shifters can be switched to quantized levels that are determined in the design stage. As opposed to an analog phase shifter, there is finite number of states of the phase shifter, depending on the number of phase shifter bits. There exists a reference state with a nonzero insertion phase. When measured differentially the other states' phases lead or lag this reference phase by certain angular increments. An n bit phase shifter has insertion phase increments of $360/2^N$. To illustrate the operation for a 3 bit phase shifter, **Table 2.1** can be examined:

Table 2.1 Nominal insertion phase of a three bit phase shifter at its 8 progressive states

State	Insertion Phase	State	Insertion Phase
000	φ0	100	φ0 + 180
001	φ0 + 45	101	φ0 + 225
010	φ0 + 90	110	φ0 + 270
011	φ0 +135	111	φ0 + 315

Also available from the table is that, all bits are not of the same power of changing the insertion phase. For instance, one could pass from state 000 to state 100 encountering a phase change of 180º. Therefore, bits exist with their significance, that is the most significant bit controls 180º and the least significant bit controls 45º. For any digital phase shifter, the most significant bit always controls 180º, but the least significant bit controls $(360/2^N)$º where N stands for the number of phase shifter bits.

The general structure of an N bit digital phase shifter is presented in **Figure 2.1**

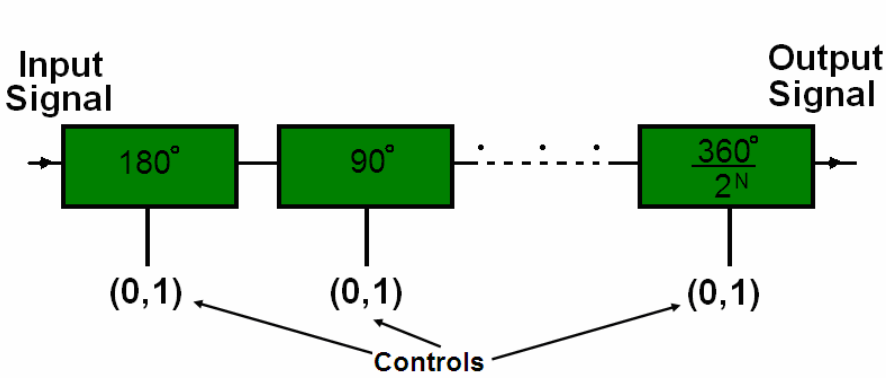

Figure 2.1 General digital phase shifter structure

From the figure, it is apparent that the phase bits are in cascade form. This structure provides the cumulative nature of the insertion phase, i.e. the signal is subject to the addition of the insertion phases of all blocks. Each block shifts the phase of the signal by the amounts indicated in the figure, thus it is possible to have all phase states by $(360/2^N)$ º degree steps.

An alternative method would be having the smallest bit as a unit and repeating it in series 2^N times. In that case, the design could be easier, but intolerable insertion loss would probably be suffered due to cascade nature of 2^N networks instead of N networks. Thus the usual approach is to have N bits of binary-increasing weights.

2.3.1. The Bit Concept

Meant by a "bit" of a digital phase shifter is a circuit that can be operated in two different states with respect to the insertion phase. At one state, the signal "sees" one circuit and at the other state it sees a different one. The phase shift is introduced by the difference of the phase incursions of these two circuits. The change in the circuit topology is provided through some switching devices. For a solid state phase shifter, available switch devices are PIN diodes, FETs mainly. For an RF MEMS type phase shifter, for example, circuit topology is varied by means of MEMS switches. The basic approach in both semiconductor and MEMS technology is to have SPDTs switching between two different networks of different phase responses. **Figure 2.2** represents this action. The isolation of SPDTs are often tried to be maximized such that only one network is effectively active at a time. Ideally, one would design two networks with desired phase and amplitude characteristics and there would be no difference in the performance of the phase shifter bit upon insertion of SPDTs as in the figure. However, finite isolation of SPDTs is a practical problem and the a-posteriori performance is usually quite different than that of the design made depending on ideal switch assumption. Therefore, noticing that responses in both states are those of two unequally fed parallel networks; the switches usually become a part of the design process.

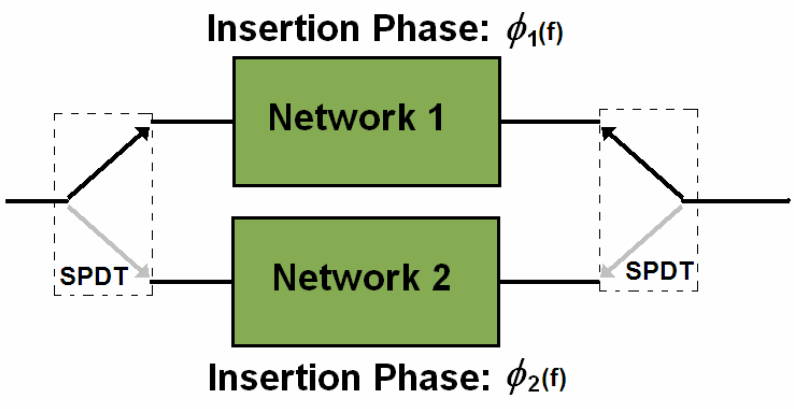

Figure 2.2 The basic phase shifter structure

2.3.2. The Number of Bits in a Phase Shifter

The number of bits of a digital phase shifter determines its phase shift resolution. Phase shift resolution is doubled upon addition of a single bit. The LSB (Least Significant Bit) of a 4 bit phase shifter is 22.5º degrees while that of a 5 bit phase shifter is 11.25º. Nonetheless, it might not be meaningful to have an 8 bit phase shifter (with 1.4º resolution) due to practical facts, i.e. phase variation over frequency. Especially for a wideband phase shifter there is always phase error and usually as the number of bits increases, so does the ratio of phase error to the phase resolution. Therefore it is futile to have very small phase steps (or many bits) unless the phase error is significantly less than the step size.

In a phased array application, the relation between the beam steer angle, θ, and the progressive phase shift, δ, between antenna elements is given as:

$$\delta = k_0 \sin\theta \qquad (2\text{-}5)$$

where k_0 is the wavenumber and θ is defined as the angle between the array boresight and the beam direction.

As the minimum progressive phase shift is equal to the LSB of the phase shifters employed in the array, the resolution of the phase shifter directly determines the steering resolution of the phased array.

However, in a large array, a number of adjacent elements can be considered as a subgroup and be fed equiphase. The next subgroup of elements is again fed equiphase w.r.t. each other but with the smallest possible phase increment w.r.t the previous group. By this method, effective phase resolution is increased by the number of elements in the subgroups.

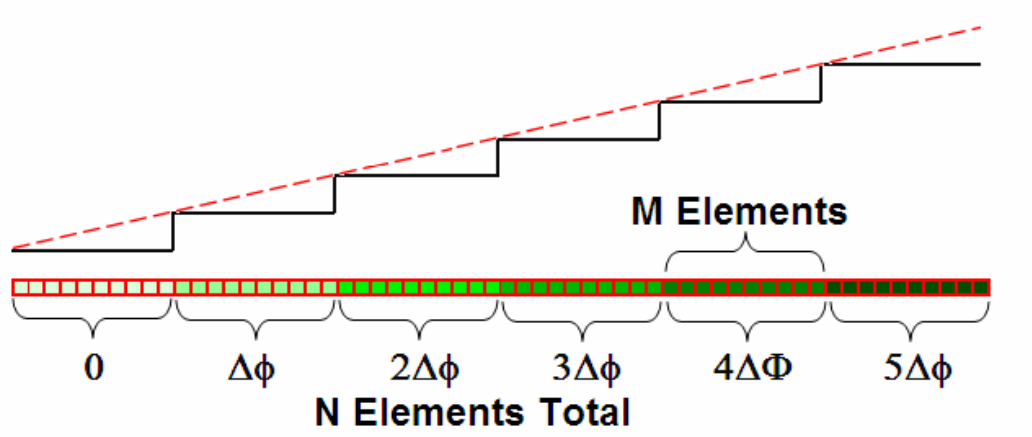

Figure 2.3 The method of virtually increasing the phase shift resolution in a phased array antenna

Referring to the figure, if Δφ is the minimum step size of the phase shifters used in the array, the feeding shown approximates the feeding scheme where the minimum step size is Δφ/M and each antenna element's phases is progressed from the previous element by this much phase. Of course this is only an approximation and the system suffers from grating lobes at smaller scan angles as compared to a system with phase shifters of resolution Δφ/M.

2.3.3. Digital Phase Shifter Requirements

2.3.3.1. Phase Flatness

There is always some phase shift error in the nominal bandwidth of a phase shifter. Ideally, a phase shifter would provide constant phase shift over the entire bandwidth, but this is impossible in practice. Usually the designer adjusts the phase shift to be the desired value in the band center and allow some variation around this value. The maximum allowable phase error depends on the application but it is meaningless to have it larger than phase resolution for any phase shifter.

Opposed to this requirement, a switched line phase shifter has inherently linear phase shift characteristics with frequency, because the phase shift depends merely on the difference between the electrical lengths of the two lines. It turns out that a switched

line phase shifter is a time shifter indeed. However this could sometimes be desirable: When operating a phased array over a bandwidth and when the beam is required to remain untilted as the frequency is varied, it is best to have linear phase shift characteristics. With this feature, the progressive phase shift between array elements increases in proportion with the frequency, which provides true time delay. Therefore the signals from all elements are added in phase at the same angle at all frequencies. If, on the contrary, the phase characteristic is flat, the beam is tilted as the frequency changes, which could result in angle errors in detection.

2.3.3.2. Number of Bits

The number of bits of a digital phase shifter determines the phase steps. For a phased array application, this is critical since the minimum progressive phase shift is equal to the minimum phase step of the phase shifter.

2.3.3.3. Amplitude Imbalance

An ideal phase shifter does not affect the magnitude while changing the phase of the signal passing through it. However, in practice, from state to state there is some change in the amplitude of the signal. Moreover this change is a function of frequency. This modification of amplitude is undesirable. In communication circuits this phenomena would result in PM/AM conversion. Furthermore, for a phased array with some desired tapering, amplitude imbalance may result in undesired perturbation of the amplitude distribution while steering the beam of the antenna. The sidelobe levels might increase a few dBs unless the amplitude imbalance is low enough or there exists variable attenuators that could correct the amplitude terms. It is best to keep the amplitude imbalance as low as possible to have a phase shifter that can be used at any system, possibly an array with amplitude tapering.

2.3.3.4. Insertion Loss

The insertion loss is of course something undesirable, but it could be tolerated if it is not too high. While evaluating the insertion loss of a phase shifter, the number of bits must be taken into account in order not to be too harsh or too tolerant. Usually it is logical to have more insertion loss with more bits, because the bits are in cascaded form. With other properties being the same, a 4 bit phase shifter with 6 dB insertion

loss could be counted more useful than a 3 bit phase shifter with 5.9 dB insertion loss. Furthermore, the bandwidth of the phase shifter is also important. To have a wider bandwidth (in terms of phase flatness for example), more insertion loss could be tolerated.

2.3.3.5. Return Loss

As in almost all microwave circuits, the return loss of a phase shifter is somehow critical. The phase shifter is usually only a part of a more complex system. To be able to operate the phase shifter as desired and also not to disturb peripheral circuits of the phase shifter, the return loss must be as low as possible. The first example that comes into mind is a beam-forming network where the phase shifter is most probably cascaded with an attenuator. If the return loss is not sufficiently low, several perturbations over the attenuator and phase shifter settings might be necessary to finely tune the strip to the desired amplitude and phase setting. This is partly a result of reflections between the phase shifter and the attenuator.

2.3.3.6. Switching Speed

The switching speed is a measure of how quick the phase shifter responds to a change in the desired phase setting. Therefore the importance of the switching speed depends on the application. In the most famous application area, the phased array antenna, the switching speed determines the beam steering speed. In the modern electronic warfare age of complex track and search and ECM environment the required beam steering period might be in the order of microseconds. For IC phase shifters the switching speed depends upon the technology and the circuit topology. On the other hand, for ferrite phase shifters, the hysteresis characteristic of the ferrite material is the main factor influencing the switching speed of the device. As for the mechanical phase shifter, though not digital, the rate of phase change is obviously very poor.

2.3.3.7. Driver Voltages

Digital phase shifters are operated by means of digital signals controlling the gate bias (for a FET type phase shifter) or the electrode voltage (for a PIN diode phase shifter). It is usually necessary to have a level translation circuit between the gates or

electrodes and the digital signals of the control system. For example, negative voltages are required to pinch off a depletion type MESFET, while CMOS; TTL or LVDS voltages might be common to elsewhere in the system. This level translation could be on the chip or, an extra interface could handle this job, freeing the designer of the phase shifter form adding the driving circuitry to the chip.

2.3.3.8. Bandwidth

Certainly, the bandwidth of a phase shifter is very important, but the bandwidth is defined considering the degradation of some of the above mentioned parameters with frequency such as phase flatness, insertion loss, and amplitude imbalance. The bandwidth of the phase shifter is between the two extreme frequencies where these parameters remain within tolerable limits.

2.3.3.9. Power Handling

The power handling requirement of a phase shifter depends on the application. A phase shifter in the transmit array of a satellite antenna may have to operate well with power levels of several hundred watts coming from a TWTA, while a phase shifter on the receive strip of a T/R module is required to operate at a few milliwatts.

2.3.3.10. Size

The size is a critical issue in some aspects. First, at the user's side, smaller is almost always favored, because it leads to smaller system and more room remains for something else. Second, at the designer's side; considering an IC phase shifter, smaller chip size results in either less area on the wafer for the same number of chips, or more chips on the same area.

CHAPTER 3

DESIGN OF MMIC PHASE SHIFTERS

3.1. Common Phase Shifter Topologies

3.1.1. Switched Line Phase Shifters

The most basic transmission type phase shifter is the switched line phase shifter. As the name implies, there are two lines of different electrical lengths, which are switched to yield the desired phase shift. The return loss of the switched line phase shifter is determined by the line impedances with the SPDT switches considered ideal. Therefore, selecting the lines matched to the desired characteristic impedance, return loss is taken granted and the design is relaxed. Another relaxing factor having the inherent matching is that the magnitude of the return loss does not change from state to state, thanks to lossless lines. The following figure represents the switched line phase shifter:

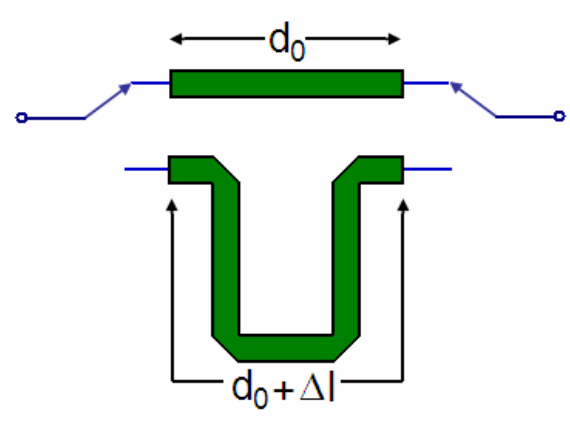

Figure 3.1 Topology of the switched line phase shifter

The electrical lengths of the lines are the physical lengths times the propagation constant β:

$$\theta_1 = \beta d_0$$
$$\theta_2 = \beta(d_0 + \Delta l) \qquad (3\text{-}1)$$

Switching between the lines results in a differential phase shift proportional to the difference between the lengths of the lines:

$$\Delta\phi = \theta_2 - \theta_1 = \beta\Delta l \qquad (3\text{-}2)$$

Apparent from the result is that, the phase shift offered by the switched line phase shifter is proportional to the frequency due to the frequency dependence of β.

3.1.1.1. Sample Design

Here is the simulation result of an ideal switched line phase shifter designed to shift the phase by 90° @ 9.5 GHz:

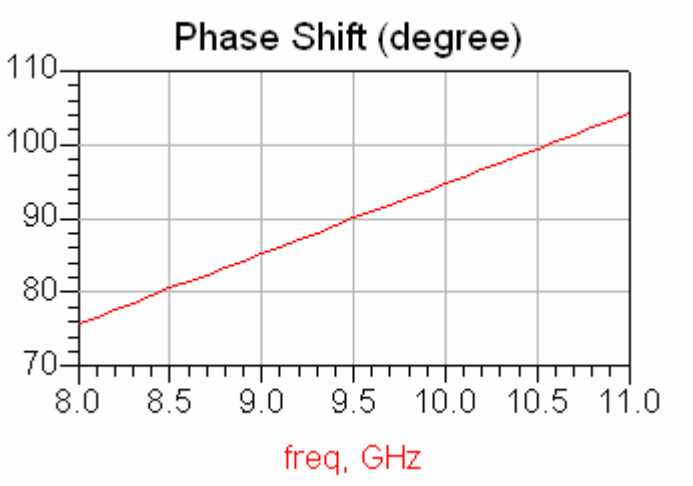

Figure 3.2 Differential phase shift of the ideal switched line phase shifter

The proportionality of the differential phase shift is readily observed in **Figure 3.2**. As mentioned before, this is due to the constant time delay between the two paths in the phase shifter.

The loss, the amplitude imbalance and the return loss of the ideal switched line phase shifter is not necessary to be presented here because they are perfect. Of course, the design is not this simple when the practical switches and transmission lines are employed.

3.1.2. High Pass - Low Pass Type Phase Shifters

It is known that a low pass filter with series inductors and shunt capacitors introduces phase delay whereas a high pass filter composed of series capacitors and shunt inductors introduces phase advance. Upon proper selection of the element values in these networks, it is possible to have their insertion phases track each other with almost constant offset within an appreciable band. For a typical phase shifter application, it is also required that the insertion losses of both networks are low and close to each other. Therefore both filters must be operated within their passband and this passband should certainly be common to both filters. The two options, TEE type and PI type HP/LP networks are given in **Figure 3.3** and **Figure 3.4**. In a phase shifter application, there is no drawback in having one filter in TEE configuration and the other in PI configuration.

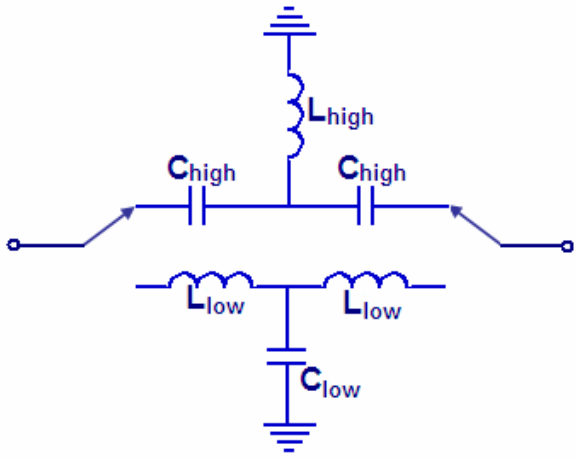

Figure 3.3 TEE type LP/HP phase shifter

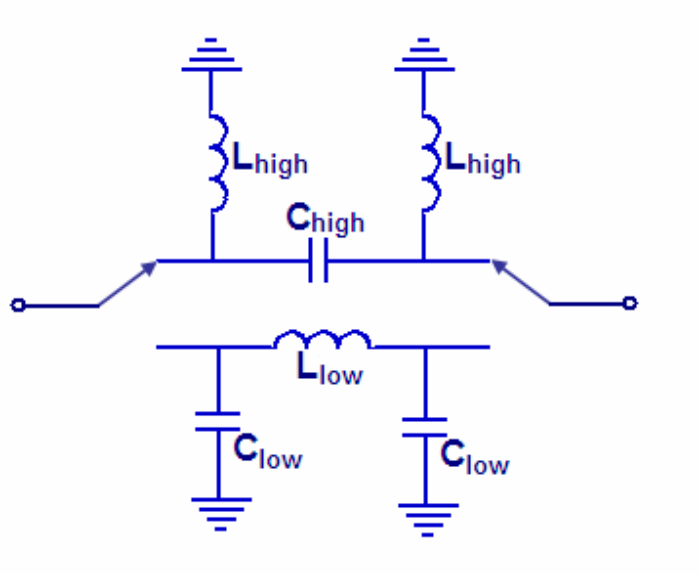

Figure 3.4 PI type LP/HP phase shifter

In order to derive the element values of the filters, S parameters of the filters must first be obtained. It is best to use ABCD to S parameter transformation for the ladder type networks because the ABCD matrix of a cascade connection is simply the product of the individual ABCD matrices of the series and shunt components. The ABCD matrix of a series element with impedance Z seen in **Figure 3.5** is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \qquad (3\text{-}3)$$

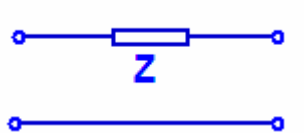

Figure 3.5 Series impedance Z

Similarly, the ABCD matrix of a shunt admittance Y is given as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \qquad (3\text{-}4)$$

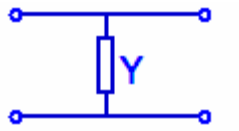

Figure 3.6 Shunt admittance Y

Hence the ABCD matrix of a TEE type network is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1+YZ & 2Z+YZ^2 \\ Y & 1+YZ \end{bmatrix} \qquad (3\text{-}5)$$

Using this expression, the ABCD parameters of the network in **Figure 3.7** is found as in:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1-BX & 2jX-jBX^2 \\ jB & 1-BX \end{bmatrix} \qquad (3\text{-}6)$$

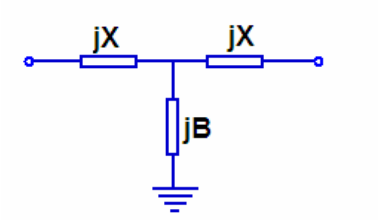

Figure 3.7 Generic TEE type network

The insertion loss of any network (inserted into a Zo Ω system) is derived from its ABCD matrix as:

$$S_{21} = \frac{2}{A+B/Zo+CZo+D} \qquad (3\text{-}7)$$

Applying this transformation for the network in **Figure 3.7**,

$$S_{21} = \frac{2}{2(1 - B_N X_N) + j(B_N + 2X_N - B_N X_N^{\,2})} = \frac{2}{2(1 - BX) + j(BZo + 2X/Zo - BX^2/Zo)} \qquad (3\text{-}8)$$

It is readily seen that the magnitude of S_{21} will remain the same, but the phase of S_{21} will change sign, if a network with $-jX_N$ and $-jB_N$ is considered. This idea is explained in the following figure.

In **Figure 3.8**,

$$B_N = BZo$$
$$X_N = X/Zo \qquad (3\text{-}9)$$

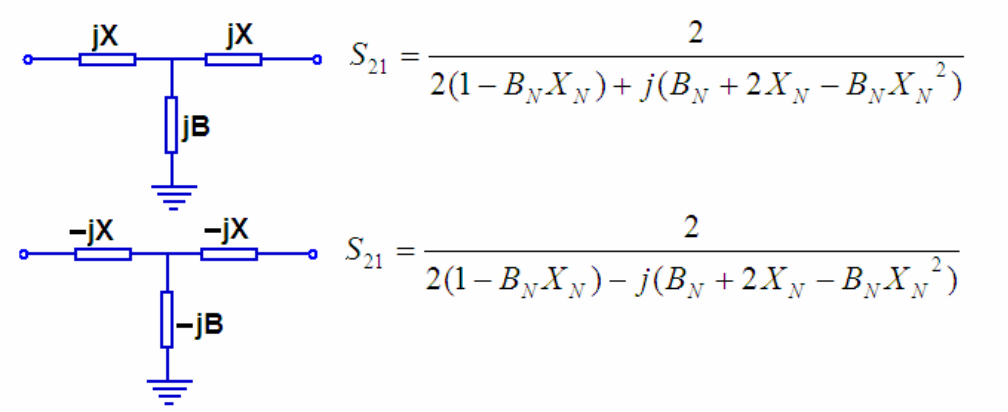

Figure 3.8 The insertion loss comparison of the two T type networks

The equality of the magnitudes of susceptance and reactance values of the two networks is valid only at a single frequency, which is to be selected as the center frequency of the phase shifter.

The low pass filter is the one with positive reactances and susceptance and the high pass filter is the other network.

The insertion phases of these networks are derived from the S_{21}'s as:

$$\phi^{high} = \tan^{-1}\left[\frac{B_N + 2X_N - B_N X_N^2}{2(1 - B_N X_N)}\right] \qquad (3\text{-}10)$$

$$\phi^{low} = \tan^{-1}\left[-\frac{B_N + 2X_N - B_N X_N^2}{2(1 - B_N X_N)}\right] = -\tan^{-1}\left[\frac{B_N + 2X_N - B_N X_N^2}{2(1 - B_N X_N)}\right] \qquad (3\text{-}11)$$

The differential phase shift is found by taking the difference of the insertion phases of the two networks:

$$\phi^{Diff} = \phi^{high} - \phi^{low} = 2\tan^{-1}\left[\frac{B_N + 2X_N - B_N X_N^2}{2(1 - B_N X_N)}\right] \qquad (3\text{-}12)$$

The element values B_N and X_N are related to each other by the requirement of perfect match or zero insertion loss; in a lossless network these conditions are equivalent. Therefore imposing zero insertion loss, the relation between B_N and X_N is obtained:

$$B_N = \frac{2X_N}{1 + X_N^2} \qquad (3\text{-}13)$$

Inserting in the differential phase shift expression, X_N and thus B_N can be obtained:

$$X_N = \tan\left(\frac{\phi^{Diff}}{4}\right) \qquad (3\text{-}14)$$

$$B_N = \sin\left(\frac{\phi^{Diff}}{2}\right) \qquad (3\text{-}15)$$

A similar analysis can be carried out for the PI type circuits, however using the TEE – to – PI transformation as in **Figure 3.9**, this effort could be circumvented.

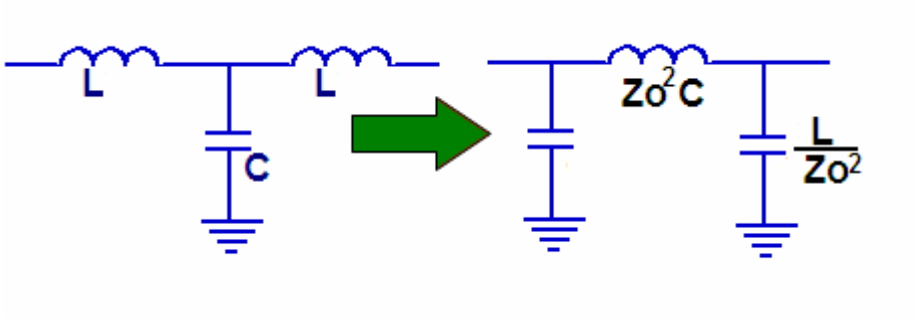

Figure 3.9 TEE to PI conversion

The normalized reactance of a series inductance L is given by:

$$X_{NN}^{Tee} = \frac{\omega L}{Zo} \qquad (3\text{-}16)$$

The normalized susceptance of a shunt capacitance C is given by:

$$B_N^{Tee} = \omega C Zo \qquad (3\text{-}17)$$

In the PI type circuit,

$$X_N^{pi} = \frac{\omega Zo^2 C}{Zo} = \omega C Zo \qquad (3\text{-}18)$$

and

$$B_N^{pi} = \frac{\omega L}{Zo^2} Zo = \frac{\omega L}{Zo} \qquad (3\text{-}19)$$

It is obvious that the B_N of the TEE type circuit becomes the X_N of the PI type circuit and vice versa. Thus, for a PI type phase shifter network that is supposed to provide a differential phase shift of ϕ^{Diff} ,

$$X_N = \sin\left(\frac{\phi^{Diff}}{2}\right) \quad (3\text{-}20)$$

$$B_N = \tan\left(\frac{\phi^{Diff}}{4}\right) \quad (3\text{-}21)$$

3.1.2.1. Sample Design

A 90 degree bit of a theoretical phase shifter with ideal switches that is supposed to operate at 8-11 GHz was designed. For the sake of diversity, PI type network was selected as the low pass filter while TEE type network was selected as the high pass filter (**Figure 3.10**). Element values were found as in **Table 3.1**. The performance of the ideal 90° HP/LP phase shifter can be seen at **Figures 3.11** to **3.15.**

Table 3.1 Element values for the PI type low pass and TEE type high pass filters.

Llow	0.592 nH
Clow	139 fF
Lhigh	1.185 nH
Chigh	809 fF

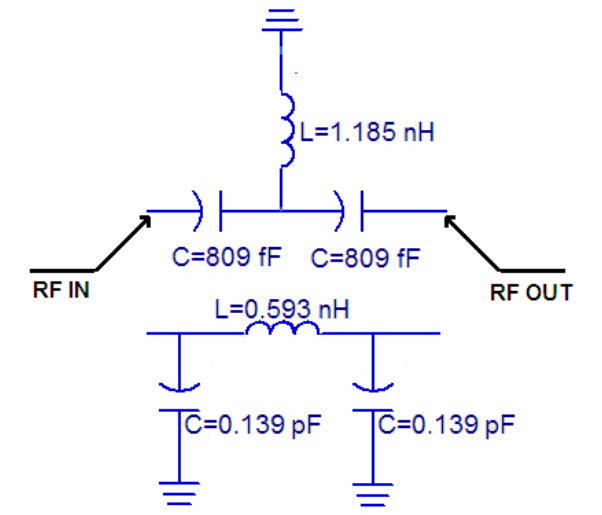

Figure 3.10 Circuit Diagram for the 90º phase shifter with ideal SPDT switches and passive elements.

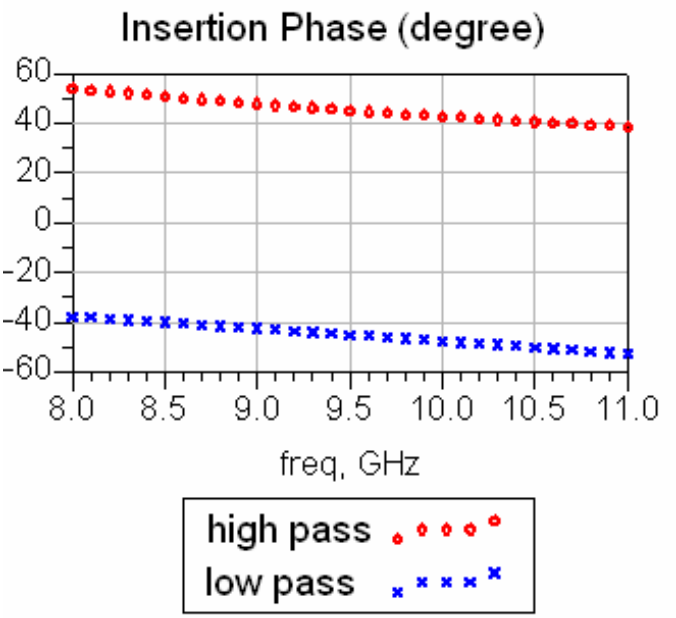

Figure 3.11 Insertion phases of the two filters used in the ideal 90° HP/LP phase shifter

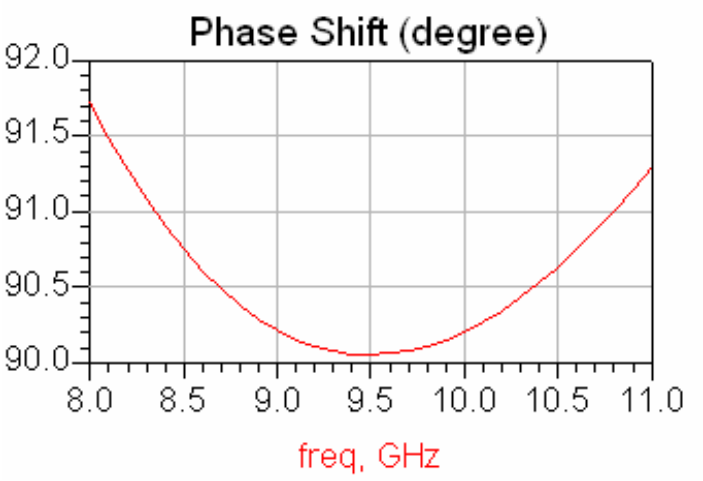

Figure 3.12 Differential phase shift of the ideal 90º HP/LP phase shifter

Figure 3.13 Insertion Losses of the two states of the ideal 90º HP/LPphase shifter

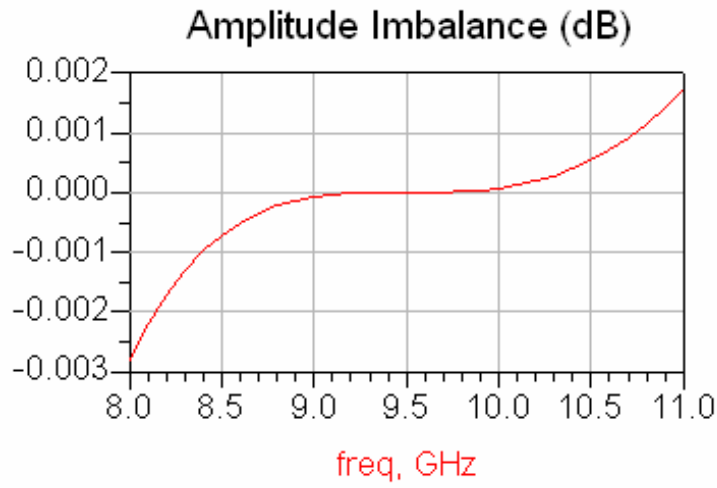

Figure 3.14 Amplitude imbalance between the two states of the ideal 90º HP/LP phase shifter

Figure 3.15 Return losses of the two states of the ideal 90° HP/LP phase shifter

As seen from the graphs, the insertion loss of the phase shifter remains negligibly small between 8 and 11 GHz and the amplitude imbalance is also very low. The flatness of the differential phase shift is thanks to the fact that the phase response of one network is followed by the other with an almost constant offset in the frequency domain. Furthermore, a maximum phase error of 1.8 degree is suffered within the band and this value is the 2% of the total phase shift, which is a fair ratio for this much bandwidth. However the perfect characteristics of this ideal design must not be misleading and it should be noted that the ideality of the elements and the absence of real SPDT switches are the major factors behind the achievement of these almost-perfect responses, such as phase flatness, low insertion loss and low amplitude imbalance.

3.1.3. Loaded Line Phase Shifters

Another common type of phase shifter suitable for digital implementation, loaded line phase shifter, is also widely studied in the literature. In this topology (**Figure 3.16**), a transmission line is loaded with reactive elements at its both ends. In the figure, B_1 and B_2 represent the normalized susceptances and θ stands for the electrical line length of the line. By properly selecting the susceptance B, and the line length, θ, this network can be adjusted to yield a sufficiently flat differential phase

shift within a 20-30% bandwidth. It has been reported that, selecting the line length, θ, equal to π/2 and choosing B_1=-B_2 results in the widest bandwidth [28]. However, due to limitations in the susceptance values dictated by the matching conditions over the bandwidth, this type of phase shifter is useful for phase shifts up to 45º. Moreover, the line length is usually of the order of λ/4, which limits the minimum frequency of operation when the size of the circuit must be kept small.

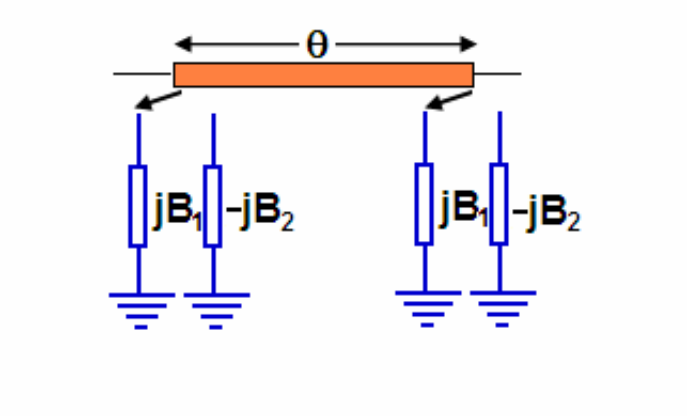

Figure 3.16 Topology of the loaded line phase shifter.

The analysis of this phase shifter bit could be again done by the help of ABCD matrices, but this analysis will not be presented here. With the line length chosen as λ/4 and B_1= –B_2, the differential phase shift, Δφ, is given as:

$$\Delta\phi = 2\tan^{-1}\left(\frac{B}{1-0.5B^2}\right) \qquad (3\text{-}22)$$

3.1.3.1. Sample Design

An ideal loaded line phase shifter with 22.5° phase shift at 9.5 GHz is designed and simulated. The line length is selected as λ/4. As the shunt loads, an inductor of 4.293 nH and a capacitor of 65.4 fF are used. These values are obtained using the given formulae. Following results are obtained:

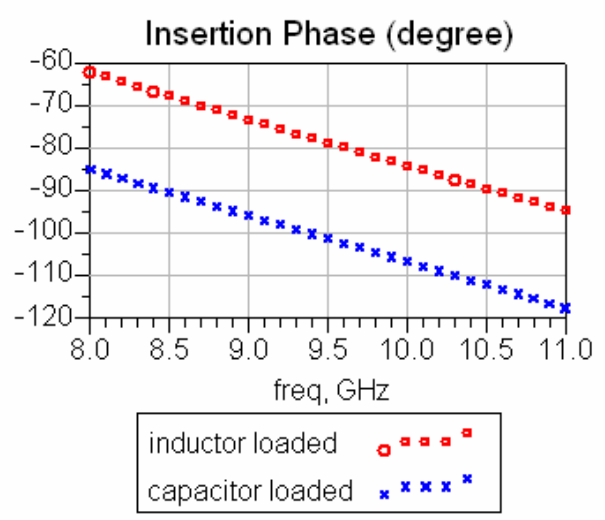

Figure 3.17 Insertion phases at two states of the ideal loaded line phase shifter

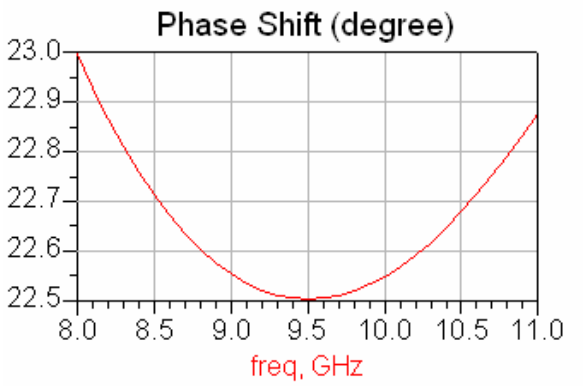

Figure 3.18 Differential Phase Shift of the ideal loaded line phase shifter,

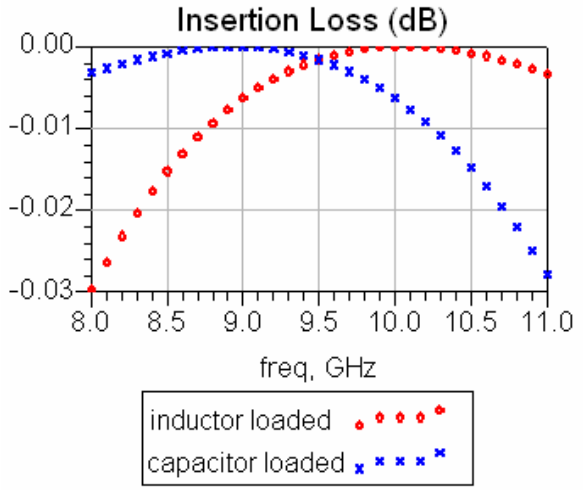

Figure 3.19 Insertion losses in two states of the ideal loaded line phase shifter

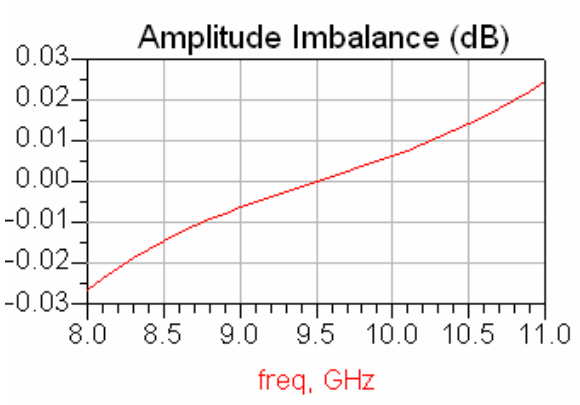

Figure 3.20 Amplitude imbalance between the two states of the ideal loaded line phase shifter

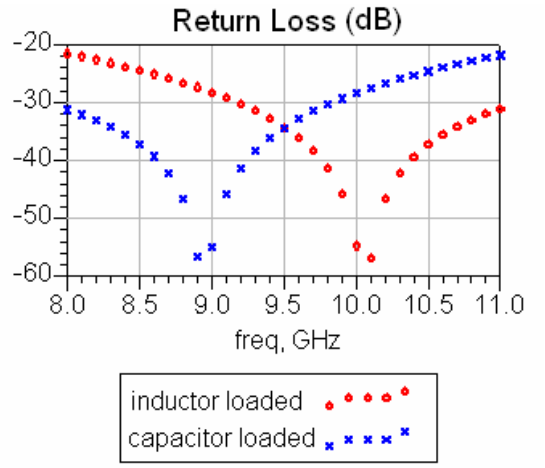

Figure 3.21 Return losses of the two states of the ideal loaded line phase shifter

3.1.4. Reflection Type Phase Shifters

The phase shifter topologies presented up to here were all transmission type, that is, they alter phase of the transmitted signals. Nonetheless, it is also possible to shift the phase of the reflected signal by changing the phase of the mismatched loads. Hybrids are generally used to divert the reflected signal to a separate port. Isolators are not utilized in MMIC due to difficulty in incorporation of ferrite material. As a matter of fact, because of the large area occupied by quarter wavelength lines in the hybrid, reflective topologies are not preferred at low frequencies. The following figure demonstrates the analog and digital phase shifter structures implemented with a 90 degree hybrid.

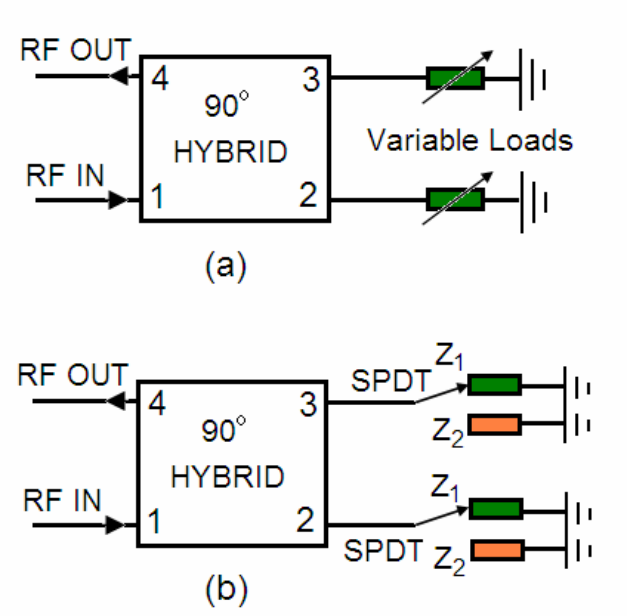

Figure 3.22 Reflection type phase shifter with 90 degree hybrid: (a) analog implementation (b) digital implementation

In either the analog or the digital case, the phase shift is incurred by the change in the identical loads at ports 2 & 3. If the reflection coefficients associated with the loads at two different states are Γ_1 and Γ_2, then the differential phase shift is

$$\Delta\phi = phase(\Gamma_2) - phase(\Gamma_1) \qquad (3\text{-}23)$$

Loads are usually selected reactive for lossless phase shifting. In fact, if the loads are purely resistive, the topology is a good candidate for being an attenuator rather than a phase shifter. In digital case, wideband phase shift performance is achieved if switching is between opposite signed but magnitude-wise equal reactances.

3.1.4.1. Sample Design

A 90 degree hybrid with 9.5 GHz center frequency is first designed with ideal quarter wavelength transmission lines. Ideal SPDTs assumed to exist at the ports 2 & 3 of the hybrid. Then necessary load values for a 180 degree reflective phase shifter are determined as in **Table 3.2**.

Table 3.2 Element values required for 180 degree reflective phase shifter

Z1 @ 9.5 GHz	Z2 @ 9.5 GHz
-j50 Ω (335 fF)	j50 Ω (0.837 nH)

Following results are obtained:

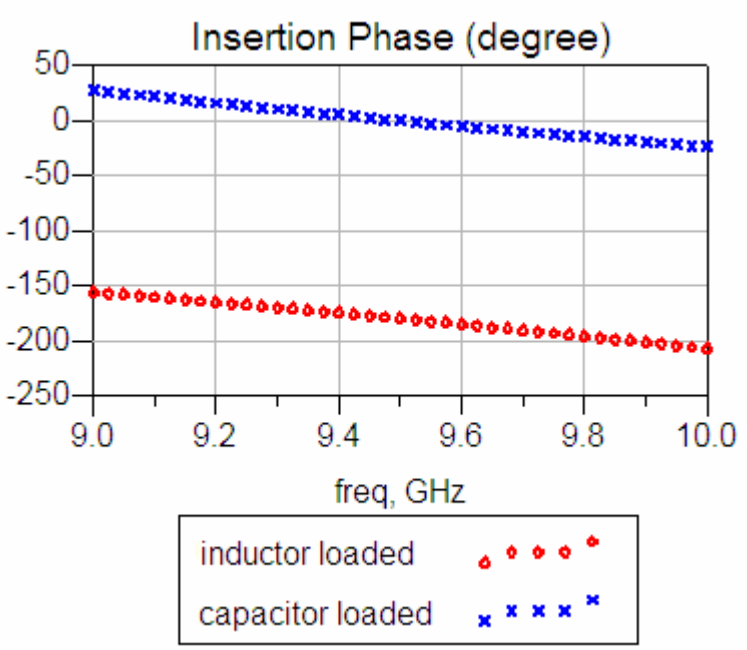

Figure 3.23 Insertion phases in the two states of the ideal reflective phase shifter

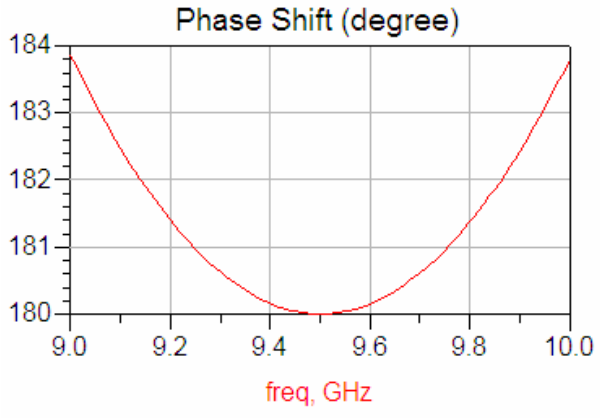

Figure 3.24 Differential phase shift of the ideal reflection type 180° phase shifter

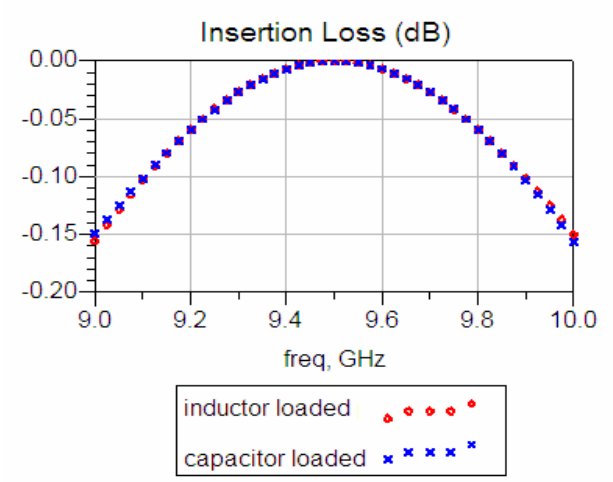

Figure 3.25 Insertion losses in two states of the ideal reflection type 180° phase shifter

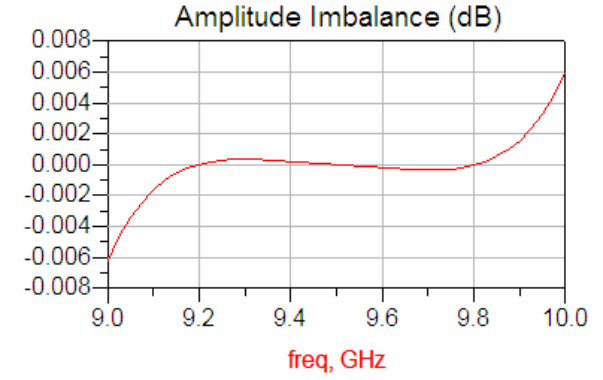

Figure 3.26 Amplitude imbalance between the two states of the ideal reflection type 180º phase shifter

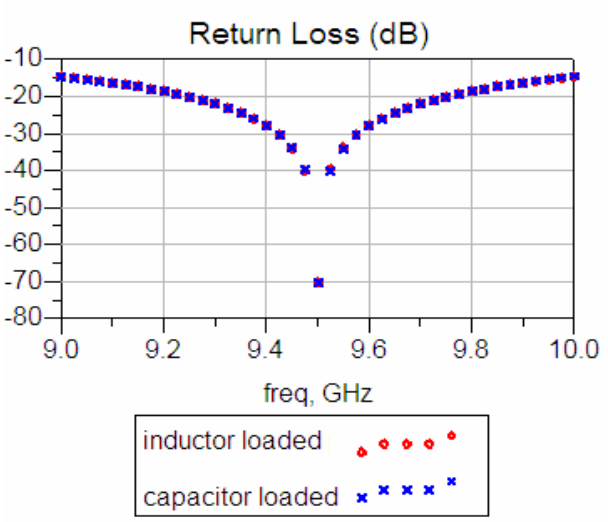

Figure 3.27 Return losses of in two states of the ideal reflection type 180° phase shifter

3.2. The role of GaAs FETs in MMIC phase shifters

All digital MMIC phase shifters require a circuit component that offers different characteristics according to the applied bias voltage or current. Early MMICs use PIN diodes for that purpose. The PIN diode can be used as a switch considering that it exhibits a low impedance at forward bias and a high impedance at reverse bias. The following figure displays the usage of a PIN diode as a single pole single throw (SPST) switch.

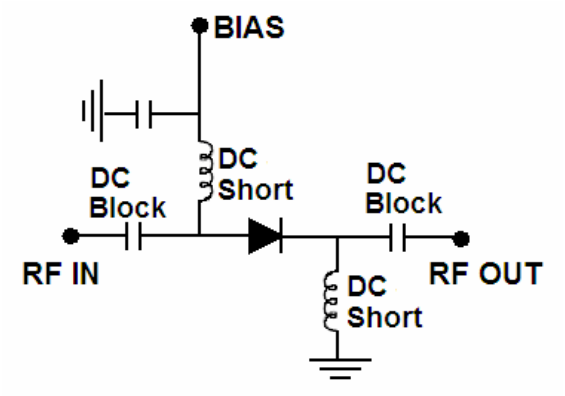

Figure 3.28 PIN diode in SPST configuration

Modern MMIC switches and phase shifters generally use GaAs FETs as switching elements due to advantages over PIN diodes. These advantages are simplified bias

and driver networks, smaller DC power requirements and faster switching speeds of FETs [34].

In MMIC phase shifters, FETs are either used as the main building blocks of SPDTs that are employed for switching between two different networks, or they are used as variable circuit elements that shift the insertion phase of the circuit.

Many different analytical and equivalent circuit FET models exist in literature [35]. They are all good models with regard to particular operation conditions. Some models explain and fit small signal operation very well while some models are optimum for noise behavior. A generally accepted model for switch operation is a small series resistance in ON mode and a capacitor representing the OFF mode.

3.2.1. GaAs FET Switching Mechanism

While using the FET as a switch mode, it is in fact in the linear mode of operation. **Figure 3.29** demonstrates $I_d - V_{ds}$ behavior of FET with respect to gate bias voltage. It is seen that, below some value of the gate bias, no drain current flows through the device, no matter how high the drain-to-source voltage is. This is due to the pinch-off phenomenon of FET. When the gate – to – source voltage is larger in magnitude than the pinch-off voltage of the device, the channel is completely depleted of from free charge carriers and therefore the drain source resistance is very high. This corresponds to the OFF state of the FET. However the FET is not only a high resistance in the OFF state. Under these conditions, the FET can be approximated by series and parallel combinations of resistors and capacitors as shown in **Figure 3.30**. If the gate termination represents a sufficiently large RF impedance at the frequency of operation, the OFF-state equivalent circuit can be expressed as a parallel combination of a capacitor and a resistor. Referring to **Figure 3.30**, when $1/\omega C_g >> r_g$, the effective drain-to source capacitance is simply $(C_{sd} + C_g/2)$ and the effective drain resistance is the parallel combination of r_d and $2/(\omega^2 C_g^2 r_g)$ [34].

On the other hand, under the zero gate bias condition the channel region is virtually open, except for the zero field depletion layer thickness. Thus, for current levels less than the saturated channel current, I_{dss}, the FET can be modeled as a linear resistor

[34], which is apparent from the characteristic given in **Figure 3.29**. The slope of the I_d vs. V_{ds} curve is steepest when V_{gs}=0. The FET is usually operated at V_{ds}=0, where negligible current flows from drain to source.

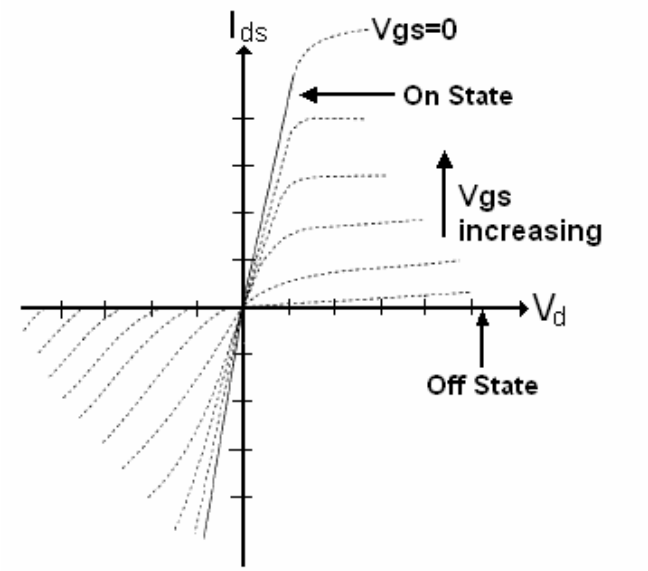

Figure 3.29 Linear operating regions of a FET Switch[34]

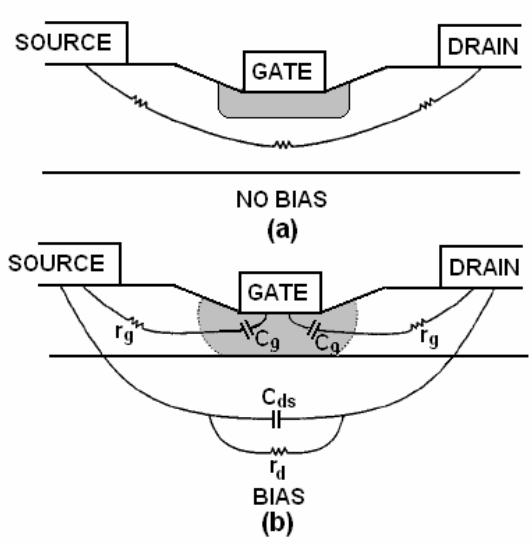

Figure 3.30 Cross section of FET switch with resistive and capacitive regions: (a) ON state (b) OFF state [34]

3.2.2. Comparison of MESFET and HEMT

The basics of FET operation will not be repeated here, because there are plenty of sources on this fairly old topic. These principles apply to HEMTs as well. For details, the reader can refer to [33].

The operations of MESFET and HEMT are indeed very similar, keeping in mind that they are both field effect devices. The difference is that HEMT utilizes a vertical architecture, which incorporates layers of different materials that are chosen to form a device channel in which the electrons are physically separated from their donors. This leads to large electron mobility, as ionized impurity scattering is reduced [34].Thus comes the name "high electron mobility transistor" for HEMT. **Figure 3.31** and **Figure 3.32** demonstrate the cross sections of these devices. Although there are definite differences in physical structure, the current voltage characteristics of MESFET and HEMT are very similar.

As a fundamental difference, in MESFETs, the current flows from drain to source via a **conducting** channel, while in HEMTs the current flow is within a **high mobility** channel [34].

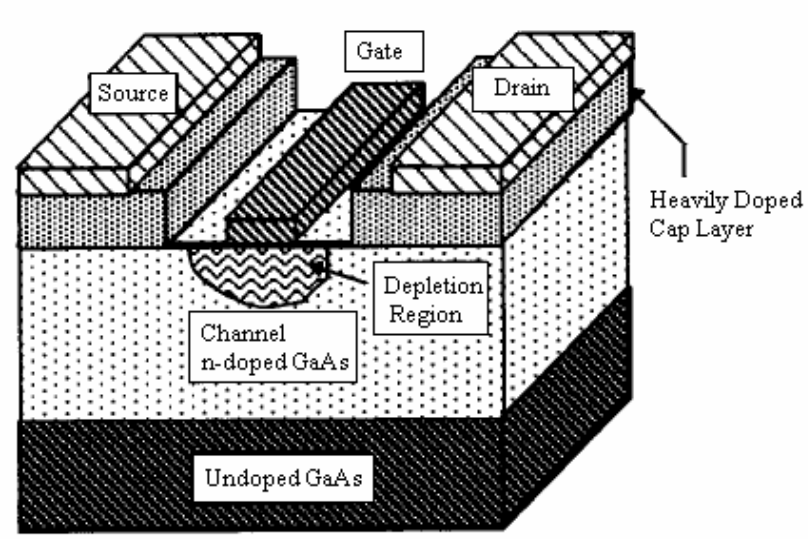

Figure 3.31 Cross section of MESFET [34]

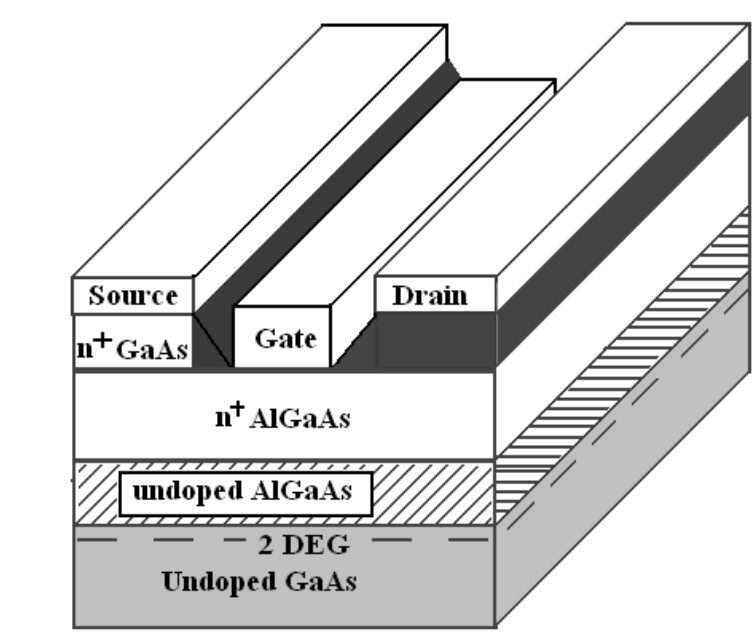

Figure 3.32 Cross section of AlGaAs/GaAs HEMT [34]

3.3. Working in Cooperation with A MMIC Foundry

A MMIC foundry is an institution that owns the necessary facilities to manufacture MMIC chips. Some foundries are attached to an electronics corporation and makes production in accordance with the requirements of that corporation. Some foundries, on the other hand, allow customers, which are most of the time some other company, to get their designs implemented. A large financial, scientific and engineering background is essential for the emergence and maintenance of a foundry. That is the reason why most MMIC foundries are founded and funded by strong microwave companies. Some MMIC foundries produce Silicon based ICs as well as GaAs. Below are the major worldwide foundries by the year 2005 [34].

Table 3.3 List of worldwide MMIC foundries by 2005

GaAs		Silicon
Agilent	Motorola	Agilent
Alcatel-Telettra	NDI	Analog Devices
Alenia	NEC	Atmel
Alpha Industries	Northrop Grumman	Conexant
Anadigics	OKI	Harris
Celeritek	OMMIC	IBM
Conexant	Raytheon	Infineon
EiC Corp.	RF Micro Devices	Maxim
Filtronic	Samsung	Motorola
Fujitsu	Sanders	National Semiconductor
GaAsTEK	Sharp	NEC
Hexawave	Sony	Philips
Hitachi	Stanford Microdevices	Qualcomm
Honeywell	Toshiba	RF Micro Devices
Infineon	Triquint	SGS-Thompson
M/A-COM	Velocium (TRW)	Texas Instruments
Marconi Caswell	UMS	
Matsuhita	Eoncom	
Mitsubishi	WIN	

In general, the foundries provide their design kits and manuals belonging to a specific process and the customer makes the design in the light of the information included in the design kits, using a simulator program supported by the design kit. The distinguishing part of a process is sometimes the gate length of the FETs in the process, for it is the principal factor determining the maximum frequency of the IC's to be produced with that process. Furthermore, a process for example might be dedicated to low noise amplifier design or it could be optimized for switching applications.

The content of the design kit varies from foundry to foundry and it determines the designer's part in the design phase. For instance, a designer might have to create a

component in the simulator as a combination of ideal elements with the help of the design manual. On the other hand, the design kit might be friendly enough to allow the designer to drag and drop foundry's elements from some menu and change the values instantly. The ease of design is directly related to the design kit coverage. A "good" design kit should contain as much information/data as possible so as to end up the designer with a reliable design layout. Generally, design kits include the models of active and passive elements that the foundry is capable of producing on the chip. These models could be parametric, or could pertain to a discrete set of element values. Furthermore, layout rules namely, dos and don'ts of the layout generation are necessary for the designer to accomplish the layout phase. The reliability and the comprehensiveness of the design kit is quite a determining factor on the so called "first time success", as well as the capability of the designer.

Obtaining the layout, customer submits the layout to the foundry. The foundry might investigate the design for possible errors, for instance layout rule violations. The customer then could be asked for a modification that would lead to a valid design. When everything is seen all right, the foundry is ready to produce the chips as many as the customer desires, within the minimum and maximum numbers that the foundry allows. Some foundries allow small numbers of chips to be produced by arranging periodic runs in which a wafer is shared among different customers. This is called a "multi chip project" and is suitable for prototyping studies. Multi chip projects save the customers from the risks of having a thousand useless circuits and paying a significant amount of money in vain. If the prototyping is successful, the customer may go for a dedicated production. If it is not, the customer tries to find the reason(s) behind failure and continues prototyping.

The nature of MMIC does not allow post production tuning. Indeed if the chip is not working close to expectations, it might be very hard to localize the source of the problem. Therefore, a precise and high-yield design is necessary, but not sufficient to avoid wasted products. It is also partly the foundry's responsibility to guarantee the asserted precision in modeling and production.

3.3.1. Models

A foundry ought to provide the models of the active and passive devices it is capable to manufacture. These models are usually valid in some limited domain of element parameters. The source of the information behind models is the extensive modeling studies executed by the foundry itself. The models should be in compliance with the measurement results which may or may not be provided by the foundry. A model can not represent the real device for all frequencies, dimensions and perhaps bias points. Instead the foundry indicates the restrictions on these parameters to the designer's interest. However the foundry is bound to guarantee the compliance of the behavior of components on the produced chip with the models provided.

3.3.2. Measurements

A foundry may release some measurement results associated with the active or passive elements to its customers. For the active elements, these might be S parameter data sets, load pull measurement results, noise parameters and some i-v curves. For the passive elements, S parameters corresponding to a discrete set of element values could be provided. In both cases, the advantage is the better prediction of device behavior as compared to models. The undesired thing with the measurement data is that the element values are discrete, be they passive or active. This sounds similar to hybrid circuit issues and is a challenge to the designer especially when the desired value is not close enough to the available values.

To obtain and supply the measurement data, the foundry generates prototypes of several different elements and makes a lot of on wafer measurements. The models are indeed extracted from these measurements. The measurement domain is not only the frequency but various bias points for active devices. It is the responsibility of the foundry to apply the appropriate de-embedding procedure to get the real data of the device.

3.3.3. Limitations

As indicated before, a process can not support arbitrarily high frequency, as the gate length of the transistors determines the maximum allowable operation frequency. Circuits operating well over 100 GHz with HEMTs of 0.1 μm gate length have been reported [34]. Even if no transistors are used in the design, passive elements are not parasitic free although the nature of MMIC offers very fine parasitic performance. For that reason, after some frequency, lumped implementations are quitted and distributed designs with either microstrip or CPW are preferred. Moreover, greater the element values, larger the area they occupy. As a matter of fact, a process might offer different implementations for different element ranges. For instance, below some picofarads, a capacitor is realized with interdigital lines, while MIM (Metal – Insulator – Metal) technology is essential for size considerations beyond that value. Another limitation on component values arises from modeling difficulties. A component of some extreme value might have too much parasitics to be modeled. Equally bad is that a component of an extreme value might be manufactured on the wafer but it might be impractical to measure and therefore model it.

3.3.4. Layout Concepts

A design is not mature and production ready unless it has a proper layout. The layout represents the real circuit to be produced and it is the principal bridge between the designer and the foundry. The foundry's part is mainly to inform the designer of the layout rules of the process. Second, it is very nice for the designer to have a good layout kit for the process by which he/she can carry out the layout phase easily. In the early schematic phase anything can be placed anywhere. In the layout however, finite sizes, the geometry of components and layout regulations of the foundry make things difficult. For instance a capacitor has two terminals, but its behavior could change if the terminals are selected to be some other points recommended by the design kit. Next, if for the sake of making two edges meet, the width or length of the capacitor is varied with keeping its value the same, the insertion loss or insertion phase could change significantly especially if the frequency is high. If such things are the case, one should go back to schematic and make necessary changes to have a

reasonable layout. Hence, successive iterations between schematic and layout are usually carried out in order to obtain a consistent layout.

CHAPTER 4

STUDIES WITH WIN FOUNDRY

4.1. Switch Process of WIN Foundry

At the early phases of this study, the MMIC chip was to be produced by WIN Foundry of Taiwan, who offers quite low prices per chip area. The design was initiated and it was abandoned due to some layout difficulties that will be explained later. However some designs for 180 and 90 degree bits were made in the schematic level and they are worth presenting here.

Before going into the details of designs, the process offered and material provided by WIN foundry will be mentioned. ASELSAN was already in contact with WIN foundry for a low noise process of WIN foundry at the time this study began. For the implementation of the phase shifter however, a different process was offered to ASELSAN by the WIN foundry: 0.5 μm gate length InGaAs pHEMT Switch Process. This process was claimed to be suitable for an X band phase shifter due to sufficient f_{max}, which is as high as 20 GHz. As well as planar inductors, mesa resistors and MIM capacitors, the process covers a family of transistors of several different gate width and number of gate fingers. For the resistors and capacitors, models are given, and for the inductors, S parameter measurements are provided.

Although the f_{max} of the process is 20 GHz, this process was dedicated to lower frequencies, such as GSM bands. Therefore the models of pHEMTs are consistent with the on and off state S parameter measurements below 6 GHz and WIN foundry does not guarantee the models above this frequency. Also, the on and off state S parameters were not provided as a part of the design kit. At some later time in the

schedule, WIN foundry released the S parameters of below transistors at on and off states obtained from on-wafer measurements:

- 4x80 μm (Triple Gate)
- 4x125 μm (Single Gate, Dual Gate, Triple Gate)
- 8x125 μm (Single Gate, Dual Gate, Triple Gate)
- 16x125 μm (Single Gate, Dual Gate, Triple Gate)
- 20x125 μm (Single Gate, Dual Gate, Triple Gate)

The S parameter data was available with 200 MHz steps. Within the band of interest, data at following frequency points were given: 9.1, 9.3, 9.5, 9.7, 9.9 GHz. In fact, the entire data were between 0.1 and 10.1 GHz with 200 MHz steps. Although it was a sparse set, it was used. In the measurement setup (reported by WIN Foundry), gates of transistors were grounded. In the simulations, however, the gate was pulled down to the ground via a large resistor, which is essential when the transistor is to be used as a switching device. If the gate was perfectly grounded, there would be no problem with this, but the finite inductance between the gate and the true ground was a predicament regarding the reliability of the simulation.

4.2. Design of a 90 Degree Bit

4.2.1. Design of an SPDT with WIN Components

Apparently, this set of transistors is quite a limited set and the transistors are relatively large. The transistor sizes are not well optimizable parameters because of absence of parametric models and limited domain. Phase shifter topologies incorporating transistor off state capacitances were not easy to design with this transistor set, because the success of these topologies is highly dependent on the optimization of the transistor parameters. With the given conditions, classical switched filter designs were considered and realized. First, a proper SPDT was designed with available transistors. Optimization of transistors was necessary anyway, but this was manually carried out with a trial error approach.

The SPDT structure in **Figure 4.1** was ended up:

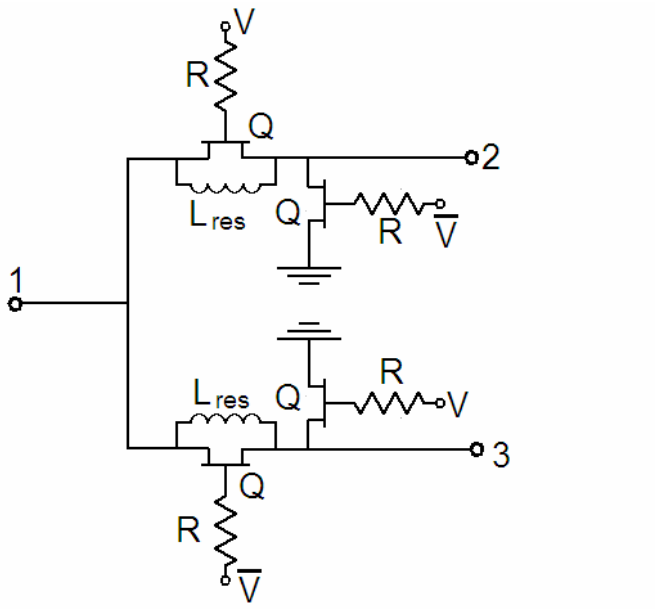

Figure 4.1 Schematic of the SPDT switch designed with WIN foundry's 0.5 um switch pHEMT process

The resistors connected to the gates of transistors are used to increase the isolation of the gate from RF and they are usually kept high. In the SPDT above, their size is 4 µm x 100 µm and they are about 5 kΩ. The 4 transistors are identical and they are 4x125µm. The resonating inductor is 2.195nH and it enhances the isolation by 13 dB while degrading the insertion loss 0.12 dB. All elements are simulated in the light of measured data, except that, for the resistors model is used. With the given configuration, following results are obtained:

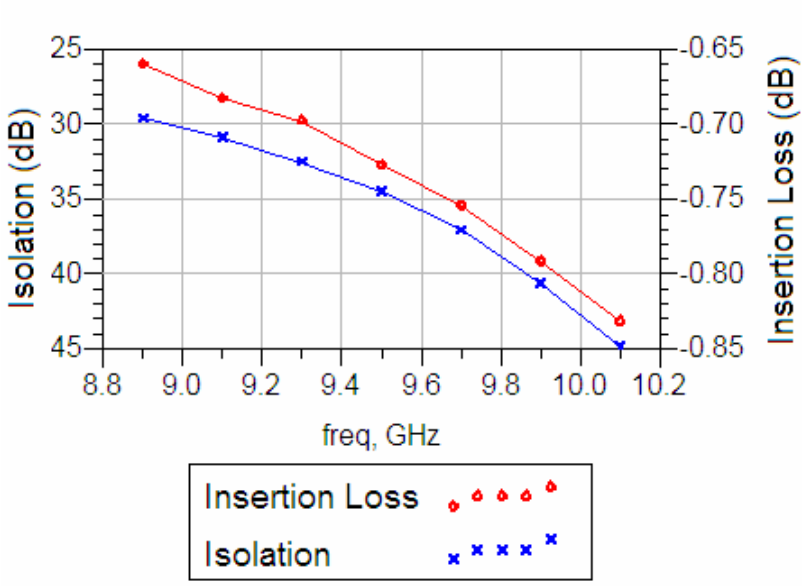

Figure 4.2 Isolation and the insertion loss of the SPDT designed with WIN components

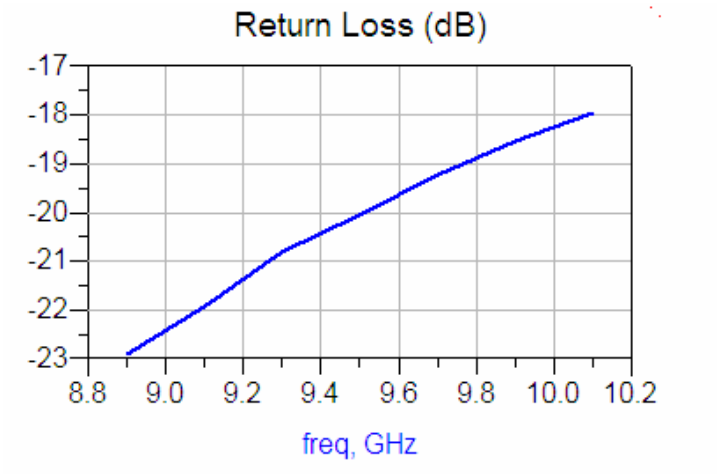

Figure 4.3 Input return loss of the SPDT designed with WIN components

4.2.2. Combining the SPDTs with filters

A 90 degree bit was then designed first using ideal elements and this SPDT. Next, ideal capacitors were replaced with the foundry models and the ideal inductors are replaced with S- parameter data. Due to some difficulties in layout preparation using the design kit, the design did not proceed to the layout phase. Following figure shows the schematic of the designed 90° bit. The same configuration was used for the 180 degree as well.

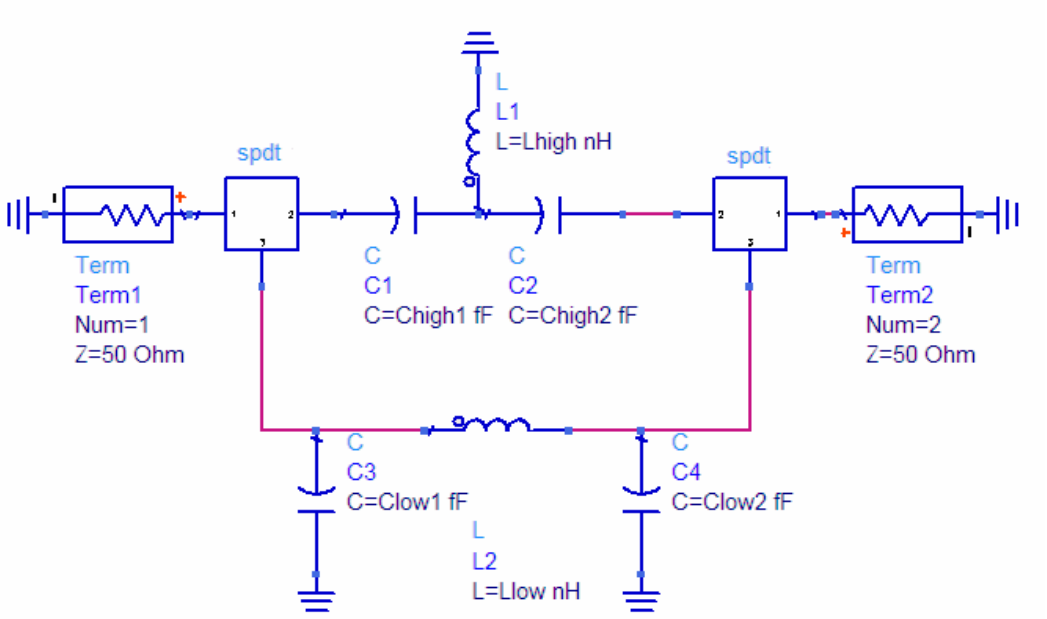

Figure 4.4 SPDT switch designed with design kit of WIN Foundry's 0.5 um switch pHEMT process

For both high pass and low pass filters, one-inductor configurations are preferred because usage of inductor is a design difficulty. That explains the TEE type low pass and PI type high pass section in the bit. In the schematic, filter elements are seen as variables. The values are given in the following table:

Table 4.1 Ideal component values in the 90 degree phase bit

Llow	0.630 nH
Lhigh	0.786 nH
Clow1	167 fF
Clow2	145 fF
Chigh1	1.836 pF
Chigh2	3.247 pF

The capacitors are possible to be produced at arbitrary values but the inductors must be equal to one of the available values. With the ideal components whose values are given in **Table 4.1**, the performance in the **Figure 4.6** is obtained. For the legend details of the following performance plots, **Figure 4.5** can be referred. It applies throughout this chapter.

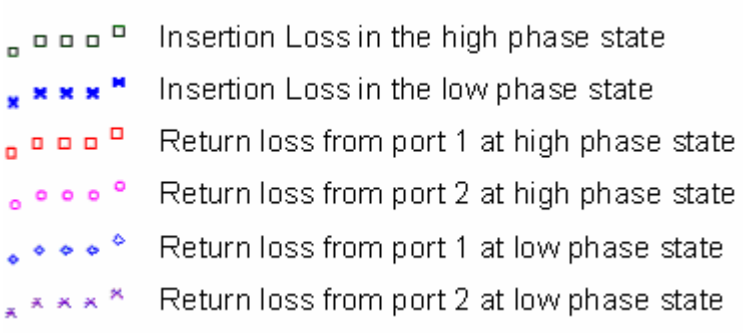

Figure 4.5 The legend to be referred for the bit-performance graphs

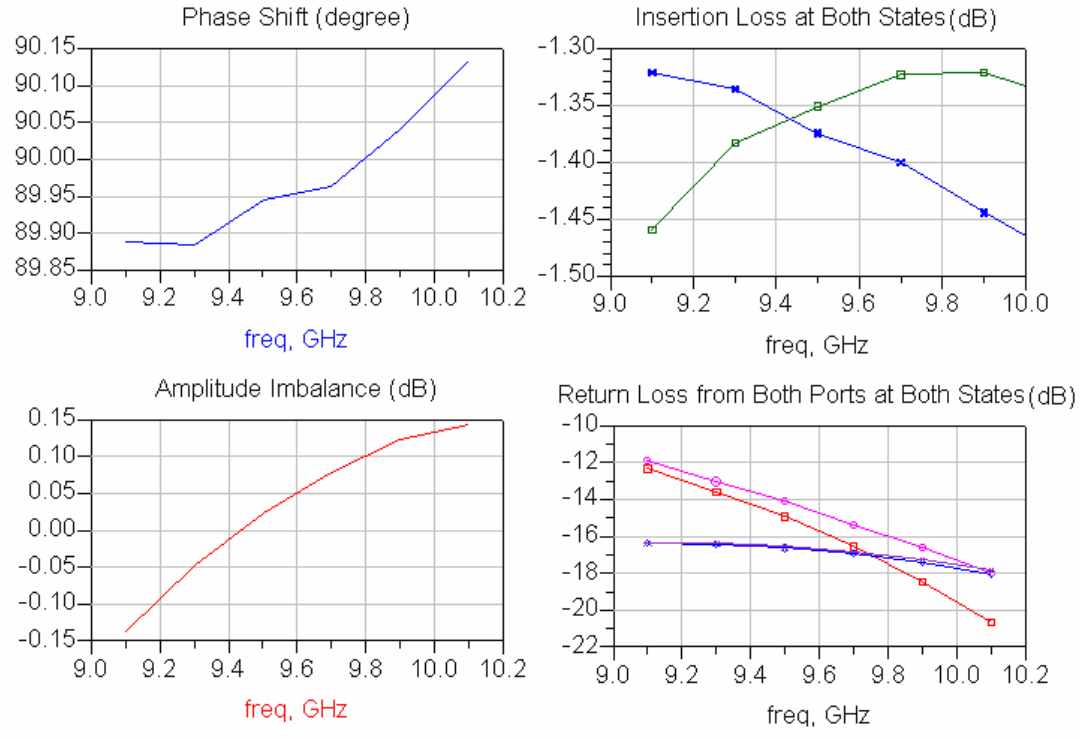

Figure 4.6 Overall performance of the 90 degree bit designed with ideal filter elements but practical SPDT.

The return loss was not an optimization target and it is therefore not good enough. This is indeed critical when all phase shifter bits are to be cascaded. With this much return loss, the phase shift of the overall phase shifter will be somehow different than the sum of individual phase shifts of the bits. However, if the return loss being below -15 dB is also an optimization goal, none of the goals are accomplished close enough.

In the next phase where the inductors are replaced with S - parameter data, most close elements were first selected from the given set. Having the ideal elements as initial values for the practical elements, the effort for making the design with the provided models and measurements initiated.

The values are updated as in the **Table 4.2** after a second optimization is executed.

Table 4.2 Component values of the 90 degree phase shifter bit upon replacement of ideal elements with S parameters or models and re-optimization

Llow	0.787 nH
Lhigh	0.973 nH
Clow1	125 fF (17.3 um x 19.7 um)
Clow2	137.5 fF (11.3 um x 32.3 um)
Chigh1	1.53 pF (85 um x 55 um)
Chigh2	1.62 pF (101.4 um x 50.6 um)

In fact, the inductance values of inductors are not supplied by the foundry. Instead, the foundry gives the number of turns and amount of gap between the turns of the inductor attached to the name of the associated s parameter file. The values in the table are only approximate and are extracted for information purposes. As observed, the inductance values are seriously different than the ideal component values. This is due to the unavailability of the closer values. Again the capacitors are not defined with their capacitance, but they are described with their sizes. The last capacitor in the table seems large but it should be kept in mind that the transistors are no smaller than that.

Below seen is the performance of the phase shifter with ideal capacitors replaced with models and ideal inductors replaced with measurement data.

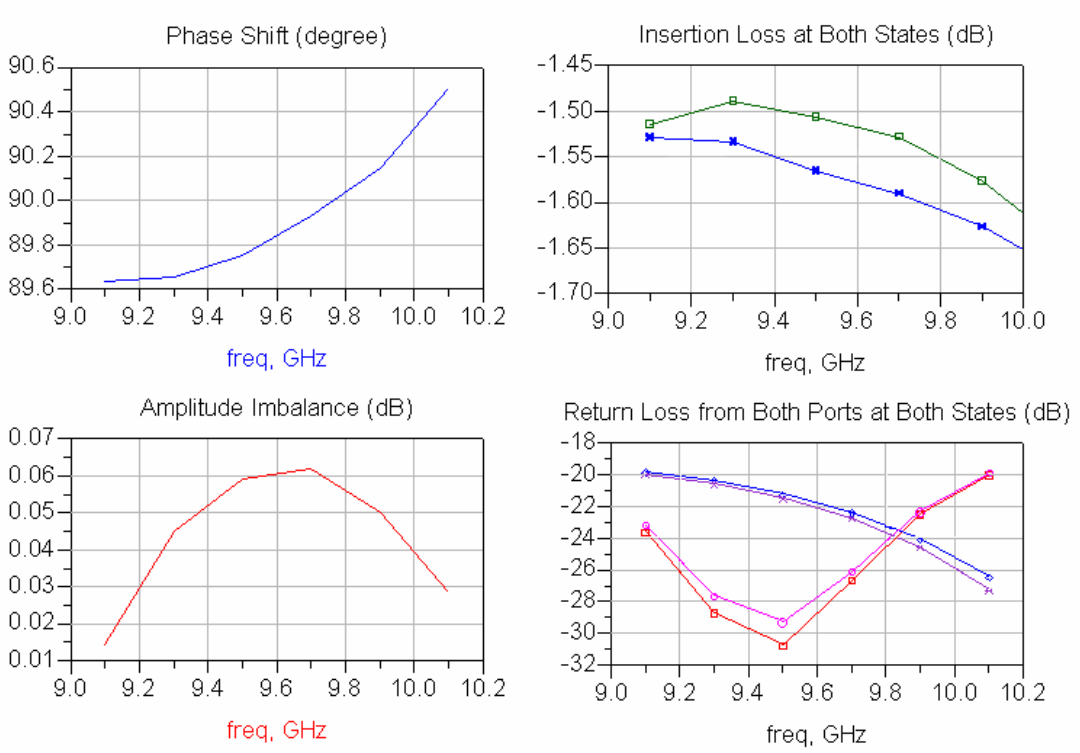

Figure 4.7 Performance of the 90 degree bit upon replacement of ideal components with more realistic ones: Capacitors with models and inductors with measurements.

Apart from the phase variation, the performance of the design with non-ideal components seems not to fall behind that with the ideal components. Return loss is almost below -20 dB for both states and amplitude imbalance is close to zero. It seems that parasitics are not always malignant.

4.3. Design of the 180 Degree Bit

Same SPDT and same filter configurations are used in the design of 180 degree bit. Again, ideal inductors and capacitors are used in the beginning. **Figure 4.8** demonstrates the performance of the designed 180 degree bit:

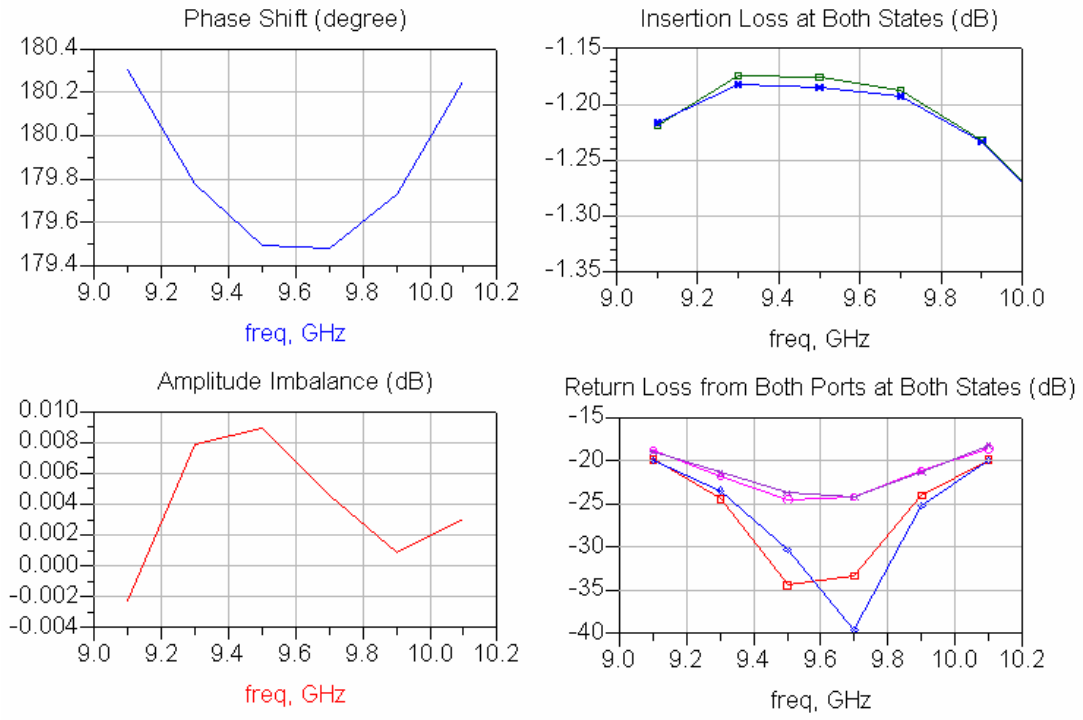

Figure 4.8 Overall performance of the 180 degree bit designed with ideal filter elements but practical SPDT

The ideal component values are given in **Table 4.3**. (For the variable names, refer to **Figure 4.4**.)

Table 4.3 Ideal component values in the 180 degree phase bit

Llow	0.818 nH
Lhigh	0.827 nH
Clow1	323 fF
Clow2	347 fF
Chigh1	323 fF
Chigh2	345 fF

Next, the capacitors were replaced with capacitor models of the foundry and the inductors were replaced with the measurement data.

Table 4.4 Component values of the 180 degree phase shifter bit upon replacement and re-optimization

Llow	0.81 nH
Lhigh	0.81 nH
Clow1	346 fF (33 um x 31.2 um)
Clow2	347 fF (94 um x 10.1 um)
Chigh1	337 fF (91 um x 10.1 um)
Chigh2	351 fF (42.8 um x 24.5 um)

The overall performance of the 180 degree bit is given in **Figure 4.9**.

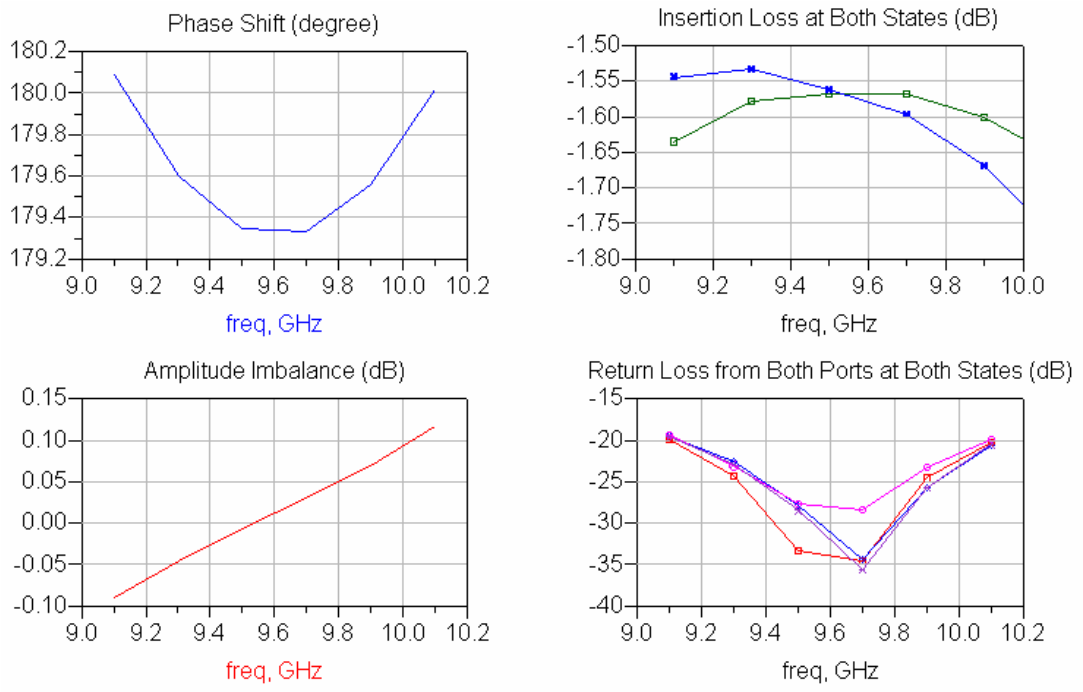

Figure 4.9 Performance of the 180 degree bit upon replacement of ideal components with more realistic ones: Capacitors with models and inductors with measurements.

4.4. Layout Phase

In the layout phase need for an intensive mailing with foundry aroused, because the process had no back via option. The foundry authorities advised to circulate a ground plane around the circuit and use shunt elements by connecting them to that ground plane. Also, the single gate transistors had two gate access points and two independent meanders connected to these access points as seen in **Figure 4.10**. Again, when the advice of the foundry authorities was asked for, it was recommended to connect these two points with transmission lines. Due to difficulties in modeling of these situations, the design was terminated at this point.

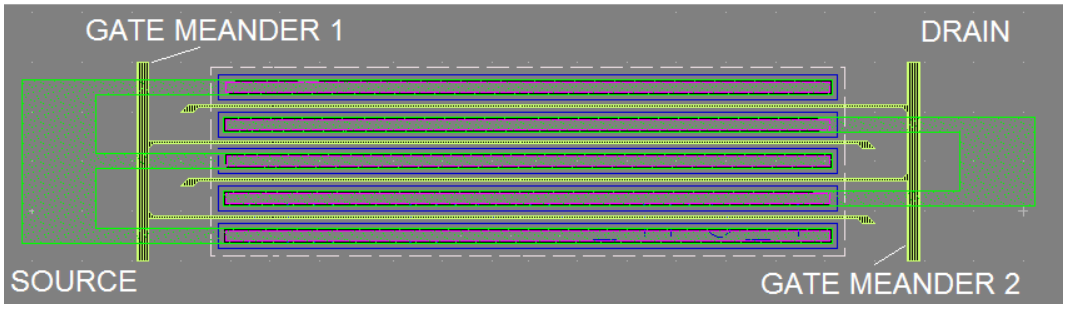

Figure 4.10 Layout of a 4x125µm Single Gate Transistor in the 0.5 um InGaAs Switch pHEMT process of WIN Foundry.

CHAPTER 5

STUDIES WITH OMMIC FOUNDRY DESIGN KIT

Not able to complete the design with WIN foundry, the study went on with the design kit for the ED02AH process of the OMMIC foundry. The name of the process implies the availability of both enhancement and depletion type 0.2 μm gate width pHEMT transistors. Since the gate width of the transistors is 0.2 μm, the f_{max} of the process is reported to be as high as 60 GHz. This much f_{max} is definitely sufficient for an X band phase shifter. The transistor gate fingers can be 2, 4, 6, or 8, while the gate width can be between 15 μm and 50μm. In fact, one can pick lower values of gate widths than 15 μm and greater values of gate widths than 50 μm, but the foundry does not guarantee the validity of the models outside this range.

The OMMIC foundry design kit, upon installation, allows the user to pick devices from its own component palette just like any other component palette in the ADS®. Furthermore, the user can easily edit component properties just like the standard components in ADS. The components are parametrically modeled such that they behave according to the model depending on the entered parameter values. This property of the design kit, coupled with a large domain of available element values in the process grants great design flexibility. There is no quantization of passive element values and transistor gate width in the process. Moreover, there is one to one correspondence between a schematic item and a layout item, which not only allows easy and instant generation of layout from schematic but quick transition to schematic from layout as well. The user can also start the design from the layout to see the real dimensions and geometry. For instance, if the value of a capacitor is varied, the sizes are automatically updated. On the other hand, if the width of a capacitor is altered, the capacitance value is automatically updated. In brief, having these user-friendly features no brute force is spent during the design with OMMIC design kit.

5.1. Usage of OMMIC FET as a Switch

To use the FET as a switch, be it a MESFET or a pHEMT, it is operated in passive configuration, that is, the drain – to – source voltage must be 0. The signal is either injected from the drain and gathered from the source or injected from the source and gathered from the drain, as the device is reciprocal in this configuration. The switching is done by means of altering the gate voltage between two values: 0 V and some value below pinch-off voltage of the pHEMT. However, care must be taken with the application of gate bias. The RF signal is not desired to appear at the DC control of the gate; therefore either a low pass filter or a high choking resistance is used to isolate the DC source from RF signals. Due to its simplicity, resistor is usually preferred for this purpose. With the gate pulled down to the supply via a high resistance, the pHEMT can be approximately modeled as a small resistor in the ON state and a small capacitor at the OFF state. The quality of the pHEMT as a switch could be measured by the product of the ON state resistance and the OFF state capacitance. For an ideal switch this product is equal to zero. To have good switching action, the ON state resistance and the OFF state capacitance must be as low as possible to have small insertion loss in the ON state and to have large isolation in the OFF state. The setup in **Figure 5.1** is used to simulate the isolation of the gate bias circuitry from drain and source terminals. The combination of **DC feed** and **DC block** acts as a bias tee and they are inserted for measurement purposes. To make the transistor OFF, gate voltage is pulled to -2 Volts which is well below the pinch-off voltage of the OMMIC transistor (-1.1 Volts).

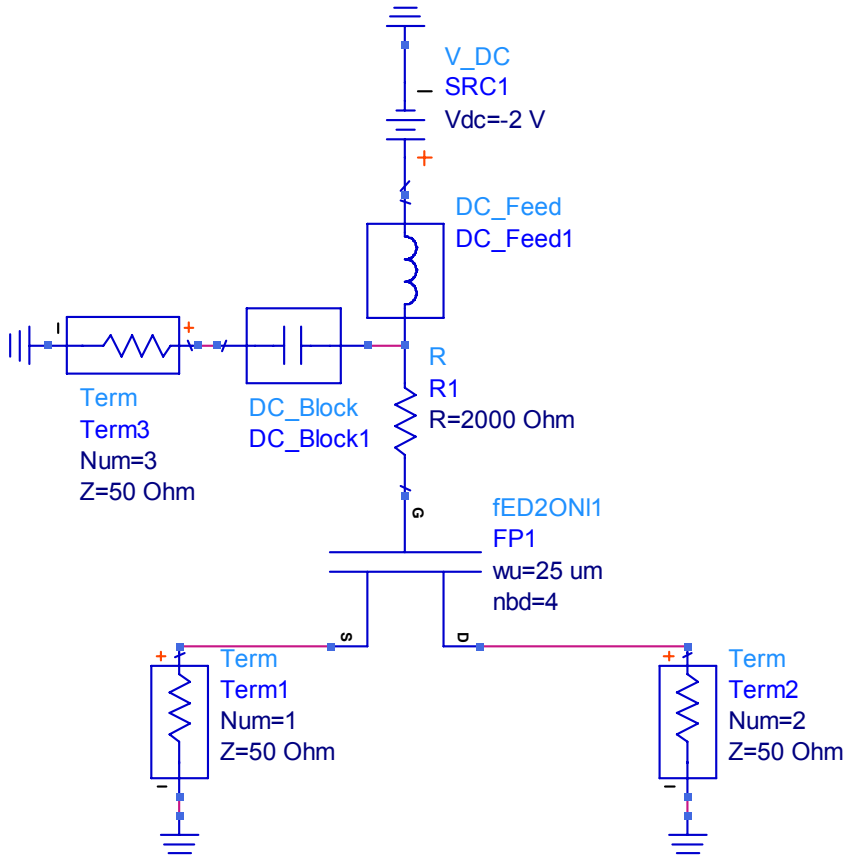

Figure 5.1 Setup for measuring isolation between gate and the drain terminals

In the simulation, the gate width is swept between 15 µm and 50 µm with 5 µm steps and the number of gate fingers is swept between 2 and 8 with steps of 2. The sweep is executed in nested manner, that is, all combinations are simulated. The following isolation values are obtained for gate resistances of 3000, 2000 and 1000 Ωs. The results are always below -32 dB for the gate resistor value 2kΩ. Increasing the value of this resistor further could make the gate – drain isolation down to 40-45 dB, but the resistor size becomes hard to lay-out. Smaller values of resistor, of course, result in worse isolation and isolation drops rapidly for resistor values less than 1000 Ω.

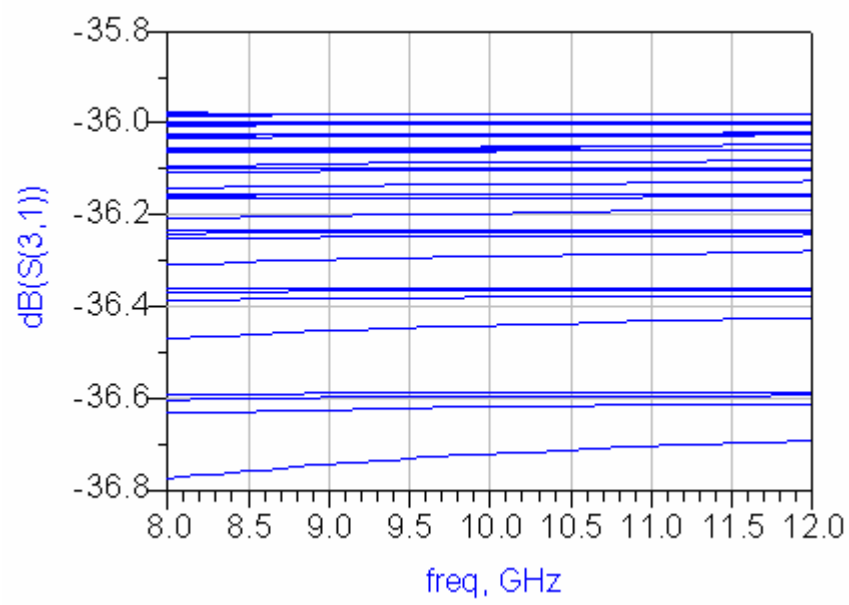

Figure 5.2 Result of swept simulation with Rg = 3000 Ω (Isolation between gate and drain)

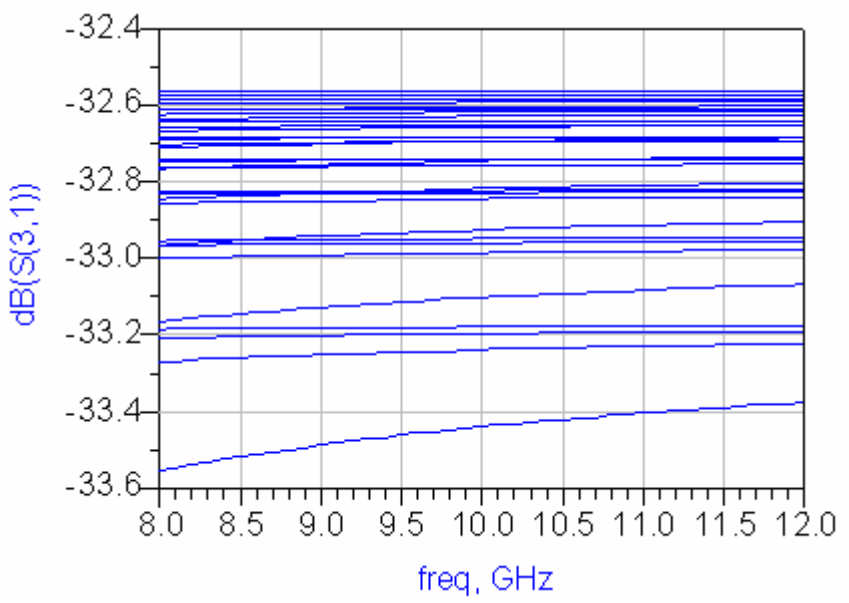

Figure 5.3 Result of swept simulation with Rg=2000Ω (Isolation between gate and drain)

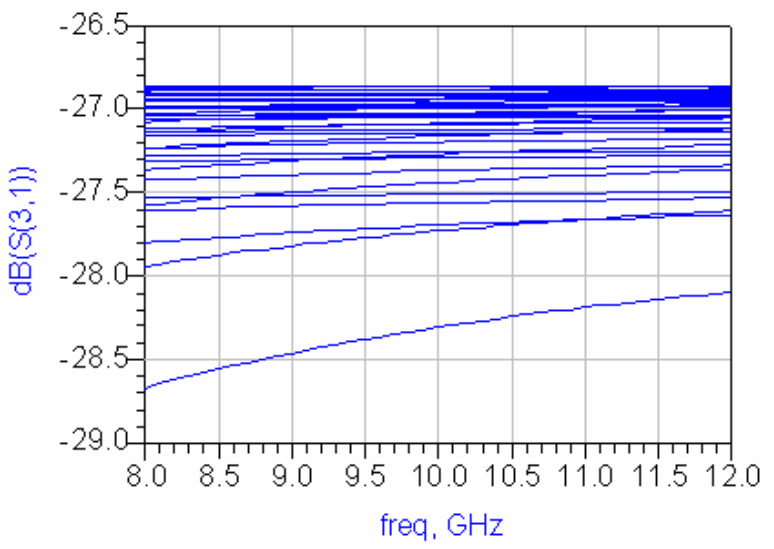

Figure 5.4 Results of swept simulation with Rg=1000 Ω (Isolation between gate and drain)

The setup in **Figure 5.1** was also used for finding the insertion loss of the ON state and the isolation of the OFF state in order to investigate the effect of gate resistor on these values. Below is the result of the swept simulation where the gate resistor is swept between 500 Ω and 3000 Ω. The transistor is ON, that is Vg=0. The geometry of the transistor is selected an average one: 40 μm gate width and 4 gate fingers. The insertion loss decreases as the gate resistor is increased. As seen in the graph, the improvement in the insertion loss for values larger than 2000 Ω is not significant. Therefore, better isolation of the gate favors better ON characteristics.

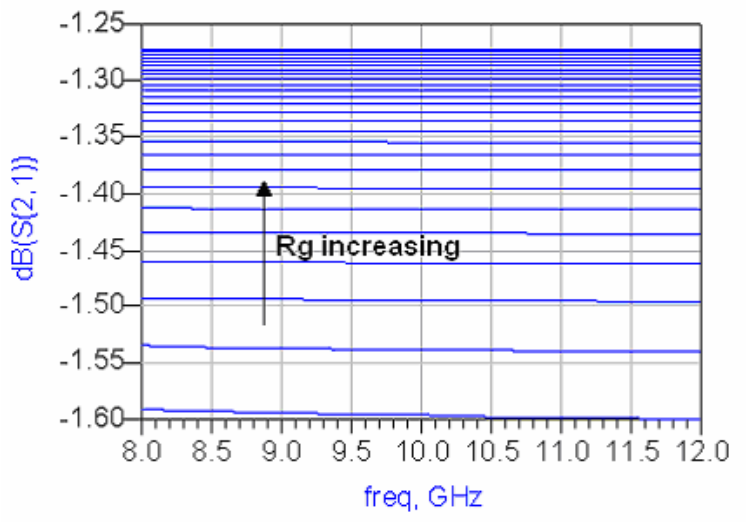

Figure 5.5 Effect of Rg on the insertion loss of the transistor in the ON state

The effect of the gate resistance to isolation in the OFF state is also investigated, the below result is obtained:

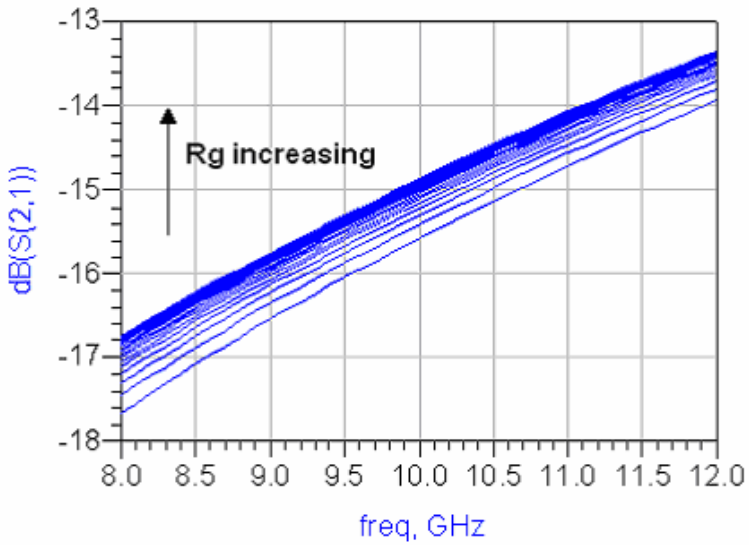

Figure 5.6 Effect of Rg on the isolation of the transistor in the OFF state (Isolation between source and drain)

Although the isolation deteriorates slightly for larger gate resistances, it is not attractive enough to prefer small gate resistance, keeping the gate isolation in mind. Further, it is understood that the leakage to the gate is a strong candidate for the reason of the improvement in the isolation of drain and source.

These simulations help to conclude that the required resistor to be connected to the gate of the transistor is about 2000 Ω. Keeping it smaller than this value aggravates both the insertion loss and the isolation of the gate from drain and source in the ON state. Increasing it, is of no significant improvement and complicates the layout of the overall circuitry. In the following SPDT and phase bit designs, the gate resistance is always 2000 Ω.

5.1.1. Design of an SPDT with OMMIC Components

A single pole double throw switch to be used in switched filter type phase bits was designed with the OMMIC components. The structure is a series-shunt switch because the isolation of a series transistor is not sufficient (not more than 20 dB) as

seen in **Figure 5.6**. In a series shunt SPDT, the gate biases of the series and shunt transistors of an arm are complementary. That is, when the series transistor is ON, the shunt transistor is OFF and vice versa. **Table 5.1** and **Figure 5.7** can be referred for operation of the series-shunt SPDT:

Table 5.1 The list of gate bias values for each transistor in **Figure 5.7** to select ports 2 or 3

Gate Bias of Q1	Gate Bias of Q2	Gate Bias of Q3	Gate Bias of Q4	Selected Port
0 V	-2 V	-2 V	0 V	Port 2
-2 V	0 V	0 V	-2 V	Port 3

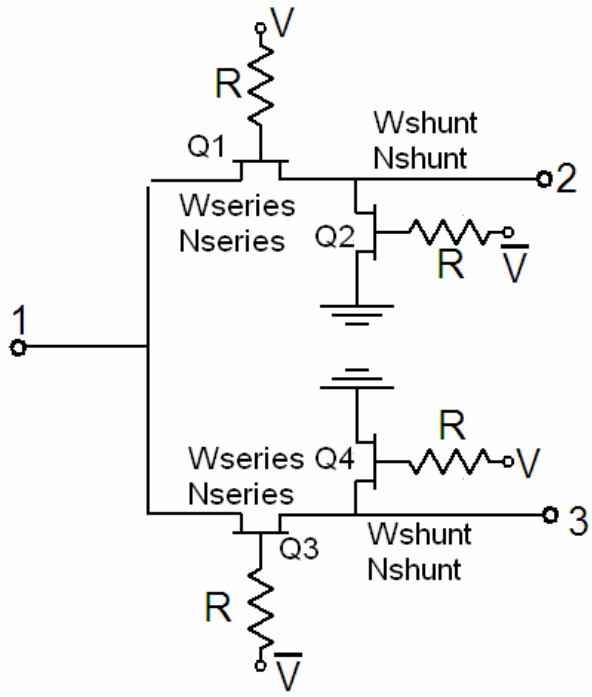

Figure 5.7 Series – Shunt SPDT structure

The gate widths and numbers of gate fingers of the above three port device were optimized to have low insertion loss, good match at the input and high isolation:

The optimization goals were:

- Input return loss < -20 dB
- Insertion loss of the selected arm < 1.2 dB
- Isolation of the unselected arm from the input > 25 dB

The optimization goal for the insertion loss of the selected arm was 1.2 dB because even a single medium sized transistor had more than 1.2 dB loss (Refer to **Figure 5.5**). The optimization engine could not find a solution with the above goals. Relaxing the goals is not desired, as these are already relaxed goals. If more loss is allowed, then the insertion loss of the phase shifter bit that uses this switch will probably be more than 2.5 dB, because there are two switches in the path. If less isolation is allowed, the leaking signal will enter the inactive phase path and interfere with the signal in the active path. Therefore, the topology must be changed at this conjecture. A resonating inductor is added in parallel with the series transistor as seen in the following figure:

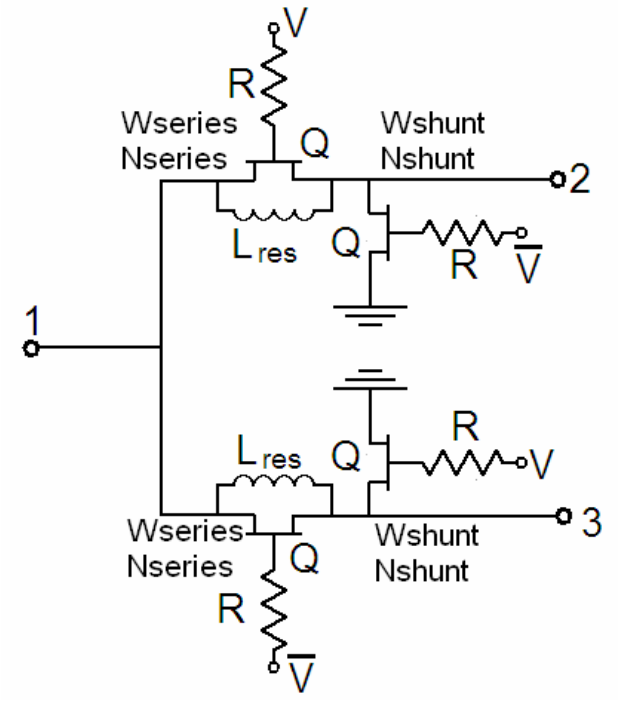

Figure 5.8 Series – Shunt SPDT with resonating inductor

Same optimization goals are maintained. The introduction of the resonating inductor increases the isolation and relaxes variables for optimizing other parameters (return loss and insertion loss).

With the values in **Table 5.2** found by optimization, the performance in **Figure 5.9** and **Figure 5.10** is obtained:

Table 5.2 Components used in the SPDT with resonating inductor

Wseries, Nseries	45.9 µm, 4
Wshunt, Nshunt	38.9 µm, 6
Lres	1.79 nH
R	2000 Ω (W=10µm)

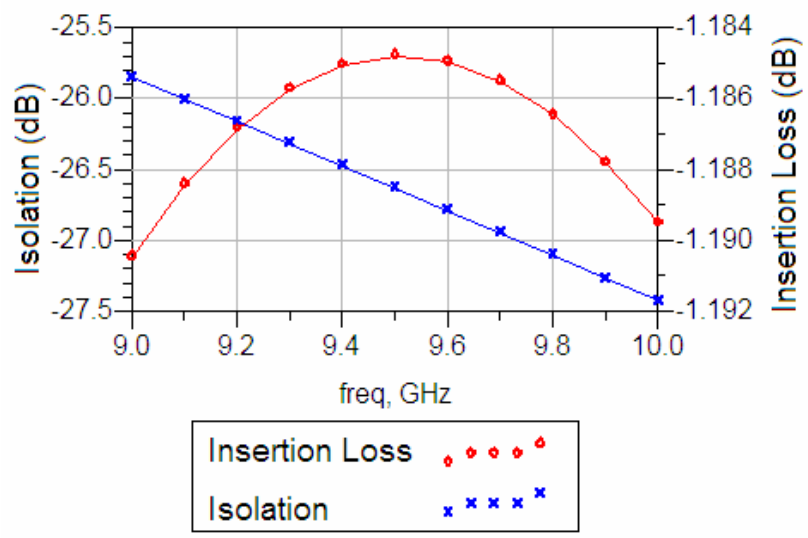

Figure 5.9 Isolation and insertion loss of the SPDT designed with OMMIC components

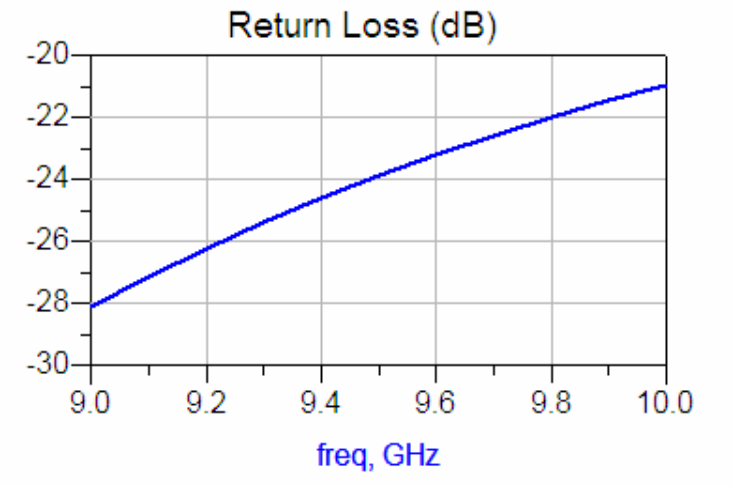

Figure 5.10 Input return loss of the SPDT designed with OMMIC components

The performance is definitely better than that of the SPDT without resonating inductor. However this SPDT, if its layout is constructed, will be quite large because the resonating inductor is approximately 180 μm by 180 μm and there will be 4 of them, if a switched filter topology is designed. Therefore, an SPDT with very good isolation might not be preferred if a narrowband phase shifter is to be designed, because of its augmented size.

Ignoring the layout practicality, using these SPDTs, a 90 degree bit with ideal elements has been designed and simulated. The values of filter elements are found out by (3-14) and (3-15), and they are not re-optimized for the purpose of observing the degradation. The degradation of the phase bit is observed for two cases: 1) SDPT used is the one with a resonating inductor; 2) It is the one without a resonating inductor. The performances corresponding to these two cases are seen in **Figure 5.12** and **Figure 5.13**, respectively.

In **Figure 5.11** the legend for the following performance graphs is given. It applies throughout this chapter.

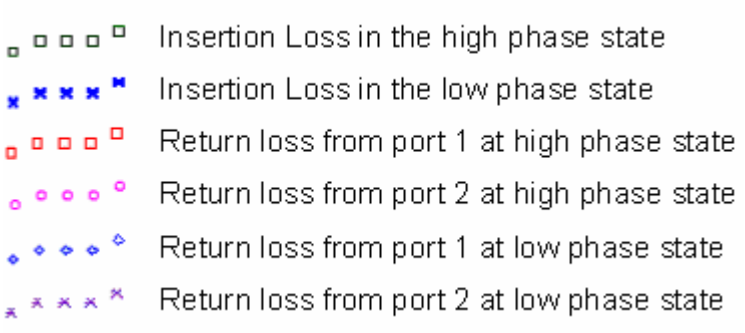

Figure 5.11 The legend to be referred for the bit-performance graphs

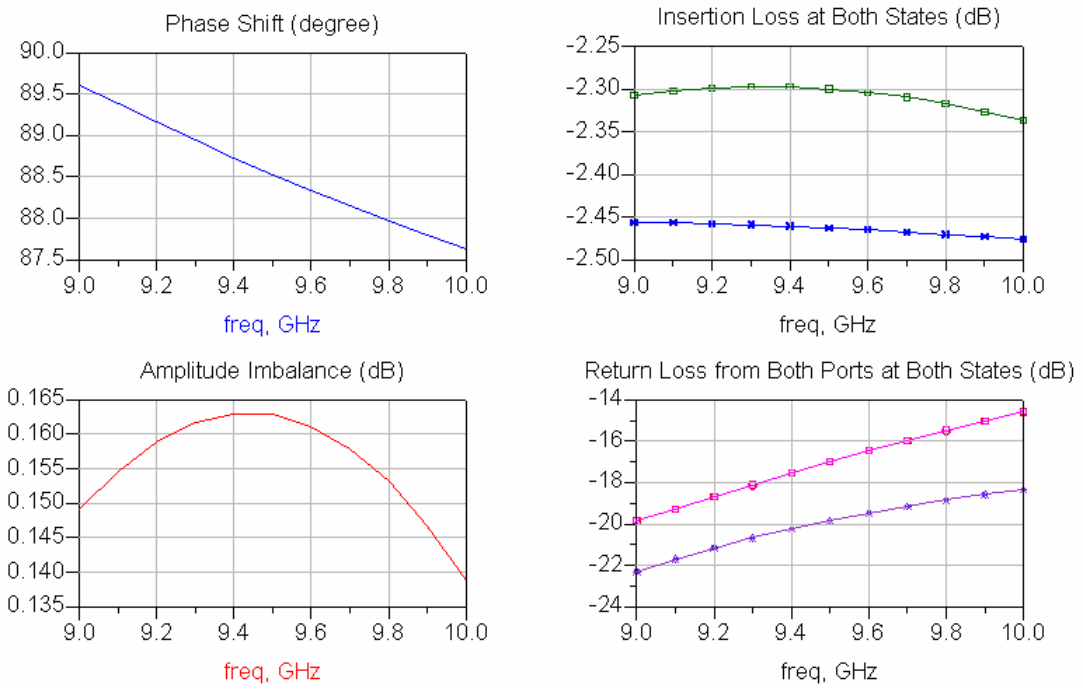

Figure 5.12 Performance of 90 degree bit where SPDT **does** have a resonating inductor

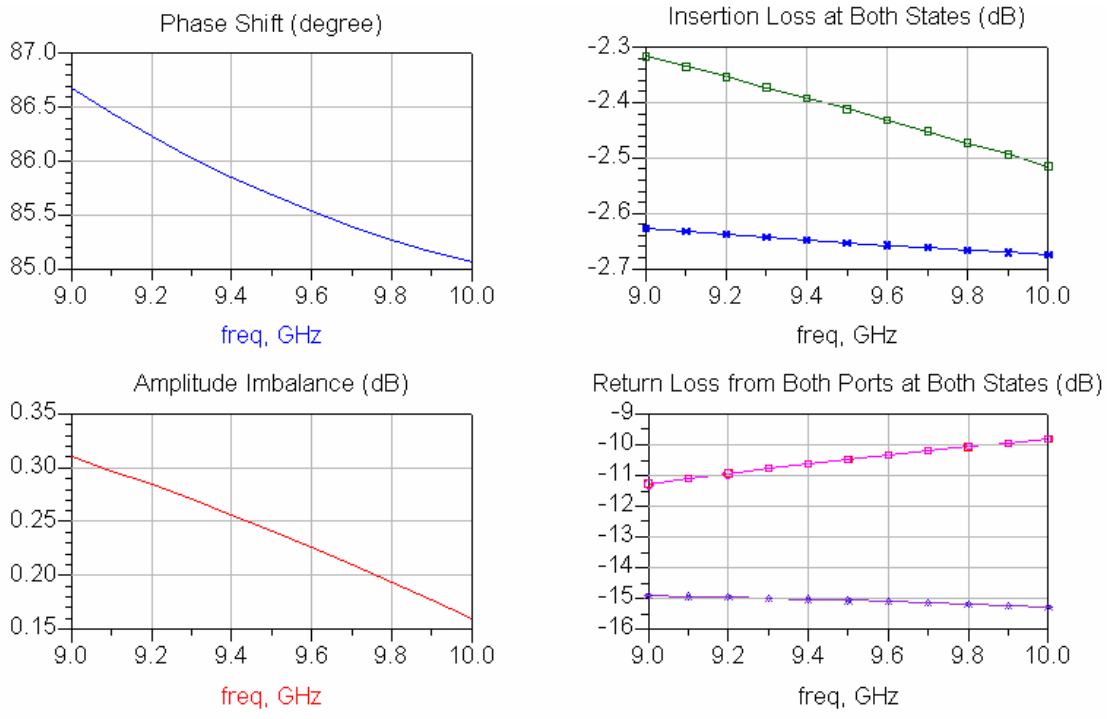

Figure 5.13 Performance of 90 degree bit where SPDT **does not** have a resonating inductor

Examining the two graphs, it is seen that when the employed SPDT isolation and return loss are in conformity with the desired goals, the degradation suffered is more graceful than that suffered when the SPDT isolation and return loss are poor.

However, in any case, the phase shift is not the same as the designed phase shift and the return loss and amplitude imbalance are not sufficiently well. To enhance these properties, optimization can be carried out on both filter elements and SPDT transistors. Keeping in mind that, be there a resonating inductor or not, these SPDTs are quite large and complicated for layout, single series transistor switch appears as a solution. Therefore, instead of optimizing these structures, HP/LP networks with single series transistors are studied and optimized.

5.1.2. SPDTs used for the 90° and 180° bit

The insufficient isolation offered by the series shunt SPDT with large area and complicated layout encouraged the usage of single series transistors as switches due

to the lower insertion loss and fairly easy layout offered. Every element in the following structures in **Figure 5.14** and **Figure 5.15** therefore, is optimized to have the desired phase shift, insertion loss, return loss and amplitude imbalance. The approach of first designing the filters and compensating for the degradation upon introduction of SPDTs is abandoned. Now, the leakage to the unselected filter is handled by overall optimization of all components.

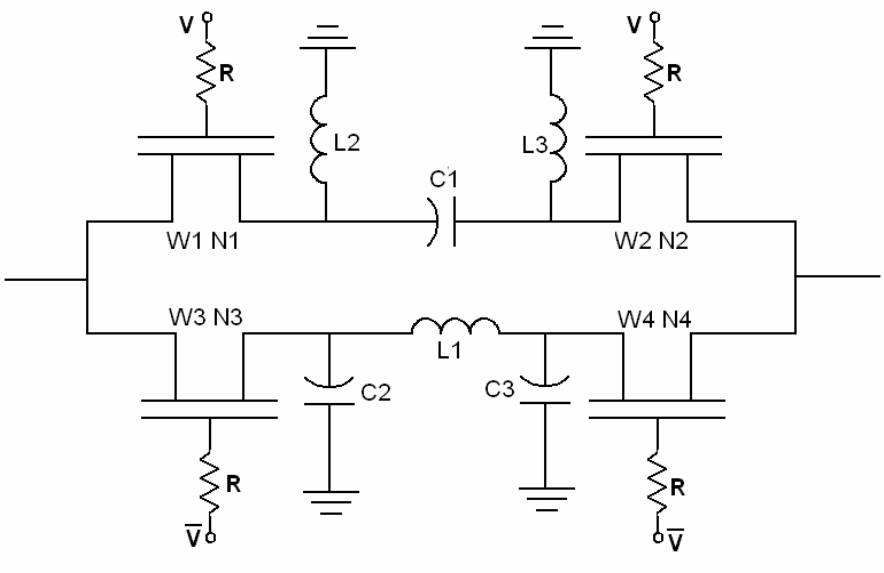

Figure 5.14 Topology used for the 90º bit

The reason for selecting the high pass section as PI type is to guarantee that the drains of the transistors at that arm do not float. The shunt inductors not only serve as filter elements, but they also provide choking paths for the upper transistors. For the lower transistors, however, the drains float regardless of the filter being TEE type or PI type. Care must be taken when integrating this bit into the circuit such that the sources of the lower transistors are somehow choked to the ground at any state of the phase shifter.

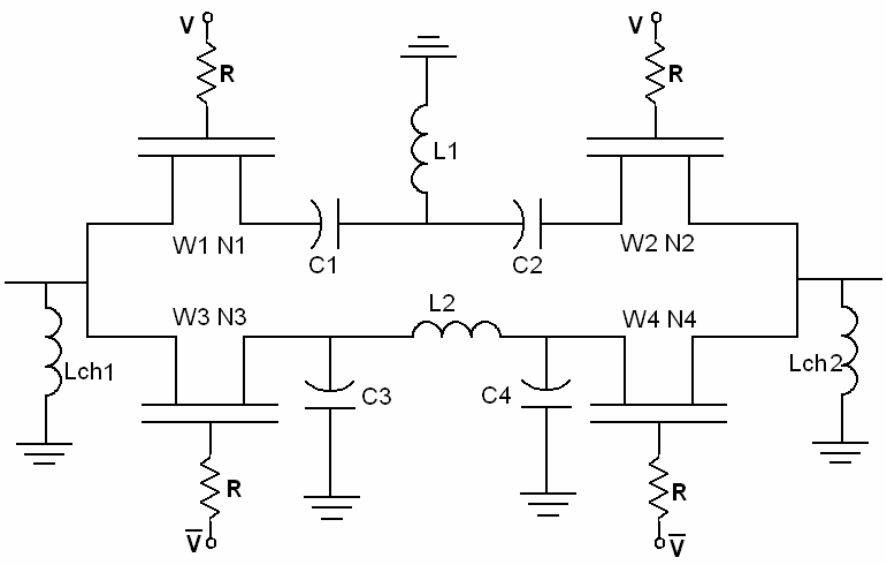

Figure 5.15 Topology used for the 180º bit

As for the 180 degree bit, the design is such that none of the 4 transistors suffer from any possible floating problem, thanks to the two choking inductors at the input and the output. Furthermore, they are ready to survive the neighboring transistors from such a problem. Also, there is no need for the high pass filter to be PI type and therefore single inductor for both HP and LP section can be used. The cost of guaranteeing that the drain's not floating is the increased circuit size and layout complexity. The details of designs of these two bits will be given later.

5.2. Design of a Seven Bits of the Phase Shifter

The principal problem of designing a digital phase shifter of several phase bits is the selection of appropriate topology for each bit. In fact, any network having two different phase states is a phase shifter, but answers to following questions are critical:

- Is this network matched at these two states?
- Do any of the two states introduce too much insertion loss?
- Is there a severe difference of insertion losses between two states?
- Is the desired phase shift maintained sufficiently flat over a bandwidth?

- Does the circuit occupy too much area, when its layout is constructed?

These questions are not new and are no irrelevant to the phase shifter requirements explained in Chapter 2. However, these discussions are dedicated to a single bit of a phase shifter, rather than the whole device. As a single bit is concerned, the return loss is a bit more critical than the return loss of the overall phase shifter circuit. The reason behind this is that, the degradation of the bit performance is strictly dependent on its own return loss and the return loss of the peripheral bits. Therefore, throughout the design process of the phase shifter, the matching of the bits was under consideration.

Actually, the requirements of a digital phase shifter have no regulation for the return losses of individual bits. Thus, a designer might select the way of designing the whole chip at once, without caring for the internal reflections. But for a 7 bit phase shifter, or even a 4 bit phase shifter, this means too many states to be simulated at the same time. Also at the optimization period, too many variables exist and too many goals are to be satisfied simultaneously. Although modern optimizers are quite powerful, this is a really difficult problem and the optimizer may not find a solution at all. The author's idea is that, this is not a better way than bit – by – bit design. Another advantage of the bit – by – bit design is the layout flexibility: Knowing the part at hand is matched to any other part, it can be placed anywhere whenever there is nothing preventing to do that.

5.2.1. Topologies Used in Design of the 7 Bit Phase Shifter

The design of the least significant three bits is relatively trivial compared to the more significant bits in the phase shifter, because the amount of the phase shift is small enough to be created by small perturbations in the networks. Also, relatively narrow bandwidth requirement allows this idea to be implemented. Hence, the bits 2.8125º, 5.625º and 11.25º are implemented in low pass / low pass type topologies. Indeed these topologies are specific to this study, but are not outstanding enough to be called "novel" due to their narrow bandwidth. By the term low pass – low pass, it is meant that, the circuit is a low pass structure in the first state and again a low pass structure

with a shifted pass-band in the other state. The details will be presented in the following sections, where the design of each bit is under focus.

For the most significant 2 bits, namely the 180º and 90º bits, a couple of different structures in the literature has been examined. The famous topology in [8] that incorporates the transistor OFF state capacitances as filter elements has been constructed and simulated for these bits, but due to the wideband nature of the topology, fairly large insertion loss was suffered. For the 90º bit, some topologies recommended for 45 degree bits at different frequency bands were checked out. Final decision was to use the classical switched LP/HP filters because none of the topologies studied was superior to that one at all criteria, such as insertion loss, return loss, phase flatness and size.

For the intermediate bits, 22.5º and 45º, the low-pass / high pass structures are not recommended because element values become impractical (an inductor of 2.19 nH for 45º and a capacitor of 3.4 pF for the 22.5º) to implement. The LP/LP type structures employed for the smallest 3 bits can not be used for these bits because the phase shift is not slight enough. Thus, although used at different bands, the common topology in [15] and [17] are utilized for the 22.5º bit. Finally, the network studied in [14] turned out to be a good remedy for the 45 degree bit.

In the following parts, the design, performance and layout of each bit will be explained in more detail. The design was not carried out in the given order. As a matter of fact various topologies were investigated for best performance for each bit. For the sake of neatness, the order of explanation will be from the least significant bit to the most significant bit.

5.2.2. Design of the Bits

5.2.2.1. Design of the 2.8125 degree bit

The following structure is used to generate 2.8125º phase shift:

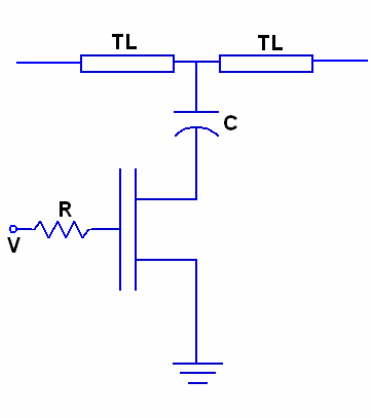

Figure 5.16 Structure for the 2.8125 degree bit

The transistor is ON in the first state and OFF in the second state. As the transistor is more or less equal to a small resistor in the ON state and a small capacitor in the OFF state, the circuit exhibits low pass characteristics in both states. The difference is that the shunt capacitance is smaller when the transistor is OFF, which results in different pass-bands and slightly different insertion phases between 9 and 10 GHz.

Layout of the bit is given below. The size of the bit is 185 μm x 250 μm.

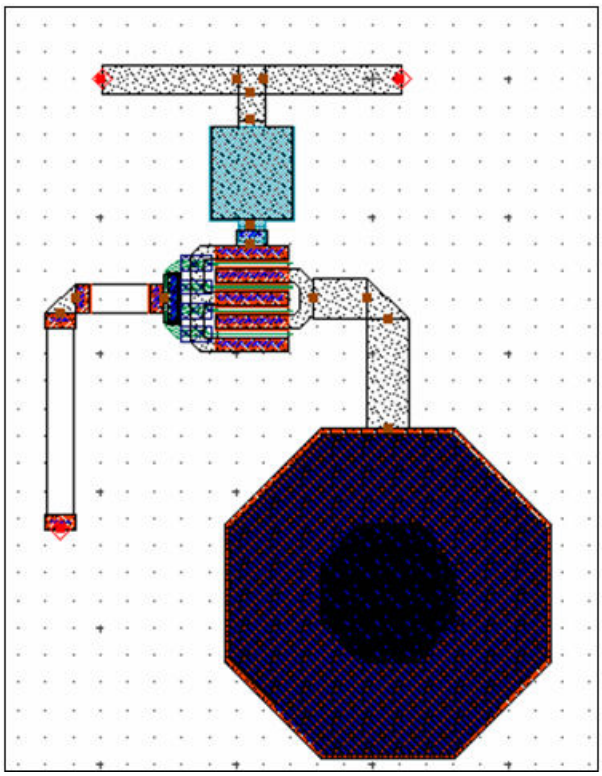

Figure 5.17 Layout of the 2.8125º bit

The bill of materials for the 2.8125º bit is given in the following table:

Table 5.3 List of components in the final 2.8125º bit

TL (Width, Length)	10 µm x 50 µm
C (Capacitance, Width)	57.4 fF, 30 µm
R (Resistance, Width)	2000 Ω, 10µm
Transistor (Gate Width, # of Gate Fingers)	24 µm , 4

In **Figure 5.18**, overall performance of the 2.8125º bit is observed.

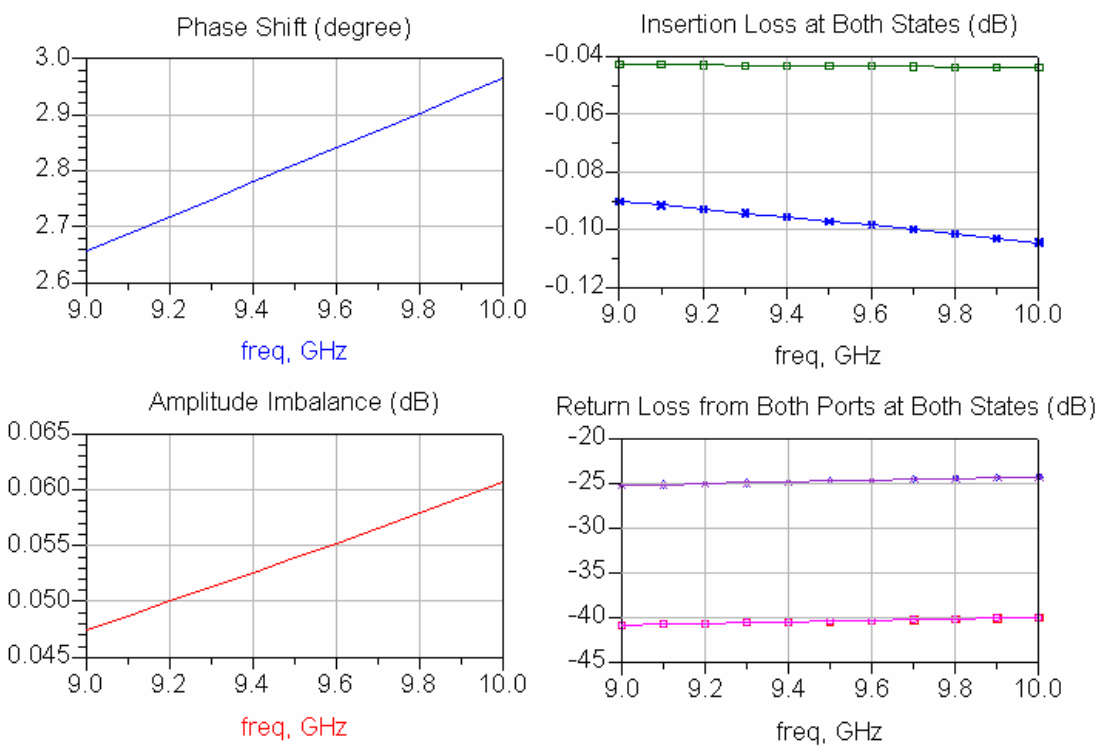

Figure 5.18 Final performance of the 2.8125° bit

The phase shift deviation for 2.8125 º bit in the operation band is ±0.15 degrees. Amplitude imbalance is low but always negative in the band due to LP/LP switching. Insertion loss is almost negligible and return loss is below -24 dB in both states from both ports, which is a promising performance regarding the integration of this bit with the others.

5.2.2.2. Design of the 5.625 degree Bit

Similar to the 2.8125º bit, the topology is again a LP/LP for the 5.625º bit. The sole difference from 2.8125º is the series inductors replaced with series transmission lines, as seen in the figures below. The theory of operation is the same as that of the 2.8125° bit.

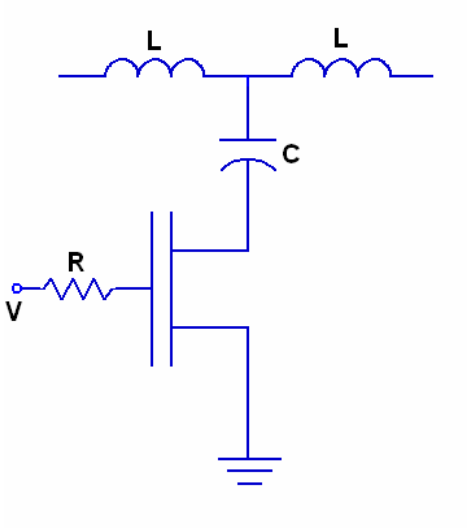

Figure 5.19 Structure for the 5.625 degree bit

The layout is given in **Figure 5.20**. The bit size is 295 µm x 185µm.

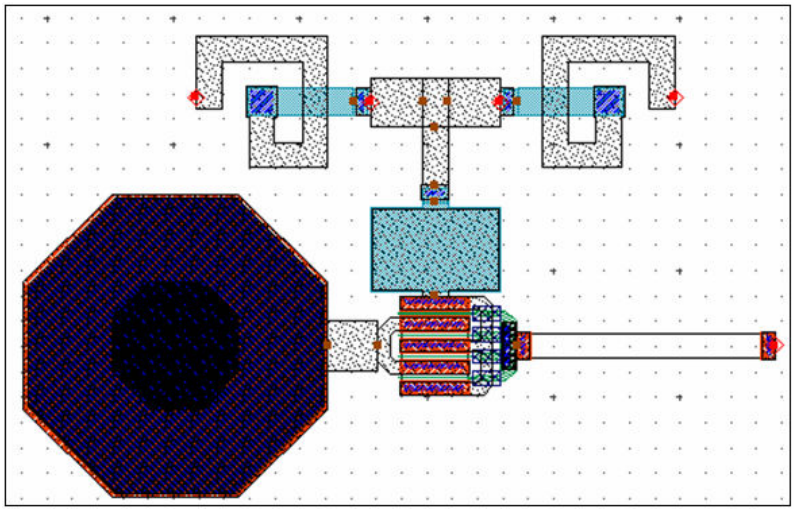

Figure 5.20 Layout of the 5.625º bit

The bill of materials for the final 5.625º bit is given in the following table:

Table 5.4 List of components in the final 5.625º bit

L (Inductance, Gap Width, Line Width)	0.121 nH, 10 µm,10 µm
C (Capacitance, Width)	89.2 fF, 50 µm
R (Resistance, Width)	2000 Ω, 10µm
Transistor (Gate Width, # of Gate Fingers)	29.6 µm , 4

In the following figure overall performance of the 5.625° bit is presented:

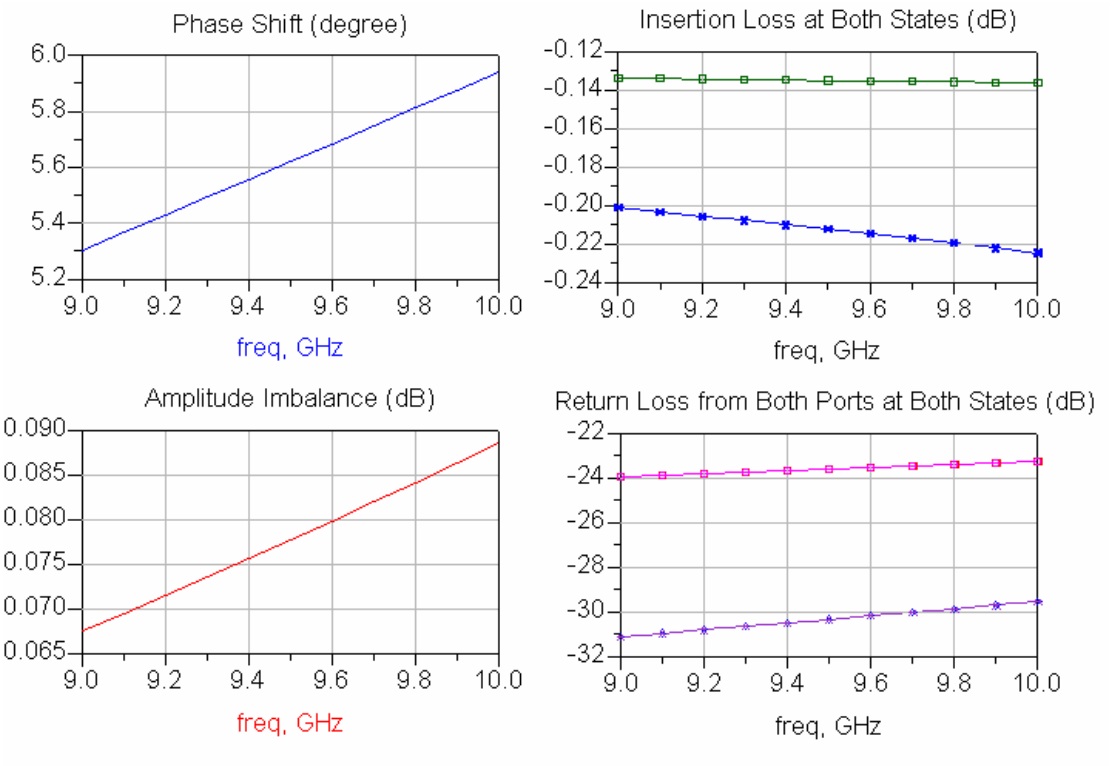

Figure 5.21 Final performance of the 5.625° bit

This bit also has good return loss at both ports and probably will not impose any problem in the integration period.

5.2.2.3. Design of the 11.25º Bit

The structure employed for 11.25º is again a LP/LP but it was hard to match the bit when the TEE type LP circuit used for the 5.625º was tried. Thus a PI type LP circuit with two shunt transistors is constructed and optimized for the 11.25º bit. Below are the circuit diagram and the component properties:

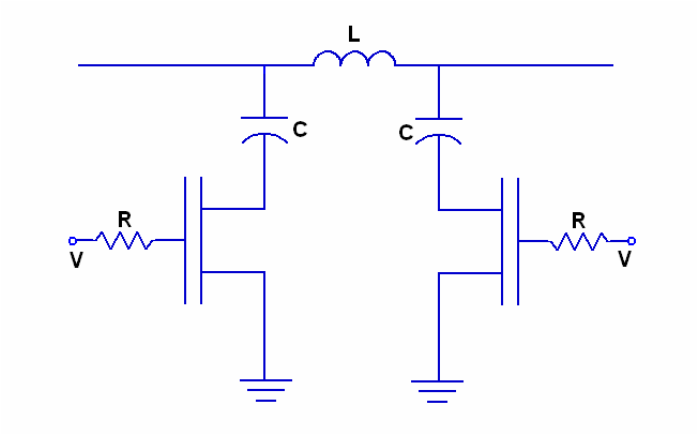

Figure 5.22 Structure for the 11.25° bit

The difference from the previous two bits is the PI type structure of the low pass filter used. Again the circuit is a low-pass filter when the transistors are both on and off, but the phase responses are offset within the band 9-10 GHz.,

Below is the layout of the bit. A single via grounds the drains of the transistors, which shrinks the layout of the bit slightly. The size of the bit is 445 µm x 275 µm.

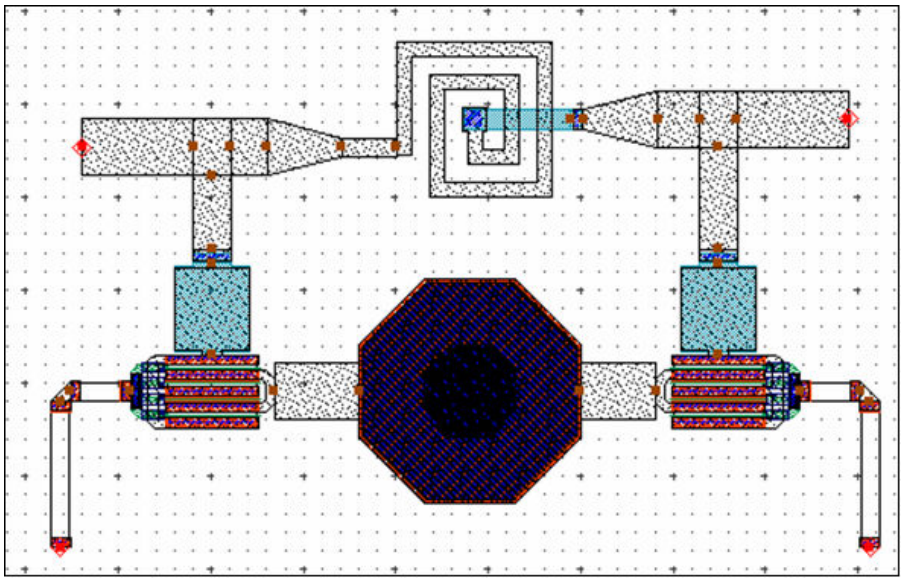

Figure 5.23 Layout of the 11.25° bit

For the final element values, following table can be referred:

Table 5.5 List of components in the final 5.625º bit

L (Inductance, Gap Width, Line Width)	0.377 nH, 10 µm, 8 µm
C (Capacitance, Width)	98 fF, 40 µm
R (Resistance, Width)	2000 Ω, 10µm
Transistors (Gate Width, # of Gate Fingers)	50 µm , 4

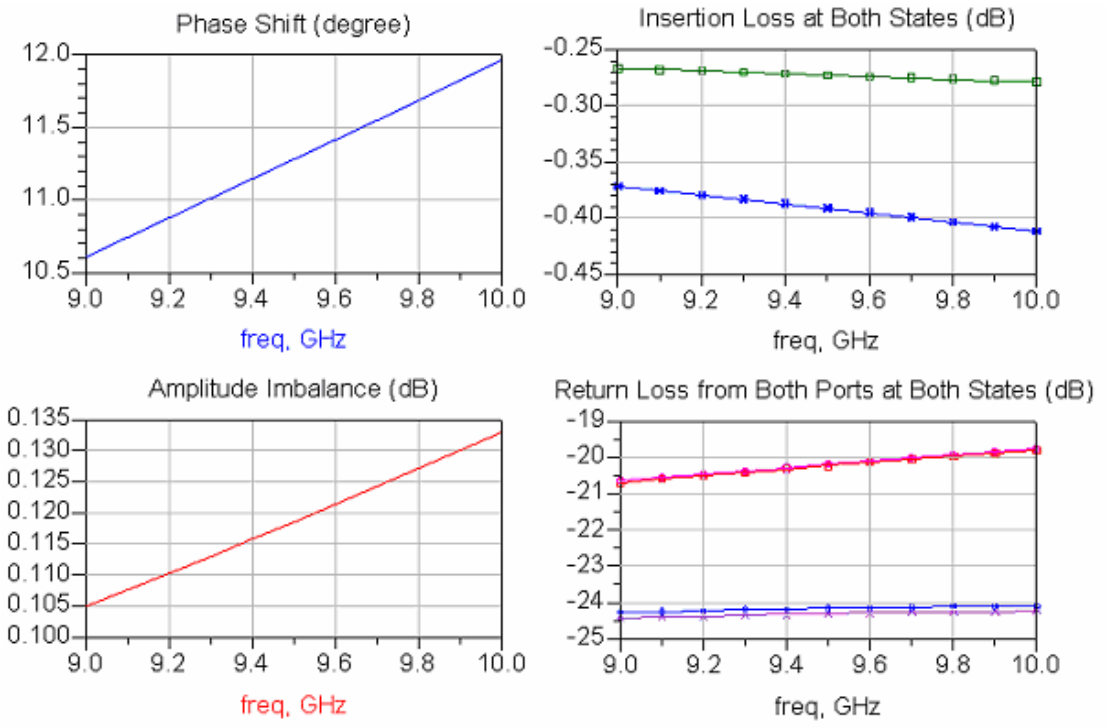

Figure 5.24 Final performance of the 11.25° bit

The phase error (±0.75°) and the amplitude imbalance (0.133 dB max) are a bit higher than the previous bits. These could be made better to the expense of sacrificing from the return loss but in that case, the phase error and amplitude imbalance of the overall chip could degrade when this bit is cascaded with the others.

5.2.2.4. Design of the 22.5º Bit

In the design of the 22.5° bit, the topology recommended commonly in [15] and [17] is used and optimized. The structure is given in **Figure 5.25**. The upper two transistors, Q1 and Q2, are commonly biased and the lower shunt transistor, Q3 is biased complementary to them. When Q1 and Q2 are ON and Q3 is OFF a high pass

filter with high shunt impedance is realized. When the biases are just the other way, a TEE type low pass filter appears [15]. The wideband response of the designed circuit revealing the high pass and low pass behavior at two states is given in **Figure 5.26**.

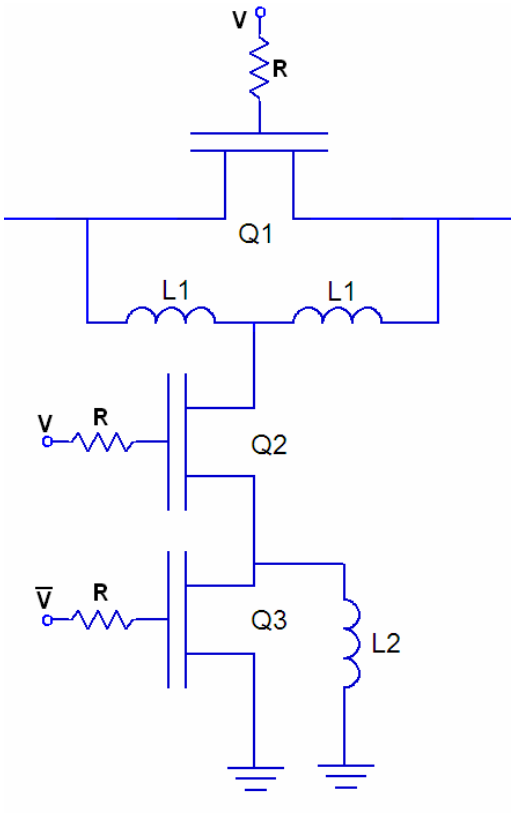

Figure 5.25 Structure utilized for the realization of 22.5° bit [15], [17]

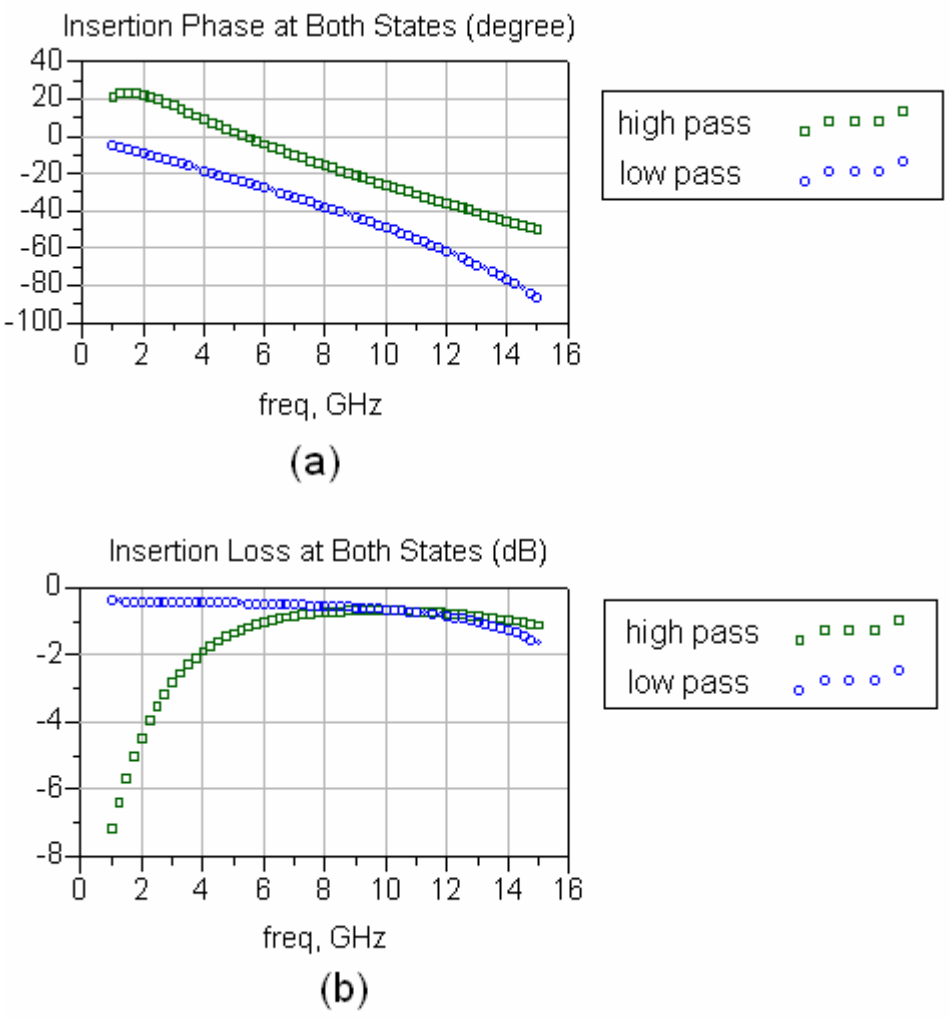

Figure 5.26 (a) Insertion phases and (b) insertion losses corresponding to high pass and low pass states of the 22.5° bit in 1-15 GHz band

The layout of the bit is given in **Figure 5.27**. The size of the bit is 600 μm x 760 μm.

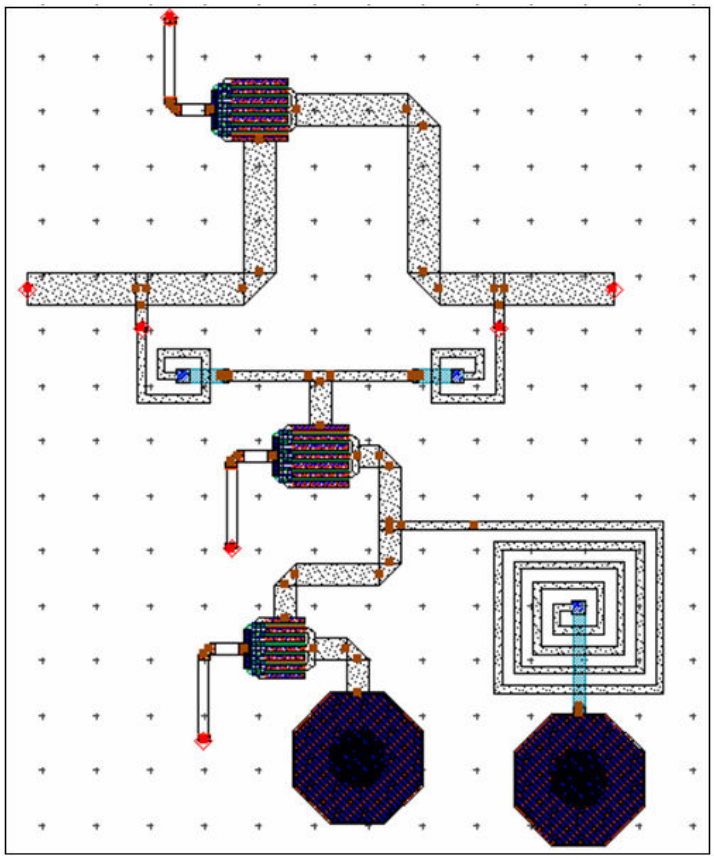

Figure 5.27 Layout of the 22.5° bit

A tedious second optimization was necessary after the layout was constructed because of the insertion of microstrip lines between the ports and the terminals of the transistor Q1 (**Figure 5.25**). Final element values are in **Table 5.6**.

Table 5.6 List of components in the final 22.5º bit

L1 (Inductance, Gap Width, Line Width)	0.210 nH, 11 µm, 7 µm
L2 (Inductance, Gap Width, Line Width)	1.75 nH, 11 µm, 7 µm
R (Resistance, Width)	2000 Ω, 10µm
Q1 (Gate Width, # of Gate Fingers)	50 µm , 6
Q2 (Gate Width, # of Gate Fingers)	49.5µm , 6
Q3 (Gate Width, # of Gate Fingers)	35 µm , 6

The overall performance of the 22.5° bit is given in **Figure 5.28**.

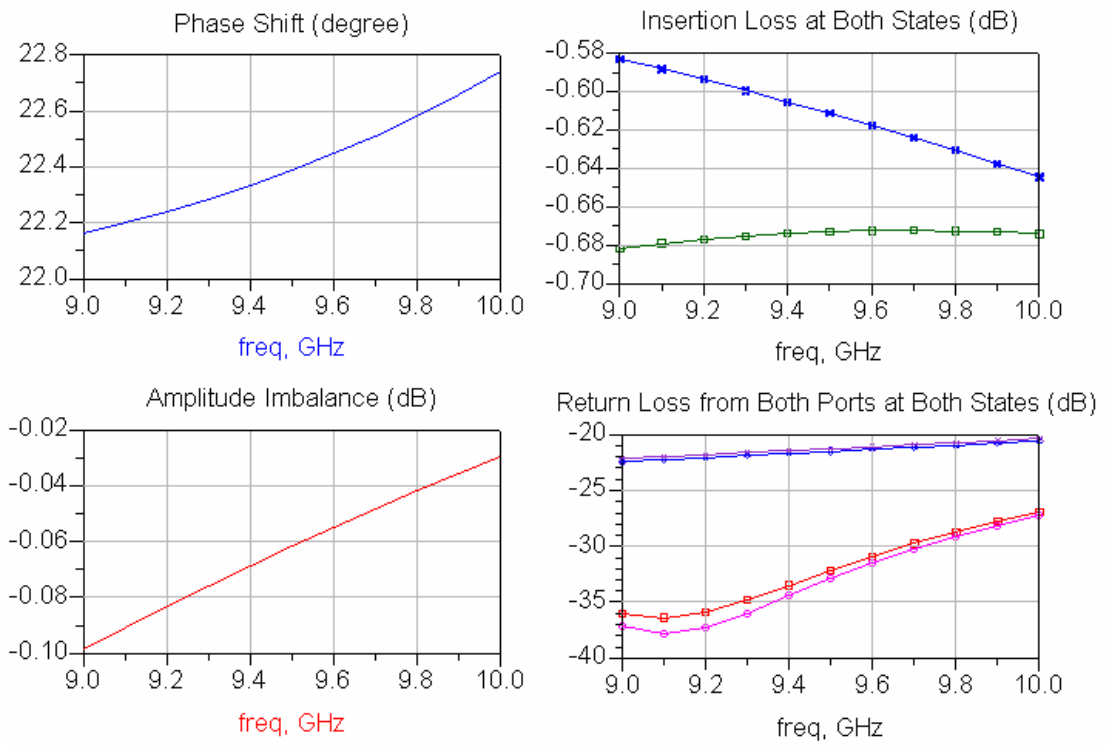

Figure 5.28 Final performance of the 22.5° bit

The topology used for the 22.5 degree bit was not proven successful for the 45°, that is, either too much phase variation was suffered, or return loss became intolerably high. A different topology was sought and found in [14]. Although the technology is a bit different, relying on mHEMTs, the bandwidth of operation is the same and satisfactory performance was obtained. The topology recommended in [14] is given in **Figure 5.29**.

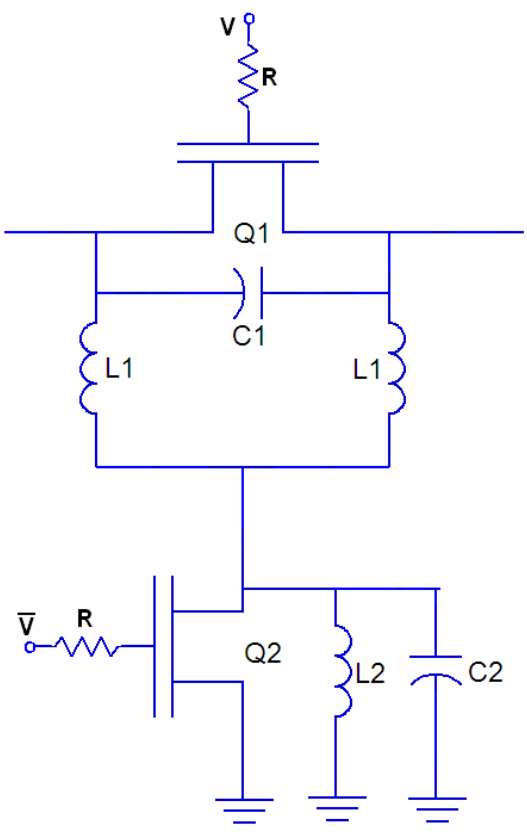

Figure 5.29 Structure utilized for the realization of 45° bit [reference]

The two transistors are operated in complementary fashion. The circuit is a PI type high pass filter when Q1 is OFF and Q2 is ON. On the other hand, when biases are reversed, the OFF capacitance of the transistor Q2 and plus the capacitor C2 resonates with the inductor L2. Therefore they isolate the upper part from the ground and the signal effectively flows through the ON resistance of Q1 [14].

The layout of the bit is given in **Figure 5.30**. The size of the bit is 500µm x 720µm.

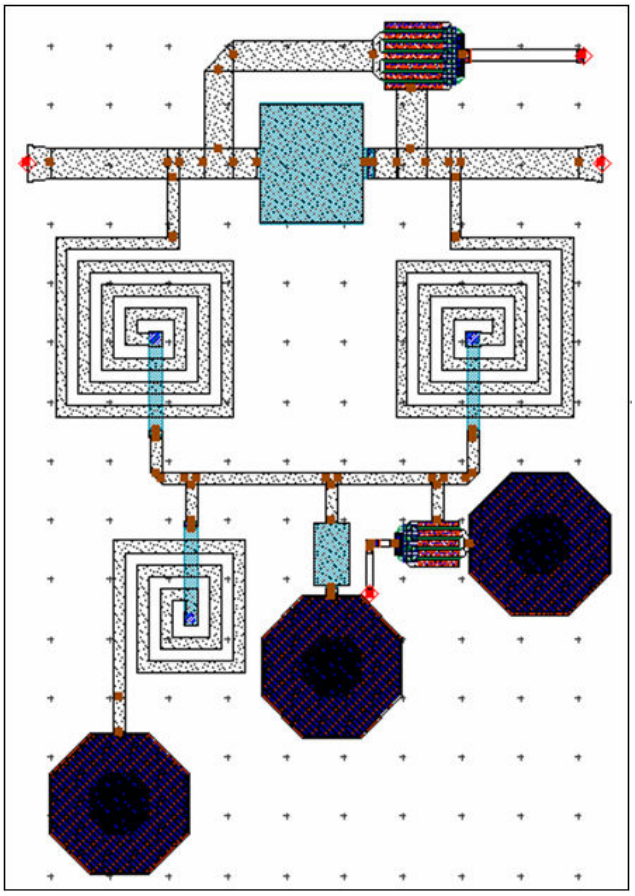

Figure 5.30 Layout of the 45° bit

The element values are in the following table.

Table 5.7 List of components in the final 44.5º bit

L1 (Inductance, Gap Width, Line Width)	1.2 nH, 10 µm, 10 µm
L2 (Inductance, Gap Width, Line Width)	0.662 nH, 10 µm, 10 µm
C1 (Capacitance, Width)	450 fF, 100 µm
C2 (Capacitance, Width)	83.6 fF, 30 µm
R (Resistance, Width)	2000 Ω, 10µm
Q1 (Gate Width, # of Gate Fingers)	48 µm , 6
Q2 (Gate Width, # of Gate Fingers)	34 µm , 4

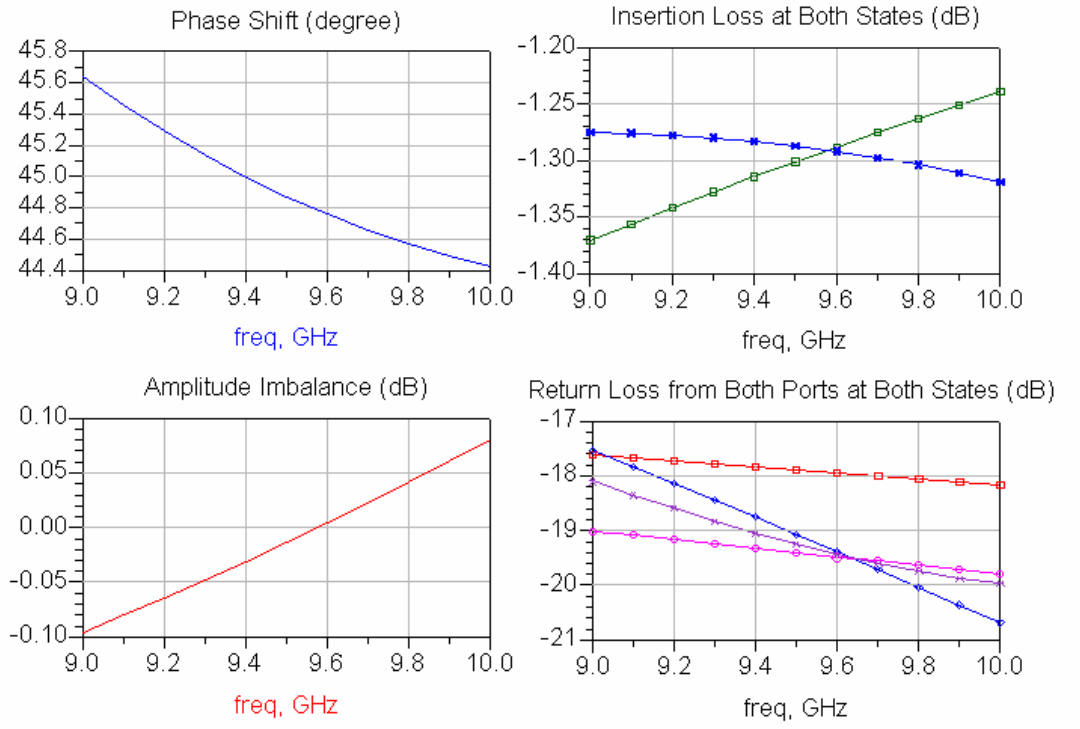

Figure 5.31 Performance of the 45° bit

5.2.2.5. Design of the 90° bit

As explained before, HP/LP topologies are used for the 90° and 180° bits. The SPDTs are composed of a single series transistor only. There is no claim that they have enough isolation, but the limited isolation they present is taken into consideration by overall optimization of the circuit elements. The following structure where both high pass and low pass sections are realized in PI type networks serves as the 90° bit. The mission of two shunt inductors in the high pass part is two fold: They are filter elements but they also protect the transistors Q1 and Q2 from floating drain or source situations. For the LP section the same feature can not be maintained with either TEE type or PI type because there is no shunt inductor in either case. When the bit is carefully placed among the other bits such that the lower transistors find a DC path to the ground, the problem is overcome.

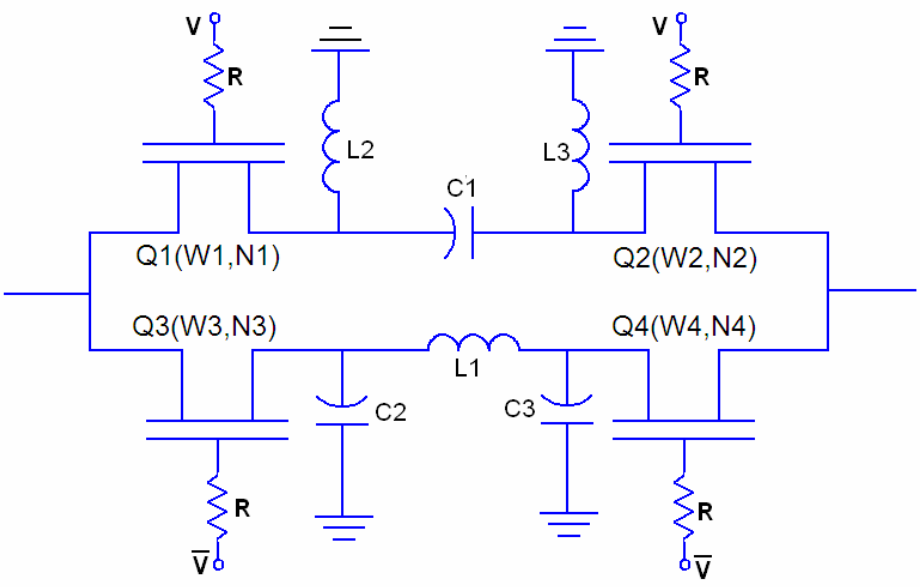

Figure 5.32 HP/LP topology used for realization of the 90° bit

The layout of the bit looks like the following. The bit size is 600 µm x 750 µm.

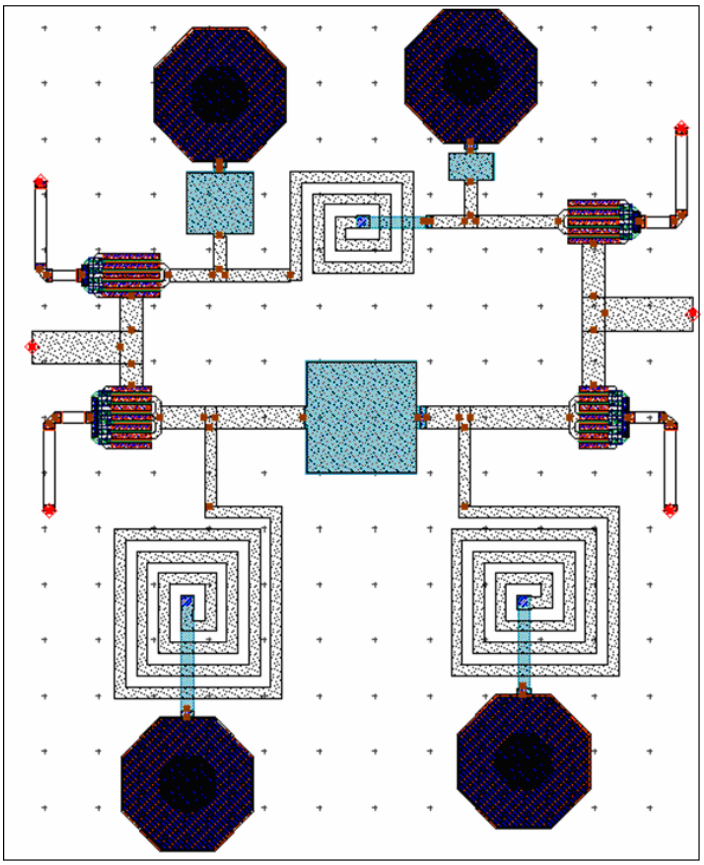

Figure 5.33 Layout of the 90° bit

Referring to **Figure 5.32**, the element values are given in the table below:

Table 5.8 List of components in the 90° bit

L1 (Inductance, Gap Width, Line Width)	0.5 nH, 10 µm, 10 µm
L2 (Inductance, Gap Width, Line Width)	1.377 nH 10 µm, 10µm
L3 (Inductance, Gap Width, Line Width)	1.246 nH, 10 µm, 10 µm
C1 (Capacitance, Width)	504 fF, 100 µm
C2 (Capacitance, Width)	171.5 fF, 60 µm
C3 (Capacitance, Width)	52.2 fF, 40 µm
R (Resistance, Width)	2000 Ω, 10µm
Q1 (Gate Width, # of Gate Fingers)	34.0 µm , 6
Q2 (Gate Width, # of Gate Fingers)	24.5 µm , 6
Q3 (Gate Width, # of Gate Fingers)	50.0 µm , 4
Q4 (Gate Width, # of Gate Fingers)	44.5 µm , 4

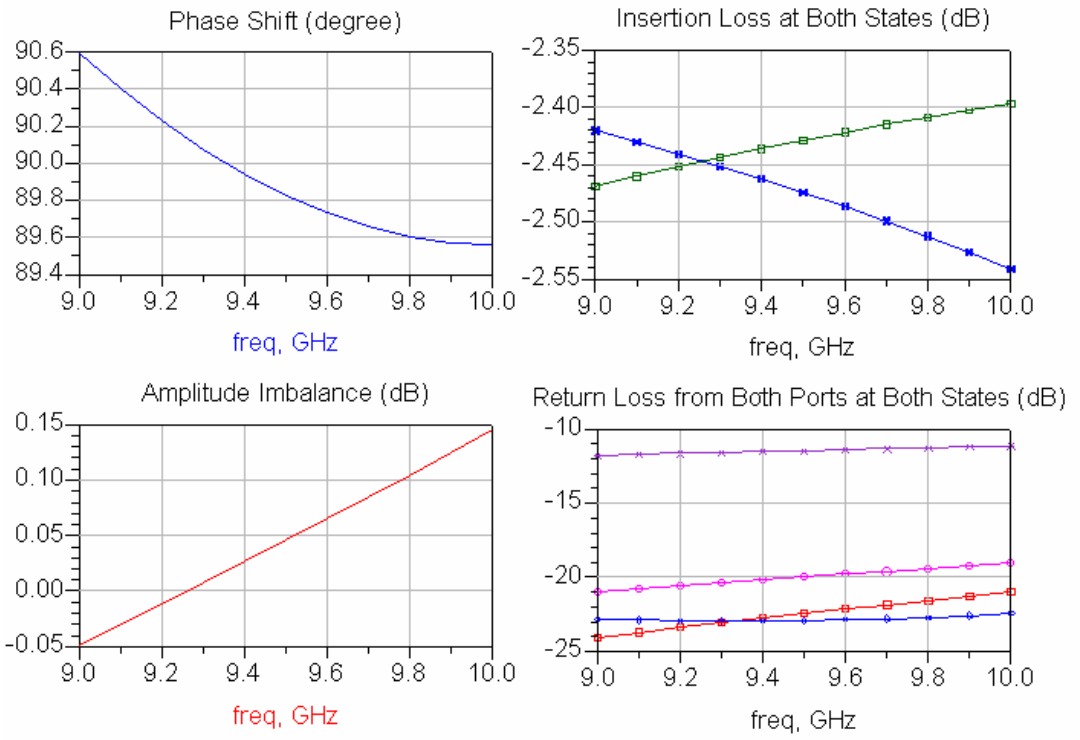

Figure 5.34 Performance of the 90° bit

5.2.2.6. Design of the 180º bit

In order to avoid floating source or drain problems in the 180° bit and possibly in two other bits, choke inductors are placed at the input and the output of the 180° bit, as seen in the figure.

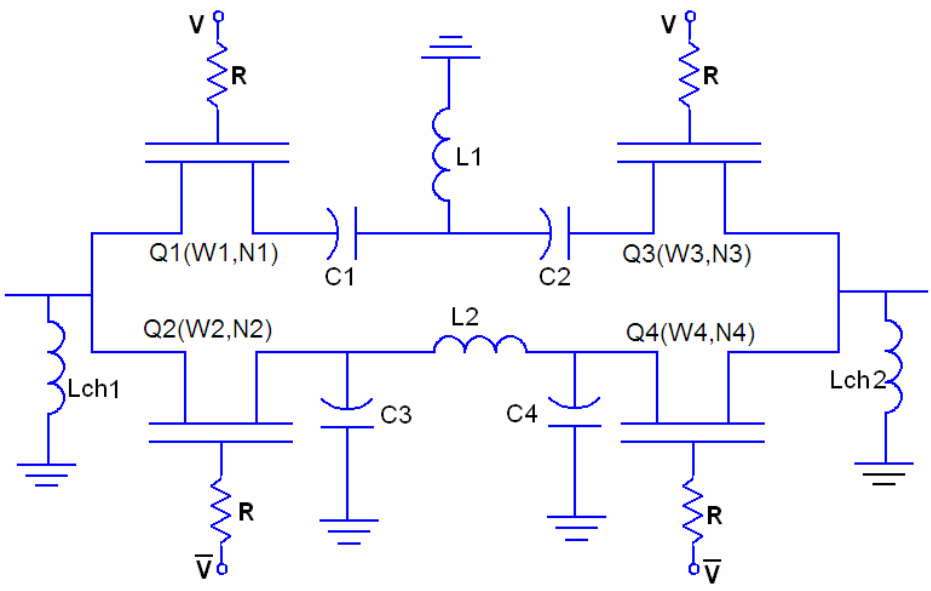

Figure 5.35 HP/LP topology used for realization of the 180° bit

The layout corresponding to this schematic is the following. The size of the bit is 770 µm x 815µm.

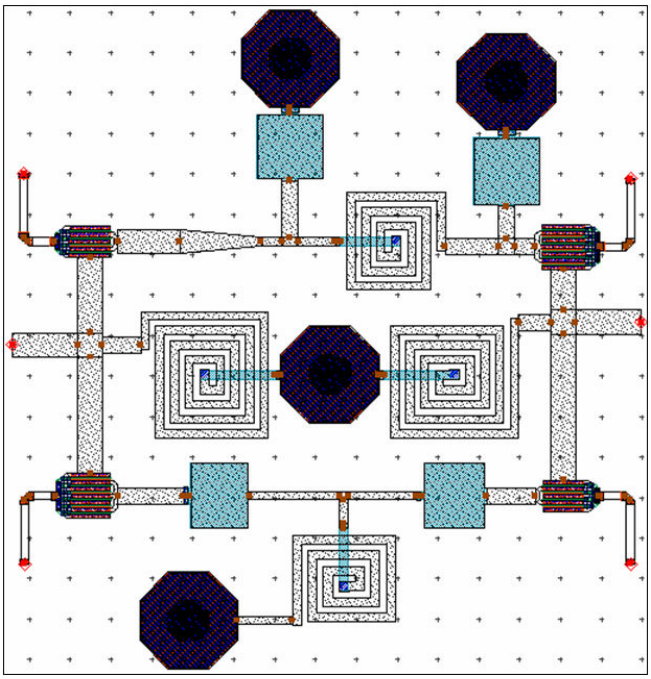

Figure 5.36 Layout of the 180° bit

All variables seen in **Figure 5.35** are again optimized to yield the desired response and these final values are obtained.

Table 5.9 List of components in the 180° bit

L1 (Inductance, Gap Width, Line Width)	0.697 nH, 8 µm, 11 µm
L2 (Inductance, Gap Width, Line Width)	0.765 nH 8 µm, 10µm
Lch1 (Inductance, Gap Width, Line Width)	1.344 nH, 8 µm, 10 µm
Lch1 (Inductance, Gap Width, Line Width)	1.4 nH, 8 µm, 10 µm
C1 (Capacitance, Width)	302.7 fF, 80 µm
C2 (Capacitance, Width)	287.7 fF, 80 µm
C3 (Capacitance, Width)	337.8 fF, 80 µm
C4 (Capacitance, Width)	323.1 fF, 80 µm
R (Resistance, Width)	2000 Ω, 10µm
Q1 (Gate Width, # of Gate Fingers)	49 µm , 4
Q2 (Gate Width, # of Gate Fingers)	50 µm , 6
Q3 (Gate Width, # of Gate Fingers)	47.1 µm , 6
Q4 (Gate Width, # of Gate Fingers)	48.1 µm , 4

The overall performance of 180º bit is seen in **Figure 5.37**.

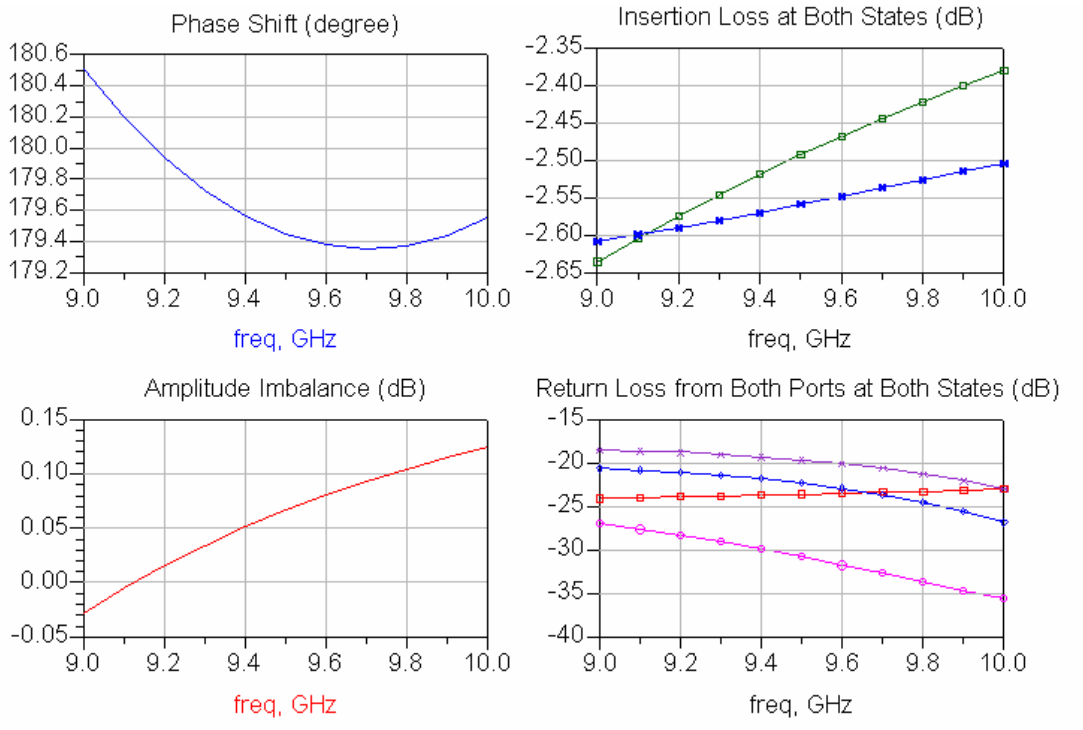

Figure 5.37 Performance of the 180° bit

CHAPTER 6

INTEGRATING THE BITS OF THE PHASE SHIFTER

The ease of integrating the bits, or the overall performance of the phase shifter, as mentioned before, strongly depends on the matching between the bits. The performance summary of all bits is given in **Table 6.1**. Apart from the 90º bit, the goal of maintaining low return loss at all bits is almost accomplished. Therefore, the 90º bit must be placed properly among others, so that return loss, phase variation, phase error and amplitude imbalance do not become intolerable. The number of different bit arrangements is computed to be as many as 80640, considering the order of bits and the possibility of flipping the asymmetrical ones. There is not an intuitive way of optimizing every parameter at the same time, but it does not either seem practical to carry out a full Monte Carlo analysis due to extremely large number of combinations and simulations to be carried out. Furthermore, the performance of the phase shifter is not composed of a single parameter. For an optimization to make sense, the performance parameters must be weighted properly, which is subject to discussion. Thus, an optimization was not executed for the arrangement of the bits.

Two methods were tried when integrating the bits. First the bits are simply cascaded in the order of significance. Second, they are cascaded in the light of a MATLAB program whose details will be given later.

Table 6.1 The summary of critical performance parameters for every bit

Bit	S_{21} @ 9.5 GHz (averaged over 2 states)	S_{11} and S_{22} at both states	Phase error	Amplitude Imbalance
180º	-2.5 dB	< -18 dB	±0.6º	< 0.12 dB
90º	-2.5 dB	< -11 dB	±0.5º	< 0.14 dB
45º	-1.28 dB	< -18 dB	±0.6º	< 0.09 dB
22.5º	-0.64 dB	<-20 dB	±0.3º	< 0.10 dB
11.25º	-0.33 dB	< -19 dB	±0.7º	< 0.14 dB
5.625º	-0.18 dB	< -22 dB	±0.3º	< 0.09 dB
2.815º	-0.07 dB	< -24 dB	±0.15º	< 0.06 dB

6.1. Integration 1

The bits are cascaded in order of significance as in **Figure 6.1**.

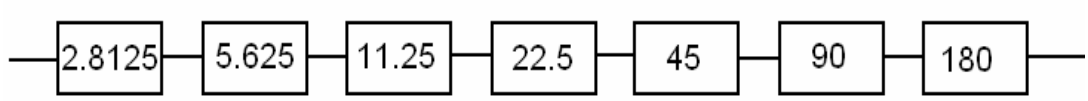

Figure 6.1 The sequence of the bits

The phase error of the phase shifter is seen in **Figure 6.2**.

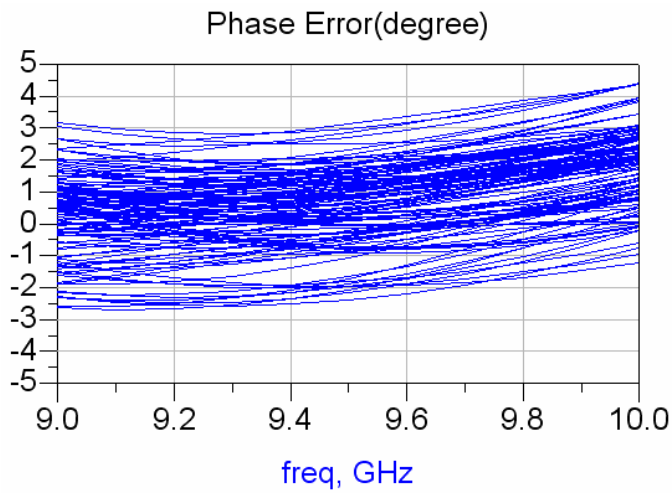

Figure 6.2 The phase error of the phase shifter at all 128 states

In **Figure 6.3** and **Figure 6.4** the return losses from ports 1 and 2 are seen respectively.

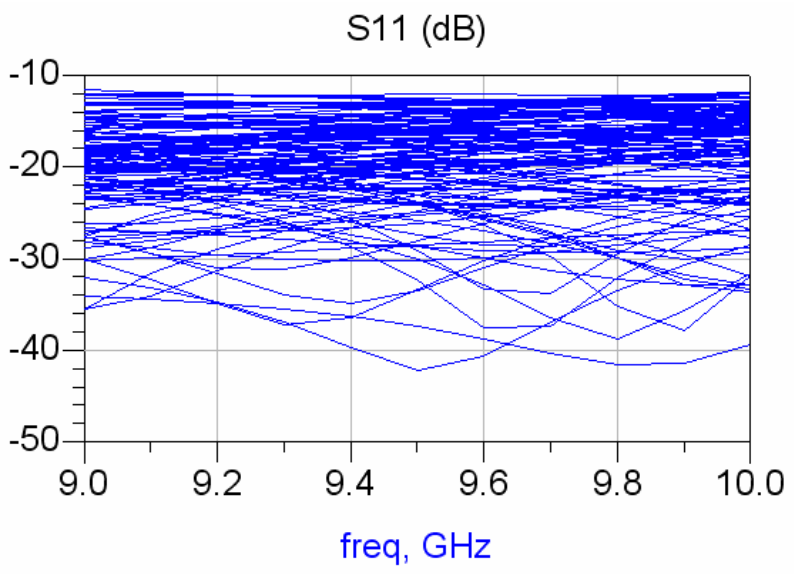

Figure 6.3 The return loss from the first port of the phase shifter at all 128 states

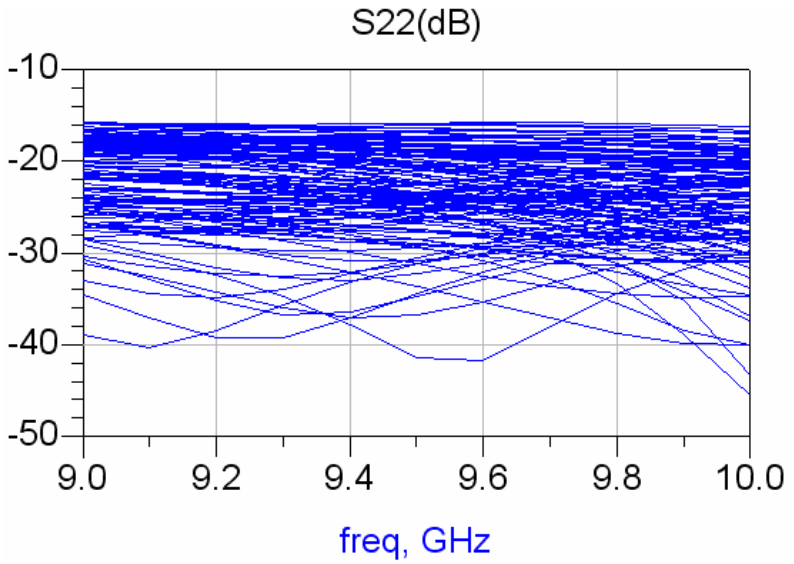

Figure 6.4 The return loss from the second port of the phase shifter at all 128 states

The reference phase state was chosen as the one with the lowest insertion phase. Following plot shows the amplitude variations from the reference amplitude (The amplitude at reference phase state).

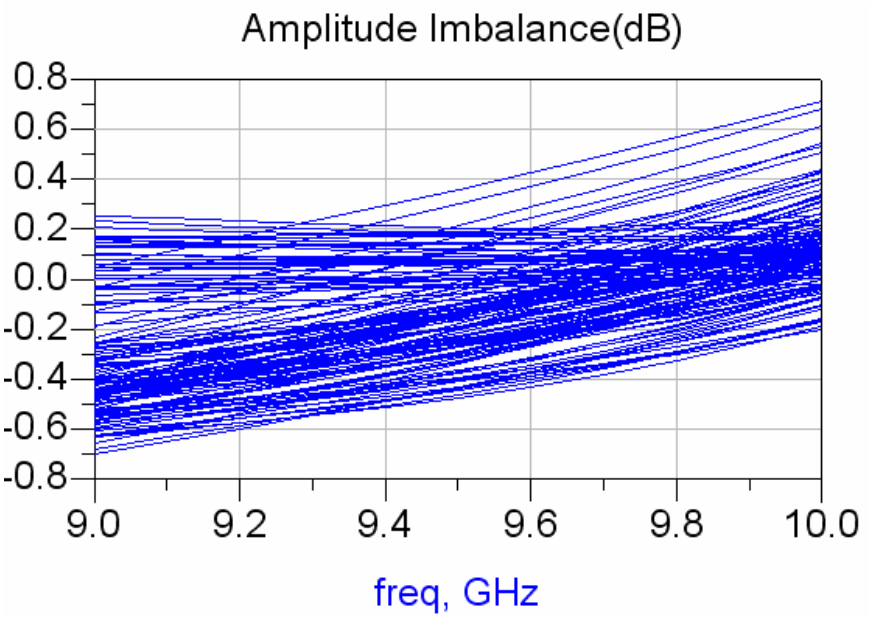

Figure 6.5 The amplitude variation of the phase shifter referenced to the lowest phase state

In the following graph, the insertion loss at all 128 states can be observed.

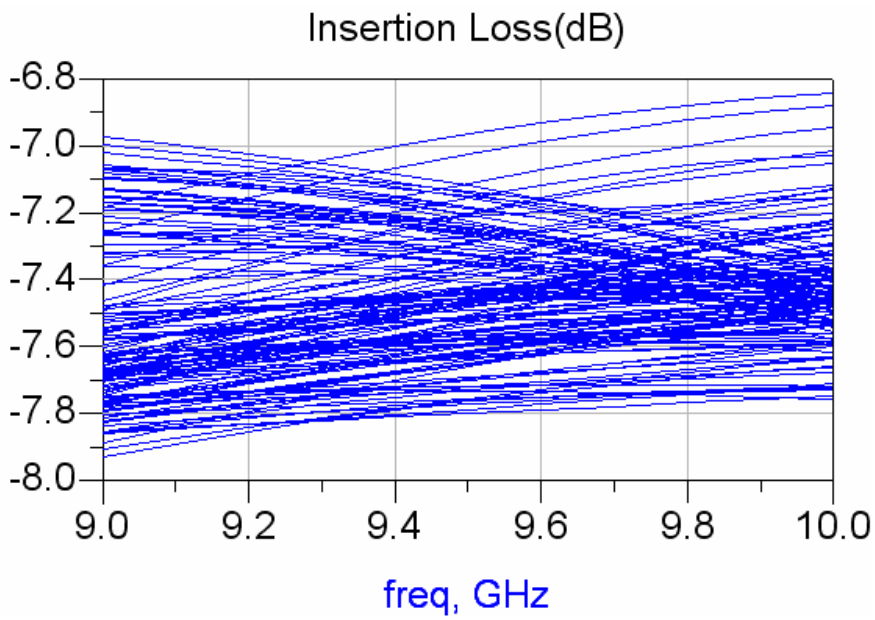

Figure 6.6 The insertion loss of the phase shifter at all 128 states

6.2. Integration 2

The sequence of the bits was not altered, but the 90º bit was changed. In the design of the first 90º bit, the optimization goal was to make return loss from two ports at both states below -20 dB. The optimization resulted such that the return loss from port 2 at low phase state is only better than -11 dB while the other three values were below -18 dB. In the new 90º bit all 4 return loss values (refer to **Figure 5.11**) are desired to remain below -15 dB. The optimization resulted in a more balanced return loss, in other words, the overall return loss was not three good return losses and one bad return loss. Now all 4 return loss values are close to each other but they are all below -15 dB. The performance of this new 90º bit is given in **Figure 6.7**. This modification resulted in an upgraded phase error as seen in **Figure 6.8**. However, the return loss is slightly degraded (**Figure 6.9** and **Figure 6.10**)

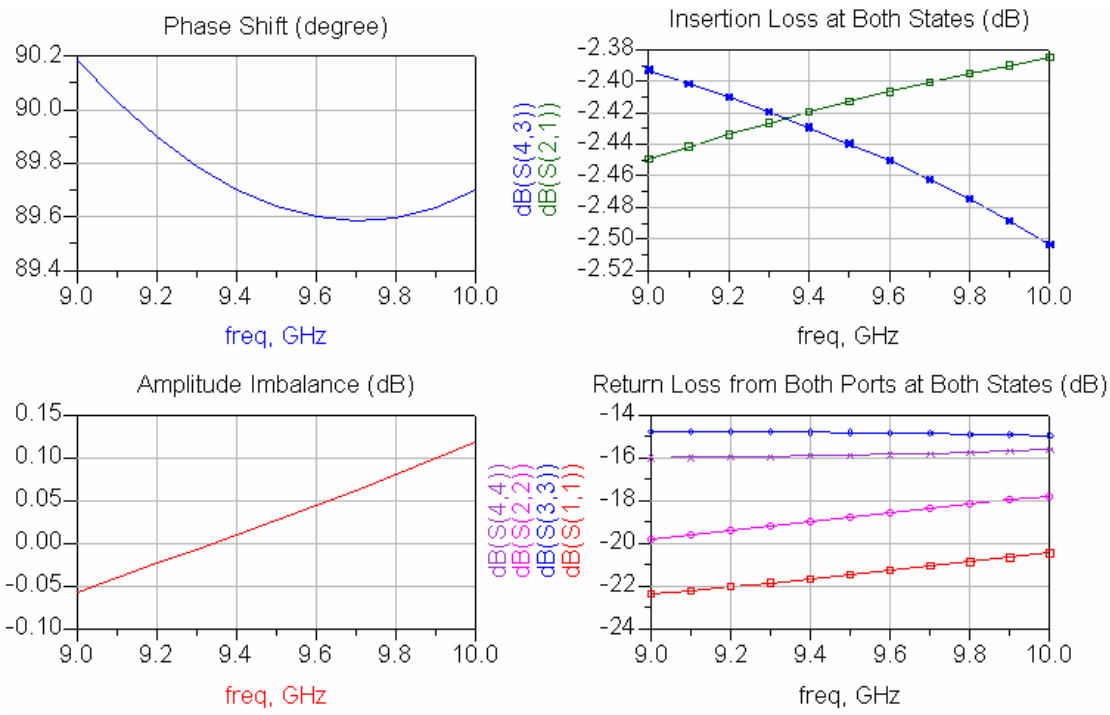

Figure 6.7 Performance of the modified 90º bit

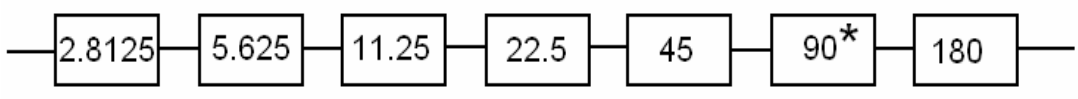

Figure 6.8 The phase shifter schematic with modified 90º bit

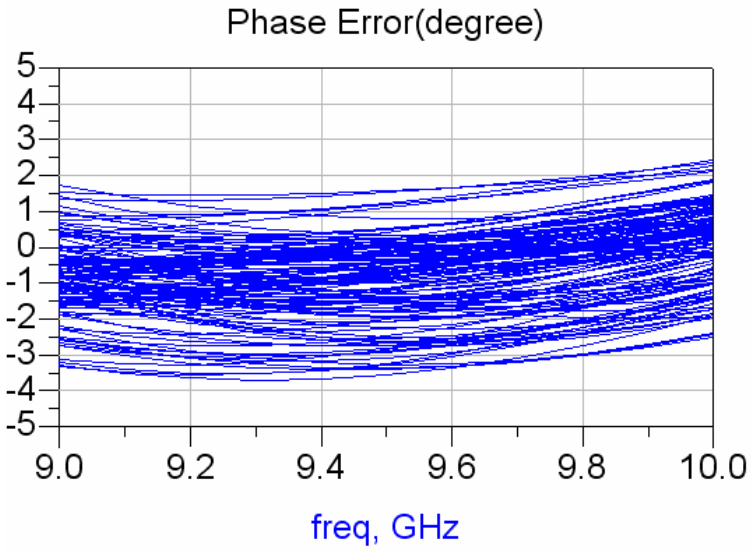

Figure 6.9 The phase error of the phase shifter with the modified 90º bit

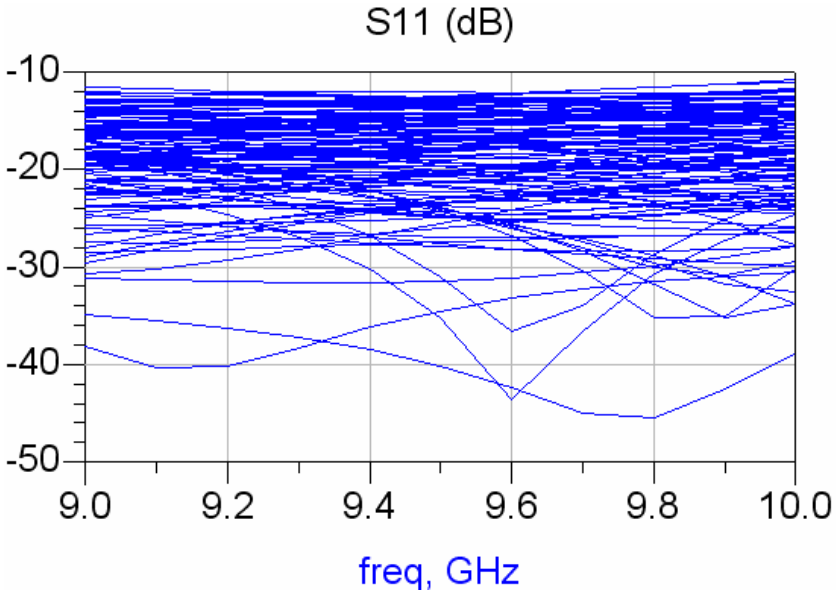

Figure 6.10 The return loss from the first port of the phase shifter with the modified 90º bit

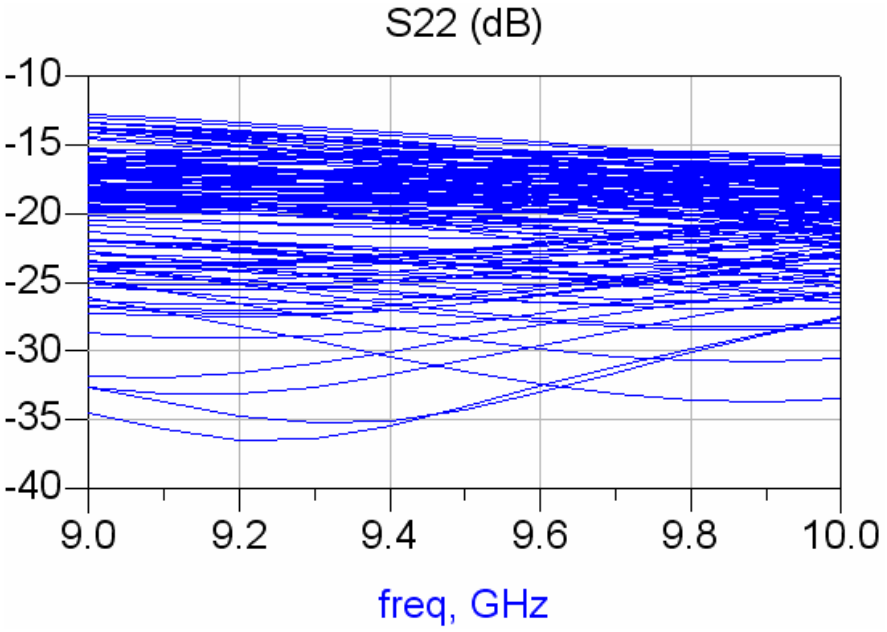

Figure 6.11 The return loss from the second port of the phase shifter with the modified 90º bit

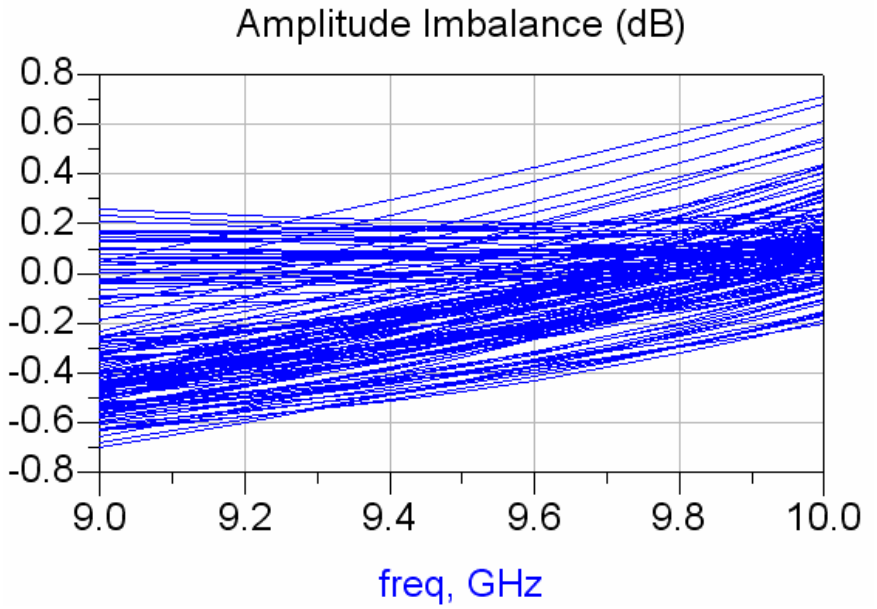

Figure 6.12 The amplitude variation of the phase shifter with the modified 90º bit

6.3. A MATLAB Program for Integration of Bits

Cascading the bits in order of significance is definitely not a smart way of obtaining the best performance. As mentioned previously, discarding the layout feasibility, there are 80640 different bit arrangements possible. Among these arrangements some of them offer low phase error while some offer good input or output match. It was felt that optimizing the behavior at the center frequency will probably lead to optimum performance over the operating bandwidth. A MATLAB program was built in order to see the worst case performance (worst among all states) of all different bit arrangements at 9.5 GHz. The program covers all possibilities by taking all permutations of 7 bits and for all permutations, allowing 4 of the 5 asymmetrical bits to flip horizontally.

The code was verified by the ADS program by taking random bit arrangements in ADS and observing that the numerical results are exactly the same. The sub-optimum bit arrangements will be evaluated for production but of course the layout feasibility and floating drain or source problems must be kept in mind.

The MATLAB code written does the following in essence:

- Takes the low-phase-state and high-phase-state S parameters of all bits as input (14 files).
- Converts these S parameters to ABCD parameters.
- Loops for 2^4 x 7!=80640 different bit arrangements.
- For a particular arrangement;
    - finds out S parameters of all 128 states of the phase shifter at center frequency by first multiplying the ABCD parameters of the bits in accordance with that particular arrangement, and then re-converting the overall ABCD parameters to S parameters again.
    - Records the following (only @ 9.5 GHz)
        - Worst case S_{11}
        - Worst case S_{22}
        - Worst case amplitude variation
        - Peak phase errors of all states

        - Rms phase errors of all states
        - Average insertion loss of all states
    - Finds the arrangement for
        - Lowest S_{11}
        - Lowest S_{22}
        - Lowest amplitude variation
        - Lowest rms phase error
        - Lowest peak error

6.3.1. Results of the Batch Simulation

MATLAB plots obtained by the batch simulation are presented here. In these plots the horizontal axis represents the entire family of different bit arrangements.

In **Figure 6.13** the quantity exhibited is the peak phase error of the phase shifter. It is seen that the peak phase error might be as high as 8º for some arrangements. The lowest value is determined to be 1.7º and the corresponding bit arrangement is 1 – 6 – 5 – 4 – 3 – 7 – 2, where 1 corresponds to the least significant and 7 corresponds to the most significant bit. Also important is that the bits 6 and 7 are flipped. (w.r.t the layout given in Chapter 5). The worst return losses for this configuration are -9.2 dB (S_{11}) and -12.7 dB (S_{22}) The ADS simulation corresponding to this arrangement will be given later.

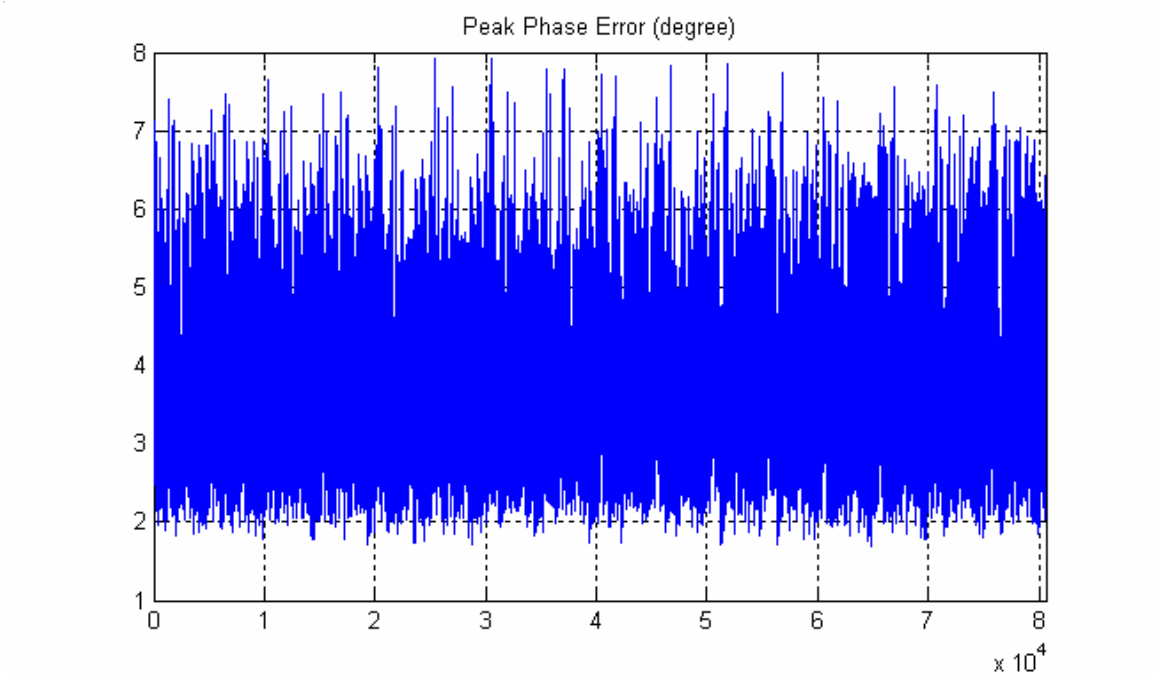

Figure 6.13 The variation of peak phase error of the phase shifter for all 80640 different bit arrangements

In **Figure 6.14** the rms phase error is presented. It varies between 0.74º and 5.27º. The lowest value, 0.74, occurs for the following bit arrangement: 1 – 5 – 2 – 7 – 3 – 4 – 6 with bit 4 flipped. Worst case S_{11} and S_{22} at 9.5 GHz for this arrangement are -10.2 dB and -10.6 dB respectively. This arrangement offers an amplitude imbalance (at 9.5 GHz) less than 0.7 dB for all states. The detailed ADS results will be given later.

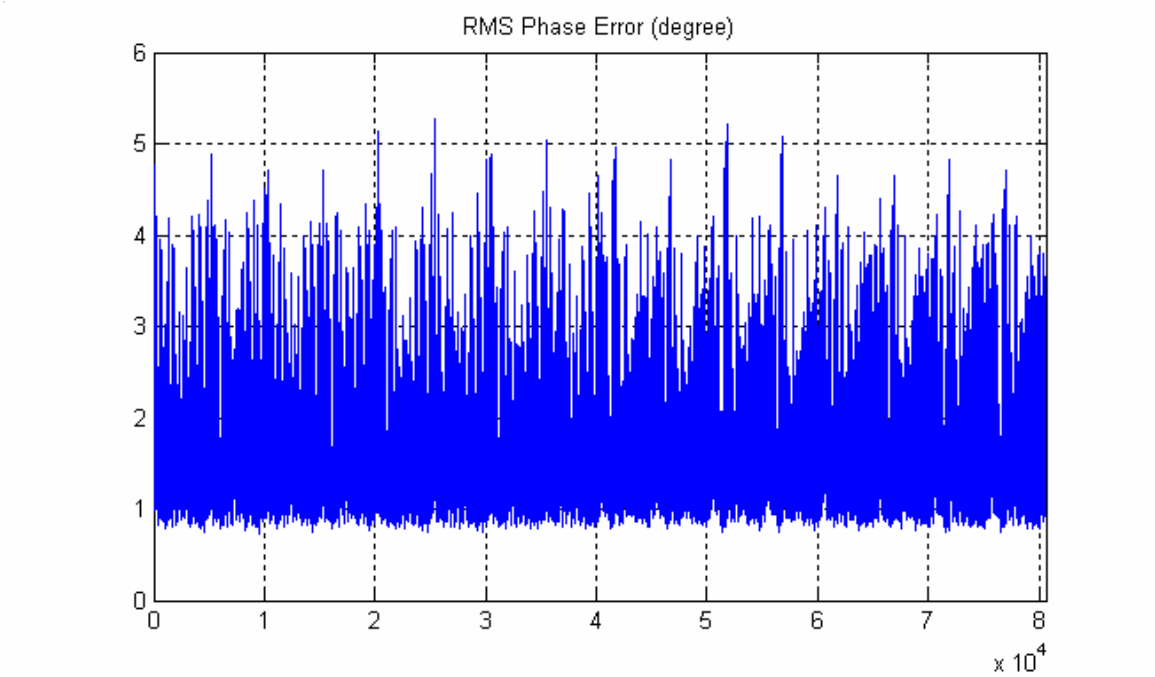

Figure 6.14 The variation of rms phase error of the phase shifter for all 80640 different bit arrangements

In the **Figure 6.15** and **Figure 6.16** the histograms of the phase error is given for two cases. In the first case, the bits are arranged such that the peak phase error is minimized. It is seen that the distribution for this case is more condense. However, looking at the histogram for the case where the bits are cascaded such that the rms phase error is minimized, it is observed that the peak error is larger but the phase error is more concentrated about zero, thus resulting in the lower rms error.

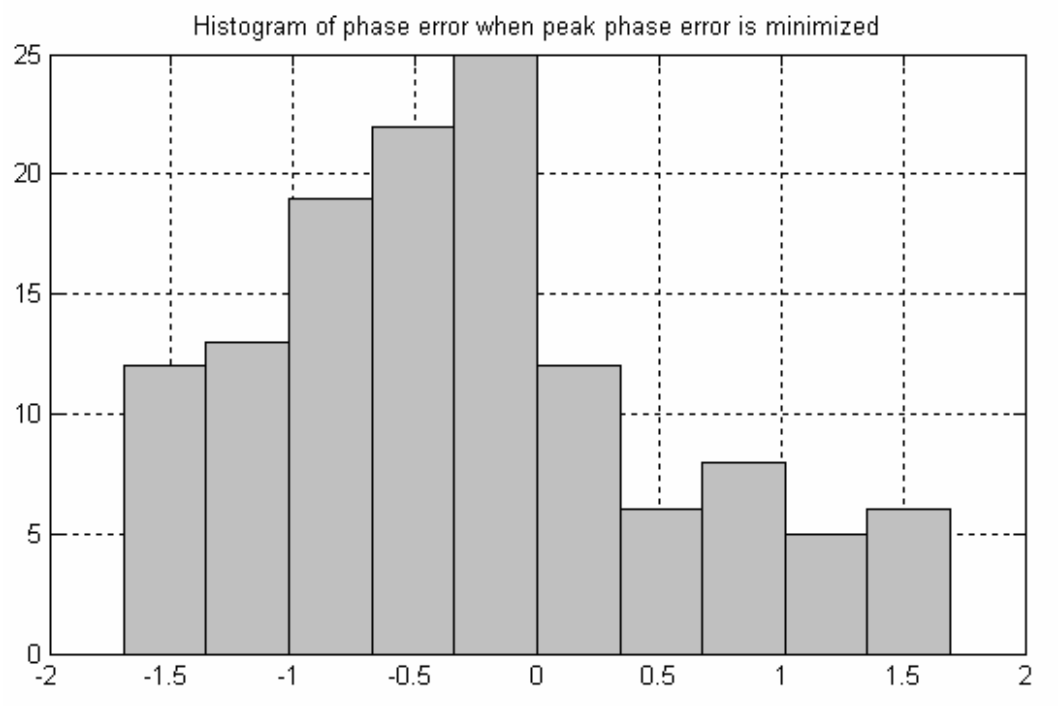

Figure 6.15 Histogram of phase error when the bits are arranged to minimize peak error

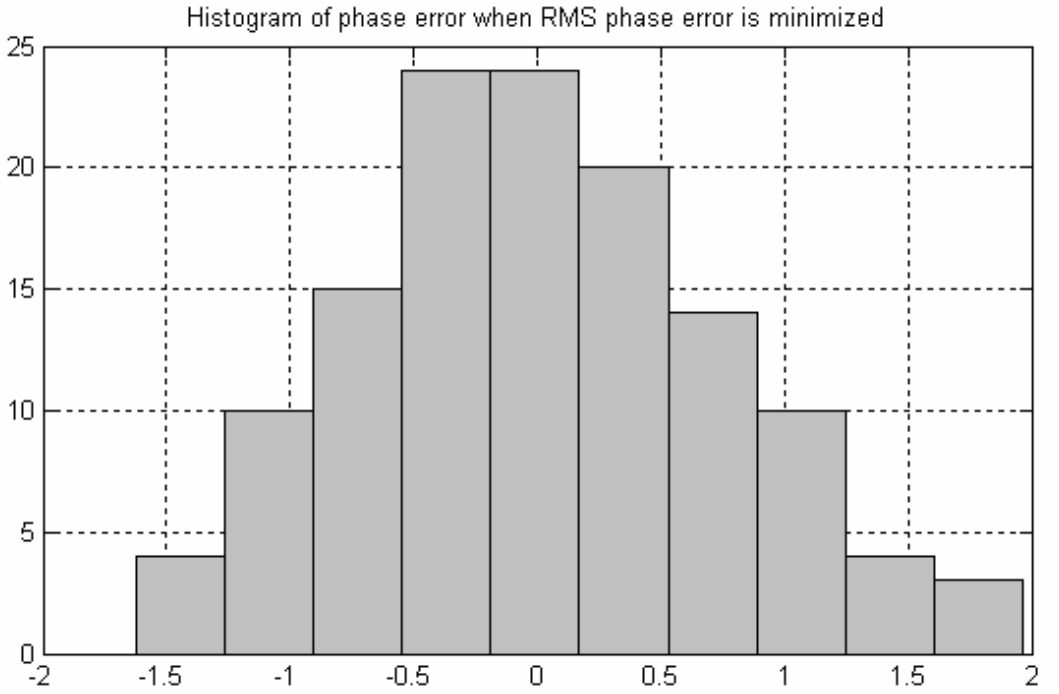

Figure 6.16 Histogram of phase error when the bits are arranged to minimize rms error

The difference between the maximum insertion loss and the minimum insertion loss of all 80640 arrangements is given in **Figure 6.17**. The minimum value of amplitude imbalance is 0.41 dB and it occurs for 4 – 2 – 5 – 6 – 7 – 1 – 3 with bits 7 and 5 flipped. It is determined that, without flipping the bits, the amplitude imbalance is 0.57 dB for the same sequence of bits. This shows that flipping is indeed effective on the amplitude imbalance. Further conclusion is that, examining **Table 6.1**, it is seen that the sum of amplitude imbalance values for each bit is 0.74 dB, but a large number of unlucky arrangements may well exceed this value. On the other hand, it is seen that it is possible to have lower values of amplitude imbalance as well. S_{11} and S_{22} for this arrangement are -14.4 and -11.7 dB respectively.

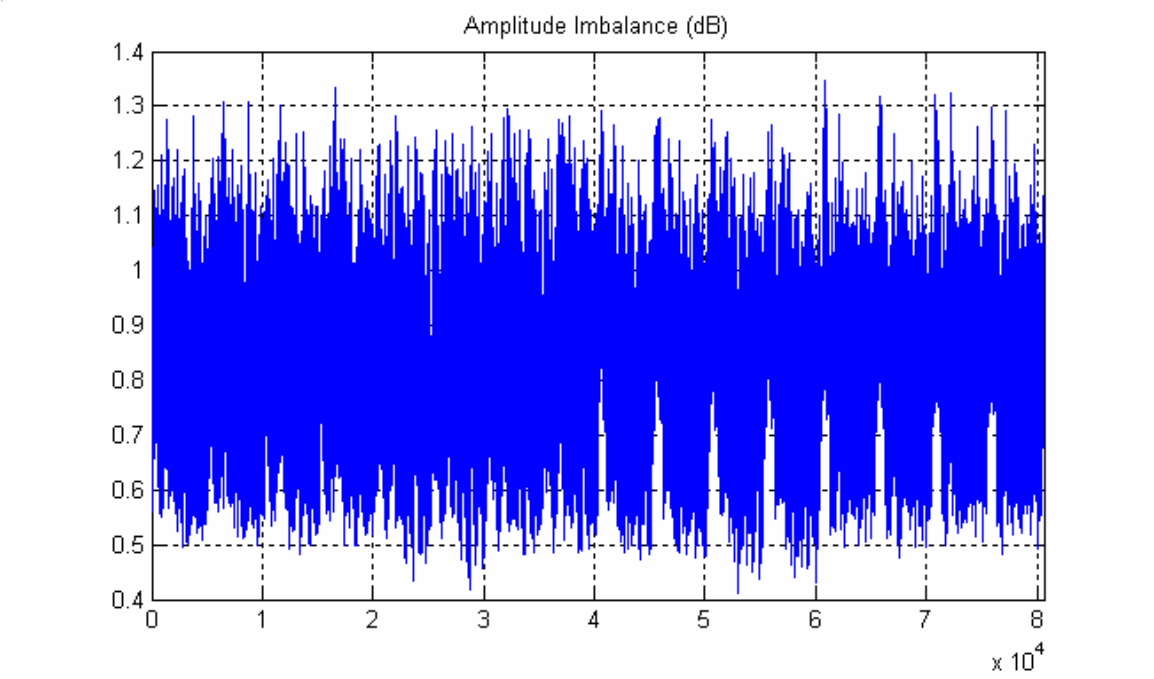

Figure 6.17 The variation of maximum amplitude imbalance of the phase shifter for all 80640 different bit arrangements

The average insertion loss is seen in **Figure 6.18**. The average is taken over 128 states for a particular arrangement. It can be deduced that the average insertion loss is relatively insensitive to bit arrangement and it is about 7.45 dB ± 0.1dB. A sub-optimum arrangement for insertion loss is therefore not sought. It should be noted that the average insertion losses of bits in **Table 6.1** add up to 7.43 dB.

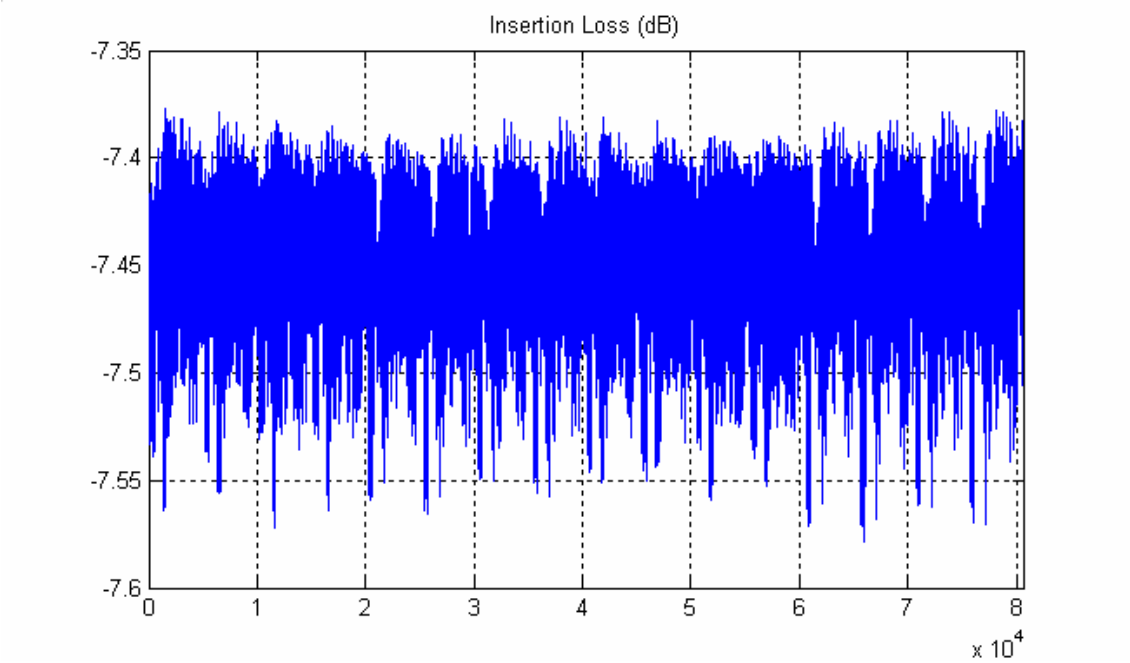

Figure 6.18 The variation of average loss of the phase shifter for all 80640 different bit arrangements.

Figure 6.19 and **Figure 6.20** respectively shows the variation of the return losses S_{11} and S_{22}. It is seen that they are both between -17 dB and -8 dB. If S11 is minimized (-16.9 dB) by selecting the bit order as 7 – 4 – 5 – 1 – 6 – 2 – 3 with bit 4, 5, 6, and 7 flipped, S22 is -10.6 dB. If S22 is minimized (-16.9 dB) by selecting the order of bits as 3 – 2 – 6 – 1 – 5 – 4 – 7 with none of the bits flipped, S11 is -10.7 dB. However if their sum is minimized by selecting the bit order as 3 – 4 – 5 – 6 – 2 – 7 – 1 with bit 6 flipped, S11 is -13.7 dB and S22 is -15.9 dB. The overall performance for this case will be given later.

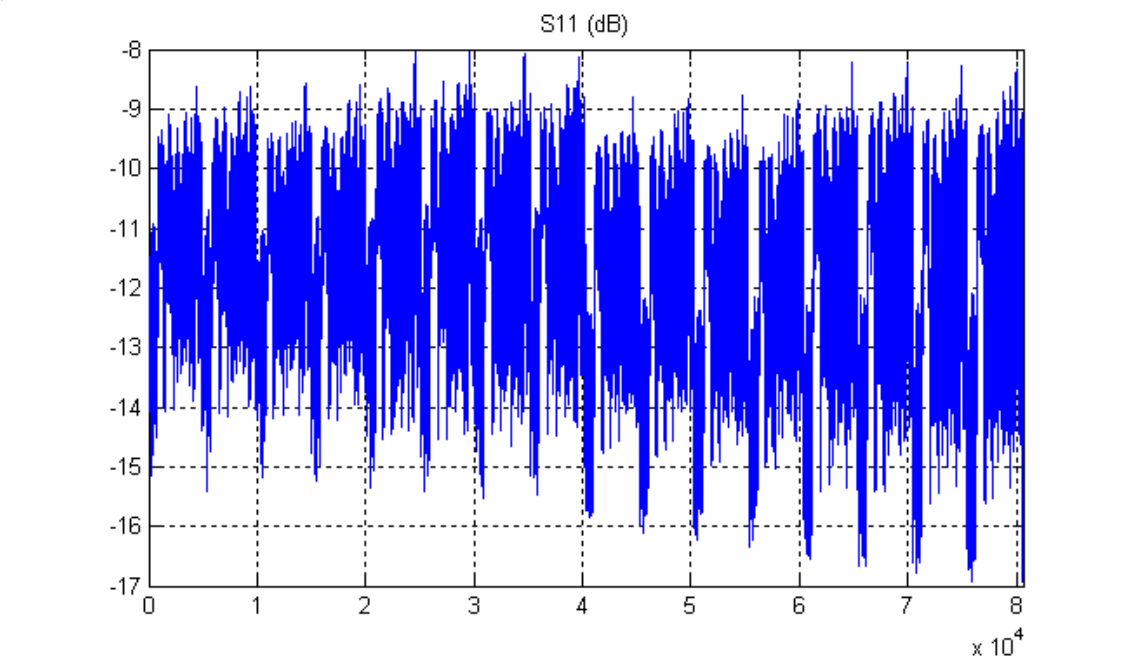

Figure 6.19 The variation of maximum S11 of the phase shifter for all 80640 different bit arrangements

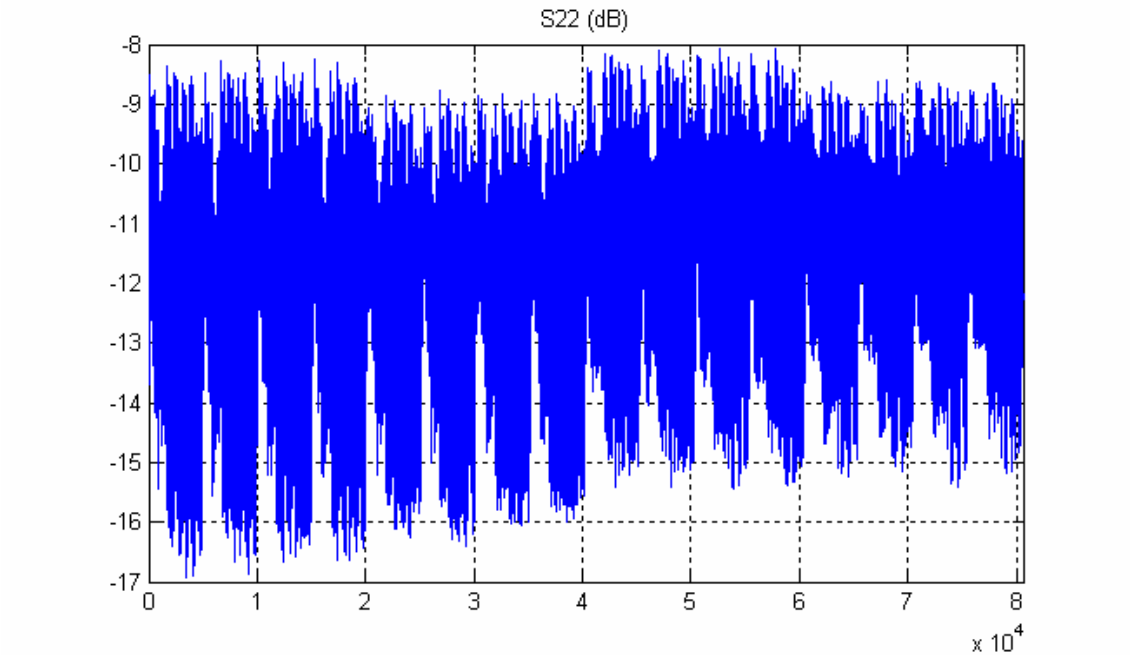

Figure 6.20 The variation of maximum S22 of the phase shifter for all 80640 different bit arrangements

6.3.2. ADS Results for Sub-optimum Arrangements

In this section, the ADS simulation results for the sub-optimum arrangements found with the help of MATLAB code will be presented. These sub-optimum arrangements are summarized in **Figure 6.21**.

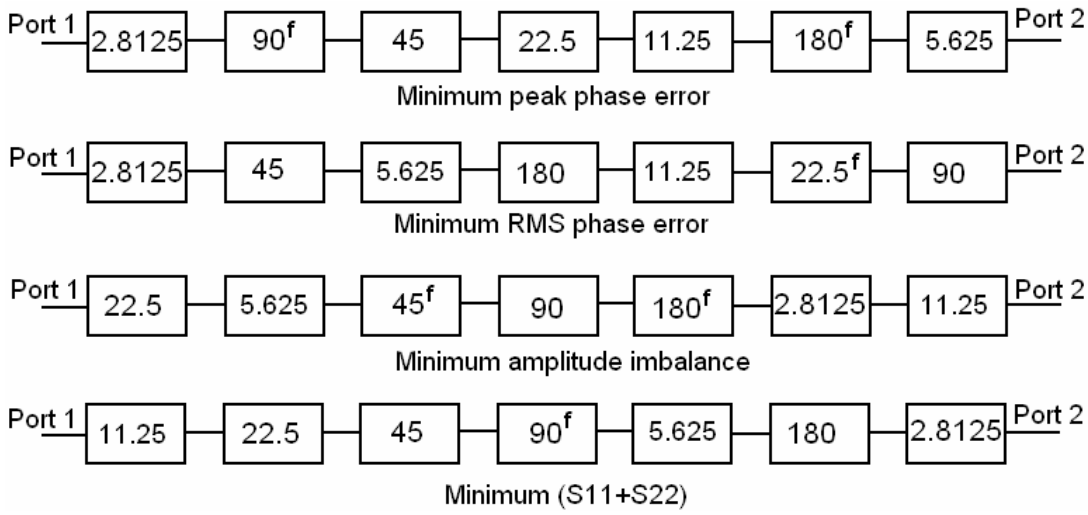

Figure 6.21 Summary of sub-optimum bit arrangements for the 7 bit phase shifter (f stands for flipping w.r.t the layout conventions in Chapter 5)

6.3.3. Arrangement 1: Minimum Peak Phase Error

With the arrangement to minimize peak phase error below results are obtained. The MATLAB program operates over the S parameters at 9.5 GHz, but the ADS simulation is over the full bandwidth of the phase shifter.

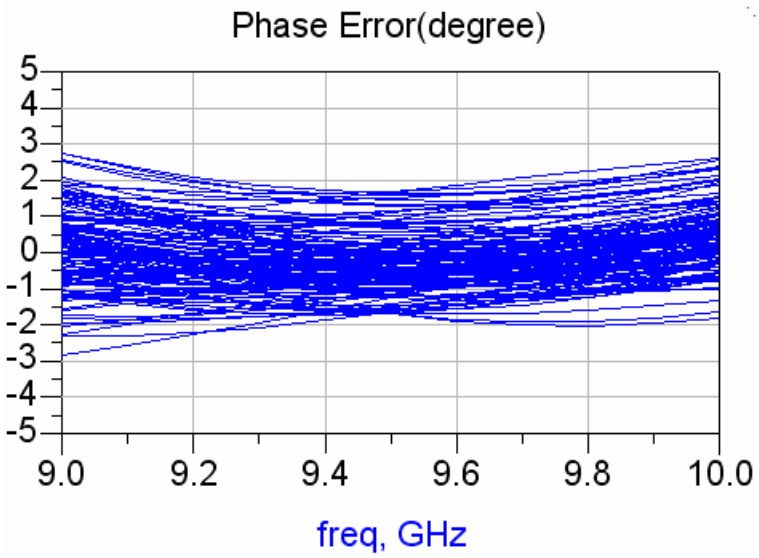

Figure 6.22 Phase error of the phase shifter when the bits are arranged so as to minimize the peak phase error

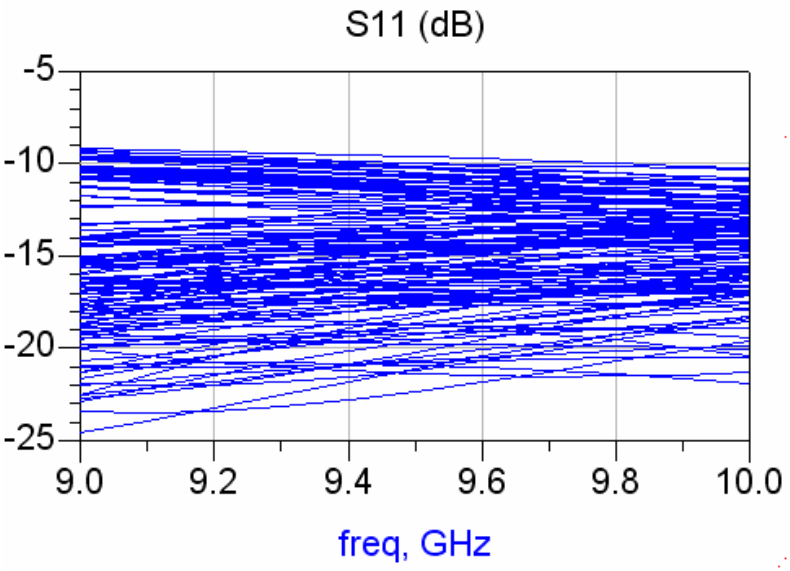

Figure 6.23 S_{11} of the phase shifter when the bits are arranged so as to minimize the peak phase error

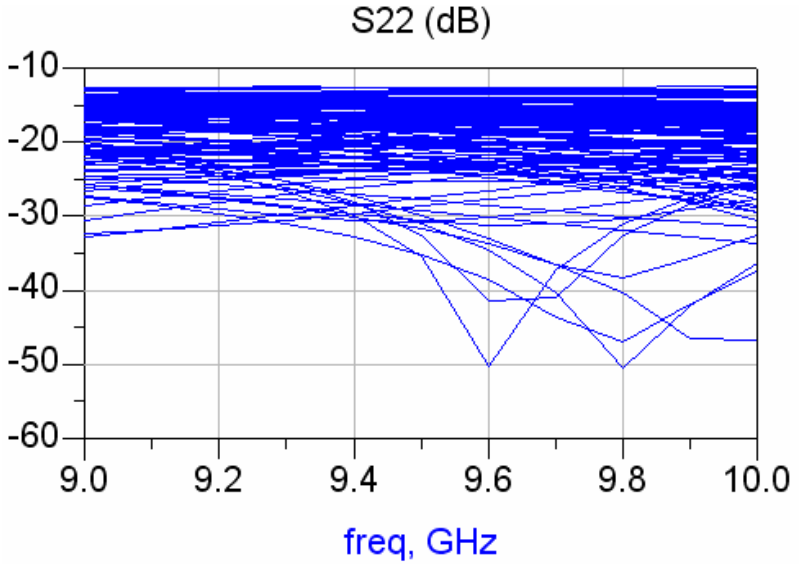

Figure 6.24 S_{22} of the phase shifter when the bits are arranged so as to minimize the peak phase error

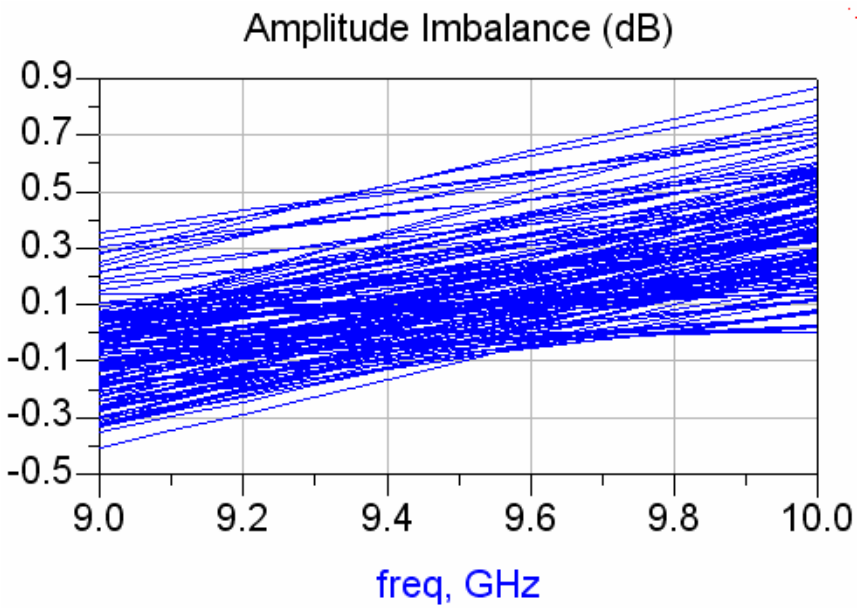

Figure 6.25 Amplitude imbalance of the phase shifter when the bits are arranged so as to minimize the peak phase error.

The summary of the performance for this bit arrangement is given in **Table 6.2**.

Table 6.2 Summary of performance when the bit arrangement is such that the peak phase error is minimum at 9.5 GHz

	Phase Error		Average Insertion Loss[3]	Amplitude Imbalance[4]	Worst S_{11}	Worst S_{22}
	Peak[1]	Rms[2]				
9 GHz	2.8º	1.13º	7.60 dB	< 0.41dB	-9.2 dB	-12.7 dB
9.5 GHz	1.7º	0.88º	7.52 dB	< 0.68 dB	-9.6 dB	-12.6 dB
10 GHz	2.6º	1.00º	7.48 dB	< 0.87 dB	-10.3 dB	-12.5 dB

[1] Peak phase error is the maximum phase error over all 128 states w.r.t the commanded phase shift.

[2] Rms phase error for a specific bit arrangement is computed as:

$$\varepsilon_{RMS} = \sqrt{\frac{\sum_{n=1}^{128} \left(\phi_{desired}(n) - \phi_{resultant}(n)\right)^2}{128}} \qquad (6\text{-}1)$$

[3] Average Insertion Loss is the average of the insertion losses of 128 states at a single frequency and it is found in MATLAB

[4] Amplitude imbalance is computed w.r.t the reference state. However, in the MATLAB code, it was the difference between the maximum insertion loss and the minimum insertion loss. In ADS results the reference amplitude for amplitude imbalance is always the value at 9.5 GHz. If, for each frequency, the reference is the insertion loss of the reference state at that frequency, the amplitude imbalance would appear lower.

6.3.3.1. Arrangement 2: Minimum Rms Phase Error

With the arrangement that minimizes rms phase error, below results are obtained.

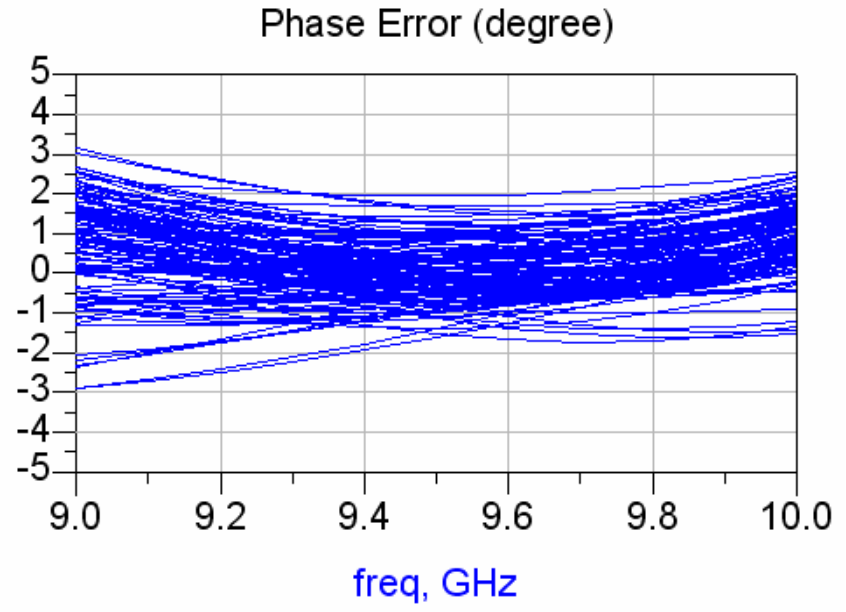

Figure 6.26 Phase error of the phase shifter when the bits are arranged so as to minimize the rms phase error

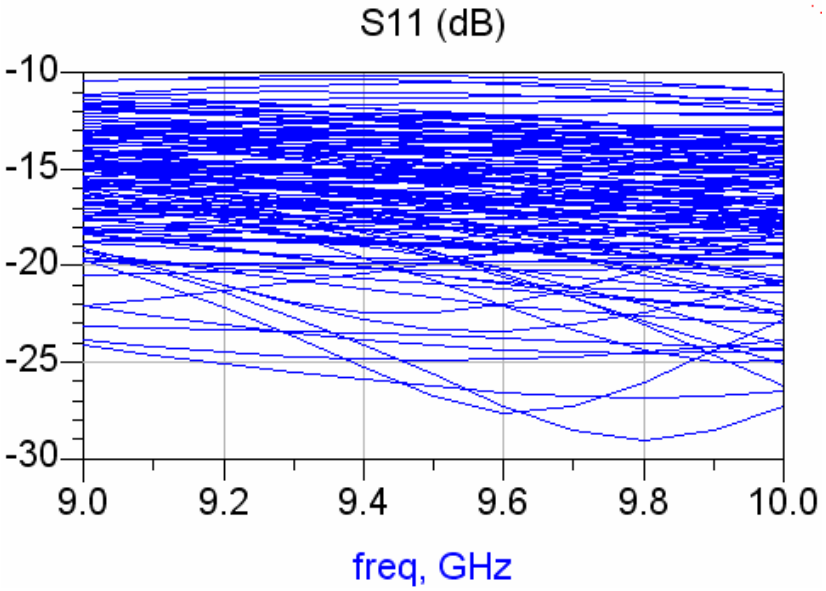

Figure 6.27 S_{11} of the phase shifter when the bits are arranged so as to minimize the rms phase error

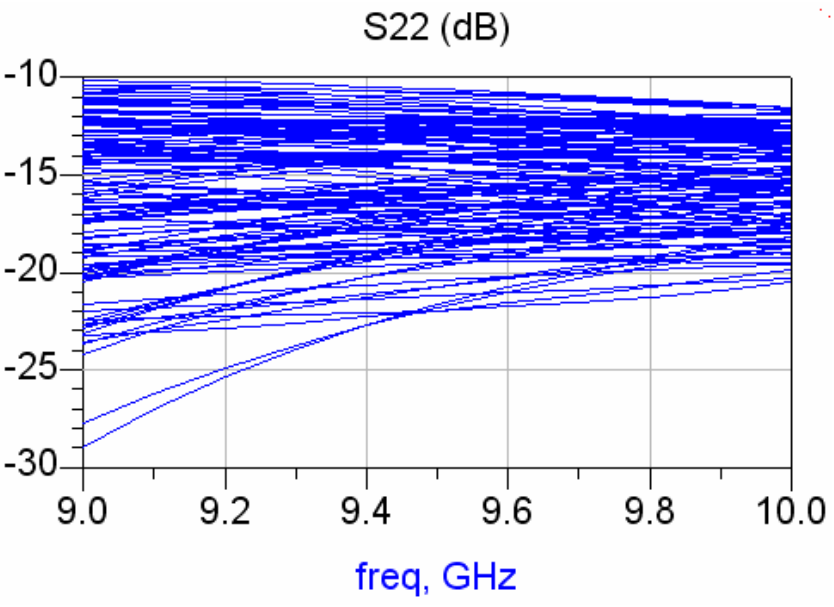

Figure 6.28 S_{22} of the phase shifter when the bits are arranged so as to minimize the rms phase error

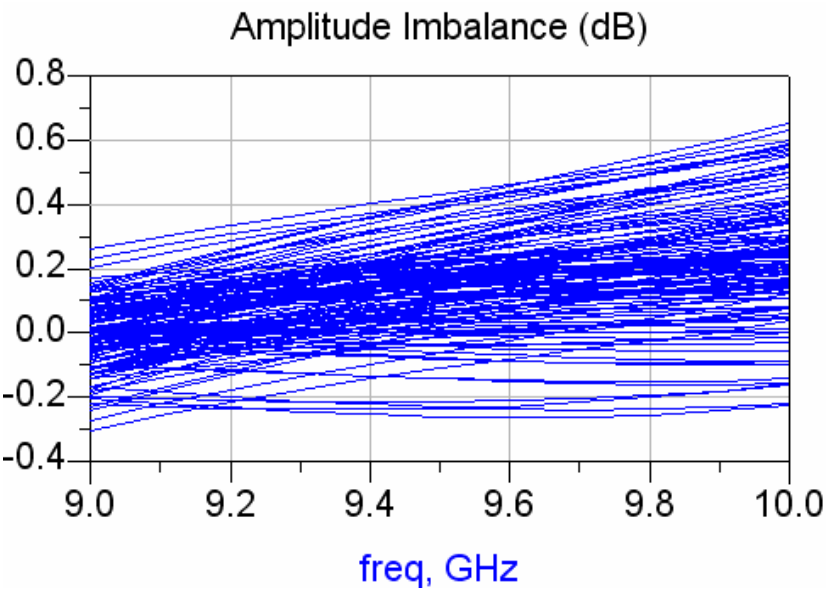

Figure 6.29 Amplitude imbalance of the phase shifter when the bits are arranged so as to minimize the rms phase error.

The summary of the performance for this bit arrangement is given in **Table 6.3**.

Table 6.3 Summary of performance when the bit arrangement is such that the rms phase error is minimum at 9.5 GHz

	Phase Error		Average Insertion Loss	Amplitude Imbalance	Worst S_{11}	Worst S_{22}
	Peak	Rms				
9 GHz	3.16º	1.46º	7.56 dB	< 0.31dB	-10.4 dB	-10.2 dB
9.5 GHz	1.96º	0.74º	7.48 dB	< 0.68 dB	-10.2 dB	-10.6 dB
10 GHz	2.53º	1.19º	7.44 dB	< 0.65 dB	-10.9 dB	-11.5 dB

6.3.3.2. Arrangement 3: Minimum Amplitude Imbalance

With the arrangement to minimize the amplitude imbalance, below results are obtained. Amplitude imbalance is minimum at 9.5 GHz as seen in **Figure 6.33**.

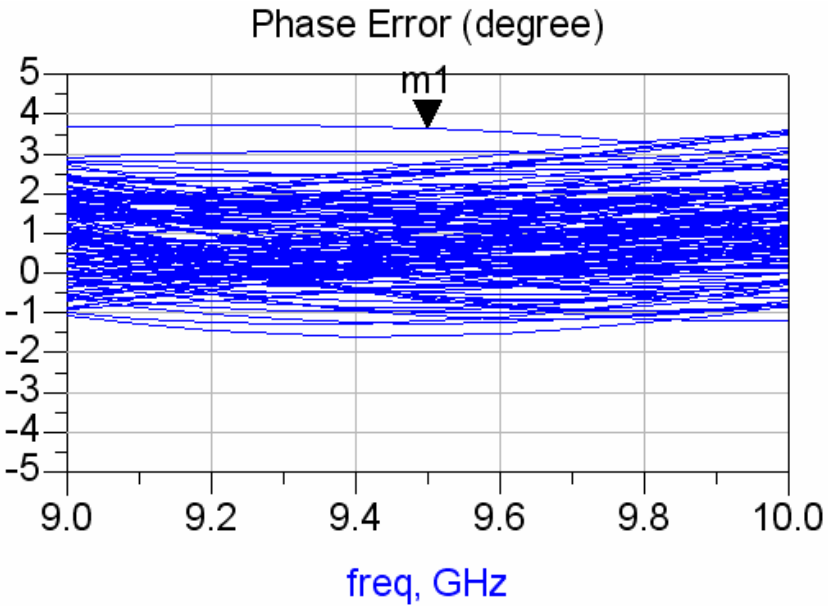

Figure 6.30 Phase error of the phase shifter when the bits are arranged so as to minimize the amplitude imbalance

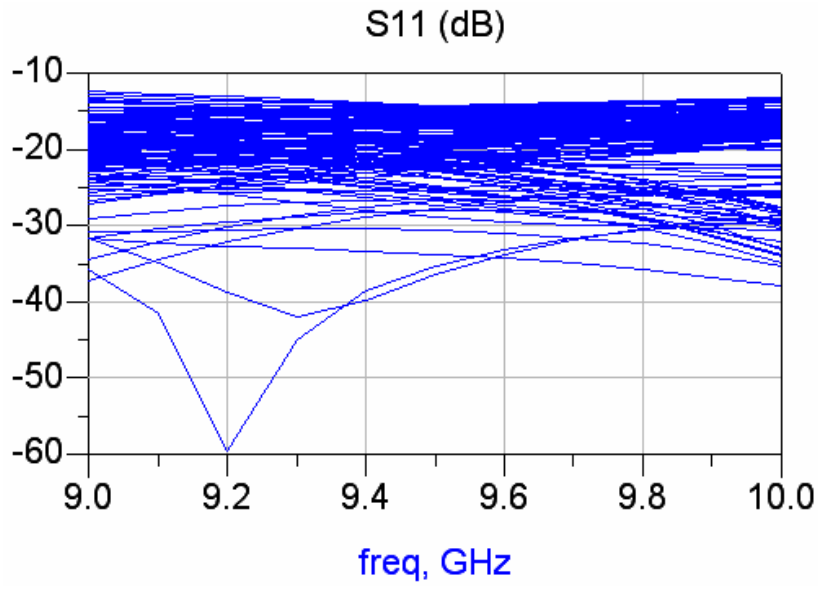

Figure 6.31 S_{11} of the phase shifter when the bits are arranged so as to minimize the amplitude imbalance

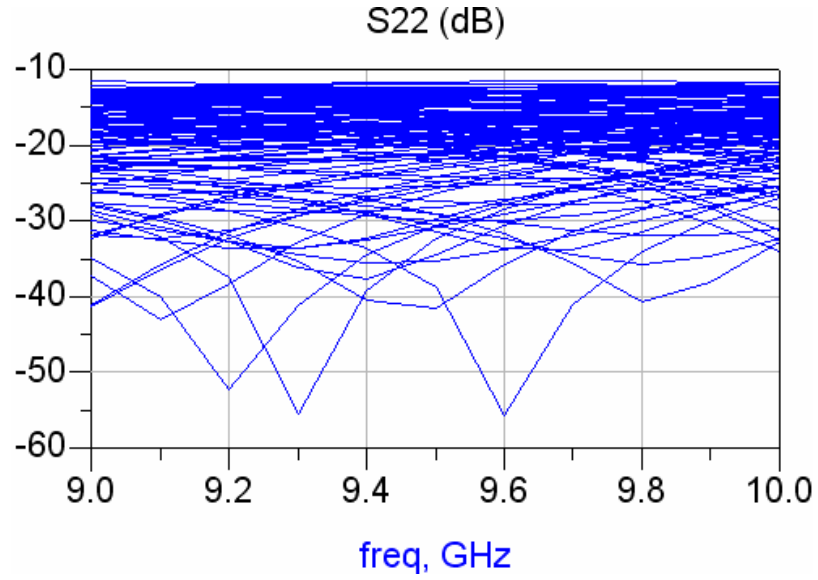

Figure 6.32 S_{22} of the phase shifter when the bits are arranged so as to minimize the amplitude imbalance

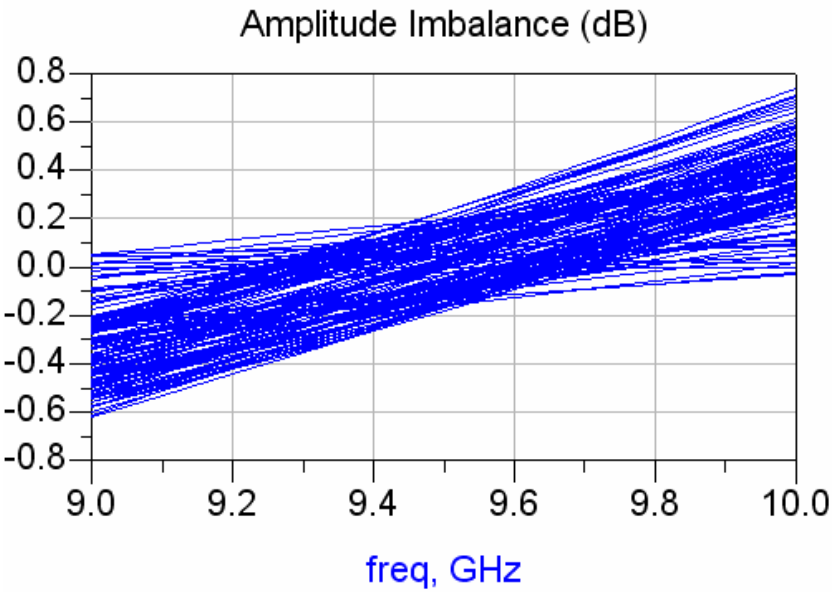

Figure 6.33 Amplitude imbalance of the phase shifter when the bits are arranged so as to minimize the amplitude imbalance

The summary of the performance for this bit arrangement is given in **Table 6.4**.

Table 6.4 Summary of performance when the bit arrangement is such that the amplitude imbalance minimum at 9.5 GHz

	Phase Error		Average Insertion Loss	Amplitude Imbalance	Worst S_{11}	Worst S_{22}
	Peak	Rms				
9 GHz	3.67º	1.40º	7.52 dB	< 0.62 dB	-12.5 dB	-11.5 dB
9.5 GHz	3.64º	1.29º	7.43 dB	< 0.23 dB	-14.4 dB	-11.7 dB
10 GHz	3.59º	1.59º	7.40 dB	< 0.74 dB	-13.3 dB	-11.8 dB

6.3.3.3. Arrangement 4: Minimum S11+S22

With the arrangement to minimize the sum of the return losses S_{11} and S_{22}, below results are obtained. As the return losses are optimized, other parameters are degraded in conformity with the expectations.

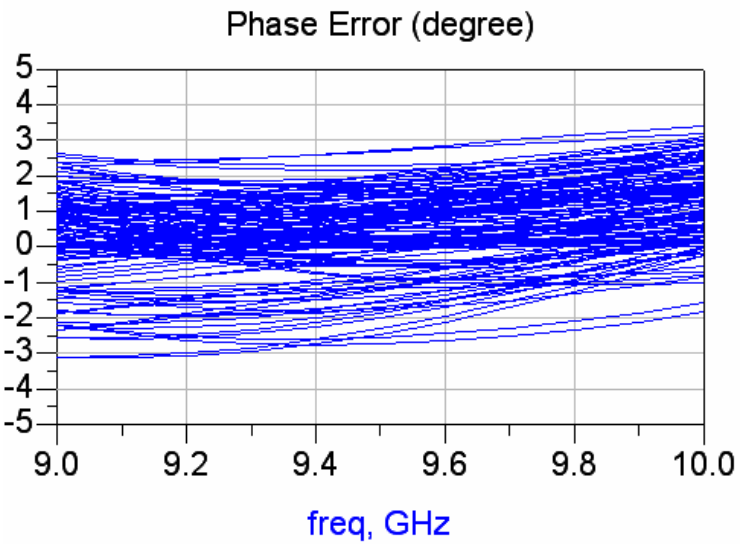

Figure 6.34 Phase error of the phase shifter when the bits are arranged so as to minimize the sum of S_{11} and S_{22}

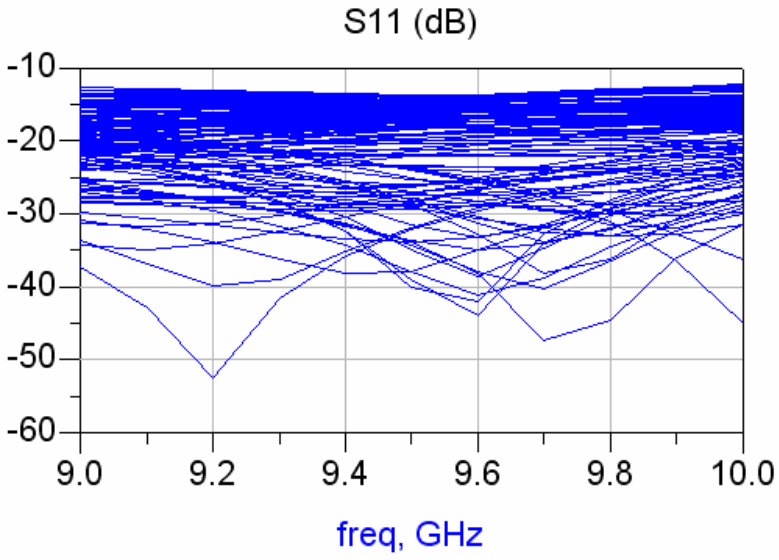

Figure 6.35 S_{11} of the phase shifter when the bits are arranged so as to minimize the sum of S_{11} and S_{22}

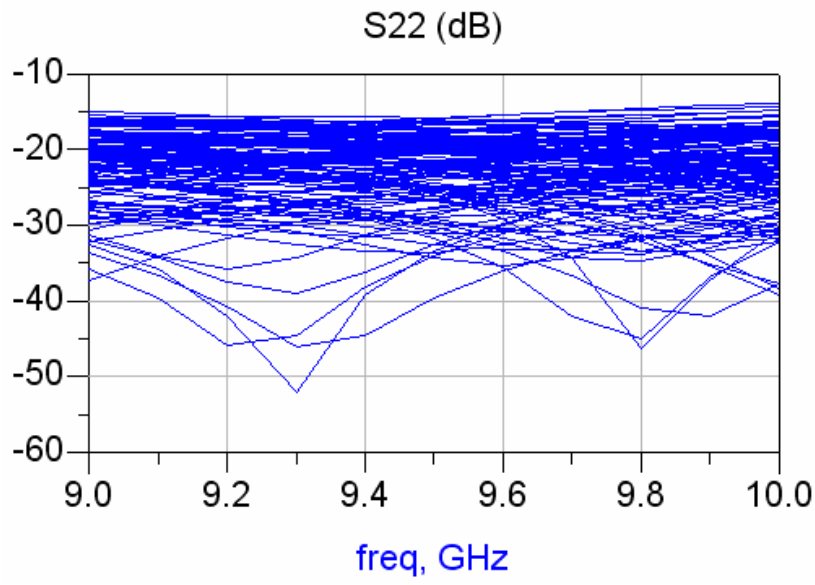

Figure 6.36 S_{22} of the phase shifter when the bits are arranged so as to minimize the sum of S_{11} and S_{22}

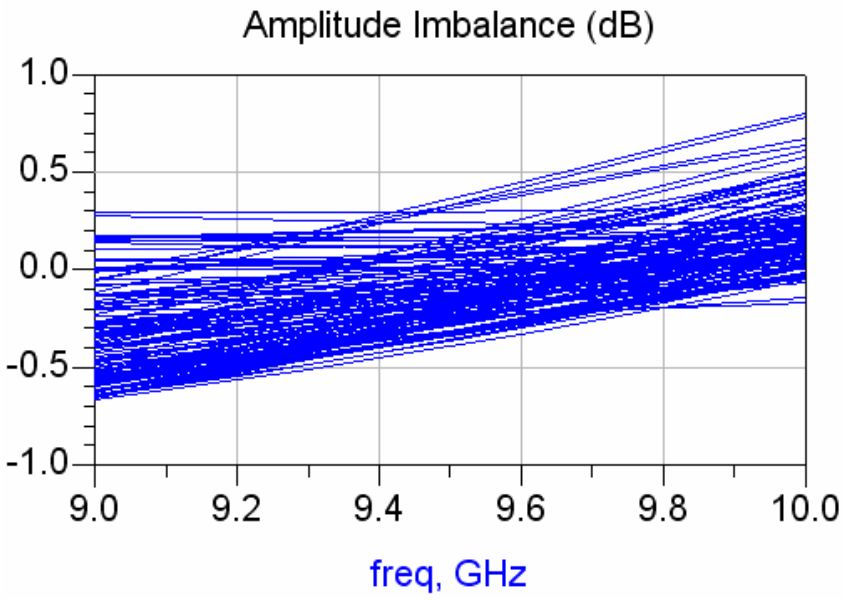

Figure 6.37 Amplitude imbalance of the phase shifter when the bits are arranged so as to minimize the sum of S_{11} and S_{22}

The summary of the performance for this bit arrangement is given in **Table 6.5**.

Table 6.5 Summary of performance when the bit arrangement is such that the sum of S_{11} and S_{22} is minimum at 9.5 GHz

	Phase Error		Average Insertion Loss	Amplitude Imbalance	Worst S_{11}	Worst S_{22}
	Peak	Rms				
9 GHz	3.10º	1.32º	7.48 dB	< 0.67 dB	-12.7 dB	-15.0 dB
9.5 GHz	2.75º	1.21º	7.40 dB	< 0.39 dB	-13.7 dB	-15.9 dB
10 GHz	3.39	1.63º	7.39	< 0.80 dB	-12.2 dB	-13.8 dB

6.4. Layout of the Minimum Rms Error Arrangement

It is seen that the performance of the arrangement for minimum rms error is a fair one in terms of the amplitude imbalance and return loss offered. The rms phase error is already the best among all possible arrangements. This arrangement was investigated for floating source or drain situations and it was seen that no problem exists in that sense. **Figure 6.38** can be referred for the evaluation of the phase shifter with regard to existence of necessary DC paths. The least significant three bits have shunt transistors connected directly to ground and therefore do not suffer from floating terminals by any means. The 45º bit has a series transistor but it is grounded in DC with the DC Path 1 in below figure. It also gets ground connection by the choking inductors in 180º bit. As for the 22.5 º bit, the series transistor is connected to the ground through the DC path 2. Same DC path connects the transistors that are in series with the low pass section in the 90º bit.

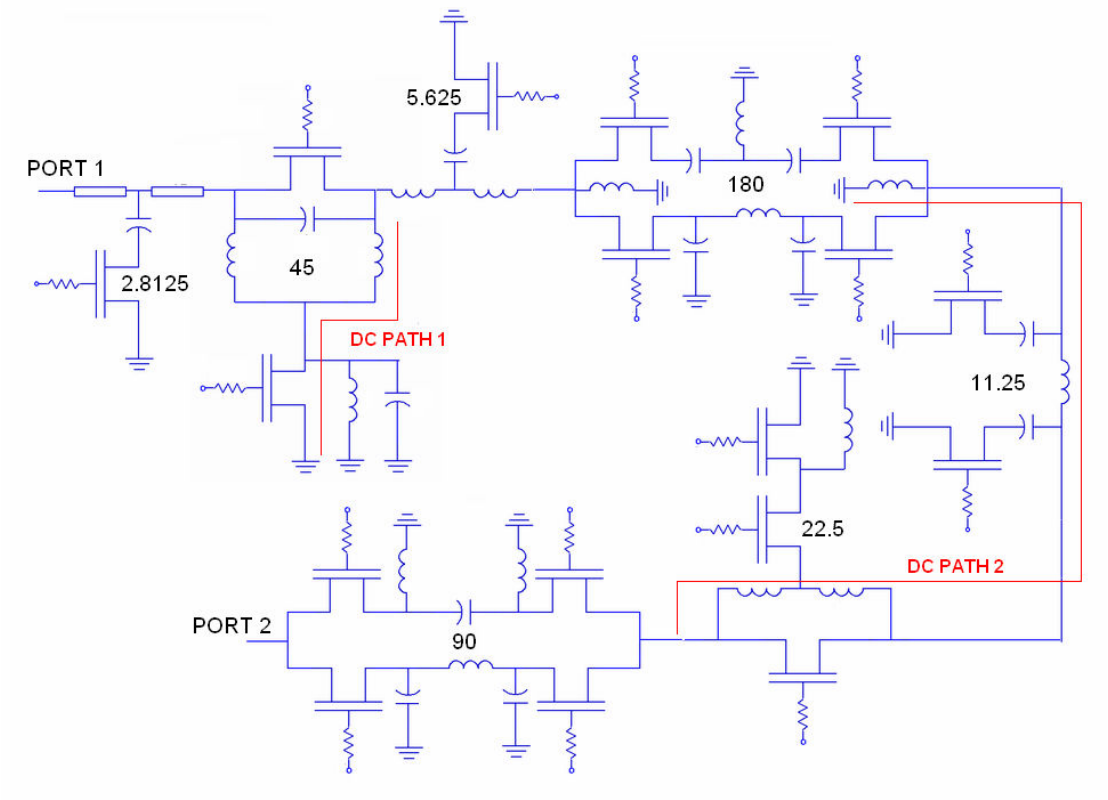

Figure 6.38 Schematic of the 7 bit phase shifter demonstrating critical DC paths

In **Figure 6.39** the layout of the phase shifter is presented. The layout consists of CPW pads for on wafer measurement and control pads. The chip size is 3630 μm by 1350 μm.

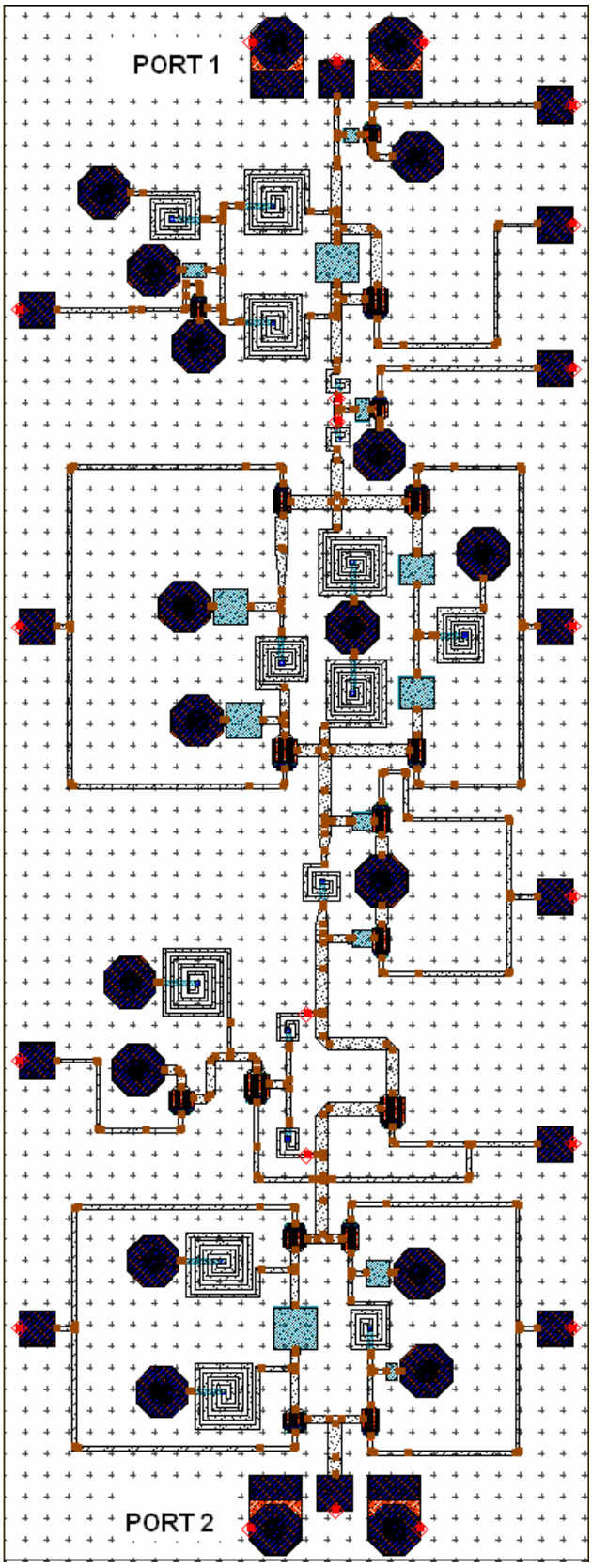

Figure 6.39 Final layout of the phase shifter with minimum rms phase error

CHAPTER 7

CONCLUSIONS

In this study, phase shifter topologies were designed with design kits of two different MMIC foundries. The WIN Foundry offers attractively low prices but it has limited support for designers. On the other hand, OMMIC Foundry's prices are almost one order of magnitude higher than that of WIN's but they provide outstandingly helpful and crucial design and layout ease in their design kit. It is understood that, having a proper design kit and a mature process at hand is critical from the designer's point of view. With OMMIC Foundry components, seven bits of a phase shifter with 360 degree coverage have been designed. Various topologies available in the literature have been examined for each bit and most proper ones have been selected. Apart from the 180º and 90º bits, all bits have low insertion loss values. The bits are designed in such a fashion that they individually satisfy acceptable performance in terms of critical parameters of a phase shifter network. All but 90º bit have the capability of being interfaced with any other bit from any port, thanks to the low return loss values at both ports at both states. All possible ordering of bits have been tested in order to minimize phase error, amplitude imbalance or return loss of the overall circuit. With the arrangement that minimizes rms phase error; 1.5 degree rms, 3.2 degree peak phase error is obtained between 9 and 10 GHz. The average insertion loss of this topology is 7.6 dB with a maximum amplitude imbalance of 0.7 dB. The return loss at both ports at any state is better than -10.2 dB in 9-10 GHz band.

While designing the phase shifter bits, one must be careful on some features of the bit network. First the phase bit must yield the desired phase shift sufficiently flat over a bandwidth. Second, there must be little amplitude difference between two states of the phase bit. Third, the return loss from both ports should be as low as possible at both states of the phase bit, because this is critical while cascading the bits. Finally, the insertion loss of the phase shifter must be kept low. All these conditions call for selection of the proper topology for a particular phase bit. It is best to select the

topologies, wherever possible, where transistor's on and off state equivalent circuits act as the elements of phase shifting networks, since these topologies generally impose lower insertion loss and offer wider bandwidth than switched network type topologies. However, these topologies have proved successful in the designs of intermediate bits such as 45º and 22.5º as proposed in the literature. As for the small bits, usage of shunt transistor topologies is appropriate due to absence of transistors in the series path and thus too much loss. For the most significant two bits, although there are again embedded filter type and therefore wideband topologies available in the literature, these ones achieve wideband performance by allowing large insertion loss (3-4 dB per bit). Another disadvantage of these topologies is that they include quite a lot of active and passive elements, which complicates the layout.

As for the integration of the individual bits of a phase shifter, there are some points worth mentioning. First, although none of the individual return losses of phase bits exceed -15 dB at both states at each port, the return loss of the overall phase shifter might be as bad as -8 dB (see **Figure 6.19** and **Figure 6.20**) if the bits are arranged haphazardly. Moreover, the amplitude imbalance and phase error could be up to 1.4 dB and 8º, if again no care is taken during arrangement of the bits. Next, it is seen that the average insertion of the phase shifter is almost insensitive to order of the bits.

The studies for finding the sub-optimum bit arrangements executed in this study could be extended in different ways. In the MATLAB code written, all arrangements were simulated only at center frequency, but it is also possible that the whole band behavior is simulated and checked for most appropriate arrangements. It was felt that finding the optimum arrangement by working on the center frequency would also be optimum in the whole band, but from **Table 6.2** it is apparent that the peak error is minimal at center frequency but it starts to spread as departed from the center frequency. Thus it is better to operate over the entire bandwidth while finding the desired arrangement, but this will bring computation complexity.

Another extension of the generated MATLAB code might be finding the global optimum for bit arrangement by using the results of batch simulation. It is only a matter of finding the proper weighting coefficients for each performance parameter

such as phase error, amplitude imbalance and return losses from both ports (As insertion loss is not affected significantly from the bit order, it may not be included in the weighted parameters). The weighted vectors will be summed and the sum will be used to find the best configuration. Perhaps the weights will be dependent on the application where some particular shortcoming could be compensated by other components in the system, but some parameter is more critical. For instance, amplitude imbalance problem may be overcome by the existence of variable attenuators in series with the phase shifter and in that case, the phase shifter might have the opportunity to have optimum phase error by allowing a large amplitude imbalance. Or the phase error might be sacrificed considering that the phase commands can be optimized to have less error, that is the desired phase shift may be better approximated by advancing or retarding the commanded phase. However both approaches necessitate some intelligence in the related system.

Although it did not catch up to the end of this work, this phase shifter will be manufactured by OMMIC Foundry, which is indeed a future work from the viewpoint of this thesis. This is not only necessary to have a real chip, but it is also a necessary step to continue the cyclic work: design – produce – measure – and review design.

REFERENCES

[1] Burns R., W., Holden, R. L. and Tang, R., "Low Cost Design Techniques for Semiconductor Phase Shifters", IEEE Transactions On Microwave Theory And Techniques, Vol. MTT-22, No. 6, pp 675- 688, June 1974.

[2] Garver R., V., "Broad-band Diode Phase Shifters," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-20, pp. 314–323, May 1972.

[3] Rizzi, P. A. "A Lumped Element Diode Phase Shifter", Microwave Symposium Digest, GMTT International, Vol 72, Issue 1, pp. 49-51, May 1972.

[4] Coats, R., Klein, J., Pritchett, S., D., Zimmermann, D., "A Low Loss Monolithic Five Bit PIN Diode Phase Shifter", IEEE MTT-S International Microwave Symposium Digest, , pp. 915-918, Vol. 2, May 1990.

[5] Maruhashi, K., Mizutani, H., Ohata, K., "A Ka-Band 4-Bit Monolithic Phase Shifter Using Unresonated FET Switches", Microwave Symposium Digest, 1998 IEEE MTT-S International, Vol. 1. June 1998.

[6] Andricos, C., Bahl, I. J., Griffin, E. L., "C-Band 6-Bit GaAs Monolithic Phase Shifter", IEEE Transactions on Microwave Theory and Techniques (ISSN 0018-9480), Vol. MTT-33, pp. 1591-1596, December 1985.

[7] Dai, Y., S., Chen, X., J., "A Novel Multi-Octave Five-Bit Monolithic Phase Shifter", Microwave and Millimeter Wave Technology, 2nd International Conference on ICMMT, pp 215-218, 2000.

[8] Ayasli, Y., Miller, S., W., Mozzi, R., and Hanes, L., K., "Wide Band Monolithic Phase Shifter," IEEE Trans. Electron Devices, Vol. ED-3 1, pp. 1943-1947, Dec. 1984.

[9] Purnell, K., Katz, A., “A Novel Phase Shifter Using AlGaAs MESFET in Passive Configuration”, IEEE MTT-S International Microwave Symposium Digest, Vol. 2, pp. 1197-1200, 1996.

[10] Takasu, H., Kamihashi, S., Tokuda, H., Tanaka, M., and Hase, Y., “K-Band GaAs MMIC Phase Shifter Using Self-Switched Filter Circuits” , IEEE International Symposium on Phased Array Systems and Technology, pp. 41-43, 1996.

[11] Hancock, T., Rebeiz, G., M.,“A 12-GHz SiGe Phase Shifter With Integrated LNA”, IEEE Transactions On Microwave Theory And Techniques, Vol. 53, No. 3, March 2005.

[12] H. Hayashi and M. Muraguchi, “An MMIC Active Phase Shifter Using a Variable Resonant Circuit”, IEEE Trans. Microwave Theory Tech., Vol. 47, pp. 2021–2026, Oct. 1999.

[13] Maruhashi, K., Mizutani H., Ohata, K., “Design and Performance of a Ka-Band Monolithic Phase Shifter Utilizing Nonresonant FET Switches”, IEEE Transactions On Microwave Theory And Techniques, Vol. 48, No. 8, August 2000.

[14] Khalil, A., I., Mahfoudi, M., Traut, F., Shifrin, M., Chavez, J., “A X-Band 4-Bit mHEMT Phase Shifter”, Compound Semiconductor Integrated Circuit Symposium, 2005.

[15] Lee, H., D., Kang, D., W., Kim, C., H., Hong, S., “A Ku Band MOSFET Phase Shifter MMIC”, IEEE MTT-S International Microwave Symposium Digest, Vol.1, pp. 191- 194. June 2004.

[16] Chen, P., Y., Huang, T., W., Wang, H., Wanh Y., C., “K-Band HBT and HEMT Monolithic Active Phase Shifters Using Vector Sum Method”, IEEE Transactions On Microwave Theory And Techniques, Vol 52, Issue 5, pp. 1414- 1424, May 2004.

[17] Ya, S., Jiyi, C., Xiaojian, C., Hui, L., and Jinting, L., “A Compact L-Band 4 Bit MMIC Phase Shifter”, International Conference on Microwave and Millimeter Wave Technology Proceedings, pp. 242-244, 1998.

[18] F Campbell and S. A. Brown, “A Compact 5-Bit Phase Shifter MMIC for K-Band Satellite Communications Systems,” 2000 IEEE MTT-S International Microwave Symposium Digest, Vol. 1, pp. 217-220, June 2000.

[19] Ya, S., Jiyi, C., Tangsheng, C., Xiaojian, C., Jinting, L., “A X-Band Five Bit MMIC Phase Shifter”, 2nd International Conference on Microwave and Millimeter Wave Technology, pp. 200-202, 2000.

[20] D. C. Boire, G. St. Onge, C. Barratt, G. B. Norris, and A. Moysenko, “4: 1 Bandwidth Digital Five-Bit MMIC Phase Shifters,” in IEEE Microwave and MM-Wave Monolithic Circuits Symposium. pp. 69-73, 1989.

[21] Schindler M., J., Miller, M., E., “A Three Bit K/Ka Band MMIC Phase Shifter”, Microwave and Milimeter Wave Monolithic Circuits Symposium, Digest of Papers, pp. 95-98, 1988.

[22] F. Ellinger, R. Vogt, and W. Bächtold, “Compact Reflective Type Phase Shifter MMIC for C-Band Using a Lumped Element Coupler,” IEEE Trans. Microwave Theory Tech., Vol. 49, pp. 913–917, May 2001.

[23] D. Adler and R. Popovich, “Broadband Switched-Bit Phase Shifter Using All-Pass Networks,” 1991 IEEE MTT-S Int. Microwave Symp. Dig., Vol. 1, pp. 265-268, June 1991.

[24] Zarei, H., Ecker, A., Park, J., and Alstot, D., J., “A Full-Range All-pass Variable Phase Shifter for Multiple Antenna Receivers”, IEEE International Symposium on Circuits and Systems, pp. 2100-2103, May 2005.

[25] D. Viveiros Jr., D. Consonni, and A. K. Jastrzebski, “A Tunable All-Pass MMIC Active Phase Shifter,” IEEE Transactions on Microwave Theory and Techniques., Vol. 50, no 8, pp. 1885–1889, Aug. 2002.

[26] Skrivervik, A., K., and Carrier, J., P., "Composite Right/Left Handed Transmission Line Metamaterial Phase Shifters (MPS) in MMIC Technology", IEEE Transactions on Microwave Theory and Techniques, Vol. 54, Issue 4, Part 1, pp 1582-1589, June 2006.

[27] Kholodnyak, D., Serebryakova, E., Vendik, D., Vendik, O., "Broadband Digital Phase Shifter Based on Switchable Right Handed and Left Handed Transmission Line Sections", IEEE Microwave and Wireless Components Letters, Vol. 16, Issue 5, pp. 258-260, May 2006.

[28] S. K. Koul and B. Bhat, "Microwave and Millimeter Wave Phase Shifters", Volume II, Boston, MA: Artech House, 1991.

[29] Serraiocco, J., L., "Compact Phase Shifter Design Using Barium Strontium Titanate Thin Film Varactors", A master thesis submitted to the Department of Electrical and Computer Engineering of University of California at Santa Barbara, September 2003.

[30] Mazumder, S., R., Isham, C., M., "Performance of a 6 to 18 GHz Frequency Translator Utilizing GaAs MMIC 5-Bit Digital Phase Shifter", Microwave and Millimeter-Wave Monolithic Circuits Symposium - Digest of Papers, pp. 141-144, May 1995.

[31] Andricos, C., Bahl, I., J., Griffin, E., L., "C-Band 6-Bit GaAs Monolithic Phase Shifter", Microwave and Millimeter-Wave Monolithic Circuits, Vol. 85, Issue 1, pp.8-9, June 1985.

[32] White J., F., "Diode Phase Shifters for Array Antennas", EEE Transactions on Microwave Theory and Techniques, Vol. 22, Issue 6, pp. 658 – 674, June 1974.

[33] Golio, J., M., "Microwave MESFETs and HEMTs" Artech House, Boston – London, 1991.

[34] Robertson, I., D., Lucyszyn, S., “RFIC and MMIC Design and Technology”, IEE Circuits Devices and Systems Series 13, London, 2001.

[35] Altay, M., “Comparison and Evaluation of Various MESFET Models”, A master thesis submitted to the Department of Electrical and Electronics Engineering of Middle East Technical University, March 2005.