

X-BAND RF SWITCH IMPLEMENTATION IN SUBSTRATE INTEGRATED  
WAVEGUIDE

A THESIS SUBMITTED TO  
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES  
OF  
MIDDLE EAST TECHNICAL UNIVERSITY

BY

TUNCAY ERDÖL

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS  
FOR  
THE DEGREE OF DOCTOR OF PHILOSOPHY  
IN  
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2012

Approval of the thesis:

**X-BAND RF SWITCH IMPLEMENTATION IN SUBSTRATE  
INTEGRATED WAVEGUIDE**

submitted by **TUNCAY ERDÖL** in partial fulfillment of the requirements for  
the degree of **Doctor of Philosophy in Electrical and Electronics  
Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan ÖZGEN \_\_\_\_\_  
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İsmet ERKMEN \_\_\_\_\_  
Head of Department, **Electrical and Electronics Eng.**

Assoc. Prof. Dr. Şimşek DEMİR \_\_\_\_\_  
Supervisor, **Electrical and Electronics Eng. Dept., METU**

Prof. Dr. Altuncan HIZAL \_\_\_\_\_  
Co-Supervisor, **Electrical and Electronics E. Dpt., METU**

**Examining Committee Members :**

Prof. Dr. Sencer KOÇ \_\_\_\_\_  
Electrical and Electronics Engineering Dept., METU

Assoc. Prof. Dr. Şimşek DEMİR \_\_\_\_\_  
Electrical and Electronics Engineering Dept., METU

Assoc. Prof. Dr. Lale ALATAN \_\_\_\_\_  
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Nevzat YILDIRIM \_\_\_\_\_  
Electrical and Electronics Engineering Dept., METU

Assoc. Prof. Dr. Vakur B. ERTÜRK \_\_\_\_\_  
Electrical and Electronics Eng. Dept., Bilkent University

Date: 12.09.2012

**I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.**

Name, Last name : Tuncay ERDÖL  
Signature :

# **ABSTRACT**

## **X-BAND RF SWITCH IMPLEMENTATION IN SUBSTRATE INTEGRATED WAVEGUIDE**

ERDÖL, Tuncay

Ph.D., Department of Electrical and Electronics Engineering

Supervisor: Assoc. Prof. Dr. Şimşek DEMİR

September 2012, 92 pages

An RF switch in substrate integrated waveguide (SIW) technology for X-band is designed and demonstrated. Design is based on embedding shunt pin diodes of the switch in an evanescent mode waveguide filter. At reverse bias, pin diodes formed a part of filter's capacitances. Thus switch also functions as a filter when it is in "on" state. At forward bias of diodes, capacitances of the filter are short circuited to obtain a good isolation. The same circuit structure is used to design a tunable filter and an RF power limiter which also functions as a filter. Several RF functions usually used in RF frontends (power limiting, filtering, switching) are combined in a single circuit which helps miniaturization of the frontend. The circuit can be produced with standard PCB and chip&wire technology. The circuits developed have comparable performances with microstrip counterparts and they are advantageous to use in microwave systems using SIW as the basic transmission medium and need filtering functionality.

Keywords: Substrate Integrated Waveguide (SIW), RF Switch, RF Power Limiter, Tunable Filter

# ÖZ

## TABAN MALZEMEYE BÜTÜNLEŞİK DALGA KILAVUZUNDA X-BANT RF ANAHTAR UYGULAMASI

ERDÖL, Tuncay

Doktora, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Doç. Dr. Şimşek DEMİR

Eylül 2012, 92 sayfa

Taban malzemeye bütünleşik dalga kılavuzu (TMBDK) yapısı içinde X-bant için bir RF anahtar tasarlanıp gösterilmiştir. Tasarım, anahtarın paralel pin diyotlarının sönümlenen dalga kılavuzu filtre tasarımında kullanılmasına dayanır. Ters beslemede bu diyotlar, filtrenin sığalarının bir kısmını oluşturur. Böylece anahtar açıkken filtre görevi de görür. Doğru beslemede ise filtrenin sığaları kısa devre edilerek iyi bir izolasyon elde edilir. Aynı devre yapısı ayarlanabilir filtre tasarımında ve filtre görevi de gören RF güç sınırlayıcı tasarımında kullanılmıştır. RF önkatlarda genellikle kullanılan birkaç RF fonksiyon (güç sınırlama, filtreleme, anahtarlama) tek bir devrede gerçekleştirilerek önkatin küçültülmesine katkı sağlanmıştır. Devre standart baskı devre ve hibrid üretim tekniğiyle üretilebilmektedir. Devreler mikroşerit eşlenikleriyle benzer performansa sahiptir ve temel iletim teknolojisi olarak TMBDK'yı kullanan ve filtreleme gereği olan sistemlerde kullanımı avantajlıdır.

Anahtar Kelimeler: taban malzemeye bütünleşik dalga kılavuzu (TMBDK), RF anahtar

To My Family

## ACKNOWLEDGMENTS

I want to express my gratitude towards my family for their support throughout this study.

I am grateful to Assoc. Prof. Dr. Şimşek DEMİR, Assoc. Prof. Dr. Lale ALATAN, Assoc. Prof. Dr. Vakur B. ERTÜRK for providing valuable suggestions, guidance and motivation for years.

I am also grateful to Prof. Dr. Nevzat YILDIRIM, Prof. Dr. Sencer KOÇ for valuable recommendations about writing of this thesis.

I want to thank Dr. Mustafa AKKUL, Şebnem SAYGINER and Dr. Taylan EKER for their support throughout the doctoral period.

Technical assistances of Ömer ÖÇAL, Murat SERTKAYA, Tülay CAN, Murat MUTLUOL and Sedat PEHLİVAN during the implementation of the circuits are gratefully acknowledged.

I want to express my special thanks to my colleagues Mustafa Barış DİNÇ, Hasan Hüseyin KILIÇ, Keziban AKKAYA for their support during this study.

Finally I want to thank to ASELSAN Company for technical support during this work.

# TABLE OF CONTENTS

ABSTRACT...	iv
ÖZ.....	v
ACKNOWLEDGMENTS.....	vii
TABLE OF CONTENTS .....	viii
LIST OF TABLES.....	xi
LIST OF FIGURES.....	xii
LIST OF ABBREVIATIONS.....	xvi
CHAPTERS	
1 INTRODUCTION .....	1
1.1 Background and Scope.....	1
1.2 Organization of the Thesis .....	10
2 DESIGN OF AN RF SWITCH IN SUBSTRATE INTEGRATED WAVEGUIDE STRUCTURE.....	11
2.1 Introduction .....	11
2.2 Shunt Diodes in a Waveguide.....	13
2.2.1 Single Post in a Waveguide.....	14
2.2.2 Three Posts in a Waveguide .....	15
2.2.3 SPDT in a Waveguide .....	16
2.3 Discussion.....	17
2.4 Conclusion .....	19
3 RF SWITCH UTILIZING EVANESCENT MODE WAVEGUIDE FILTER .....	20
3.1 Introduction .....	20



3.2	Substrate Integrated Waveguide.....	21
3.3	Pin Diode .....	21
3.4	Implementation of Shunt Resonators .....	22
3.5	Modeling of Shunt Resonators.....	24
3.6	Analysis of Waveguide Junction.....	32
3.7	Conclusion .....	35
4	DESIGN EXAMPLES OF RF SWITCH IN SIW.....	36
4.1	Introduction .....	36
4.2	SIW Parameters and Microstrip Transitions.....	37
4.3	SPST.....	38
4.3.1	Design of SPST.....	38
4.3.2	Prototyping and Measurements of SPST .....	43
4.4	SPDT .....	48
4.5	Conclusion .....	53
5	OTHER APPLICATIONS OF PIN DIODES IN SIW .....	54
5.1	Introduction .....	54
5.2	RF Power Limiter .....	54
5.2.1	Basic Limiter Circuit.....	54
5.2.2	SIW RF Power Limiter.....	57
5.2.3	Power Handling of SIW RF Power Limiter.....	61
5.2.4	SIW RF Power Limiter/Switch .....	65
5.3	Tunable Filter .....	68
5.4	Conclusion .....	70
6	CONCLUSIONS AND FUTURE STUDIES.....	71
	REFERENCES.....	74
	APPENDICES	
A.	EVANESCENT-MODE WAVEGUIDE FILTER DESIGN.....	80

B. MATERIALS AND DEVICES USED AT THE DESIGN AND PROTOTYPES .....	90
CURRICULUM VITAE .....	92

## LIST OF TABLES

### TABLES

Table 2.1	Properties of the substrate integrated waveguide .....	13
Table 3.1	Simulation parameters for the modeling of discontinuity .....	28
Table 3.2	The parameters used to calculate $n$ and $L_p$ values.....	33
Table 4.1	Substrate and filter properties of SPST .....	38
Table 5.1	Thermal resistances of the diodes.....	63
Table 5.2	Thermal resistance of diodes and maximum allowed power dissipation on diodes.....	63
Table B.1	Properties of GC4271 .....	90
Table B.2	Properties of CLA4604 and CLA4607 .....	91
Table B.3	Some electrical properties of RO4003 .....	91

# LIST OF FIGURES

## FIGURES

Figure 1.1 SIW structure .....	2
Figure 1.2 Cross sectional view of folded SIW (FSIW) structure [33].....	5
Figure 1.3 Dominant Mode in HMSIW and SIW [18].....	5
Figure 1.4 Simple microstrip to SIW transition [5] .....	5
Figure 1.5 Different variations of SIW structure.....	6
Figure 2.1 Top view (not to scale) and 3D view of a single post in a waveguide. Arrows show the direction of propagation. ....	14
Figure 2.2 Simulated isolation of single post in a waveguide .....	14
Figure 2.3 Top view (not to scale) and 3D view of three posts in a waveguide. Arrows show the direction of propagation. ....	15
Figure 2.4 Simulated isolation of three posts in a waveguide.....	15
Figure 2.5 Top view (not to scale) of SPDT in waveguide using only shunt diodes.....	16
Figure 2.6 Simulated isolation of SPDT in waveguide.....	17
Figure 2.7 Decreasing the width of the waveguide around diodes to improve isolation .....	18
Figure 3.1 The equivalent circuit of a diode.....	21
Figure 3.2 3-D view of diode mounted on the waveguide.....	23
Figure 3.3 Top view of the discontinuity .....	23
Figure 3.4 Test structure to model the discontinuity and top view of the simulation model. ....	24
Figure 3.5 Circuit representation of the test structure except the input and output waveguides .....	25
Figure 3.6 Approximate shunt equivalent of the T-network model .....	26

Figure 3.7 Top view of the HFSS model used for simulation.....	27
Figure 3.8 $j\omega Y$ vs. $\omega^2$ plot with $s=2.1\text{mm}$ and $C_{\text{lumped}}=0.7\text{pF}$ .....	29
Figure 3.9 $C_{\text{eq}}$ and $L_{\text{eq}}$ vs. $C_{\text{lumped}}$ .....	29
Figure 3.10 Top view of a 3 <sup>rd</sup> order evanescent mode waveguide switch	30
Figure 3.11 Top view of a resonator that is at the junction of waveguides	31
Figure 3.12 Test model for the discontinuity at the waveguide junction ...	31
Figure 3.13 Test circuit for the discontinuity at the waveguide junction...	31
Figure 3.14 Test structure to calculate waveguide step parameters .....	32
Figure 3.15 Lumped element representation of test structure .....	32
Figure 3.16 $n$ and $L_p$ values versus frequency for symmetric junction.....	34
Figure 3.17 $n$ and $L_p$ values versus frequency for asymmetric junction....	34
Figure 4.1 Drawings of TRL calibration kit.....	36
Figure 4.2 Drawing and Photograph of SIW thru line .....	37
Figure 4.3 Measured response of SIW thru line .....	38
Figure 4.4 Gain of the ideal filter .....	40
Figure 4.5 Modeling data for offset 0.9mm.....	41
Figure 4.6 Final filter response.....	41
Figure 4.7 Lossy simulation results of SPST.....	42
Figure 4.8 Simulation result of SPST in isolation mode.....	43
Figure 4.9 Photograph of the discontinuity before the mounting of diode and capacitors.....	44
Figure 4.10 Photograph of 3 <sup>rd</sup> order SPST switch prototype .....	44
Figure 4.11 Photo of diode and capacitor mounted next to each other ....	45
Figure 4.12 Linear measurement result of SPST at “on” state .....	46
Figure 4.13 Linear measurement result of SPST at “off” state .....	46
Figure 4.14 Built-in voltage on the pin diodes vs input power .....	47
Figure 4.15 Gain vs. input power measurement result of SPST.....	48
Figure 4.16 Top view of the simulation model of the SPDT switch.....	49
Figure 4.17 3D view of the simulation model of the SPDT switch .....	49
Figure 4.18 Performance of SPDT switch “on” and “off” branches.....	50

Figure 4.19 Performance of SPDT switch “on” and “off” branches with modified capacitors .....	51
Figure 4.20 Photograph of SPDT without bias lines and diodes .....	51
Figure 4.21 Measured and simulated gain of open arm of SPDT switch with $C_1=0.5\text{pF}$ and $C_2=0.4\text{pF}$ .....	52
Figure 5.1 Simple RF power limiter. Arrows represent RF power flow proportional to their sizes .....	55
Figure 5.2 Three regions of pin diode operation.....	56
Figure 5.3 3-diode RF power limiter .....	57
Figure 5.4 Picture of SIW RF power limiter .....	58
Figure 5.5 Photo of CLA4604 diode and capacitors mounted together ....	58
Figure 5.6 Insertion loss of RF power limiter .....	58
Figure 5.7 Comparison of measurement of CLA4604 diode with the simulation with modified parameters .....	59
Figure 5.8 Comparison of measurement of CLA4607 diode with the simulation with modified parameters .....	60
Figure 5.9 Comparison of IL vs. Pin measurement of SIW limiter with the simulation .....	60
Figure 5.10 Comparison of $P_{\text{out}}$ vs. $P_{\text{in}}$ measurement of SIW limiter with the simulation .....	61
Figure 5.11 Thermal resistance model of the diode on a via.....	62
Figure 5.12 Dissipated power in the diodes of SIW RF power limiter.....	64
Figure 5.13 Fundamental component of voltages across the diodes of SIW RF power limiter .....	64
Figure 5.14 A representative single diode in limiter.....	65
Figure 5.15 Single diode of RF switch biased with an Op-Amp.....	66
Figure 5.16 Response in isolation mode .....	66
Figure 5.17 Insertion loss and return loss of the switch for low power levels .....	67
Figure 5.18 $P_{\text{in}}$ vs. $P_{\text{out}}$ for SIW RF power limiter.....	67
Figure 5.19 Variation of the filter response while tuning.....	68

Figure 5.20 Variation of the filter response with single voltage tuning.....	69
Figure 5.21 The values $C_1$ and $C_2$ take with respect to center frequency.	69
Figure A.1 Filter formed by L-C resonators coupled by J-inverters .....	80
Figure A.2 Definition of J-Inverter.....	81
Figure A.3 J-Inverter coupled band pass filter circuit.....	82
Figure A.4 Equivalent circuit of waveguide transition .....	83
Figure A.5 J-Inverter coupled band pass filter circuit with equivalent circuits of waveguide junctions at both end. ....	84
Figure A.6 J-Inverter circuit representation .....	84
Figure A.7 Lumped equivalent of a J-Inverter .....	85
Figure A.8 Equivalent circuit of a waveguide in cutoff.....	85
Figure A.9 Equivalent circuit of a J-inverter and its equivalent one as a EWG section between two shunt inductive impedances ( $Z_3$ ) .....	86
Figure A.10 Evanescent mode filter with waveguide steps at both ends...	87
Figure A.11 Evanescent mode filter with waveguide steps at both ends...	87
Figure A.12 Flowchart for the general design procedure of the filter .....	89
Figure B.1 The drawing of the pin diode used for the design and the fabrication of the prototypes .....	90

## LIST OF ABBREVIATIONS

<b>DC</b>	:	Direct Current
<b>EM</b>	:	Electromagnetic
<b>EWG</b>	:	Evanescent-Mode Waveguide
<b>FDFD</b>	:	Finite Difference Frequency Domain
<b>FET</b>	:	Field-Effect Transistor
<b>MMIC</b>	:	Monolithic Microwave Integrated Circuit
<b>Op-Amp</b>	:	Operational Amplifier
<b>PCB</b>	:	Printed Circuit Board
<b>PEC</b>	:	Perfect Electric Conductor
<b>RF</b>	:	Radio Frequency
<b>SIW</b>	:	Substrate Integrated Waveguide
<b>SPDT</b>	:	Single Pole, Double Throw
<b>SPST</b>	:	Single Pole, Single Throw



# CHAPTER 1

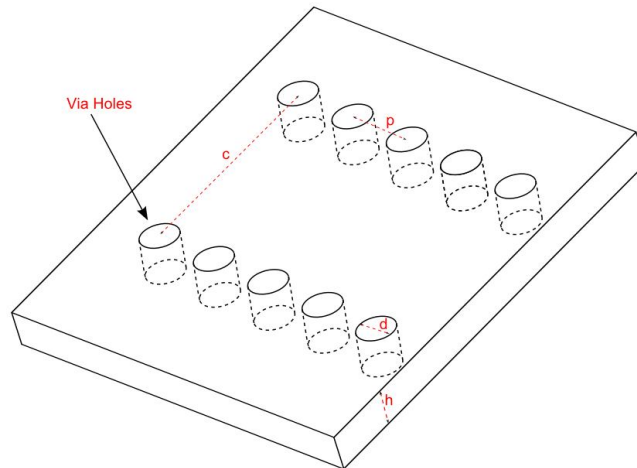
## INTRODUCTION

### 1.1 Background and Scope

For modern RF and microwave systems and circuits, low cost, easy fabrication, high integration capability and minimization of physical area are critical requirements. Planar structures like multilayer printed circuit boards are convenient for these purposes and they are also suitable to use with surface mount technology. This microwave circuit fabrication technology is very mature, cheap, easy and widespread. On the other hand, planar transmission structures like microstrip and coplanar waveguide are not very suitable for high-frequency applications because of their high insertion loss along with coupling and isolation problems. At high frequencies, waveguides have obvious advantages compared to planar transmission lines. They are immune to radiation losses and have excellent isolation since the transmission media is closed. Insertion loss of hollow waveguides is lower than planar transmission lines which use a dielectric as the transmission medium. However, since conventional waveguides are 3D metallic structures, they are more expensive, more difficult to fabricate and bulky. They are also difficult to integrate with planar circuitry which is essential for system development since most parts of complete systems are fabricated with PCB technology.

Substrate integrated waveguide (SIW), which is introduced in [1], is a waveguide structure that can be fabricated with conventional microwave

planar circuit techniques and integrated easily with planar circuitry. SIW is essentially a rectangular waveguide implemented by PCB manufacturing techniques. The bottom and top metal walls are formed by two metal layers of a multilayer PCB and lateral walls are constructed by densely, regularly placed plated vias instead of solid metallic walls which is usually not possible with standard PCB production technologies.



**Figure 1.1** SIW structure

Although lateral walls constructed from plated vias seem to complicate the analysis of SIW structure, it can easily be analyzed approximately as a rectangular waveguide by appropriately choosing an effective waveguide width according to via diameters and spacing between the vias. This effective width is usually calculated by empirical formulas. In the literature there are at least three different formulas with different levels of accuracy, one of which is given in [2].

Since the SIW structure is introduced, different problems have arisen about SIW. In the last decade, these problems are investigated in detail. The problem of transition between SIW and other transmission media are investigated and various transition structures are designed. Due to the discontinuous lateral walls, dispersion properties will be different than conventional waveguide. Discontinuous lateral walls also result in leakage

loss. These characteristics of SIW are analyzed in various works. SIW is also applied to many microwave components and systems. Some of the works involving SIW structures are summarized in this chapter.

The equivalence between SIW and rectangular waveguide is theoretically investigated in [3] and [4].

Wideband microstrip-SIW transitions are investigated as this is crucial for integration of SIW with planar integrated circuits. A simple microstrip-SIW transition is investigated in [5] and shown in Figure 1.4. Transition from microstrip to thicker SIW is also possible. Coplanar waveguide-SIW transition is investigated in [6]. H-plane step,  $90^\circ$  bend,  $90^\circ$  curvature, post resonator structures are also investigated [7] since these are frequently used structures at conventional waveguide circuits.

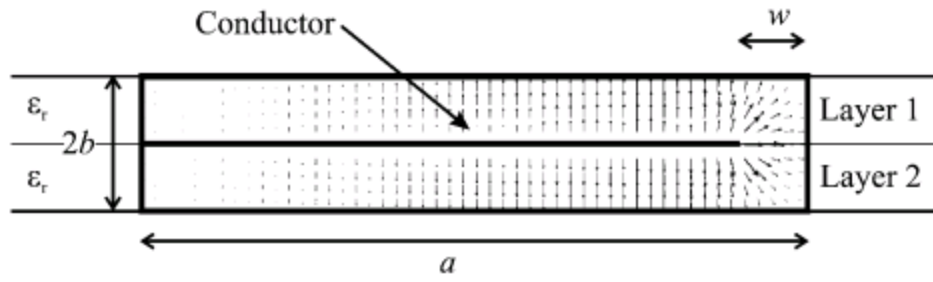
Microstrip-SIW transitions in multilayer substrates at which SIW is thicker than microstrip is investigated by Ding and Wu [8]. Ridged waveguides can be used as intermediate steps at this transition. Alternatively direct coupling or coupling by probe between microstrip and SIW can be used. 3-D transition examples to incorporate connectors to SIW circuits are given by Suntives and Abhari [9].

Transmission properties like dispersion and modes of SIW are investigated in several works. Dispersion characteristics of SIW are derived theoretically in [2]. In this work it is verified that guided wave transmission properties of SIWs are equivalent to rectangular metallic waveguides with an equivalent effective width. Similarly guided wave and mode characteristics of SIW structure are investigated in detail [10]. An important difference between SIW and rectangular waveguides is that TM modes do not exist in SIW. The reason is that lateral walls are discontinuous in the propagation direction

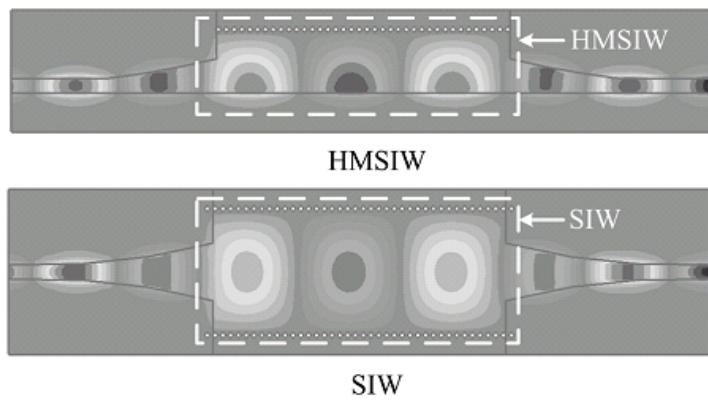
and cannot support transverse magnetic fields parallel to vias of lateral walls.

Since the lateral walls are not solid metal, there will be energy leakage between the vias, which must be kept low. This energy leakage is investigated by both theoretical methods and electromagnetic simulation [11]. The results of this work give some guidelines for effective SIW design.

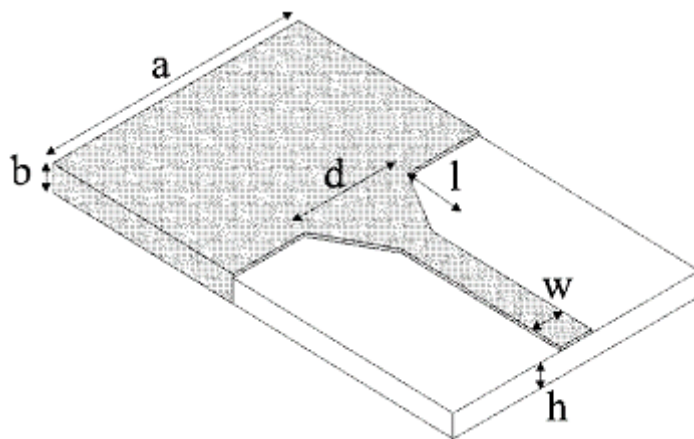
There are many variations of classical SIW structure. FSIW (Folded SIW) and HMSIW (Half mode SIW) [12] are two modifications to conventional SIW. Although the underlying principles are the same, their widths are nearly half of the SIW. Since the vertical E-field is maximum at the center of the SIW, the center line can be considered as an equivalent magnetic wall. If half of the SIW is cut away from this line, field distribution at the remaining part remains almost the same as shown in Figure 1.3, because the height of the SIW is much lower than the width of the SIW. FSIW is analyzed in detail [13]. The width of FSIW is also half of the SIW, but it is a multilayered transmission medium as shown in Figure 1.2. Rectangular waveguide is not the only waveguide type that can be integrated in a planar circuit. There are also other techniques which enables other waveguide types such as dielectric or image guides to be integrated with planar circuits. Some of the examples are Substrate Integrated Slab Waveguide (SISW), Substrate Integrated Non-Radiating Dielectric (SINRD) guide, Substrate Integrated Image Dielectric Guide (SIIDG), Substrate Integrated Inset Dielectric Guide (SIINDG) and Substrate Integrated Insular Dielectric Guide (SIIG) [1]. Pictures of these waveguides are shown in Figure 1.5. The transmission properties of these waveguides are different than rectangular waveguides. To use the standard PCB fabrication techniques and maintain the rigidity of the structure, the hollow regions are implemented by filling the area with unplated large vias in these transmission structures.



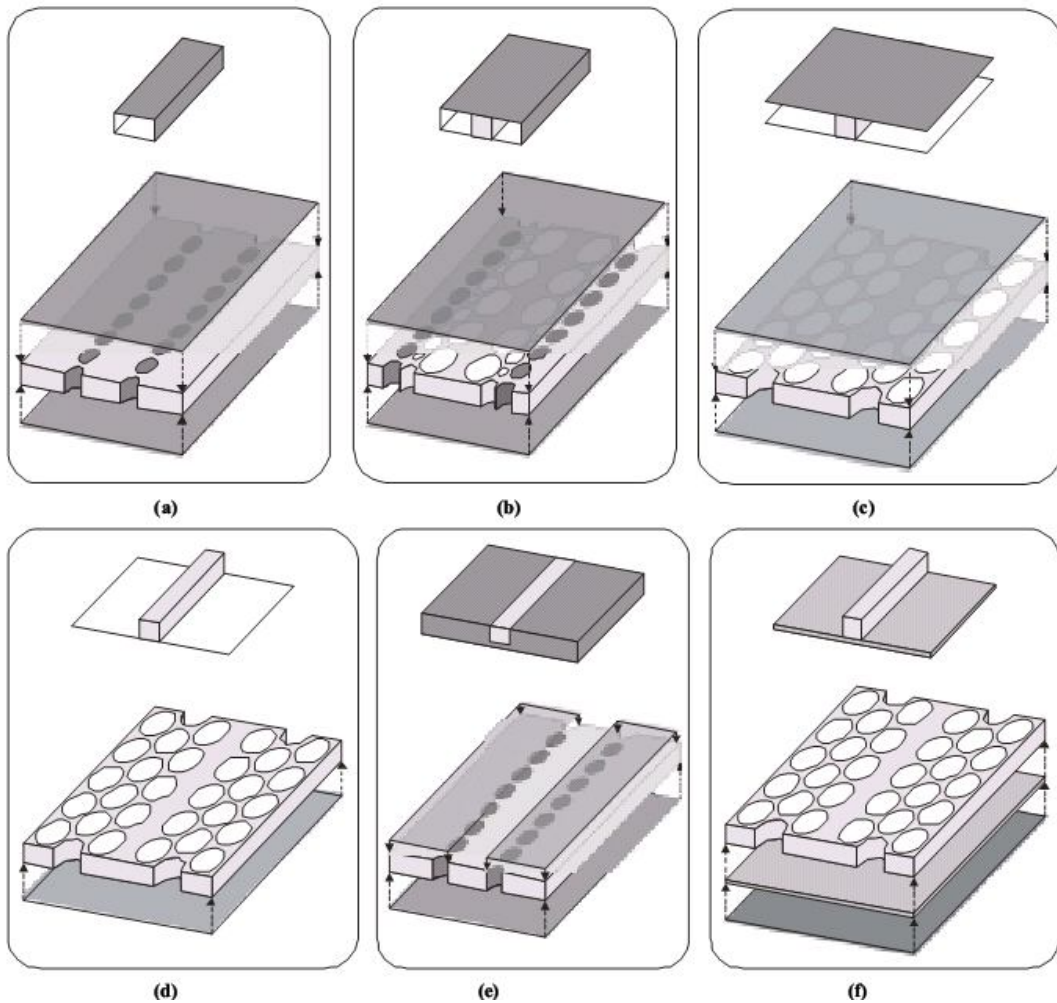
**Figure 1.2** Cross sectional view of folded SIW (FSIW) structure [33]



**Figure 1.3** Dominant Mode in HMSIW and SIW [18]



**Figure 1.4** Simple microstrip to SIW transition [5]



**Figure 1.5** Different variations of SIW structure: (a) Substrate Integrated Waveguide (SIW), (b) Substrate Integrated Slab Waveguide (SISW), (c) Substrate Integrated Non-Radiating Dielectric (SINRD) guide, (d) Substrate Integrated Image Dielectric Guide (SIIDG), (e) Substrate Integrated Inset Dielectric Guide (SIINDG), (f) Substrate Integrated Insular Dielectric Guide (SIIG) [1]

Many microwave components previously implemented using conventional waveguides are adapted to SIW structure. A power divider [14] and a balun [15] are implemented using SIW. Two compact coupler structures in SIW form is proposed [16], [17]. HMSIW structure is also used to realize a coupler [18], a directional filter [19] which also incorporates couplers and a band pass filter [20]. HMSIW structure is shown in Figure 1.3.

Waveguide antenna or antenna array structures can be easily adapted to SIW structure with their feed networks. The most natural antenna type to design with SIW is the slot antenna which is frequently used with conventional rectangular waveguides. A single slot antenna working near 96 GHz is designed and implemented [21]. Different configurations of slots are also used to implement various kinds of antennas and arrays in SIW and HMSIW structure [22]. Low side lobe slot arrays are implemented in SIW and HMSIW structures [23]. Yang et al. showed the realization of another slotted waveguide array and its SIW feed network [24]. 4-by-4 slot antenna array is implemented using SIW and microstrip feed network [25].

Waveguide filters are one of the most common structures adapted to SIW form. Hao et al. proposed an elliptical filter implemented using SIW [26]. It also incorporates microstrip input and output by SIW-microstrip transitions. Deslandes and Wu investigated the integration of planar circuits with waveguide filters by microstrip or coplanar waveguide to SIW transitions and they gave an example by implementing a waveguide inductive post filter in SIW [27]. A quasi-elliptic filter is designed using SIW structure [28]. A SIW cavity is investigated by finite difference frequency domain (FDFD) in terms of quality factor (Q) and resonance frequency and then a waveguide cavity filter is designed using the defected ground structure by Zhang et al. [29]. High-pass characteristics of a waveguide are combined with the band stop characteristics of periodic structures to realize very wideband band pass filters in [30]. Two SIW filters are designed which utilizes cross-coupling for high-selectivity [31]. An inductive post waveguide filter and a dual-mode filter are implemented [32]. Waveguides and a direct coupled cavity filter are realized using FSIW structure [33]. A kind of tunable filter realization in SIW is investigated in [34].

SIW technology enables easy integration of slot antenna arrays and their feed networks with planar circuitry. A passive frontend example is given by

Deslandes and Wu which incorporates two slot array antennas, a dual-mode waveguide filter, a waveguide power divider and a microstrip to SIW transition [35]. This is a good example to show the potential of SIW technology.

Active elements like diode and transistor are also incorporated in SIW to implement various components. Active elements are used either as a nonlinear element as in oscillators, amplifiers and mixers, or as a control element as in switches, phase shifters and tunable filters. Resonators form an important part of both filters and oscillators. Cavity resonators are particularly easy to implement in SIW. Resonance frequency of these cavities can even be made continuously tunable using varactor diodes ([36], [37] and [38]). Microwave oscillators are designed in SIW using cavity resonators and Gunn diode [39] or FET [40] as the active element. An X-Band amplifier is designed in [41] with SIW input and output. A single balanced diode mixer is designed and implemented in SIW [42] by using a  $180^\circ$  hybrid, a low pass filter, quarter wave resonators and diodes. Analogue voltage controlled phase shifters based on hybrid couplers loaded with varactor diodes are implemented in SIW [43].

Various kinds of switches are designed and used in RF and microwave systems. Switches can be made mechanical, solid state or ferrite based. In general, pin diode or FET based switches produced with MMIC technology are used in these systems because of their high performance and small size. Their small size cause problems for high power applications, because dissipated heat cannot be removed easily from small base area. For higher power handling, switches are designed using discrete high power pin diodes which are used in shunt configuration instead of series configuration for more effective heat removal. For very high power applications, waveguides are generally used as the transmission medium and ferrite based waveguide switches are used for switching applications. Mechanical



switches offer very low loss at high frequency and low power dissipation, but these switches suffer from low switching speed and limited number of cycles. In the end, a suitable switch type is chosen according to the application and performance requirements.

RF switches are also realized in SIW. An RF switch is realized in SIW by shorting out a longitudinal opening in the upper wall of the waveguide by beam-lead diodes [44]. Recently another RF switch is designed in SIW by loading the sidewalls of SIW by rectangular ferrite slabs [45]. These two switch designs are based on shifting the cutoff frequency of the structure. In [44] this is done by modifying the upper wall of the waveguide. In [45], application of a magnetic bias on ferrite slabs shifts the cutoff frequency of the SIW to a higher frequency and thus reflects the incident wave back.

In this work, an RF switch in SIW for X-band is designed and demonstrated. This switch differs from the other RF switches in SIW found in literature, by that this switch also functions as an RF filter. So that different RF functions like filtering and switching are combined in one component which relaxes physical space requirements. In “off” state, high isolation is obtained in a small space. An SPDT switch is designed and demonstrated to show the extendibility of the design to switches with multiple arms. It is also shown that using this physical structure, RF power limiting functionality can also be included in an RF filter and a tunable filter can be designed.

SIW structures are frequently preferred in microwave systems instead of conventional waveguide structures due to their advantages like lightweight, low cost, easy fabrication etc. These waveguide structures might be slot antenna arrays, waveguide filters, etc. SIW is typically used at the frontends of these systems. So the design of RF components like RF switches, pre-selector filters and RF power limiters which are usually utilized at these frontends is a necessity. Since SIW is a waveguide, it has a lower cutoff

frequency and SIW components are typically much larger than microstrip components at X-band. Physical area is an important limitation for SIW components and these components should be designed as small as possible. Another technique that provides physical advantages would be to combine several RF functions in a single component. This can be useful since in a typical microwave frontend, RF power limiter, RF switch and RF pre-selector filter are found together and usually in series to each other. Considering these facts, the work described in this thesis is thought to be beneficial in SIW systems.

## **1.2 Organization of the Thesis**

In Chapter 2, initial works to design an RF switch in SIW and conclusions of these works are given. At first stage, only shunt diodes in a uniform SIW are used to design a switch.

In Chapter 3, the design of an RF switch in SIW is described. The design is based on and starts with the design of an evanescent mode waveguide filter. The details about the implementation and modeling are given.

In Chapter 4, the measurement results of SPST and SPDT switches designed using the technique described in Chapter 3 are given. The measurement results confirm the design technique and show good switch response.

In Chapter 5, some alternative components designed using the same circuit structure are described. These components are RF power limiter and tunable filter.

Conclusions derived from the works described in this dissertation and possible improvements for the future are given in Chapter 6.

## CHAPTER 2

# DESIGN OF AN RF SWITCH IN SUBSTRATE INTEGRATED WAVEGUIDE STRUCTURE

### 2.1 Introduction

RF Switch is an RF component that opens or closes a certain path for the transmission of RF signals. They are frequently used components of RF systems and subsystems. They can be mechanical (relay, MEMS etc) or electrical (FET, pin diode etc). RF switches can be designed in a way suitable to surface mount technology using FETs (field-effect transistor) or pin diodes. In general these switches are designed to be used with planar transmission line technologies (microstrip, coplanar waveguide etc). However, if SIW is used in an RF subsystem as the main transmission structure, it is cumbersome to make a transition to microstrip and then to SIW again, just to incorporate an RF switch to the path. So it is advisable to design a switch that can be effectively incorporated in a SIW transmission path.

The main parameters of an RF switch are insertion loss in the “on” state, isolation (insertion loss in the “off” state), switching speed (time required for the transition from the “on” state to “off” state or vice versa) and power handling. Power handling mainly depends on the active elements used and pin diode switches that handle hundreds of watts are available. Switching speed depends on the capacitance of the diode and the biasing circuit. For

typical microwave switches, switching speeds are in the order of nanoseconds. Isolation values around 40-50dB and insertion loss values around 0.5-1dB are also typical values for microwave switches in X-band.

There are RF switches developed for SIW structure in literature. In [44], beam-lead pin diodes are used to short out a longitudinal opening in the upper wall of SIW. This structure is both physically large and can cause radiation loss because of the opening at upper wall. Another RF switch is designed in [45]. This structure uses vertical ferrite slabs in dielectric and this structure is not suitable for standard PCB manufacturing technique. Both switches have good switching performance in terms of isolation and insertion loss. The aim should be to design an RF switch with similar performance but without the disadvantages mentioned.

SPST (single pole single throw) switches will be considered first, because of their simplicity. These switches have one input and one output, and are used to enable or disable the transmission of RF signals between input and output.

As the active element, pin diodes are chosen instead of FETs for the design of switch, since they are very suitable to incorporate in a waveguide because of their physical structure.

Although the aim is to implement a switch in SIW, the major part of the analysis can be done using a conventional rectangular waveguide. At the final part, a minor modification will be done to the width of the waveguide according to (3-1) to use SIW instead of rectangular waveguide.

In this work lower X-band (between 8-9GHz) is aimed as the operating frequency band. So a waveguide with a cutoff frequency around 5GHz is chosen. Since SIW is fabricated using printed circuit board technology a

substrate should be chosen. RO4003C© [55] from Rogers Corporation is chosen. Its relative dielectric permittivity is around 3.38. So waveguide width is chosen to be 16mm which gives a cutoff frequency of 5.1GHz. These waveguide properties are used in all simulations. The properties of the waveguide are summarized in Table 2.1.

All electromagnetic simulations are done by HFSS®, a full-wave 3-D electromagnetic simulation software [53].

**Table 2.1** Properties of the substrate integrated waveguide

<b>Waveguide Property</b>	<b>Value</b>
Substrate	RO4003C
Relative Dielectric Permittivity Of The Substrate	3.38
Waveguide Width	16mm
Waveguide Height	0.5mm
Cutoff Frequency	5.1GHz

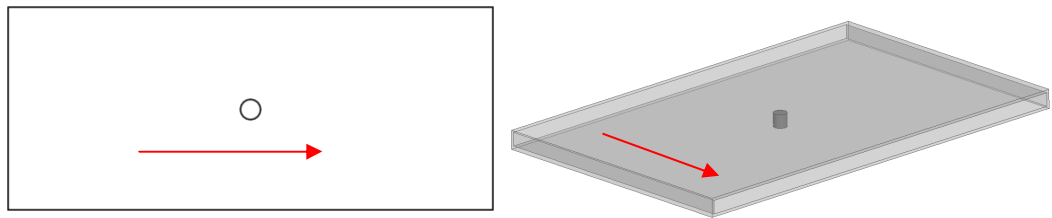
## **2.2 Shunt Diodes in a Waveguide**

The most obvious way to implement a switch in a waveguide is to place shunt diodes in the waveguide. If these diodes are biased to decrease their resistance to very small values, they will make a nearly short circuit between the top and bottom walls of the waveguide and put the waveguide in isolation mode.

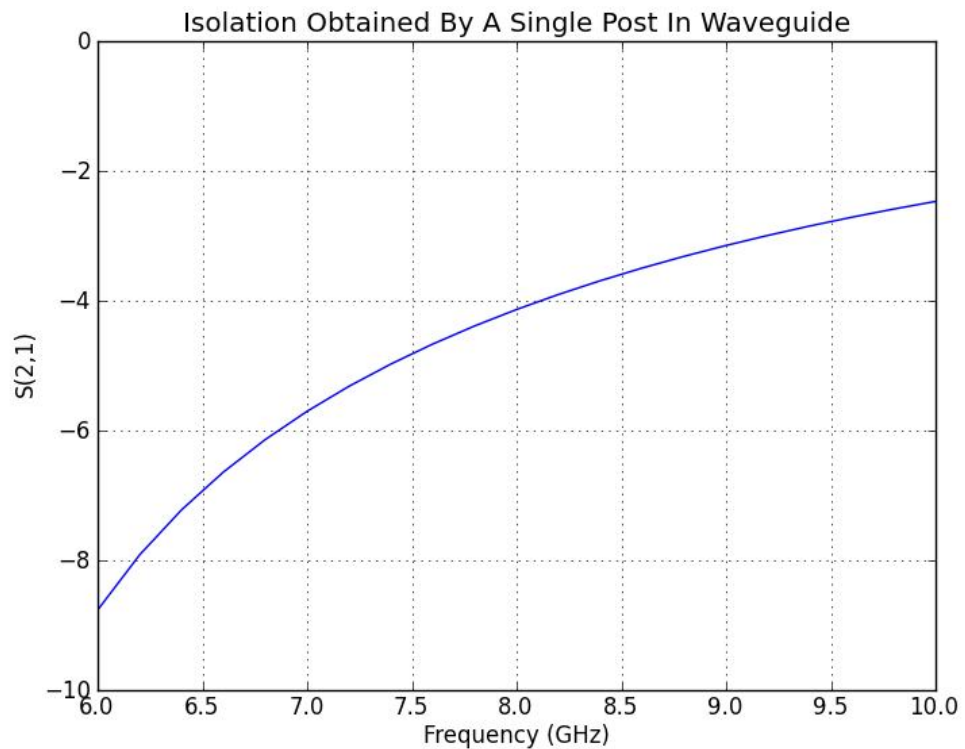
Although the details of a pin diode will be given in the next chapter, in this chapter a shunt mounted diode in a waveguide is basically modeled by a conductive post when it is in “on” state. Before going into the details of the diode model, simple posts can be put in a waveguide to see the isolation values that can be achieved by this method. Using a real diode model would give worse results because of finite series resistance of diode.

## 2.2.1 Single Post in a Waveguide

As the first step, isolation of a single shunt PEC post in a rectangular waveguide is investigated. The configuration is shown in Figure 2.1. The diameter of the post is chosen to be 20mil, because the width of RF pin diodes that have a low parasitic capacitance is approximately at this value. Wider diodes could have higher parasitic capacitance which will negatively affect the insertion loss of the switch when the diode is reverse-biased. The simulation result is shown in Figure 2.2.



**Figure 2.1** Top view (not to scale) and 3D view of a single post in a waveguide. Arrows show the direction of propagation.

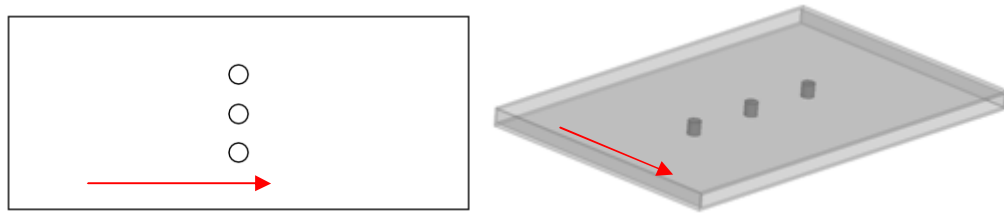


**Figure 2.2** Simulated isolation of single post in a waveguide

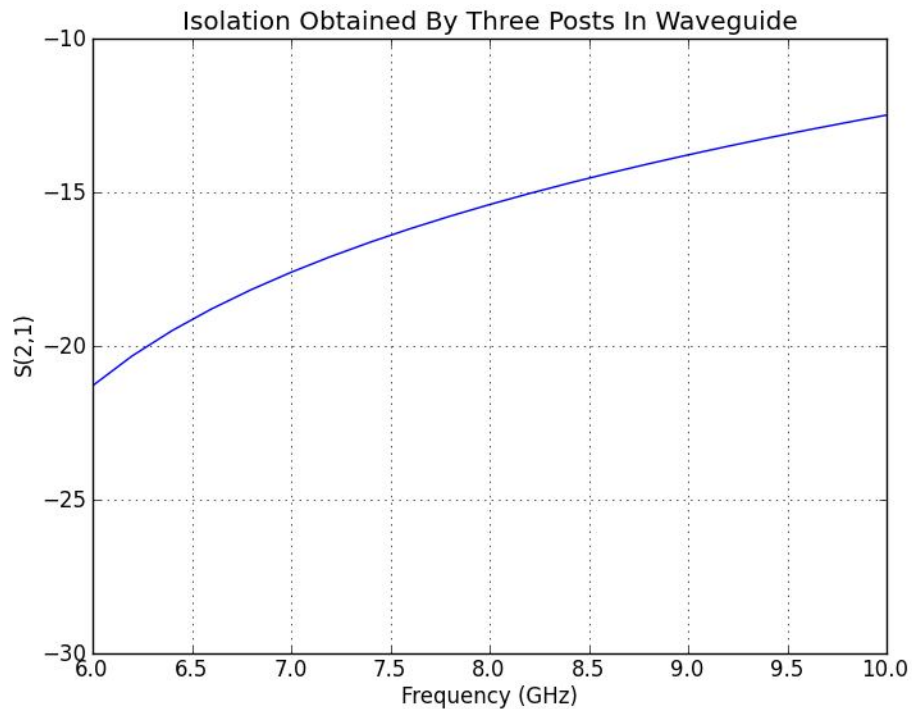
The isolation obtained using a single post is around 4dB at 8-9GHz frequency range which is an unacceptable isolation value.

### 2.2.2 Three Posts in a Waveguide

Single post is found to be inadequate to short this waveguide for a sufficient isolation. So a trial with three posts is done. The configuration is shown in Figure 2.3. The optimum separation between the posts is found to be 3mm by optimization. The simulation result is shown in Figure 2.4.



**Figure 2.3** Top view (not to scale) and 3D view of three posts in a waveguide. Arrows show the direction of propagation.



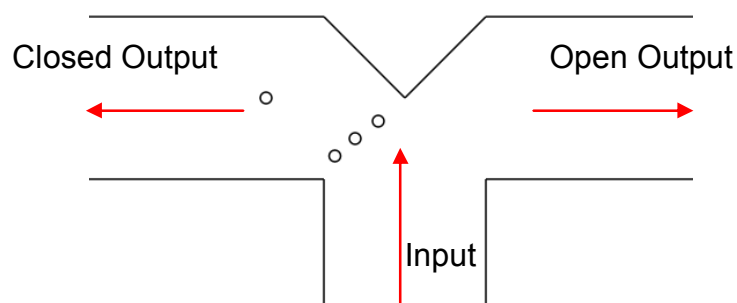
**Figure 2.4** Simulated isolation of three posts in a waveguide

The isolation obtained using three posts is around 16dB at 8-9GHz frequency range. Although a vast improvement (13dB) is obtained with respect to single post case, this is still a very low value for an isolation specification.

Isolation can be increased by further increasing the number of pin diodes. But this method is inefficient since increasing the number of diodes will inevitably increase the insertion loss of the switch in “on” state. It will increase the cost too. Before looking for an alternative way to increase the isolation, isolation that can be obtained in a SPDT switch will be analyzed.

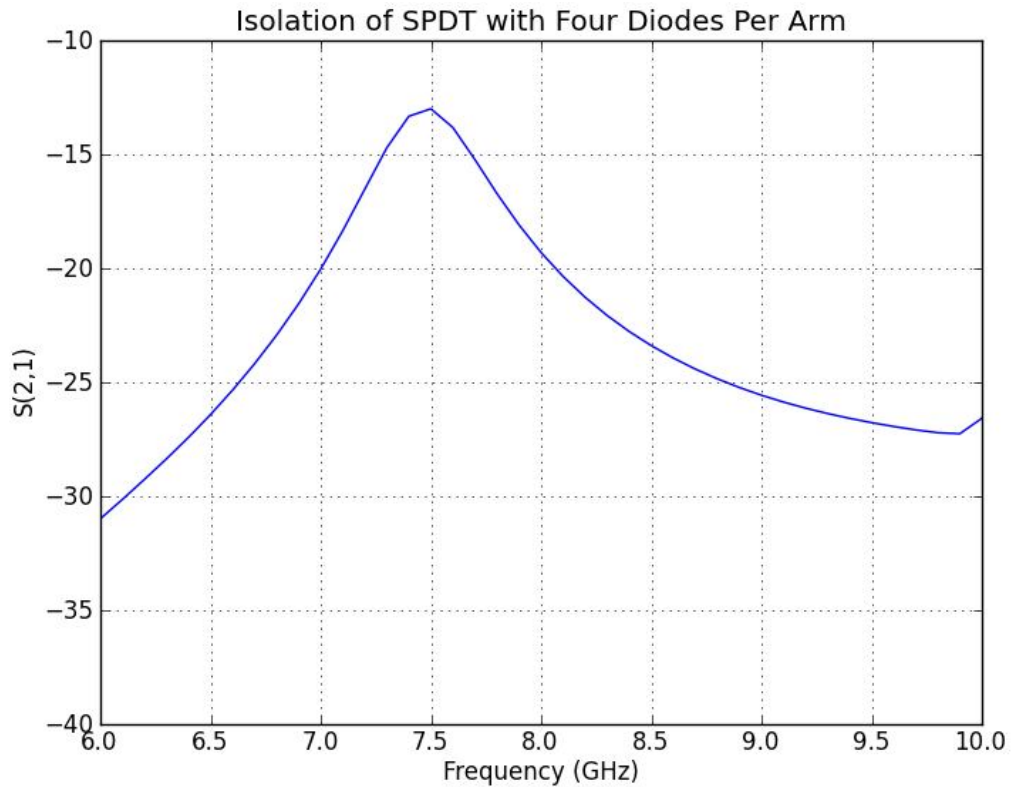
### 2.2.3 SPDT in a Waveguide

SPDT switches are frequently used in microwave systems for various functions like switching between transmit and receive paths in frontends. In this part, isolation of an SPDT switch will be analyzed. For this purpose an SPDT switch is designed in a waveguide. Four diodes are used at each arm. Three diodes are in a row and fourth diode is placed a certain distance away and this distance is adjusted to optimize the isolation at 9-10GHz band. Even in this case isolation is found to be between 25-30dB. The configuration is shown in Figure 2.5. The simulation result is shown in Figure 2.6. Although this isolation value could be enough for some applications, it is much lower than a typical microwave switch designed in microstrip with four diodes per arm.



**Figure 2.5** Top view (not to scale) of SPDT in waveguide using only shunt diodes





**Figure 2.6** Simulated isolation of SPDT in waveguide

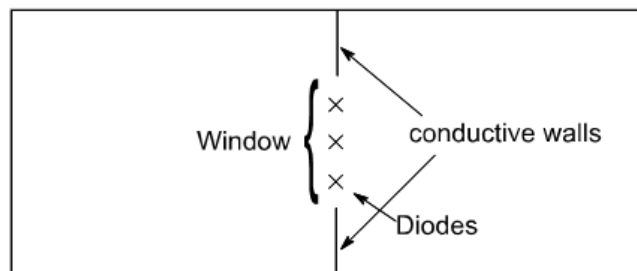
## 2.3 Discussion

As shown in this chapter, shunt diodes in a rectangular waveguide are not enough for a sufficient isolation. Of course the number of diodes can be increased, but it is not an efficient way. At microstrip technology, isolation values in excess of 50dB can be achieved using three diodes for an SPST switch, which should be a target for SIW switch.

The main reason for the low isolation values is thought to be the ratio between the width of a diode and the width of the waveguide. Since it is almost impossible to find a higher width diode with low parasitic, the width of the waveguide should be decreased. Since the cutoff frequency of the waveguide should stay the same, a substrate with a higher dielectric

permittivity can be chosen, but this is not always possible, because our structure is designed to be integrated with other RF components on a single PCB, and other components may dictate a particular substrate because of other factors such as low loss, high temperature durability etc. So a method that will work with a broad range of dielectric permittivity values should be developed.

Another approach is to use the same waveguide, but decrease the width of the waveguide only around the diodes as shown in Figure 2.7. This method surely increases the isolation, but it introduces another problem. The switch should exhibit low loss at the “on” state. If the posts are taken out, the iris formed by the conductive walls will be a serious discontinuity and increase the return loss of the switch.



**Figure 2.7** Decreasing the width of the waveguide around diodes to improve isolation

In general, waveguide structures are used in relatively narrowband systems. So the discontinuity of iris can be matched at this relatively narrow frequency band to improve the return loss. But there is a better solution. A natural way to decrease the width of the waveguide with inherent matching is to design a waveguide filter since waveguide filters have iris-like discontinuities in them to implement shunt inductances and other elements. At these discontinuities, filter has only a narrow window. Diodes can be placed in these narrow windows to obtain a better isolation. Among the filter alternatives an evanescent mode waveguide filter that will cover the operating frequency band of the system, is the best choice. There are

obvious advantages of using this approach with an evanescent mode waveguide filter. These advantages are listed below.

1- Since evanescent mode waveguide section is narrower than conventional waveguide, shunt diodes will be more effective at obtaining a good isolation.

2- Additionally, waveguide width will be decreased more around the diodes, to implement the shunt inductances needed for filter topology. So the effectiveness of the diodes at obtaining a good isolation will be increased.

3- Since it is a filter, if the design is done properly such that the diodes will be a part of the filter, the matching of the structure will not be an additional problem.

Shunt diodes can be incorporated easily into such a filter structure to add switching functionality to the filter and design an RF switch.

## **2.4 Conclusion**

In this chapter, the feasibility of designing an RF switch by using shunt diodes in a uniform SIW is investigated. One of the most important parameters of an RF switch is the isolation in “off” state. So isolation values that can be achievable using shunt diodes in SIW is investigated and found to be inadequate. The reason is thought to be that the SIW is much wider than the pin diode. The method that will be followed is to narrow the waveguide locally by designing an evanescent mode waveguide filter that covers our operating frequency band.

In the following chapter, the details about the design of an RF switch starting from a filter design will be investigated.

## CHAPTER 3

# RF SWITCH UTILIZING EVANESCENT MODE WAVEGUIDE FILTER

### 3.1 Introduction

In this chapter, design and implementation details of a substrate integrated waveguide switch is given. The design is based on the design of an ideal evanescent mode waveguide filter. This kind of filter is investigated in [51] and filter design between identical waveguides is described in Appendix A for reference. The design steps can be listed as follows:

- 1- Determination of substrate, input and output effective waveguide widths. Often substrate is dictated by the whole system design. Then waveguide widths should be determined according to operating frequency band.
- 2- Determination of SIW parameters like via diameter, via pitch and input and output waveguide widths depending on operating frequency band. There are empirical equations for this purpose.
- 3- Choosing the evanescent mode waveguide width
- 4- The parameters of equivalent circuit of waveguide transitions at the input and output
- 5- Design of the filter and calculating the effective inductances and capacitances values of the shunt resonators.
- 6- Design of the shunt resonators.

The details of these steps are given in this chapter.

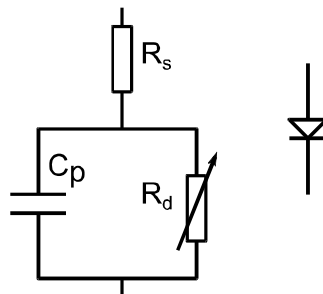
### 3.2 Substrate Integrated Waveguide

A 3-D view of substrate integrated waveguide is shown in Figure 1.1. Although the distance between two rows of vias is “c”, it is not the effective width that determines the cutoff frequency of the waveguide. The effective width of rectangular waveguide can be found using via diameter (d), via pitch (p) and lateral spacing (c), either by full wave methods or empirical equations. Empirical equations [46] are used for simplicity and they are verified using 3D EM simulation. Effective width of the waveguide is given in [2] as:

$$w_{eff} = c - \frac{d^2}{0.95p} \quad (3-1)$$

### 3.3 Pin Diode

Pin diode is the nonlinear device used at the SIW RF switch. Pin diodes, different from p-n junction diodes, have an intrinsic layer between p and n layers. This property enables them to be used as a current controlled resistor which makes them ideal for RF switching applications. The equivalent circuit of a pin diode is shown in Figure 3.1.  $R_s$  is a small (1-2 Ohms) series ohmic resistance.  $C_p$  is parasitic package capacitance and  $R_d$  is current controlled resistance. Without a bias current, pin diode is effectively a capacitor. When an adequate DC current is applied to the diode, the resistance of current controlled resistor decreases and the diode becomes effectively short circuit and impedance becomes  $R_s$ .



**Figure 3.1** The equivalent circuit of a diode

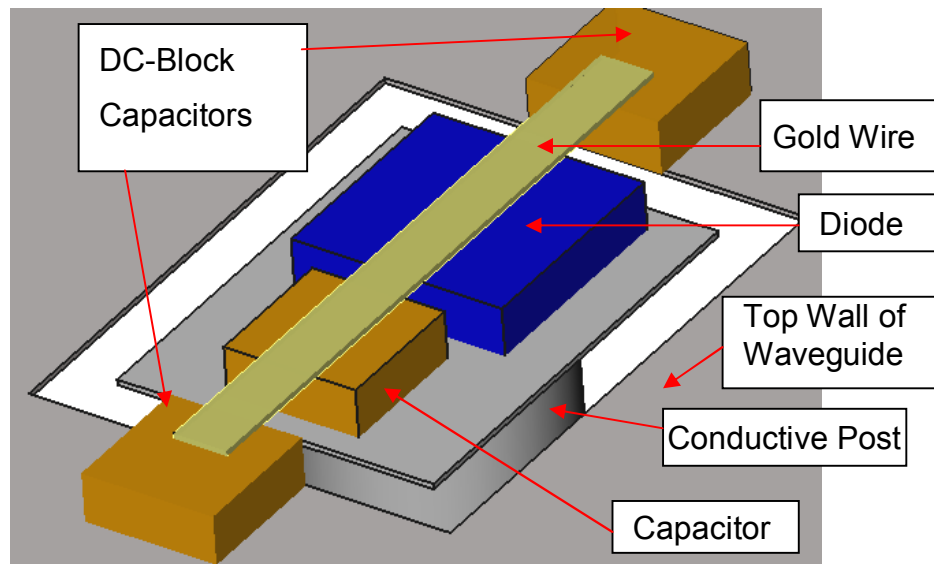
In this application, pin diode will be used in shunt configuration. A typical pin diode that can easily be used in shunt configuration is GC4271 from Microsemi [47] and it is used for simulations and prototypes. The properties of the diode are given in Appendix B.1.

### **3.4 Implementation of Shunt Resonators**

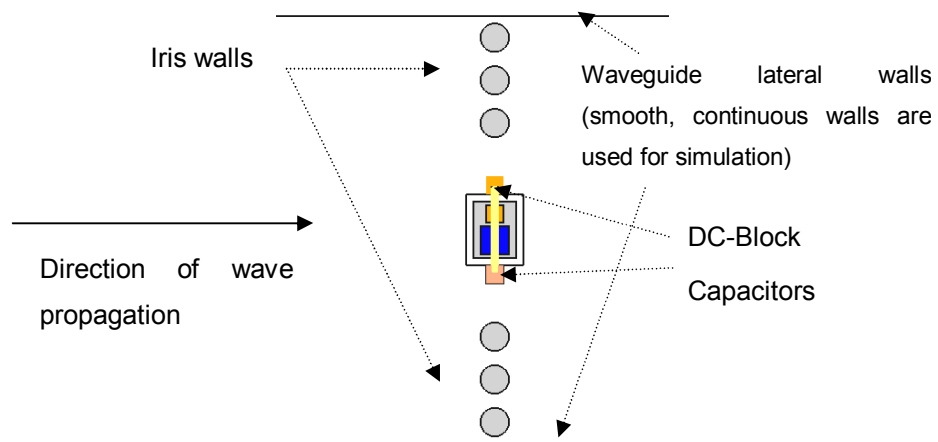
Shunt resonators of filter consist of shunt inductors and shunt capacitors. For switching action, pin diode is placed in shunt configuration. While reverse biased, pin diode behaves mostly like a capacitor. So it is reasonable for the diode to be part of one of the filter's shunt capacitors. At first glance it might seem plausible to open an un-plated hole in the substrate and putting the diode in the hole, but the height of the diode (typically 4mil) might be much lower than a typical substrate height which makes this method impractical. Instead, an alternative mounting structure is proposed which is more suitable for fabrication. In this structure, diode is placed on the top of a conductively filled via. The upper face of the via, on which diode is placed, is electrically isolated from the upper wall of the waveguide with a moat. The anode of the diode should be shorted to upper wall of the waveguide at the operating frequency band. But a DC block capacitor should be placed between the anode of the diode and the upper wall of the waveguide since the diode will be biased for switching action. DC bias is given from the upper plates of these capacitors. The mounting structure is shown in Figure 3.2. The capacitance of the diode and the parallel plate capacitor mounted next to the diode forms the capacitor needed by the filter. For a better electrical performance, the number of connections from the diode and parallel plate capacitor to DC block capacitors can be increased at the cost of production difficulty. This mounting structure is effective and easy to produce provided that suitable diode and capacitors exist. SIW can be easily produced with standard PCB production technology. The most uncommon feature is the conductively

filled via, but nowadays it has become widespread technology too. Capacitors and diode can be mounted using hybrid chip & wire technology.

A shunt inductor effect in a waveguide can be realized by an inductive iris [49]. A typical inductive iris requires vertical walls just like lateral walls of the waveguide. In SIW, for inductive iris, vertical walls are implemented by plated vias just like lateral walls. Top view of the structure is shown in Figure 3.3.



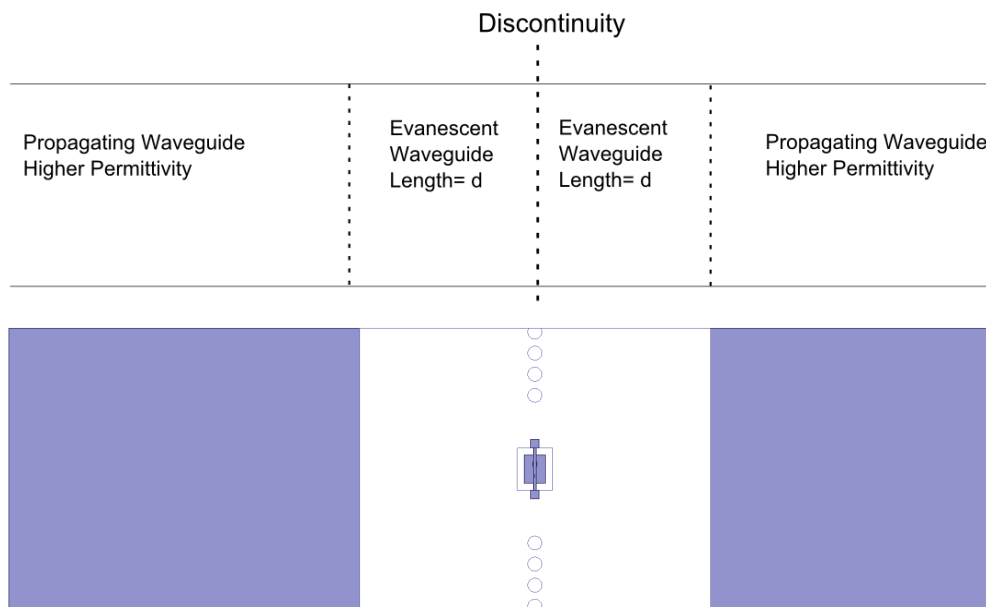
**Figure 3.2** 3-D view of diode mounted on the waveguide



**Figure 3.3** Top view of the discontinuity

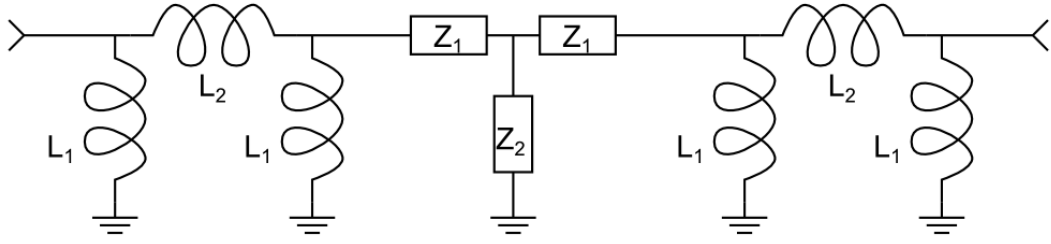
### 3.5 Modeling of Shunt Resonators

The field distribution in a waveguide is much different than a transmission line, so the capacitor might have a very different effective value in this structure. Also, closed form expressions are not available for SIW inductive iris. This structure can behave as a shunt L-C resonator at a moderate bandwidth. Effective shunt L and C values of shunt L-C resonator equivalent to this structure can be calculated by 3D EM simulation. In the simulation, regular rectangular waveguide will be used with smooth walls for effective use of computational resources. The test structure shown in Figure 3.4 will be used for simulation and modeling of the discontinuity. Test structure is formed by a physically uniform waveguide with the same dimensions as the evanescent-mode SIW. The discontinuity to be modeled is placed at the center of the waveguide. At both sides of the discontinuity, evanescent mode section of the waveguide extends by  $d$ . The substrate is the same as the filter itself. Since the input and output waveguides should allow propagation at the simulation frequency, a higher permittivity dielectric material will be used at the remainder of the waveguide.



**Figure 3.4** Test structure to model the discontinuity and top view of the simulation model.





**Figure 3.5** Circuit representation of the test structure except the input and output waveguides

The discontinuity can simply be modeled as a T-network. Electrical equivalent circuit of the structure excluding the input and output waveguides is shown in Figure 3.5. Waveguide step formed by only a change of substrate has little parasitic effect, so waveguide step is neglected in this model.  $L_1$  and  $L_2$  values form the lumped element equivalent of evanescent mode waveguide section with length  $d$ . Their values can be calculated using the equations (A-16), (A-17) and (A-18). The  $Z_1$  and  $Z_2$  impedances can be calculated once the ABCD matrix of the T-network is determined. The ABCD matrix of the whole structure can be calculated from the s-parameters calculated by 3D EM simulation of the waveguide structure. In the simulation, propagating-mode waveguides are excluded by de-embedding. ABCD matrix of the T-network representing the discontinuity is given as;

$$T = E^{-1} \cdot A \cdot E^{-1} \quad (3-2)$$

where;

A: ABCD matrix of the whole structure

E: ABCD matrix of the evanescent mode waveguide section

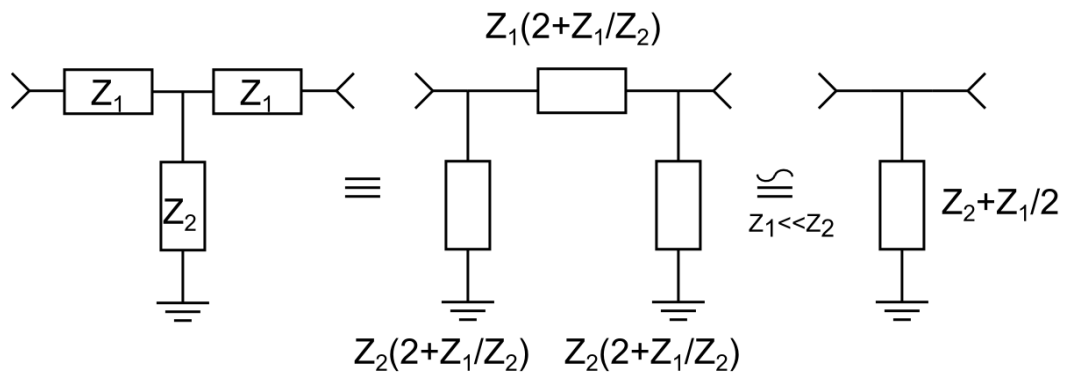
T: ABCD matrix of the T-network

ABCD matrix of whole structure can be calculated using 3D EM simulation. Once the ABCD matrix of the T-network is determined, ABCD matrix is converted to Z-matrix and then  $Z_1$  and  $Z_2$  can be determined from (3-3) and (3-4).

$$Z_2 = Z_{12} \quad (3-3)$$

$$Z_1 = Z_{11} - Z_{12} \quad (3-4)$$

Shunt impedance equivalent of this structure is being sought. So  $Z_1$  impedances are not a part of the filter and in fact their values are very low compared to reference impedance and  $Z_2$ . T-network is converted to a Pi-network and series element is neglected to approximate this T-network by a shunt element.  $Z_1$  impedances could be neglected from T-network directly, but this method worked better.

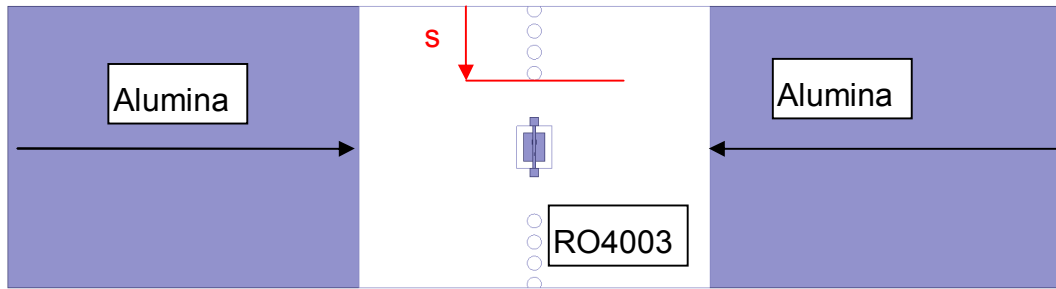


**Figure 3.6** Approximate shunt equivalent of the T-network model

This shunt element is expected to be a parallel combination of L and C values. So equation (3-5) should be satisfied for its admittance.

$$j\omega Y = \frac{1}{L_{eq}} - \omega^2 C_{eq} \quad (3-5)$$

In this equation  $C_{eq}$  and  $L_{eq}$  are the equivalent C and L of the structure. If the structure behaves like a parallel combination of L and C in shunt configuration, the  $j\omega Y$  vs.  $\omega^2$  plot should be approximated by a line near the design frequency. Then  $C_{eq}$  can be calculated using the slope of this line and  $L_{eq}$  can be calculated using the point at which the line crosses the  $\omega^2$  axis, if the line is extended. Alternatively  $L_{eq}$  and  $C_{eq}$  can be calculated using two frequency points on the plot near the design frequency.



**Figure 3.7** Top view of the HFSS model used for simulation

The details of the structure used for simulation is given in Figure 3.7. Two independent parameters are needed to adjust  $C$  and  $L$  concurrently. If the diameters of vias and spacings between them are determined and fixed beforehand, there are two parameters left that can be adjusted to obtain suitable  $L$  and  $C$  values. These are;

- $s$ ; the width of one of the walls forming the iris (Figure 3.7)
- $C_{\text{lumped}}$ ; lumped capacitor value, placed next to the diode.

Lumped capacitor can be incorporated in linear simulation to decrease the number of EM simulations. EM simulation is done with 3 ports; 2 waveguide ports at the input and output of the structure and a lumped port at the place of lumped capacitor in the structure. 2-port S-parameters of the structure can be obtained by connecting a lumped capacitor to the related port of the 3-port S-parameters of the test structure using a linear simulator. This calculation is done using an in-house computer code instead of the linear simulator to work more efficiently. By this way S-parameters of the test structure for a fixed  $s$  value can be obtained for any value of lumped capacitor by a single EM simulation. After the 3-port S-parameter simulations for multiple values of  $s$  are done, all simulation data would be available to calculate  $s$  and  $C_{\text{lumped}}$  values that will give required  $C_{\text{eq}}$  and  $L_{\text{eq}}$  values.

Simulations are done with the parameters given in Table 3.1.

**Table 3.1** Simulation parameters for the modeling of discontinuity

Parameter	Value
Dielectric in EWG section	RO4003
Dielectric in Input & Output sections	Alumina
Total EWG length	10cm
Waveguide width	8mm
Waveguide height	0.5mm
$C_{lumped}$	0.7pF
s	2.1mm

In addition to these parameters, the DC block capacitors between the anode of the diode and the upper wall of the waveguide are modeled as parallel plate 28pF capacitor. The capacitor has 10mil square plates and 4mil height. The diode is modeled also as parallel plate capacitor with width of 5mils and height of 4mil. The relative permittivity of the dielectric of this capacitor is adjusted such that the capacitance is 0.1pF which is the junction capacitance of the diode taken from the datasheet.

The plot of  $j\omega Y$  vs.  $\omega^2$  is shown in Figure 3.8 with the line fit calculated near the operating frequency (8.5 GHz,  $\omega^2=2.85e21$ ). This line or the data points of the plot itself can be used to calculate the  $C_{eq}$  and  $L_{eq}$  values.

For the same parameters except  $C_{lumped}$ ,  $C_{eq}$  and  $L_{eq}$  values are calculated for different values of  $C_{lumped}$ , and  $C_{eq}$  vs  $C_{lumped}$  and  $L_{eq}$  vs  $C_{lumped}$  are plotted in Figure 3.9. A single EM simulation data is used for this plot.

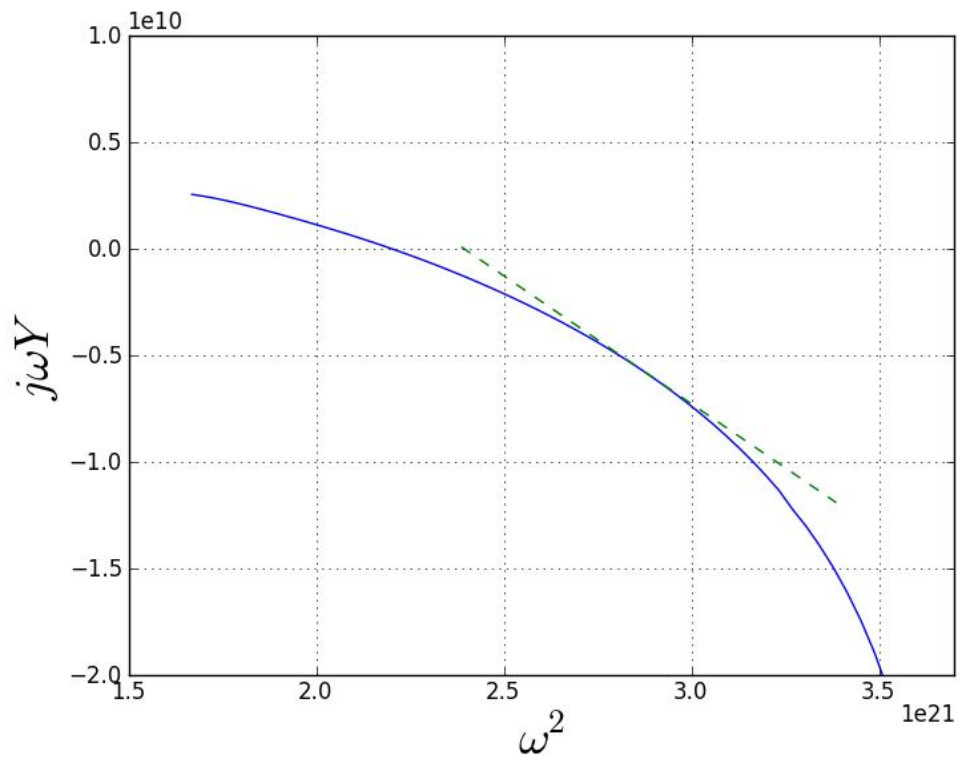


Figure 3.8  $j\omega Y$  vs.  $\omega^2$  plot with  $s=2.1\text{mm}$  and  $C_{\text{lumped}}=0.7\text{pF}$ .

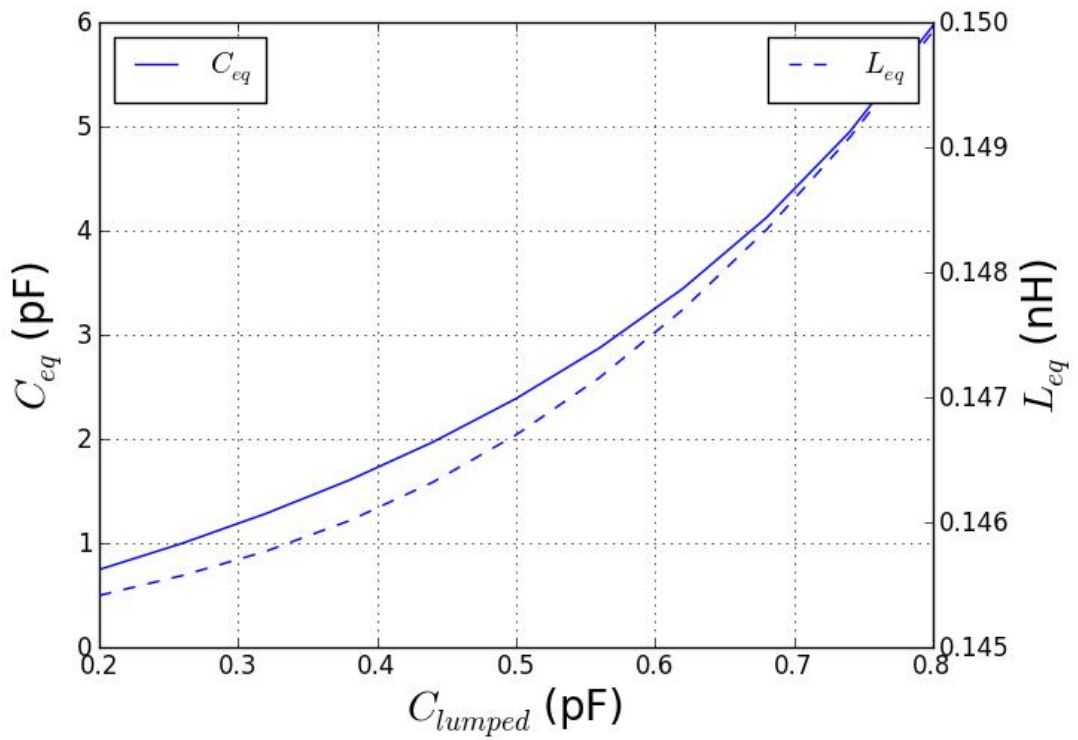
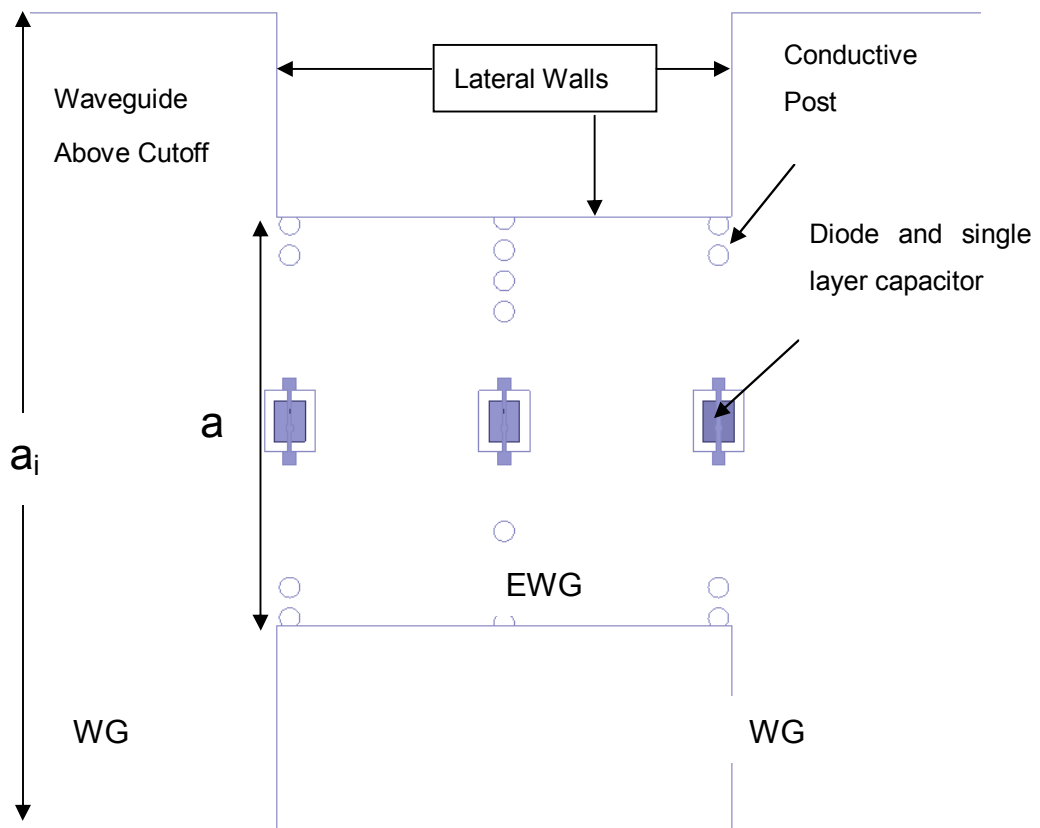


Figure 3.9  $C_{\text{eq}}$  and  $L_{\text{eq}}$  vs.  $C_{\text{lumped}}$

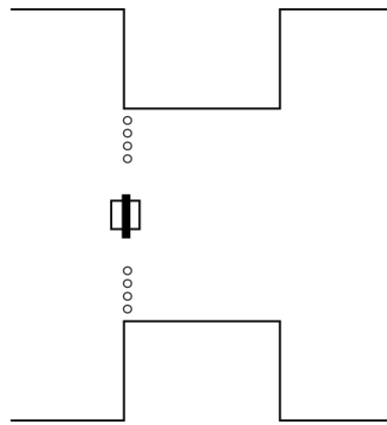
In these simulations pin diode is modeled as a parallel plate capacitor with the value equal to the reverse bias capacitance of the diode. An alternative approach is using another lumped port instead of pin diode. By this way a 4-port S-parameters are calculated by EM simulation and a more detailed lumped diode model can be used while using linear simulator to obtain 2-port S-parameters. But since the series impedance of the diode is very small, this approach is not used.

For simplicity a 3<sup>rd</sup> order filter will be used as the basis of the switch. Top view of a 3<sup>rd</sup> order switch design using this discontinuity type to implement the shunt resonators is shown in Figure 3.10. This view is taken from the simulation program HFSS<sup>®</sup>. Lateral walls are shown as smooth continuous walls as used in EM simulations.

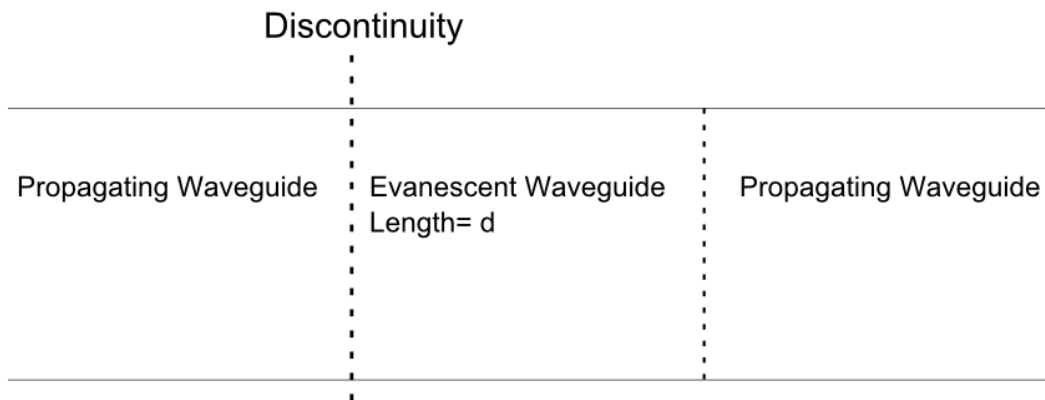


**Figure 3.10** Top view of a 3<sup>rd</sup> order evanescent mode waveguide switch

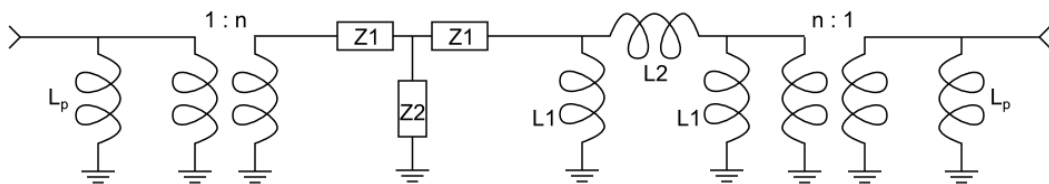
The method described so far in this part can be used for any discontinuity of the filter except the first and last ones. Since the first and last resonators are on the waveguide junction (Figure 3.11), field distribution might be very different than the other discontinuities. So they should be treated differently. For those resonators, the test structure shown in Figure 3.12 can be used. The equivalent circuit of this structure is shown in Figure 3.13.



**Figure 3.11** Top view of a resonator that is at the junction of waveguides



**Figure 3.12** Test model for the discontinuity at the waveguide junction

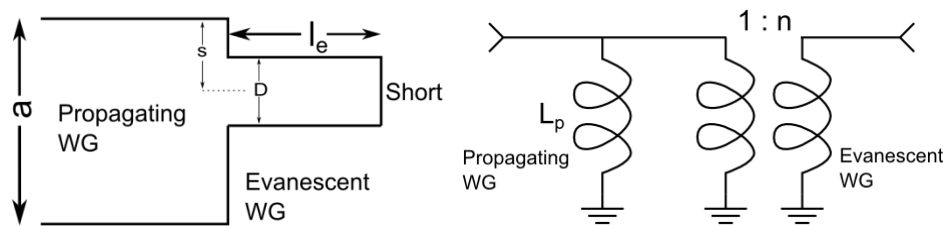


**Figure 3.13** Test circuit for the discontinuity at the waveguide junction

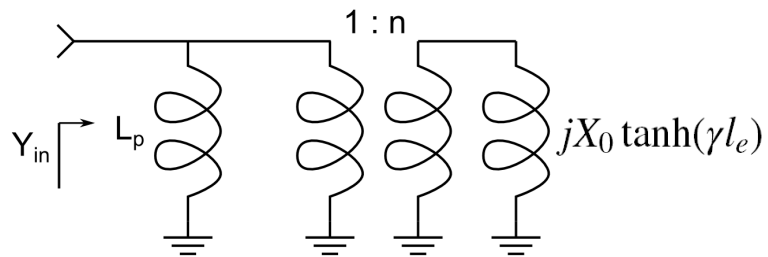
The remaining details are very similar to the modeling of other resonators and will not be repeated here.

### 3.6 Analysis of Waveguide Junction

The equivalent circuit of a waveguide junction is given in Figure 3.14 [49]. Although the parameters  $n$  and  $L_p$  can be calculated in closed form for simple structures, they are not available for all waveguide configurations. A better way to calculate them is using 3D EM simulation. A method similar to the one described in [48] is used. Consider the test structure in Figure 3.14, for which lumped element equivalent circuit is given in Figure 3.15.



**Figure 3.14** Test structure to calculate waveguide step parameters



**Figure 3.15** Lumped element representation of test structure

Input admittance of this structure is given in (3-6). There are two unknowns here, so two equations are needed which can be obtained using two different values of  $l_e$ . Two input admittance values are obtained for two different values of  $l_e$  by 3D EM simulation. Then  $n$  and  $L_p$  values can be calculated using the equations (3-7) and (3-8).



$$Y_{in} = \frac{1}{j\omega L_p} + \frac{n^2}{jX_0 \tanh(\gamma l_e)} \quad (3-6)$$

$$n^2 = \frac{Y_{in1} - Y_{in2}}{\frac{1}{jX_0 \tanh(\gamma l_{e1})} - \frac{1}{jX_0 \tanh(\gamma l_{e2})}} \quad (3-7)$$

$$L_p = \frac{1}{j\omega Y_{in1} - \frac{n^2}{jX_0 \tanh(\gamma l_{e1})}} \quad (3-8)$$

where;

$jX_0$ : evanescent mode waveguide impedance

$\gamma$ : propagation constant in evanescent mode waveguide

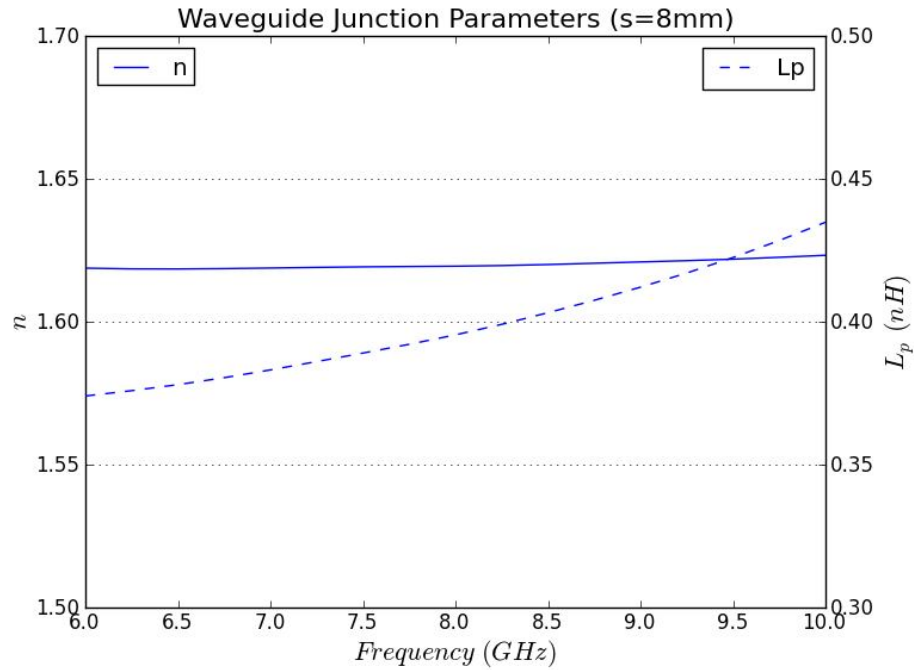
For these calculations,  $l_{e1}$  and  $l_{e2}$  should not be chosen too large. For large values of  $l_e$  input admittance becomes almost independent of  $l_e$ , because field is decaying in evanescent waveguide. For too large values of  $l_{e1}$  and  $l_{e2}$ , due to numerical precision problems, it is difficult to discriminate between two different values of  $Y_{in}$  and calculate  $n$  and  $L_p$ .

$n$  and  $L_p$  values are calculated by simulation using the parameters given in Table 3.2.

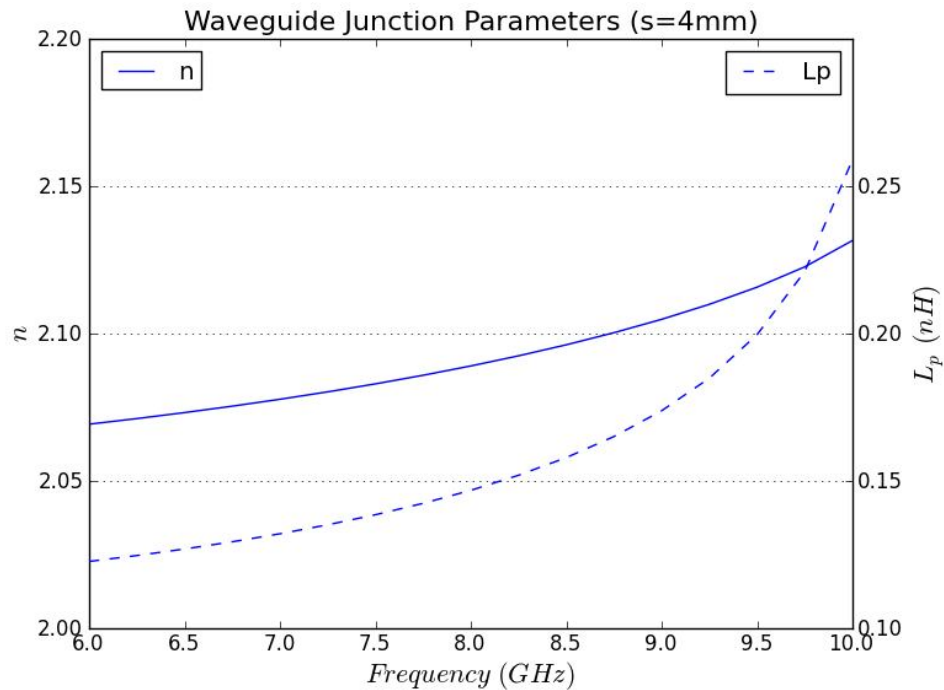
**Table 3.2** The parameters used to calculate  $n$  and  $L_p$  values

Parameter	Value
Dielectric material	RO4003
Waveguide Width (a)	16mm
Evanescent Waveguide Width (D)	8mm
Evanescent Waveguide Length 1 ( $l_{e1}$ )	2mm
Evanescent Waveguide Length 2 ( $l_{e2}$ )	5mm
Waveguide Height (h)	0.5mm

Simulations are done for symmetric ( $s=8\text{mm}$ ) and fully asymmetric cases ( $s=4\text{mm}$ ). Simulation results are shown in Figure 3.16 and Figure 3.17. As shown in the plots  $n$  and  $L_p$  values do not change much with frequency which justifies the filter design procedure outlined in the previous chapter.



**Figure 3.16**  $n$  and  $L_p$  values versus frequency for symmetric junction



**Figure 3.17**  $n$  and  $L_p$  values versus frequency for asymmetric junction

### **3.7 Conclusion**

In this chapter, details about the implementation of the RF switch are given. Modeling begins with developing a discontinuity structure that will form the shunt resonators of the filter and a diode mounting topology. A discontinuity structure which is easy to manufacture using standard PCB and chip&wire technology and a suitable way to embed diode in this structure is devised. A method to calculate the equivalent circuit of this discontinuity using 3D EM simulation is developed. Another method to calculate the equivalent circuit waveguide transitions at both ends of the filter using 3D EM simulation is also described.

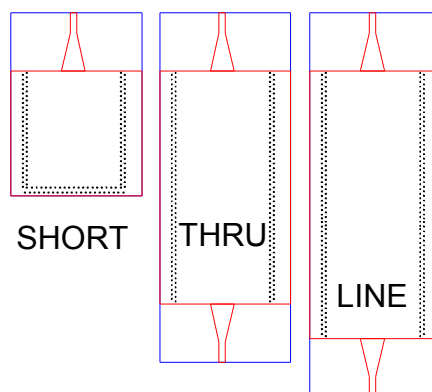
In the next chapter, an SPST and an SPDT RF SIW switches are designed, prototyped and measured to test the theory and assess the performance of the SIW RF switch.

## CHAPTER 4

### DESIGN EXAMPLES OF RF SWITCH IN SIW

#### 4.1 Introduction

In this chapter, an SPST and an SPDT RF switches in SIW are designed using the technique described in previous chapter. The switches are prototyped and measured. The measurements are done with a network analyzer using coaxial connectors. So at the input and output of the switch, there are microstrip-SIW transitions. These transitions are de-embedded using TRL calibration. A TRL calibration kit specifically designed for this purpose are produced and used. TRL kit includes SHORT, THRU and LINE standards and every standard includes the same coaxial to microstrip and microstrip to SIW transitions that are used at the switch prototypes. The length of LINE is optimized for 8.5GHz. The drawings of TRL kit are shown in Figure 4.1. An in-house computer code is written for de-embedding using [52] as reference.



**Figure 4.1** Drawings of TRL calibration kit

## 4.2 SIW Parameters and Microstrip Transitions

Before building the prototypes, parameters of substrate integrated waveguide should be determined and tested. The aim is to design a switch between 8-9GHz and at the highest frequency of operation (9GHz) wavelength in RO4003 is 18.1mm. So 0.4mm diameter which is the smallest via diameter that can be achieved at the prototyping apparatus is enough. The gap between the vias is also 0.4mm. Several rows of vias with increasing separations are used to decrease radiation loss from lateral walls.

A microstrip to SIW transition is designed by optimization in 3D simulator to be able to measure the switch using coaxial connectors. These transitions will be used at the input and output of the switch. To test these SIW parameters and microstrip-SIW transition a thru line is produced and measured. The structure is shown in Figure 4.2 and the response is shown in Figure 4.3. The ripples in  $S_{11}$  and  $S_{21}$  are caused by imperfect microstrip-SIW transitions as can be deduced from the length of SIW and frequency period of ripples. These transitions will be de-embedded at the switch measurements. Insertion loss is around 1.5-2.0dB.

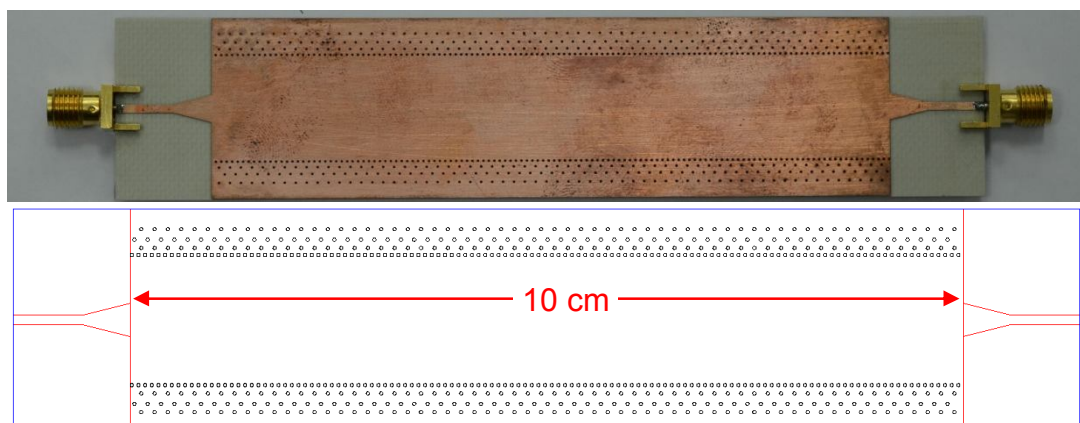
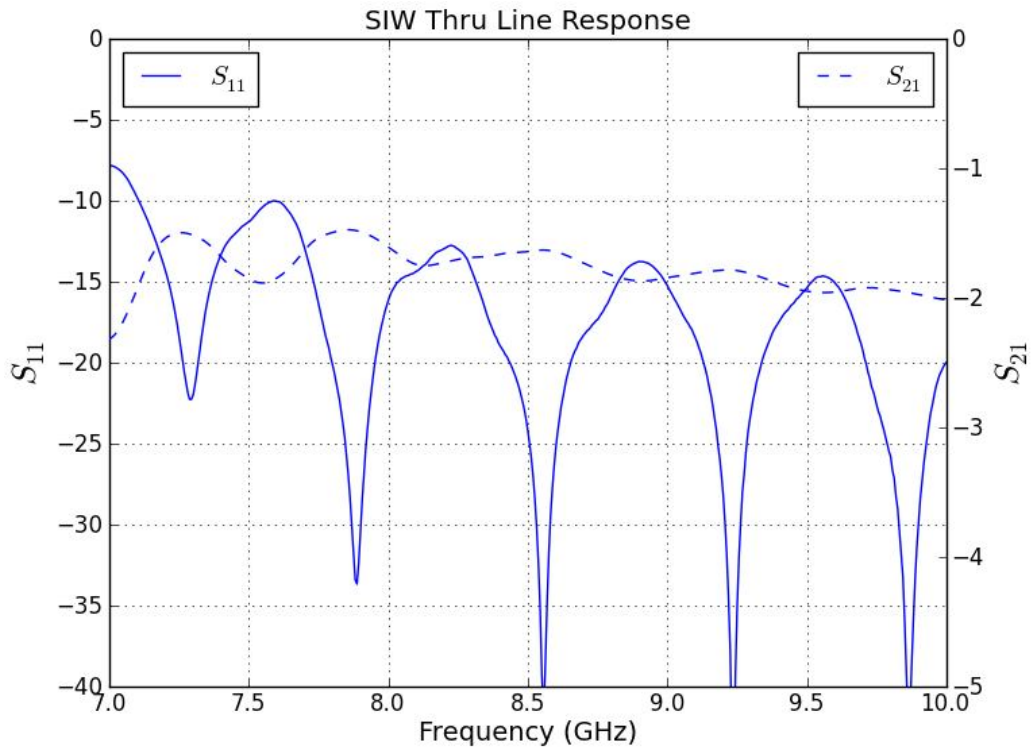


Figure 4.2 Drawing and Photograph of SIW thru line



**Figure 4.3** Measured response of SIW thru line

## 4.3 SPST

### 4.3.1 Design of SPST

A prototype SPST switch based on a 3<sup>rd</sup> order evanescent mode band pass filter is designed using the technique summarized in the previous chapter. The properties of the substrate and filter used are given in Table 4.1.

**Table 4.1** Substrate and filter properties of SPST

Dielectric material	RO4003
Height	0.5mm
Width of input and output waveguides	16mm
Center frequency	8.5GHz
Fractional Bandwidth	0.12

The first step is to design the band pass filter with ideal elements using the equations given in Appendix A. Chebyshev type will be used in this switch. The width of the evanescent mode waveguide sections is chosen to be 8mm. In a 3<sup>rd</sup> order filter, the value of the second capacitor is arbitrary and it is chosen such that  $C_2/C_1$  ratio is 0.8. This mainly affects the realizability of the filter, because for some capacitor values, inductor values cannot be realized accurately. Using the equations given in Appendix A, the length of the evanescent mode sections, inductances and capacitances are calculated. These capacitance values can be tuned a little to compensate for the frequency dependence of waveguide junction parameters ( $n$ ,  $L_p$ ), but in general it is not necessary. Frequency dependent values of  $n$  and  $L_p$  are given in Figure 3.16. The capacitance and inductance values and the length of evanescent mode waveguide sections are calculated as following:

$$C_1 = 4.55 \text{ pF} \quad (\text{Capacitor of first resonator})$$

$$L_1 = 0.098 \text{ nH} \quad (\text{Inductor of first resonator})$$

$$C_2 = 3.64 \text{ pF} \quad (\text{Capacitor of first resonator})$$

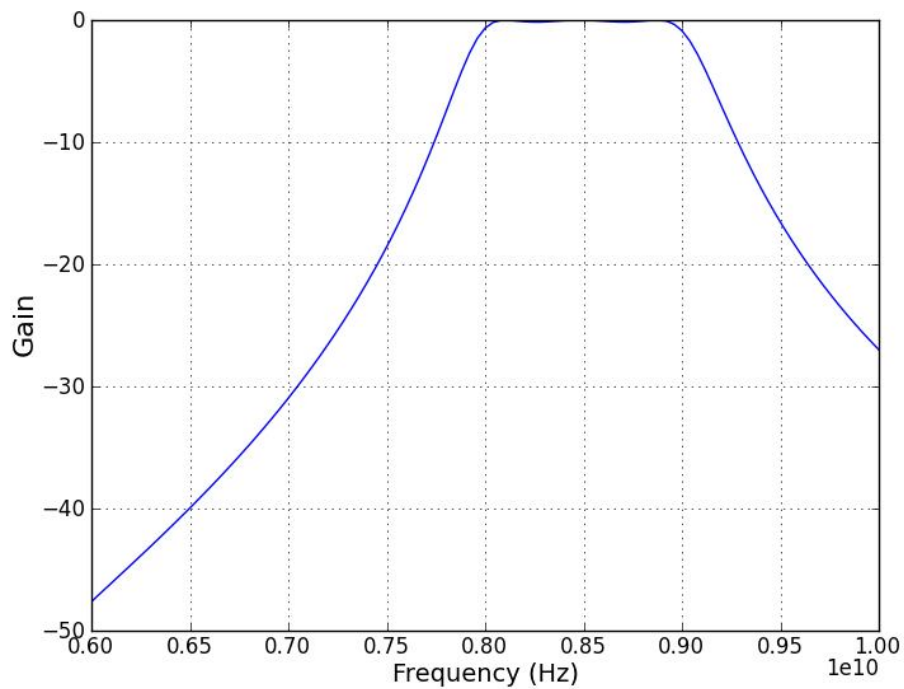
$$L_2 = 0.148 \text{ nH} \quad (\text{Inductor of first resonator})$$

$$d = 4.58 \text{ mm} \quad (\text{Length of evanescent mode waveguide section})$$

The ideal filter response corresponding to these values is given in Figure 4.4.

The next step is to find the offset (parameter “s” in Figure 3.7) and lumped capacitor ( $C_{\text{lumped}}$ ) values corresponding to these capacitance and inductance values. At the modeling stage, effective inductance ( $L$ ) and capacitance ( $C$ ) values for discrete values of  $s$  and  $C_{\text{lumped}}$  are obtained by 3D full-wave simulation and separate datasets for inductance ( $L(s, C_{\text{lumped}})$ ) and capacitance ( $C(s, C_{\text{lumped}})$ ) are generated. 2-D interpolation on these datasets can be used to obtain  $L$  and  $C$  values for any value of  $s$  and  $C_{\text{lumped}}$ . On the other hand, inverse of these datasets ( $s(L,C)$  and  $C_{\text{lumped}}(L,C)$ ) can be generated and 2-D interpolation on these datasets can be used to obtain  $s$  and  $C_{\text{lumped}}$  directly. The offset for the center resonator is

found to be close to 2.1mm and lumped capacitor value is found to be close to 0.63pF.  $C_{eq}$  vs  $C_{lumped}$  and  $L_{eq}$  vs  $C_{lumped}$  are given in Figure 3.9. The offset for the first resonator is similarly found to be approximately 0.9mm and its lumped capacitor value is approximately 0.5pF.  $C_{eq}$  vs  $C_{lumped}$  and  $L_{eq}$  vs  $C_{lumped}$  are given in Figure 4.5 for 0.9mm offset. As the lumped capacitors, Di-Cap type single layer capacitors (SLC) are used from Dielectric Laboratories (DLI) [59].



**Figure 4.4** Gain of the ideal filter

A 3-D simulation model is constructed using these offset values in HFSS. Lumped ports are placed instead of lumped capacitors of resonators. This 5-port structure can be used to find the final capacitor values. EM simulation result of this 5-port structure is imported in a linear circuit simulator, and the capacitors connected to lumped ports are optimized to find the final capacitor values. After the optimization both lumped capacitor values are increased by approximately 0.05pF. The final response is shown in Figure 4.6. In this simulation, all materials are assumed to be lossless.



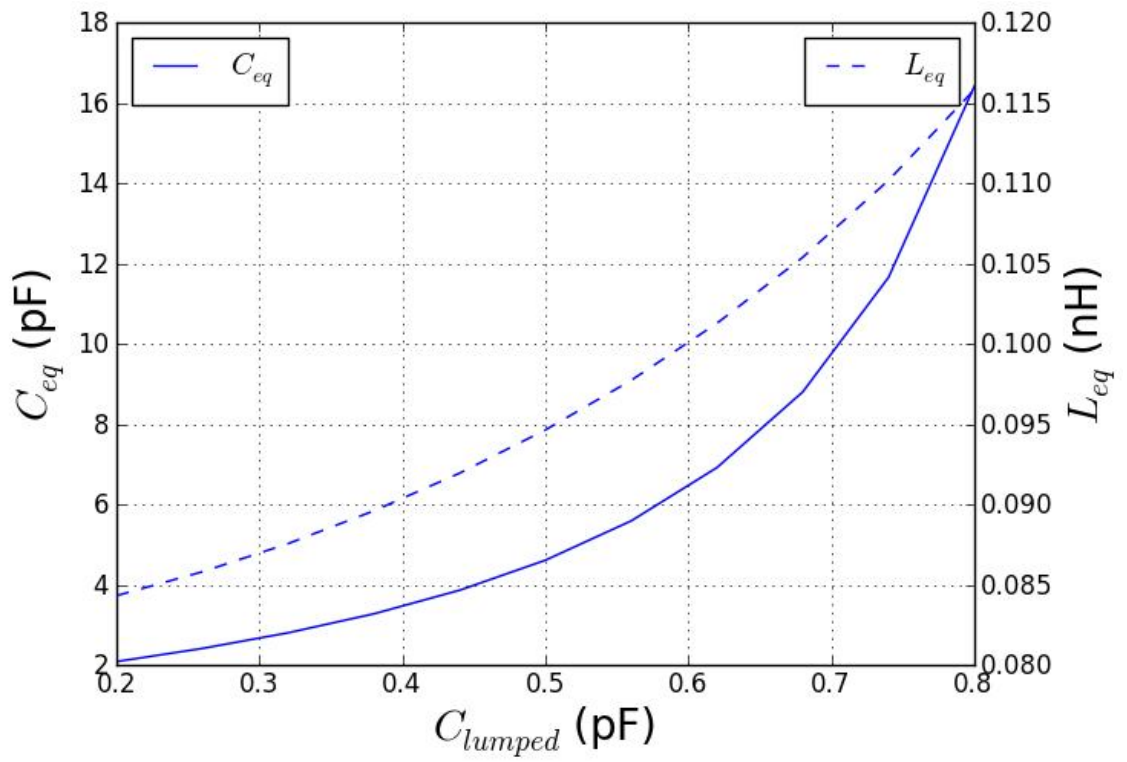


Figure 4.5 Modeling data for offset 0.9mm

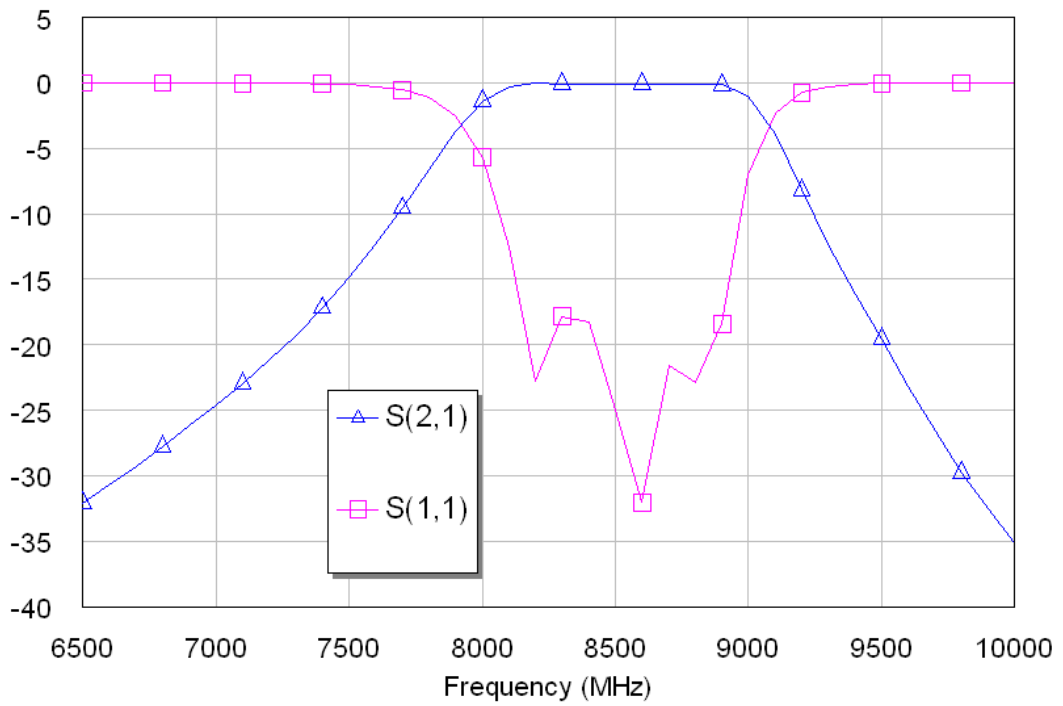
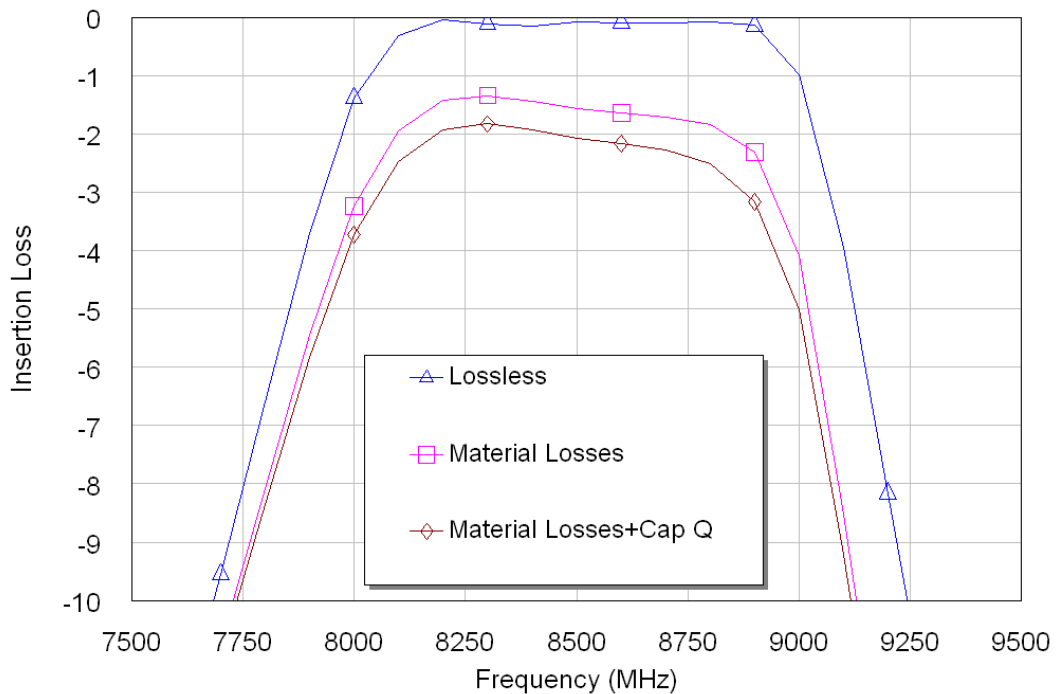


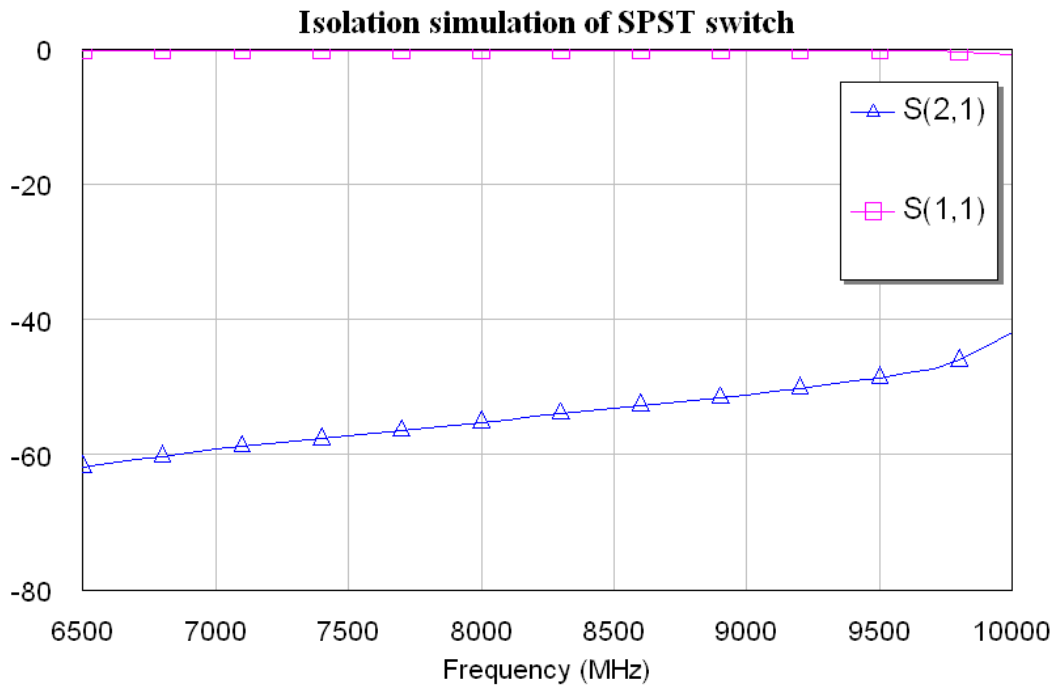
Figure 4.6 Final filter response

Initial simulations of SPST switch are done using lossless materials to decrease computer simulation time. At the final stage, two simulations with lossy materials are done. At the first one, copper waveguide walls, gold wires and lossy RO4003 material is used and this simulation is labeled as “Material Losses” in Figure 4.7. Diode and lumped capacitors are modeled as ideal capacitors in this first simulation. At the second one, series resistance of the diodes and lossy ideal model of lumped capacitors are added and this simulation is labeled as “Material Losses+Cap Q” in Figure 4.7. Capacitors are modeled according to DLI Di-Cap model [57] which is the capacitor model used in prototypes. According to these simulations, major part of the insertion loss comes from dielectric and conductor losses in the waveguide.

Isolation of the SPST switch is also simulated by modeling the diode with only its series parasitic resistance. The result is shown in Figure 4.8.



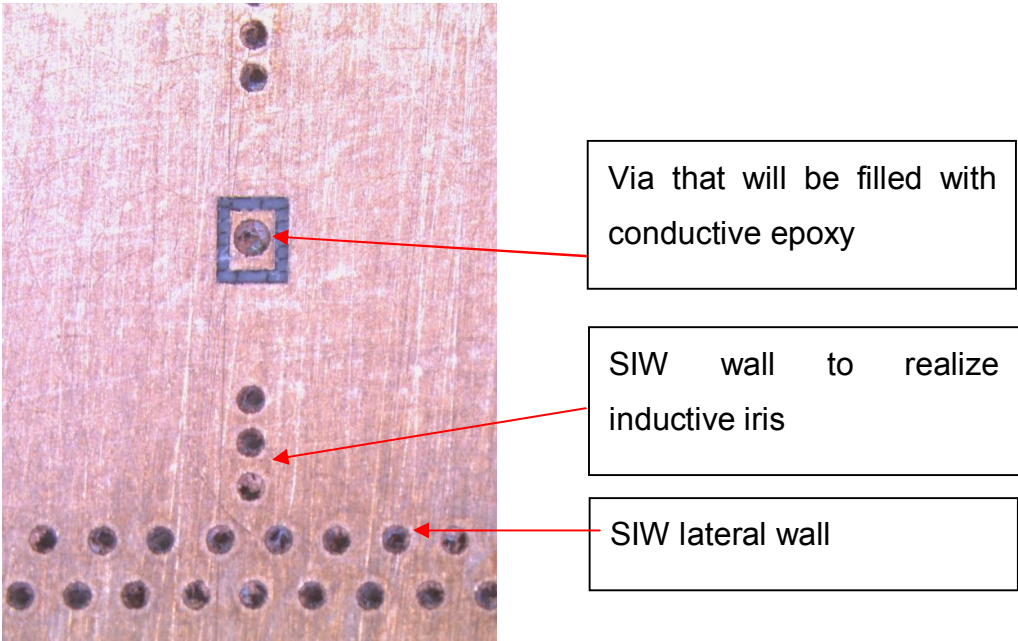
**Figure 4.7** Lossy simulation results of SPST



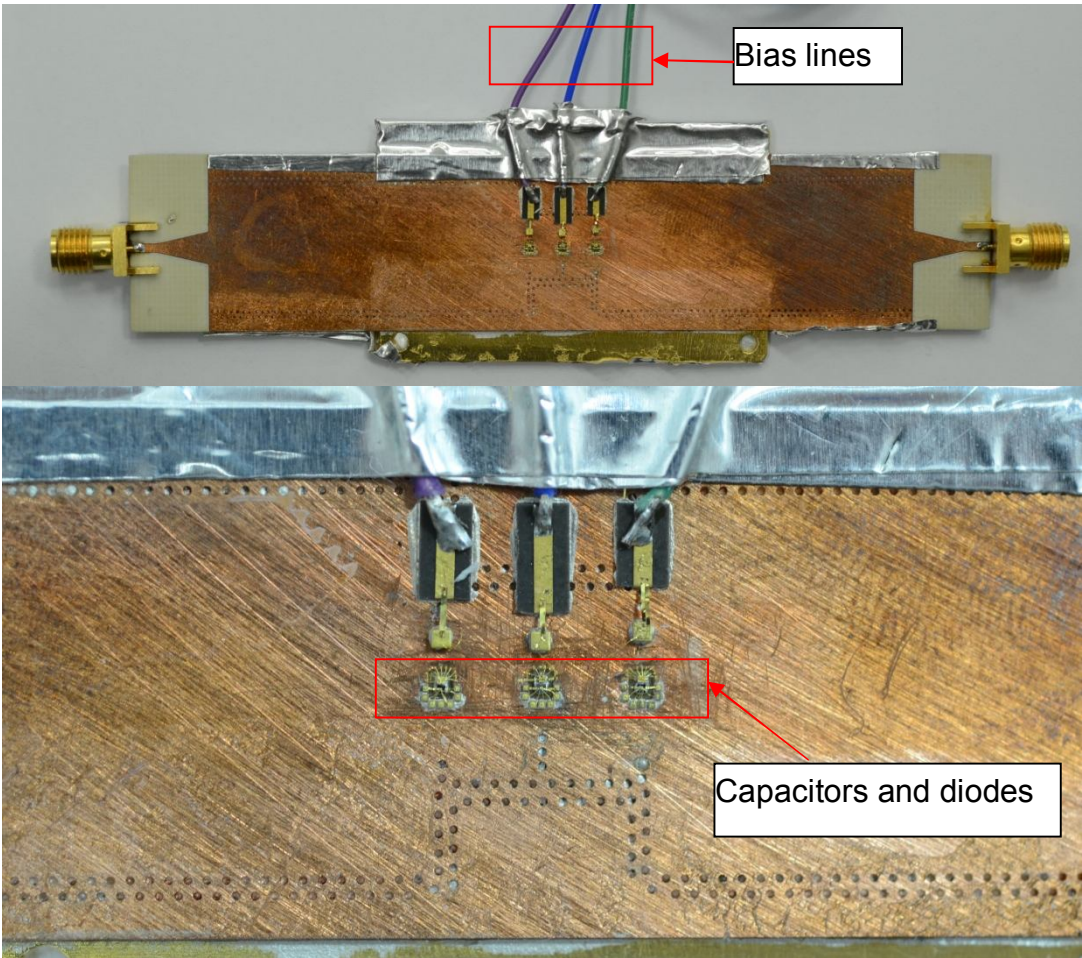
**Figure 4.8** Simulation result of SPST in isolation mode

### 4.3.2 Prototyping and Measurements of SPST

A prototype of SPST is built with microstrip-SIW transitions at the input and output of the circuit. These transitions are de-embedded using the TRL calibration kit that is designed for this work. A photograph of the discontinuity to realize a resonator before the mounting of diode and capacitors is shown in Figure 4.9. Before mounting the diode and capacitors, the via at the center is filled with conductive epoxy after attaching a metal piece to the board from bottom side. This method is used to build the prototype because a facility to make filled vias was not available during the prototyping stage. At production, it is best to use copper-filled vias because a much smoother surface can be obtained to mount diodes and capacitances on. A photograph of the prototype is shown in Figure 4.10.



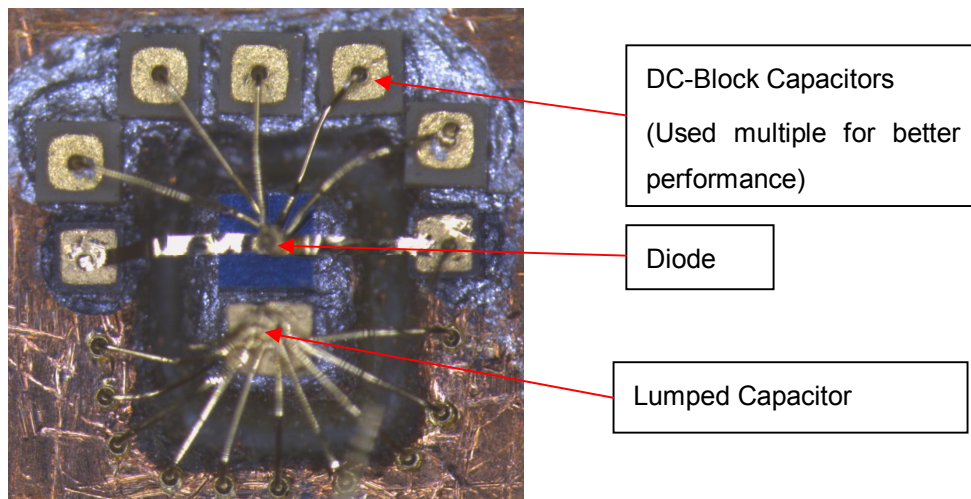
**Figure 4.9** Photograph of the discontinuity before the mounting of diode and capacitors



**Figure 4.10** Photograph of 3<sup>rd</sup> order SPST switch prototype

### 4.3.2.1 Linear Response

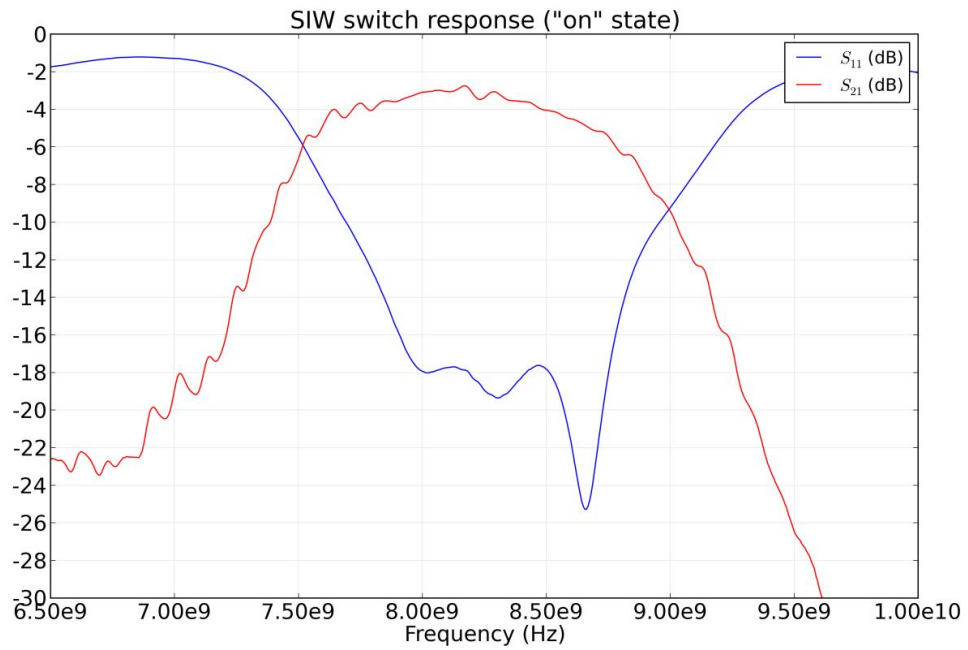
Insertion loss measurement of the SPST switch is shown in Figure 4.12. According to this measurement, the center frequency of the switch is somewhat shifted to lower frequencies. The reason should be that only lumped capacitor values which are an integer multiple of 0.1pF could be used at the prototypes. It is not possible to find any value as a single layer capacitor. So the capacitance values are rounded to the nearest higher capacitance value available. As will be pointed out in the next chapter, center frequency is very sensitive to capacitor values and some mechanism to tune the capacitor at the testing stage should be implemented. Insertion loss is 1dB higher than expected. The reason for this difference could be poor prototyping or poor modeling of the lumped capacitor and diode. Number of connections on diode and lumped capacitor are increased which resulted in 1-2dB performance improvement. Photo of the connected diode and capacitor is shown in Figure 4.11.



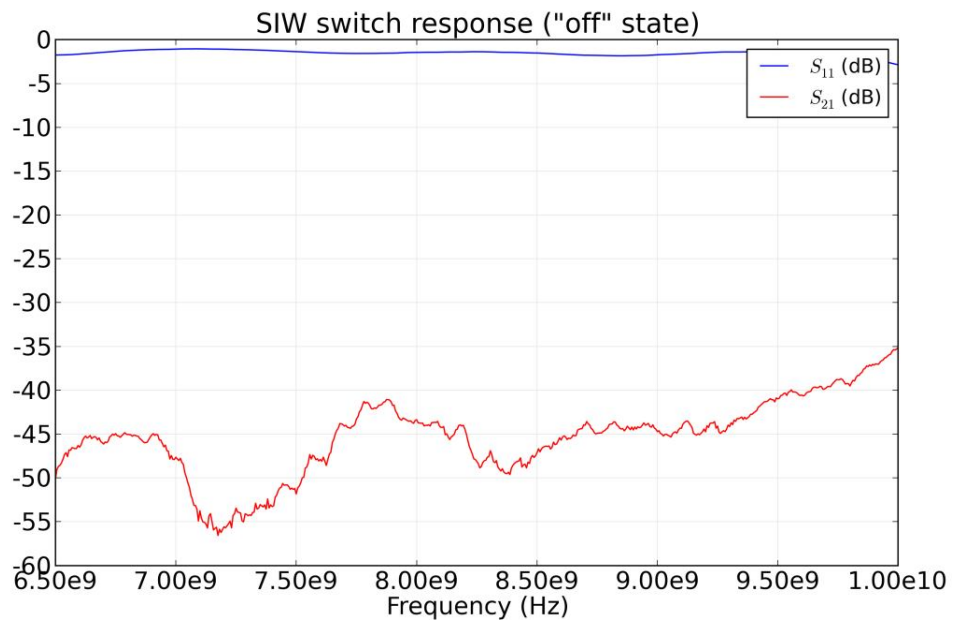
**Figure 4.11** Photo of diode and capacitor mounted next to each other

Isolation of the switch is measured by injecting a total of 15mA current to each diode. The measurement result is shown in Figure 4.13. The measurement result is close to simulation result shown in Figure 4.8.





**Figure 4.12** Linear measurement result of SPST at “on” state



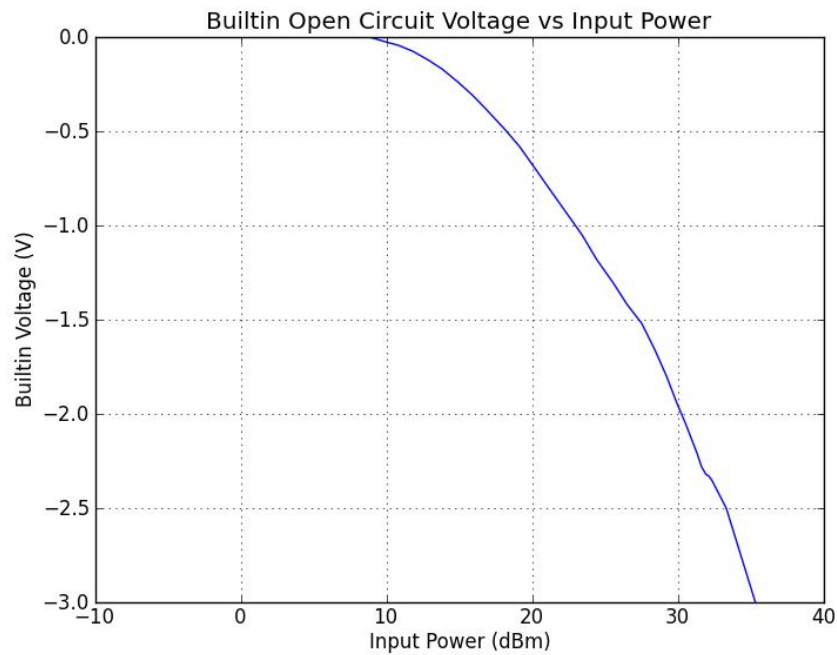
**Figure 4.13** Linear measurement result of SPST at “off” state

#### 4.3.2.2 1-dB compression point

1-dB compression point is measured at 8.5GHz. In the “on” state, 1-dB compression point of pin diode RF switches is strongly related to the reverse bias voltage applied to diodes. 1-dB compression point increases

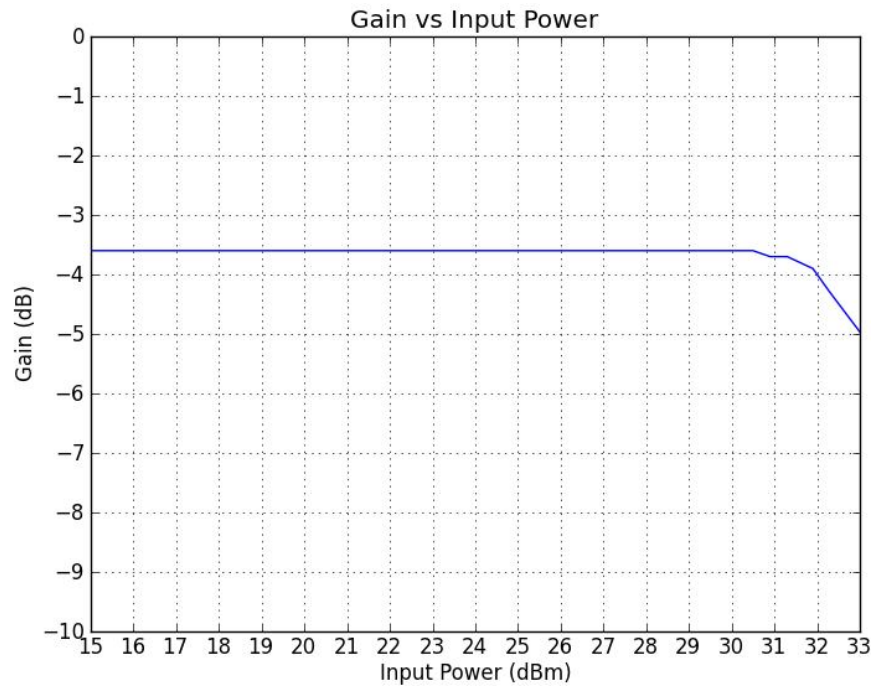
with applied reverse voltage. For a 1-dB compression point specification, minimum reverse voltage that should be applied can be measured by the method described in [58]. In this case, all three diodes are reverse biased with the same voltage for easier biasing. Built-in voltage vs. input power is measured using that method (Figure 4.17) and it is seen that -5V reverse bias is enough for minimum 30dBm 1-dB compression point although peak RF voltage corresponding to 30dBm is 10V.

SPST switch is confirmed to work up to 40dBm without damage at room temperature.



**Figure 4.14** Built-in voltage on the pin diodes vs input power

Gain vs. input power is measured and plotted in Figure 4.15. Input 1-dB compression point is measured as 32.8dBm.



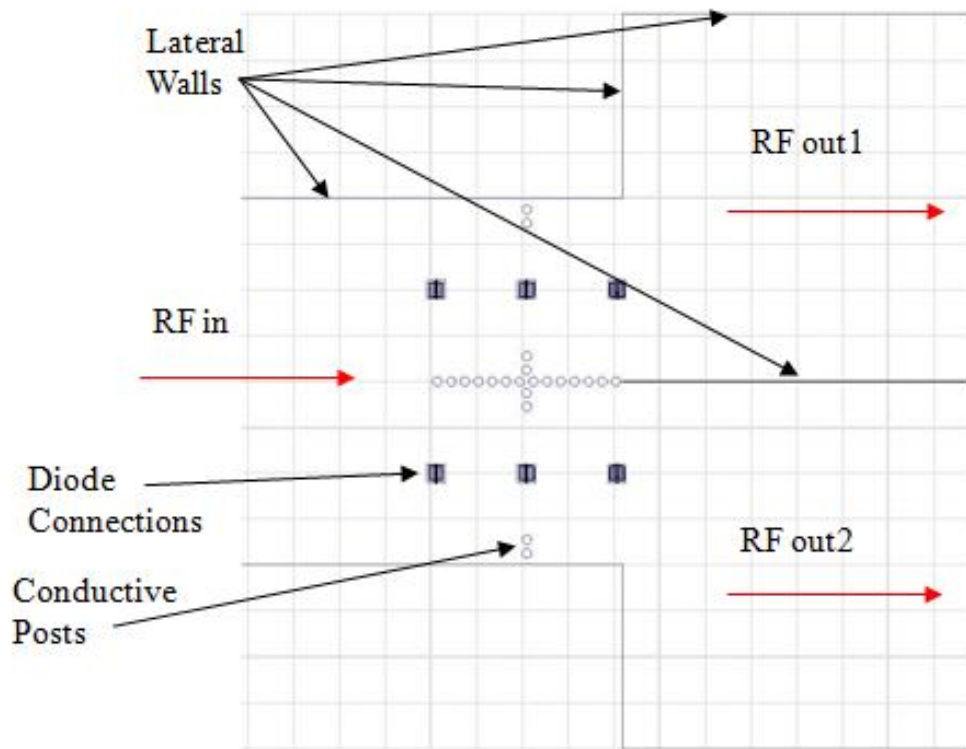
**Figure 4.15** Gain vs. input power measurement result of SPST

## 4.4 SPDT

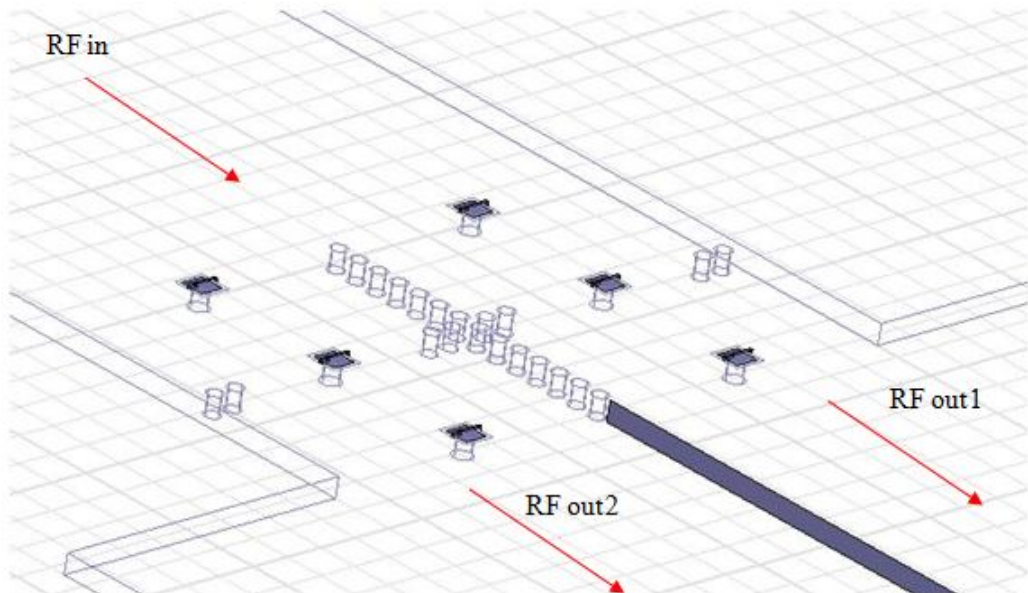
The same method can be used to design an SPDT switch. The layout of the SPDT is shown in Figure 4.16 and a 3D view is given in Figure 4.17 for clarity. In the simulations conventional lateral walls are used due to insufficient computer resources. A final simulation can be done after replacing these walls with metalized vias.

The closed arm of the switch presents a nearly short circuit at the first and last resonators. So the open arm can be considered as an SPST switch with fully asymmetric input and output waveguide transitions. The design methodology is the same as SPST except the values of the waveguide transition parameters. The simulation result is shown in Figure 4.18.





**Figure 4.16** Top view of the simulation model of the SPDT switch



**Figure 4.17** 3D view of the simulation model of the SPDT switch

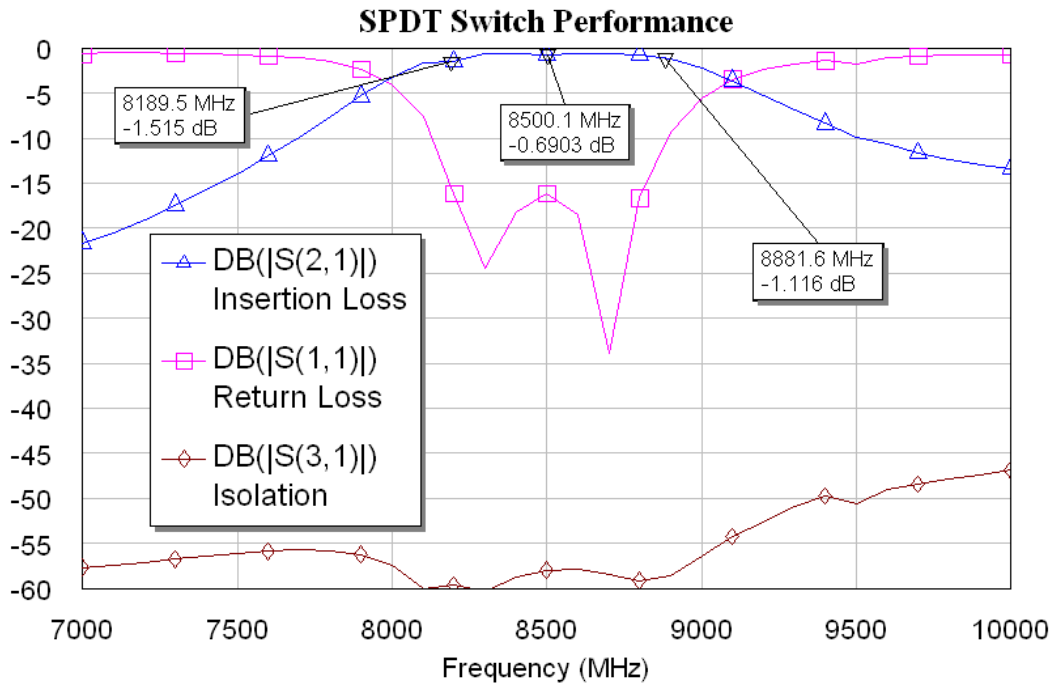
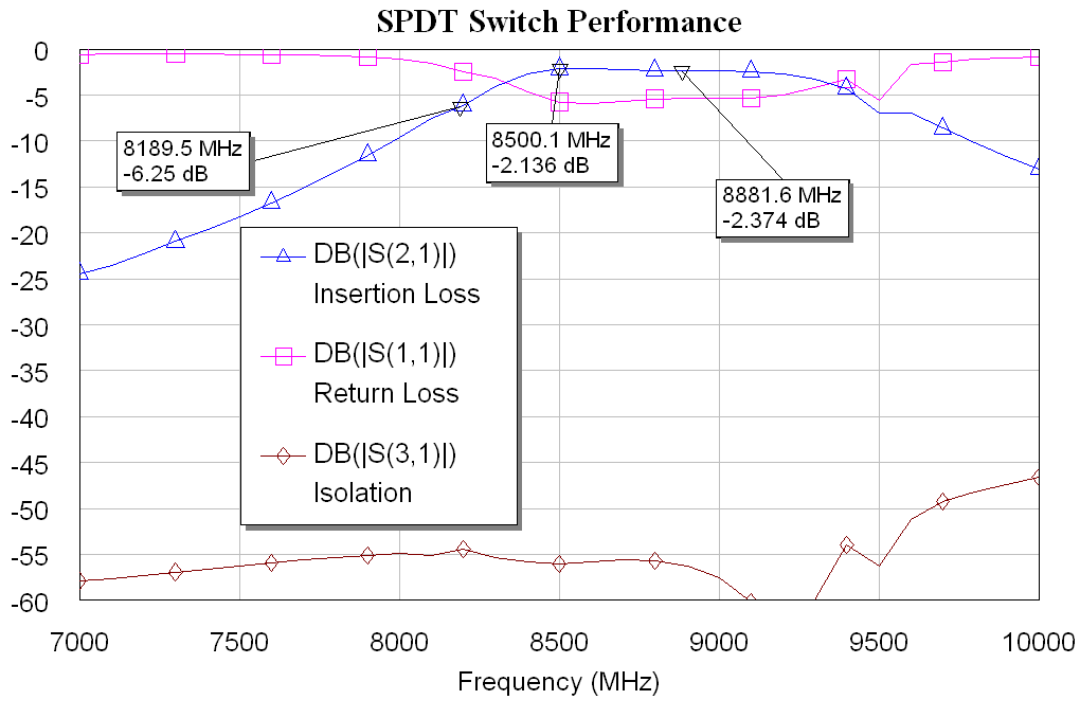


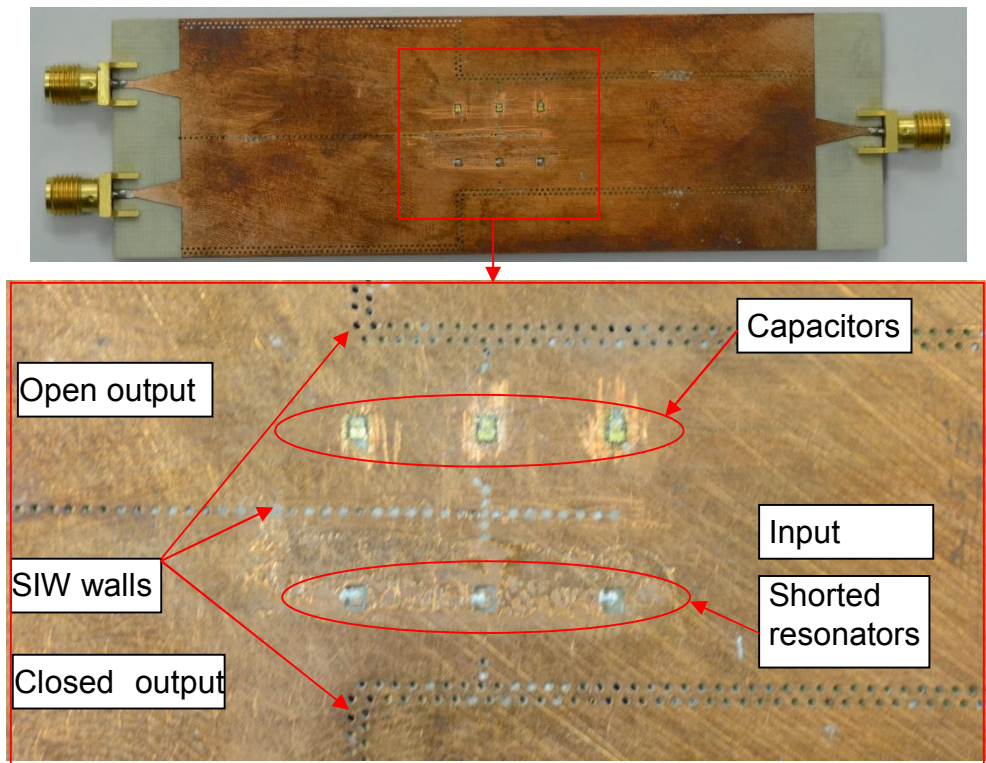
Figure 4.18 Performance of SPDT switch “on” and “off” branches

For a center frequency of 8.5GHz, lumped capacitor values should be 0.56pF and 0.48pF. Available off-the-shelf lumped capacitors are integer multiples of 0.1pF. So a prototype with capacitor values 0.5pF and 0.4pF is measured and compared with the simulation result with the same capacitor values. Due to this capacitor change, filter response, which is shown in Figure 4.19, is distorted.

The prototype built is shown in Figure 4.20. This prototype is built without diodes and bias lines to easily test the performance, so that one arm was always on, while the other one was always off. Only chip capacitors are used at the resonators of the open arm and the resonators of closed arm are short circuited by conductive epoxy as shown in Figure 4.20.

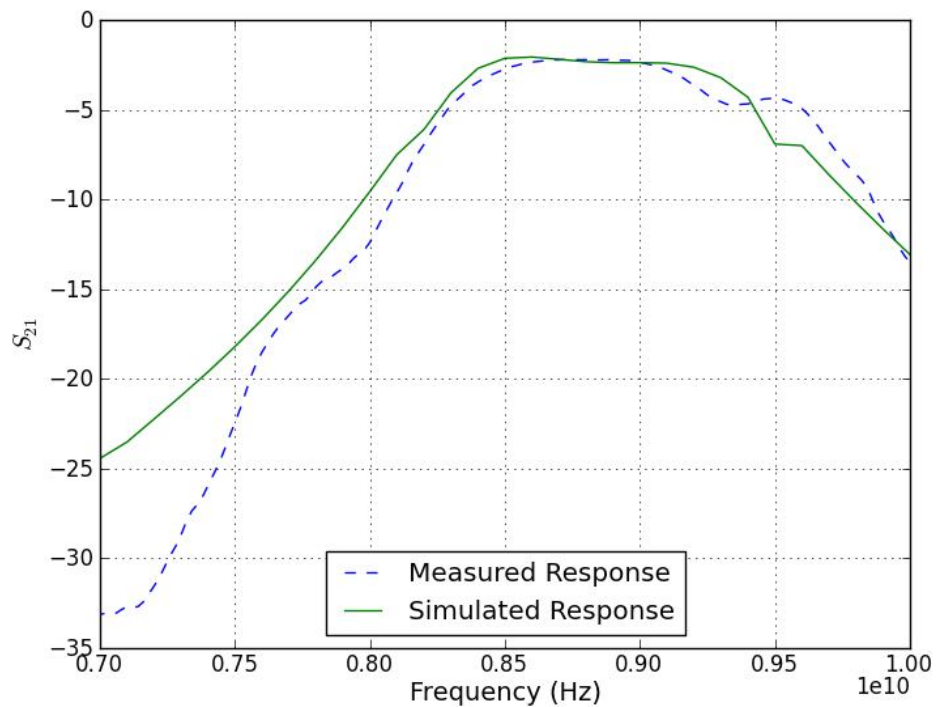


**Figure 4.19** Performance of SPDT switch “on” and “off” branches with modified capacitors



**Figure 4.20** Photograph of SPDT without bias lines and diodes

The measured and simulated gains of the switch are plotted together at Figure 4.21. Measured and simulated results are fairly close to each other. Since the capacitor values had to be changed during prototyping, filter response is distorted and the deterioration in the insertion loss simulation is mainly caused by the deterioration in the return loss instead of resistive losses. Return loss is only around 5dB as shown in Figure 4.19.



**Figure 4.21** Measured and simulated gain of open arm of SPDT switch with  $C_1=0.5\text{pF}$  and  $C_2=0.4\text{pF}$

## 4.5 Conclusion

In this chapter, design examples are given for an SPST and an SPDT switch. Both switches are built and measurement results of both are given. In addition to linear measurements, 1-dB compression point and maximum input power of SPST is measured for the sake of completeness.

The linear measurement results of these prototypes confirm the general design method developed in the previous chapter.

These RF switches have comparable performances in terms of isolation and return loss, with broadband microwave switches designed for use in microstrip, although a narrow band microstrip switch with better isolation can be designed with three diodes per arm. Insertion loss seems higher than microstrip counterparts, but this switch also has filtering functionality which partly justifies high insertion loss and can be used at SIW systems that require an RF filter in series with the switch. SIW switch is also much bigger than microstrip switches which can also be justified with the existence of a filter.

Considering the wide availability and high performances of microstrip filters and switches, and the need for microstrip-SIW transitions, the circuit structure explained in this thesis should be considered primarily for SIW circuits instead of microstrip circuits.

## CHAPTER 5

### OTHER APPLICATIONS OF PIN DIODES IN SIW

#### 5.1 Introduction

In this chapter, some different applications of this structure will be described. The circuits that are realized using shunt diodes in microstrip, can also be realized in SIW using this structure. One such circuit, namely RF power limiter is described in the first part of this chapter. The diodes are also part of the capacitances of the filter, so varactor diodes can be used to design a tunable filter which is described in the second part.

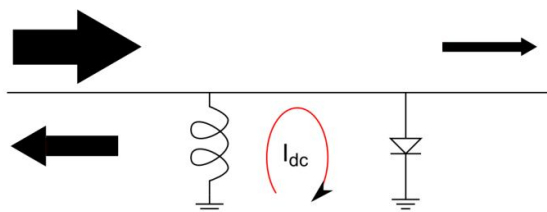
#### 5.2 RF Power Limiter

A well known circuit that consists of shunt pin diodes is an RF power limiter. RF power limiters are circuits that have little insertion loss when the input power is low, but limit the RF power at their output for higher input powers. They are generally used after the antenna and before the RF frontend to protect sensitive circuits like low noise amplifiers in the frontend of RF and microwave systems.

##### 5.2.1 Basic Limiter Circuit

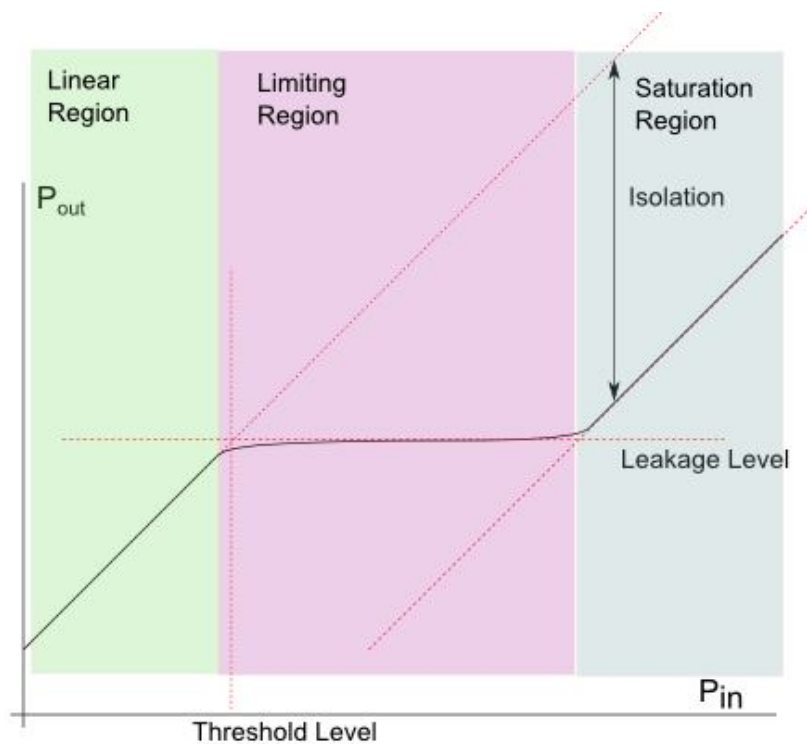
Consider the circuit shown in Figure 5.1, built by an inductor and a pin diode shunt mounted on a transmission line. When an RF signal is transmitted to this circuit, pin diode behaves like a rectifier and a DC current is generated on the diode. The inductor provides the DC return for the current. This DC

current decreases the resistance of the diode and as the result of this decrease, insertion loss of the circuit increases.



**Figure 5.1** Simple RF power limiter. Arrows represent RF power flow proportional to their sizes

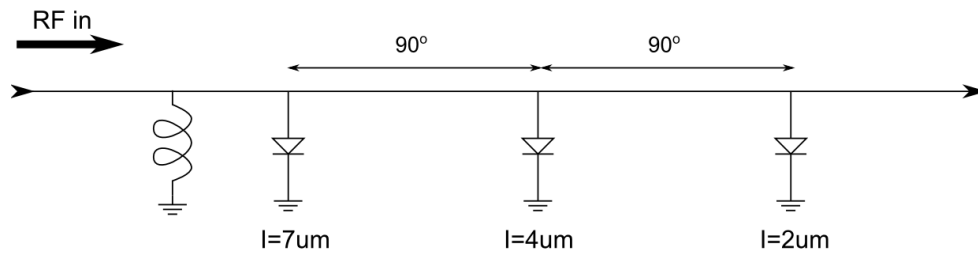
$P_{out}$  vs.  $P_{in}$  graph is shown in Figure 5.2. According to the incident power level, the limiter has three operating regions, namely linear, limiting and saturation regions. For low RF power levels, the generated current is negligible, diode resistance is high and diode is essentially a capacitor. If this capacitor is matched properly, RF signal passes through with low loss. These low power levels correspond to the linear region of the diode. As the RF power increases, DC current increases and diode resistance begins to decrease. Some of the incident RF power reflects back, because of the lower resistance of the diode. As the incident power increases more, an even higher percentage of incident power reflects back and gain decreases more. This negative feedback limits the RF power incident to the rest of the circuit, thus protecting the circuit from high RF power levels. These power levels correspond to the limiting region of the diode. If the incident power is very high,  $R_d$  is essentially short circuit and diode behaves as a resistance with value  $R_s$  for higher power levels. So the insertion loss of the circuit is essentially constant and very high (isolation state). For higher power levels, transmitted power increases as the incident power increases. This region is the saturation region of the limiter and a limiter should not be used in this region since the power dissipated at the diode increases rapidly as the input power continues to increase from this point on.



**Figure 5.2** Three regions of pin diode operation

For low leakage levels, pin diodes with thin I-layers should be used because diodes with thinner I-layers begin to compress at lower power levels. But for high power handling, diodes with thick I-layers should be used because RF power threshold level for saturation increases with the thickness of I-layer. For both high power handling and low leakage levels, a few pin diodes with different I-layer thicknesses are used together. RF power should be incident on the diode with the thickest I-layer, and other diodes should be placed next in the order of decreasing I-layer thicknesses. The last diode should be the one with the thinnest I-layer to minimize the leakage level. There should be  $90^\circ$  transmission lines between each diode to maximize the voltages on each diode, so that the limiting action would be most efficient. There can be a common DC return for all diodes. The parasitic capacitance of each diode should be matched and the impedance of DC return inductor should be high enough all over the operating band.



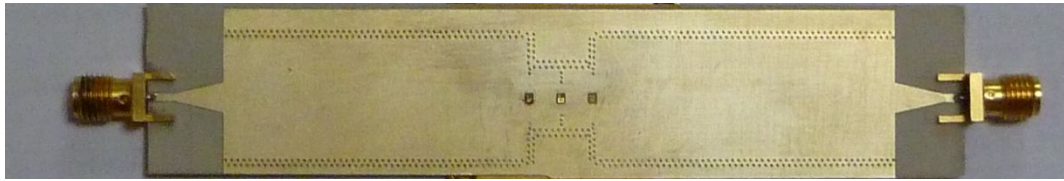


**Figure 5.3** 3-diode RF power limiter

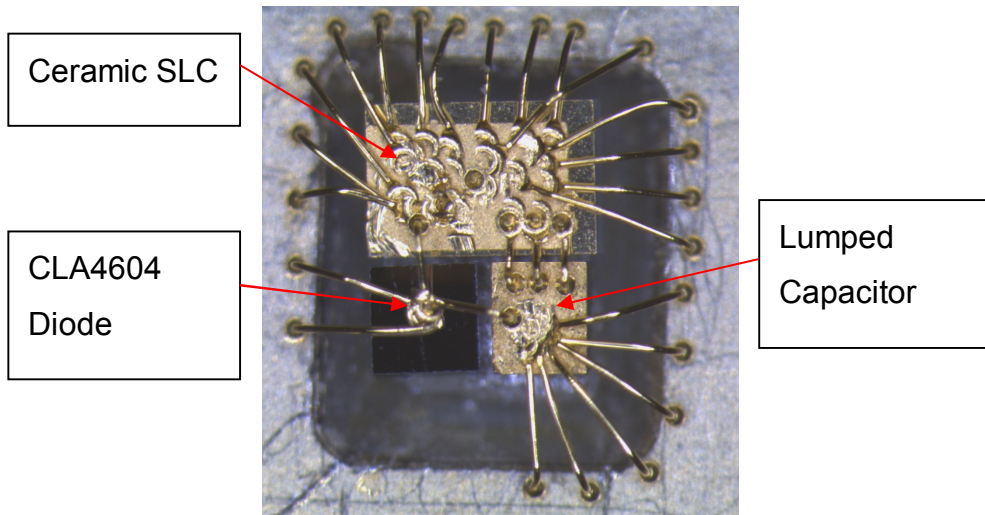
### 5.2.2 SIW RF Power Limiter

An RF Power Limiter is SIW structure can be designed using the same principles. The methodology is similar to the design of microstrip limiter except that the discontinuity in the SIW structure must be properly designed according to the linear model of the diodes. Since limiter is a nonlinear device, simulations are done with AWR<sup>®</sup> [54] using the harmonic balance method.

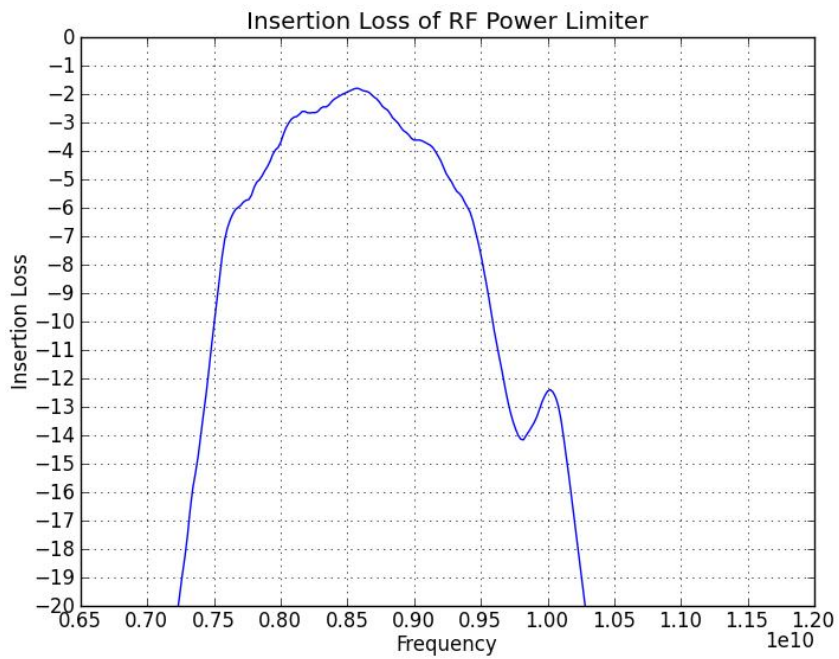
SIW RF power limiter will be demonstrated with two diodes for simplicity. In the design of the limiter, two different diodes will be used which are CLA4607 and CLA4604 of Skyworks Inc. CLA4607 diode has a thicker intrinsic layer and thus higher compression point. It can handle higher powers than CLA4604 which has a thinner intrinsic layer and lower compression point. So the CLA4607 diode will be used at the second resonator while at the last one CLA4604 will be used. The capacitor values in the linear models of the diodes are used to design the proper discontinuity which gives the necessary shunt inductance and capacitance values. A ceramic SLC is also used with lumped capacitor to increase the number of connections to the upper wall of the waveguide. Capacitance of this ceramic SLC is taken into account and added to lumped capacitance. Mounted diode and capacitors are shown in Figure 5.5. SIW power limiter prototype is shown in Figure 5.4. Linear insertion loss measurement of the limiter is shown in Figure 5.6.



**Figure 5.4** Picture of SIW RF power limiter

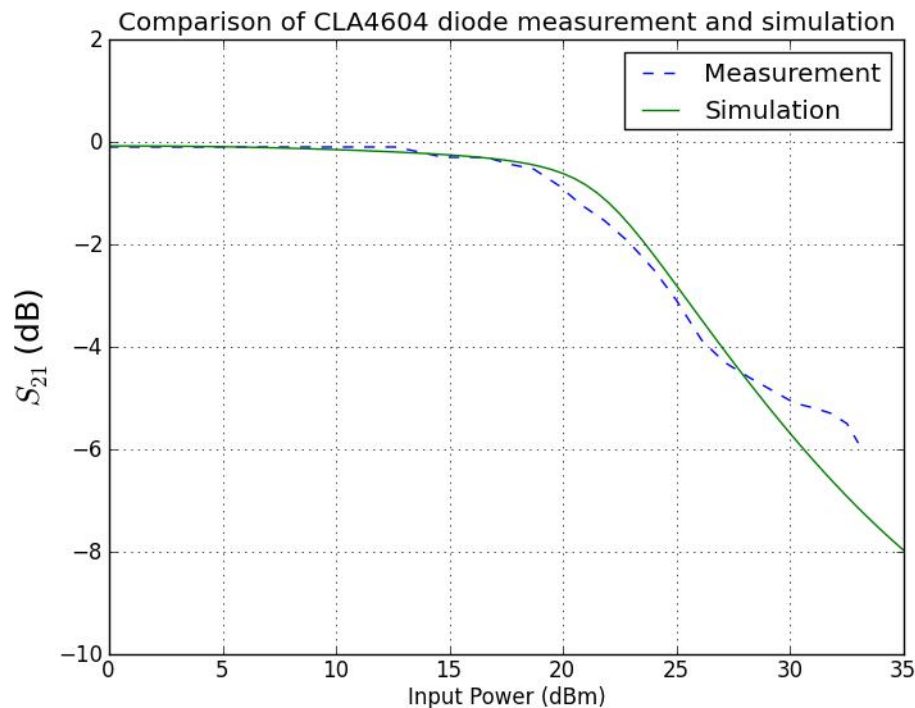


**Figure 5.5** Photo of CLA4604 diode and capacitors mounted together

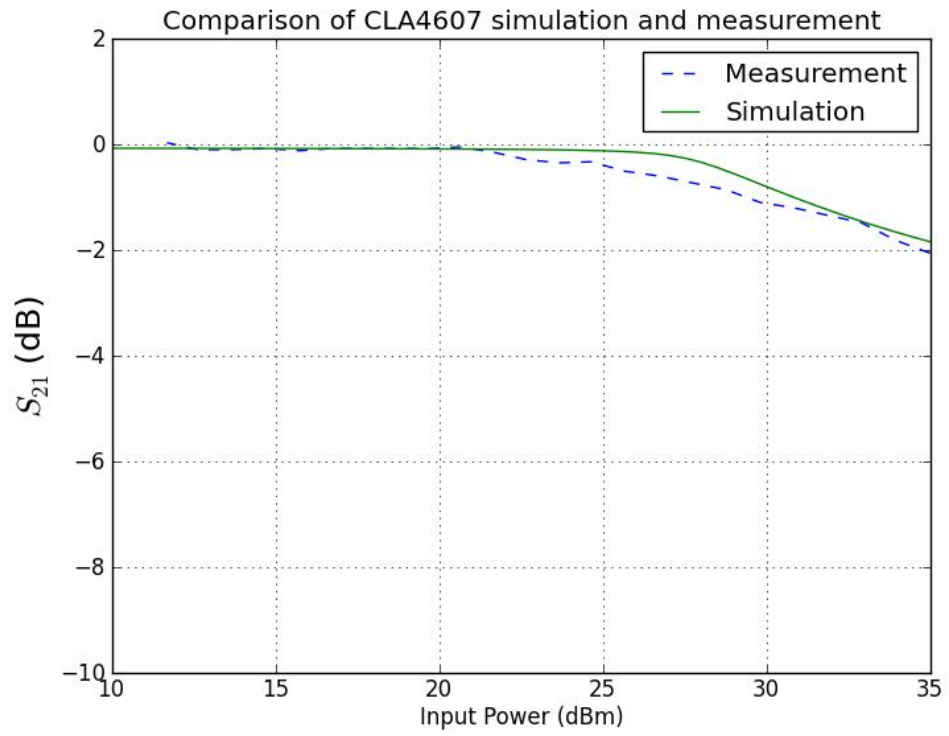


**Figure 5.6** Insertion loss of RF power limiter

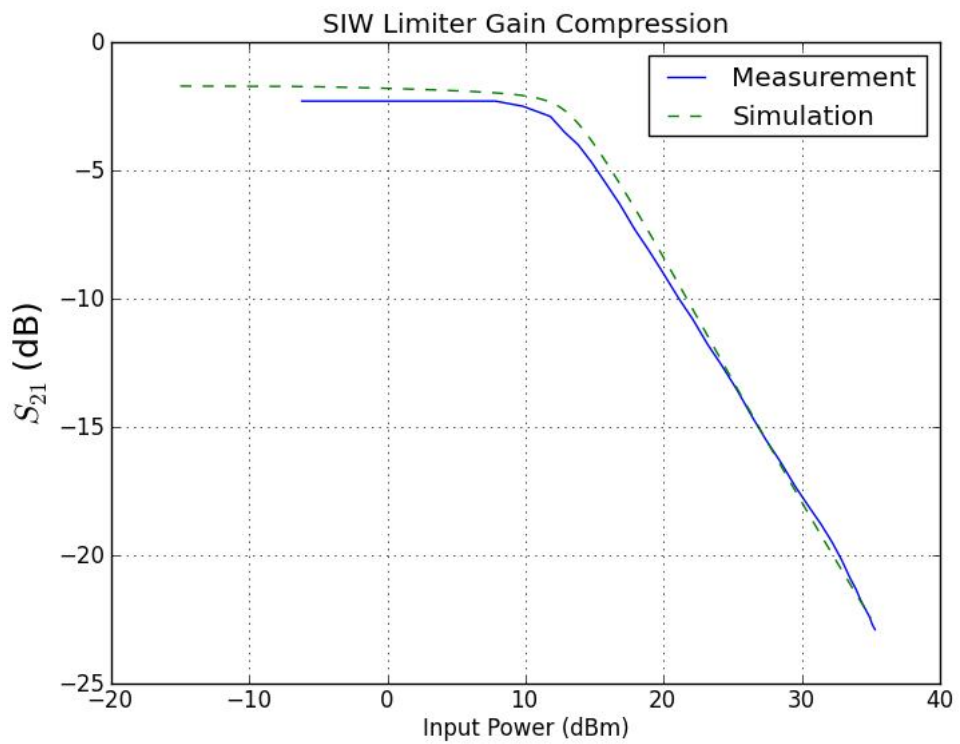
In the nonlinear simulation of the structure, the parameters given in the datasheets did not give very accurate results using the Robert-Caverly pin diode model in AWR. So each diode's nonlinear response ( $P_{out}$  vs.  $P_{in}$ ) is measured and diodes' parameters in the simulator are optimized such that simulation result is coincident with the measurement result. The measured result for CLA4604 diode and its simulated result with optimized parameters are shown in Figure 5.7. By the same way, the measured result for CLA4607 diode and its simulated result with optimized parameters are shown in Figure 5.8. Using these parameters, SIW RF power limiter is simulated. The simulation results are compared with the measurements results in Figure 5.9 and Figure 5.10. Measurement is done at 8.5GHz. In the prototyping, the same SIW PCB is used as the RF switch. Only the diodes and capacitors differ from the switch. Additionally top of the diode and capacitors are connected directly to the upper wall of the waveguide and DC block capacitors are not used.



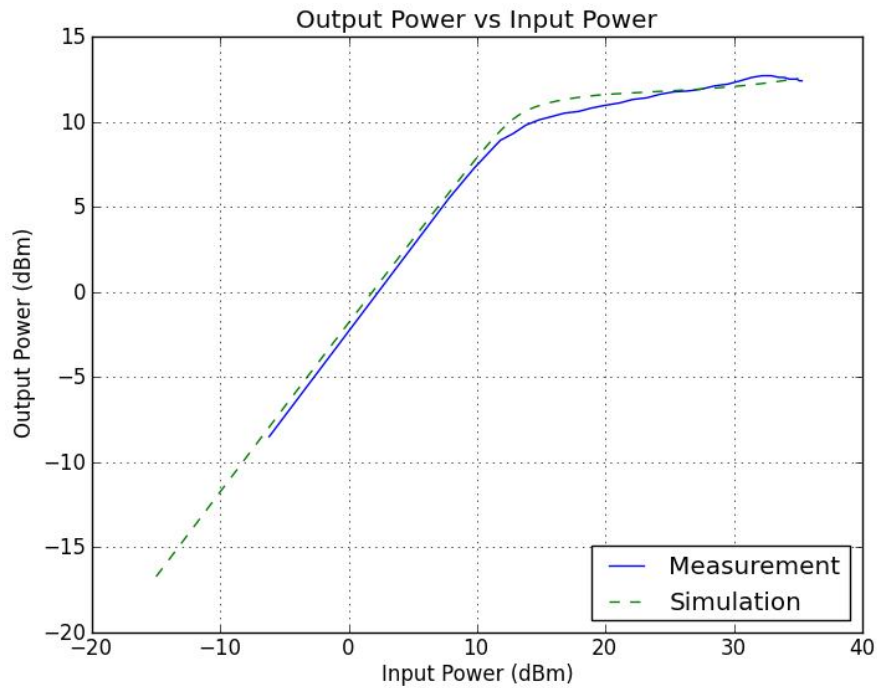
**Figure 5.7** Comparison of measurement of CLA4604 diode with the simulation with modified parameters



**Figure 5.8** Comparison of measurement of CLA4607 diode with the simulation with modified parameters



**Figure 5.9** Comparison of IL vs. Pin measurement of SIW limiter with the simulation



**Figure 5.10** Comparison of  $P_{out}$  vs.  $P_{in}$  measurement of SIW limiter with the simulation

### 5.2.3 Power Handling of SIW RF Power Limiter

The diodes can fail by different mechanisms when a high power is incident to the RF power limiter. These mechanisms are:

- 1- Thermal failure
- 2- Failure due to high RF peak voltage

As the incident power increases, heat dissipated in the diodes increase. Dissipated heat in the diode, results in an increase in channel temperature and this increase in the temperature is related to thermal impedance between the diode's channel and the base of the waveguide according to (5-1). If the channel temperature exceeds a certain value, diode fails. Power dissipated in the diode is related to minimum impedance of the diode, peak power, duty cycle and pulse width of the incident RF signal. In the remaining part the power handling of the RF power limiter will be investigated for a CW incident signal.

The temperature difference between the diode's channel and the base of the waveguide is related to the thermal impedance between the diode channel and environment through the formula:

$$\Delta T = T_{channel} - T_C = \Delta Q R_T \quad (5-1)$$

where;

$\Delta Q$ : Heat generated in the channel of the diode

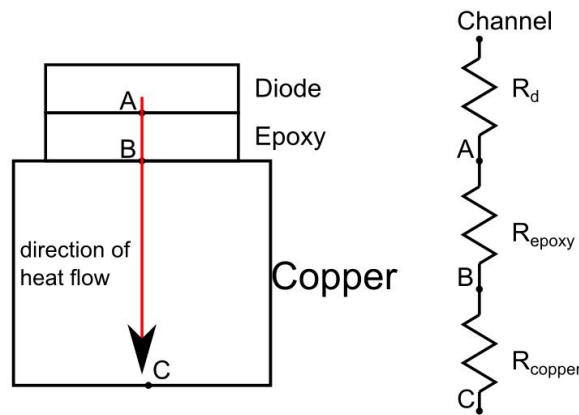
$R_T$ : Thermal resistance from the channel of the diode to the base of the waveguide

If it is assumed that the main path for the removal of heat from a diode is through the via beneath the diode, the thermal resistance model of the structure would be as shown in Figure 5.11. In this model;

$R_d$ : Thermal resistance from the diode's channel to diode's base

$R_{epoxy}$ : Thermal resistance of epoxy layer used to bond the diode.

$R_{copper}$ : Thermal resistance of the filled via.



**Figure 5.11** Thermal resistance model of the diode on a via

Then  $R_T$  can be calculated by the following equations;

$$R_T = R_d + R_{epoxy} + R_{copper} \quad (5-2)$$

$$R_{epoxy} = \frac{t_{epoxy}}{k_{epoxy} S_{epoxy}} \quad (5-3)$$

$$R_{copper} = \frac{t_{copper}}{k_{copper}S_{copper}} \quad (5-4)$$

where;

$t_{epoxy}$  and  $t_{copper}$  are the thickness of epoxy layer and copper via.

$k_{epoxy}$  and  $k_{copper}$  are the thermal conductivities of epoxy and copper.

$S_{epoxy}$  and  $S_{copper}$  are the surface area of epoxy layer and copper via.

$R_d$  can be looked up from the datasheets and given in Table 5.1.

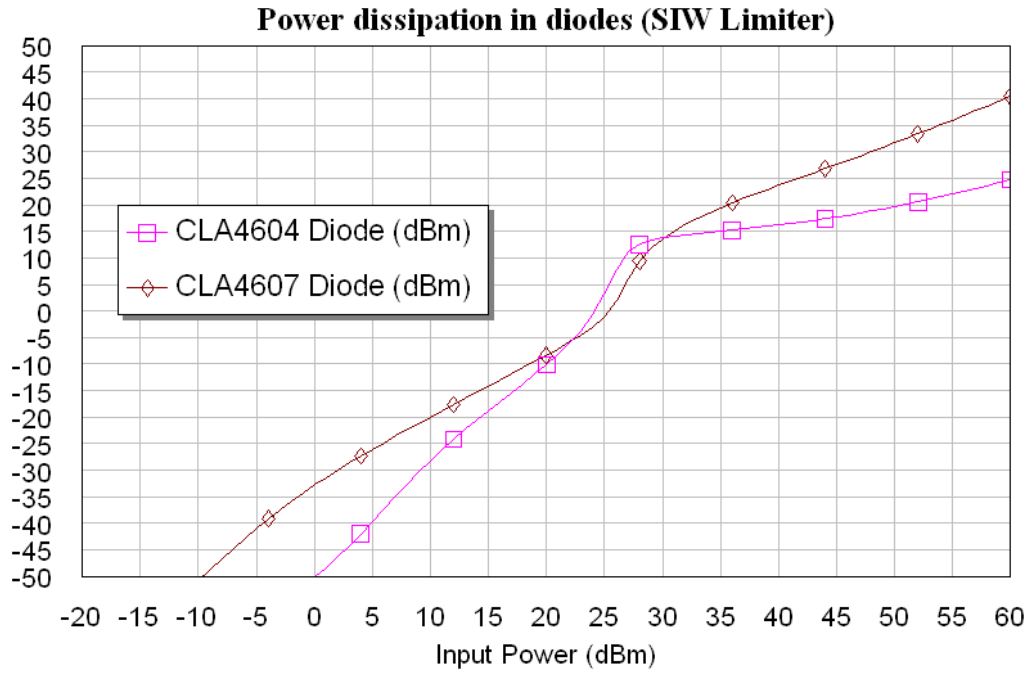
**Table 5.1** Thermal resistances of the diodes

Diode	$R_d$ ( $^{\circ}\text{C}/\text{W}$ )
CLA4607	40
CLA4604	100

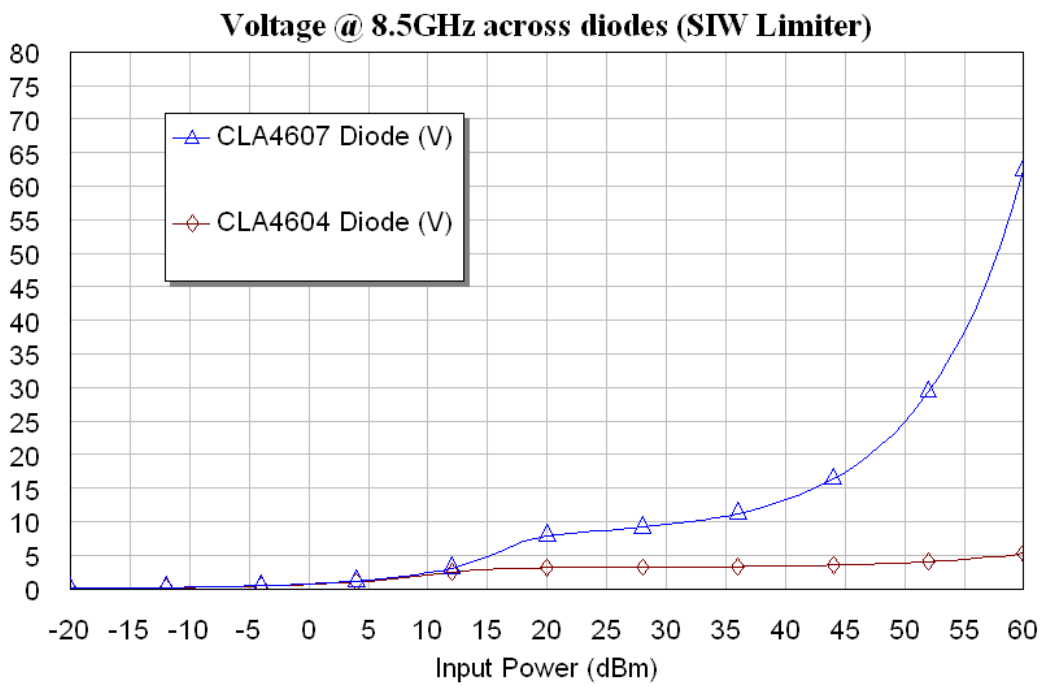
Epoxy layer is in the shape of a square prism with 16mil side length and 1mil thickness (same as diode). Copper via is in cylindrical shape with 0.25mm radius and 0.5mm height. Maximum channel temperature for each diode is  $175^{\circ}\text{C}$  and base of the waveguide is assumed to be at  $85^{\circ}\text{C}$ . Using these data and thermal conductivity values for epoxy and copper,  $R_T$  and maximum allowable dissipated heat for each diode are calculated using (5-1) thru (5-4) and given in Table 5.2.

**Table 5.2** Thermal resistance of diodes and maximum allowed power dissipation on diodes

Diode	$R_T$ ( $^{\circ}\text{C}/\text{W}$ )	Maximum power dissipation (dBm)
CLA4607	48.5	32.7
CLA4604	108.5	29.2



**Figure 5.12** Dissipated power in the diodes of SIW RF power limiter



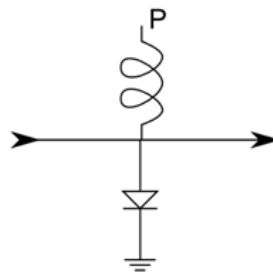
**Figure 5.13** Fundamental component of voltages across the diodes of SIW RF power limiter



Dissipated powers in the diodes of SIW RF power limiter are given in Figure 5.12 with respect to input power. By inspecting this plot, if only the thermal failure of diodes is considered, the power limiter can handle a maximum of 52dBm. Peak voltage levels on diodes are plotted in Figure 5.13. Only the peak voltage associated with the fundamental component is plotted since the other harmonics are much lower than the fundamental. CLA4604 can handle 30V peak voltage and CLA4607 can handle 120V peak voltage. So, according to Figure 5.13, failure due to peak voltage is a less stringent failure mechanism than failure due to thermal breakdown. The same voltage appears on the lumped capacitors too. For this reason, lumped capacitors should be able to withstand the same voltage levels. Lumped capacitors with 100V breakdown voltage are available and they can be used.

#### 5.2.4 SIW RF Power Limiter/Switch

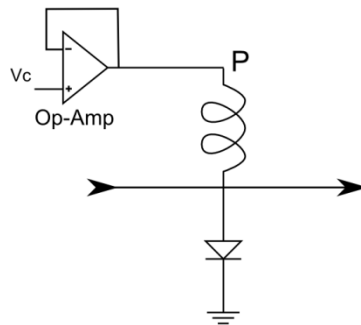
For moderate power levels, this limiter structure can also be used as an RF switch. Suppose that a SIW limiter is constructed by using CLA4607 diodes at the first two resonators and CLA4604 diode at the last one. Consider a single diode in this limiter as shown in Figure 5.14.



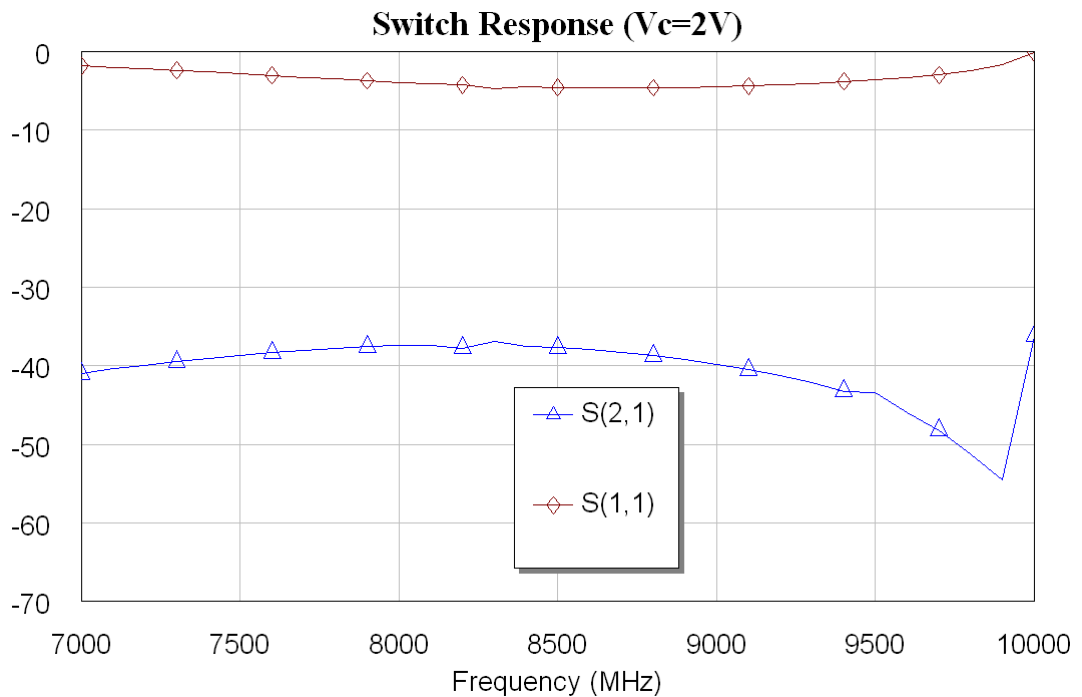
**Figure 5.14** A representative single diode in limiter

If point P is shorted to ground, then this diode functions as a limiter. But if an adequate current is injected to the diode by applying a suitable DC voltage at this point, then diode becomes essentially short circuit and isolates the input and output. So this structure can function both as a power limiter and an RF switch if it is biased with a voltage source with low output impedance.

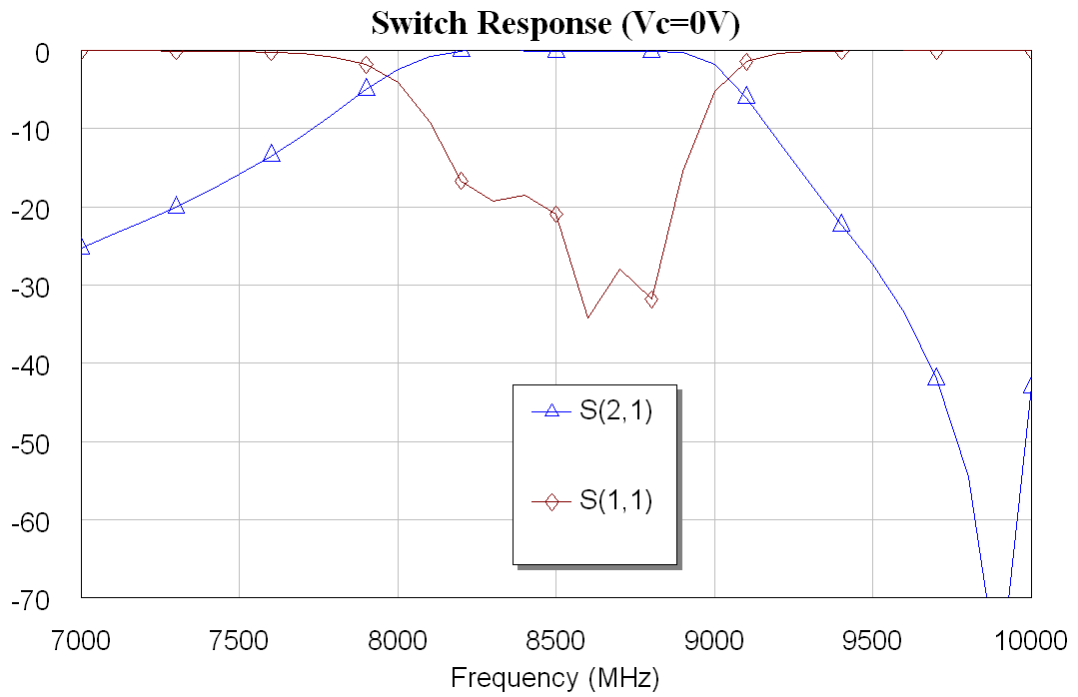
A voltage source with this property is an operational amplifier. This method can work only for moderate RF power levels due to limited output current capability of operational amplifiers, but voltage sources with higher current capability can be designed and used by other means. In the simulations, LM8261 Op-Amp [56] is used in buffer configuration (Figure 5.15). Spice model of LM8261 is used for simulations. If 2V is applied to the Op-Amp, then the diode becomes essentially short circuit. If 0V is applied to the Op-Amp, then the diode behaves as an RF power limiter. Simulation results are given in Figure 5.16, Figure 5.17 and Figure 5.18.



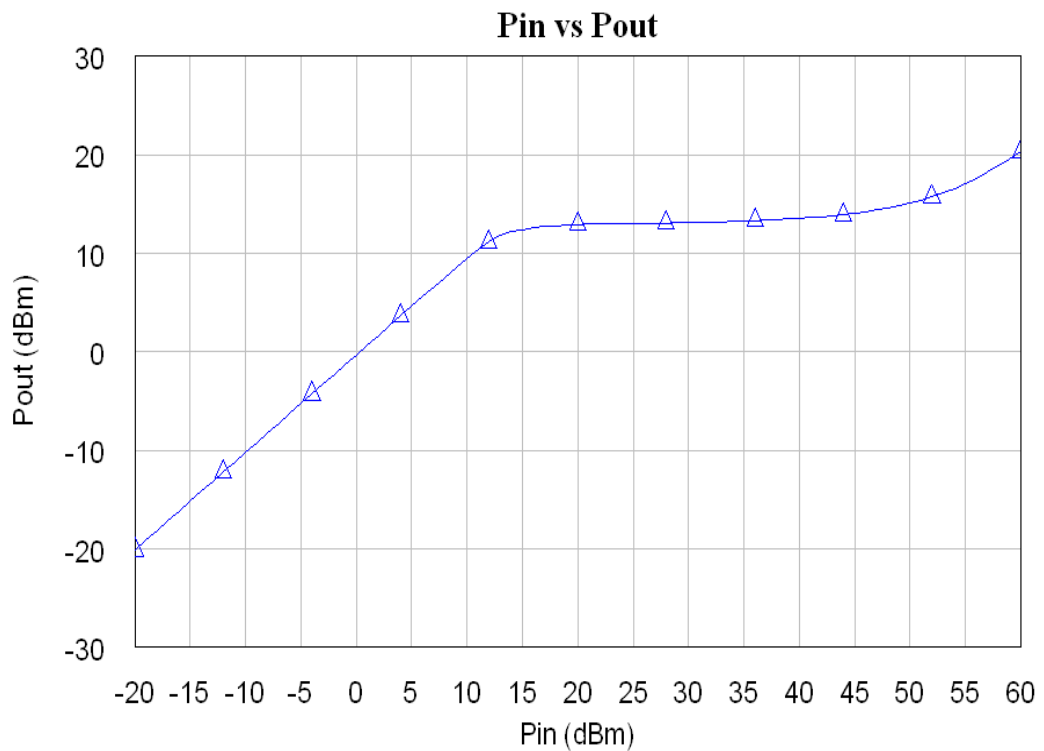
**Figure 5.15** Single diode of RF switch biased with an Op-Amp



**Figure 5.16** Response in isolation mode



**Figure 5.17** Insertion loss and return loss of the switch for low power levels



**Figure 5.18**  $P_{in}$  vs.  $P_{out}$  for SIW RF power limiter

### 5.3 Tunable Filter

This structure can be used as a tunable filter to some degree. There are two different capacitor values in a 3<sup>rd</sup> order filter ( $C_1$  and  $C_2$ ). The center frequency of the filter can be changed by only varying these two capacitor values. Although the shape of the filter is distorted a bit with varying center frequency, the filter remains usable. The simulated response of the filter for various values of capacitors is shown in Figure 5.19.  $C_1$  and  $C_2$  are found by tuning for each center frequency. Variations of  $C_1$  and  $C_2$  values with respect to center frequency are given in Figure 5.21. The difference between  $C_1$  and  $C_2$  remains almost constant with varying center frequency. This suggests that for moderate frequency tuning ranges, a 3<sup>rd</sup> order tunable filter can be designed with a single type of varactor diode and center frequency can be tuned with a single voltage. The variation of filter response with respect to  $C_1$  while  $C_2 - C_1$  is constant (0.12pF) is plotted in Figure 5.20. As shown in the plot, center frequency can be tuned over a frequency range comparable to the filter's bandwidth with single voltage without a significant distortion in response.

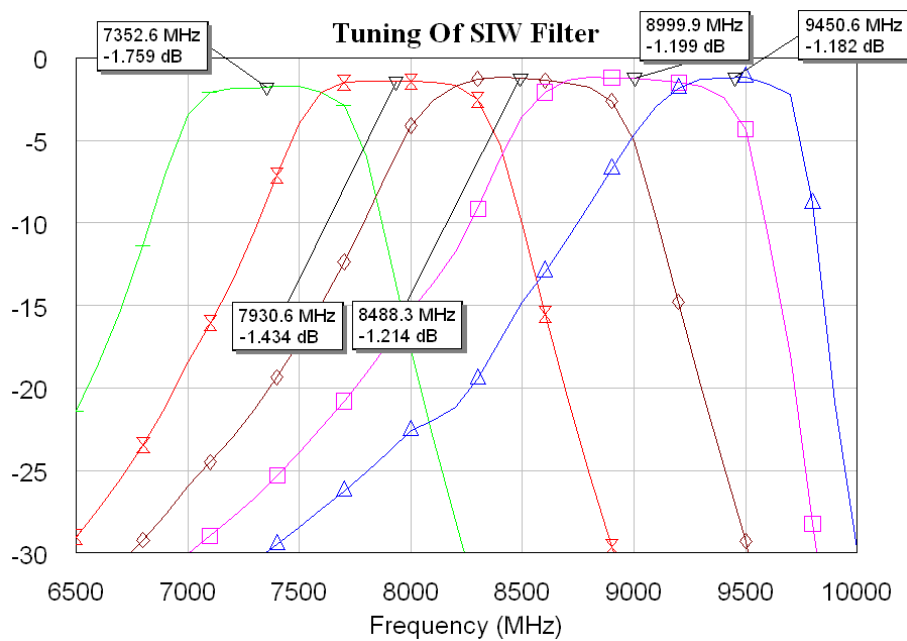
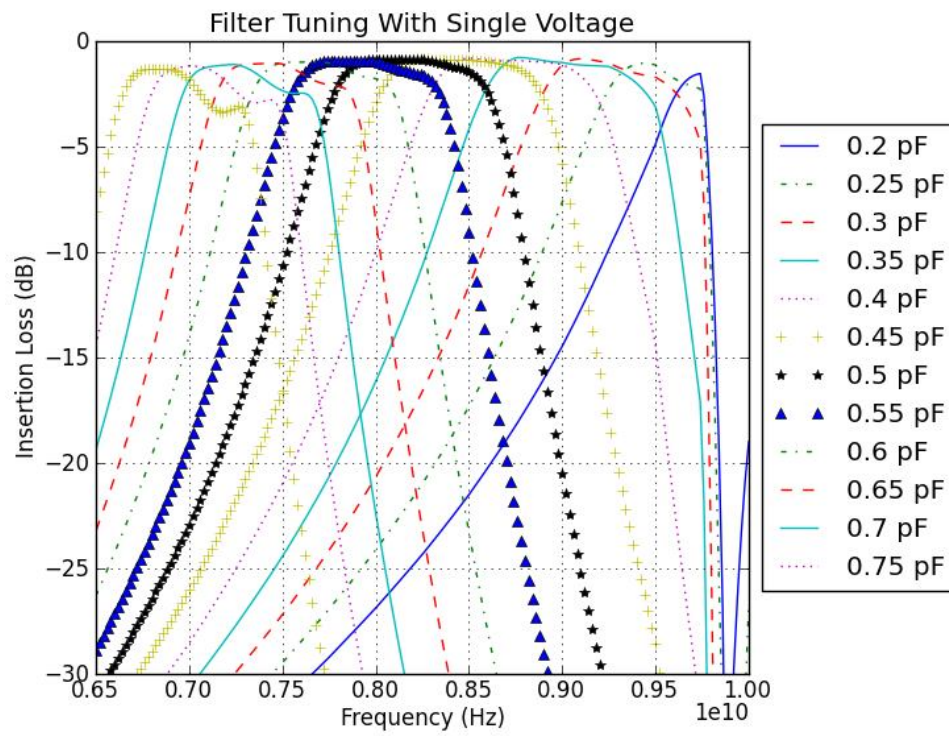
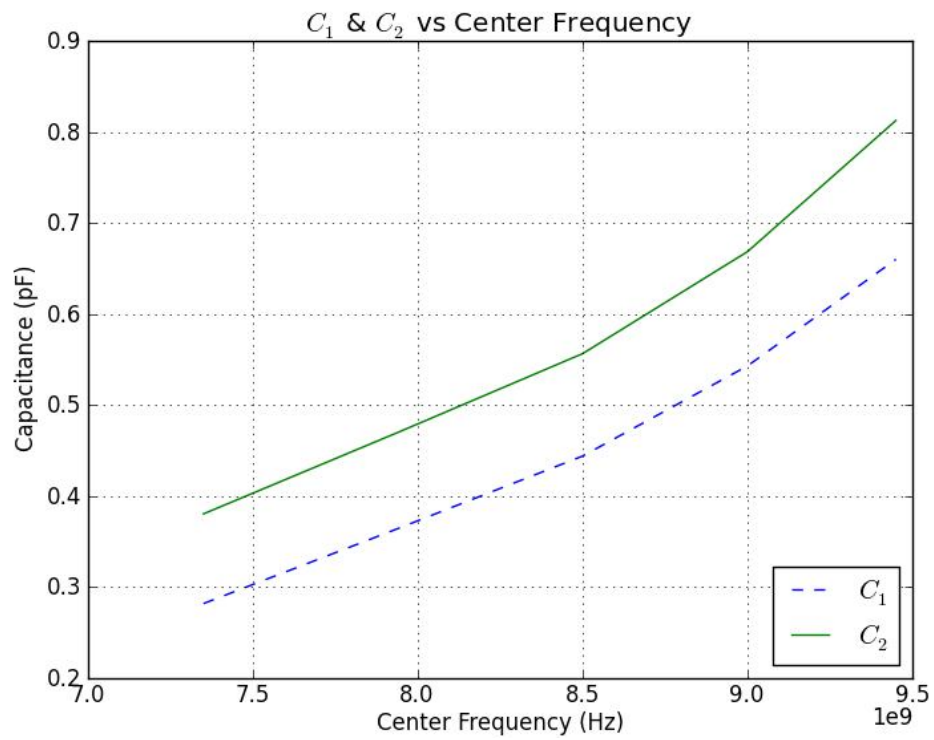


Figure 5.19 Variation of the filter response while tuning



**Figure 5.20** Variation of the filter response with single voltage tuning



**Figure 5.21** The values  $C_1$  and  $C_2$  take with respect to center frequency

## 5.4 Conclusion

In this chapter two different applications of the same topology used in SIW switch is given. The main difference between these circuits and the SIW RF switch is the choice of diode types. In the RF power limiter application, pin diodes with high power handling are chosen while varactor diodes are used for tunable filter. Several RF functions can be combined in the same circuit which enables integration of different capabilities in a smaller physical area. RF power limiter and RF switch functions are combined in a single circuit as an example. Varactor diodes and pin diodes can be used together to design a switch with tunable center frequency. All the capacitors in the filter should be tuned at the same time according to the center frequency of the filter to tune the filter with low loss.

## CHAPTER 6

### CONCLUSIONS AND FUTURE STUDIES

In this thesis a design method for RF switches in a PCB using SIW structure is described. This method enables incorporation of RF switches in substrate integrated waveguide structures (slot arrays, power distribution circuits etc.). The same circuit structure can also be used for other similar circuits involving shunt diodes like tunable filter and RF power limiter. Several RF functions can also be combined in a single circuit.

Although the RF components described in this thesis do not have any particular performance advantages over similar RF components designed for microstrip environment, they are more advantageous to use in SIW environments. In a system which uses SIW as the basic transmission medium, it is cumbersome to make transitions first to microstrip and then back to SIW just to incorporate an RF switch in the path. These transitions decrease the performance and increase physical space requirements.

At the front-ends of typical microwave receivers, several RF components are present almost invariably. RF power limiters are used to protect sensitive circuits from high power signals coming to the antenna. Pre-selector filters are used to receive only the signals in the operating frequency band and improve the spurious-free dynamic range of the system. RF switches are also used at the input of systems to isolate the signals coming from outside while measuring the noise level of the system. Also during self-calibration and self-test of the system, incoming signals

may corrupt the process, so an SPST switch at the input of the system is used to prevent this. Another important advantage of the structure described in this work is that several functions – like filter, power limiter, switch or tunable filter - that are frequently used at the input of receiver systems can be combined in a single circuit and by this way physical space requirements are decreased. In a frontend of a microwave system which incorporates a SIW antenna, the remaining components can also be implemented in SIW and the component described in this work can be utilized in this system.

The circuit described in this work has some drawbacks too. If this component is considered only as a switch, the insertion loss is higher than typical microwave switches. In fact RF paths that include an RF filter are the most appropriate ones to use this component, because if filtering functionality is not needed, extra insertion loss of this structure might not be justified. Considering the production stage, filled vias should be used which may increase the production cost of the PCB. Filled via is needed to mount the components on and for better electrical and thermal conductivity to the base of the waveguide.

Single-pole multiple-throw switches can be used at antenna switching networks and SIW power distribution networks. SPDT switches can be used to select between transmit and receive chain while using a common antenna for both. Although only SPST and SPDT switch are demonstrated in this work, this method can be applied to design switches with multiple arms.

The circuit described in this work can be improved further. The filter response is very sensitive to capacitor values as shown in the section about tunable filter application. The single layer capacitors (SLC) used in the filter should have low tolerances. It is also important to make the opening on the waveguide around the diode as small as possible to decrease the insertion



loss. So a better solution for capacitors is to make a custom single layer capacitor with tight tolerance and with a special geometry to cover the opening as much as possible while at the same time allowing the mounting of a diode. A tuning mechanism at the production stage can be useful. Two kinds of tuning mechanism can be used:

- 1- Varactor diodes can be used for fine tuning of capacitance.
- 2- Custom built SLC capacitors can be designed in a special shape to allow tuning with ribbon or bond wires at the testing stage of production.

## REFERENCES

- [1] Wu K., Deslandes D., Cassivi Y., "The Substrate Integrated Circuits - A New Concept for High-Frequency Electronics and Optoelectronics", 6<sup>th</sup> International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Service, 2003. TELSIS 2003. Volume 1, 1-3 Oct. 2003 Page(s): P - III-P-X vol.1.
- [2] Cassivi, Y., Perregrini, L., Arcioni, P., Bressan, M., Wu K., Conciauro, G., "Dispersion Characteristics of Substrate Integrated Rectangular Waveguide", IEEE Microwave and Wireless Components Letters, Volume 12, Issue 9, Sep 2002 Page(s): 333 - 335.
- [3] Che W., Deng K., Wang D. and Chow Y.L., "Analytical equivalence between substrate-integrated waveguide and rectangular waveguide", IET Microwaves, Antennas & Propagation, Volume 2, Issue 1, February 2008, Page(s):35 – 41.
- [4] Che W., Xu L., Wang D., Deng K., Chow Y.L., "Short-circuit equivalence between rectangular waveguides of regular sidewalls (rectangular waveguide and sidewalls of cylinders (substrate-integrated rectangular waveguides), plus its extension to cavity", IET Microwaves, Antennas & Propagation, Volume 1, Issue 3, June 2007 Page(s):639 – 644.
- [5] Deslandes D., Wu K., "Integrated Microstrip and Rectangular Waveguide in planar form", IEEE Microwave and Wireless Components Letters, Feb. 2001, Vol: 11, No: 2, Page(s):68-70.
- [6] Deslandes D., Wu K., "Integrated transition of coplanar to rectangular waveguides", IEEE Microwave Symposium Digest, Volume 2, May 2001, Page(s):619 - 622.
- [7] Deslandes D., Wu K., "Design Consideration and Performance Analysis of Substrate Integrated Waveguide Components", IEEE European Microwave Conference, Oct. 2002, Page(s):1 – 4.
- [8] Ding Y., Wu K., "Substrate Integrated Waveguide-to-Microstrip Transition in Multilayer Substrate", IEEE Transactions on Microwave Theory and Techniques, Volume 55, Issue 12, Part 2, Dec. 2007 Page(s):2839 - 2844.

- [9] Suntives, A., Abhari, R., "Transition Structures for 3-D Integration of Substrate Integrated Waveguide Interconnects", IEEE Microwave and Wireless Components Letters, Volume 17, Issue 10, Oct. 2007, Page(s):697 - 699.
- [10] Xu F., Wu K., "Guided-Wave and Leakage Characteristics of Substrate Integrated Waveguide", IEEE Transactions on Microwave Theory and Techniques, Volume 53, Issue 1, Jan. 2005, Page(s):66 - 73.
- [11] Zhang S. Z., Yu Z. Y., Li C., Deng J. H., "Electromagnetic Energy Leakage Characteristics of Substrate Integrated Waveguide", Asia-Pacific Microwave Conference Proceedings, APMC 2005, Volume 2, Dec. 2005.
- [12] Hong W., Liu B., Wang Y., Lai Q., Tang H., Yin X. X., Dong Y. D., Zhang Y., Wu K., "Half Mode Substrate Integrated Waveguide: A New Guided Wave Structure for Microwave and Millimeter Wave Application", Joint 31st International Conference on Infrared Millimeter Waves and 14th International Conference on Terahertz Electronics, IRMMW-THz, Sept. 2006, Page(s):219 – 219.
- [13] Che W., Geng L., Deng K., Chow, Y.L., "Analysis and Experiments of Compact Folded Substrate-Integrated Waveguide", IEEE Transactions on Microwave Theory and Techniques, Volume 56, Issue 1, Jan. 2008, Page(s):88 – 93.
- [14] Germain S., Deslandes D., Wu K., "Development of substrate integrated waveguide power dividers", IEEE Canadian Conference on Electrical and Computer Engineering, Volume 3, May 2003, Page(s):1921 - 1924.
- [15] Zhang Z.-Y., Wu K., "A Broadband Substrate Integrated Waveguide (SIW) Planar Balun", IEEE Microwave and Wireless Components Letters, Volume 17, Issue 12, Dec. 2007, Page(s):843 - 84.
- [16] Liu B., Hong W., Zhang Y., Tang H. J., Yin X. X., Wu K., "Half Mode Substrate Integrated Waveguide 180° 3-dB Directional Couplers", IEEE Transactions on Microwave Theory and Techniques, Volume 55, Issue 12, Part 1, Dec. 2007, Page(s):2586 - 2592.
- [17] Djeraji T., Wu K., "Super-Compact Substrate Integrated Waveguide Cruciform Directional Coupler", IEEE Microwave and Wireless Components Letters, Volume 17, Issue 11, Nov. 2007, Page(s):757 - 759.
- [18] Liu B., Hong W., Wang Y.-Q., Lai Q.-H., Wu K., "Half Mode Substrate Integrated Waveguide (HMSIW) 3-dB Coupler", IEEE Microwave

and Wireless Components Letters, Volume 17, Issue 1, Jan. 2007, Page(s):22 - 24.

[19] Cheng Y., Hong W., Wu K., "Half Mode Substrate Integrated Waveguide (HMSIW) Directional Filter", IEEE Microwave and Wireless Components Letters, Volume 17, Issue 7, July 2007, Page(s):504 - 506.

[20] Wang Y., Hong W., Dong Y., Liu B., Tang H. J., Chen J., Yin X., Wu K., "Half Mode Substrate Integrated Waveguide (HMSIW) Bandpass Filter", IEEE Microwave and Wireless Components Letters, Volume 17, Issue 4, April 2007, Page(s):265 - 267.

[21] Stephens, D., Young, P.R., Robertson, I.D., "W-band substrate integrated waveguide slot antenna", IEE Electronics Letters Volume 41, Issue 4, Feb. 2005, Page(s):165 - 167.

[22] Hong W., Liu B., Luo G.Q., Lai Q.H., Xu J.F., Hao Z.C., He F.F., Yin X. X., "Integrated Microwave and Millimeter Wave Antennas Based on SIW and HMSIW Technology", International Workshop on Antenna Technology: Small and Smart Antennas Metamaterials and Applications, IWAT '07, March 2007, Page(s):69 - 72.

[23] Hong W., Xu J., Lai Q., Chen P., "Design and implementation of low sidelobe slot array antennas with full and half mode substrate integrated waveguide technology", IEEE European Microwave Conference, Oct. 2007, Page(s):428 - 429.

[24] Yang S., Suleiman, S.H., Fathy, A.E., "Low Profile Multi-Layer Slotted Substrate Integrated Waveguide (SIW) Array Antenna with Folded Feed Network for Mobile DBS Applications", IEEE Antennas and Propagation International Symposium, June 2007, Page(s):473 - 476.

[25] Yan L., Hong W., Hua G., Chen J., Wu K., Cui T. J., "Simulation and Experiment on SIW Slot Array Antennas", IEEE Microwave and Wireless Components Letters, Volume 14, Issue 9, Sept. 2004 Page(s):446 - 448.

[26] Hao Z. C., Hong W., Chen X. P., Chen J. X., Wu K., Cui T. J., "Multilayered Substrate Integrated Waveguide (MSIW) Elliptic Filter", IEEE Microwave and Wireless Components Letters, Volume 15, Issue 2, Feb. 2005 Page(s):95 - 97.

[27] Deslandes D., Wu K., "Single-Substrate Integration Technique of Planar Circuits and Waveguide Filters", IEEE Transactions on Microwave Theory and Techniques, Volume 51, Issue 2, Part 1, Feb. 2003 Page(s):593 - 596.

- [28] Chen X., Hong W., Hao Z., Wu K., "Substrate Integrated Waveguide Quasi-Elliptic Filter Using Extracted-Pole Technique", Asia-Pacific Microwave Conference Proceedings, APMC 2005, Volume 1, Dec. 2005.
- [29] Zhang Y. L., Hong W., Wu K., Chen J. K., Tang H. J., "Novel Substrate Integrated Waveguide Cavity Filter With Defected Ground Structure", IEEE Transactions on Microwave Theory and Techniques, Volume 53, Issue 4, Part 1, April 2005, Page(s):1280 - 1287.
- [30] Hao Z. C., Hong W., Chen J. X., Chen X. P., Wu K., "Compact Super-Wide Bandpass Substrate Integrated Waveguide (SIW) Filters", IEEE Transactions on Microwave Theory and Techniques, Volume 53, Issue 9, Sept. 2005, Page(s):2968 - 2977.
- [31] Chen X. P., Wu K., "Substrate Integrated Waveguide Cross-Coupled Filter with Negative Coupling Structure", IEEE Transactions on Microwave Theory and Techniques, Volume 56, Issue 1, Jan. 2008, Page(s):142 - 149.
- [32] Deslandes D., Wu K., "Millimeter-wave substrate integrated waveguide filters", IEEE Canadian Conference on Electrical and Computer Engineering, Volume 3, May 2003, Page(s):1917 - 1920.
- [33] Grigoropoulos, N., Sanz-Izquierdo, B., Young, P.R., "Substrate Integrated Folded Waveguides (SIFW) and Filters", IEEE Microwave and Wireless Components Letters, Volume 15, Issue 12, Dec. 2005, Page(s):829 - 831.
- [34] Armendariz M., "Tunable Substrate Integrated Waveguide Filters Implemented With Pin Diodes and RF MEMS Switches", M. Sc. Thesis, Dec. 2010.
- [35] Deslandes D., Wu K., "High Isolation Substrate Integrated Waveguide Passive Front-End for Millimeter-Wave Systems", IEEE Microwave Symposium Digest, June 2006, Page(s):982 - 985.
- [36] He F. F., Wu K., Hong W., Han L., Chen W., "A Low Phase-Noise VCO Using an Electronically Tunable Substrate Integrated Waveguide Resonator", IEEE Transactions on Microwave Theory and Techniques, Volume 58, Issue 12, Dec. 2010, Page(s):3452 - 3458.
- [37] Sirci S., Martinez J.D., Taroncher M., Boria V.E., "Varactor-Loaded Continuously Tunable SIW Resonator for Reconfigurable Filter Design", Proceedings of the 41<sup>st</sup> European Microwave Conference, Oct. 2011, Page(s):436 - 439.

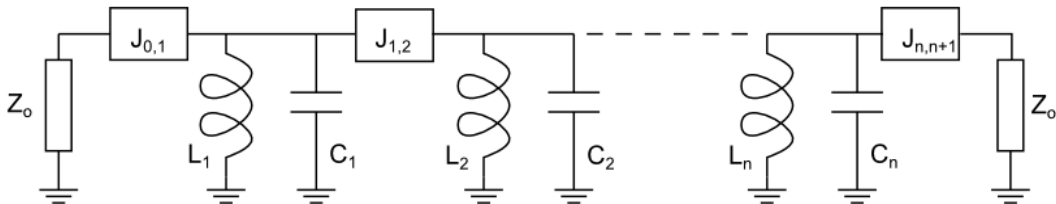
- [38] Senior D. E., Cheng X., Yoon Y.-K., "Electrically Tunable Evanescent Mode Half-Mode Substrate-Integrated-Waveguide Resonators", IEEE Microwave and Wireless Components Letters, Mar. 2012, Vol: 22, No: 3, Page(s):123-125.
- [39] Zhong C., Xu J., Yu Z., Zhu Y., "Ka-Band Substrate Integrated Waveguide Gunn Oscillator", IEEE Microwave and Wireless Components Letters, July 2008, Vol: 18, No: 7, Page(s):461-463.
- [40] Senior D.E., Cheng X., Yoon Y. K., "A Compact, Single-Layer Substrate Integrated Waveguide (SIW) Cavity-Backed Active Antenna Oscillator", IEEE Antennas and Propagation Letters, 2012, Vol: 11, Page(s):431-433.
- [41] Abdolhamidi M., Shahabadi M., "X-Band Substrate Integrated Waveguide Amplifier", IEEE Microwave and Wireless Components Letters, Dec. 2008, Vol: 18, No: 12, Page(s):815-817.
- [42] Zhang Z. Y., Wei Y. R., Wu K., "Broadband Millimeter-Wave Single Balanced Mixer and Its Applications to Substrate Integrated Wireless Systems", IEEE Transactions on Microwave Theory and Techniques, Volume 60, Issue 3, Mar. 2012, Page(s):660 - 669.
- [43] Sbarra E., Marcaccioli L., Gatti R. V., Sorrentino R., "Ku-band analogue phase shifter in SIW technology", Proceedings of the 39<sup>th</sup> European Microwave Conference, Sep. 2009, Page(s):264 – 267.
- [44] Ruo Feng Xu, B. Sanz Izquierdo, P. R. Young, "Switchable Substrate Integrated Waveguide", IEEE Microwave and Wireless Components Letters, Apr. 2011, Vol: 21, No: 4, Page(s):194-197.
- [45] Ghiotto A., Adhikari S., Wu K., "Ferrite-Loaded Substrate Integrated Waveguide Switch", IEEE Microwave and Wireless Components Letters, Mar. 2012, Vol: 22, No: 3, Page(s):120-122.
- [46] Farrall A. J., Young P. R., "Substrate Integrated Rectangular Waveguides", IEEE High Frequency Postgraduate Student Colloquium, 2004.
- [47] GC4271 product page, 15.04.2012, <http://www.microsemi.com/en/products/product-directory/77022>, Last accessed on 17-08-2012.
- [48] Sickel T., "Tunable Evanescent Mode X-Band Waveguide Switch", Ph. D. Thesis, Dec. 2005.

- [49] Marcuvitz N., Waveguide Handbook (IEEE Electromagnetic Waves Series), 1986.
- [50] Microstrip Filters for RF/Microwave Applications. Jia-Sheng Hong, M. J. Lancaster, John Wiley & Sons, 2001.
- [51] Craven G. F., Mok C. K., “The Design of Evanescent Mode Waveguide Bandpass Filters for a Prescribed Insertion Loss Characteristic”, IEEE MTT, March 1971.
- [52] Engen G. F., Hoer C. A., “Thru-Reflect-Line, An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer”, MTT, December 1979.
- [53] ANSYS HFSS 3D EM Simulation software <[www.ansys.com](http://www.ansys.com)>, Last accessed on 26-08-2012.
- [54] Advanced Wave Research (AWR) Official Web Page, <[www.awrcorp.com](http://www.awrcorp.com)>, Last accessed on 26-08-2012.
- [55] RO4000 Series High Frequency Circuit Materials, Rogers Corp., <http://www.rogerscorp.com/documents/726/acm/RO4000-Laminates---Data-sheet.aspx>, Last accessed on 17-08-2012.
- [56] LM8261 datasheet, <http://www.ti.com/product/lm8261>, Last accessed on 19-08-2012.
- [57] DLI Di-Cap model parameters, <http://www.dliextra.net/capcad/DiCaps.aspx>, Last accessed on 26-08-2012.
- [58] “Establishing the Minimum Reverse Bias for a PIN Diode in a High-Power Switch”, Rev. V2, M/A-COM Technology Solutions application note, <http://www.macomtech.com/Application%20Notes/pdf/AN3022.pdf>, Last accessed on 26-08-2012.
- [59] Di-Cap, [http://www.dilabs.com/pdfs/Pg%208-11%20SLC%20Di-Cap\\_02-2011.pdf](http://www.dilabs.com/pdfs/Pg%208-11%20SLC%20Di-Cap_02-2011.pdf), Last accessed on 26-08-2012.

## APPENDIX A

### EVANESCENT-MODE WAVEGUIDE FILTER DESIGN

In this part, the design of an evanescent mode waveguide filter will be summarized. The design method begins with choosing a filter prototype. Since the lumped element equivalent circuit of an admittance inverter is very similar to the lumped element equivalent circuit of a waveguide section in evanescent mode, band pass filter circuit formed by shunt L-C resonators coupled by admittance inverters (J-inverters) is chosen as the starting point. The circuit is shown in Figure A.1 [50]. Circuit parameters can be calculated using equations (A-1) thru (A-4). In this derivation, it is assumed that reference impedance of both ports are equal to each other ( $Z_0$ ).



**Figure A.1** Filter formed by L-C resonators coupled by J-inverters

$$J_{0,1} = \sqrt{\frac{FBW\omega_0 C_1}{Z_0 g_0 g_1}} \quad (A-1)$$

$$J_{i,i+1} = FBW\omega_0 \sqrt{\frac{C_i C_{i+1}}{g_i g_{i+1}}} \quad (A-2)$$

$$J_{n,n+1} = \sqrt{\frac{FBW\omega_0 C_n}{Z_0 g_n g_{n+1}}} \quad (A-3)$$



$$L_i = \frac{1}{\omega_0^2 C_i} \quad (\text{A-4})$$

where;

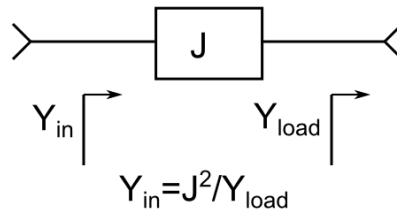
FBW: Fractional bandwidth

$g_i$ : Filter coefficients for a unit bandwidth, 1 Ohm reference impedance low-pass filter

$Z_0$ : Reference impedance

$\omega_0$ : Center angular frequency

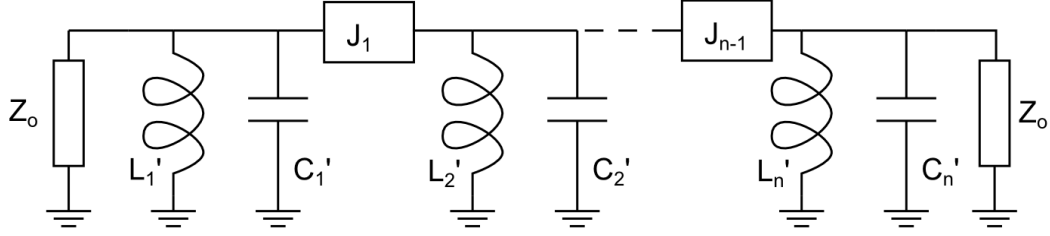
J-Inverter is an ideal element, the input admittance of which is the inverse of load admittance, multiplied by a constant (Figure A.2). This constant (J) is called the characteristic admittance of the J-inverter and ideally it is independent of frequency.



**Figure A.2** Definition of J-Inverter

This filter incorporates J-inverters and thus provides us an extra freedom about the component values; the capacitor values can be chosen arbitrarily. If  $J_{0,1}$  is equal to  $J_{n,n+1}$ , which requires that that  $C_1=C_n$ , the first and the last J-inverters can be easily eliminated by scaling the remaining component values. Capacitor values are chosen such that  $C_1=C_n$  and thus  $J_{0,1}=J_{n,n+1}=J_0$ . Then  $J_{0,1}$  and  $J_{n,n+1}$  can be eliminated without changing the insertion loss by scaling the remaining impedance values by  $Z_0^2 J_0^2$  (J and capacitor values by  $1/(Z_0^2 J_0^2)$  and inductor values by  $Z_0^2 J_0^2$ ). After this elimination, the filter becomes the one shown in Figure A.3. Although the capacitor values were chosen arbitrarily, after this scaling and elimination process, the first and the

last capacitors ( $C_1'$  and  $C_n'$ ) become a certain value regardless of their initial value.



**Figure A.3** J-Inverter coupled band pass filter circuit

$$J_i = \frac{g_0 g_1}{Z_0 C_1} \sqrt{\frac{C_i C_{i+1}}{g_i g_{i+1}}} \quad (\text{A-5})$$

$$C_i' = \frac{C_i g_0 g_1}{Z_0 FBW \omega_0 C_1} \quad (\text{A-6})$$

$$L_i' = \frac{1}{\omega_0^2 C_i'} \quad (\text{A-7})$$

$g_i$  can be calculated according to the chosen filter response shape. If the main functionality of the circuit is RF switching and out-of-band response is not important, then Butterworth response can be chosen which provides maximally flat insertion loss response in the pass band of the filter. If the filtering functionality is important too, then Chebyshev response can be chosen which provides steepest skirts at the edges of the pass band for the same degree of filter.  $g_i$  values for Butterworth response can be calculated using (A-8) and (A-9) and  $g_i$  values for Chebyshev response can be calculated using (A-9), (A-10), (A-11) and (A-12) [50].

$$g_i = 2 \sin\left(\frac{(2i-1)\pi}{2n}\right) \quad i = 2..n \quad (\text{A-8})$$

$$g_0 = g_{n+1} = 1.0 \quad (\text{A-9})$$

$$\gamma = -\sinh\left(\frac{1}{2n}\ln\left(\tanh\left(\frac{R_{db}}{17.37}\right)\right)\right) \quad (\text{A-10})$$

$$g_1 = \frac{2}{\gamma}\sin\left(\frac{\pi}{2n}\right) \quad (\text{A-11})$$

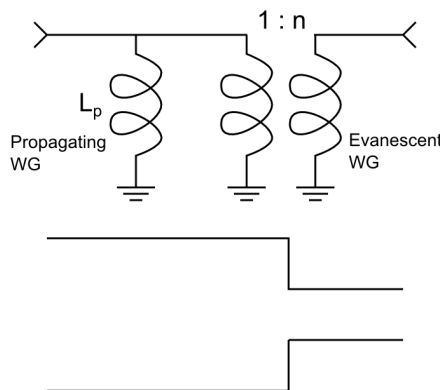
$$g_i = \frac{1}{g_{i-1}} \frac{4\sin\left[\frac{(2i-1)\pi}{2n}\right]\sin\left[\frac{(2i-3)\pi}{2n}\right]}{\gamma^2 + \sin^2\left[\frac{(i-1)\pi}{n}\right]} \quad i = \quad (\text{A-12})$$

where;

n: degree of the filter.

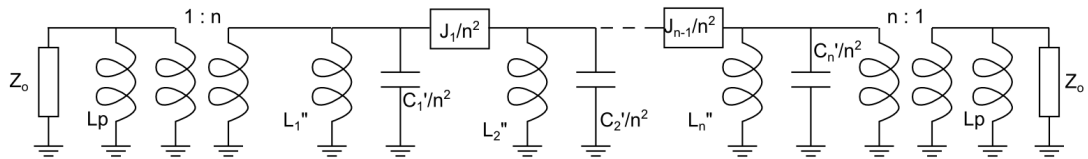
R<sub>db</sub>: ripple of insertion loss in dB

The input and output waveguides should allow propagation at the operating frequency band. However, the cutoff frequency of the waveguide in which the filter is built is above the operating frequency band and the wave is evanescent. So there should be a waveguide discontinuity at both ends of the filter. A EWG-WG junction can be modeled by a susceptance and a transformer (Figure A.4) [49]. The n and L<sub>p</sub> parameters of the equivalent circuit are given in [49] for a symmetric hollow waveguide transition, but full-wave simulation should be used to calculate the exact values for an arbitrary waveguide transition.



**Figure A.4** Equivalent circuit of waveguide transition

These junctions can be absorbed in filter design by scaling all impedance values in the circuit by  $1/n^2$  and modifying the first and last inductance values. It is assumed that input and output waveguides of the filter are identical. The resultant circuit is shown in Figure A.5. The circuit in Figure A.5 should be functionally equivalent to the circuit in Figure A.3, so the equations (A-13) and (A-14) should be satisfied.



**Figure A.5** J-Inverter coupled band pass filter circuit with equivalent circuits of waveguide junctions at both end.

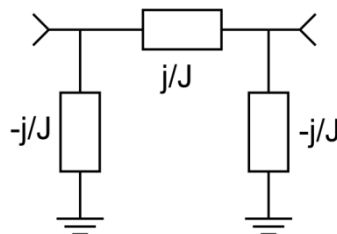
$$L_i'' = \frac{n^2}{\frac{1}{L_i'} - \frac{1}{L_p}} \quad i = 1, n \quad (\text{A-13})$$

$$L_i'' = n^2 L_i' \quad i = 2..n - 1 \quad (\text{A-14})$$

The ABCD matrix of an ideal admittance inverter (J-inverter) is

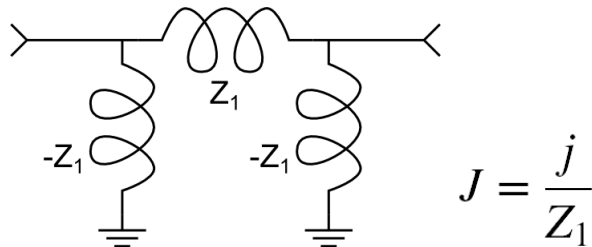
$$ABCD = \begin{bmatrix} 0 & \pm \frac{1}{jJ} \\ \mp jJ & 0 \end{bmatrix} \quad (\text{A-15})$$

The circuit equivalent of a J-inverter that will result in the same ABCD matrix is shown in Figure A.6.



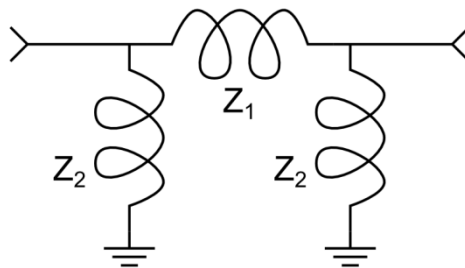
**Figure A.6** J-Inverter circuit representation

Although the susceptances in this ideal circuit are frequency independent, at a narrow frequency band they can be realized by positive and negative valued inductances (Figure A.7). The characteristic admittance of the inverter will be exact only at the mid-band frequency.



**Figure A.7** Lumped equivalent of a J-Inverter

The equivalent circuit of a section of uniform waveguide in cutoff is given in Figure A.8. The impedance values can be calculated by equations (A-16), (A-17) and (A-18). The field in an evanescent mode waveguide decays exponentially. The waveguide impedance is complex for the frequencies below cutoff. The equivalent circuit can be considered as an attenuator renormalized by complex characteristic impedance.



**Figure A.8** Equivalent circuit of a waveguide in cutoff

$$Z_1 = jX_0 \sinh(\gamma l_e) \quad (\text{A-16})$$

$$Z_2 = \frac{jX_0}{\tanh\left(\frac{\gamma l_e}{2}\right)} \quad (\text{A-17})$$

$$X_0 = \frac{2b}{a} \sqrt{\frac{\mu_0}{\epsilon_0 \epsilon_r}} \frac{k}{\gamma} \quad (\text{A-18})$$

where;

$l_e$ : Length of the evanescent mode waveguide section

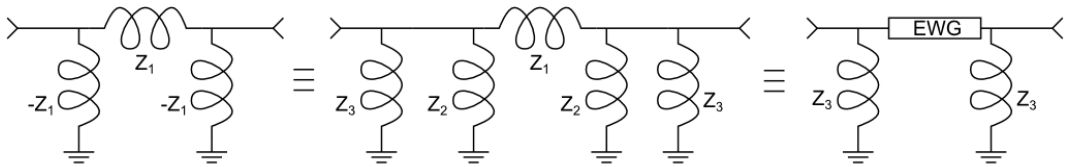
$X_0$ : Absolute value of the characteristic impedance of evanescent mode waveguide section at frequencies below cut-off

$\gamma$ : Absolute value of the propagation constant of the evanescent mode waveguide section

$b$ : Height of the evanescent mode waveguide section

$a$ : Width of evanescent mode waveguide section

J-inverters in Figure A.3 can be replaced by an EWG section between two shunt inductors. This transformation is shown in Figure A.9. The equations about this transformation are given in (A-19), (A-20), (A-21) and (A-22). The length of EWG section is calculated from J-inverter value by equations (A-19) and (A-20) and shunt susceptances at input and output of EWG section is calculated by (A-22).



**Figure A.9** Equivalent circuit of a J-inverter and its equivalent one as a EWG section between two shunt inductive impedances ( $Z_3$ )

$$Z_1 = -\frac{1}{jJ} \quad (\text{A-19})$$

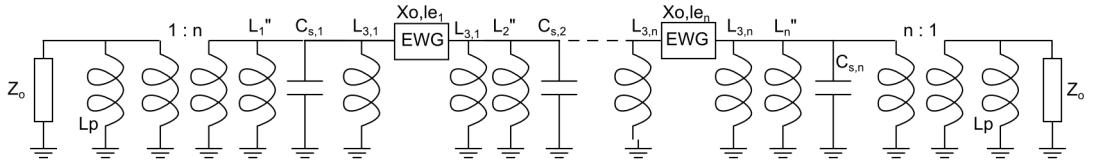
$$Z_1 = jX_0 \sinh \gamma l_e \quad (\text{A-20})$$

$$Z_2 = \frac{jX_0}{\tanh\left(\frac{\gamma l_e}{2}\right)} \quad (\text{A-21})$$

$$Z_3 = -jX_o \tanh \gamma l_e \quad (\text{A-22})$$

where  $X_o$ ,  $l_e$  and  $\gamma$  are impedance, length and absolute value of propagation constant of the EWG section respectively. Note that parallel combination of  $Z_2$  and  $Z_3$  is equal to  $-Z_1$ .

After this transformation the filter circuit becomes the one shown in Figure A.10. Equivalent shunt inductor values of  $Z_3$  impedances for each J-inverter are calculated at center frequency of the filter. The final simplified circuit is shown in Figure A.11. Equations (A-23) thru (A-28) should be used to calculate the parameters of circuit elements.

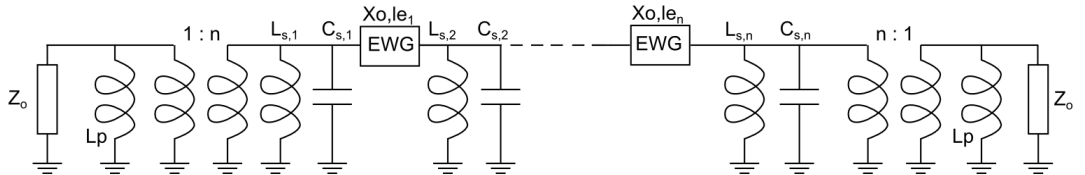


**Figure A.10** Evanescent mode filter with waveguide steps at both ends

$$C_{s,i} = \frac{C_i'}{n^2} \quad (\text{A-23})$$

$$l_{e,i} = \frac{1}{\gamma} \sinh^{-1} \left( \frac{n^2}{J_i X_o} \right) \quad (\text{A-24})$$

$$L_{3,i} = - \frac{X_o \tanh \gamma l_{e,i}}{\omega_o} \quad (\text{A-25})$$



**Figure A.11** Evanescent mode filter with waveguide steps at both ends

$$\frac{1}{L_{s,1}} = \frac{1}{L_{3,1}} + \frac{1}{L_1''} \quad (\text{A-26})$$

$$\frac{1}{L_{s,n}} = \frac{1}{L_{3,n}} + \frac{1}{L_n''} \quad (\text{A-27})$$

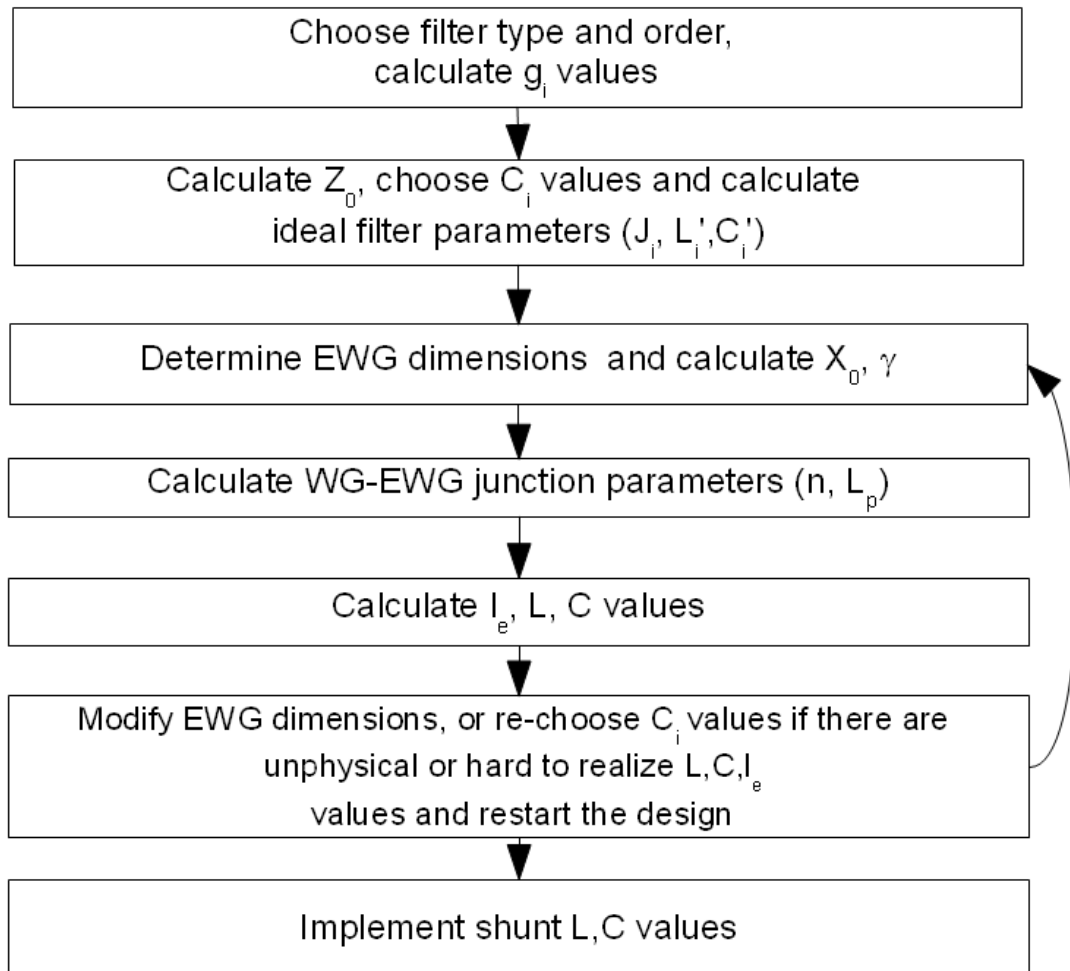
$$\frac{1}{L_{s,i}} = \frac{1}{L_{3,i-1}} + \frac{1}{L_{3,i}} + \frac{1}{L_i''} \quad i = 2..n - 1 \quad (\text{A-28})$$

Consider the transformation in Figure A.9 again.  $Z_1$  is determined by the value of the J-inverter and it is related to the impedance ( $X_0$ ), propagation constant ( $\gamma$ ) and the length of the EWG section ( $l_e$ ). Physically the dimensions of the EWG and the design frequency determine the characteristic admittance of the J-inverter. In general, the width, height, dielectric material etc, are determined beforehand, and the frequency is chosen to be the center frequency of the filter. Thus,  $X_0$  and  $\gamma$  is fixed and length is calculated according to the characteristic admittance of a J-inverter.

So after the determination of the ideal filter components (Figure A.3), the dimensions of the EWG must be chosen. For SIW structure it is best to choose the height the same as the input and output waveguides. So only the width of the EWG is should be chosen such that the cutoff frequency of the waveguide is higher than the maximum operating frequency of the filter. The dimensions of the EWG and the center frequency determine the impedance of the EWG ( $X_0$ ), the  $n$  and  $L_p$  of the junction. The component values of the ideal filter would be manipulated according to  $n$ ,  $L_p$  values to absorb the junction in the filter design. At this point J-inverter characteristic admittances are known and they should be used to calculate the lengths of EWG sections. Then  $X_0$  and lengths of the EWG sections will be used to calculate  $Z_3$  values in Figure A.9. These  $Z_3$  values and  $L_p$  values are used to calculate new inductor values of the circuit. At this point equivalent inductance, capacitance values and dimensions of EWG sections are



known and so the final filter circuit has been designed. In Figure A.12, this procedure is summarized.



**Figure A.12** Flowchart for the general design procedure of the filter

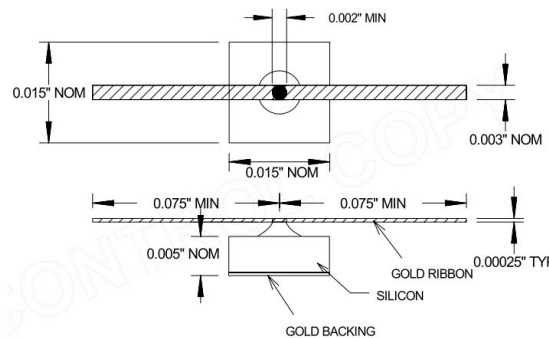
## APPENDIX B

### MATERIALS AND DEVICES USED AT THE DESIGN AND PROTOTYPES

In this part, the specifications of various devices and materials utilized in the design and implementations will be summarized. The data shown are mostly gathered from the official datasheets of the devices and the name of the manufacturer can be referred as the reference of the data presented.

#### B.1. GC4271 Pin Diode

GC4271 diode of Microsemi[47] is the pin diode used for prototyping the RF switches. It comes with its own gold wires on it which makes it easier to use. The drawing of the diode's package is shown in Figure B.1 and the properties of the diode are shown in Table B.1.



**Figure B.1** The drawing of the pin diode used for the design and the fabrication of the prototypes

**Table B.1** Properties of GC4271

Model Number	Breakdown Voltage	Junction Capacitance	Series Resistance	Carrier Lifetime	Thermal Resistance
GC4271	70V	0.1pF	1.0 Ohm	100ns	70 °C/W

## B.2. CLA4604 and CLA4607 Pin Diodes

CLA4604 and CLA4607 are the two diodes used in the RF power limiter circuit. CLA4607 is the first diode at the input of the limiter which has a thicker I-region and higher RF power handling. CLA4604 is the second diode with thinner I-region and lower RF leakage power. Properties of these diodes are given in Table B.2.

**Table B.2** Properties of CLA4604 and CLA4607

Model Number	Breakdown Voltage	Junction Capacitance	Series Resistance	I-Region Thickness	Thermal Impedance For CW Signals
CLA4604	30V	0.12pF	2.5 Ohm	2 $\mu\text{m}$	100 $^{\circ}\text{C/W}$
CLA4607	120V	0.20pF	2.0 Ohm	7 $\mu\text{m}$	40 $^{\circ}\text{C/W}$

## B.3. RO4003 Substrate Material

RO4003 is the substrate of SIW used in this work. The electrical specifications of the RO4003 substrate are shown in Table B.3. More information about the substrate can be found at from [55].

**Table B.3** Some electrical properties of RO4003

Manufacturer	ROGERS CORPORATION
Dielectric Constant	3.38
Dissipation Factor, $\tan\delta$	0.0023

# CURRICULUM VITAE

## PERSONAL INFORMATION

Surname, Name: Erdöl, Tuncay

Nationality: Turkish (TC)

Date and Place of Birth: 5 September 1981, Trabzon

Phone: +90 312 592 26 03

Email: terdol@aselsan.com.tr

## EDUCATION

Degree	Institution	Year of Graduation
BS	Bilkent University	2002
MS	Bilkent University	2005

## WORK EXPERIENCE

Year	Place	Enrollment
2002-Present	ASELSAN A.Ş.	RF/Microwave Engineer

## FOREIGN LANGUAGES

English

## PUBLICATIONS

1. T.Erdöl, V.B.Ertürk, "An Asymptotic Closed-Form Paraxial Formulation for the Surface Fields on Electrically Large Dielectric Coated Circular Cylinders", 4th European Workshop on Conformal Antennas, 2005