NANOSTRUCTURE ENHANCED PHOTOVOLTAIC DEVICES

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ABSTRACT

NANOSTRUCTURE ENHANCED PHOTOVOLTAIC DEVICES

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There are mainly three generations of solar cells that have been categorized by considering their efficiency and manufacturing cost. Although lots of investigations and research is going on in this field, but the first generation solar cells are most commercially available solar cells. First generation solar cells consist of single and multi-crystalline silicon (Si), which has been doped typically by phosphorus and boron in a p-n junction configuration. Si is non-toxic, relatively low cost and naturally abundant semiconducting material, which make it quite beneficial to be employed in microelectronics and photovoltaic industry. In general, Si solar cells contain, a Si active layer sandwiched with antireflection layer and metallic contacts. Solar cells fabricated from solar grade Si shows high efficiency; however, the impurity level should be kept in minimum. Moreover, cell production process consists of high energy consuming steps such as co-firing of the contacts in metallization step (900°C) and antireflective coating deposition via plasma enhanced

chemical vapor deposition (PECVD) which necessitate high temperatures (400°C) and vacuum.

Improving performance of conventional Si solar cells and decreasing costs by consuming less expensive materials is an important challenge that should be overcome. Employing nanostructured materials instead of bulk or thin film components can be a promising route, which recently inspired many scientists.

Nanowires that are synthesized via low-cost and solution-based methods can be utilized in any of the cell components to provide distinct advantages, which is the main theme of this thesis. In this regard, independently, vertically aligned zinc oxide nanowires are utilized as antireflection coatings, random silver nanowire networks are used as top electrodes and vertically aligned Si nanowires on ultrathin Si wafers are used as the active layer in crystal Si solar cells.

Keywords: ZnO nanorods, Ag nanowires, Si nanowires, ultrathin Si solar cells.

ÖZ

NANOYAPILAR İLE GELİŞTİRİLMİŞ FOTOVOLTAİK AYGITLAR

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Verimlilik ve maliyetlerine göre kategorize edildiğinde üç ayrı nesil güneş gözesinden bahsedilebilir. Bu alanda birçok inceleme ve araştırma yapılmasına rağmen sadece birinci nesil güneş gözeleri ticari olarak mevcuttur. Birinci nesil güneş gözeleri, p-n eklemleri oluşturan, fosfor ve bor ile katkılanan tek ve çoklu kristal silisyumdan oluşur. Silisyum zehirli olmayan, göreli olarak düşük fiyatlı ve doğada bol bulunan bir malzemedir, bu durum da onu mikroelektronik ve fotovoltaik endüstrisinde en çok kullanilan malzeme yapmaktadır. Genel olarak silisyum güneş gözeleri, yansımayı onleyici tabaka ve kontaklarla sandviç yapı oluşturan aktif silisyum tabakadan oluşur. Safsizlik seviyesi çok az olan göze kalitesindeki silisyum ile üretilen cihazlar yüksek verimlilik göstermektedir. Göze üretimi metalizasyon sirasindaki fırınlama işlem (900 °C) ile yansımayı onleyici kaplama sırasında yüksek vakum ve sıcaklığa (400 °C) ihtiyaç duyan plazma destekli kimyasal buhar biriktirme (PECVD) işlemi gibi yüksek enerji gerektiren adimlardan oluşmaktadir.

Ticari silisyum hücrelerin performanslarının artırılmasi ve daha ucuz malzemelerin kullanımı ile maliyetlerinin düşürülmesi gerekmektedir. Hacimli malzemeler ve ince fılmler yerine kullanilacak olan nanomalzemeler bu doğrultuda bir çözüm sunabilir ve birçok bilim insanı için bir ilham kaynağı olmuştur.

Ucuz maliyetli ve cözelti esasli yöntemlerle üretilen nanotellerin ceşitli göze bileşenlerinde belirgin avantajlar sağlaması amaciyla kullanılması, bu tezin temel amacını oluşturmaktadır. Bu bağlamda birbirinden bağimsiz olarak dikey hizalanan çinko oksit nanoteller yansımayı onleyeci tabaka olarak; gümüş nanotel ince fılmler üst elektrot olarak ve dikey hizalanmış silisyum nanoteller ultra ince silisyum güneş gözelrinde aktıf tabaka olarak kullanılmıştır.

Anahtar Kelimeler: çinko oksit nanoteller, gümuş nanoteller, silisyum nanoteller, ultra ince silisyum güneş gözeleri.

To Moon, Angel and Cypress

ACKNOWLEDGEMENTS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

FIGURES

NOMENCLATURE

a-Si	Amorphous Si
AFM	Atomic Force Microscopy
Ag NWs	Silver Nanowires
AM	Air Mass
ARC	Antireflection Coating
AWR	Average Weighted Reflectance
BSF	Back Surface Field
CIGS	Cupper Indium Gallium Selenide
CNT	Carbon Nanotube
CVD	Chemical Vapor Deposition
EE	Electroless Etching
EQE	External Quantum Efficiency
FETs	Field Effecting Transistor
FF	Fill Factor
IQE	Internal Quantum Efficiency
Jsc	Short Circuit Current
LEDs	Light Emitting Diodes
MACE	Metal Assisted Chemical Etching
MOCVD	Metal Organic Chemical Vapor Deposition
NPs	Nanoparticles
PECVD	Plasma Enhanced Chemical Vapor Deposition
$POCl_3$	Phosphorous Oxychloride
PSG	Phosphosilicate Glass
QDs	Quantum Dots
R_s	Series Resistance
R_{sh}	Sheet Resistance

RCA	Radio Corporation of America
RMS	Root Mean Square
SEM	Scanning Electron Microscopy
Si NWs	Silicon Nanowires
STC	Standard Test Condition
TEM	Transmission Electron Microscopy
V_{oc}	Open Circuit Voltage

CHAPTER 1

INTRODUCTION

1.1 Current Status of Photovoltaic Industry

Nowadays, scientists consider photovoltaic technology as the most realistic way to compensate the growing energy needs of the future. Solar cells, directly convert sunlight (referred to as an infinite source of energy) into electricity. In addition to being a natural source of energy, critical facts such as global warming and pollution also increase the demand for the solar cells. Almost, more than 80% of the energy is obtained from fossil fuels [1]. Greenhouse gases that result from fossil fuels are the main source of pollution and health problems and they also lead to global warming. Furthermore, fossil fuels are not renewable. In other words, when they burn, they cannot be re-evaluated. By growing the awareness of the need to find alternative energy sources and considering solar cell advantages compared to other energy sources, more interest expanded towards photovoltaics. This caused an increase in production rate of photovoltaics by 15-20% resulting in a further reduction in production costs in the late 1990's [2]. Reduced cost opened new fields of research and application so that great diversity of materials including, gallium arsenide, crystal silicon, amorphous silicon as well as semiconducting polymers have been applied in photovoltaic technology. The development of photovoltaic technology during last forty years and the related cell efficiencies is shown in Figure 1.1 [3].
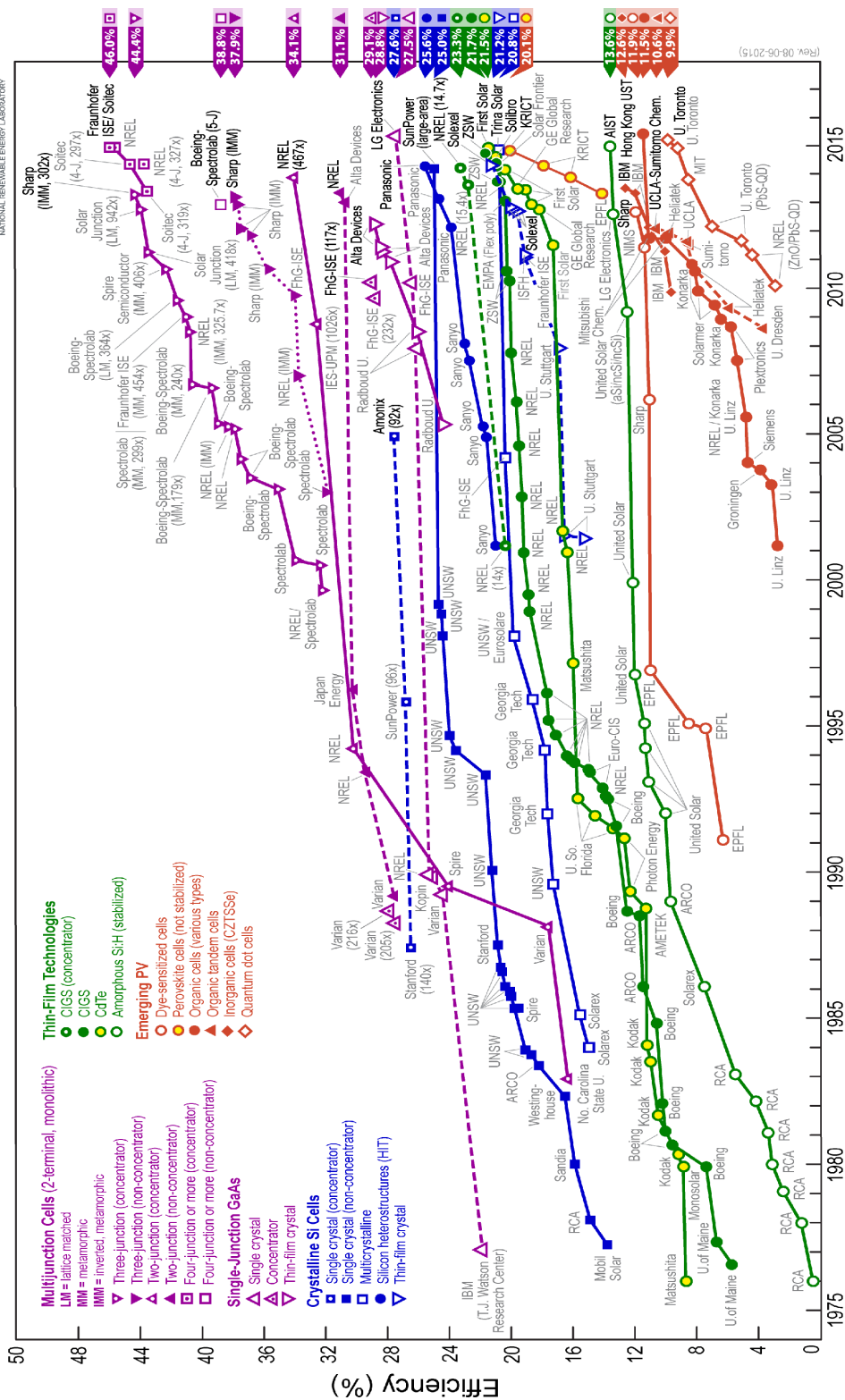
Figure 1.1 NREL's best research cell efficiencies [3].

Solar cell technologies are classified in to three main groups. First generation solar cells are Si wafer based solar cells. Both mono and multicrystalline Si wafers are in use as base materials for this type of solar cells. Despite its lower efficiency values, multicrystalline cell production is preferable due to lower fabrication costs in comparison to the monocrystalline solar cells.

Second generation solar cells are thin film solar cells. In these cells, active layers are deposited on glass or flexible substrates in form of thin films (a few microns thick) by a physical or chemical process depending on the type of material. Amorphous Si, copper indium gallium selenide (CIGS) and cadmium telluride (CdTe) are major thin film materials that are commercially used as active layers in thin film solar cells. Thin film materials have high absorption coefficient, so a few micron thick material would be enough to absorb the incoming light. This fact decreases the material consumption as well as cost significantly; but, their low efficiencies could not compete with crystal Si cells. Moreover, thin film solar cells show instability problems resulted from sunlight exposure.

In third generation solar cells, fabrication of very cheap cells with high conversion efficiencies is targeted and a variety of novel materials including solar dye, multi-junction concepts (tandem solar cells), quantum structure, conductive plastics, solar inks and also organic materials have been investigated. Very cheap cells with moderate efficiency values (10-15%) in addition to very high efficiency (>30%) and expensive systems are all considered as third generation solar cells [3]. Perovskite solar cells are the recently added to the group of third generation solar cells .They include a perovskite structured compound most commonly a hybrid organic-inorganic based material as the light-harvesting active layer. High efficiency (20.1%) and low production costs make them a commercially attractive option [3].

Global Market Share by PV Technology
from 1990 to 2013
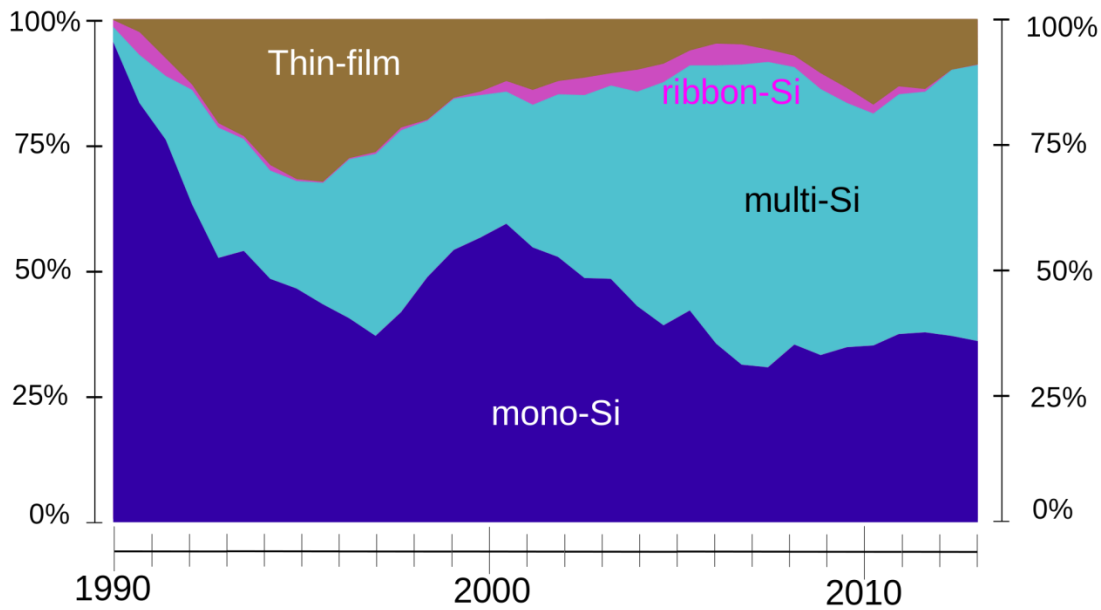
Figure 1.2 Global market share by photovoltaic technology since 1990 [5].

Although many studies have been conducted in laboratories to fabricate variety of solar cells using different materials, most of the solar cells that are commercially exist are bulk type single or multi crystalline Si solar cells [4]. By analyzing the market share of different photovoltaic technologies which is shown in Figure 1.2, it is concluded that crystalline Si technology have been dominating the market for more than 40 years and has reached a market share of 83% by the year 2010 [5].

Si is stable and relatively low cost element processed from sand, which is the most abundant material forming the Earth's crust. Moreover, there is extensive experience and knowledge in processing this material. Another benefit of Si solar cells is their high efficiency and compatibility with manufacturing technologies that are currently in use within industry. Therefore, fascinating properties of Si makes the reason of Si photovoltaic market share domination evident.

1.2 Solar Irradiation

Solar irradiation is the energy of the sun light incident on Earth's surface, which is approximately 1360 W/m^2 outside the atmosphere. It is absorbed, reflected or scattered by dust particles and gas molecules such as carbon dioxide (CO_2) and water vapor (H_2O) while travelling through the atmosphere. Highly modified solar spectrum is shown in Figure 1.3 [6].
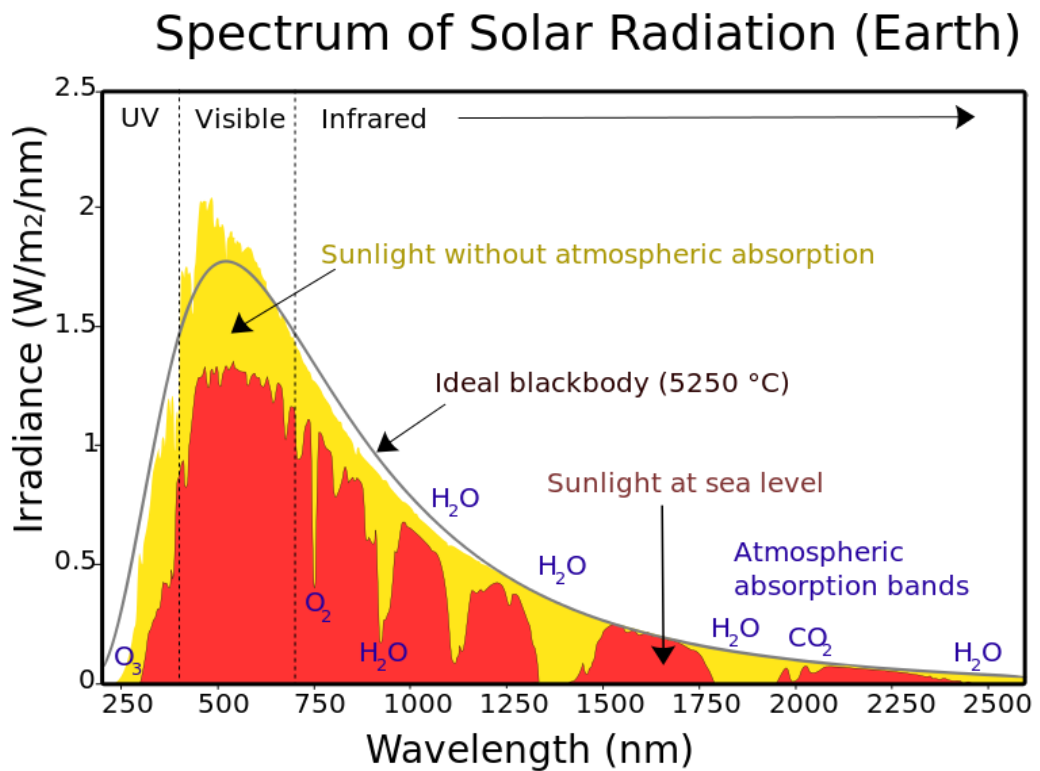
Figure 1.3 Solar spectrum on the surface of the Earth [6].

Air mass (AM) defines the ratio of the path length that light travels through the atmosphere to the path length that it travels when the sun is directly overhead.

AM0 defines the solar radiation just outside the atmosphere, whereas AM1 and AM1.5 condition refers to the sun positioned along the vertical direction and at an angle of 48.2^o with the vertical axis respectively (Figure 1.4). Following equation is applied to calculate air mass;

$$\text{Air mass (AM)} = \frac{1}{\cos\theta} \qquad\qquad \text{(Eq.1.1)}$$

θ is the angle between sun and its vertical axis, also called as zenith angle. At AM1.5 condition, irradiance outside the atmosphere is taken as 1000 W/m^2, which is named as 1 SUN. AM1.5 condition, at T=25°C is taken to be standard test conditions (STC) for solar cell measurements.
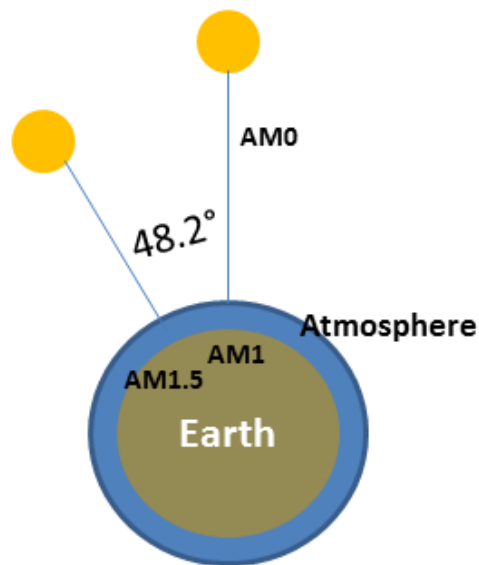
Figure 1.4 Schematic of AM0, 1 and 1.5 conditions.

1.3 Solar cell Parameters and Characteristics

1.3.1 Current- Voltage Characteristics

Without illumination, solar cell is a simple diode and has the same electrical characteristics. By introducing light to the cell, the I-V curve of the diode shifts as the cell begins to generate power. So the current of a dark diode changes to:

$$I = I_0 \left[\exp\left(\frac{qv}{nkT}\right) - 1\right] - I_L \qquad \text{(E.q. 1.2)}$$

,where; I_0 is reverse saturation current determined by diode properties, q is electron charge, V is voltage applied between the terminals of the cell, k is Boltzmann constant, T is cell temperature in Kelvin, I_L is the light generated current and I is the net current flowing through the cell. The effect of light on the characteristics of a p-n junction is shown in Figure 1.5.

1.3.2 Conversion Efficiency

Efficiency is defined as the ratio the output energy of the cell to input energy from the sun. It is usually used to compare the performances of the cells and depends on the intensity of incident light and cell temperature.
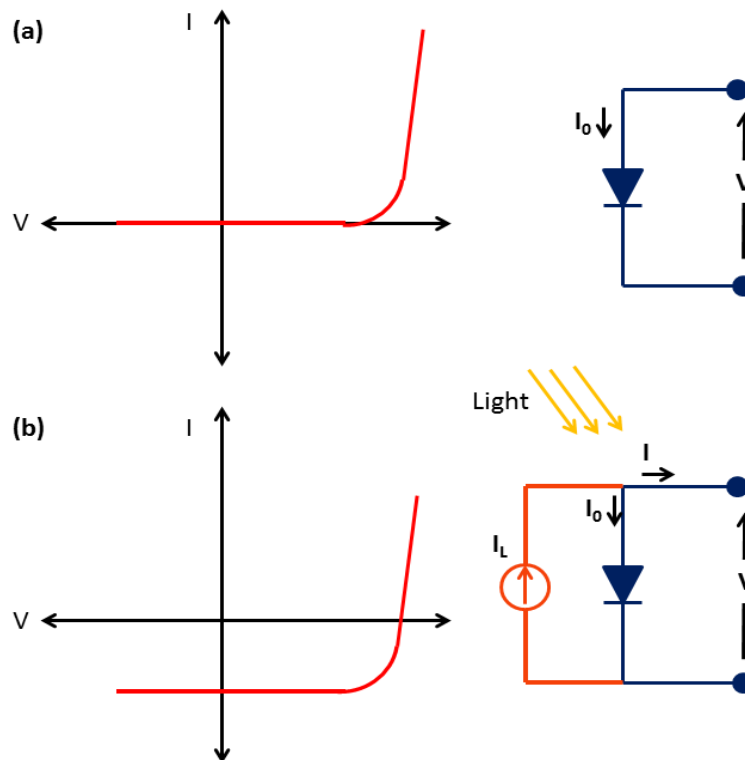
Figure 1.5 Effect of light on the current-voltage characteristics of a p-n junction.

It can be calculated from the equation below;

$$\eta = \frac{V_{oc} \, J_{sc} \, FF}{P_{in}} \qquad (E.q.1.2)$$

$$P_{max} = V_{oc} \, J_{sc} \, FF \qquad (E.q.1.3)$$

, where V_{oc} is the open-circuit voltage, J_{sc} is the short-circuit current density, *FF* is the fill factor and η is the efficiency. The input power for efficiency calculations is 1 kW/m^2 or 100 mW/cm^2.

1.3.3 Open Circuit Voltage

Open circuit voltage (V_{oc}), is the maximum voltage that can be obtained from solar cell and it occurs when no current flows through the device. It is govrned by the equation below;

$$V_{oc} = \frac{nkT}{q} \, Ln \left(\frac{I_L}{I_0} + 1 \right) \qquad (E.q.1.4)$$

V_{oc} mostly depends on the saturation current (I_0) or on the amount of recombination in the solar cell. In high quality single crystal Si solar cells, V_{oc} is up to 730 mV under one sun and AM1.5 conditions, while this amount is around 600 mV for multi crystalline Si cells. V_{oc} value of a solar cell is shown in the I-V curve demonstrated in Figure 1.6.
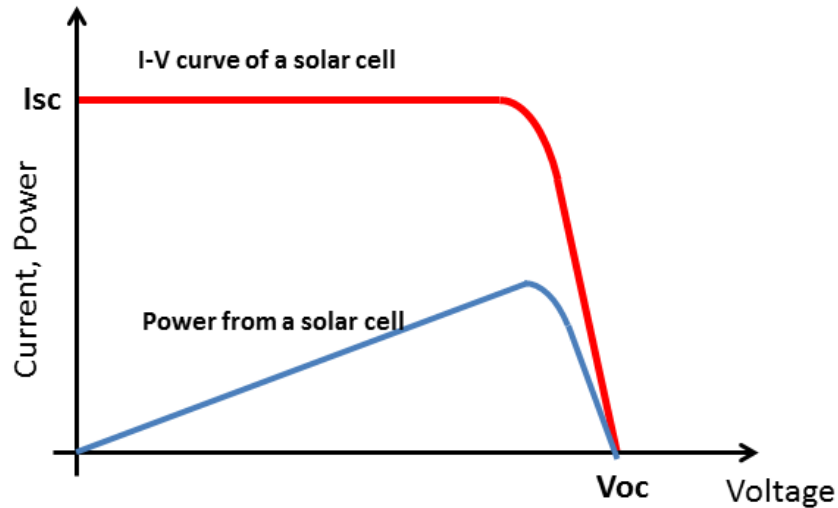
Figure 1.6 I-V curve of a solar cell showing the short-circuit current.

1.3.4 Short Circuit Current

Short circuit current (I_{sc}) is the current flowing through the cell under zero voltage. By setting V to zero in Eq. 1.2 I_{sc} value will be equal to the light generated current I_L. I_{sc} value of a solar cell is shown in the I-V curve demonstrated in Figure 1.6.

I_{sc} depends on a number of factors such as the area of the solar cell, intensity and spectrum of the incident light, optical properties of the cell (absorption and reflection) and collection probability.

1.3.5 Fill Factor

The area under I-V curve is equal to output power of the cell and graphically more square-like curve will result in a higher power output and thus higher efficiency values. Fill factor (FF) is defined as the ratio of the maximum power from the solar cell to the product of V_{oc} and I_{sc} , which can be obtained from the equation below;

$$FF = \frac{V_{mp} \, I_{mp}}{V_{oc} \, I_{sc}} = \frac{\text{Area A}}{\text{Area B}} \tag{E.q.1.5}$$

Figure 1.7 shows the output current and power of the solar cell as a function of the voltage. The maximum power point is shown in the picture as well.
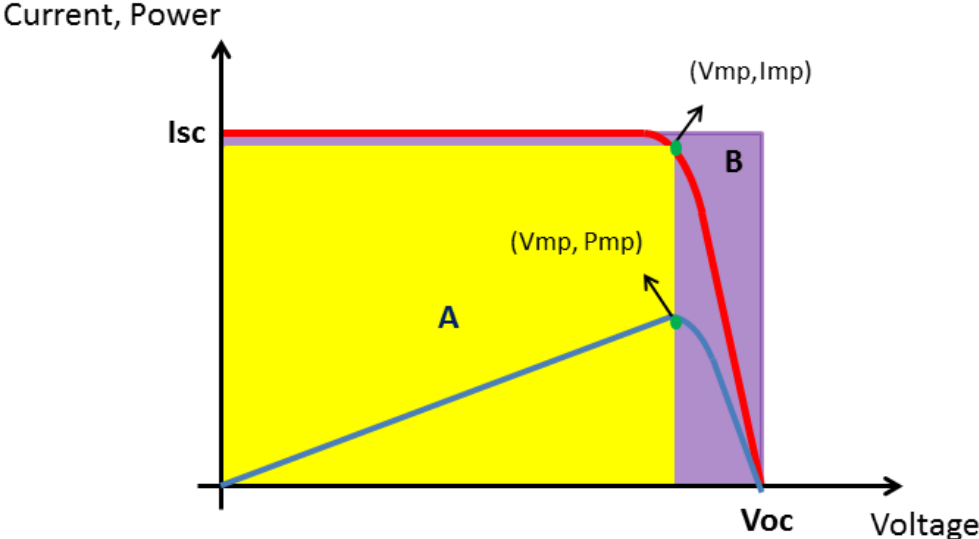
Figure 1.7 Output current (red line) and power (blue line) of a solar cell as a function of voltage. Maximum power point (V_{mp} ,I_{mp}) is shown in the picture.

1.3.6 Series Resistance

Generated light in the solar cell encounters resistance while passing through the semiconductor (active layer), metal (electrode)-semiconductor interface and also metal contact. Overall resistance of the structure is called as series resistance (R_s) and is defined by equation below;

$$R = \left(\frac{1}{\left(\frac{dI}{dv} \right)} \right)_{v=v_{oc}} \qquad\qquad (E.q.1.6)$$

Figure 1.8 shows an equivalent circuit of a solar cell with series resistance. For the better performance of the cell it is desirable to minimize the series resistance. R_s can be easily calculated from derivative of the measured I-V at $V_{oc} = 0$.

10
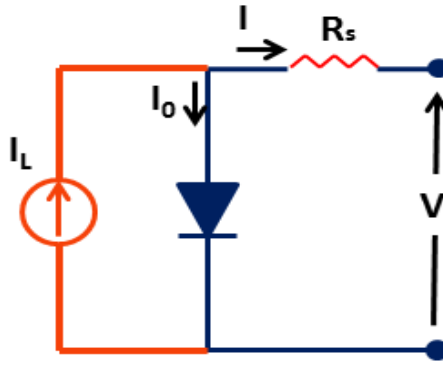
Figure 1.8 Equivalent circuit of solar cell with series resistance.

1.3.7 Shunt Resistance

Shunt resistance (R_{sh}) could be mainly attributed to the manufacturing imperfections rather than poor cell design. R_{sh} value is as an evidence of current leakages within the cell. It indicates the presence of alternative paths for the light generated current passing through cell rather than being collected at an external load. Shunt resistance could be expressed as;

$$R_{sh}=\left(\frac{1}{\left(\frac{dI}{dv}\right)}\right)_{V=0} \qquad (E.q.1.7)$$
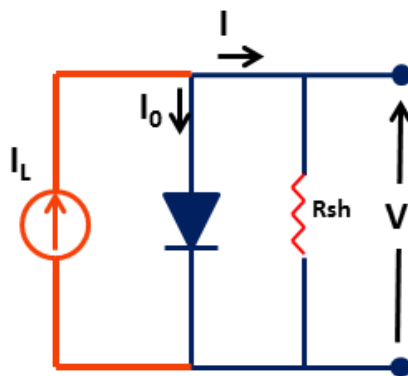
Figure 1.9 Equivalent circuit of a solar cell with shunt resistance.

For better cell performance, it is desirable to keep R_{sh} as high as possible.

1.3.8 Quantum Efficiency

Quantum efficiency (QE) is the ratio of the number of carriers collected by the solar cell to the number of photons incident on the solar cell. In ideal case, in which all incident photons are absorbed and all generated charge carriers are collected by the cell, QE would be unity as shown in Figure 1.10 [7]. For the non-ideal case, there will be a reduction in the QE for shorter wavelengths due to front surface recombination. Also, for longer wavelengths, low absorption of the light and short diffusion length of the generated charge carriers will reduce QE. Moreover, reflection losses and poor collection of generated carriers will result in a decrease of the QE along the whole spectrum. For external quantum efficiency (EQE), optical losses like reflection and transmission are taken into consideration. For internal quantum efficiency (IQE), on the other hand, optical losses are excluded from the calculation.
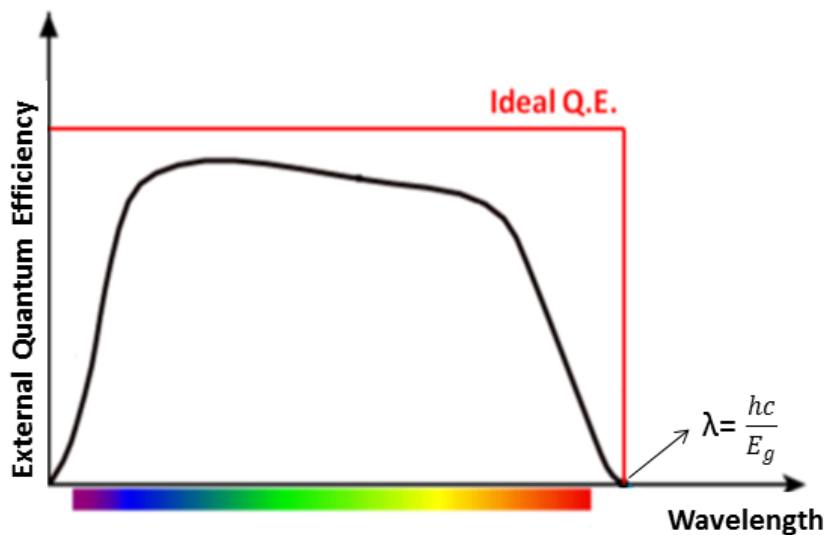
Figure 1.10 A typical EQE plot for Si solar cell [7].

1.4 Fabrication of Single Crystalline Si Solar Cells

In photovoltaic devices, electron-hole pairs are generated within the semiconducting layer through the absorption of light. The carriers generated within a diffusion length of depletion region are separated by the internal electric field and collected by two electrodes to give rise to photocurrent. Crystal Si solar cells consist of an active p-n junction layer of n-type emitter ($< 1\mu m$) on a thick p-type single or multi-crystal Si wafers. The schematic of fabrication steps of crystal Si solar cells are demonstrated in Figure 1.11. Fabrication steps will be explained briefly.
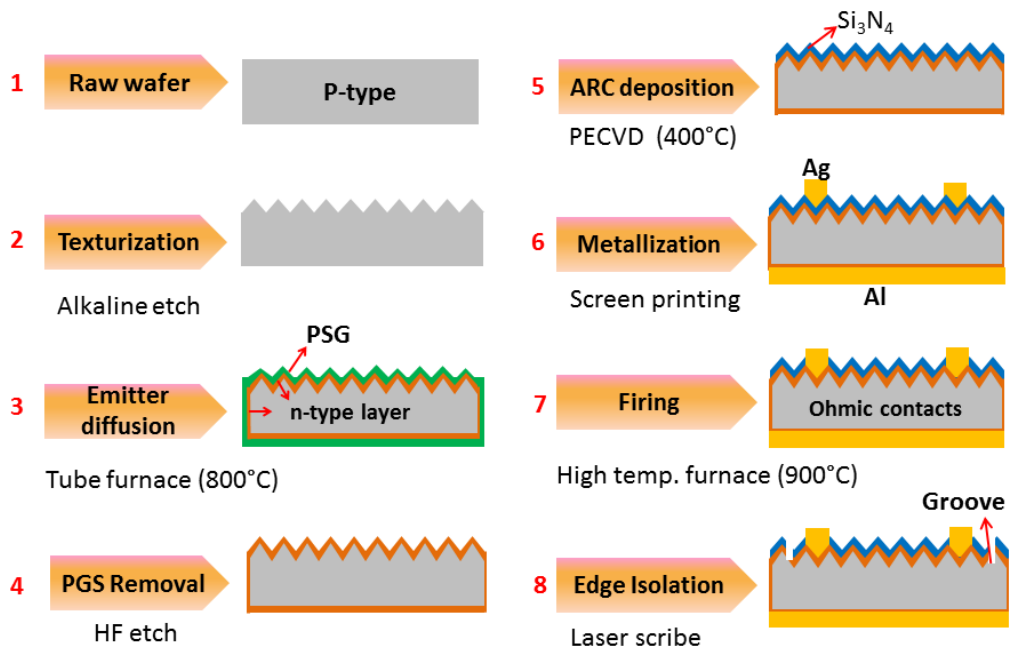
Figure 1.11 Fabrication steps of conventional crystal Si solar cells.

13

1.4.1 Surface Texturing

Si has a band gap of 1.12 eV, which corresponds to a wavelength of 1100 nm and photons with energy less than 1.12 eV will be insufficient to be absorbed by Si to generate electron-hole pairs. Therefore, almost 50% of the incident solar radiation cannot be absorbed by Si. Absorption coefficient and depth of Si within the wavelength region of 200-1400 nm is provided in Figure 1.12. According to the figure, photons up to 1100-1200 nm can be absorbed by Si when the thickness of Si wafers is around 0.1-0.2 cm. Increasing Si wafer thickness enhances light absorption at the same time it also increases the probability of carrier recombination by enlarging the path length travelled by the generated carriers [8].
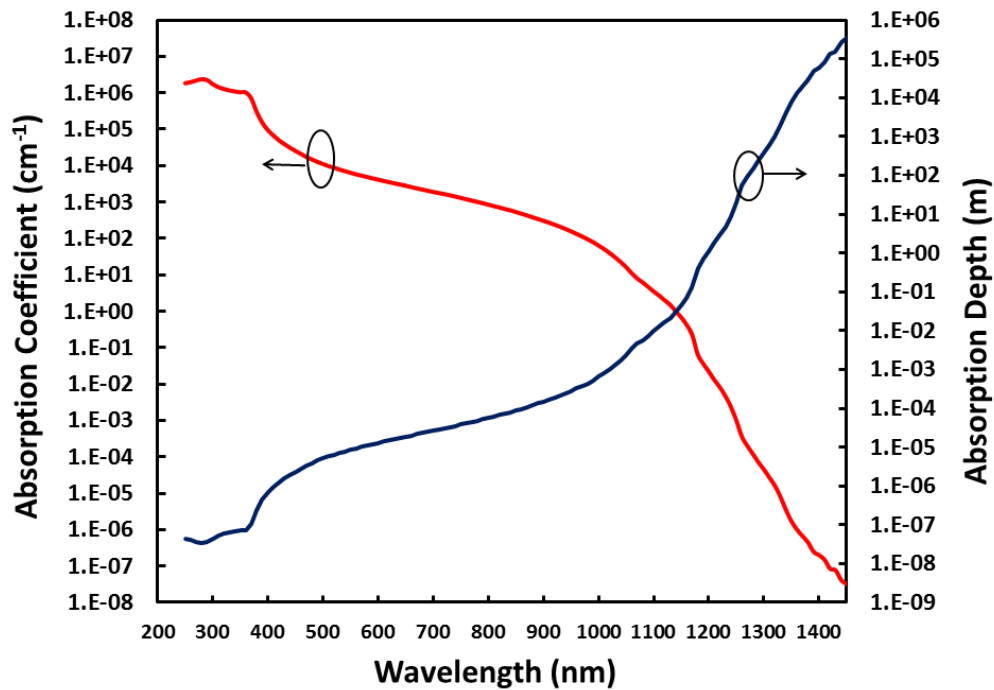
Figure 1.12 Absorption coefficient and depth of intrinsic Si at 300 °K [8].

Optical path length is the distance travelled by an unabsorbed photon before escaping out of the material. Light trapping strategies are applied to make optical path length longer than the actual device thickness, which results in a mechanically thin but optically thick device. One effective and practical method for light trapping is texturing of the Si wafer surface, which can be obtained by wet chemical etching. In

Si wafers with pyramidal surface, incident light refracted in non-perpendicular angle with the surface so that the light will make several internal reflections inside the sample. This will increase the probability of absorption of the light and carrier generation, as schematically illustrated in Figure 1.13.

a)   b)
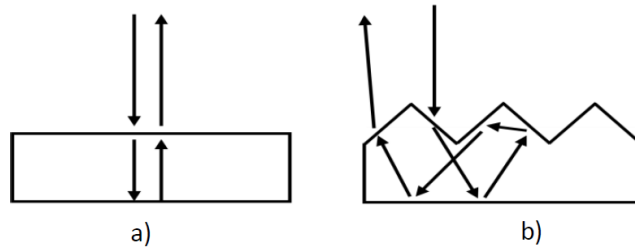
Figure 1.13 Reflection of light from (a) flat and (b) textured Si wafers.

Another advantage of texturing is reducing of the intensity of reflected light due to double light bouncing on the surface, therefore total reflectivity of the surface decreases from R to R^2, where R is reflectance with a value between 0 and 1 [Figure 1.14].

a)   b)
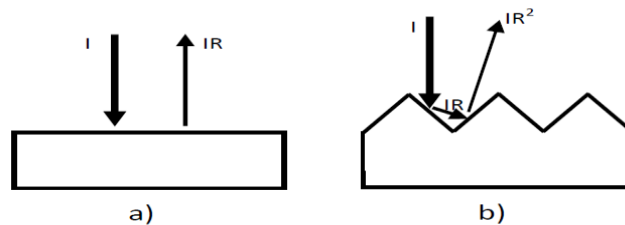
Figure 1.14 Intensity of reflected light decreases from (a) IR in planar Si to (b) IR^2 in textured surface due to double bouncing.

During anisotropic etching of Si using potassium hydroxide (KOH) solution, the following equation occurs [9];

$$Si + 4OH^- \rightarrow Si(OH)_4 + 4\ e^-$$ (Eq. 1.8)
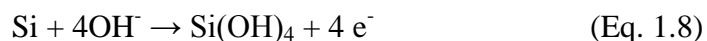
During etching process, pyramids with (111) walls will form as a result of different etching rates in different crystallographic orientations due to different planar atomic

densities. For example, etching is faster along (110) direction compared to (100) and slowest along (111) direction (Figure 1.15).
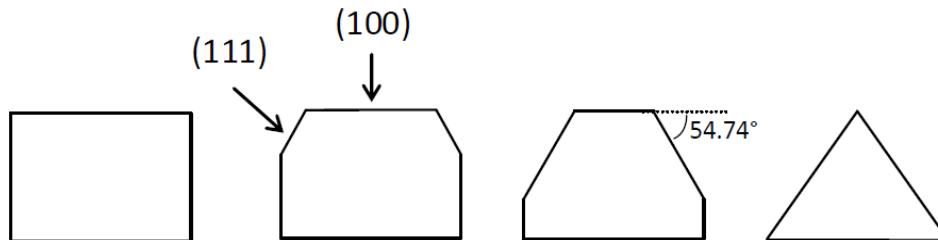
Figure 1.15 Anisotropic etching process of (100) oriented Si wafer. (100) planes are etched faster than (111) planes, until pyramid structures are formed and no (100) planes remain.

1.4.2 Solid State Diffusion (Doping)

Doping is the next critical step in Si solar cell fabrication in which p-n junction is created via solid state diffusion. In doping process, the electrical properties of a semiconductor material can be changed by adding impurity atoms into crystalline lattice. It will be accomplished by breaking lattice bonds and reformation of bonds between the other lattice atoms and impurity atoms. Therefore, it requires high process temperatures between 800-900°C.

Si belongs to fourth group of the periodic table, which means it makes four covalent bonds to its four nearest neighbouring atoms. For n-type doping of Si, fifth group elements like phosphorous (P) with five valance electrons is usually used. By adding P atom to the system, four valance electrons of it make covalent bonds with Si atoms; but, the fifth electron which does not firmly bond to P atom can easily move throughout lattice even at room temperature. This increases conductivity compared to the intrinsic case. In the case of p-type doping of Si, third group elements such as boron (B) is commonly utilized. All three valance electrons of B contribute to covalent bonds with Si atoms and the missing electron or additional hole will increase the lattice conductivity.

In a standard solar cell structure, n-doped layer is formed on the surface of a p-doped Si wafer using liquid phosphorus oxychloride ($POCl_3$) as phosphorous source. Figure 1.16 shows the schematic of a tubular diffusion furnace used for n-type doping of Si wafers. $POCl_3$ is carried by nitrogen (N_2) gas to the furnace and oxygen gas (O_2) is used to help $POCl_3$ deposition according to the chemical equations;

$$4\ POCl_3 + 3\ O_2 \rightarrow 2\ P_2O_5 + 6\ Cl_2 \qquad\qquad \text{(Eq. 1.9)}$$

$$P_2O_5 + Si \rightarrow SiO_2\ (P) \qquad\qquad \text{(Eq. 1.10)}$$
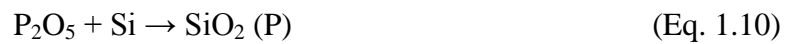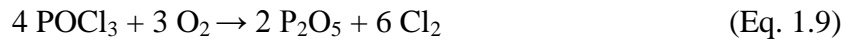
P atoms are firstly, embedded into oxide layer and then diffuse towards the wafer by the concentration gradient. The phosphosilicate glass (PSG) layer formed on the surface is removed from the surface following the doping process.
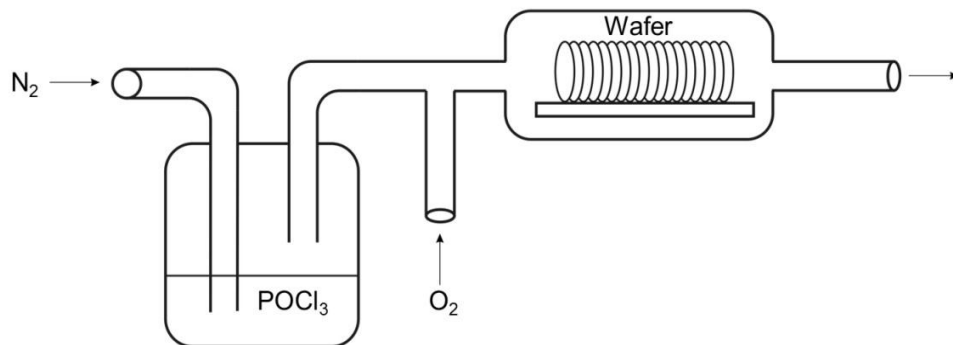
Figure 1.16 Tubular diffusion furnace for solid state diffusion.

1.4.3 Antireflective Coatings (ARC)

Reflectance spectrum of bare Si is shown in Figure 1.17 [10]. The average reflectance of Si is 35% in the visible range (400-700nm). In a solar cell configuration, since reflective losses are detrimental to photovoltaic conversion efficiency, it is desired to decrease the reflectance. This will increase the number of absorbed photons and thus current output of the device.
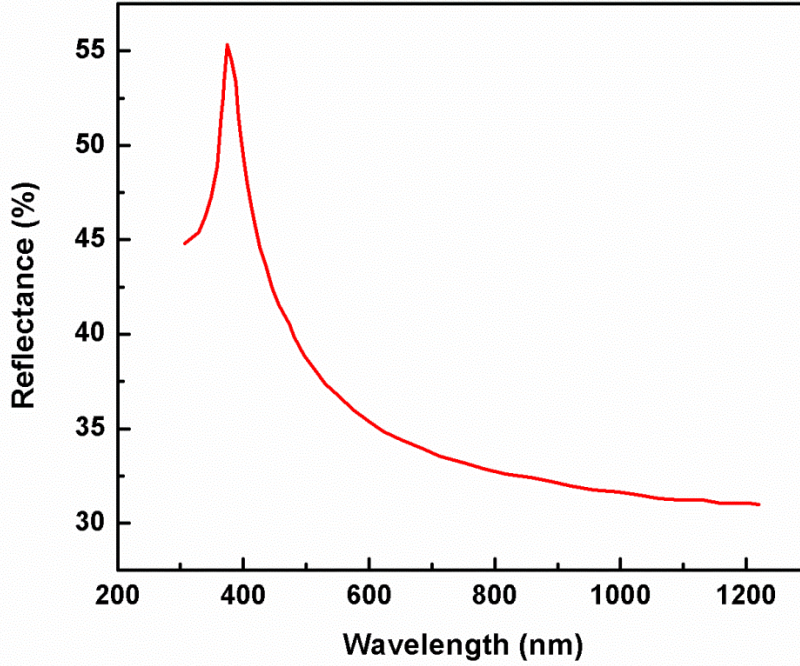
Figure 1.17 Reflectance spectrum of bare Si [10].

In solar cells, ARCs are applied to prevent light reflection from the cell surface. They cause destructive interference between rays reflected from the substrate and the AR film, hence the total reflected intensity drops to zero. When light travels from a medium with refractive index of n_0 to a substrate with refractive index of n_s, the reflectance, R, is given by;

$$R = \left(\frac{n_0 - n_s}{n_0 + n_s}\right)^2 \qquad \text{(Eq. 1.11)}$$

If there is an AR layer at the interface of two mediums, reflection changes as;

$$R = \frac{(n_0 - n_s)^2 + \left(\frac{n_0 n_s}{n_a} - n_a\right)^2 \left(tan\frac{2\pi n_a t cos\theta}{\lambda}\right)^2}{(n_0 + n_s)^2 + \left(\frac{n_0 n_s}{n_a} + n_a\right)^2 \left(tan\frac{2\pi n_a t cos\theta}{\lambda}\right)^2} \qquad \text{(Eq. 1.12)}$$

, where n_a is the AR layer refractive index and θ is the angle of incidence. For normal incidence ($\theta = 0$) the reflectance makes minimum at;

$$n_a = \sqrt{n_s n_0} \qquad \text{(Eq. 1.13)}$$

The minimum thickness of a AR coating used for destructive interference is given by;

$$t = \frac{\lambda}{4 n_a} \qquad \text{(Eq. 1.14)}$$

Both the refractive index and thickness of the AR film can be calculated using equations above. By assuming $n_s = 3.44$ for Si and $n_0 = 1$ for air, the optimum ARC refractive index is calculated as;

$$n_a = \sqrt{3.44} = 1.87 \qquad \text{(Eq. 1.15)}$$

The thickness of the film with an index of 1.87 with reflectance minimum at 600 nm is found as;

$$t = \frac{600}{4 \times 1.87} = 80.2 \text{ nm} \qquad \text{(Eq. 1.16)}$$

600 nm is chosen because the spectral irradiance of the solar spectrum is the highest at this wavelength. The reflectance spectrum for an ARC with a refractive index of 1.87 and thickness 80 nm can be plotted using equations above, as shown in Figure 1.18.
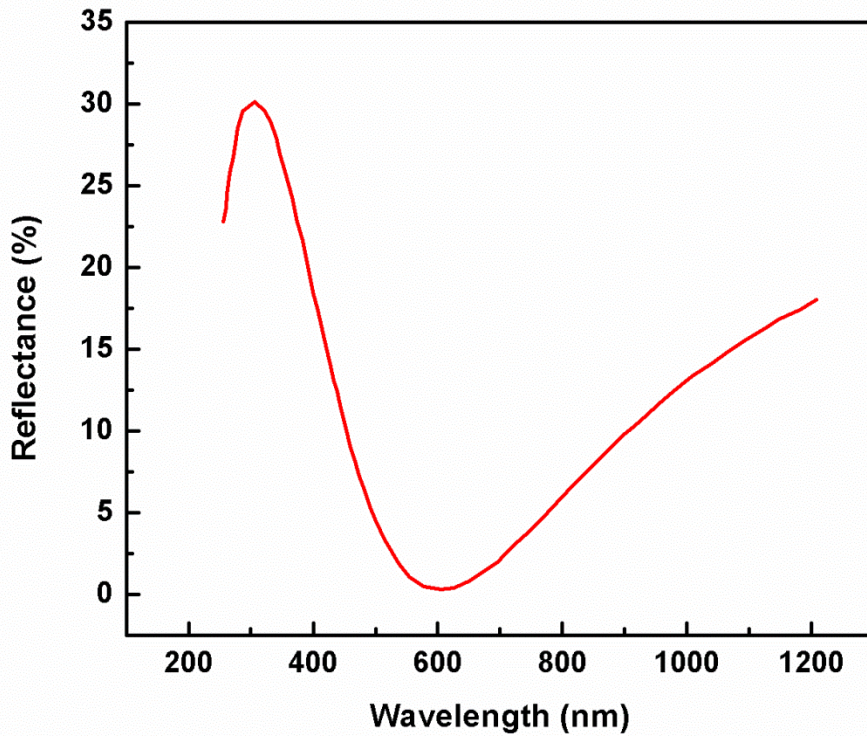
Figure 1.18 Reflectance spectra of Si wafer with an ARC [9].

It is obvious in Figure 1.17 that the average reflectance is below 15% and in 600 nm it is nearly zero, which reveals the importance of using of ARC for an efficient solar cell. In conventional Si solar cells, a thin layer of Si nitride (Si_3N_4) layer (n_a = 2.00) with a thickness of 80 nm is used as the ARC. Si_3N_4 deposition on cells is carried out by a PECVD system operating at temperatures between 300-400 °C using silane (SiH_4) and ammonia (NH_3) gases. The chemical process during the deposition is given as;

$$3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 24\ H_2 \qquad \text{(Eq. 1.17)}$$
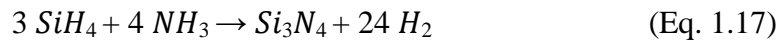
From the consideration above, the desired thickness of the Si_3N_4 layer for a wavelength of 600 nm can be found as;

$$t = \lambda 4 n_a = 600 \times 4 \times 2 = 75\ nm \qquad \text{(Eq. 1.18)}$$

1.4.4 Metallization

The function of metallic contacts is to collect light generated carries from the cell. One of the essential factors in fabricating high efficiency solar cells is to minimize resistive losses resulted from emitter and top grid contact. Figure 1.19 (a), shows top contact design and Figure 1.19 (b) is a schematic of current follow direction and resistive components in conventional Si solar cell. Fortunately, to a great extent, series resistance can be overcome by optimizing top contact design for each type and size of solar cell.
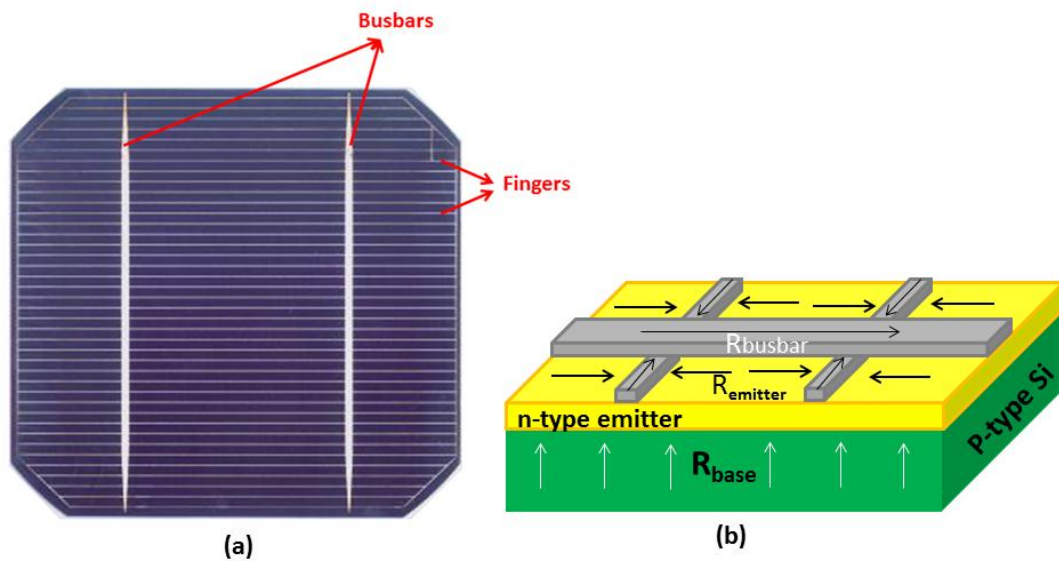
Figure 1.19 (a) Top contact design and (b) schematic of current flow directions and resistive components in a solar cell.

Top grid contact consists of busbars and fingers. Busbars are directly connected to the external load and fingers collect current from all cell surface area and deliver it to the busbars. Some important issues in designing cell top contacts are as follows;

i. Minimizing resistive losses in emitter, which results from the spacing between finger bars. Therefore, fingers with short separation are desirable.

ii. Minimizing grid resistance, which is determined by the resistivity of the metal used in contacts. Regarding this, high aspect ratio and low resistivity metals are required. Top surface metal contact with different aspect ratios is shown in Figure 1.20.

$$Aspect\ ratio = \frac{heigth}{width}$$
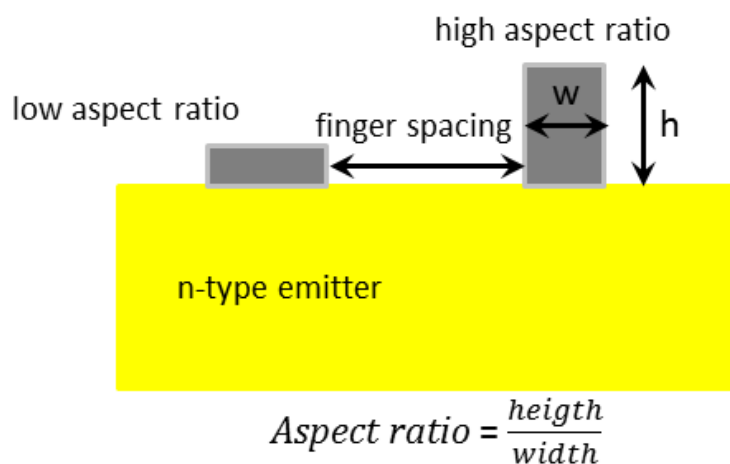
Figure 1.20 Top surface contact schemes.

In solar cell industry, screen printing method is used to deposit the top and rear contacts on Si solar cells. In this method, a squeegee is applied to force a paste through the mask, which is transparent to paste in some regions to print pattern onto Si substrates. Printing quality can be affected by parameters like, squeegee pressure, squeegee speed, snap off between screen and the substrate, operation temperature and the separation speed. Therefore, this process should be carried out in a climatically controlled room.

One of the disadvantages of screen printing method is the low aspect ratio of the contacts. Low aspect ratio contacts reduce the shadow effect but as previously mentioned, high aspect ratio grid lines are needed to decrease the series resistance. Therefore an optimum condition is used during screen printing process. Standard masks are designed, manufactured and utilized in metallization process. Generally, front side metallization mask is used to form 2-3 busbars and 65-75 fingers of silver (Ag) paste. Back side metallization mask allows full coverage of the back side of the cells with aluminum (Al) paste.

Metallization pastes include metal molecules, resin and some other solvents. Usually Al, Ag and Al/Ag mix pastes are used in standard metallization. Each paste has different viscosity and a firing recipe. An annealing process should be performed after screen printing to dry the pastes. 250 °C would be enough for annealing step.

Firing is the last step in metallization process, which is the most important step in this process. Metal solidification, creation of back surface field (BSF) and metal

diffusion through Si_3N_4 ARC take place in firing process. A belt furnace with different heating zones is used in this process to rise the temperature of the cells to 850-950˚C and then rapidly cool them to room temperature.

1.4.5 Edge Isolation

In diffusion furnace, all the surfaces of the Si wafer including both sides and edges become n-type doped as shown in Figure 1.21 (a). This causes electron hole pairs to recombine, decreasing the cell performance. Edge isolation solves shortcutting problem by electrically isolating the front and back sides of the cell from each other. This is accomplished by laser scribing the front surface edges until reaching the p-type region, as shown in Figure 1.21 (b).
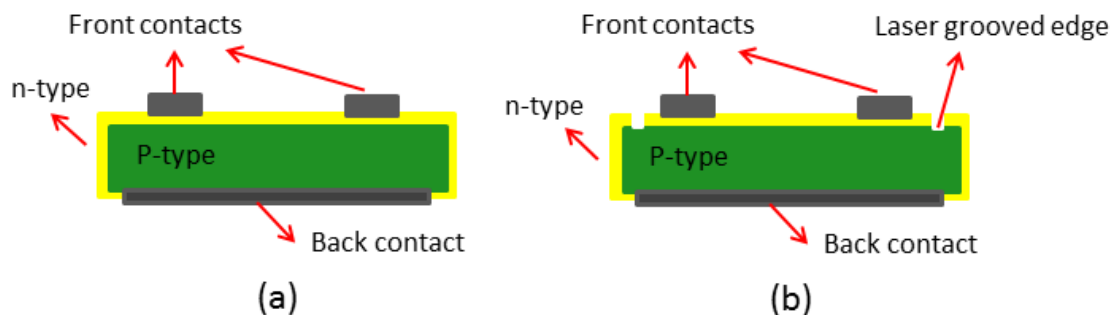
Figure 1.21 Schematic of a solar cell (a) before and (b) after edge isolation by laser grooving.

1.5 Nanostructure in Solar Cells

Si impurities reduce the Si solar cell efficiency. The use of high quality Si in solar cell production increases the manufacturing costs significantly. Therefore, it is desirable to have both reduction in solar cell module manufacturing cost and enhancement in conversion efficiency of the cells at the same time but it cannot be accomplished by using the conventional materials and solar cell structures. Moreover, the shortage of the feedstock of high-purity Si is predicted in the near future. Therefore, many investigations are in progress to develop solar cells with low manufacturing cost, less material consumption and high conversion efficiency. In

order to produce equally efficient solar cells using low cost and impure Si material instead of pure Si, researchers should develop promising alternatives. One of these alternatives could be employing new nanostructured materials instead of bulk materials in fabrication of the solar cells.

Nanostructured materials exhibit different properties than bulk or thin films of the same compound. Their large surface to volume ratio and quantization effect can provide many advantages. Nanostructures are developed to be used in different optoelectronic devices to manage to light via plasmonic enhancement [11] and light trapping effect [12].

Nanostructured solar cells are based on nanostructures such as nanowires, nanotubes, nanoparticles and quantum dots in particular. Although there are challenges to overcome, the potential benefits are still worth the efforts. Remarkable investigations are conducted to develop ordered nanostructured materials [13]. One dimensional (1-D) nanowire, nanotube and nanorod structures, which includes highly ordered titanium dioxide (TiO_2) nanotubes, carbon nanotube (CNT) and Si nanowire arrays [14–17] and bandgap-tunable zero-dimensional (0-D) nanomaterials, such as cadmium sulfide (CdS) [18-20], lead sulfide (PbS) [21, 22], bismuth sulfide (Bi_2S_3) [21, 23], cadmium selenide (CdSe) [24] and indium phosphate (InP) [25] quantum dots (QDs) have represented exceptional optical and electronic properties that provide opportunities for revolutionary developments in photovoltaic devices. Moreover, promising characteristics and geometry of 1-D nanostructures provide direct path for charge transport and large surface areas for light harvest. For example, the mobility of electrons in 1-D nanostructures is typically several orders of magnitude higher than that commonly used in semiconductor nanoparticle films [14]. In photovoltaic devices, in addition to light trapping effect, coaxially doped vertical nanorod arrays, improves the photo carrier collection orthogonalizing the direction of light absorption and electron-hole pair transport. The schematic of the process is shown in Figure 1.22.
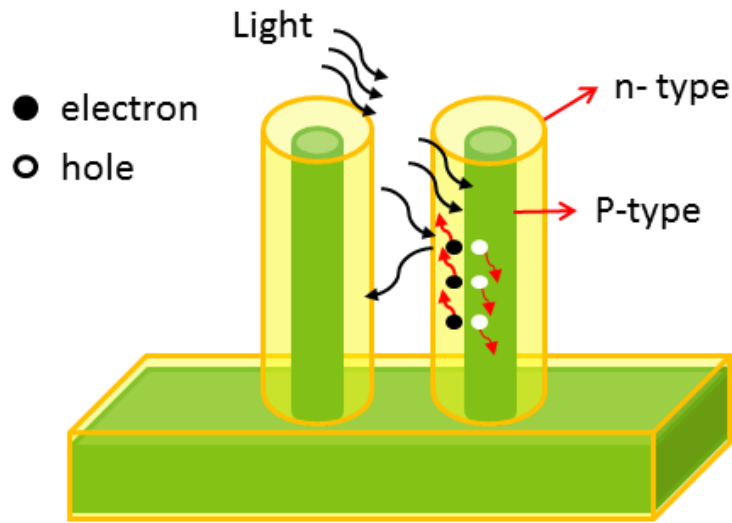
Figure 1.22 Schematic of light interaction with radial junction nanorod solar cell.

Metallic nanoparticles (NPs) can covert light into electricity by plasmonic resonances. This can be accomplished by prolonging optical path inside sample (far field effect), locally enhancing energy conversion (near field effect) and by creating high energy charges and transferring them to the cell (Figure 1.23).
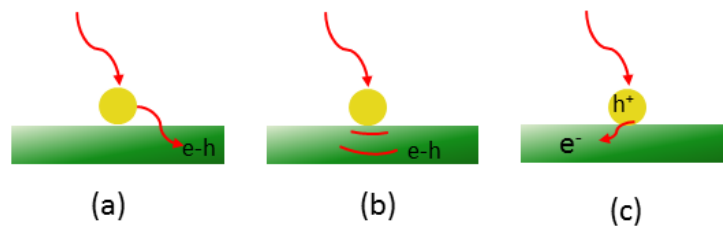
Figure 1.23 Schematics of light interaction with metal NP through (a) far field effect (b) near field effect and (c) transferring high energy charges to cell.

This thesis addresses synthesis and application of the 1 D nanostructures such as zinc oxide (ZnO) nanorods, silver (Ag) and Si nanowires (NW) and incorporation of these nanomaterials as different components of Si solar cells to improve conversion efficiency and decrease fabrication expenses. As previously explained in Section 1.4, in conventional Si solar cells, ARC (Si_3N_4) is deposited under high vacuum and temperature (400°C) in PECVD system and metallization process is carried out via screen printing of pastes followed by firing at high temperatures (900°C). Both of the

processes are costly and energy consuming; therefore, In Chapter 2 we focused on the use of solution grown ZnO nanorods as antireflective coatings in Si solar cells instead of Si_3N_4 thin film layer. In Chapter 3, the use of transparent and conducting Ag NW network as top electrode of Si solar cells was investigated instead of conventional metallization process.

In Si solar cell fabrication, Si wafer price has great impact on the cell cost. 180 μm thick silicon wafers are usually used for fabrication and reduction in the amount of silicon or wafers thickness would be desirable to reduce the cost. Regarding this, in Chapter 4 the applicability of ultrathin Si wafers decorated with Si nanowires as active layer in homojunction Si solar cells was studied. The aim of this thesis is schematically shown in Figure 1.24.
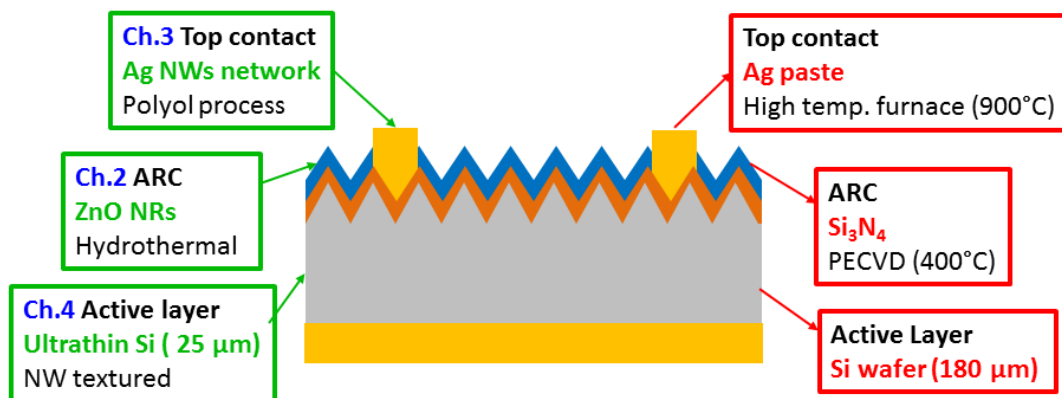
Figure 1.24 Schematic presentation of the aims of the thesis.

CHAPTER 2

ZINC OXIDE NANORODS AS ANTIREFLECTIVE COATINGS FOR INDUSTRIAL SCALE SINGLE-CRYSTALLINE SI SOLAR CELLS

2.1 Introduction

2.1.1 The Role of Antireflective Coatings in Si Solar Cells

Elimination of reflection losses is a fundamental factor in producing high-efficiency solar cells, which results in an enhancement of absorbance of solar irradiance by the cell and higher rate of electron-hole pair generation. [26]. Bare Si surface reflects more than 30% of incident sunlight for wavelengths corresponding to energies larger than the band gap of Si [27]. Thus, optical enhancement techniques such as texturing and the use of an antireflection coating (ARCs) are mostly employed to reduce the reflective losses [28–30].

Ideally, in addition to the reduction in optical losses, ARC layer simultaneously provides a reasonable degree of surface passivation. The goal of passivation of crystalline Si surfaces is to avoid minority carrier recombination due to high defect density at the surfaces and high surface recombination velocities. It has been shown that immersion of Si wafers in hydrofluoric acid (HF) solution would provide high effective carrier lifetime. This is because HF always results in a surface with Si–H bond and virtually no dangling bonds [29]. Similarly, deposition of a protective thin film on crystalline Si also provides passivation, through the satisfaction of bond requirements and minimization of the number of dangling bonds. Surface

recombination is very effectively suppressed by means of silicon dioxide (SiO_2) layer grown through high-temperature (~900°C) oxidation processes [32]; however, high-temperature oxidation has not been implemented into the majority of industrial cell processes. This is because the bulk Si lifetime is highly sensitive to the high-temperature processes, which would increase the recombination of the carriers via traps within the energy gap [34]. Hence, low-temperature surface passivation alternatives are required for the production of industrial scale high-efficiency Si solar cells.

In crystalline Si photovoltaic industry, amorphous silicon nitride (a-$Si_{1\_x}N_x$:H), [34,35] deposited by plasma enhanced chemical vapor deposition (PECVD) method, at temperatures around 400°C, is mostly used for passivation. Besides, with a proper thickness, it is also used as an ARC on the illuminated side of the solar cell [36]. However, when SiN_x is deposited onto a p-type substrate, the short-circuit current density is strongly reduced in comparison to the SiO_2-passivated cell [37]. This is because of the large density of fixed positive charges associated with the SiN_x layer that induce an inversion layer in the p-type Si underneath the SiN_x layer. Aluminum oxide (Al_2O_3) has also attracted a lot of attention because of the negative fixed charge density, which provides an excellent level of surface passivation on low-resistivity p-type and n-type Si wafers [38–40].

ARCs usually consist of one or more dielectric layers with different refractive indexes, either in the form of a quarter wave thickness film that exhibits a wavelength sensitive reduction in reflection due to the interference or as a nanoporous film that takes advantages of light trapping for more broadband response via moth-eye effect [41,42]. Latter involves fabrication of subwavelength structures by a novel nanostructuring technology that necessitates either electron beam lithography or complex etching processes [43–45]. Therefore, the fabrication costs are high and large area applicability remains to be resolved.

2.1.2 ZnO Nanorods as Antireflective Coatings

Nanowire arrays show anti-reflective and light trapping properties. They provide broadband reflection suppression with very little wavelength dependence due to their refractive index gradient allowing impedance matching between Si and air. Si NW arrays with a few microns length have been shown to have strong broadband optical absorption with dark visual appearance [46–48]. It has been followed by the demonstration of the use of indium tin oxide (ITO) nanowires as efficient antireflective coatings for gallium arsenide (GaAs) solar cells [49]. In both of these works, it has been concluded that nanowires provide wide broadband reflection reduction and this property seems to be a common characteristic of nanowire arrays [50,51].

Quite recently, ZnO nanorods have been proved to present excellent antireflection performance [52]. ZnO, is a promising dielectric material with a wide band gap and good optical transparency, appropriate refractive index (n = 2, at a wavelength of 600 nm). Textured ZnO films have been already considered as anti-reflection coatings [53]. The wurtzite structure of ZnO allows easy growth within nanowire morphology due to the surface energetics of its crystal facets [54–56]. ZnO nanowires can be produced using cheap precursors and applicable at low temperatures and over large areas, [57] which makes them attractive candidates for photovoltaic ARCs.

In addition to light trapping effect of ZnO nanowires, gradual transition of the effective refractive index from air (n=1) to Si micropyramids (n=3.4), which is caused by ZnO nanorods (n=2), also results in broadband reflection suppression (Figure 2.1).
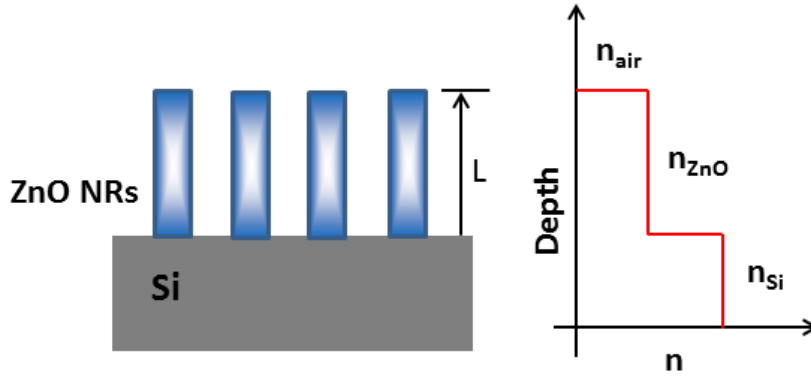
Figure 2.1 Effective refractive-index profile of the interface between air and Si with ZnO nanorods as ARCs on Si surface.

2.1.3 ZnO Nanowire/Nanorod Synthesis Methods

There are various methods to synthesize ZnO nanowires/ nanorods and they usually divide into two groups according to the synthesis temperature. High temperature (up to 1000 °C) or gas condensation methods such as chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD) and pulsed laser deposition (PLD) are using catalytic reactions [58–60], includes intricate vacuum deposition systems, limiting nanowire/nanorod synthesis to only small-scale substrates. On the other hand, hydrothermal growth and electrodeposition methods are classified as low temperature (below 100 °C) methods and are not typically limited with the substrate size.

2.1.4 Hydrothermal Method

Among these conventional methods, hydrothermal method is a low temperature, vacuum-free and thus a low cost method. It is applicable to large and various substrates, such as polymers and textiles, which cannot tolerate high temperatures. Hydrothermal method for the growth of ZnO nanorods was developed by Vayssieres et al. [61] and improved by Greene et al. [62–64]. Unalan et al. [57] later

demonstrated the rapid synthesis of ZnO nanorods by slightly modifying the hydrothermal method using a commercially available microwave oven for heating the growth solution. This shortened the growth time of nanorods from hours to a few minutes. Moreover, high quality nanowires with high yield were obtained using environmentally friendly chemicals via this method.

In this chapter, the effect of using microwave grown vertically aligned ZnO nanorods as ARCs on both planar and textured industrial scale (156 mm × 156 mm) single-crystalline wafer scale Si solar cells is presented. Industrially applicable nanorod growth process was carried out within a few minutes through a commercial microwave oven. The detailed investigations concerning the influence of the length of ZnO nanorods on the optical and antireflective properties as well as their passivation properties have been discussed in detail.

2.2 Experimental Details

2.2.1 Si Solar Cell Fabrication

In this work, to texturize Si surface, p-type, single-crystalline Si (100) wafers (resistivity 1–3 Ω.cm), with dimensions of 156 mm × 156 mm × 180 μm for length, width and thickness were used, respectively. All chemicals were purchased from Sigma-Aldrich (Steinheim, Germany) and used without further purification. For the first process, the wafers were dipped into 1:20 HF: DI solution to remove the natural oxide on the surface. After natural oxide removal, the wafers were ready for saw damage removal process using a 20% sodium hydroxide (NaOH) solution. This was done at 80°C for 2 min. To create pyramidal structure and texturing, wafers were etched in a temperature controlled KOH- acidic texturing tank, containing KOH, DI water and isopropyl alcohol (IPA) with concentrations of 2:88:10 KOH:DI:IPA. The solution was prepared inside the tank and the heater was set to the desired temperature (80°C for 35 minutes). During the heating of the solution, the magnetic stirrer and N_2 bubbler was used to help KOH dissolve into the solution.

Hydrofluoric acid (HF) cleaning, deionized (DI) water (resistivity 18.3 MΩ) rinsing, and nitrogen gas drying carried out subsequently. The surface of the texturized Si was examined using scanning electron microscope (SEM). The SEM images of saw etched and textured Si are provided in Figure 2.2 (a) and (b), respectively.
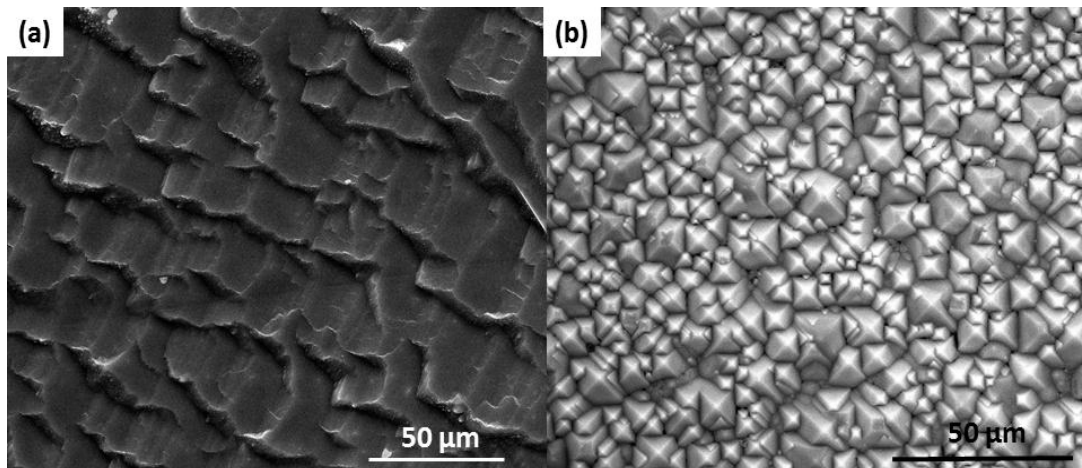
Figure 2.2 SEM images of (a) saw damage etched and (b) textured Si.

Before doping of the p-type wafers, a cleaning process should be carried out to remove organic-inorganic contaminants and the natural oxide that may have grown on the wafer surface. First of all, native oxide on the wafers, were removed using 1:4 HF: DI solution. This also makes the surface of the wafers hydrophobic. RCA-1 process is followed by oxide removal by dipping wafers into in to a solution of H_2O_2: NH_4OH: DI with a concentration of 1.5:1:6 at 70°C for seven minutes. In this step, organic contaminants were removed from the wafer surface. To remove metal contaminations RCA-2 process was applied to wafers using H_2O_2: HCl: DI solution with 1.5:1:6 concentrations at 70°C for 7 minutes and followed by rinsing.

In the last step of, natural oxide removal carried out again using dilute solution of HF. The wafers rinsed and dried in a centrifugal drier and became ready for solid state diffusion.

To n-type dope the wafers, $POCl_3$ as a source of P was used in the diffusion furnace. Cleaned wafers were placed in a quartz boat inserted into the heated furnace with a

slow pace under N_2 flow to prevent thermal stress due to sudden temperature changes. After thermal equilibrium under O_2+N_2 environment, predeposition step was started with the flow of $POCl_3+O_2+N_2$. After 40 minutes, wafers were pulled out of the furnace slowly and left for cooling outside the furnace. Phosphosilicate glass (PSG) grown on the surface of the wafer was removed by dipping the cells into 1:4 HF: DI solution for 30 seconds. The wafers were then rinsed with water and dried with a drier. Following doping, the sheet resistance of the wafers was measured as $50\Omega/\square$ with a four point probe measurement tool.

The back Al and front Ag contacts [Ferro Electronic Materials (Mayfield Heights, OH) NS3116 Silver Conductor and AL5130 Aluminum Conductor] were then deposited through screen printing (thickness ~30 μm), which was followed by a co-firing process conducted at 875°C. Screen printer system used in this study was an ASYS X1 SL model printer with a manual load and unload. It was adjustable for different size of wafers and printing parameters. The process could be fully controlled by a computer. The belt furnace used for this work had 7 heating zones. Belt speed and each zone temperature can be adjusted by a computer. Photograph of printer and firing furnace are shown in Figure 2.3 (a) and (b), respectively.
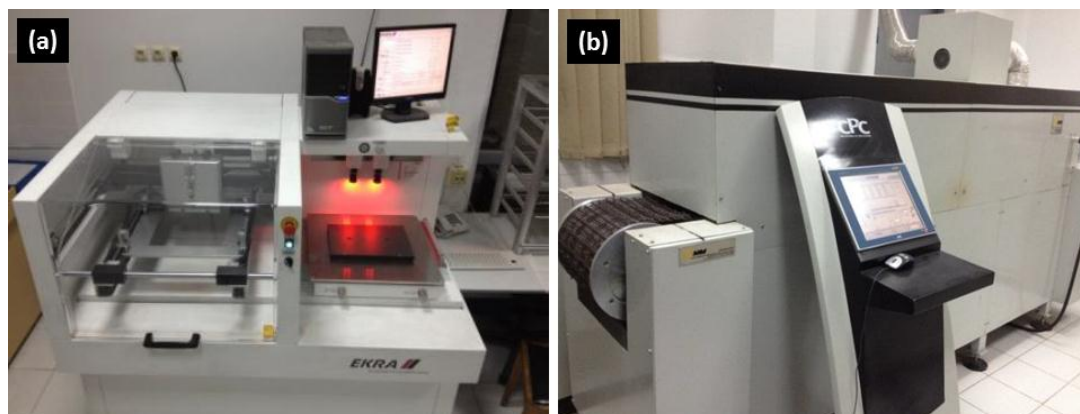
Figure 2.3 Photographs of (a) screen printing system and (b) firing furnace of GUNAM Laboratories.

2.2.2 Synthesis of ZnO Nanorods Antireflective Coatings

ZnO nanorods were synthesized following the metallization process via hydrothermal method using microwave heating. A 10 mM solution of zinc acetate dehydrate [$Zn(O_2CCH_3)_2(H_2O)_2$, 99%] in 1-propanol was prepared as the seed solution. A few hours bath sonication was needed to obtain a uniform solution. It was then spin coated onto (n-type) single- crystalline Si substrates (for life time measurements) and solar cells at 2000 rpm for 60 seconds. The substrates were then heated at 120°C for a minute following each spin coating step to enhance drying and adhesion. A uniform seed layer was obtained after three times of spin coating. A few nanometer (5-10 nm) ZnO film sputtered on Si substrates can also be used as seed to grow ZnO nanowires.

For the growth of ZnO nanorods, preseeded substrates were dipped into an aqueous growth solution of equimolar, 20 mM, zinc acetate dihydrate [$Zn(O_2CCH_3)_2(H_2O)_2$, 99%] and hexamethylenetetramine (HMTA, $(CH_2)_6N_4$, 99%). Heating process was carried out using a commercially available microwave oven (2.45 GHz) using a power setting of 700 W at atmospheric pressure. To investigate the effect of time, which would then determine ZnO nanorods length, nanorods were grown for durations ranging from 1 to 4 minutes. The growth solution renewed in every minute. This is because evaporation could change the molarity of the growth solution. The following reactions took place during the formation of ZnO nanorods:

$$C_6H_{12}N_4 + 6H_2O \rightarrow 6HCHO + 4NH_3 \qquad \text{(Eq. 2.1)}$$

$$NH_3 + H_2O \rightarrow NH_4^+ + OH^- \qquad \text{(Eq. 2.2)}$$

$$Zn + 2NH_4^+ \rightarrow Zn_2^+ + 2NH_3 + H_2 \qquad \text{(Eq. 2.3)}$$

$$Zn_2^+ + 2\,OH^- \rightarrow Zn(OH)_2 \rightarrow ZnO(S) + H_2O \qquad \text{(Eq. 2.4)}$$
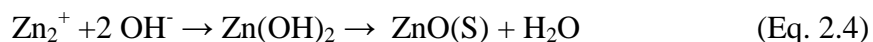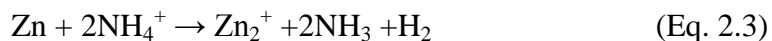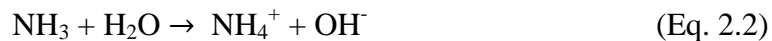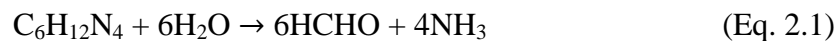
The reaction of HMTA with water resulted in the formation of ammonia, which dissociates into ammonium and hydroxide ions. These ions further react with zinc ions to from ZnO nanorods. After desired growth durations the substrates were

removed from the growth solution, rinsed with DI water and dried under nitrogen flow.

The surface morphology and size distribution of vertically aligned ZnO nanorods were characterized by SEM [FESEM (FEI, Eindhoven, Netherlands), Nova SEM 430]. Top view and cross section view of ZnO nanorods grown on polished Si wafers have been shown in Figure 2.4.
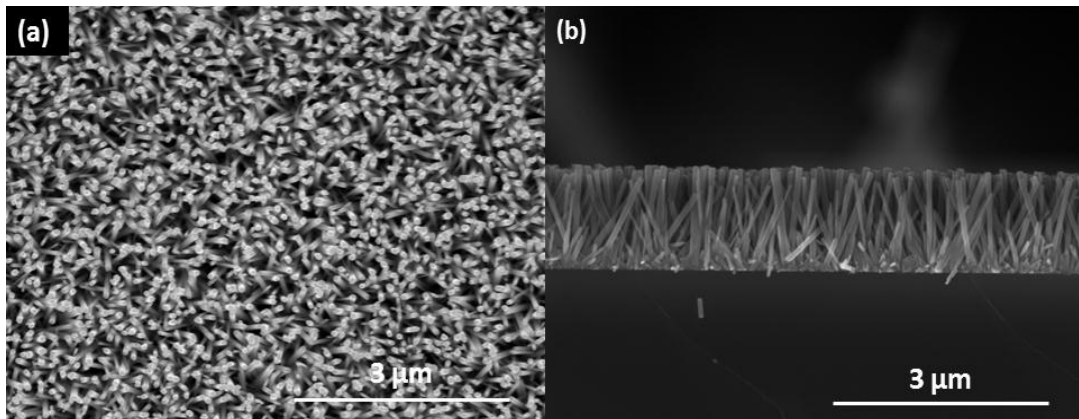
Figure 2.4 (a) Top-view and (b) cross-sectional SEM images of ZnO nanorods grown on polished Si substrate.

Figure 2.5 shows photographs of textured solar Si wafers with and without ZnO nanorods. The difference in wafer colors is obvious due to light trapping effect of the nanorods. Wafer with the nanorods was also quite uniform in color.
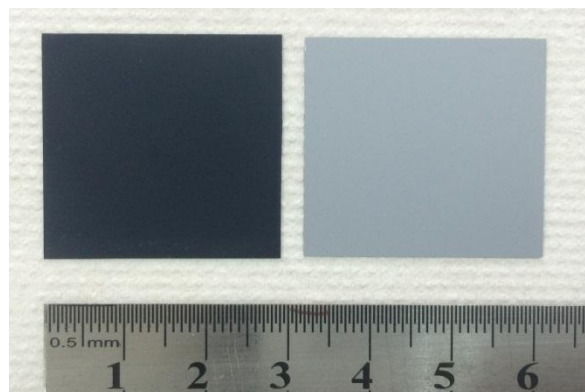
Figure 2.5 Photographs of textured solar wafers with (left) and without (right) ZnO nanorods.

Figure 2.6 shows the schematic of the fabricated Si solar cells with ZnO nanorods grown on top of textured pyramids as ARCs.
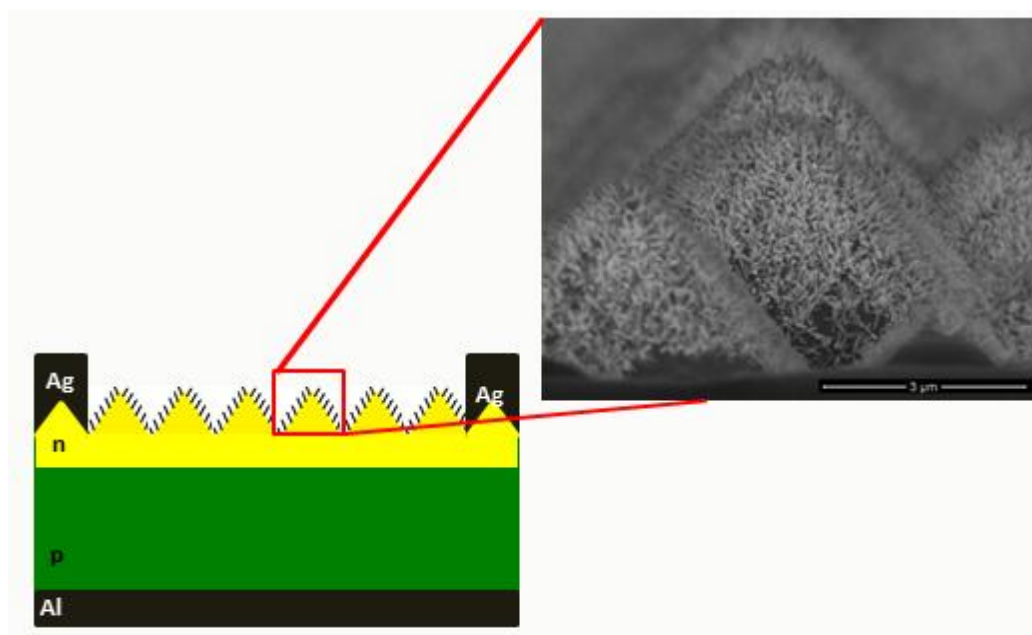
Figure 2.6 Schematic of the fabricated single-crystalline Si solar cell with an SEM image of ZnO nanorods ARCs on pyramids.

2.3 Results and Discussion

2.3.1 Morphology and Size of ZnO Nanorods

SEM images of ZnO nanorods with different lengths, grown on textured devices are shown in Figures 2.7 (a)–(h) shows. Homogeneous and uniform coverage of the nanorods were obtained. Pyramidal structures behind the ZnO nanorods are also apparent in the images. Average diameter, lengths, and density of the ZnO nanorods were measured using SEM images and are provided as a function of growth time in Figure 2.8.
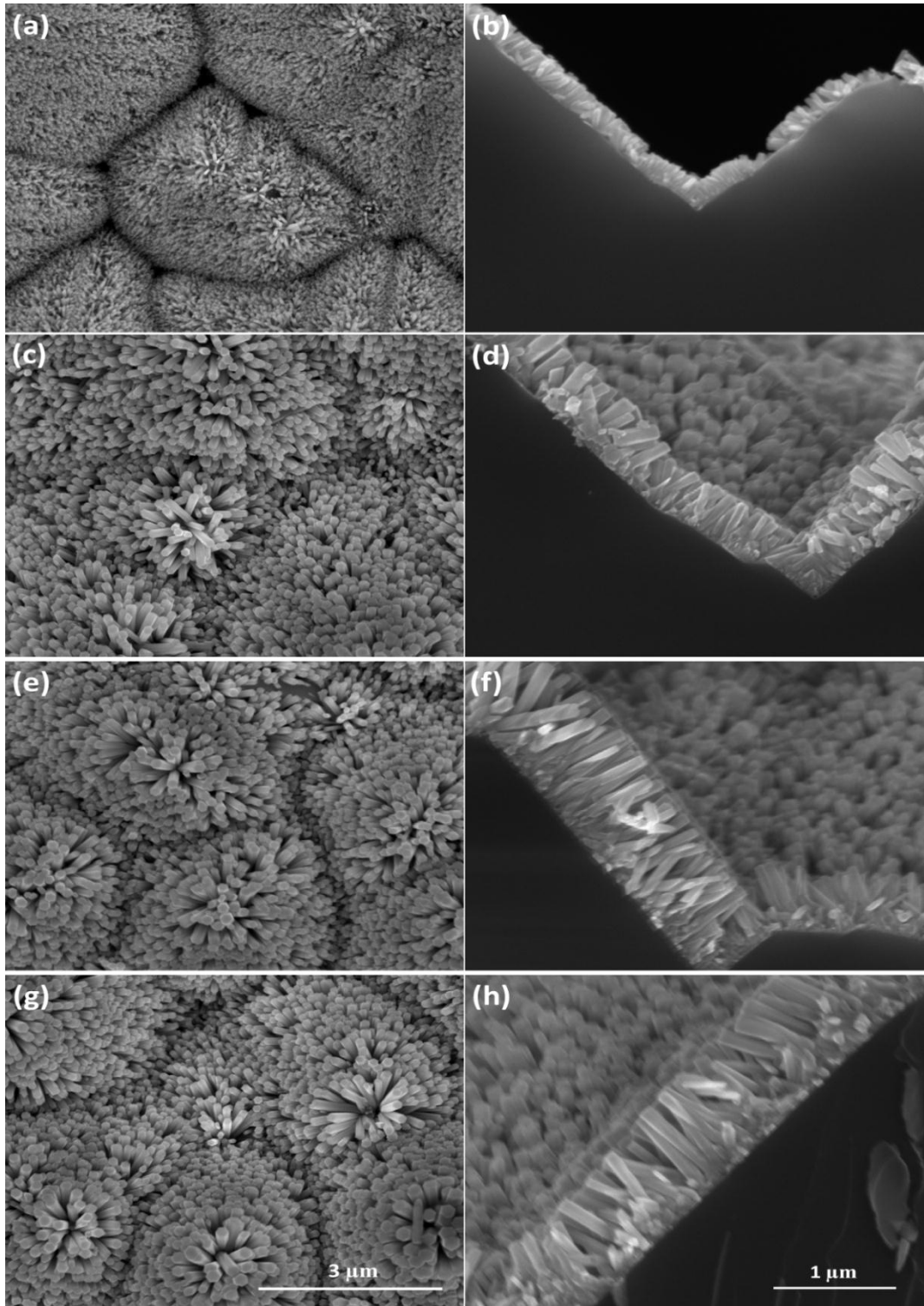
Figure 2.7 Top (a), (c), (e), and (g) and cross-sectional (b), (d), (f), and (h) SEM images of the ZnO nanorods grown on textured Si substrates for 1,2,3, and 4 minutes, respectively.
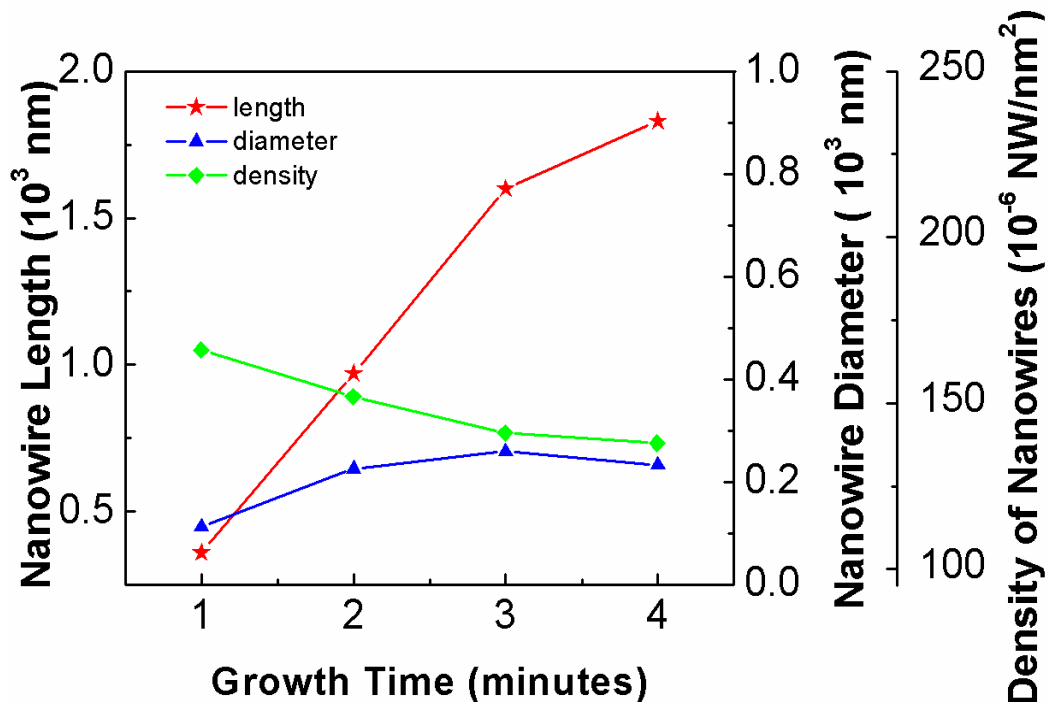
Figure 2.8 Plots of average length, diameter and density of ZnO nanorods as a function of growth time.

From the cross-sectional SEM images, length and diameter of more than 100 individual nanorods were measured using image analysis software, Image J. Similarly, the densities of the nanorods were measured from the top view images. Nanorod densities could be little underestimated due to the overlapping. The nanorods grown for a minute had a diameter and length of 110 and 360 nm, respectively. A nanorod density of 166×10^{-6} NW/nm^2 was obtained for those samples. With prolonging the growth time, the length of the nanorods increased steadily during the reaction period, whereas their diameters slightly increased. This resulted in a small decrease in the nanorod density.

2.3.2 Optical Measurements

Reflection measurements were made through a Si photodetector calibrated integrated sphere [Newport (Irvine, CA) 70679NS], which also takes into account the diffuse reflectance. Reflectance spectra in the wavelength range of 400–1100 nm, for the textured and planar Si substrates with different ZnO nanorod growth times, are given

in Figures 2.9 (a) and (b), respectively. For comparison, reflectance spectra of bare substrates without the nanorods have also been provided.
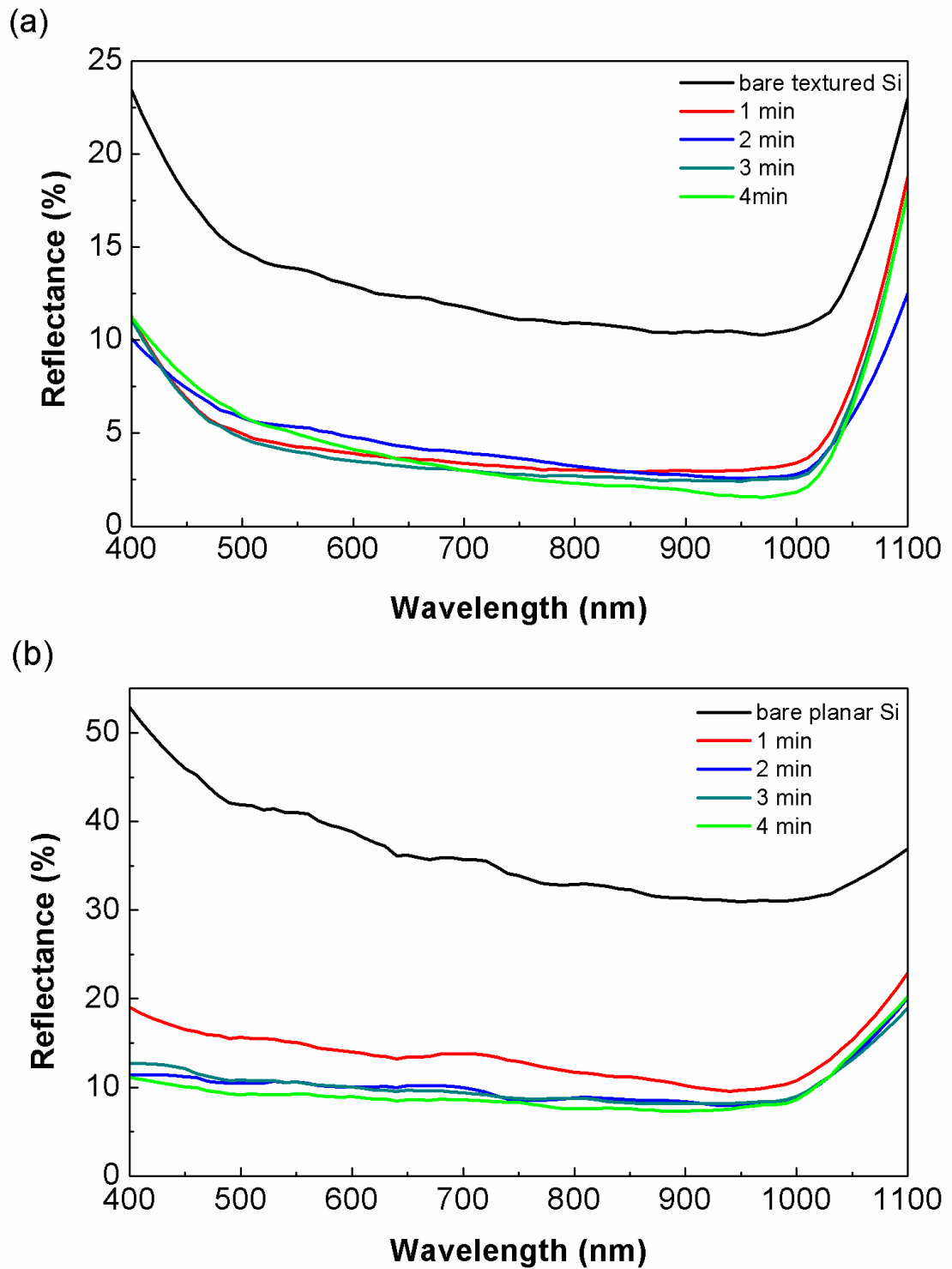
Figure 2.9 Reflectance spectra of ZnO nanorods with different growth time on (a) planar and (b) textured Si substrates.
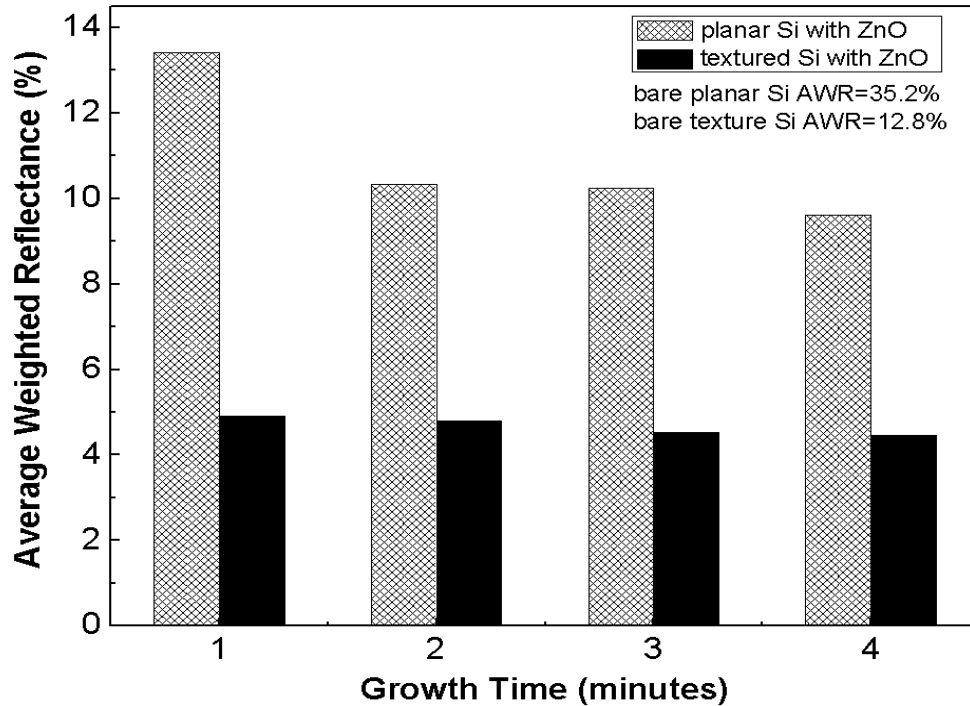
Figure 2.10 AWR values of ZnO nanorods with different growth times.

For clarification, the average weighted reflectance (AWR) values of the nanorods were calculated and is shown in Figure 2.18. In this work, we have investigated the effect of nanorod length (from about 300 nm to 1.7 μm) on the antireflection performance of the solar cells. We have not used any agents to control the diameter of the nanorods.

Seed solution spin coating repetitions determined the nanorod density; however, we preferred to fix it as well. Length of the nanorods was found to have almost no effect on the reflectivity of the Si surface (for both planar and textured) within the investigated range. We refrained ourselves to grow even longer nanorods (simply by increasing the growth duration), as we know from experience that excessive scattering takes place between longer nanorods and the nanorod array losses its transparency. This could have limited the amount of light that was absorbed by the solar cells. In addition, this would make it difficult to make physical contacts to electrodes.

For both planar and textured Si substrates, reflectivity of the samples was found to decrease within the investigated wavelength range upon the growth of ZnO nanorods.

Reflectivity of the planar Si substrates was found to decrease from 35.2% for bare substrates to 9.6% for the ones with ZnO nanorods grown for 4 minutes. Similarly, reflectivity of the textured Si substrates was found to decrease from 12.8% for bare substrates to 4.5% for the ones with ZnO nanorods grown for 4 minutes. It was also found that the absolute reflectance values of the samples were not considerably changed with the growth time, in other words with the nanorod length. A relative improvement of almost 73% in the reflectivity of the surface was obtained for the planar Si substrates revealing the higher effectiveness of ZnO nanorods as ARCs on planar Si substrates compared with the textured counterparts.

2.3.3 Life Time Measurements

Carriers that are photogenerated in crystalline Si, recombine in the bulk and at its surfaces. The time these carriers spend in the crystalline Si, before recombination is referred to as effective lifetime (τ_{eff}) and is given by the expression taking into account overall lifetime in the crystalline Si bulk (τ_{bulk}) and at its surface (τ_{surf}):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{surf}} + \frac{1}{\tau_{bulk}}$$ (Eq. 2.5)

In this work, Czochralski (n-type) grown single-crystalline Si substrates with ZnO nanorods on both sides were used as symmetrical samples for the measurements. Bare Si substrates were also measured for comparison. As ZnO nanorod grown substrates did not experience any high temperature during nanorod growth and as both substrates (bare Si and ZnO nanorod grown) would be subjected to the same cofiring process (conducted at 875°C) following the screen printing of the metal contacts, we assume the same τ_{bulk} for both the samples. The growth of nanorods can be assumed to change only τ_{surf}, which can then be directly correlated with τ_{eff}.

The experimentally accessible property is the (excess) conductivity induced in crystalline Si by the excess photogenerated carriers. This excess conductance can be measured in a contactless fashion by different techniques. Quasi-steady-state photoconductance is one of these techniques; in which during a long and

exponentially decaying light pulse (~2 ms), the conductivity of the wafer is measured simultaneously with the illumination level using a calibrated photodetector. To ensure a homogeneous carrier generation throughout the whole crystalline Si bulk, a filter mounted on the flash lamp provides infrared illumination. Surface passivation property of ZnO nanorods was investigated by measuring the minority carrier lifetime of the samples using a Si wafer lifetime tester (Sinton instruments, Boulder, CO) prior to metallization. With the growth of ZnO nanorods, τ_{eff} increased from 9 to 71 µs at a carrier injection level of 10^{15} cm^{-3}. This clearly indicates the surface passivation property of ZnO nanorods in addition to their ARC property. The surface passivation can result either from the field effect of the band alignment at the ZnO/n-Si interface or the chemical improvement of the interface. The former case can be understood by the energy band diagram [65] provided in Figure 2.11. Given the wide band gap energy and electron affinity values, ZnO forms an asymmetrical band alignment with the Si substrate resulting in an unfavorable condition for the carrier recombination at the ZnO/Si interface.
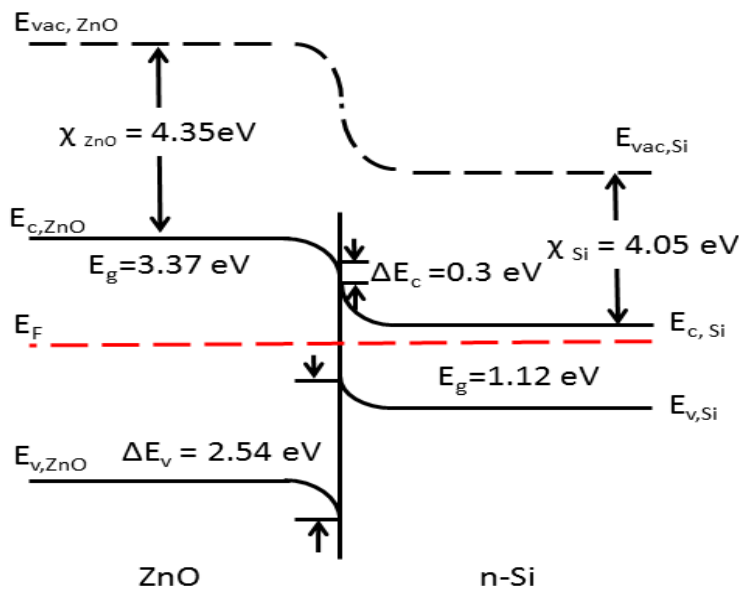
Figure 2.11 Energy band diagram at the interface between ZnO nanorods and the n-type Si.

This potential structure formed by the band offsets at the valance band reflects the holes back into the substrate, whereas the electrons in the conduction band might even pass to ZnO side and then transferred to the metal contacts. The position of the

Fermi level and the conductivity of ZnO are determined by the level of doping, which is not specifically investigated in this work. For any doping level, this asymmetrical band alignment at the interface favors the carrier separation and thus reduces the probability of carrier recombination at the ZnO/Si interface. It should be mentioned at this point that the main current flow takes place between Si surface and the metal fingers, which are formed prior to ZnO nanorod growth. In the latter case, the chemical effect of ZnO can be significant for the surface passivation. Like the SiO_2/Si interface, which is known to be well behaved in terms of the carrier recombination, oxygen atoms originating from the ZnO layer might saturate the dangling bonds at the Si side, leading to a less active interface for recombination. However, this point needs to be further clarified experimentally by a study focused on the chemical structure at the interface.

2.3.4 Solar Cell Characteristics

A Keithley (Cleveland, OH) 2440 sourcemeter was used to obtain current–voltage characteristics of the fabricated solar cells with and without ZnO nanorods coating. A solar simulator [Quicksun (Espoo, Finland), AM 1.5G, 1000 W/m^2] was used for illumination during the measurements.

The current density-voltage (J–V) characteristics of the fabricated solar cells are provided in Figure 2.12 and the photovoltaic parameters are summarized in Table 2.1. Inset in Figure 2.12 shows the photographs of the fabricated and measured planar solar cells. Dark surface of the solar cell (left) clearly reveals the ARC effect of the ZnO nanorods. Laser scribing and cutting has been performed on each side of the measured solar cells, as shown in the photographs, to eliminate the effects of backside diffusion of phosphorus. Improvement in all the photovoltaic characteristics, especially the short-circuit current (J_{sc}) density in agreement with the reflectance measurements, was obtained for the devices with ZnO nanorods as ARCs. The open circuit voltage (V_{oc}) was considerably increased due to the passivation effect of ZnO nanorods. Passivation suppresses the recombination current and thus improves the V_{oc} of the cell.
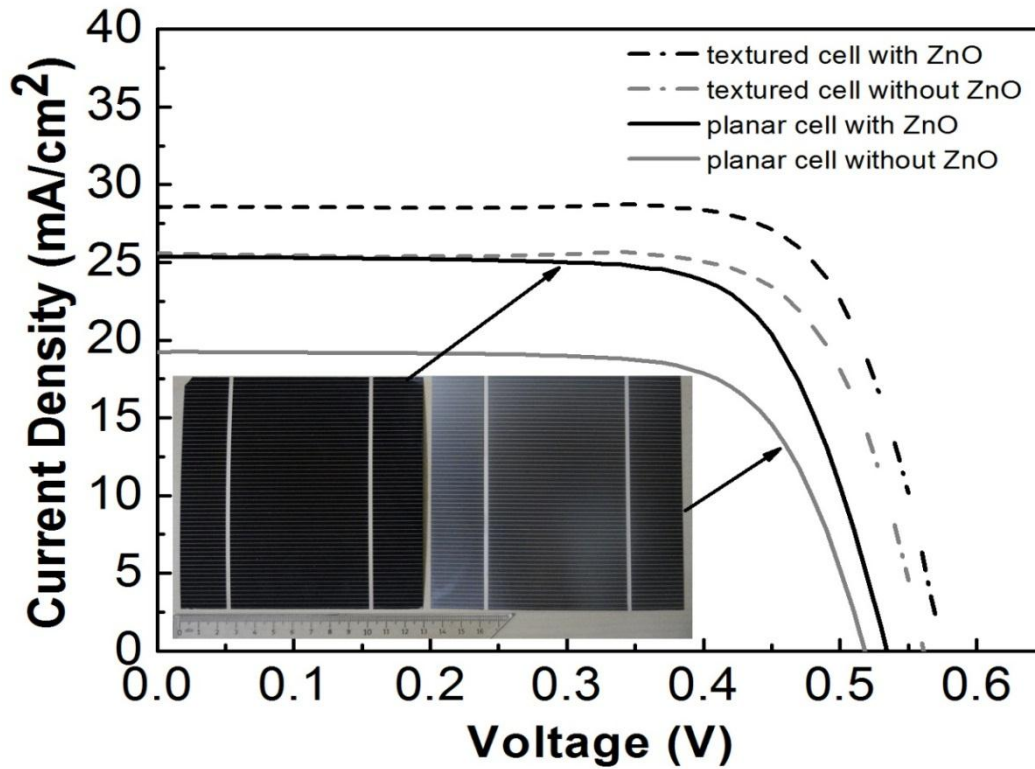
Figure 2.12 J–V curves of planar and textured solar cells with and without ZnO nanorods. Inset shows the photographs of planar solar cells with (left) and without (right) ZnO nanorods.

Table 2.1 Photovoltaic parameters of the planar and textured solar cells with and without nanorods.

Sample	Jsc (mA/cm^2)	Voc (V)	FF (%)	η (%)
Bare planar cell	19.2	0.52	70.5	7.5
Planar cell with ZnO	25.3	0.54	72	10
Bare textured cell	25.6	0.56	74	10.98
Textured cell with ZnO	28.6	0.58	74	12.74

For planar and textured single-crystalline Si solar cells, photovoltaic conversion efficiencies of 7.5% and 11% have been obtained without ZnO ARCs, respectively. A 33% enhancement in the conversion efficiency was obtained for planar single-

crystalline Si solar cells, while this value was 16% for the textured counterparts through the growth of ZnO nanorods. Obtained efficiency values for planar and textured single crystalline solar cells are low when compared with the literature.

However, we have to clarify that our intention here is not to make state-of-the-art single-crystalline Si solar cells, but instead is to demonstrate the effective use of hydrothermally grown ZnO nanorods as ARCs. ZnO nanorods as ARC on planar substrates were found to be more effective compared with the textured counterparts. This is in accordance with the change in AWR values of planar and textured Si solar cells, as shown in Fig. 2.10. Our intention to use planar Si solar cells in this work was to investigate if they could overperform the textured Si solar cells following the nanorod growth through the nanoscale morphology of the nanorods. Although the relative improvement in planar solar cells in terms of reflectance and photon conversion efficiency is higher compared with textured counterparts through the growth of ZnO nanorods, textured solar cells with and without ZnO nanorods revealed the highest photon conversion efficiencies. Our method is simple, cost effective and rapid, which can be easily adapted to the production line of the industrial scale solar cells to replace vacuum deposited and costly SiN_x thin films.

2.4 Conclusions

In summary, we have demonstrated the use of ZnO nanorods as ARC on planar and textured, industrial scale Si solar cells. The ZnO nanorods provided effective AR with a weighted reflectance of 9.6% for planar and 4.5% for textured Si surfaces over the 400–1100 nm spectral range. For planar and textured single-crystalline Si solar cells, photovoltaic efficiencies of 7.5% and 11% have been obtained without ARCs, while these values were improved to 10% and 12.7% through the growth of ZnO nanorods, respectively. An almost one order of magnitude improvement in the minority carrier lifetime indicated the passivation effect of ZnO nanorods. Our results clearly reveal the potential of ZnO nanorods to be used as ARC in solar cells instead of vacuum deposited SiN_x upon further optimization. It is also clear that the utilization of ZnO nanorods as ARCs can be extended to thin film or excitonic solar cell concepts.

CHAPTER 3

SILVER NANOWIRE NETWORK AS TRANSPARENT TOP ELECTRODE FOR SINGLE CRYSTALLINE SI SOLAR CELLS

3.1 Introduction

Crystalline Si solar cells have dominated photovoltaic market primarily due to their advantages, such as relatively high efficiency and abundant material supply. In addition to Si wafer cost, cell manufacturing processes such as solid state diffusion (900 °C), contact co-firing (900 °C) and high-vacuum chemical deposition (400 °C) of ARCs are energy intensive and expensive. In recent years, much effort has been spent to decrease Si solar cells manufacturing costs.

Screen printing and evaporation are the two main routes for the deposition of top contacts. Thermally evaporated metal electrodes require high vacuum environments and lithographical process are inevitable when there is an ARC on top, which gives rise to the expense of the process [66]. On the other hand, as previously discussed in Chapter 1, metallization via screen printing method suffers from low aspect ratio and shading losses, which affects cells efficiency [67]. It is also an energy consuming process.

One approach to reduce shading effects of top contact and increase the efficiency of the cells is to fabricate interdigitated back contact (IBC) solar cells. In IBC solar cells all or parts of the front contact grids have been removed to the rear side of the device. Another advantage of the IBC cells is the easy interconnection of the cells within the module because the cells can be placed very close to each other. But, on the other hand, in IBC cells high quality thin Si wafers should be used as active layer to collect carries generated near the top surface and to decrease series the resistance [68]. A schematic of the IBC solar cell is provided in Figure 3.1.
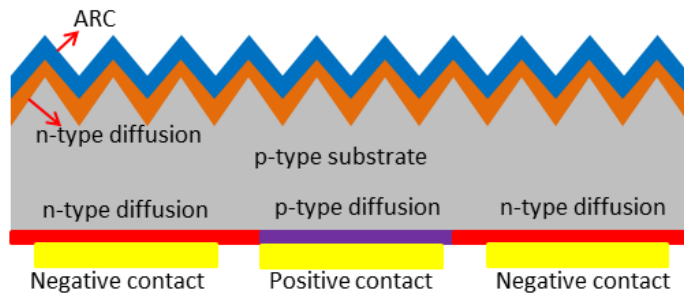
Figure 3.1 Schematic of the IBC solar cell.

Another approach to eliminate shading effect of the top contact is to replace top grid contact with transparent nanostructured electrodes. The goal of this chapter is to show the potential of silver nanowire (Ag NW) networks as transparent top electrodes for the elimination of complicated and costly metallization process in Si solar cells.

3.1.1 Transparent Conducting Films (TCFs)

Transparent conducting films (TCFs) are optically transparent and electrically conductive thin layers. They usually act as a transparent window to let the light pass through and reach the active layer of the device to generate electron-hole pairs. Simultaneously, they act as ohmic contacts to collect carries generated within the device. In addition to photovoltaics, TCFs play an important role in many other electronic devices, such as liquid-crystal displays, OLEDs and touchscreens [69].

Both organic and inorganic materials are used as TCFs in photovoltaic applications. Transparent conducting oxides (TCO) [70], such as indium tin oxide (ITO), fluorine doped tin oxide (FTO) and doped zinc oxide (ZnO) are examples of inorganic TCFs. While organic films are polymeric materials like poly(3,4-ethylenedioxythiophene) and its derivatives [69]. The most commonly used and industrialized TCO is ITO due to its good electrical and optical properties. However, ITO is brittle limiting its application in flexible devices. It also shows degradation with time when it is subjected to mechanical stresses. Also increase in cost is forcing

researchers to look for other alternatives. Recently, new generation TCFs based on nanostructures have been proposed to improve energy conversion efficiencies in photovoltaic devices. These nanostructures include carbon nanotube (CNT) films and graphene sheets. CNT films display high transparency and flexibility; but, they have mediocre conductivity due to inter nanotube junction resistances [71-73]. Graphene sheets have low cost but high sheet resistance and complicated synthesis processes [74]. Recently, highly conductive metal nanowire networks made up of gold, silver and copper nanowire networks were proposed as top metal contacts in photovoltaic devices [75-78].

3.1.2 Optical and Electrical Properties of Silver Nanowire Networks

In addition to flexibility and low fabrication cost, Ag nanowire networks have comparable transparency and sheet resistance with ITO films, which make them impressive alternatives [75-78]. These properties are the key factors in designing the top contact.

Recently, Coskun et al. have carried out detailed parametric studies on the synthesis of Ag NWs via cost effective polyol method and utilization of these NWs for fabrication of TCFs. Spray coating method was used to fabricate Ag NW networks with controlled density to obtain desired sheet resistance and transparency values. [79]. Figure 3.2 shows SEM images of Ag NW networks spray coated with different densities. The transmission spectra of Ag NW networks with different nanowire densities in comparison to commercial ITO (Delta Tech) are provided in Figure 3.3. It is obvious that increasing the density of NWs decreases transparency. However, increasing NW density decreases the sheet resistance of the networks.
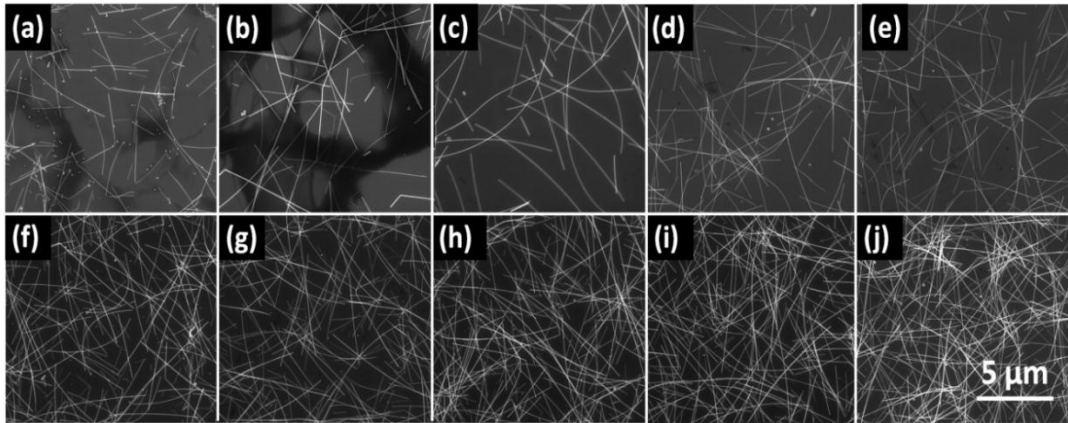
Figure 3.2 SEM images of Ag NW networks with different densities of, (a) 0.28, (b) 0.34, (c) 0.44, (d) 0.50, (e) 0.59, (f) 0.70, (g) 0.82, (h) 0.98, (i) 1.35 and (j) 1.62 NW/μm^2 [79].
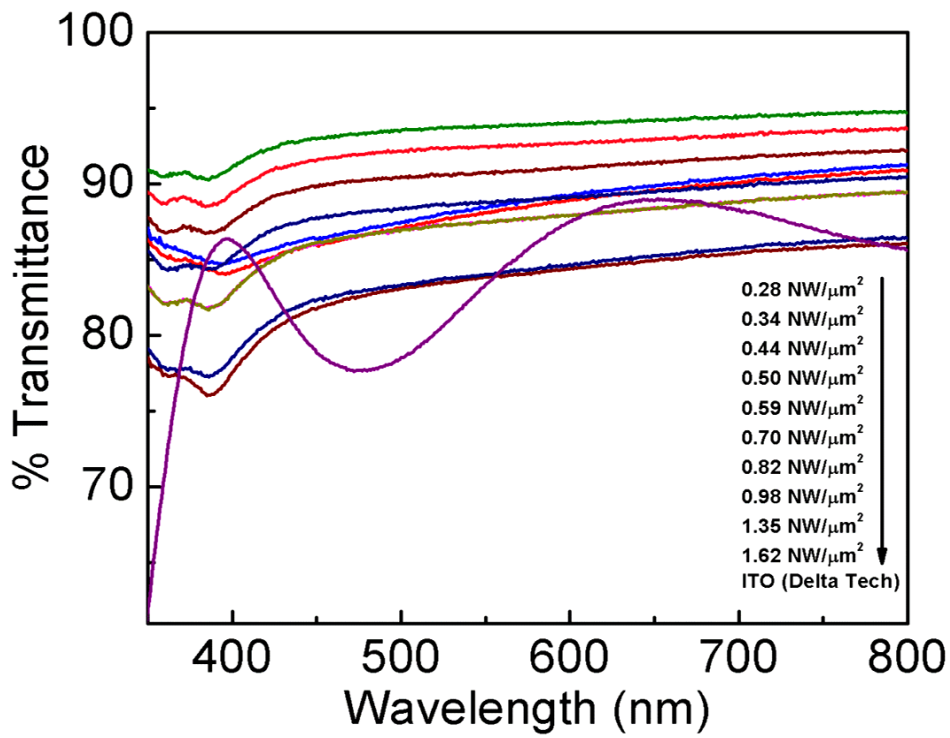
Figure 3.3 Transmission spectra of Ag NW networks with different densities [79].

During polyol synthesis polyvinylpyrrolidone (PVP) surrounds Ag NWs dictating one dimensional growth. Although intensive purification processes such as washing in acetone and ethanol is applied, a thin PVP layer still remains on the NWs. This residual PVP layer promotes dispersion of the Ag NWs in solvents like ethanol, iso propanol etc. At the same time, this residual PVP layer acts as a barrier between the NWs during charge transport in the network form.

Figure 3.4 shows sheet resistance versus transparency for Ag NW networks before and after annealing process to remove the PVP layer to make good contact between nanowires. A transparency of 88% was obtained for the film with a sheet resistance of 11 $\Omega/\square$ [79].
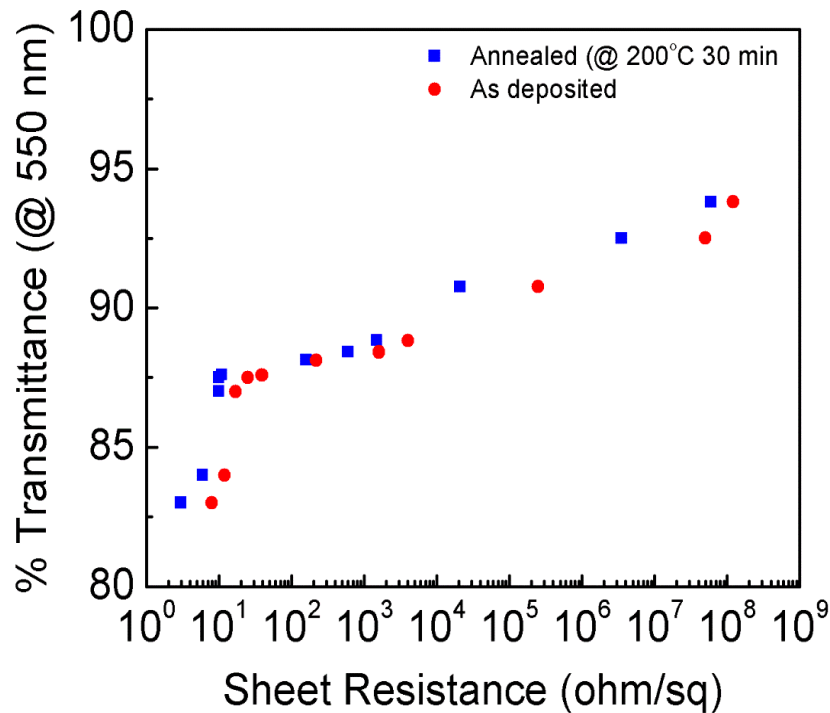
Figure 3.4 Sheet resistance with respect to transparency of Ag NW networks both before and after annealing at 200°C for 30 min [79].

Theoretically, Ag NWs could not provide the same resistivity reduction in crystal Si cells as in low mobility cells such as organic, amorphous Si and hybrid cells [80-82]. But there is still enough motivation to utilize them as top electrodes in crystalline Si

solar cells. Moreover, another advantage that can be achieved using Ag NW electrodes in Si photovoltaics is the plasmonic effects of the metallic wires [83].

3.1.3 Polyol Process

There are several methods to synthesize Ag NWs [84,85]. Among these methods, polyol process enables the synthesis of high aspect ratio wires with high yield. It provides control over the NW dimensions and is cost effective [86]. In polyol process, an inorganic salt is reduced by a solvent at high temperatures and by adding a stabilizer polymer, agglomeration of the particles is prevented. Xia et al. have developed a modified polyol process to control the shape and size of the Ag nanostructures [87]. In this method, ethylene glycol (EG) was used both as a solvent and reducing agent, poly(vinylpyrrolidone) (PVP) was used as a stabilizing agent and Ag nitrate ($AgNO_3$) was used as a Ag source. It is possible to change Ag NWs size and morphology by altering process parameters or by adding different reagents.

3.2 Experimental Details

3.2.1 Synthesis of Ag NWs

All chemicals were purchased from Sigma-Aldrich and used without further purification. The process was started by solving 7 mg sodium chloride (NaCl, 99.5%) in 10 ml, 0.45 M EG solution of PVP. An oil bath attached hotplate was used to uniformly heat the solution up to 170°C. The solution container equipped with a reflux system to prevent solution from evaporation and keep its concentration constant.

0.12 M $AgNO_3$ (99.5%) solution in 5 ml EG was injected to PVP + NaCl +EG solution using a syringe pump with a feeding rate of 5 ml/h. Moreover, the solution was stirred at a rate of 1000 rpm through a magnetic stirrer during the whole process. Once the injection process was completed, NW solution was kept for another 30 minutes at 170 °C and finally air cooled to room temperature.

By introducing Ag^+ ions into the solution, Ag nanoparticles nucleated with various shapes. With the passivation of some facets of these particles by PVP, some nanoparticles can grow into multi-twin particles. PVP is believed to passivate (100) faces of these multi-twin particles and have (111) planes active for anisotropic growth within [110] direction (Figure 3.5). As the addition of Ag^+ ions continue, multi-twin particles grow into Ag NWs [79].

Figure 3.6 shows a schematic of Ag NWs synthesis process. In order to separate Ag NWs from PVP, EG and other by products, the solution was diluted with acetone and centrifuged several times. The final product was dispersed in ethanol and stored for further processing.
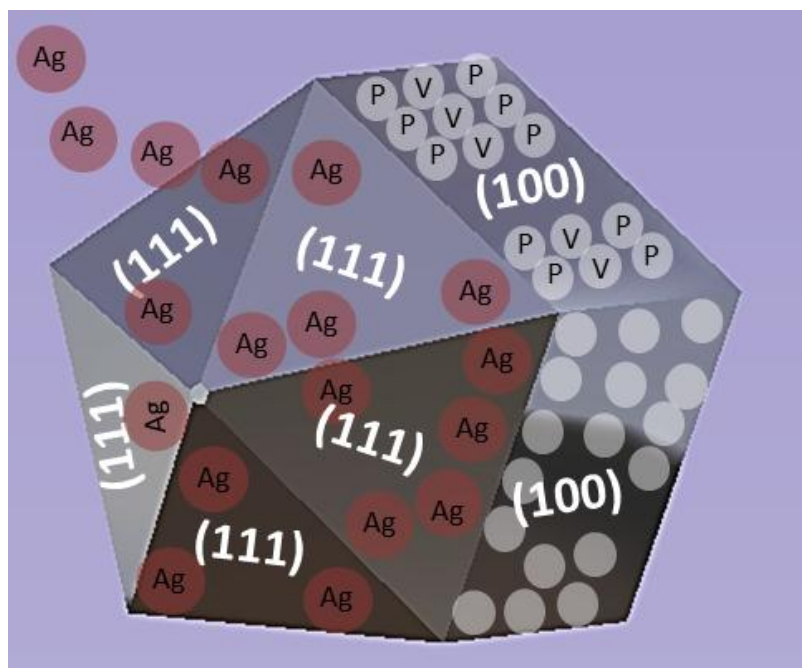
Figure 3.5 Schematic showing the growth of a Ag NW from Ag nanoparticles. PVP molecules passivate (100) faces.
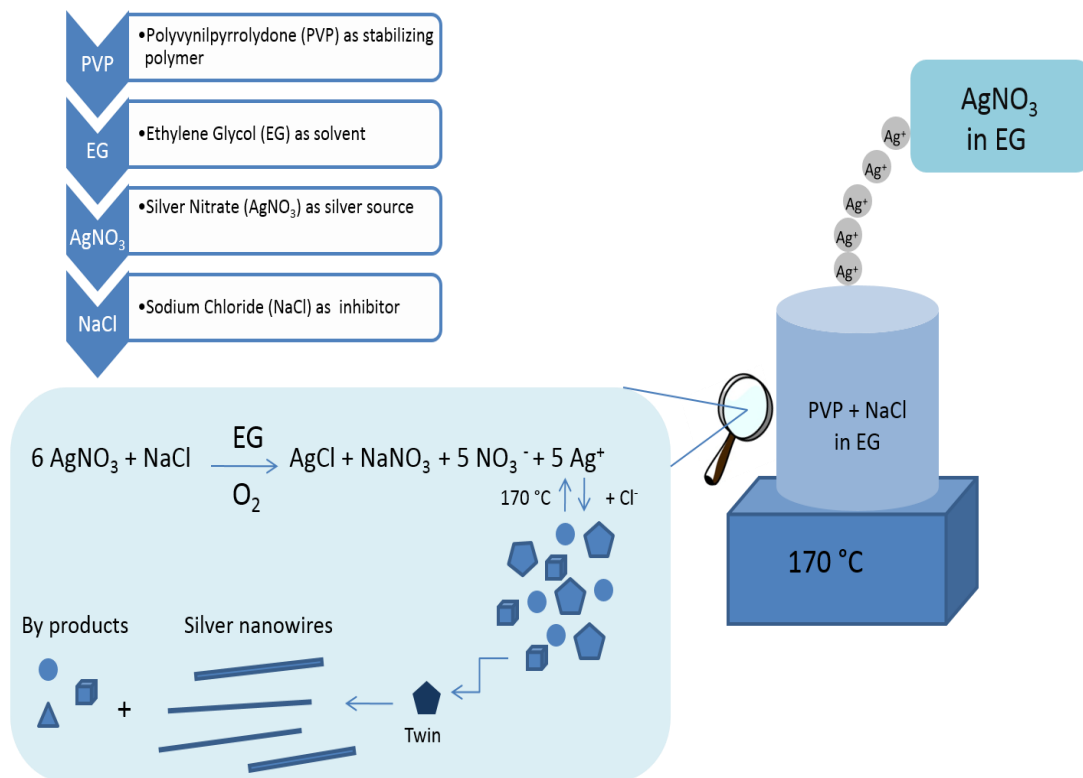
Figure 3.6 Schematic of Ag NWs synthsis via polyol process [79].

An SEM image of Ag NWs following purification is shown in Figure 3.7. The XRD pattern of Ag NWs is shown in Figure 3.8 (a). All diffraction peaks in XRD pattern are related to pure silver (JCPDS Card No. 04-0783). Figure 3.8 (b) shows a high resolution SEM image of Ag NWs, showing pentagonal cross section of a single Ag NWs.
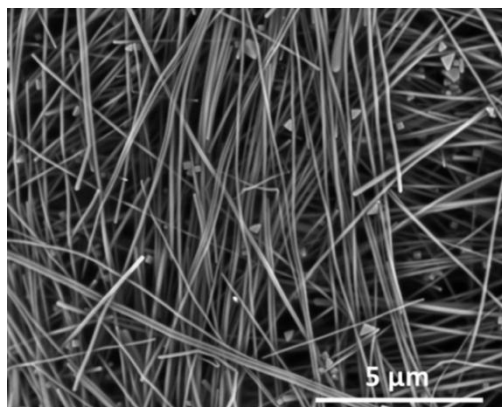
Figure 3.7 An SEM image of purified Ag NWs [79].
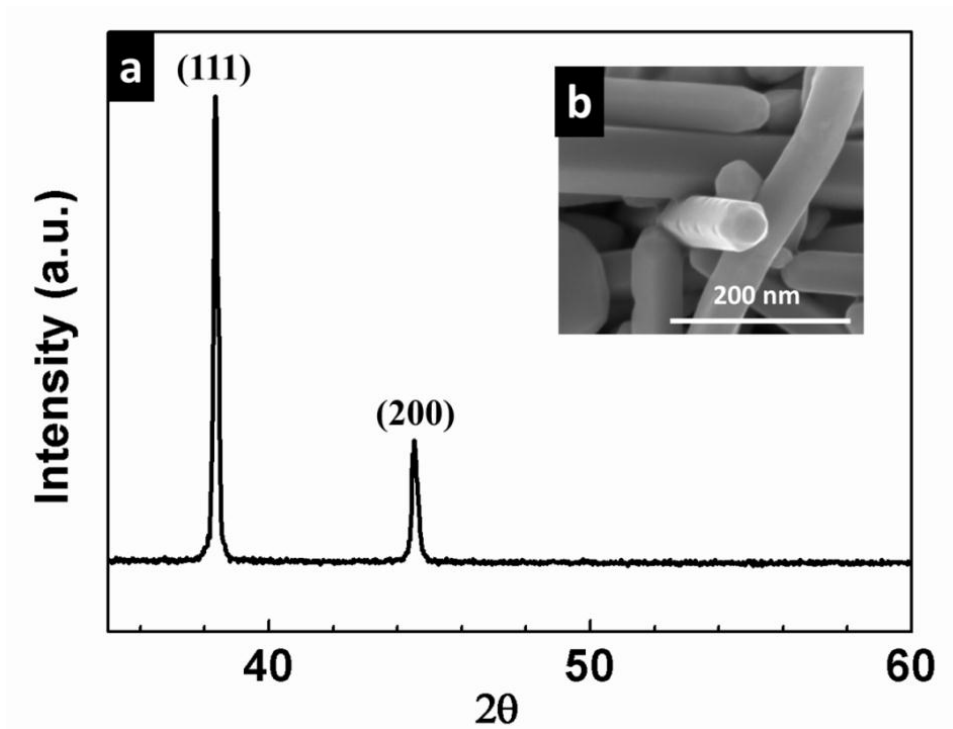
Figure 3.8 (a) XRD spectrum of Ag NWs and **(b)** high resolution SEM image of the NWs [79].

3.2.2 Deposition of Ag NW Network

Figure 3.9 shows the flowchart for the deposition of Ag NWs networks. Prepared ethanolic Ag NW suspension was then used for the deposition of Ag NW networks. Substrates to be coated, mounted were on hotplate using a heat resistant tape following cleaning through consecutive actone and isoppraponol bath sonication. The hot plate was heated to 150°C for the instant evaporation of ethanol. Through the use of an air brush fed by nitrogen gas ethanolic suspension of Ag NWs was coated onto substrates. Pressure of air brush and the distance between air brush and hot plate effect the coating process. So, these parameters were kept constant for reproducibility.
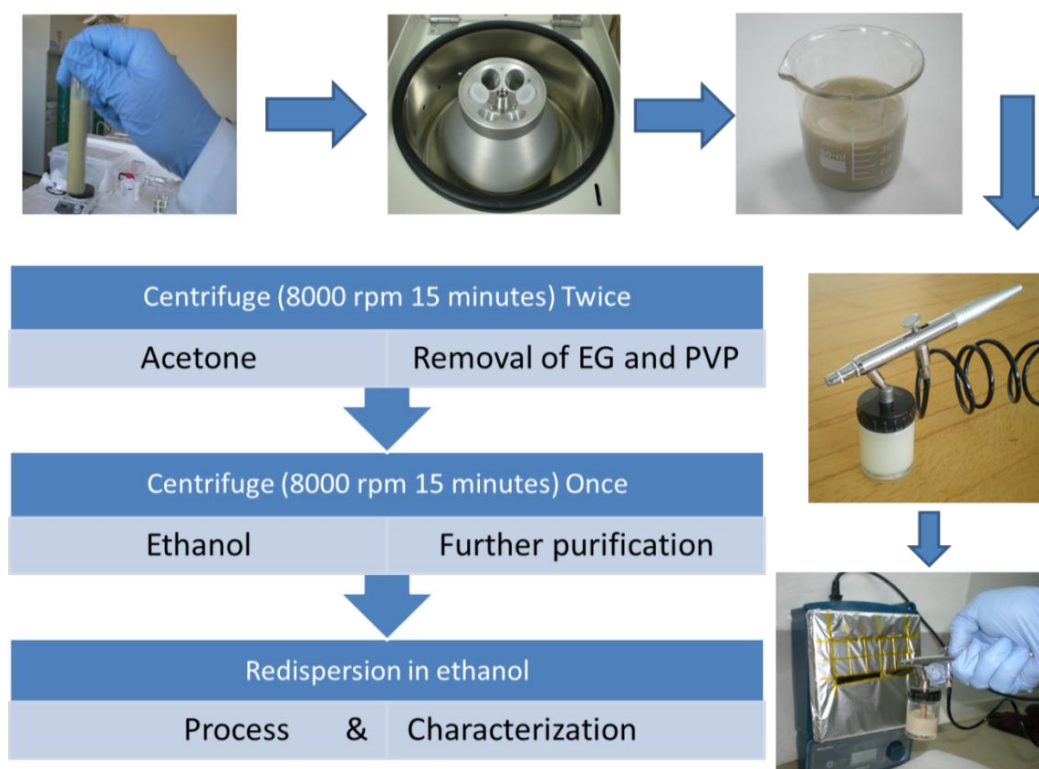
Figure 3.9 Flow chart showing the nanowire purification and deposition of Ag NW networks onto substrates [79].

In our experiments, air brush pressure was set to 2 atm and the distance between airbrush and hot plate was kept at 10 cm. Density of Ag NWs on substrates can be simply adjusted by the number of spraying cycles. An SEM image of Ag NW network on Si substrate is provided in Figure 3.10. Charge transport path is shown on the image achieved by the continuous current pathways over the NWs.
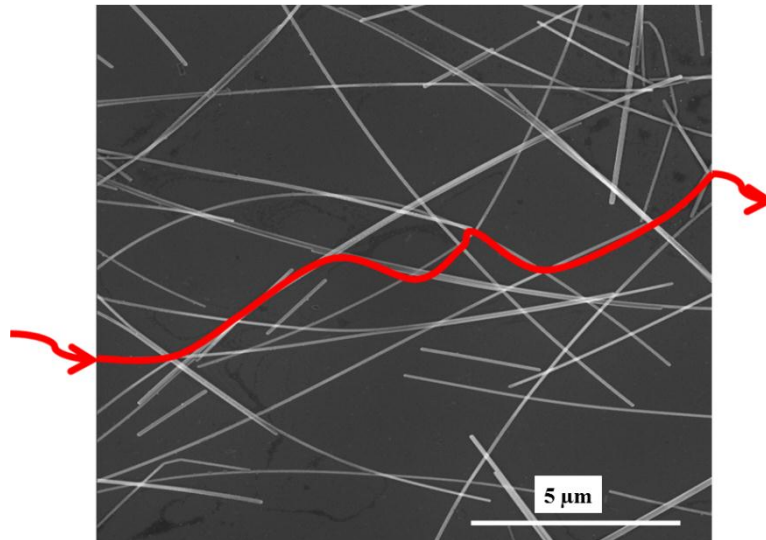
Figure 3.10 An SEM image of Ag NW networks. Possible path for charge transport is clearly marked on the image [79].

3.2.3 Fabrication of Si Solar Cells with Ag NW Network Top Electrode

The structure of fabricated solar cells on flat Si solar cells with Ag NW network top electrode is schematically shown in Fig. 3.11. To fabricate Si solar cells, p-type single-crystalline Si (100) wafers (Resistivity 1–3 Ω.cm), with dimensions of 2 cm × 2 cm × 180 μm (length, width and thickness, respectively) were used. First of all, a saw damage removal process was performed on Si substrates using a 20% sodium hydroxide (NaOH) solution. This was done at 80°C for 2 min. Hydrofluoric acid (HF) cleaning, deionized (DI) water (resistivity 18.3 MΩ) rinsing and nitrogen gas drying carried out subsequently. For the fabrication of solar cells, wafers with saw damage etched surface were n-type doped by Phosphoryl chloride (POCl$_3$) diffusion. The sheet resistance of the doped surfaces was 50 Ω/□. The back Al contacts [Ferro Electronic Materials (Mayfield Heights, OH) AL5130 Aluminum Conductor] were then deposited through screen printing (thickness ~30 μm), which was followed by a co-firing process conducted at 900°C.
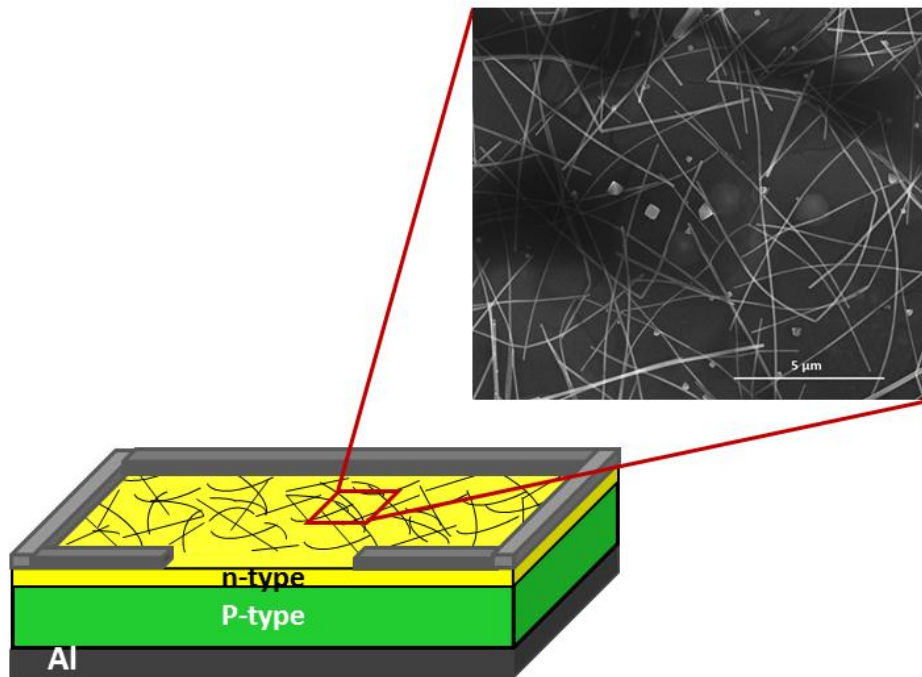
Figure 3.11 Schematic of the fabricated solar cells with Ag NW network top electrode.

Before spray coating of Ag NWs onto top surface of the Si cells, native oxide on the top surface were removed using dilute HF acid, cells were then rinsed and dried with N_2 gas. The cells were then mounted on a hot plate that was set to 150°C to spray coat the ethanolic solution of Ag NWs. Si cells and glass substrates were coated in three sets with different Ag NW densities to investigate the effect of transparency and resistivity of Ag NWs on conversion efficiency of the cells. In order to connect probes during electrical measurements, frame shape Ag paths were deposited using thermal evaporator and shadow mask. The photograph of the fabricated Si cell with Ag NW network top electrode is shown in Figure 3.12. After Ag NW deposition the cells were annealed at 200 °C for 20 minutes under N_2 atmosphere to burn the residual PVP layers and fuse the NW junctions. Annealing at low temperature of 200 °C was not enough to create ohmic contacts between Ag NWs and n-type Si and it seems that electrons could not pass the potential barrier at Ag NW/ Si interface. Therefore, other post annealing temperatures were investigated to improve electron transport from Si to Ag NWs. Important parameters of the solar cell such as short circuit current (J_{sc}), open circuit current (V_{oc}), fill factor (FF), conversion efficiency

(η) and series resistance (R_s) were measured for each cell with different Ag NW network density and compared to reference cells without NW network top contact.
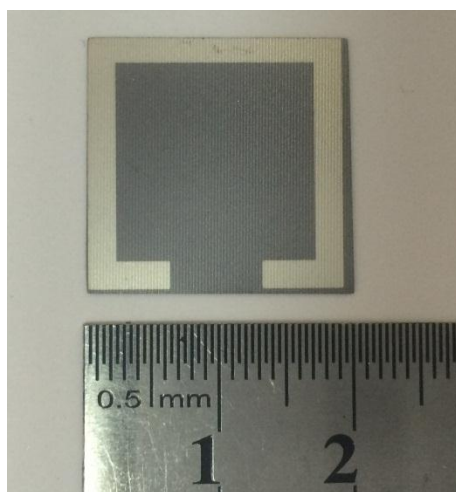
Figure 3.12 Photograph of a Si solar cell with Ag NW network top electrode and frame shape Ag paths for electrical measurements.

3.3 Results and Discussion

3.3.1 Morphology and Sheet Resistance

Three different densities of Ag NW networks were spray coated onto Si cells. Figure 3.13 shows the SEM images of the Si cells with different NW densities. Average length and diameter of the NWs were measured as 75 nm and 12 μm, respectively using an image analysis software, Image J. Similarly, the densities of the NWs were measured from the SEM images. The sheet resistance (R_{sh}) of the NWs deposited on glass substrates was measured using four-point-probe technique. Figure 3.14 shows the R_{sh} of the of the Ag NW networks with respect to NW densities. Sheet resistance of 5 ± 1, 13 ± 2 and 20 ± 5 Ω/□ was obtaind for the NW densities of 1.32, 0.28 and 0.21 NW/μm², respectively. An increase in the NW density from 0.21 to 1.32 NW/μm² resulted in a decrease in sheet resistance from 20 ± 5 to 5 ± 1 Ω/□.
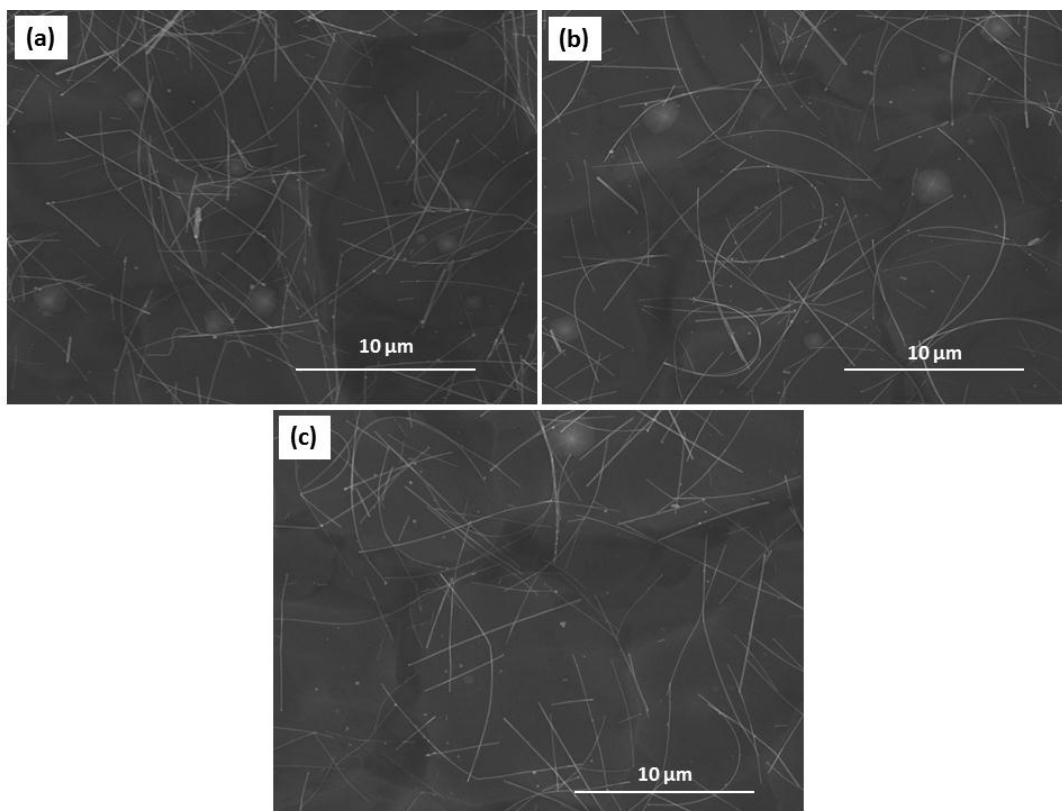
Figure 3.13 SEM images of Ag NW networks on Si with different sheet resistance (R_{sh}) of (a) R_{sh}= 5± 1 Ω/□, (b) R_{sh}=13 ± 2 Ω/□ and (c) R_{sh}= 20 ± 5 Ω/□.
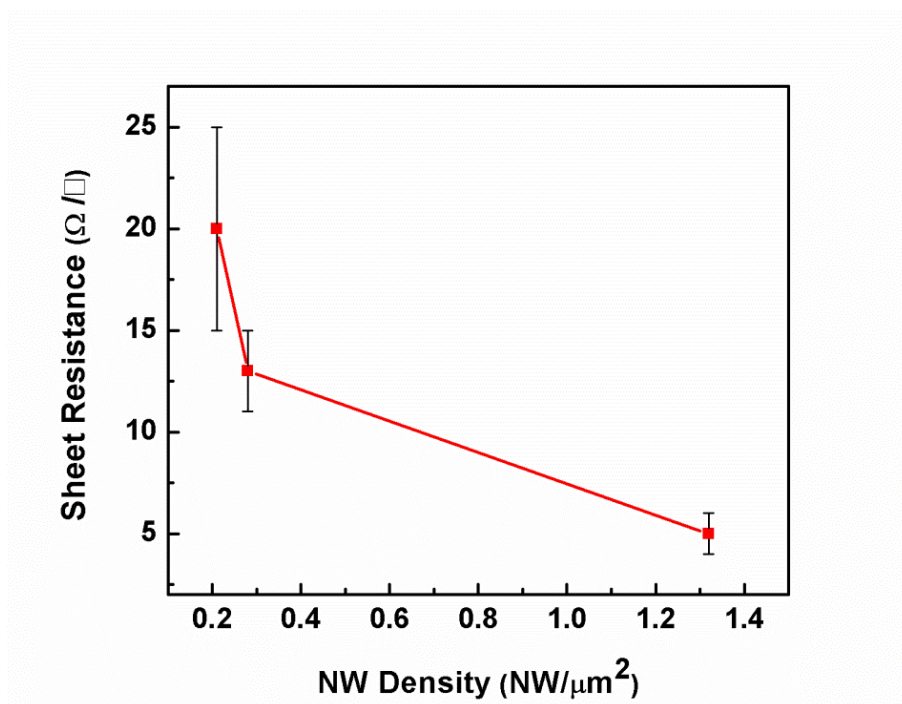
Figure 3.14 Change in sheet resistance with respect to density of Ag NW networks. Lines are for visual aid.

3.3.2 Optical Measurements

3.3.2.1 Optical Transmittance

Total and diffuse transmittance spectra for the samples with three different NW densities on glass substrates are shown in Figure 3.15 (a) and (b) respectively. From the total transmittance spectra it is observed that transmission behavior is the same for all samples and transmittance was reduced by increasing the NW density. For the wavelengths less than 700 nm, the transmittance decreased and resulted in a minimum within the wavelength range of 350-400 nm. Reduced transmission spectra was attributed to localized surface plasmon resonances (LSPRs) of Ag NWs [88,89].

Increase in the NW density resulted in an increase in diffuse transmittance. It achieved a maximum value of 9.4% at a wavelength of ~ 400 nm for the sample with the highest NW density (5±1 $\Omega/\square$). This enhancement is attributed to the fact that Ag NWs scatter light in all directions with a larger fraction of scattered light coupling into the higher refractive index medium.
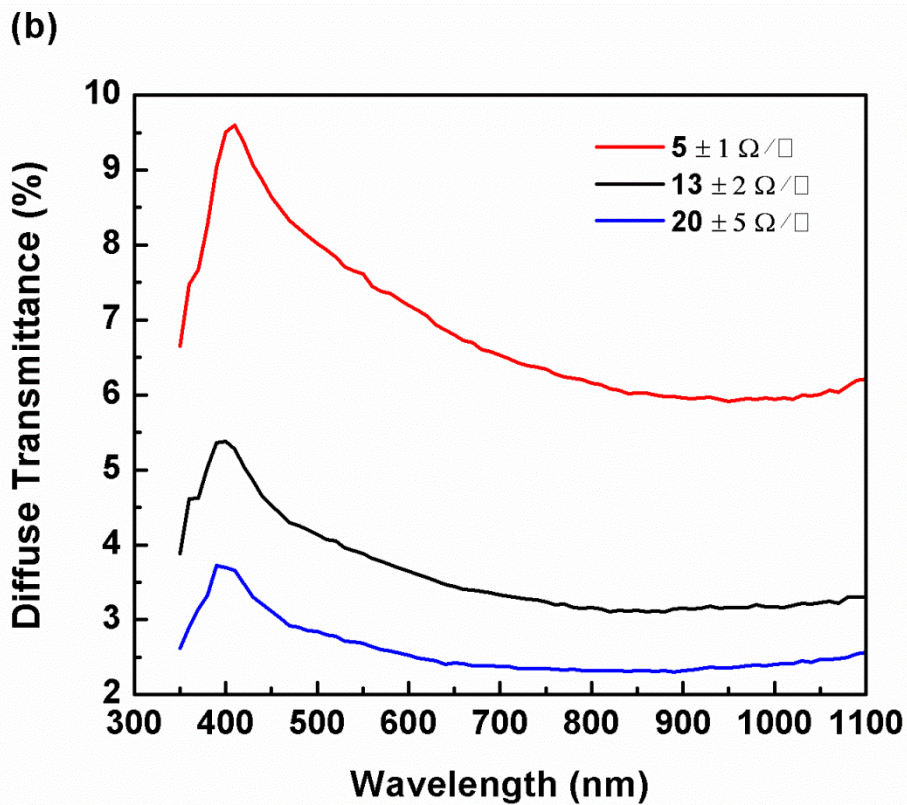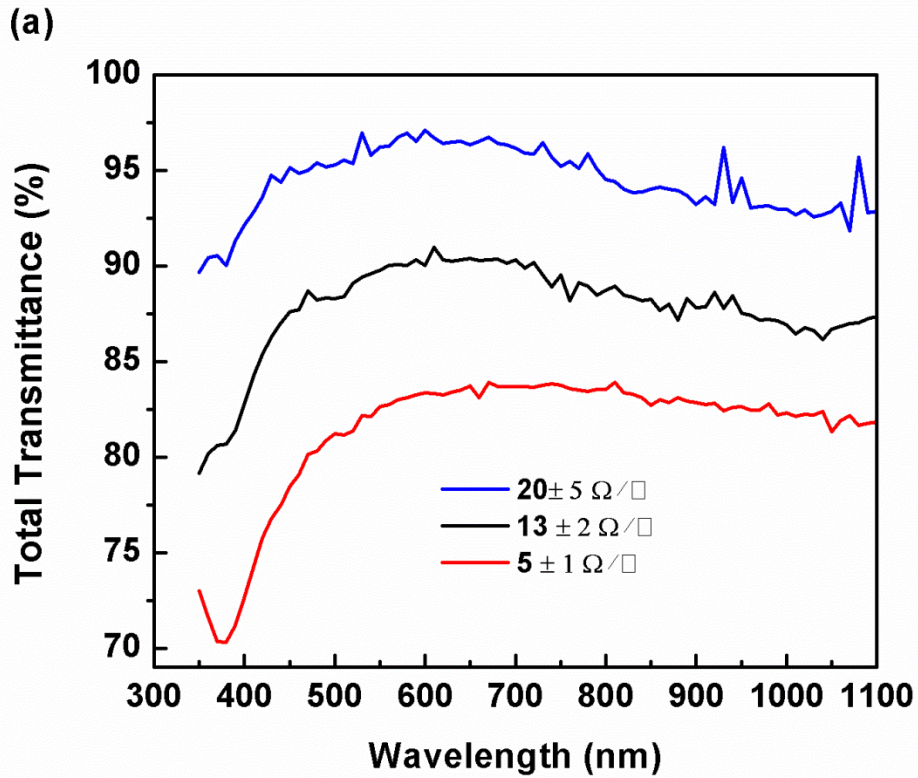
Figure 3.15 (a) Total and (b) diffuse transmittance spectra of Ag NW networks deposited onto glass with different sheet resistances.

3.3.2.2 Reflectance

The reflectance spectra of the Si substrates with different Ag NW network resistances are presented in Figure 3.16.
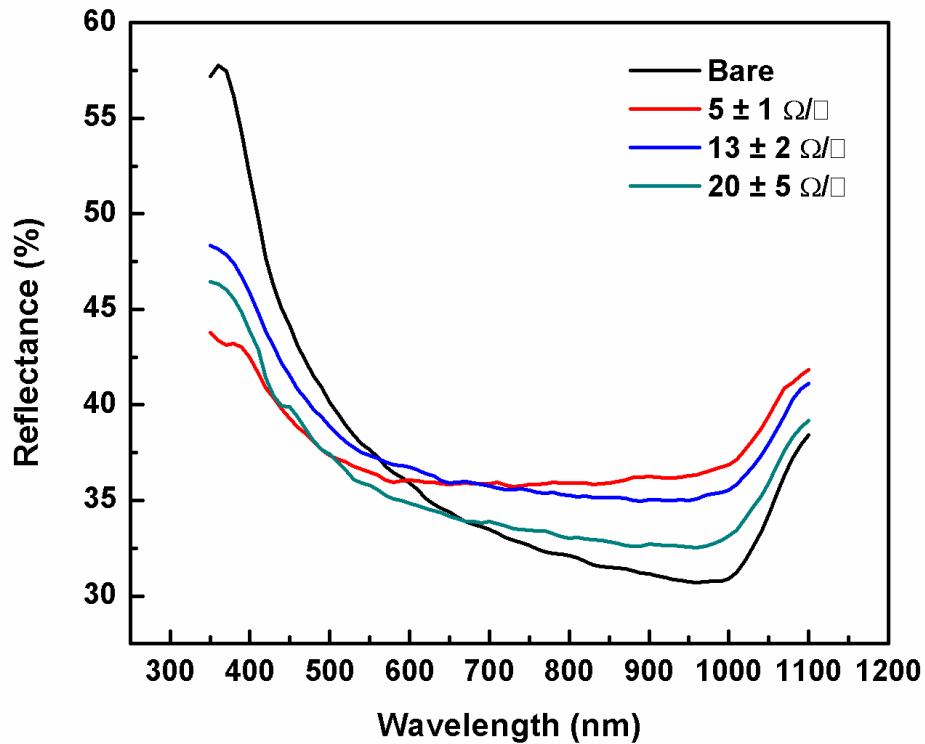
Figure 3.16 Reflectance spectra of Si cells with different Ag NW network resistances.

It was observed that through the deposition of Ag NWs onto Si, the reflectance of the substrates increase above ~ 680 nm with respect to bare Si substrate. In addition, above ~ 680 nm, reflectivity of the substrates with Ag NWs was found to scale with the NW density. This enhancement in reflectance was associated with a decrease in transmittance as shown in Figure 3.15 (a). An increase in the NW density enhanced the reflectance compared to bare Si at lower wavelengths. On the contrary, below ~ 680 nm the reflectance of the NW substrates became lower than that of bare Si. Moreover, less dense NW substrates had higher reflectance compared to bare Si. This reduced reflectance could be attributed to light scattering by the Ag NW network at LSPR frequency [88,89].

3.3.3 Solar Cell Characteristics

3.3.3.1 I-V Curves of the Cells with as Deposited Ag NWs

Following the deposition of the Ag NWs on top of the Si cells, an annealing process was conducted at 200 °C for 20 minutes under N_2 ambient to remove organic residuals. I-V curves of the cells with as-deposited Ag NW network is presented in Figure 3.17. The photovoltaic parameters are tabulated and provided in table 3.1 as well.
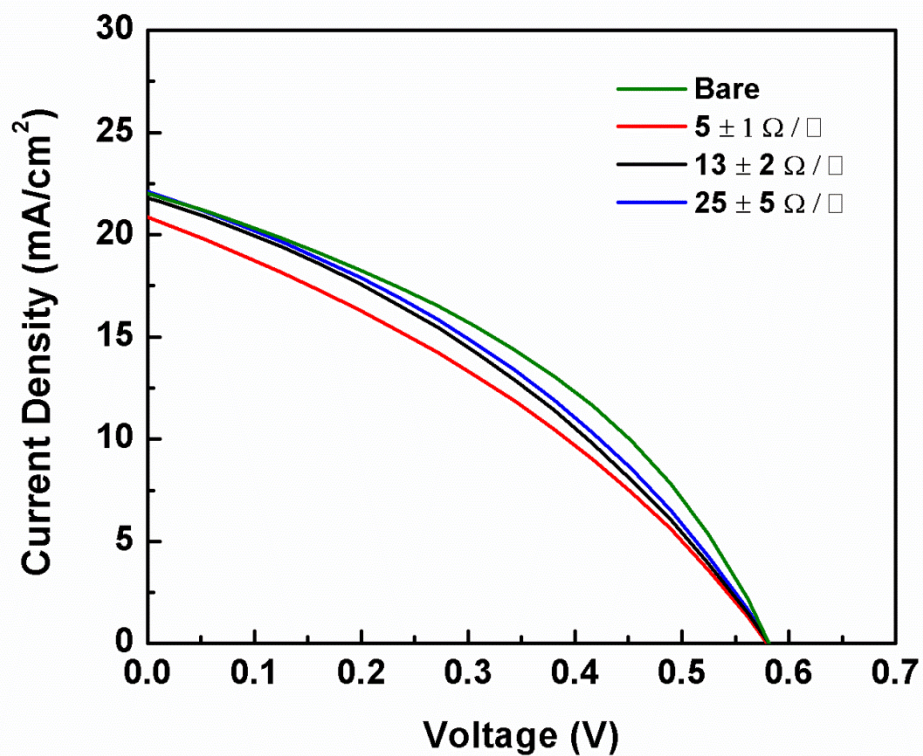
Figure 3.17 I-V curves of the solar cells with as deposited Ag NW network top contacts.

Table 3.1 Photovoltaic parameters of solar cells with as deposited Ag NW network top electrodes.

Sample	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)	R_s	R_{sh}
Bare	0.56	21.82	38.67	4.75	2.37	14.55
5 ± 1 $\Omega/\square$	0.57	21.02	33.38	4.03	3.8	16.12
13 ± 2 $\Omega/\square$	0.57	21.66	34.65	4.29	3.8	18.84
20 ± 5 $\Omega/\square$	0.57	22.07	35.24	4.41	3.24	18.75

It is clear from I-V curves of the cells that J_{sc} decreases for cells with higher NW density due to light reflection of the Ag NWs. Moreover, deposition of Ag NWs gave rise to series resistance (R_s) of the cells and R_s was enhanced with an increase in NW density, which resulted in an overall reduction in photovoltaic conversion efficiency (η). This would be attributed to the lack of ohmic contact at the Ag NWs/n-Si interface. In other words, charge carries were not able to pass through the potential barrier of the interface between Ag NWs and Si. Therefore, annealing at 200 °C was found to be insufficient to create ohmic contact between the Ag NWs and Si. A post annealing process that takes place at temperatures higher than 200 °C was designed to enhance electron extraction from Si.

3.3.3.2 Post Annealing Process

To create ohmic contacts between Si and Ag NWs, cells with a resistivity of 5 ± 1 $\Omega/\square$ were annealed at different range of temperatures for different periods. Changes in R_s and η with respect to annealing time are plotted at 4 different temperatures in 3.18 (a) and (b) respectively. From Figure 3.18 (a) it is clear that annealing the cells at 325 °C for 1, 2 and 3 minutes do not change series resistance of the cells, revealing that the ohmic contact between Ag NWs and Si do not exist in this temperature. Therefore, η of the cells did not change significantly upon annealing at this temperature, as observed in Figure 3.18 (b).
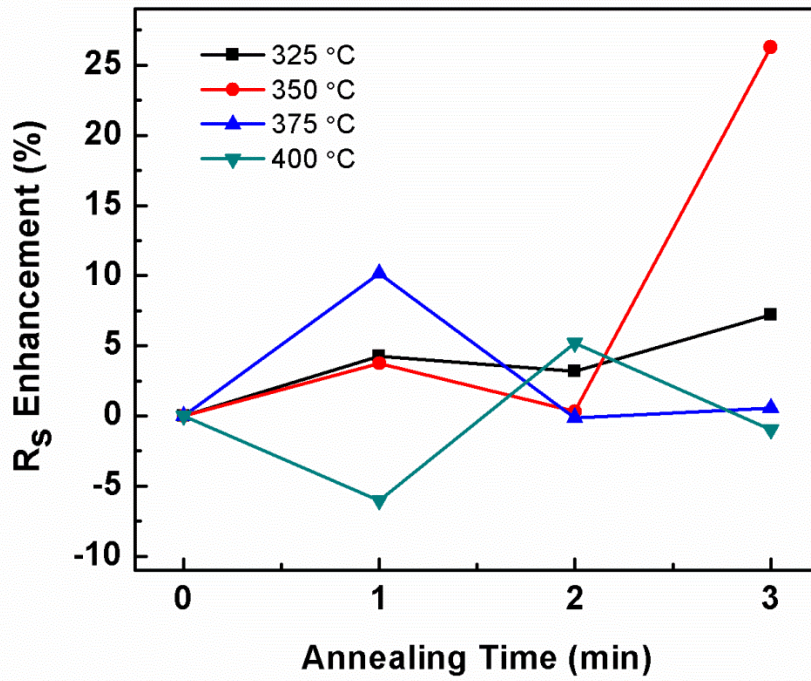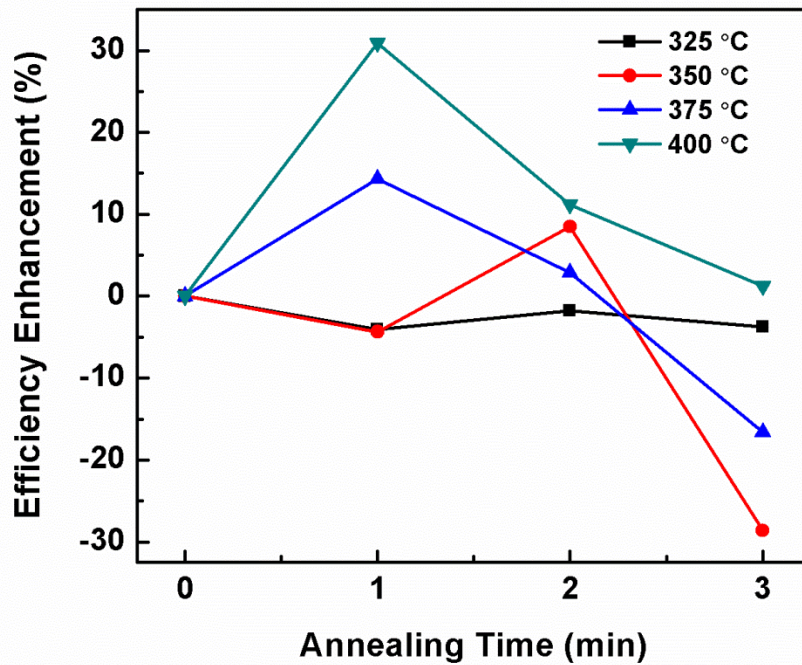
Figure 3.18 Enhancement in (a) R_s and (b) η as a function of annealing time at different temperatures for the cell with a resistance of 5±1 $\Omega/\square$. Lines are for visual aid.

Upon increasing the annealing temperature to 350 °C and 375 °C, a slight decrease in R_s was observed after 2 minutes of annealing. Reduced R_s resulted in an increase in the conversion efficiency, as observed in Figure 3.18 (a). Annealing duration was then increased to 3 minutes and the R_s was found to increase due to breaking and isolation of the Ag NWs. The maximum improvement in R_s (corresponding to 6%) was observed for the cell that was annealed at 400 °C for 1 minute. Reduced R_s enhanced η of the cell by 31% at this temperature. Longer annealing durations caused an abrupt increase in R_s and a subsequent drop in η. As a result, the optimum annealing temperature and duration determined as was 400 °C and 1 min respectively, where a good ohmic contact was formed at the Ag NW/Si interface. SEM images of the cell annealed at 400 °C for 1minute are provided in Figure 3.19. Although, NW breaking and isolations were observed in some parts of the sample but these isolated NWs still provided low resistance routes for electron transport. Therefore, electrons prefer to use these low resistance paths to travel along the Si from one point to another to reach the electrodes. This also decreases the probability of recombination.
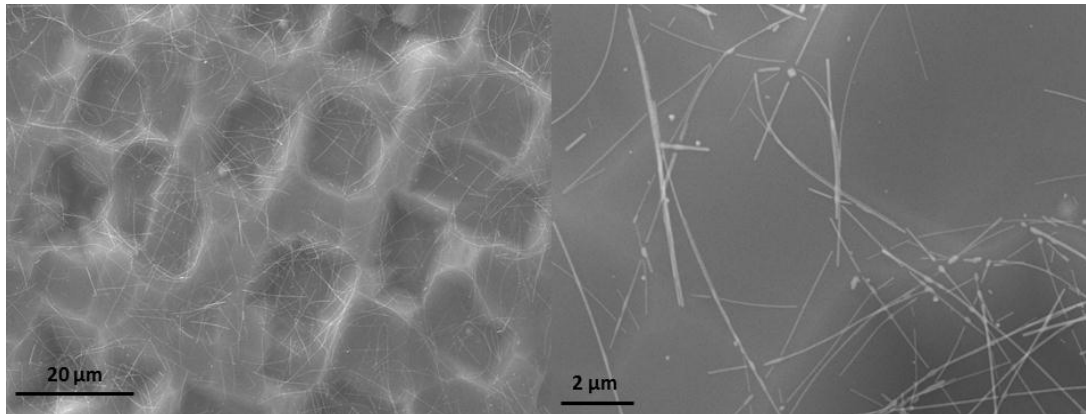
Figure 3.19 Low (left) and high (right) resolution SEM images of solar cell with Ag NW network top contact annealed at 400 °C for 1 minute.

The photovoltaic parameters of the cells that were annealed at 400 °C for various durations with different Ag NW resistivities, are provided in Figure 3.20. In all the cells with different resistances an enhancement of 10% in J_{sc} was observed after 1 to 2 minutes annealing due to the formation of ohmic contacts at the interface of Ag NWs and Si. Increase in the number of collected charge carriers, consequently

increased FF and η. An enhancement of more than 20% in η was observed for all the cells. On the contrary, V_{oc} remained unchanged during annealing process.
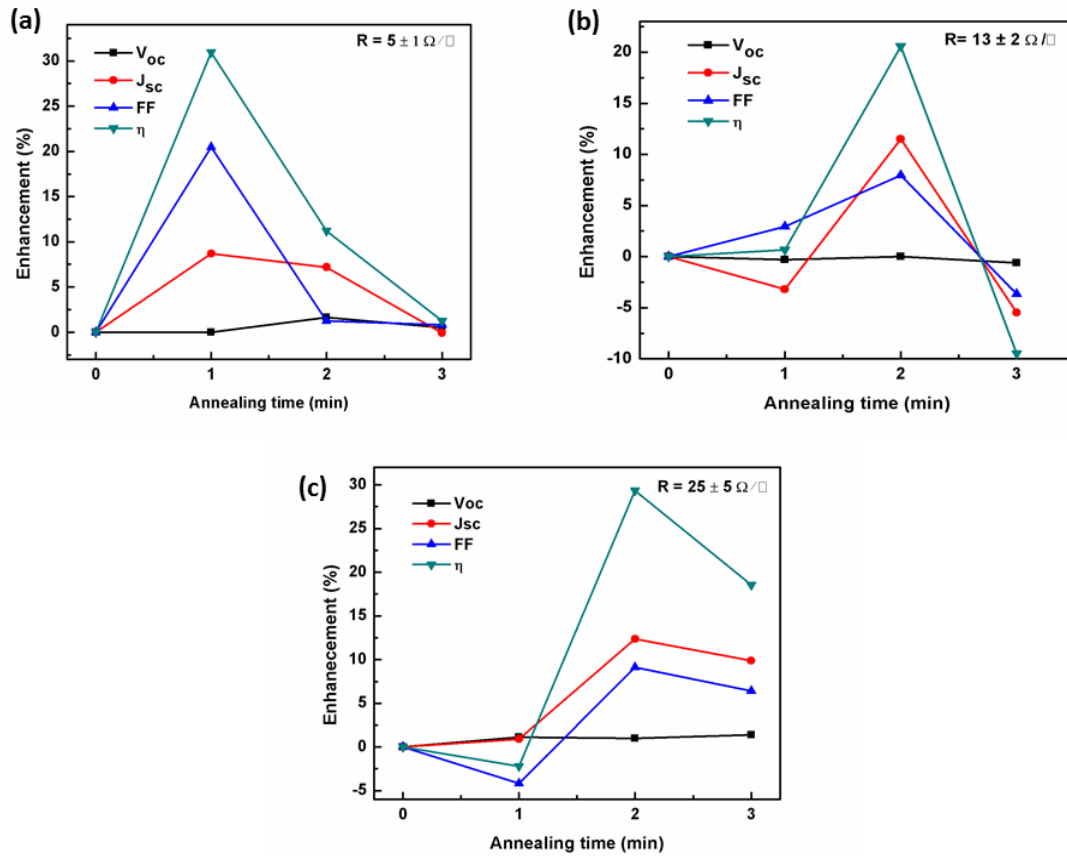
Figure 3.20 Enhancement in photovoltaic parameters of Ag NW top electrode cells with resistances of (a) R_{sh}= 5± 1 Ω/□, (b) R_{sh}=13 ± 2 Ω/□ and (c) R_{sh}= 20 ± 5 Ω/□ annealed at 400 °C as a function of annealing durations..

3.3.3.3 I-V Curves of the Cells with Optimized Top Contact

I-V curves of the cells with optimized ohmic top contact are provided in Figure 3.21. The photovoltaic parameters are tabulated and provided in Table 3.2. Unlike the cells with as-deposited Ag NWs, annealed cells showed enhancement in the J_{sc} due to improved electron collection through the Ag NWs in contrast to the reference cell.

This improvement in J_{sc} was more obvious for the cell with lower NW resistance (5 ± 1 $\Omega/\square$) due to higher amount of NWs on the surface of cells to collect carriers. It is clear from the table that V_{oc} did not change significantly for the cells with and without Ag NWs. In higher resistance Ag NW cells, FF and η were found to decrease when compared to lower resistance cell due to higher serie resistance. The highest η was obtained for the sample with the resistance of 5 ± 1 $\Omega/\square$ and a relative improvement of 21 % (from 4.75 % to 5.73 %) was obtained in η when compared to reference cell.
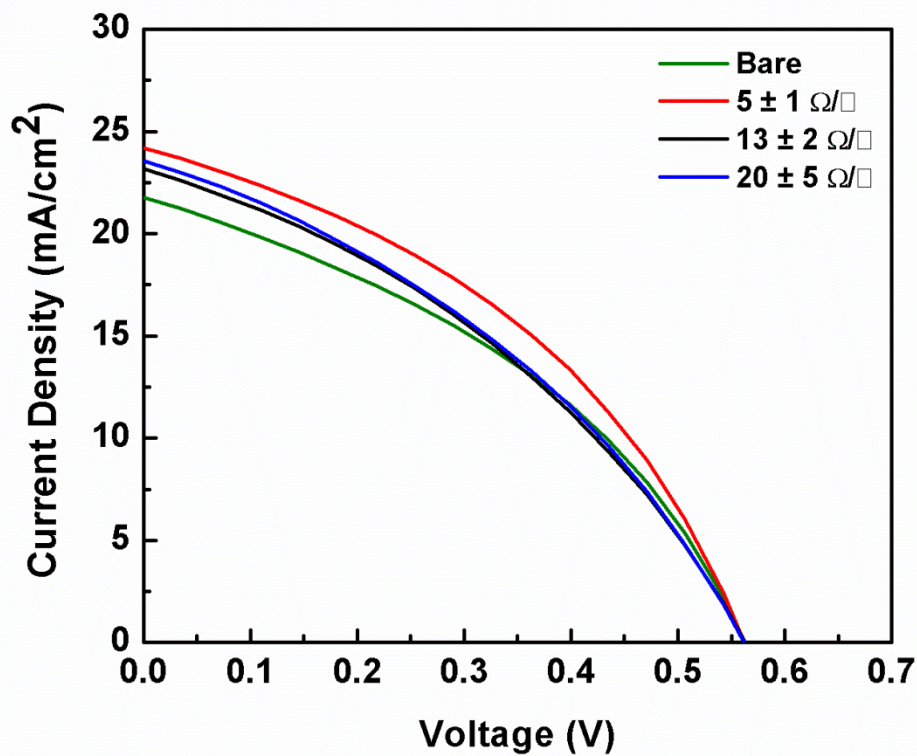
Figure 3.21 J-V curves of the cells following Ag NW network top contact optimization.

Table 3.2 Photovoltaic parameters of the cells following optimization of Ag NWs top electrode.

Sample	Voc (V)	Jsc (mA/cm^2)	FF (%)	η (%)	R_s	R_{sh}
Bare	0.56	21.82	38.67	4.75	2.37	14.55
5 ± 1 Ω/□	0.58	24.75	39.85	5.73	2.1	37.86
13 ± 2 Ω/□	0.58	23.61	36.42	4.96	3.11	25.3
20 ± 5 Ω/□	0.58	23.71	37.1	5.13	2.7	17.8

3.3.4 EQE Measurements

Figure 3.22 shows the EQE results of the reference cell and the cells with different Ag NW resistances. For the more resistive Ag NW cells (R_{sh}=13 ± 2 Ω/□ and R_{sh}= 20 ± 5 Ω/□), EQE showed a decrease through the whole wavelength range. This could be attributed to two optical behaviors of Ag NWs. In the wavelength range of 350 - 400 nm Ag NWs absorb incident light due to surface plasmon resonance (Figure 3.15 (a)); therefore, the light absorption in Si decreases reducing the number of generated carriers. In the wavelength range of 550-1100 nm, Ag NWs increase light reflection (Figure 3.16), which results in lower EQE. However, a slight increase in the EQE was observed for the cell with lower resistance (R_{sh}= 5 ± 1 Ω/□) in wavelength range of (500 - 1000 nm). This could be attributed to the improved carrier collection within the cell. Therefore, despite to lower carrier generation in this wavelength range, increase in the number of collected carriers gives rise to EQE.
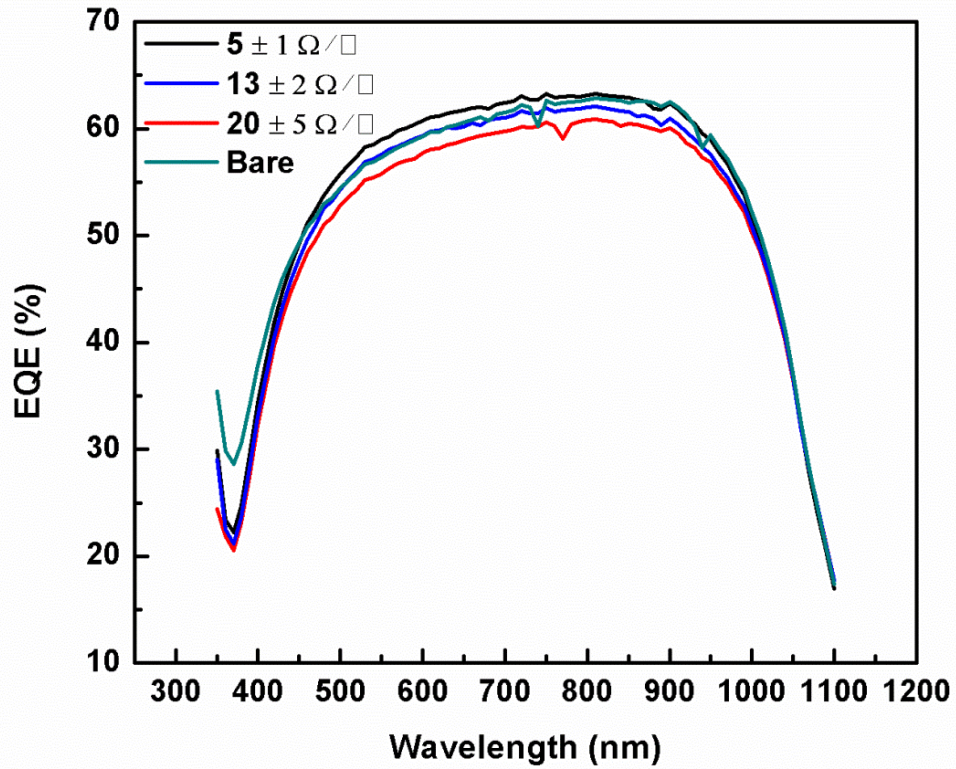
Figure 3.22 EQE plots for the cells with different densities of Ag NW network top contacts.

3.4 Conclusions

In this chapter Ag NWs synthesized via polyol process, were utilized as the top contact of the crystal Si solar cells with three different resistances. High temperature annealing was performed to induce the formation of ohmic contacts between NWs and n-type Si. A maximum relative enhancement of 31 % in efficiency was observed by annealing the cells at 400 °C for 1 min. High temperature annealing resulted in partially breaking and isolation of the NWs and limited the efficiency enhancement; but, isolated NWs still provided low resistance routes for electrons at local spots. Therefore, rather than traveling long distances in resistive Si, which increase the recombination probability electrons are using these low resistance paths to travel along the Si from one point to another to reach the electrodes. The highest η was

obtained for the sample with the lowest resistance of 5 ± 1 $\Omega/\square$ and relative improvement of 21 % (from 4.75% to 5.73%) in η was obtained for this cell compared to the reference cell without NWs.

CHAPTER 4

APPLICATION OF NANOWIRE DECORATED ULTRATHIN SINGLE CRYSTALLINE SI TO PHOTOVOLTAIC DEVICES

4.1 Introduction

4.1.1 Thin Si Applications in Photovoltaics

Although many studies have been conducted in laboratories to fabricate variety of solar cells using different materials, first generation solar cells, which are single and polycrystalline Si cells, still dominate the photovoltaic market. Compared to different photovoltaic technologies in terms of commercial availability, crystalline Si solar cells continue to be preferred due to their low cost and availability [90]. The cost-efficiency and commercial availability of different photovoltaic technologies are compared in Figure 4.1 [91]. According to the provided graph, the conversion efficiency of the crystalline Si cells is relatively high (15-20%) and their moderate manufacturing cost make them the most feasible type of solar cells. They account for about 85% of devices sold today.

Si as one of the most important materials has been driving the great success of electronics, optoelectronics and solar cell industriy, where it is used in the form of single and multicrystalline wafers and amorphous and nanocrystalline films. Crystalline Si (c-Si) is an attractive material for photovoltaic cells due to its natural abundance, extensive experience and knowledge in processing this material.
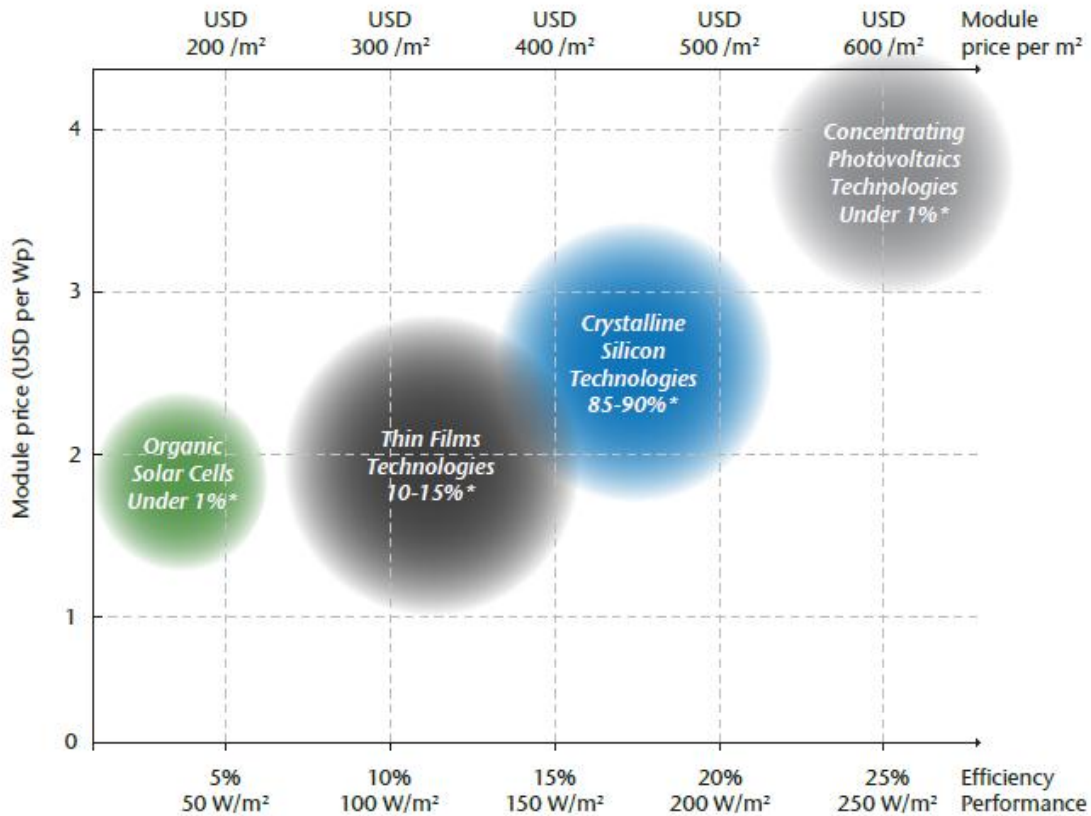
Figure 4.1 Performance and cost comparison of commercially available photovoltaic technologies [91].

A significant scaling factor driving the cost reduction in Si-based photovoltaic cells is the reduction of Si thickness, since Si materials constitute the major portion of the manufacturing costs. Si, an indirect band gap semiconductor, has a low absorption coefficient and currently requires the use of fairly thick wafers (~180 microns today) to absorb a large portion of the sun's spectrum. In addition, current technology for handling and processing of solar cells is not suited for Si wafers of thicknesses much below current ~180 micron thickness.

Figure 4.2 shows some of the thin Si based production approaches that are used to significantly reduce the cost of solar cells. In Figure 4.2 (a) a thin layer of Si has been formed by chemical vapor deposition (CVD) method [92]. Figure 4.2 (b) indicates that thin layer of Si is produced by removing a top layer of the porous Si layer [93]; Another process which is developed in IMEC has been shown in Figure 4.2 (c).

In this process, by a mechanical step such as that used in the SLIM-cut process a thin layer of Si is obtained with the help of the thin metal film [94]. By using thin layers of active materials, it would be possible to use low quality Si materials with short carrier diffusion length. It also increases fill factor and open circuit voltage and reduces Auger recombination [95,96]. Another advantage of the ultra-thin solar cells is that they allow the production of both flexible and very lightweight devices.
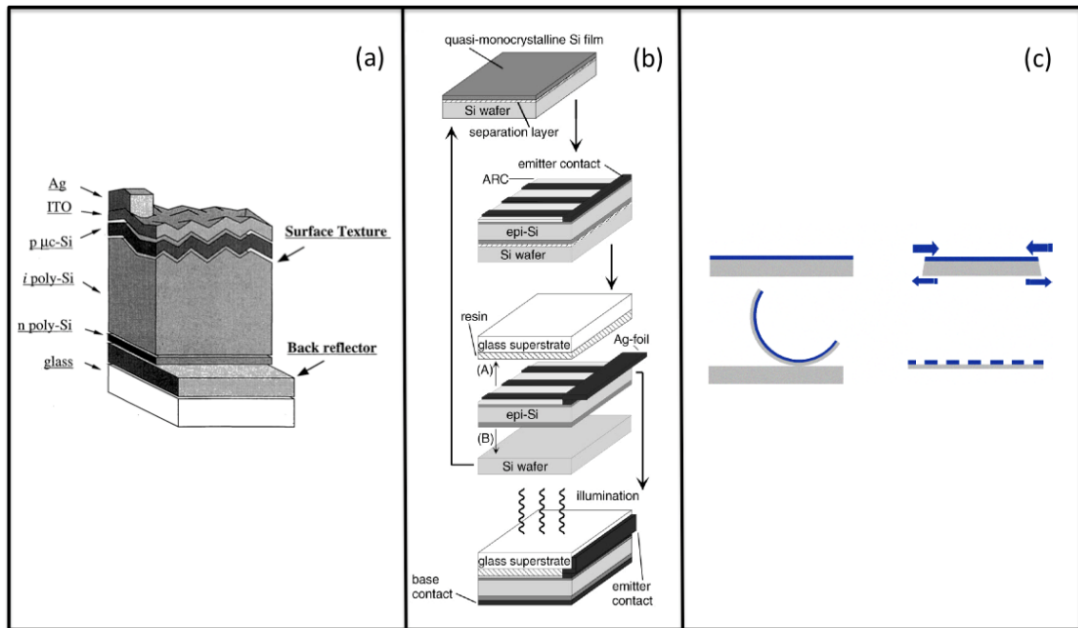
Figure 4.2 Schematics of some of the methods that were used to fabricate thin Si. (a) a cell that was made by depositing thin layer of Si using CVD [92], (b) thin layer of Si was made by removing top layer of porous Si [91]. (c) SLIM-Cut technique conducted in IMEC [94].

Most of the work done on thin-film Si cells has focused on cells which are almost a few tens of microns thick. Relatively little work has focused on the design and fabrication of c-Si solar cells with film thicknesses in the sub-micron range. Such ultrathin c-Si cells are of interest because they further limit the amount of material needed and allow for adequate electrical performance despite of the decreased carrier diffusion lengths.

Recently, ultrathin Si fabricated by Wang et al. using KOH etching, exhibited excellent mechanical flexibility and bendability. Unexpectedly, these ultrathin Si materials can be cut with scissors like a piece of paper and they are robust during various regular fabrication processes including tweezer handling, spin coating, patterning, doping, wet and dry etching, annealing and metal deposition. This can create new possibilities for ultrathin monocrystalline Si devices, particularly in applications in solar cell technologies. They studied the light trapping effect in the ultrathin Si films by a double-sided nanotextured design, showing a large improvement in light absorption [97].

Decreasing thickness of Si reduces cost; but, it also decreases efficiency of the solar cells. This effect has been shown in Figure 4.3. According to this graph, when the thickness is reduced from 200 microns to 50 microns, cell efficiency reduces by 0.5 % and wafer price drops to one-third of its primitive value. Further reduction of the thickness pushes efficiency to zero [98]. This is because of the light trapping mechanism is not considered in this graphic.
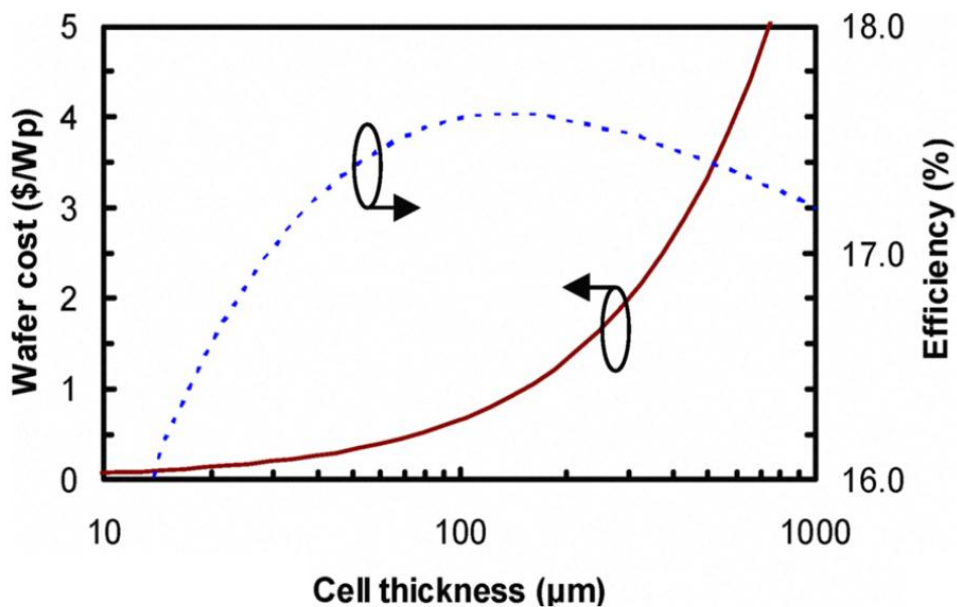
Figure 4.3 Si wafer cost and cell efficiency versus cell thickness [98].

4.1.2 Isotropic and Anisotropic Etching of Si

Etching of the thin films deposited onto a substrate or substrate itself is a necessary process in the fabrication of MEMS structures. Generally, there are two fundamental types of etching:

1. Wet etching: Chemical solution is used to dissolve the material.
2. Dry etching: Vapor phase etchant or reactive ions are used to dissolve the material.

Wet etching is the simplest and easiest etching technology and it works very well for etching thin films. It usually requires a mask, which does not dissolve in the etching solution or at least has slower etching rate in order to selectively etch the material. Some crystalline materials, such as Si exhibit anisotropic etching in certain chemicals. In anisotropic etching, the etching rate is different for different crystallographic directions. Contrarily, isotropic etching refers to a process in which etching rate remains constant in all the crystallographic directions. The problem of isotropic etching is undercutting of the mask layer by the same distance as the etch depth. The classic example of this is the <111> crystal plane sidewalls that appear when etching a hole in a <100> Si wafer in a chemical, such as potassium hydroxide (KOH). The result is a pyramid shaped hole instead of a hole with rounded sidewalls with an isotropic etchant. The principle of anisotropic and isotropic wet etching is schematically illustrated in the Figure 4.4.
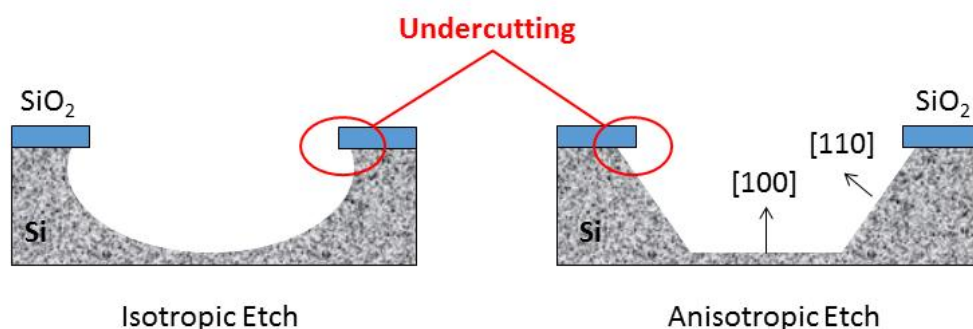
Figure 4.4 Schematics of isotropic and anisotropic etching of Si.

Anisotropic etching of Si is usually done by alkaline etchants such as aqueous KOH, tetramethylammonium hydroxide (TMAH) and other alkaline hydroxides like sodium hydroxide (NaOH) and lithium hydroxide (LiOH). Due to the strong dependence of the etch rate on crystal direction and on etchant concentration, a large variety of Si structures can be fabricated in a highly controllable and reproducible manner. Hence, anisotropic etching of (100) Si has been a key process in common MEMS based technologies for realizing 3-D structures [99].

In order to minimize the influence of other chemicals on the etching mechanism and thus, to obtain more accurate results, pure KOH solution has been preferred over a number of mixtures with moderators like ethylene diamine pyrocatechol (EDP) and isopropyl alcohol (IPA) [100].

4.1.3 One Dimensional Nanostructures for Solar cells

The need for the low cost fabrication of solar cells and to get higher efficiencies are the driving forces for scientist to search for nanostructured alternative materials that can be used in photovoltaics [101-103]. As schematically shown in Figure 4.5 all radial, axial and substrate junctions of nanowire solar cells will provide plenty of advantages in comparison with conventional wafer-based solar cells. Nanowire arrays with radial junction, maintain benefits such as enhanced light absorption, new charge separation mechanisms and strain relaxation and low cost. Although, axial junction solar cells may have low carrier separation efficiency, they still benefit from high light absorption due to light trapping effect [105].
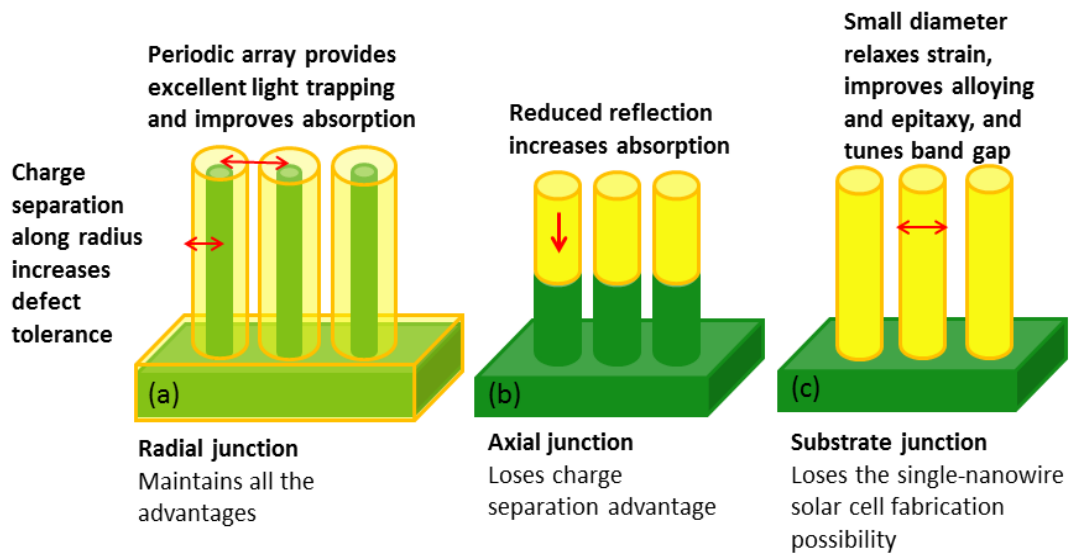
Figure 4.5 Schematics of different geometry of nanowire solar cells. (*a*) Radial, (*b*) axial and (*c*) substrate junction solar cells [105].

In practice, the efficiency of nanowire based solar cells may not exceed the limits of planar devices; but, at least they do not require expensive materials and fabrication processes.

A wide variety of materials have been used in the fabrication of nanowire based solar cells including Si, germanium, zinc oxide, zinc sulfide, cadmium telluride, cadmium selenide, copper oxide, titanium oxide, gallium nitride, indium gallium nitride, gallium arsenide, indium arsenide, and many polymer/nanowire combinations [101,106–110]. In recent years, improvements have been achieved in output efficiencies of nanowire solar cells; however, there are still challenges to be overcome.

4.1.4 Conventional Si Nanowire Synthesis Methods

Variety of methods have been reported for the fabrication of Si NWs. They are categorized according to their main mechanism, such as bottom-up and top-down methods. Some of the commonly used methods for the Si NW fabrication are listed in Figure 4.6. Bottom-up methods such as chemical vapor deposition (CVD) and vapor liquid solid (VLS) are usually costly and require high temperatures, high vacuum, complex equipment and hazardous precursors. Moreover, these methods are not applicable to large areas due to limitation of the setups used. Top-down methods are based on lithography and direct reactive ion etching (DRIE).

Electroless etching (EE) method also known as metal assisted chemical (MAC) ecthing is one of the top-down approaches. It is a solution based method which enables production of Si NWs arrays at low temperature and over large areas. The most important advantage of this method is that fabricated nanowires will have exactly the same properties of the starting Si substrates.
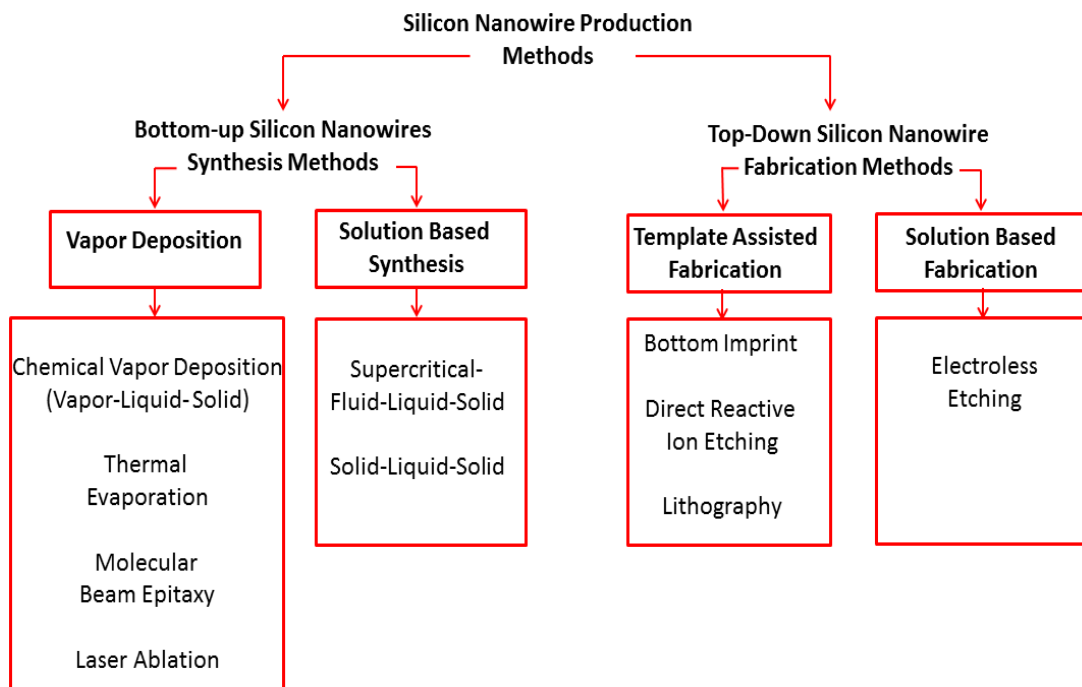
Figure 4.6 Various methods for the synthesis of Si NWs [111].

4.1.4.1 Electroless Etching Mechanism and Reactions

In EE, Si substrates are placed in HF/AgNO$_3$ solution and Ag coating and Si etching take place at the same time. Vertically aligned Si NW arrays form on Si substrates through successive reduction-oxidation reactions.

Si/AgNO$_3$/HF system is composed of a corrosion-type redox couple: the cathodic reduction of Ag$^+$ ions and its counterpart, the anodic oxidation and dissolution of Si, taking place underneath the Ag deposits. Right after immersion of the substrate into the solution, Ag$^+$ ions near the surface of the substrate come into contact and capture electrons from valence band of Si to become Ag(s) nuclei or aggregate. As the reaction continues, Ag nuclei grow into larger clusters. Simultaneously, local oxidation occurs, and SiO$_2$ is produced underneath these Ag nanoparticles. As SiO$_2$ is formed, it is etched with HF that is already present in the solution and pits would immediately form beneath the Ag nanoparticles. As a result of having a higher electronegativity, the Ag particles trapped in these pits do not move horizontally [112]. A schematic of the stages of electroless etching mechanism is shown in Figure 4.7. With longer etching times in the HF/AgNO$_3$ solution, the Ag particles that do not enter the pits would grow into branched Ag dendrites, as shown in Figure 4.8. Ag dendrites need to be removed once the reaction is completed through nitric acid rinse. Reactions governing EE process are as follows [112]:

$$Ag^+ + e^- \rightarrow Ag(s) \qquad\qquad \text{(Eq. 4.1)}$$

$$Si(s) + H_2O \rightarrow SiO_2 + 4\ H^+ + 4\ e^- \qquad\qquad \text{(Eq. 4.2)}$$

$$SiO_2 + 6\ HF \rightarrow H_2SiF_6 + 2\ H_2O \qquad\qquad \text{(Eq. 4.3)}$$
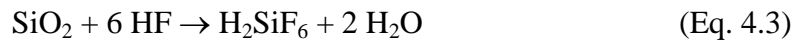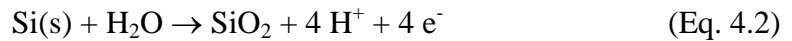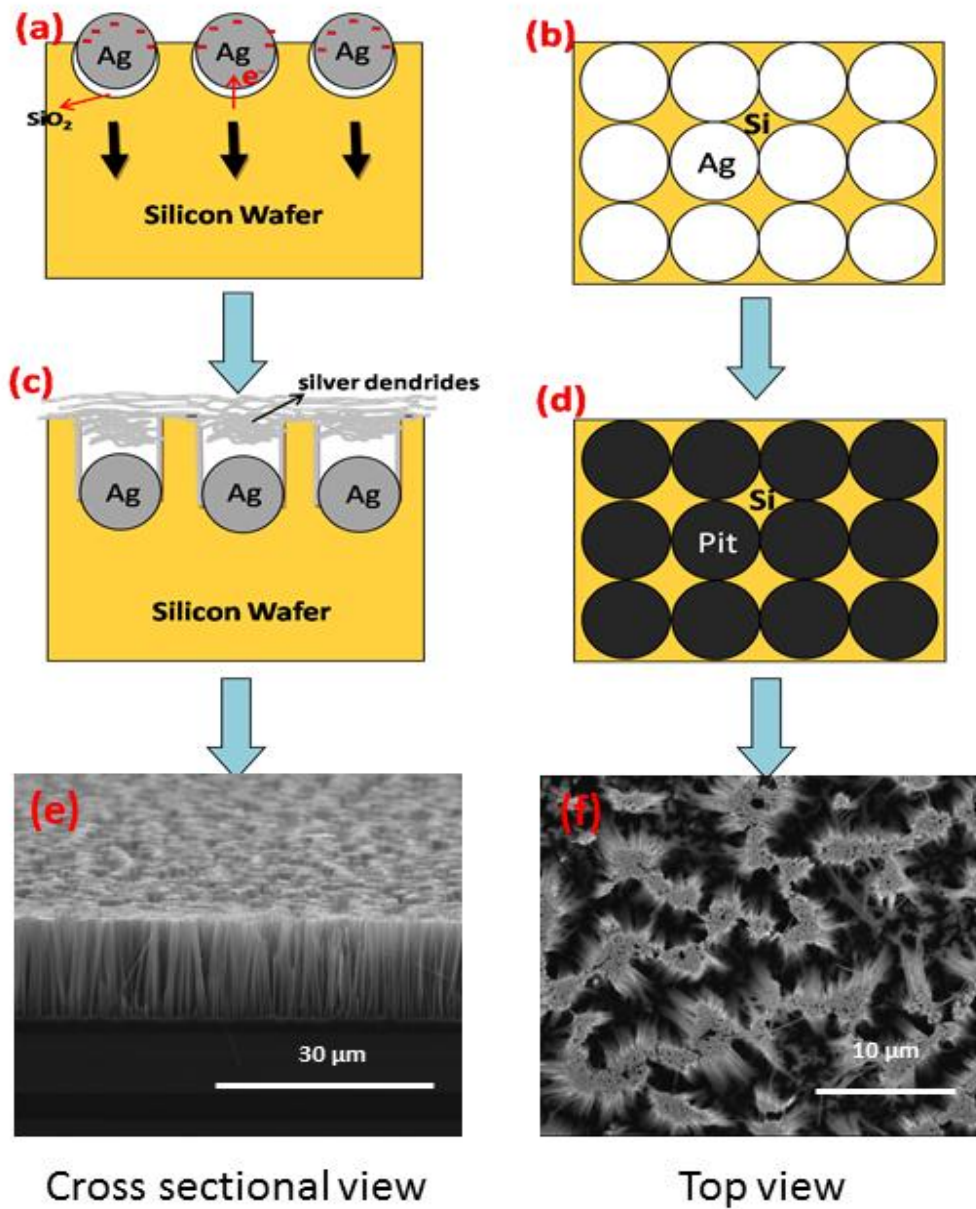
Figure 4.7 Schematic of top and cross sectional view of electroless etching method. (a), (b) represent the initial stages where Ag ions come in to contact with Si. (c), (d) show the vertical etching of Si leaving of Si nanowires. (e), (f) are top and cross sectional SEM images of Si nanowires after removing Ag dendrites [111].
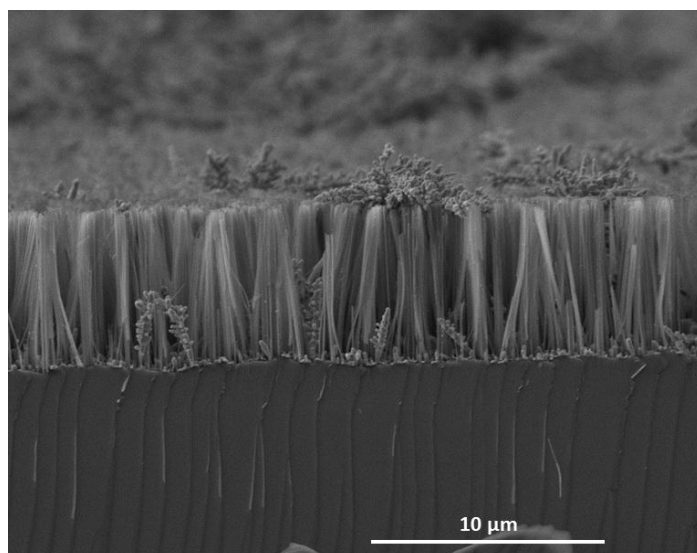
Figure 4.8 SEM images of the fabricated Si NWs via EE method before removing silver dendrites [111].

4.1.4.2 Application of Si Nanowires in Photovoltaics

Si NWs have been used in a wide range of optoelectronic devices. These applications can be listed as solar cells [113,114], lithium batteries [116], light emitting diodes (LEDs) [116] and field effecting transistor (FETs) [117]. In the following section, application of Si NWs in solar cells will be discussed in more detail.

Vertical arrays of Si NWs improve light absorption due to light trapping effect. Figure 4.9 (a) shows a photograph of the Si wafers with and without Si NWs. The dark color of the Si NW sample indicates the enhanced light absorption. The reflectance spectra of Si wafers with different length of Si NWs compared with bare one can be observed in Figure 4.9 (b). This graph indicates that Si NW arrays significantly decrease the reflectivity of the substrate. The minimum reflectivity belongs to the sample with 10 μm long Si NW arrays. By further increase in NW lengths, reflectivity also increased due to the bundle formation [114].
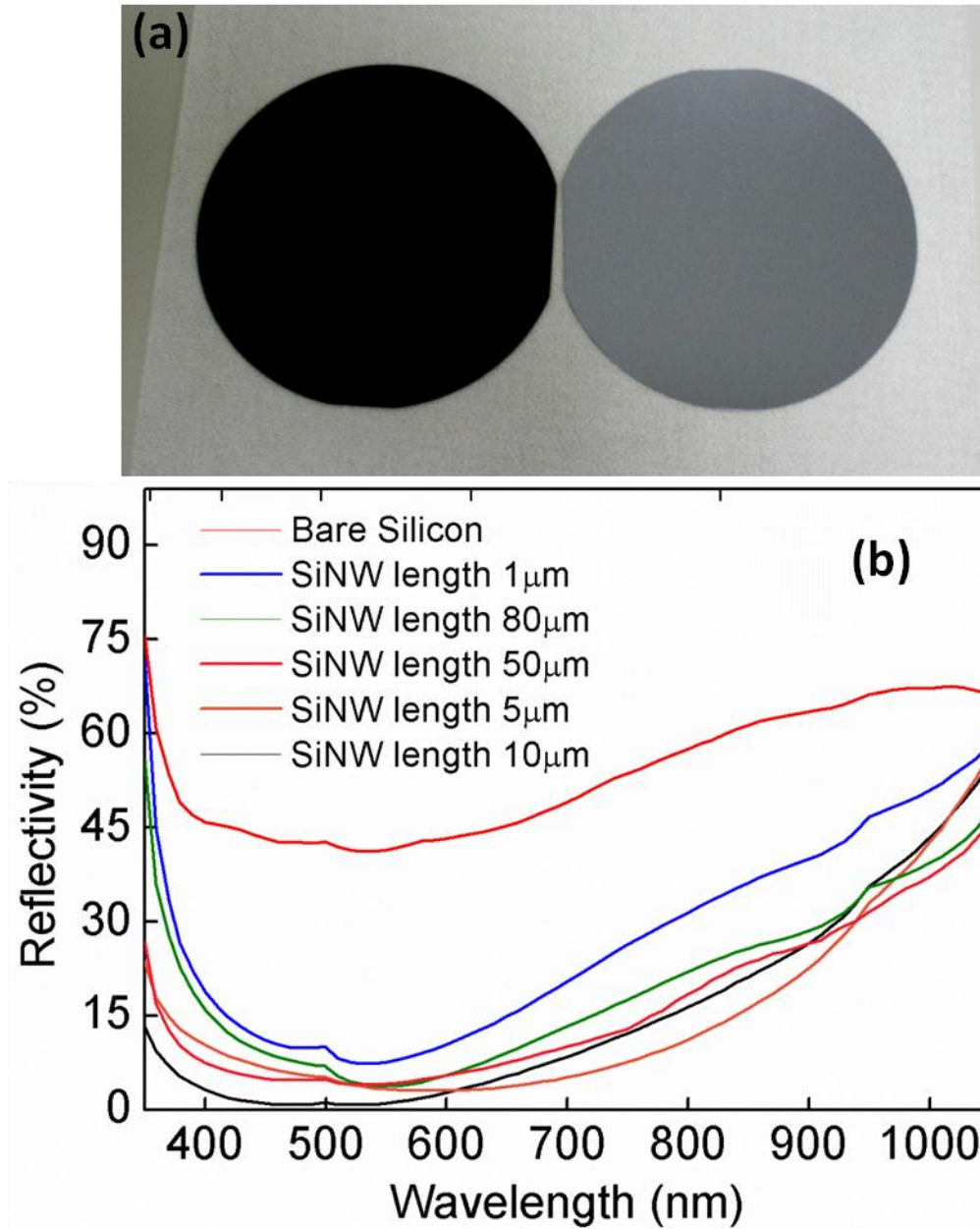
Figure 4.9 (a) Photographs of 4-inch Si wafer before (on the right) and after (on the left) Si nanowire fabricated by EE. (b) Reflectance spectra of Si wafers with different length of Si NWs [114].

Ozdemir et.al. fabricated Si NWs based radial heterojunction solar cells using a complementry p-type polymer (PEDOT:PSS). Photovoltaic conversion and external quantum efficiency of radial heterojunction cells showed great enhancement in comparison with planar ones (Figure 4.10). The conversion efficiency enhancement lost by increasing the length of the Si NWs as observed in Figure 4.10 (c) [114].
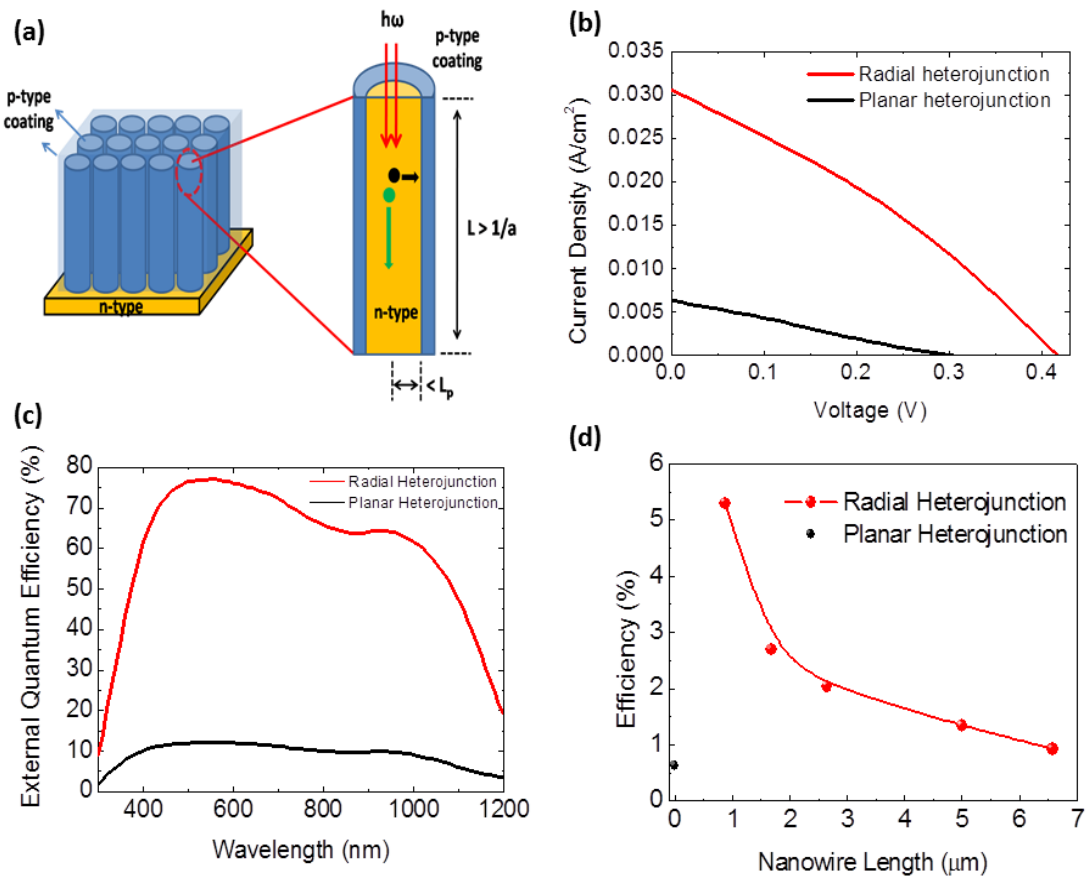
Figure 4.10 (a) Schematics of fabricated heterojunction solar cells, (b) current – voltage characteristics and (c) external quantum efficiency of radial and planar cells and (d) conversion efficiency changes versus the NW length [114].

Kulakci et al. produced NW arrays by the EE method and applied them to industrial-scale (156 mm × 156 mm) monocrystalline Si solar cells (Figures 4.11 (a)). It has been shown that Si NWs can be effectively used as a light-trapping layer. The efficiencies of solar cells with nanowires were similar to those of standard pyramid-textured cells, revealing the potential of the proposed concept. The photon conversion efficiency and EQE values decreased with an increase in the nanowire length due to the carrier recombination on the surface of the NWs (Figure 4.11(b) and (c)) [113].
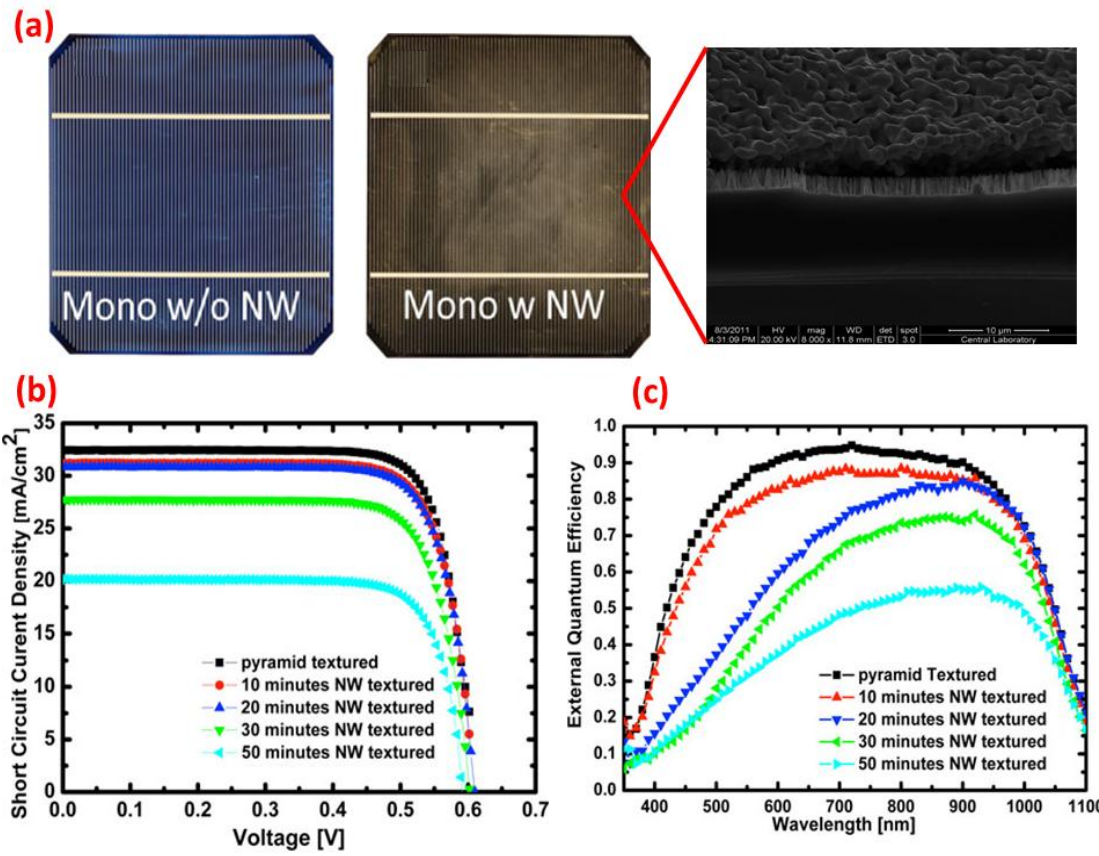
Figure 4.11 Application of Si NWs in industrial scale Si solar cells. (a) Photograph of the cells with and without Si NWs and SEM image of the NWs in contact with top electrode (b) I-V characteristics and (c) external quantum efficiency plot for the fabricated cells with different wire lengths [113].

In this chapter, we focused on making ultrathin Si wafers by KOH etching of Si wafers. Thicknesses arround 20-30 µm was obtaind through contolling the effect of solution concentration and temperature on the etching rate and roughness of the (100) Si wafers. Homojunction Si solar cells were fabricated from the obtained ultrathin Si wafers to show their applicability in photovoltaics. In order to improve the weak light absorption of these thin wafers, light trapping strategies such as the formation of Si NWs on the cell surface to increase absorption was investigated.

4.2 Experimental Details

4.2.1 Fabrication of Ultrathin Si

All chemicals were purchased from Merck and used without further purification. In order to obtain accurate results, pure KOH solution was preferred over a number of mixtures to etch Si. Chemical etching of Si depends on crystal orientation, temperature and concentration of the etchant.

Prior to etching process, Si wafers (single side polished (ssp), 500 µm thick, (100) orientation, p-type, resistivity 1–10 Ω.cm) were cleaned using RCA cleaning process and after native after oxide removal by 1:10 HF: DI, silicon nitride (SiN_x) was deposited over cleaned Si wafers, at 400 °C at a thickness of 0.16 µm using PECVD. SiN_x provides masking action in KOH solution at high temperatures. Square windows of 1.5×1.5 cm^2 size was delineated in SiN_x using photolithography. This masking action allows easy handling and processing of thin Si wafers.

4.2.1.1 Patterning SiN_x (UV Lithography)

In order to use Si_3N_4 as an etching mask during KOH etching of Si, lithography was used to open windows in Si_3N_4 which was deposited on polished side of the 4 inch single side polished (ssp) Si wafers via PECVD. Nitride coated top sides of the wafers were spin coated with photoresist S-1813 at 500 rpm for 5s and then 2000 rpm for 30 s and were soft baked at 115°C for 60 s. The thickness of the photoresist

was approximately 2 μm. Wafers were then loaded into the lithography system where they were exposed to the UV light for 5 seconds through a lithography mask with the desired pattern. After the UV exposure, the photoresist was developed with MF-319 developer solution for 40 s and rinsed and dried. Hard baking process was then carried out at 115°C for 3 minutes. Since a positive photoresist was used in this work, the photoresist area exposed to the UV light was removed, leaving behind the same pattern of the mask. The Si_3N_4 was etched away in a buffered oxide etchant (BOE), which was prepared by mixing 6 parts of 40% NH_4F and 1 part of 49% HF. BOE is a very selective etchant, meaning that it stops at Si without etching and attacking the photoresist. The etching rate was 700 A°/min. After Si was recognized clearly, wafers were rinsed with DI water. Last process was the removal of the remained photoresist layer over the wafers with acetone for a few seconds. Wafers were then rinsed and dried with N_2 gas to be ready to be etched in KOH solution. A photograph of the patterned wafer is provided in Figure 4.12.
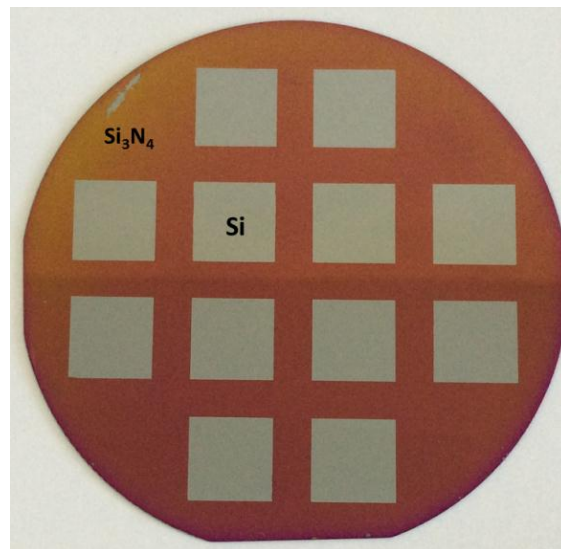
Figure 4.12 A photograph of Si_3N_4 deposited 4-inch Si wafer after window by lithography.

4.2.1.2 Potassium Hydroxide (KOH) Etching

The steps of sample preparation for wet etching are summarized in Figure 4.13. Wet etching was used to selectively remove Si.
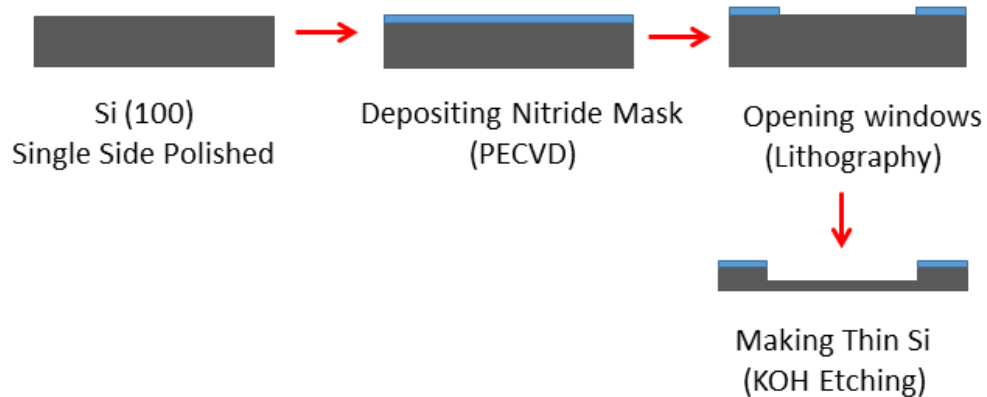
Figure 4.13 Schematics of thin Si fabrication via KOH etching using a SiN$_x$ mask.

Initially to investigate the effect of KOH solution concentration, different solutions with concentrations varying from 10% to 50% by weight were prepared to etch Si wafers. Process was conducted for 3 hours. To study the effect of temperature a solution concentration of 50 wt % was selected and Si wafers were etched at temperatures between 70 and 90°C. Quality and roughness and thickness of the etched surfaces were inspected using atomic force microscopy (AFM) and scanning electron microscopy (SEM). As a result of this study, 50 wt % KOH with an etching temperature of 90°C seemed to be the best condition to etch Si wafers. Figure 4.14 shows photographs of 20 μm thick Si wafer following KOH etching. The Si wafers begin to transmit light at thicknesses below 40 μm.
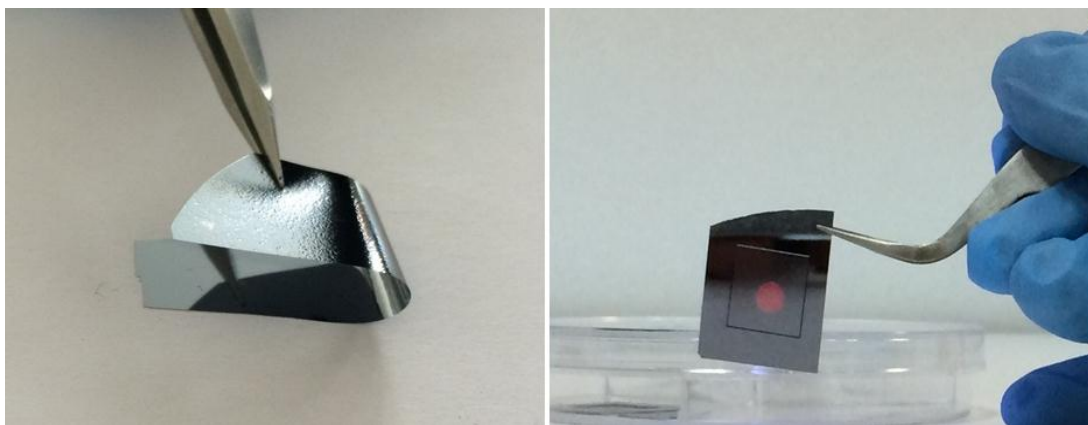
Figure 4.14 Photograph of ultrathin Si wafer with a thickness of 20 μm. Flexible Si bent with a tweezer (left) and laser light transmitted through thin Si wafer (right).

4.2.2 Fabrication of Silicon Nanowires

After etching wafers to the desired thicknesses (20-30 μm), the ultrathin wafers were immersed in boiling piranha solution (prepared by mixing sulfuric acid (H_2SO_4, 95%–97%) and hydrogen peroxide (H_2O_2, 35%) by a volume ratio of 3:1) for 20 minutes, to remove organic residues. RCA-2 solution was used to remove metal ions from wafers and for removing native oxide and Si nitride mask, diluted HF acid solution with concentration of 1:10 was applied. After DI water rinsing and N_2 gas drying, wafers were then prepared for nanowire fabrication process.

EE method was used to fabricate Si nanowires, as discussed before. Regarding this, EE solution was prepared by mixing HF (38%–40%) and $AgNO_3$ (99.5%) at a molar ratio of 4.6 M: 0.02 M. All etching procedures were carried out at room temperature and after achieving desired nanowire lengths, etching process was finalized by rinsing them with (DI) water. To remove by-products of EE (Ag dendrites), nitric acid (DI water 1:3 HNO_3 by vol. ratio) solution was used.

Morphologies of the nanowire samples were characterized through scanning electron microscopy (SEM, FEI Nova Nano SEM 430 microscope operated at 10 kV) and high-resolution transmission electron microscopy (HRTEM, JEOL TEM 2100 F microscope operated at 200 kV). Figure 4.15 (a) shows the photograph of etched wafers before (left) and after (right) the fabrication of Si NWs. The dark color of the

sample with Si NWs was obvious, which was due to enhancement of light absorption. Figure 4.15 (b) is the SEM image of the etched wafer with Si NWs. The thickness of the wafer was around 20 µm and length of the NWs were measured as 1µm, which was quiet enough to provide good light trapping effect and light absorption.
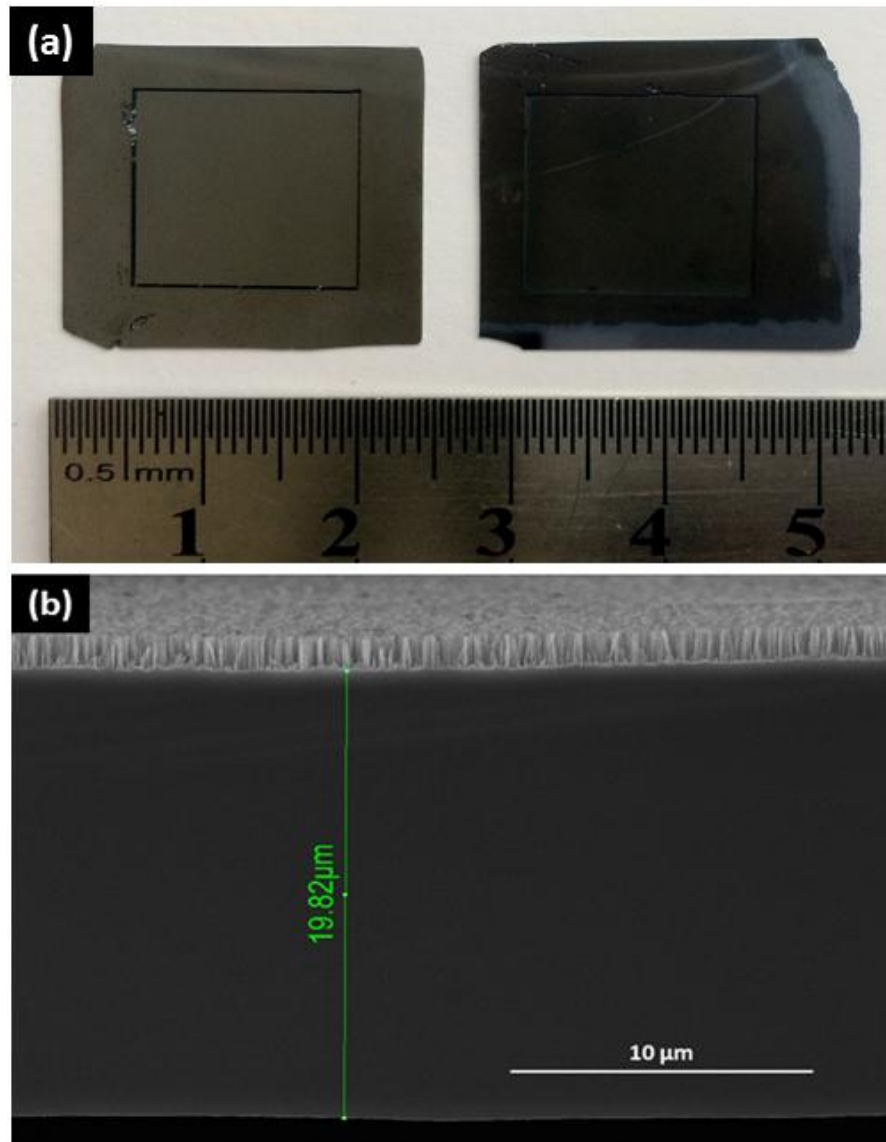
Figure 4.15 (a) Photographs of KOH etched Si wafers before (left) and after (right) the fabrication of Si NWs. (b) Cross sectional SEM image of a 20 µm thick Si wafer decorated with Si NWs.

The morphology of the fabricated Si NWs was evaluated through transmission electron microscope (TEM). To prepare TEM samples, Si nanowires were detached from the substrate by sonication in ethanol. Ethanolic solution was then drop casted onto lacey carbon coated copper grids and allowed to dry in air. The TEM images are provided in Figure 4.16 (a) and (b). Diameters of the NWs were around 60 nm and the surface of the NWs was found to be relatively smooth.
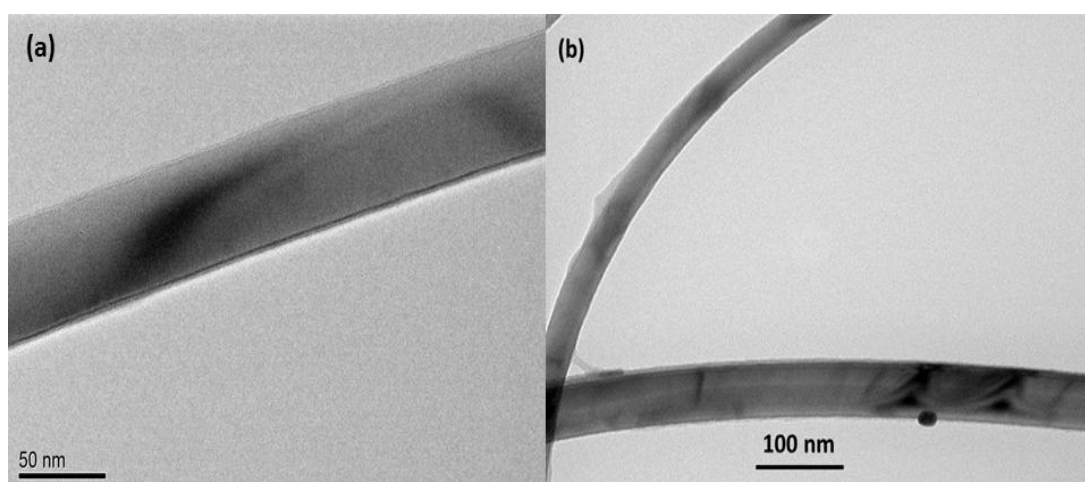
Figure 4.16 TEM images of Si NWs fabricated using EE method.

4.2.3 Fabrication of Solar Cells Using Nanowire Decorated Ultrathin Si Wafers

After Si NWs etching process, RCA cleaning and oxide removal processes were carried out again on wafers. Cleaned and oxide removed p- type wafers were then placed in diffusion furnace to be doped by $POCl_3$ to form p-n junctions. PSG formed on the surface top of Si NWs was removed as described in Chapter 1.

Metallization for the formation of ohmic front and rear contacts was conducted through thermal evaporation. 500 nm thick Al was evaporated as back contact on p-type side of the cells and annealed in N_2 ambient at 800 °C for 40 minutes. This formed back surface field (BSF) region in p-type Si.

Ag fingers with thickness of 500 nm were evaporated through a shadow mask as top contact in two ways. First, by evaporation of the metal contact on top of the Si NWs directly. In second way, metal was evaporated on the areas, which were protected by a photoresist during EE process from NWs etching. Regarding this and prior to EE process, thin wafers went through lithography to design a top contact pattern on them. Doping process and other fabrication steps were also carried respectively. Solar cell fabrication steps are shown in Figure 4.17.

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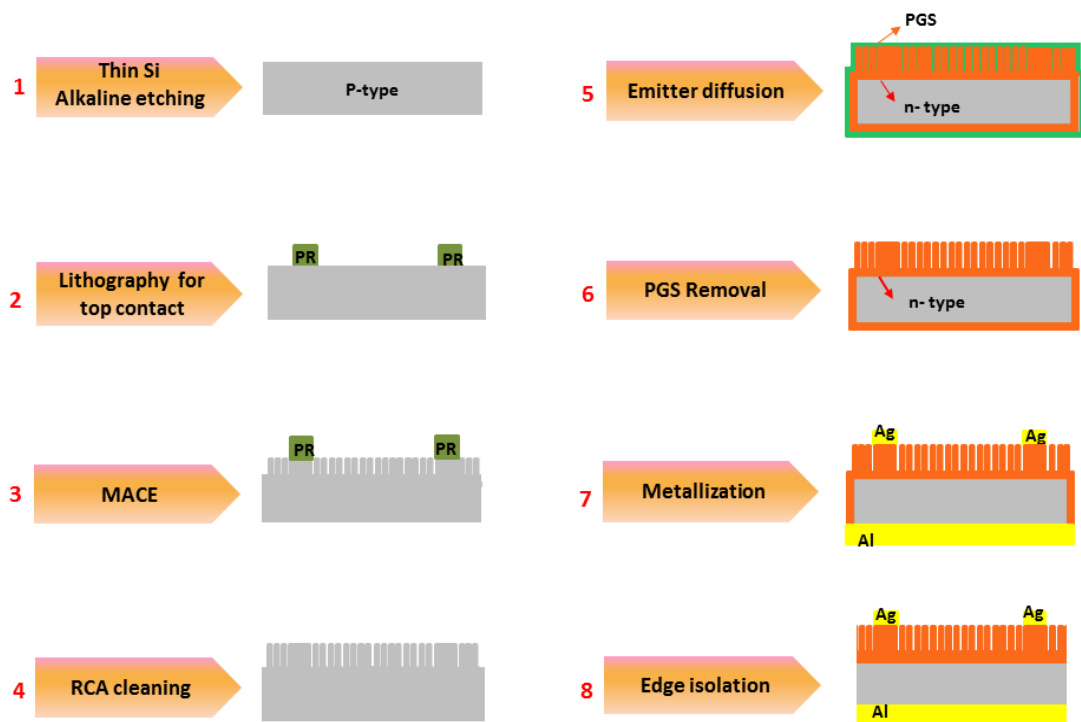
Figure 4.17 Schematics showing different steps of solar cell fabrication process.

4.3 Results and Discussion

4.3.1 Etching Rate and Roughness of the Ultrathin Si Wafers

The variation in etching rate and roughness of (100) Si with respect to solution concentration at a temperature of 80 °C, is shown in the graph provided in Figure 4.18. It is evident that the increased KOH concentration decreased the etching rate. The highest etching rate (78 µm/h) belongs to a sample that was etched in a 10 wt% KOH solution. The reaction of KOH etching in which both OH^- and H_2O participate in the reaction with Si is as follows:

$$Si + 2\,H_2O + 2\,OH^- \quad \rightarrow \quad Si\,(OH)_4 + H_2 \qquad\qquad (Eq.\ 4.4)$$
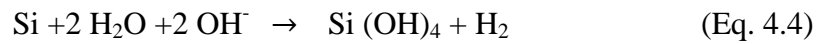
In lower concentrations OH^- is in low concentration but more H_2O is available that can be the reason for the low etching rate.
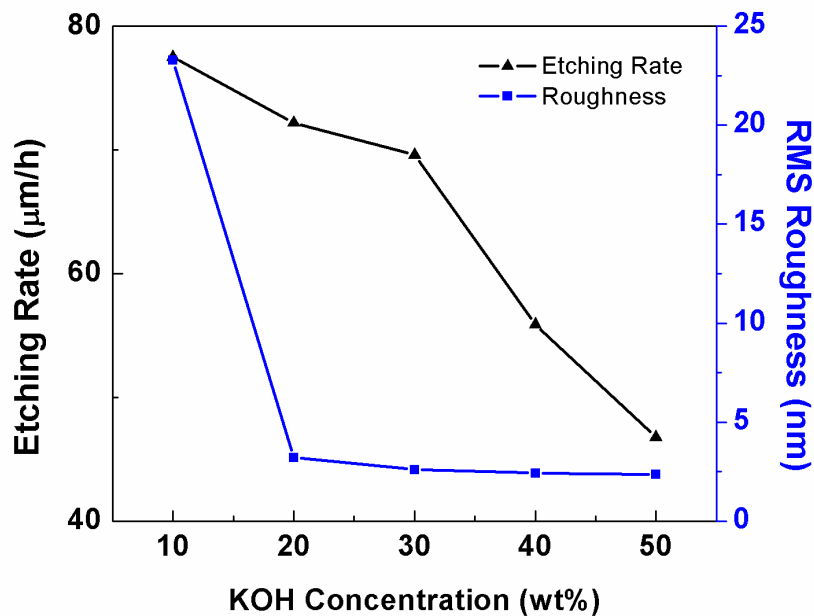
Figure 4.18 Etching rate and roughness variation of Si wafers versus KOH concentration at a constant temperature of 80°C. Lines are for visual aid.

During Si etching in KOH solution, H_2 bubbles are generated and to a large extent the quality of the etched surface depends on the rate at which these bubbles are removed from the etched Si surface. The formation of large hydrogen gas bubbles depends on the adhesion between the KOH solution and the Si wafer. If the surface is hydrophilic, only small bubbles are formed and roughness is reduced and if the surface is hydrophobic, large bubbles are formed and hence large hillocks are formed. Concentrated KOH solution tends to adhere more on Si surfaces, resulting in smaller bubbles and leads to lower roughness. These bubbles create temporary etch stops equivalent to etch masks. The minimum roughness observed for the sample etched in a solution of 50 wt% KOH at 80 °C was about 2.4 nm. The variation in roughness did not change much after the solution concentration was increased above 30 wt%. Figure 4.19 shows the variation of etching rate and roughness with respect to temperature while solution concentration was kept constant at 50 wt%. Within increase in temperature from 70 to 90 °C, etching rate increased. RMS roughness was found to increase with temperature (2.4 nm at 80°C) and then sharply decreased to 1.3 nm. Taking these into account, the most reasonable etching solution parameters to achieve both high etch rate and minimum roughness are 50 wt% KOH at a temperature of 90°C. These conditions resulted in an etching rate and roughness of 78.5 µm/h and 1.3 nm, respectively.
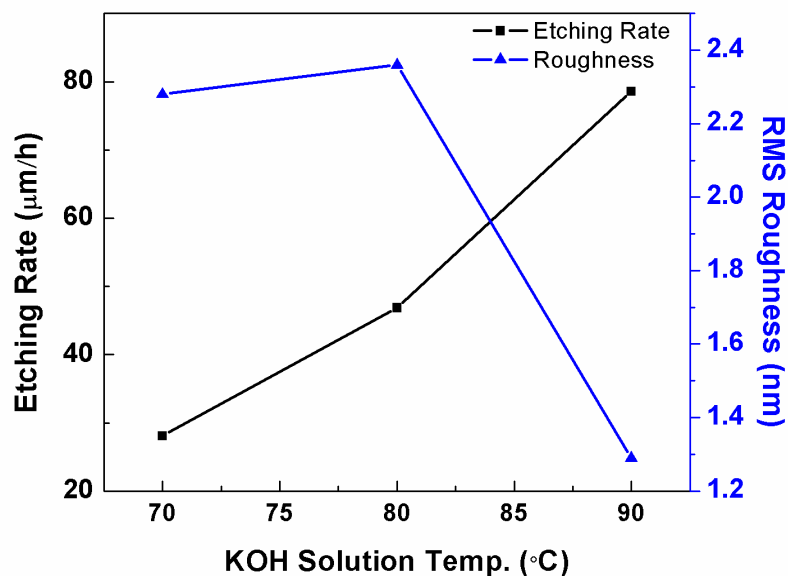
Figure 4.19 Etching rate and roughness variation of Si wafers with respect to temperature at a constant solution concentration of 50 wt%. Lines are for visual aid.

To measure the thickness of the etched wafers, scanning electron microscope (SEM) was used. The SEM images of ultrathin Si wafers etched at 90°C, from a 500 μm thick starting wafer using a solution concentration of 50 wt % KOH are provided in Figure 4.20 (a) - (c). It is clear from the SEM images that ultrathin Si wafers with thicknesses of less than 11 μm and smooth surfaces can be easily obtained using KOH etching.
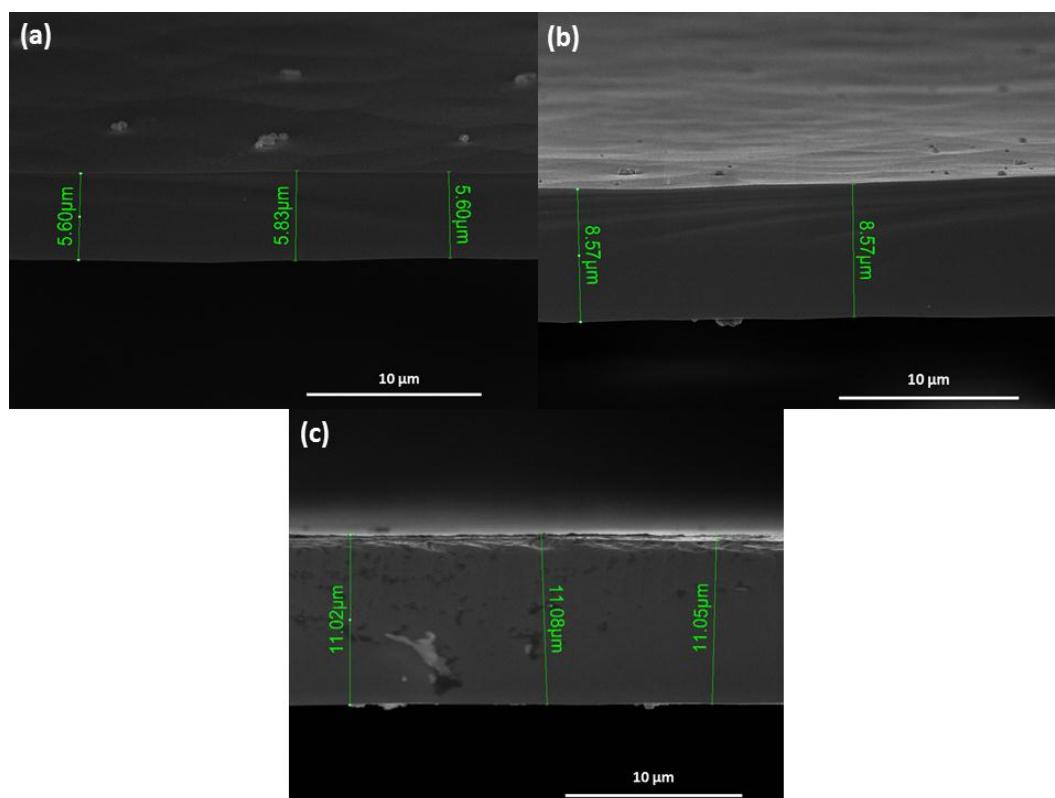
Figure 4.20 SEM images of ultrathin Si wafers etched using KOH solution with different etching durations which resulted in different thicknesses of (a) 5.8 μm, (b) 8.5 and (c) 11 μm.

Atomic force microscopy (AFM) technique was used to measure the roughness of the etched wafers. Figure 4.21 (a) and (b) shows the AFM images of Si wafers etched for 3 hours in a solution of 50 wt% KOH at temperatures of 80 and 90°C, respectively. A 1μm × 1μm area was scanned from 5 different points of the each sample and root mean square (RMS) roughness was measured for each point and averaged. Increase in the etching solution temperature from 80 to 90 °C resulted in a decrease in RMS roughness from 2.42 to 1.29 nm.

(a)
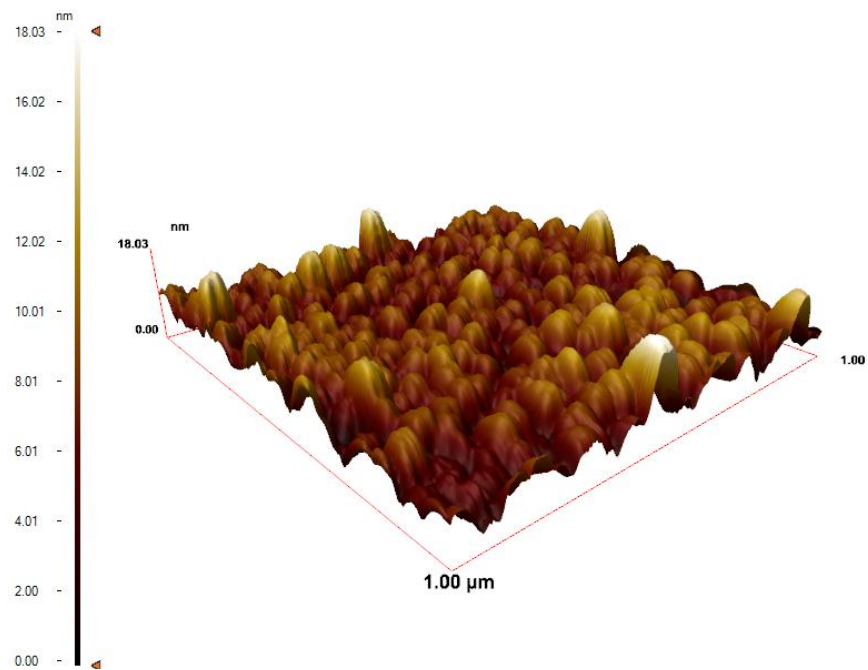
(b)
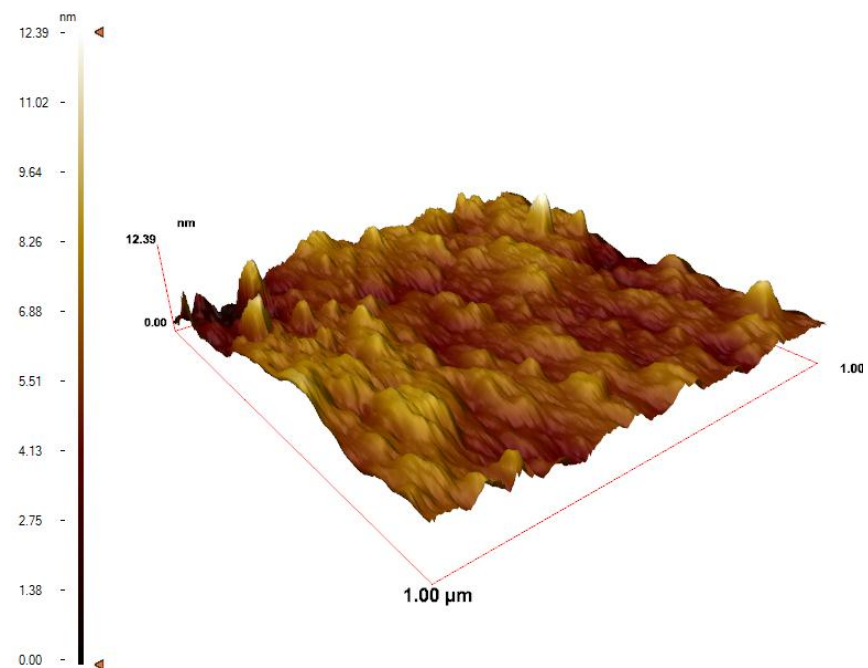
Figure 4.21 AFM images of Si wafers etched at a solution concentration of 50 wt% KOH at (a) 80 and (b) 90°C.

4.3.2 Ultrathin Si Solar Cells Characteristics

The photographs of the fabricated solar cells from thin Si wafers after edge isolation are provided in Figure 4.22. The area of the cell was 1 cm^2 and flexible nature of the cells is apparent within the Figure 4.22. The dark color of the cell was due to light trapping effect of Si NWs that are on top of the device.
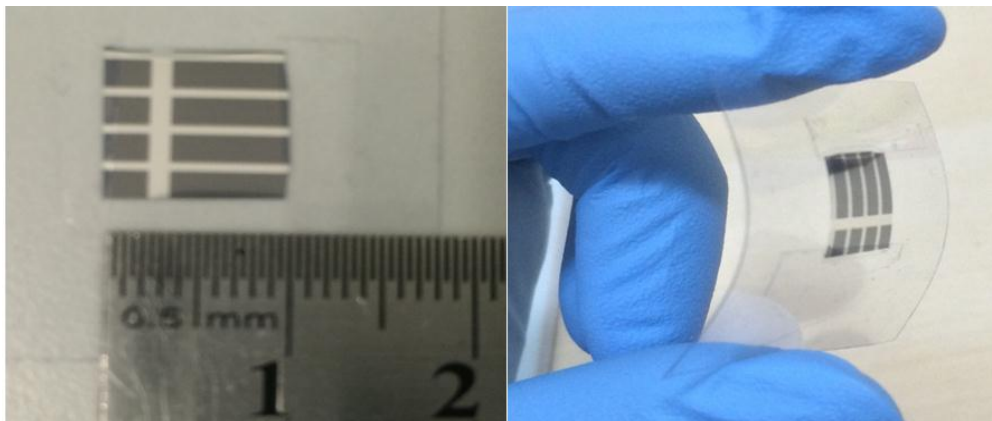
Figure 4.22 Photographs of fabricated ultrathin (left) and flexible (right) Si solar cells.

Figure 4.23 shows the SEM image of the fabricated solar cell. The thickness of the device was around 25 µm and NWs were 0.75 µm long. Top and rear contacts are also marked on the image. The inset shows the magnified image of the Si NWs. Slight etching in Si NWs were observed after PSG removal process due to oxidation in diffusion furnace which was inevitable.
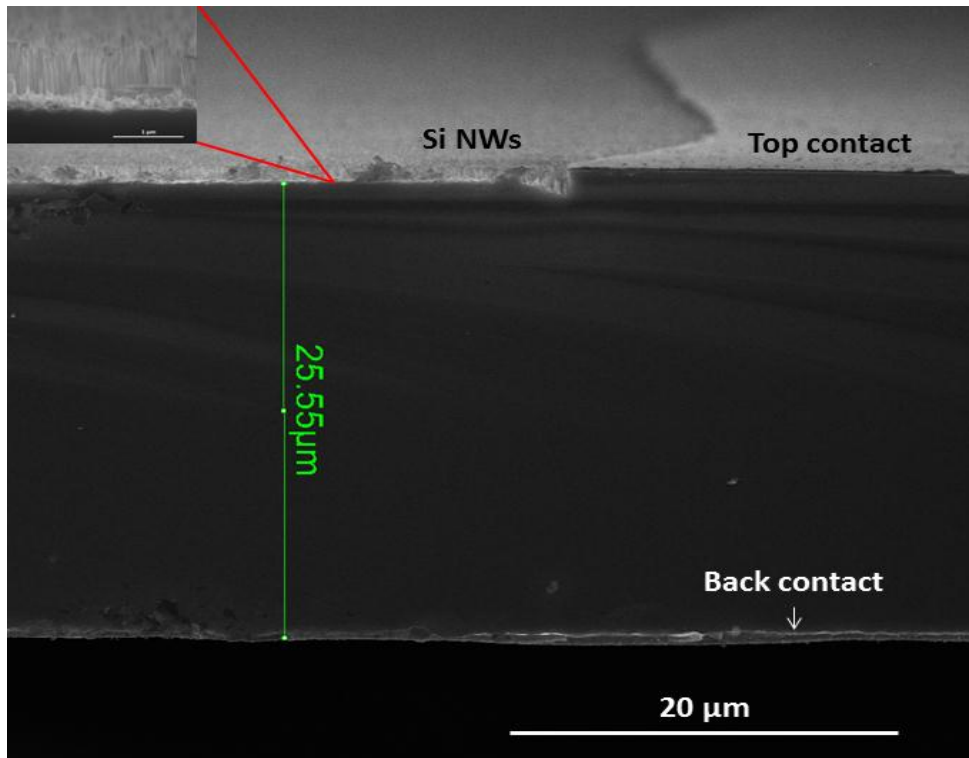
Figure 4.23 SEM image of fabricated ultrathin Si solar cell with Si NWs.

4.3.2.1 Optical Measurements

In this work, 25 μm thick Si wafers were used to fabricate solar cells. Reflectance and transmittance spectra of these Si wafers, with and without different length of Si NWs of different lengths are shown in Figure 4.24 (a) and (b), respectively. In Figure 4.24 (a) at a wavelength of 700 nm thin Si wafers begin to transmit light and in higher wavelengths the intensity of the transmitted light increases. However, by NW texturing and increasing the lengths of the NWs transmittance decreases when compared to the flat wafer. From Figure 4.24 (b), decrease in reflectance is observed for the thin Si wafers with NWs compared to the flat one. Increase in the NW length resulted in a further decrease in reflectance.
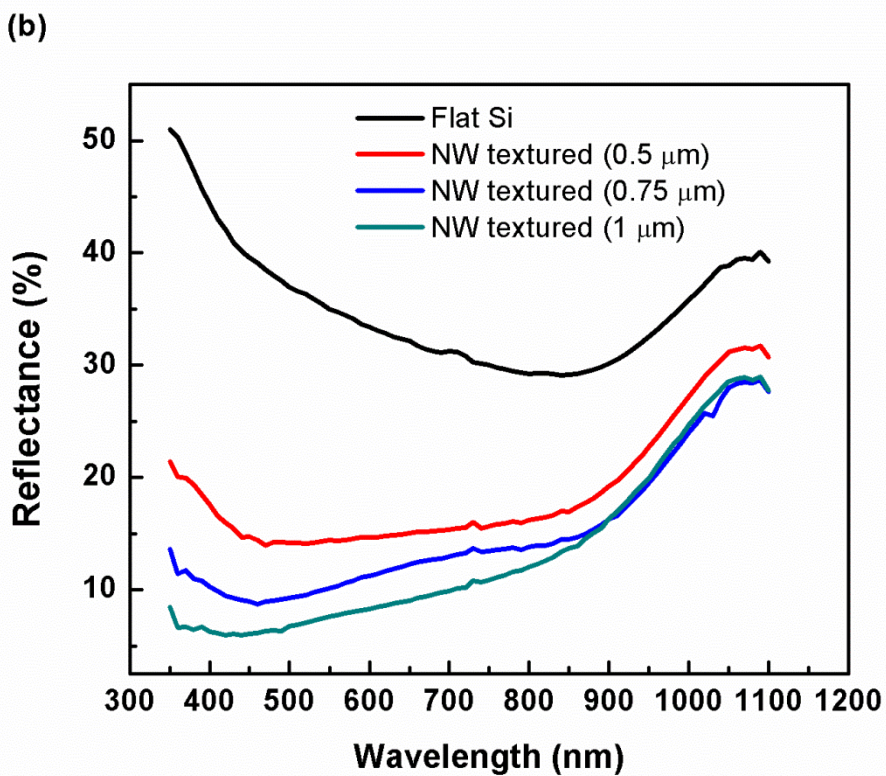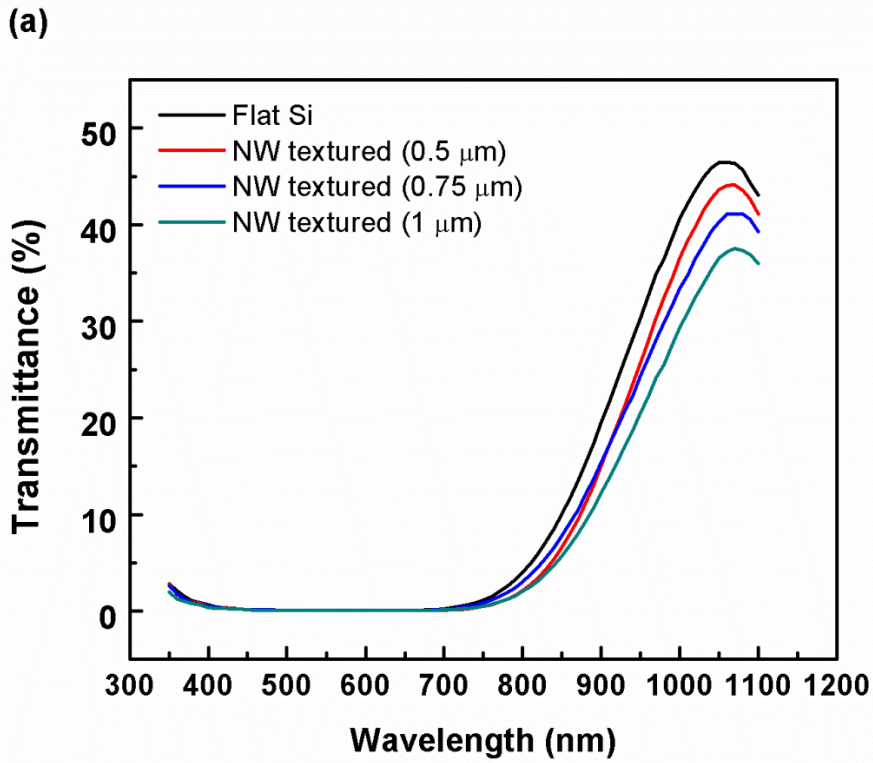
Figure 4.24 (a) Total transmittance and (b) reflectance spectra of 25 μm thick Si textured with different length of Si NWs.

For more clarification the average weighted reflectance (AWR) values of the wafers with different length of the NWs were calculated and shown in Figure 4.25. Through fabrication of Si NWs the AWR decreased from 34.6% for flat Si to 15.3 % for the wafer with 1 µm long Si NWs. This was attributed to the light trapping effect of the Si NWs, which increased light absorption in ultrathin wafers.
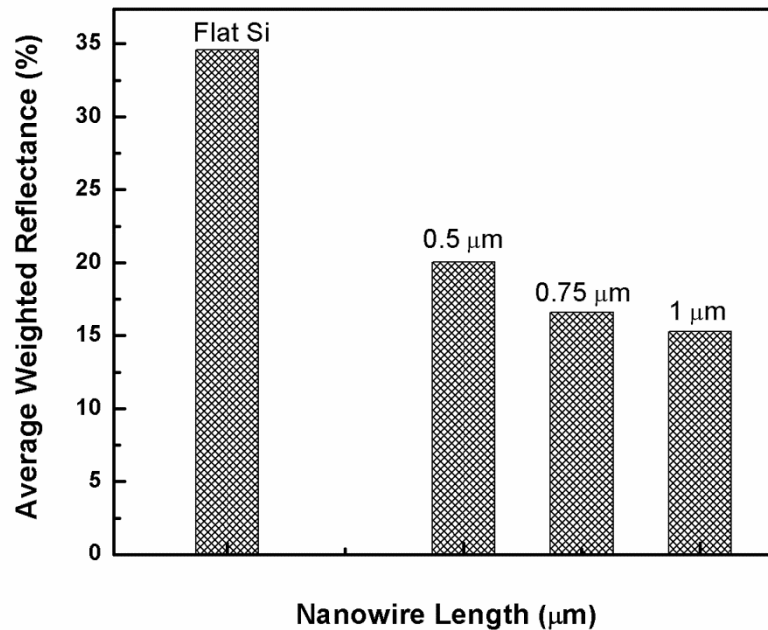
Figure 4.25 AWR values of 25 µm thick Si wafers with different length of Si NWs.

4.3.2.2 J-V Curves of the Ultrathin Si Solar Cells

Figure 4.26 shows J-V curves of flat and NW textured ultrathin Si solar cells with thickness of 30 µm in which thin film silver top contact was directly evaporated Si NWs. The length of the NWs was 2 µm and the cell area was 1 cm^2. Table 4.1 shows the photovoltaic parameters of these solar cells. Enhancement in J_{sc} was observed due to the higher light absorption and carrier generation; but, fill factor and conversion efficiency of the cells decreased due to high series resistance caused by the Si NWs and non-conformal coating of the top contact. Besides, annealing of the

top contact led to dewetting of the silver film on the walls of the Si NWs in these cells, as shown in Figure 4.27.
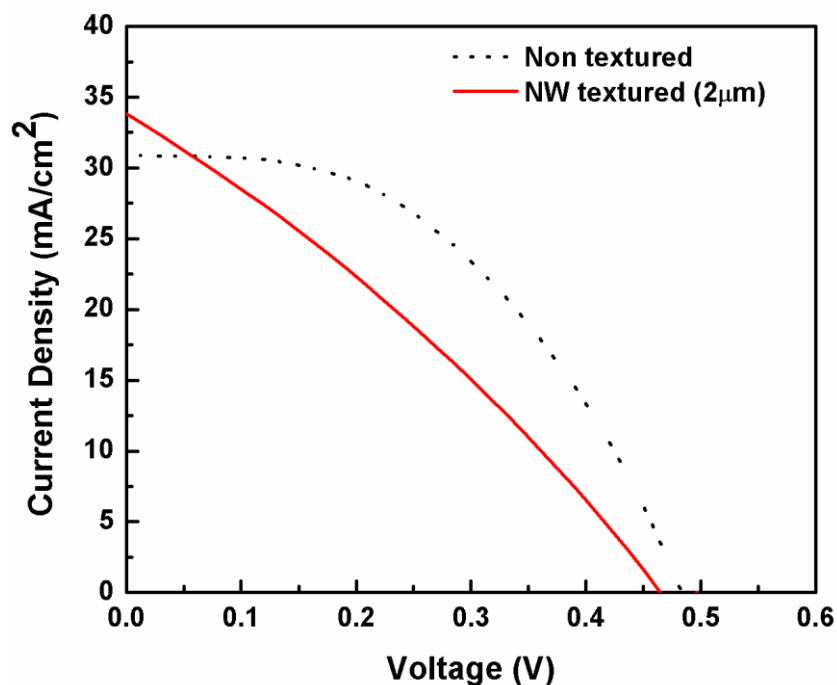
Figure 4.26 J-V curves of Si solar cells made from 30 μm thin Si with and without Si NWs. Top contact was deposited through evaporation on top of Si NWs.

Table 4.1 Photovoltaic parameters of ultrathin Si solar cells with and without Si NWs.

Sample	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)	R_s	R_{sh}
Non textured	0.48	30.8	47.1	7	15.2	1933
NW textured	0.47	34.3	30	4.85	26.3	53.8
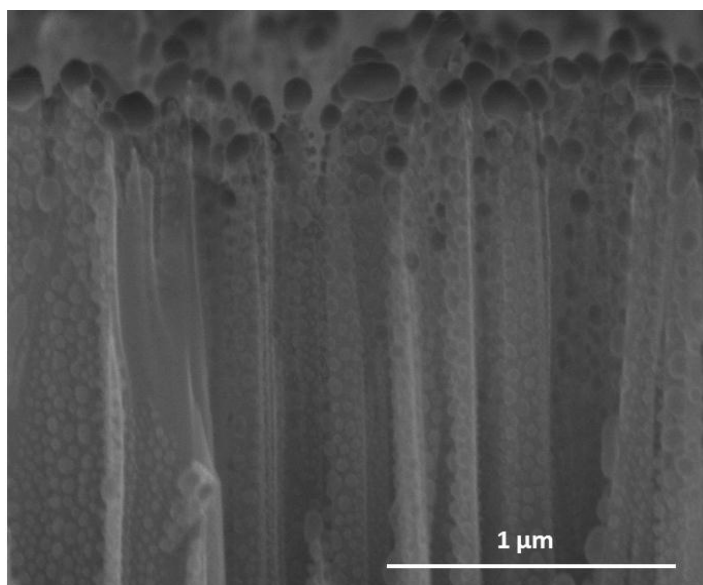
Figure 4.27 SEM image showing the dewetting of the top Ag contact due to annealing.

4.3.2.3 EQE Measurements

Figure 4.28 shows the EQE plot of the fabricating cells. That of a standard 180 µm thick Si solar cell is also provided for comparison. Decrease in the thickness of the cells resulted in decrease in the EQE. This reduction is more obvious in the infrared region of the spectrum due to higher transmittance of the cells in this region (Fig. 4.24 (a)). Thin solar cell with NW texturing had better spectral response compared to the thin flat cell in infrared region. This was attributed to the light trapping ability of NWs in textured sample which resulted in better carrier generation. However, EQE of the cell with NWs showed a decrease within blue region. This is because the blue part of the solar radiation has shorter absorption depth and the generated carriers in upper parts of the Si NWs have to travel alongside the NWs to reach the electrode and this increases the recombination probability of the carriers.
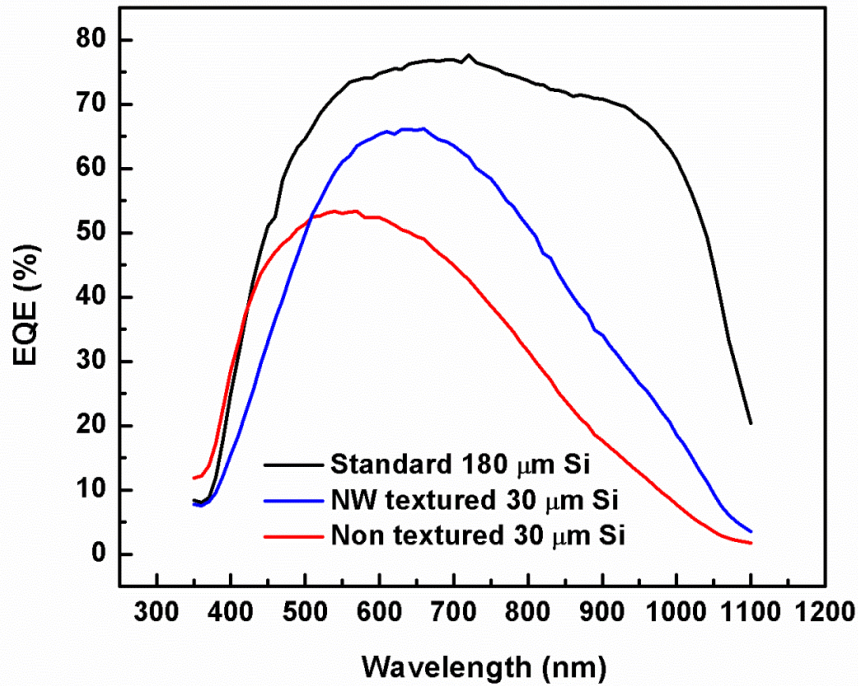
Figure 4.28 EQE plots for ultrathin Si solar cells with and without Si NWs in comparison with standard solar cell (180 μm).

4.3.2.4 J-V Curves of the Ultrathin Si Solar Cells Following Top Contact Optimization

In order to optimize the top contact design, photolithography is carried out to pattern Si NWs so that the top contact areas are protected from NW etching during EE process. The resulting J-V curves obtained from 25 μm thick Si wafers with different length of NWs are shown in Figure 4.29. The obtained photovoltaic parameters are tabulated and provided in Table 4.2. Fabrication of NWs on ultrathin Si cells resulted in an increase in J_{sc} from 19.4 to 26.5 mA/cm^2. The 36.6% relative enhancement in J_{sc} is attributed to an increase in the number of the generated carriers as a result of light trapping effect and higher absorption. The photovoltaic conversion efficiency (η) is increased from 5.8 to 6.7% when the length of the NWs are increased to 0.5 μm and reached its maximum value of 8.8% for the cell with the NW length of 0.75 μm. Therefore, a relative enhancement of 51% (from 5.8 to 8.8 %) in η is obtained

through the fabrication of NWs. Further increase in the length of NWs to 1 μm caused J_{sc} and accordingly η to decrease. This is because the carriers generated at the top parts of the NWs have to travel through the whole NW length to reach the electrode, which increases the series resistance.
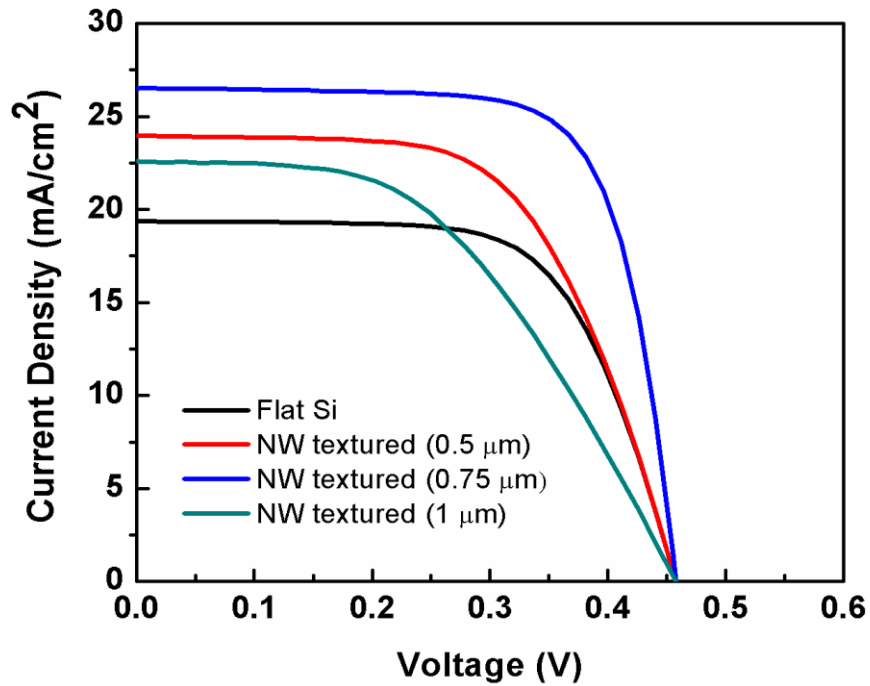
Figure 4.29 J-V curves of the 25 μm ultrathin Si solar cells decorated with different lengths of the Si NWs after top contact optimization.

Table 4.2 Photovoltaic parameters of ultrathin Si solar cells with different lengths of Si NWs following top contact optimization.

Sample	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)	R_s	R_{sh}
Flat	0.46	19.37	65.7	5.82	44.3	24855
0.5 μm NW	0.46	23.93	60.61	6.70	33.5	19874
0.75 μm NW	0.46	26.49	72.68	8.83	26.3	44700
1 μm NW	0.44	22.56	48.03	4.81	67.8	7789

4.3.2.5 EQE Measurements Following Top Contact Optimization

Figure 4.30 shows EQE plots of the cells following the top contact optimization. In all thin cells, EQE showed a decrease for the wavelengths above 700 nm. This is in compromise with transmittance spectra, which showed enhancement in this wavelength range resulting in lower light absorption and carrier generation. In the cells with 0.5 and 0.75 μm long Si NWs, EQE increased significantly throughout the investigated wavelength range compared to the flat cell. This is due to higher carrier generation as a result of light trapping effect. The cell with 0.75 μm long NWs had the highest response, which is in agreement with the conversion efficiency values. For the cell with the highest length of NWs (1 μm), EQE dropped, which means that the carriers generated due to the increase in light absorption have been lost as a result high series resistance in conjunction with increased recombination rate along the NWs. In NW cells, because the top contact was not directly deposited on the top of the Si NWs, the carriers generated close to the surface of the cell (as a result of blue light absorption) do not need to travel through the NWs to reach the electrode. Therefore, no reduction in EQE was observed in the blue region of the spectrum.
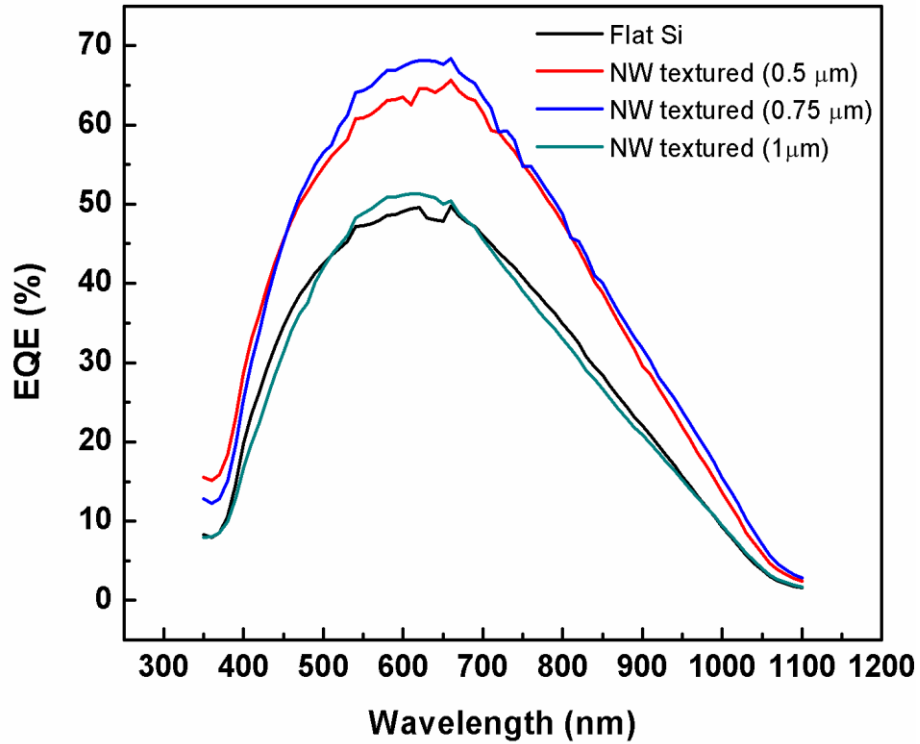
Figure 4.30 EQE plots for 25 μm thick Si solar cells with different lengths of Si NWs following top contact optimization.

4.4 Conclusions

In conclusion, ultrathin Si wafers were fabricated using optimized KOH etching starting with a 500 μm thick Si wafer. EE process was applied for NW texturization of the ultrathin Si wafers. For the first time, NW decorated ultrathin (25 μm) Si wafers were used to fabricate homojunction Si solar cells. A relative improvement of almost 56% in reflectivity was obtained for the thin Si wafer with 1 μm long Si NWs due to light trapping effect of the NWs. The problem of efficiency reduction of the cells with NWs was solved through the optimization of the top contact using photolithography. As a result a relative enhancement in the conversion efficiency of more than 51% was obtained. EQE reduction within blue region of the spectrum (an inevitable problem in NW cells) was overcome by decreasing the electron transport pathways towards the contacts.

CHAPTER 5

CONCLUSIONS AND FUTURE RECOMMENDATIONS

This thesis consists of a detailed parametric study on the synthesis of low cost one-dimensional nanostructures and their applications as different components in single crystalline Si solar cells. The aim is to increase photovoltaic conversion efficiency benefiting from nanostructures characteristics and eventually to decrease cell manufacturing cost.

Regarding this in Chapter 2, vertically aligned ZnO nanorods were synthesized via hydrothermal method and utilized as the ARC of Si solar cells. The obtained results revealed that ZnO nanorods can be effectively used as a light-trapping layer instead of conventional Si_3N_4 ARC layer. An absolute enhancement of 2% in the efficiency of ZnO nanorod cells was obtained and attributed to both the passivation and ARC properties of ZnO nanorods. Hydrothermal method is a simple process and ZnO nanorods can be utilized as ARCs on various other types of photovoltaic devices.

Chapter 3 is on the use of Ag NW networks as transparent top electrodes in single crystalline Si solar cells. Ag NWs were synthesized via polyol method and spray coated in the form of a network on top of the Si solar cells. Three different network densities were investigated. High temperature annealing was performed to form ohmic contact between NWs and n-type Si and a relative enhancement of 31 % in efficiency was observed following annealing the cells at 400 °C for 1 min. High temperature annealing resulted in partial rupture and isolation of the Ag NWs and limited the efficiency enhancement. However, isolated NWs still provided low resistance routes for the electrons at local spots. The highest η observed for the sample with the lowest resistance of 5 ± 1 Ω/□ and relative improvement of 21%

(from 4.75% to 5.73%) in conversion efficiency was obtained for this cell compared to reference cell without NW on top.

Despite of optical losses due to the reflectivity of the Ag NWs, a slight increase in EQE was observed for the cell with lowest NW resistance as a result of high charge collection probability. Therefore, the applicability of the Ag NWs as top contact in crystal Si solar cells was shown in this chapter. As a future work, plasmonic effects of Ag NWs in Si solar cells can be investigated in detail. In addition, other NWs that are metallic such as copper NWs can be also utilized as top electrodes in the Si solar cells.

In Chapter 4, ultrathin Si wafers were fabricated by KOH etching and utilized as the active layer in homojunction Si solar cells. In order to compensate the poor light absorption of ultrathin Si wafers, Si NWs were fabricated using EE method on the thin Si wafers. Solar cells with 25 μm thick Si wafers and different lengths of NWs (0.5, 0.75 and 1 μm) were fabricated. A relative improvement of almost 56% in the reflectivity was obtained for the thin Si wafer using 1 μm long Si NWs. The problem of efficiency reduction of the cells with NWs was solved through the optimization of the top contact using photolithography. A relative enhancement of 51% (from 5.82 to 8.83%) in conversion efficiency was observed due to the light trapping effect of the Si NWs. Following the top contact optimization, decrease in the EQE within the blue region of the spectrum, which is an inevitable problem in NW cells was solved by decreasing the electron transport pathway towards the electrode. NW enhanced ultrathin Si wafers can be also be used in heterojunction or hybrid solar cells. As complementary materials, polymers or amorphous Si thin films can be investigated.

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MS	Iran Science and Technology, Tehran, Iran
Solid State Physics	
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FOREIGN LANGUAGES

Advanced English, Turkish and Persian

AREAS OF EXPERTISE

Synthesis of ZnO nanorods (hydrothermal method), Synthesis of Si nanowires (EE method), Synthesis of CNT thin films (filtration technique), Synthesis of vertically aligned CNTs (PECVD technique), Patterning of nanostructures (UV lithography, phase shift lithography, e-beam lithography), Fabrication and characterization of crystal Si solar cells, Fabrication of ultrathin Si wafers (KOH etching), Light trapping in crystal Si solar cells, Li-ion Batteries, Application of Si nanowires as anode in Li-ion batteries, AFM (atomic force microscopy), SEM (scanning electron microscopy), XRD (X-ray diffraction spectroscopy).

PUBLICATIONS IN JOURNALS

- **P. Aurang,** O. Demircioglu, F. Es, R. Turan and H. E. Unalan, "ZnO Nanorods as Antireflective Coatings for Industrial-Scale Single-Crystalline Silicon Solar Cells", Journal of American Ceramic Society, Vol. 96(4), 1253–1257 (2013).
- **P. Aurang**, D. Doganay, F. Es, R. Turan and H. E. Unalan, "Silver nanowires as transparent top contacts in crystal Si solar cells", (In preparation).

- **P. Aurang**, F. Es, R. Turan, H. E. Unalan "Nanowire Decorated Ultrathin Silicon Solar Cells", (In preparation).

INTERNATIONAL CONFERENCES

- Nanowire Decorated Ultrathin Silicon Solar Cells, **P. Aurang**, F. Es, R. Turan, H. E. Unalan, MRS Fall' 2015 USA.

- Nanowire Decorated Ultrathin Single-Crystalline Silicon for Photovoltaic Devices, **P. Aurang**, W. Hadibrata, S. Yerci, R. Turan, H. E. Unalan, MRS Spring' 2015 USA.

- ZnO Nanorods as Antireflective Coatings for Single Crystalline Silicon Solar Cells, **P. Aurang**, O. Demircioglu, F. Es, R. Turan, H.E. Unalan, TMS Meeting' 2014 USA.

- ZnO Nanorods as Antireflective Coatings for Industrial Scale Single Crystalline Silicon Solar Cells, **P. Aurang**, O. Demircioglu, F. Es, R. Turan, H.E. Unalan, MRS Fall' 2013 USA.

- Nanoscale Length Dependent Photoinduced Electron Transfer Mechanism Between Silicon Nanowires and Coumarin Dye Molecules, S. Açıkgöz, **P. Aurang**, S. Sönmezoğlu, H. E. Ünalan, R. Turan, Third Turkish Solar Electricity Conference and Exhibition, SolarTR-3, 27-29 April 2015, Ankara-Turkey.

- Silver Nanowires as Transparent Top Contacts in Crystal Si Solar Cells, **P.Aurang,** S. Coskun, F. Es, R. Turan, H. E. Unalan, Third Turkish Solar Electricity Conference and Exhibition, SolarTR-3, 27-29 April 2015, Ankara-Turkey.