DESIGN OF COMBINED POWER AMPLIFIER USING 0.35MICRON SiGe HBT TECHNOLOGY FOR IEEE 802.11a STANDARD

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Abstract

In this thesis, a 5GHz Radio Frequency (RF) Power Amplifier (PA) design approach will be specified for IEEE 802.11a Wireless Local Area Network (WLAN) standard, and performance of Class-A PA will be specified in terms of power gain, Power Added Efficiency (PAE), linearity, gain, and output power. The amplifier design is based on AustriaMicroSystems (AMS) 0.35um SiGe BiCMOS HBT technology which has an ft of 100 GHz. IEEE 802.11a standard specifies the maximum power that can be transmitted in the Unlicensed National Information Infrastructure (UNII) band. These specifications are also the output power of the amplifier for frequency band of 5.18-5.8 GHz and specified as follows: 40mW (5.18-5.24GHz), 200mW (5.26-5.32GHz) and 800mW (5.74-5.8GHz). The power amplifier is designed to operate in Class A to achieve high linearity and the bias points are chosen accordingly in order to preserve linearity. After the design of a single stage power amplifier, to reach higher output power and improve linearity, Wilkinson power combining technique is used in a new design. The behaviours of two kinds of circuits are compared and layouts are drawn. All the simulations are performed in Agilent Design System (ADS) and Cadence environments.

0.35MIKRON SiGe HBT TEKNOLOJİSİ İLE IEEE 802.11a STANDARDI İÇİN BİRLEŞTİRİLMİŞ GÜÇ KUVVETLENDİRİCİSİ TASARIMI

Nilüfer TONGA KARAKAŞ

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Özet

Bu tez çalışmasında, IEEE 802.11a Kablosuz Yerel Ağ standardına uygun 5GHz Radyo Frekansı (RF) güç kuvvetlendiricisi tasarımı yapılmış ve A sınıfı güç kuvvetlendiricisinin güç kazancı, verim, lineerlik, kazanç, çıkış gücü bakımından performansı ölçülmüştür. Kuvvetlendirici tasarımı, 100GHz ft'ye sahip AustriaMicroSystems (AMS) 0.35um SiGe BiCMOS HBT teknolojisi kullanılarak yapılmıştır. IEEE 802.11a standardı, UNII bandında iletilebilecek en yüksek çıkış gücünü tanımlamaktadır. Bu tanıma aynı zamanda 5.18-5.8GHz frekans bandındaki kuvvetlendiricinin çıkış gücü de girer ve şu şekilde tanımlanır: 40mW (5.18-5.24GHz), 200mW (5.26-5.32GHz) ve 800mW (5.74-5.8GHz). Güç kuvvetlendiricisi yüksek lineerliğe ulaşmak için A sınıfında çalışacak şekilde tasarlanmıştır ve besleme gerilimleri buna gore seçilmiştir. Tek katlı güç kuvvetlendiricisi tasarımından sonra, daha yüksek çıkış gücü elde etmek ve lineerliği arttırmak için Wilkinson güç birleştirme tekniği kullanılmıştır. İki tip devrenin davranışları karşılaştırılmış ve serimi yapılmıştır. Tüm simülasyonlar Agilent Design System (ADS) ve Cadence simülatörleri kullanılarak yapılmıştır.

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Chapter 1

1 INTRODUCTION

The last few years has seen a remarkable amount of growth in the personal and wireless communications areas, and as a result, the demand for optimizing the circuits involved in wireless communications devices has increased dramatically [1]. Not only has the demand for the circuits increased dramatically, but the amount of research done in this field has surged as well. Since in a portable wireless environment all circuits are drawing power from a small battery, it seems clear that one of the most important aspects of the circuits that need to be optimized is the power consumption. Additionally, since these devices must be used in a low cost product, the cost of the circuits must be lowered as well.

There are some standards defined to make the systems compatible for wireless communications. IEEE 802.11 standard is one of them. Its operating frequency band is 5GHz instead of 2.4GHz which increases data transmission rate. In this thesis, 802.11a standard is chosen and the requirements are fixed according to its definitions. IEEE 802.11a Wireless Local Area Network (WLAN) is being used very commonly because of high speed and low interference. The important parameter for power amplifier is the transmitter's output power level. In IEEE 802.11a, the output power levels are defined according to the band. 40mW, 200mW, and 800mW are defined for the frequency bands 5.15-5.25GHz, 5.25-5.35GHz, and 5.725-5.825GHz respectively [2].

There are many power amplifier implementation techniques for a transceiver. In a Monolithic Microwave Integrated Circuit (MMIC), high efficient power amplifiers such as Class E, F, or S can be preferred [3]. But in this thesis, it is decided that the linearity is

more important and hence Class A power amplifier is designed. This class of operation also gives higher output power by implementing power combining technique which will be examined in following chapters.

Although GaAs and InP technologies are commonly used in integrated power amplifiers, SiGe technology also finds a wide implementation area for WLAN [4]. Devices in SiGe BiCMOS technology can operate at 5GHz. There is one problem about output power of a single-stage amplifier because of low collector-emitter breakdown voltage. In this study, this problem is eliminated by using multiple transistors and power combining technique. It can be said that SiGe technology is easy to implement rather than III-V compound semiconductor technologies. Also it has a cost advantage while implementing. As a result, it is decided to design the amplifier with SiGe technology because of these several advantages.

In this thesis, a power amplifier is designed using integrated power combining technique. In general, power combining is implemented by transmission lines. As explained above, the amplifier is designed according to IEEE 802.11a standard. The operating frequency is the lower frequency band of this standard which defines 40mW (16dBm) output power. Austria Micro Systems (AMS) SiGe BiCMOS technology is used in the design. All the simulations are performed in Agilent Advanced Design System (ADS®) and Cadence® environment. First of all, the operating bias values are found for a single-stage Class-A power amplifier. Then, load pull and source pull analyses are done and desired input and output impedances are found. Matching circuits are created according to these analyses and final performance of a single-stage amplifier is obtained. To reach higher output powers, power combining technique is implemented and performance is measured. The ideal and real models of passive components are compared in this amplifier. Finally, layout is created according to final design and post-layout simulations are done. All simulation results are compared as a conclusion.

In Chapter 2, general information about the power amplifier design theory is given. Architecture of an RF system is explained shortly. Then, some basic characteristics of a

power amplifier is explained and defined. Bias networks and linear classes of power amplifier are introduced in this chapter. These linear classes are A, B, AB, and C operating classes for power amplifier. In Chapter 3, power amplifier is designed. The improvement of a power amplifier can be seen in this chapter. Firstly, single-stage power amplifier is designed and simulated with ideal components in Cadence. By changing these ideal components with the real models, the real behaviour of this circuit is obtained. In the same chapter, Wilkinson power combining technique is also explained. Using the designed single-stage amplifier, two PA stages are combined and simulated. Again two different behaviours are obtained with ideal and real models of passive components. As a last stage, the layout of the combined power amplifier is created in Cadence environment. The simulations are repeated with this layout and the most realistic behaviour of the circuit is derived. Chapter 4 is the conclution chapter. While there are many simulations run for different power amplifier designs, they are compared with each other.

Chapter 2

2 RF POWER AMPLIFIER THEORY

In this chapter, basic background and some definitions are mentioned for power amplifier. Firstly, general transceiver architecture and the role of power amplifier are explained. Then, main characteristics of an amplifier such as power output capability, power added efficiency, total harmonic distortion are defined. Also basic linear power amplifier classes are mentioned shortly. These definitions will make the thesis clearer.

2.1 Architecture of an RF System

The basic structure of an RF transceiver system for personal communications is shown in Figure 2.1. Figure 2.2 and 2.3 represent the transmitter and receiver sides of this system respectively. As shown in Figure 2.2, on the transmitter side of the system, the basic operations are as follows. The digital data is first encoded, and then the independent I and Q channels of data are combined by some form of quadrature modulator, and the resulting combination is mixed up to the RF carrier frequency (or the two steps might be combined into one block). Then, after some filtering, the signal drives the power amplifier, which drives the antenna. The antenna radiates the signal into the air, and the transmission is completed.

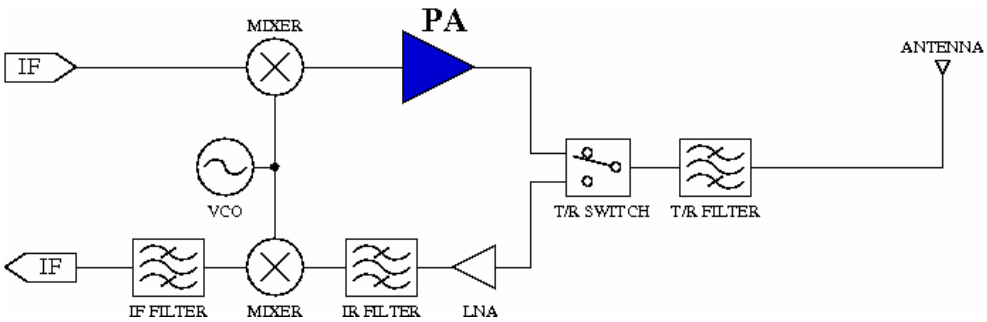


Figure 2.1 Basic RF Transceiver System

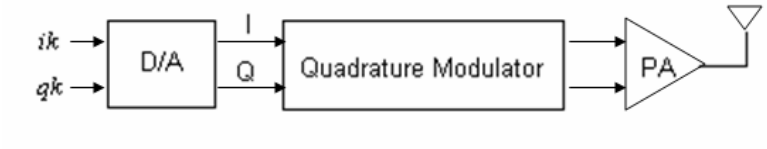


Figure 2.2 Common Transmitter Architecture

Figure 2.3 Common Receiver Architecture

The receiver side is simply the inverse (Figure 2.3) and slightly different components must be used. The signal received by the antenna is filtered to select the RF band of interest, after which it is fed into a Low Noise Amplifier (LNA). The signal is then usually filtered, and either mixed directly down to baseband, in the case of a direct conversion or homodyne receiver, or mixed to one or more intermediate frequencies (IF), in the case of a heterodyne or super-heterodyne frequency. Often the last mixing stage will separate the signal into its I and Q components. Once at baseband, the signal will be converted to digital and then processed.

2.2 Power Amplifier Basics

The RF power amplifier (PA), which is a critical element in a transmitter system, is expected to provide a suitable output power at a very good gain with high efficiency and linearity. The output power of a PA must be sufficient to get a reliable transmission. High gain reduces the number of amplifier stages required to deliver the desired output power and hence reduces the size and manufacturing cost. In another side, thermal management, battery lifetime and operational costs are improved by high efficiency. Also, good linearity is necessary for bandwidth efficient modulation [7]. All these requirements make a trade-off and an optimization is needed for a typical power amplifier design. Power amplifiers show variation in terms of linearity, output power or efficiency. Some parameters are important to quantify an amplifier's performance. These can be listed as power gain, power output capability, power added efficiency (PAE), 1-dB compression point, intermodulation distortion (IMD), Adjacent Channel Power Ratio (ACPR), and intercept point. All these characteristics are discussed in this chapter.

2.2.1 Gain

An amplifier's gain can be described as voltage gain, current gain, or power gain. The power amplifier is generally defined as its power gain. If magnitude of the output signal is shown as X_o and input signal is shown as X_i, the gain will be their ratio as shown below.

$$G = \frac{X_o}{X_i} \qquad (2.1)$$

2.2.2 Power Output Capability (Cp)

One of the most important characteristics of power amplifier is output power. The output capability factor is defined as the output power produced by 1V and 1A on the collector of a transistor. After the real voltage and current values of the collector are obtained, the multiplication of these values gives the maximum output power of the amplifier.

Different than the maximum output power, the power output capability (C_p) is the RF output power with peak drain voltage of 1V and peak drain current of 1A [5]. This quantity is unitless and defined with the below equation. Po is the RF output power, $I_{d,pk}$ is the peak drain current, $V_{d,pk}$ is the peak drain voltage and N is the number of transistors.

$$C_p = \frac{P_0}{NI_{d,pk}V_{d,pk}} \qquad (2.2)$$

In Class A power amplifier, C_p is the highest according to other classes because its operation point is at the center of its load line which will also be shown in next chapters in the simulation results. The center of load line gives the maximum voltage and current swing in the transistor.

There is also another definition, the power utilization factor (PUF), for power amplifier. When the RF power obtained by a device in a particular mode is divided into power delivered by the device in Class A mode, it gives the PUF value.

2.2.3 Power Added Efficiency (PAE)

The amplifier's efficiency is a measure of its ability to convert the dc power of the supply into the signal power delivered to the load. In an ideal amplifier, the value of efficiency is equal to one. In this case, no power would be consumed in the amplifier. In reality, this is not possible, especially for high frequency in RF circuits, the output stage and driver stage of an amplifier consume power in the amplification process.

Drain efficiency is defined as the ratio of output power at the drain to the input power supplied to the drain by the dc supply [6]. This equation is shown as;

$$\eta_d = \frac{P_0}{P_{dc}} \qquad (2.3)$$

Generally, drain efficiency is not used to characterize the performance of an RF power amplifier. Power added efficiency (PAE) gives a real approach which includes the effect of input drive power. It is defined as;

$$PAE = \frac{P_0 - P_{drive}}{P_{dc}} \qquad (2.4)$$

2.2.4 1-dB compression point ($P_{1\text{-}dB}$)

The linear region of an amplifier means a constant gain for a given frequency. In the real behaviour of an amplifier, this linear region ends at a specific frequency. This means, after this frequency, increasing the input signal does not make the output increase. The input 1dB compression point is defined as the power level for which the input signal is amplified 1 dB less than the linear gain (Figure 2.4). 1dB compression point can be shown as input or output referred. The gain decreases rapidly after this 1dB compression point. After this point, amplifier is in the nonlinear region. This means the 1dB compression point is a measure of the linear range of operation.

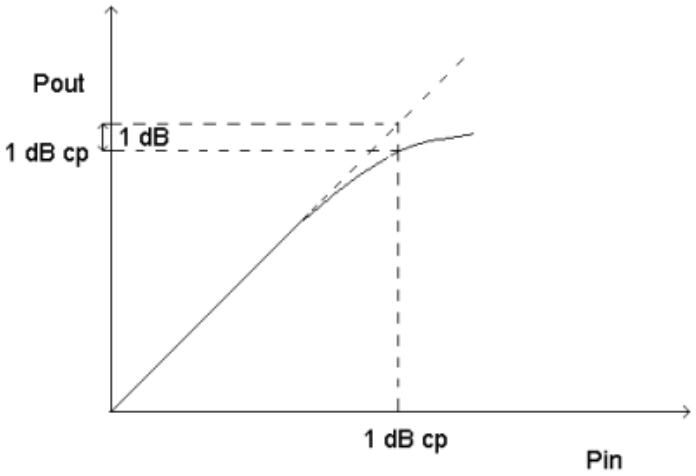


Figure 2.4 1dB compression point

2.2.5 Intermodulation Distortion (IMD)

The linear combinations of the fundamental frequency and all harmonics present in the input signal compose a nonlinear distortion. Intermodulation distortion is characterized by this distortion [7]. If f_1 and f_2 are the fundamental frequencies, then the intermodulation products are seen at frequencies given by

$$f_{IMD} = m_{f1} \pm n_{f2} \qquad (2.5)$$

where m and n are integers from 1 to ∞.

Figure 2.5 shows the higher order intermodulations. Intermodulation is specified by the ratio of power in the intermodulation product to the power in one of the fundamental frequencies. The third order intermodulation products (at frequencies $2f_1$-f_2 and $2f_2$-f_1) are typically the most critical ones because they are the closest products to the fundamentals and it is hard to filter them out from the pass band.

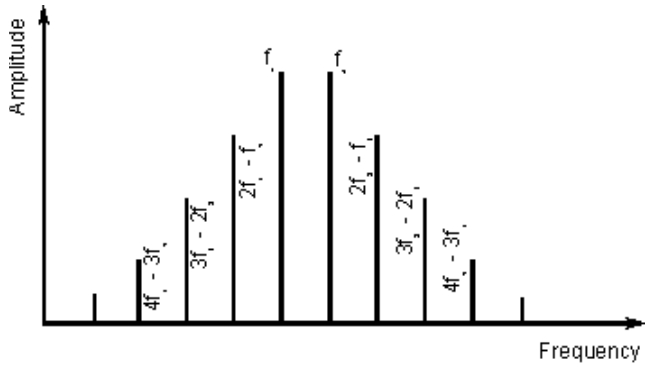


Figure 2.5 Intermodulations in an amplifier

2.2.6 Adjacent Channel Power Ratio (ACPR)

Unlike the early radio systems, modern communication systems have a modulation band that fills a bandwidth on each side of the carrier frequency. For third order products, the intermodulation (IM) bandwidth is three times the original modulation band limits. Hence, there is a leakage of power in the adjacent channel which is called adjacent channel power. The adjacent channel power ratio (ACPR) is the ratio of power in the adjacent channel to the power in the main channel (Figure 2.6). ACPR is generally used to identify the effect of intermodulation distortion and is a measure of linearity.

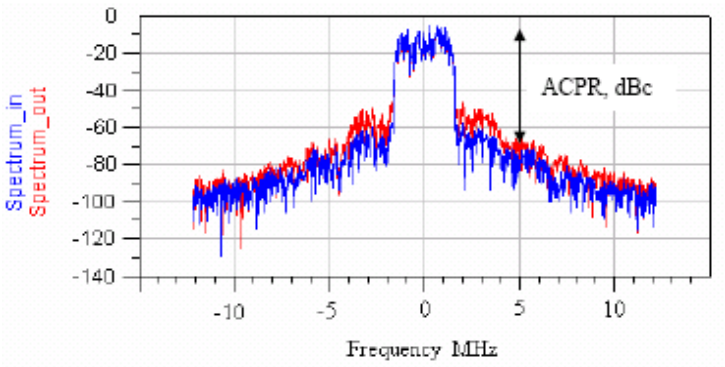


Figure 2.6 ACPR

2.2.7 Intercept Point (IP)

In the logarithmic input-output power curve, the fundamental frequency and intermodulation frequency behaviours of an amplifier can be shown together. The slopes of these two curves meet on a point which is defined as the intercept point. In this point, fundamental and intermodulation products have equal amplitude at the output of a linear circuit. But practically, these amplitudes start decreasing before this point. As a result, the third order intercept point (IP3) is defined as a meeting point of linear extrapolation of the output characteristics for small input amplitude. This point, which is shown in Figure 2.7, is important to analyze the effects of third order nonlinearities. It can be shown as input or output referred.

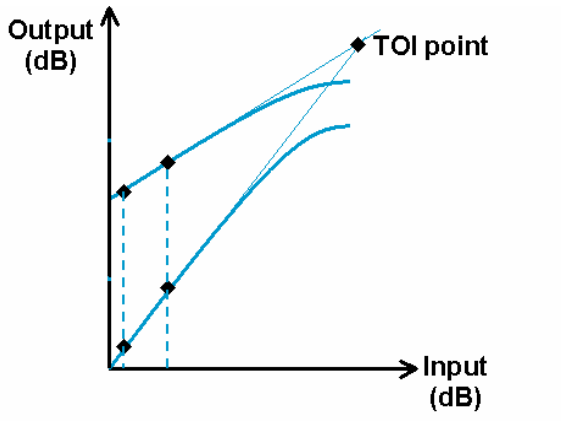


Figure 2.7 3rd Order Intercept Point

2.2.8 Total Harmonic Distortion (THD)

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental.

$$THD = \frac{\sum harmonic\_powers}{fundamental\_frequency\_power} = \frac{P_2 + P_3 + ... + P_n}{P_1}$$

Measurements for calculating the THD are made at the output of a device under specified conditions. The THD is usually expressed in percent as distortion factor or in dB as distortion attenuation. A meaningful measurement must include the number of harmonics included.

2.3 Amplifier Design Techniques

Microwave amplifiers are used to obtain low noise, high gain, or high power for different applications in communication systems. In a transceiver system, when the amplifier is used in the receiver side, its gain must be high and the noise is low. Its signal level and output power are also low. In the other hand, the transmitter side needs high power amplifier to send its output signal for long range communication [3].

There are some parameters to take into account in the design of a small-signal microwave amplifier. DC bias point is one of the most important parameters which defines the characteristic of the amplifier. Scattering parameters (s-parameters) of a transistor (or a two-port network) are also important for the performance of the amplifier. Stability, input and output matching network designs are based on these s-parameters.

The dc bias point defines the class of the amplifier. As explained before, the operating class is chosen according to the application of the amplifier will. In Figure 2.8, four different bias points are shown. Biasing the transistor at point A makes the amplifier low noise where point B gives high power gain due to big amount of current at the output node. Operating point C gives high output power which can also be said Class A operation because it is in the middle of the operating curves. And high efficiency can be obtained by biasing the transistor at point D. This graph is defined for a BJT where the bias points are defined according to different collector current values I_C and collector-emitter voltage V_{CE}. But it is also valid for a Mosfet.

As a second definition, s-parameters are used to characterize an amplifier. A transistor can be defined as a two-port network which is seen in Figure 2.9. a_1 and a_2 are the incident waves for this two-port network, where b_1 and b_2 are the reflected waves. s-parameters are shown as s_{11}, s_{12}, s_{21} and s_{22} for a two-port network and they are defined with these traveling waves.

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad (2.6)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \qquad (2.7)$$

where, 1 and 2 show the first and the second ports of the transistor. The incident and reflected waves can also be defined in terms of the voltage wave and reference impedance Z_0, in below equations (2.8) and (2.9).

$$a_1 = \frac{V_{TOWARDS\_TWOPORT}}{\sqrt{Z_0}} \qquad (2.8)$$

$$b_1 = \frac{V_{AWAY\_FROM\_TWOPORT}}{\sqrt{Z_0}} \qquad (2.9)$$

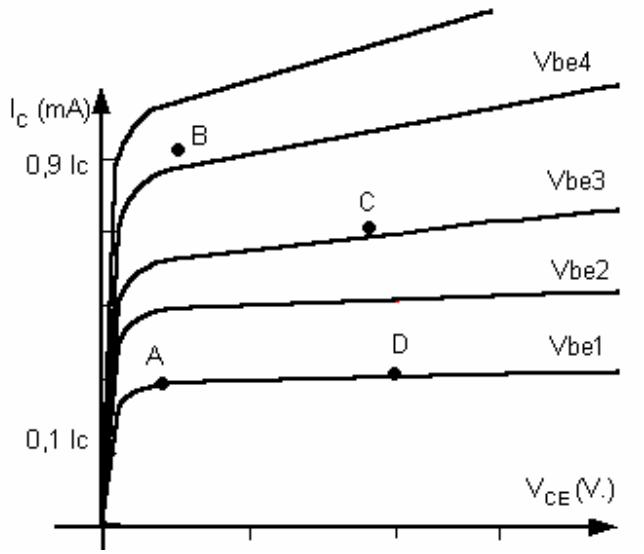


Figure 2.8 Some quiescent bias points for transistor amplifier

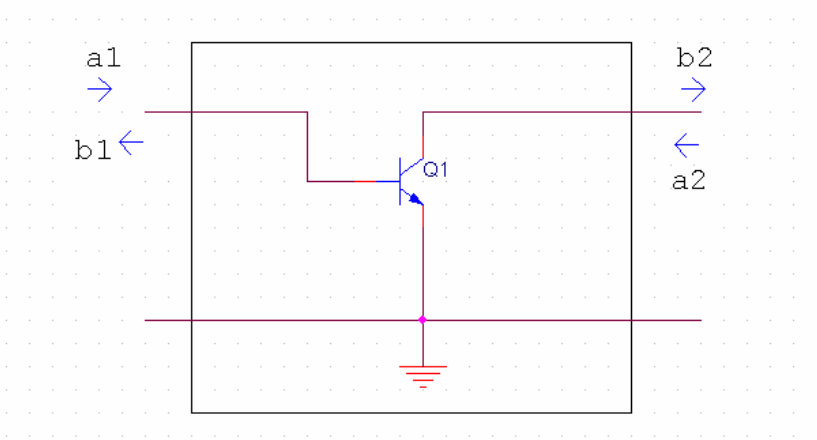


Figure 2.9 A transistor as two-port network

The s-parameters also help to define the stability of the amplifier. When negative resistance occurs at the input or output of the two-port network, there can be an oscillation. The oscillation starts when a reflection coefficient (S_{11} or S_{22}) becomes greater than one, $|\Gamma_{in}| > 1 or |\Gamma_{out}| > 1$. For stability, input and output reflection coefficients must be obtained as smaller than one for all possible values Γ_L & Γ_S using passive matching circuits.

An amplifier can be unconditionally stable or conditionally stable. If for all passive load and source impedances, the real part of the input and output impedances are greater than zero, it is unconditionally stable. But for any load or source impedance, if it becomes less than zero, it means conditionally stable. The designer can understand the condition of the amplifier by stability test for desired frequency range. Following equations help to find the stability by defining the source, load, input and output reflection coefficients. These parameters are also shown in Figure 2.10.

$$|\Gamma_S| < 1 \qquad (2.10)$$

$$|\Gamma_L| < 1 \qquad (2.11)$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \qquad (2.12)$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_L} \right| < 1 \qquad (2.13)$$

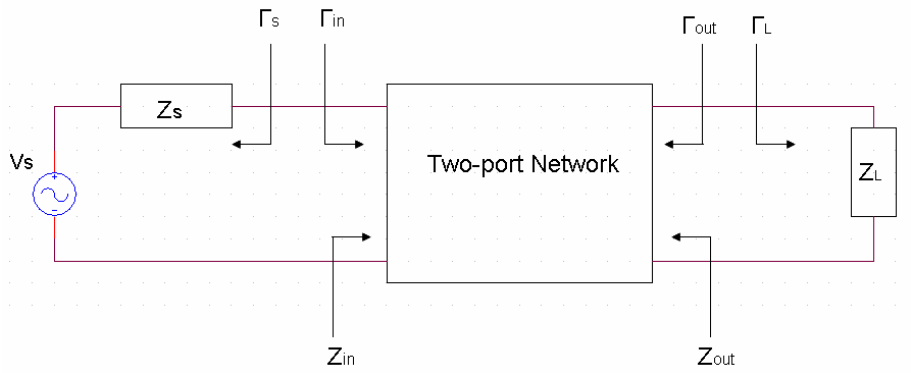


Figure 2.10 Stability of two-port network

2.4 Bias Network and Classes of PA

As mentioned in previous chapters, there are many classes of power amplifiers. They can be listed as A, B, AB, C, D, E, and etc. While going from A to E, the linearity decreases while the efficiency increases [8].

Class A, B, AB and C amplifiers can be grouped as linear mode amplifiers. As explained before, the output power is a constant multiply of the input power. In this kind of power amplifier, the output is directly derived from the input and power dissipation is high. Due to the high power dissipation, the heat increases and a solution must be used. This solution is generally using BJT at the output stage of the amplifier. This kind of transistor has a high power handling capability [9]. Class D amplifier is a switch-mode amplifier. This means the transistor is used as a switch. The efficiency of Class D amplifier is not low but high distortion levels occur. The class of the amplifier designed in this thesis is chosen as a linear mode amplifier (Class A) because high linearity is desired.

2.4.1 Amplifier Class A

There is always a trade-off between linearity, efficiency, output power and gain in power amplifiers. When the efficiency increases, linearity of the circuit decreases. This can be seen in different classes of PA. Class-A amplifier is the most linear one in all classes but its efficiency is the lowest. So, designer has to decide the class of the amplifier, which means the important characteristics, according to the application of PA. In this thesis, PA will be used in the transmitter and high output power is preferred.

A linear amplifier gives the constant multiply of input signal at the output which can be shown as below,

$$V_o(t) = AV_{in}(t) \qquad (2.14)$$

where, V_i and V_o are the input and output signals respectively, and A is a constant gain representing the amplifier gain. But if V_o is shown as the higher power of V_i, that means the amplifier is nonlinear and produces nonlinear distortion.

The most linear amplifier in all the classes is Class A amplifier. This is because of the operating point of the transistor. As mentioned before, the operating point is in the linear region. This operating point is adjusted by choosing the dc voltage of the base of the transistor to obtain high linearity and gain. Also, push-pull or single ended tuned configurations are available like Class B or C.

In Class A amplifier, the drain current is needed to be at the half of the maximum drain current. So, the waveform of the current becomes sinusoidal and maximum possible conduction angle (2π) is obtained. This also means that the transistors in the output stage conduct for the full cycle of the input signal [9]. Theoretically, maximum power efficiency in this class is 50%. Figure 2.11 shows the output current of this amplifier.

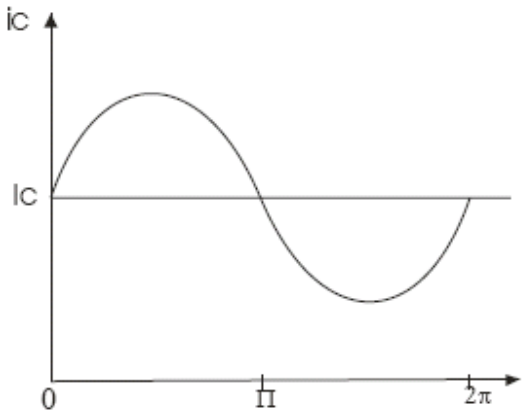


Figure 2.11 Output current waveform of a transistor in a Class-A output stage

Heat dissipation is high due to this 2π conduction angle, and the efficiency is low. But the advantage is the high linearity and low distortion in Class A. Figure 2.12 is a general layout of an output stage of Class A amplifier. In the figure, both Q1 and Q2 need to handle large power dissipations because Q1 is directly connected to VCC [10].

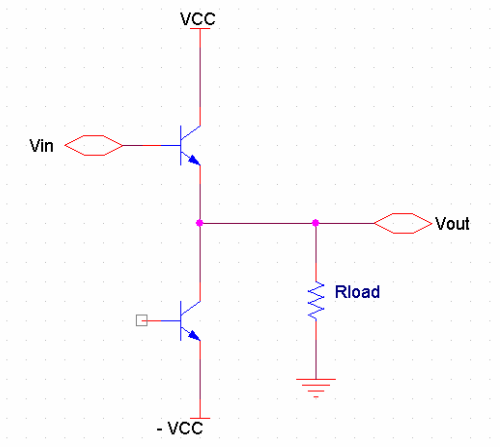


Figure 2.12 General layout of a Class-A output stage

2.4.2 Amplifier Class B

The ideal operating point of current in Class B amplifier is zero ampere, which can be classified as an opposite of Class A. This situation causes the quiescent power dissipation to be nearly zero [10]. While the dc power is related to this operating current value, it is also smaller than Class A, but the efficiency is higher. As a result, again we face the trade-off between linearity end efficiency in these classes.

Theoretically, maximum efficiency of Class B is 78% if the transistor is operating at the threshold voltage. The conduction angle is π in this class, which is the half of Class A. This also means that the device is on during the half period of the input wave. If there is a transistor pair at the output stage, they do not work at the same time. In Figure 2.13, the collector current waveform of a transistors operating in a class B stage is shown. The general layout of a class B amplifier can be seen in Figure 2.14.

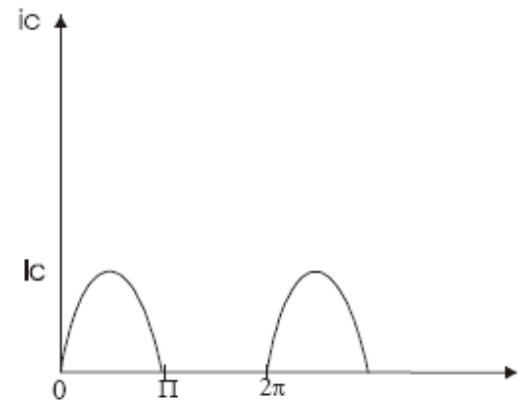


Figure 2.13 Output current waveform of a transistor in a Class-B output stage

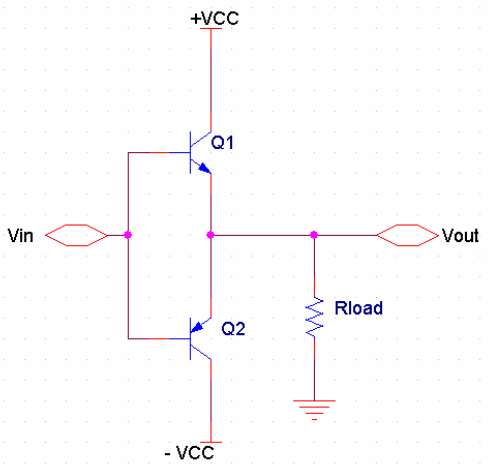


Figure 2.14 General layout of a Class-B output stage

2.4.3 Amplifier Class AB

If the trade-off between Class A and B make trouble for the designer, Class AB would be a solution for linearity and efficiency. The operating point is chosen between the former classes. Of course, the optimum point is decided according to the application. As estimated, the conduction angle of this class is between π-2π. Generally it is chosen close to the threshold voltage of the device.

If it is compared to the other ones, Class AB has higher power efficiency than Class A and wider transistor response than Class B. In telecommunication applications, this class of operation is widely used. Also there is a push-pull configuration available which is generally used in highly linear transmitters of cellular base stations.

There are several methods of biasing those complimentary output transistors. The conduction angle of a class AB output stage is over 180°, but it is still less then 360°. During (near) the intervals where the sinusoidal input signal crosses zero, both transistors conduct, and so the currents from both transistors are combined in the load. The waveforms can be seen in Figure 2.15. The class-AB amplifier is a compromise between class A and class B in terms of efficiency and linearity. The transistor is biased as close to pinch-off as possible, typically at 10 to 15 percent of I_C. In this case, the transistor will be on for more than half a cycle, but less than a full cycle of the input signal. An example of a Class-AB output stage can be seen in Figure 2.16.

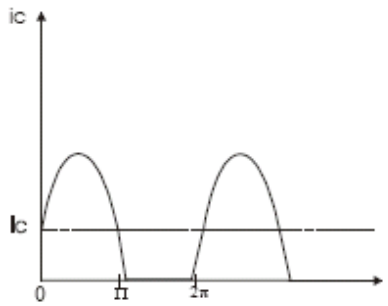


Figure 2.15 Output current waveform of a transistor in a Class-AB output stage

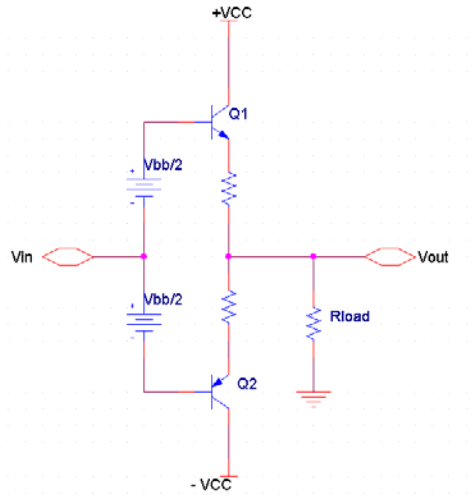


Figure 2.16 Class-AB output stage configuration

2.4.4 Amplifier Class C

The previous classes, A, B, and AB are considered linear amplifier, where the output signal's amplitude and phase are linearly related to the input signal's amplitude and phase. In the application where linearity is not an issue, and efficiency is critical, non-linear amplifier classes (C, D, E, or F) are used.

Class-C amplifier is the one biased so that the output current is zero for more than one half of an input sinusoidal signal cycle. A tuned circuit or filter is a necessary part of the class-C amplifier. Classes-A, AB, B, and C amplifiers can be defined in terms of the conduction angle *Y* as follows:

$$\text{Class of operation} \begin{cases} \text{A, } y=\pi \\ \text{B, } y=\pi/2 \\ \text{AB, } \pi/2<y<\pi \\ \text{C, } y<\pi/2 \end{cases}$$

Although the preceding analysis was for the single-ended amplifier configuration, a similar analysis can be done for the push-pull amplifier configuration. During the positive half of the signal swing, one device will push the current to the load, and during the negative half signal swing, the other device will pull the current from the load. For example, in a class-B

push-pull power amplifier, every device is on for one half of the input cycle, which means that the conduction angle is equal to 180 degrees for each device. This is similar to two class-B single-ended power amplifiers connected in a parallel line. From this observation, it is possible to conclude that the efficiency of the push-pull power amplifier is the same as that of the single-ended power amplifier with the same conduction angle, and the output power capability of the push-pull power amplifier is twice that of the single-ended power amplifier.

In Class-C amplifier, the load current flows for less then half a cycle. As a result, the current waveform looks like a train of periodic pulses. The output current waveform can be seen in Figure 2.17. If the load was to be a resistive one, this type of an output stage would not be a preferred one, as it would result in distortion. However if the load is a tuned LC circuit, then it would be possible to obtain an undistorted output. The LC circuit would have to be tuned to the frequency of the input sinusoid. Class C amplifiers are usually used in design of radio frequency (RF) power amplifiers, for example radio transmitters, TV transmitters, mobile phones, etc [10].

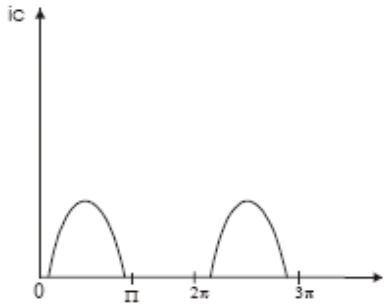


Figure 2.17 Output current waveform of a transistor in a Class-C amplifier

It is also interesting to note that the efficiency of a class C amplifier can reach up to 90%, as the power is drawn from the DC supply for only a small fraction of the cycle.

Table 2.1 brings together comparisons for different classes in terms of quiescent point and conduction angle.

Table 2.1 Classes of Operation PA [7]

Class	q-point(Vq)	Quiescent Current	Conduction Angle	Max Efficiency
A	0.5	0.5	2π	50%
B	0	0	π	78%
AB	0-0.5	0-0.5	π -2π	50%-78%
C	<0	0	0-π	Approaches to 100%

There are also a number of very high efficiency non-linear amplifiers with reduced conduction angle such as D, E, F etc. They are not to be further considered in this work due to their very poor linear characteristics, which are outside purview of this work.

Chapter 3

3 POWER AMPLIFIER DESIGN

In this thesis project, single-stage and combined Class-A Power Amplifiers (PA) are designed consecutively using the transistors available in the AMS 0.35μm SiGe BiCMOS HBT technology. These designs and evaluations will be based on first a basic DC simulation followed by a load-pull simulation.

Data communication using wireless networks such as IEEE 802.11 has found widespread use for the last few years. One of the critical components which allowed such common use of the technology can be attributed to the efficient and linear power amplifiers in the transmitter chain of the 802.11 transceivers. State-of-art power amplifier design has to be a highly efficient, high gain, ultra-linear, desired power output device while the device technology choice has also a crucial role [7]. In this study, a power amplifier design approach will be specified for IEEE 802.11a WLAN standard, and performance of different PAs will be specified in terms of power gain, PAE, linearity, gain, output power, and THD.

IEEE 802.11a standard specifies the maximum power that can be transmitted in the Unlicensed National Information Infrastructure (UNII) band. These specifications are also the output power of the amplifier for frequency band of 5.18-5.8 GHz and specified as follows: 40mW (5.18-5.24GHz), 200mW (5.26-5.32GHz) and 800mW (5.74-5.8GHz). In this thesis, the lowest frequency band is chosen as an operating frequency. So, the output power is 40mW which is equal to 16dBm.

The amplifier designs are based on AMS 0.35µm SiGe BiCMOS HBT technology which has an f_t of 40 GHz. To find the most suitable transistor for this power amplifier, seven different types of npn transistors are simulated. These transistors are symbolized as npn<c><b><e>h5 HBT which is suitable for high output voltage and power. The numbers in the symbol of the transistor <c>, <b>, and <e> refers to the number of contacts of collector, base and emitter, respectively. The typical breakdown voltages of collector-emitter and collector-base are 5.5V and 13V respectively. The capacitors and the inductors are the ideal devices defined by the process.

PA is evaluated as class A using different transistors in the AMS 0.35 µm technology using ADS environment.

3.1 Bias Point

Figure 3.1 shows a generic PA circuit for optimum transistor analysis for each class/specifications [11]. Firstly, to obtain an initial design for the load impedance, transistors are DC simulated for optimum bias values for Class-A operation. The DC simulation results are shown in Figure 3.2, where V_{CE}-I_C curves for I_B values from 20µA to 200µA are plotted. For Class-A biasing, V_{CE} should be chosen at the midpoint of the voltage swing (marker m1). This point shows V_{CE} = 2.5V and I_C = 16.34mA.

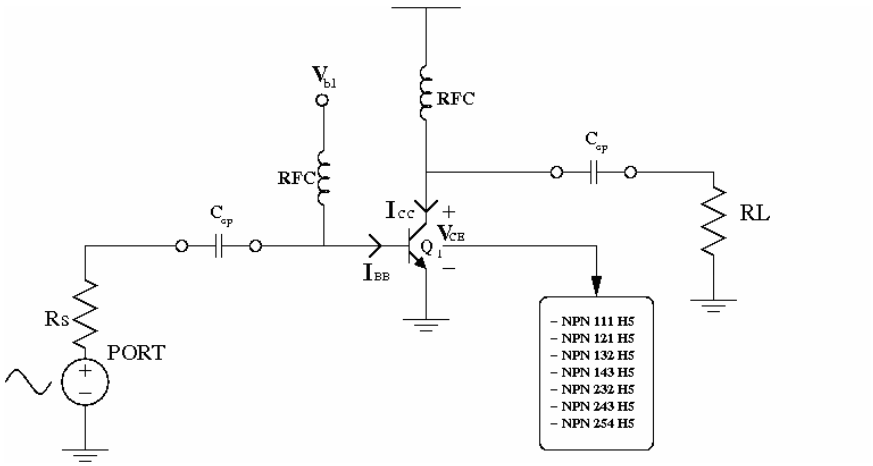


Figure 3.1 Generic PA circuit

There are seven different HBT transistors in this technology, classified based on their conductivity (power rating) and/or number of contacts at each terminals, as listed in Figure 3.1. To obtain the optimum load value for Class-A, simulations are done with the circuit shown in this figure. The capacitors on the base and collector are the by-pass capacitors and RF chokes are used for biasing. The output is terminated with variable load impedance for load-pull setup. These curves are obtained with seven different types of high-voltage HBT's in AMS technology. Due to different number of contacts at collector, base and emitters, series resistances and contact capacitances are different for each of these transistors. For Class-A bias values, $P_{out} = \frac{V_{CE}^{\ 2}}{2R_{opt}}$. After the DC simulations, optimization of the load impedance is achieved through load-pull setup.

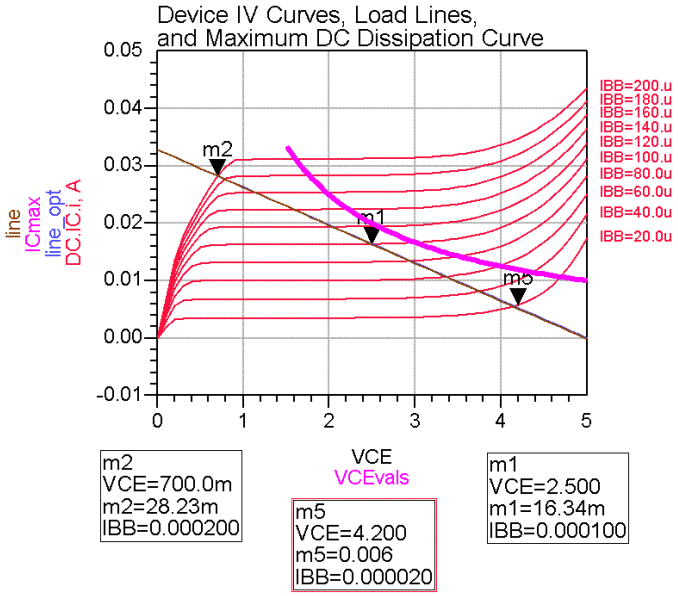


Figure 3.2 I_C-V_{CE} characteristics of single-stage PA

As a result of bias point simulations, optimum IB value is found as 100uA where npn254h5 is used. The current gain of the transistor gives 16mA IC value. The transistor will be biased according to these current values to reach the maximum power.

The bigger transistor area gives higher current capability. But for the transistors we have in AMS library, maximum area is limited with 96μm. If larger area is needed for higher

current density, more transistors have to be used. The IB and IC currents mentioned are obtained from one transistor in bias point simulations. If more than one transistor is used in parallel, higher current values can be received which also gives higher output power.

To find how many transistors should be used in parallel, several simulations are held. It is seen that we will face some disadvantages with increasing the number of transistors limitless. As an example, six transistors are used in the power amplifier and some simulation results are obtained. Figure 3.3 is the DC simulation result of six-transistor power amplifier.

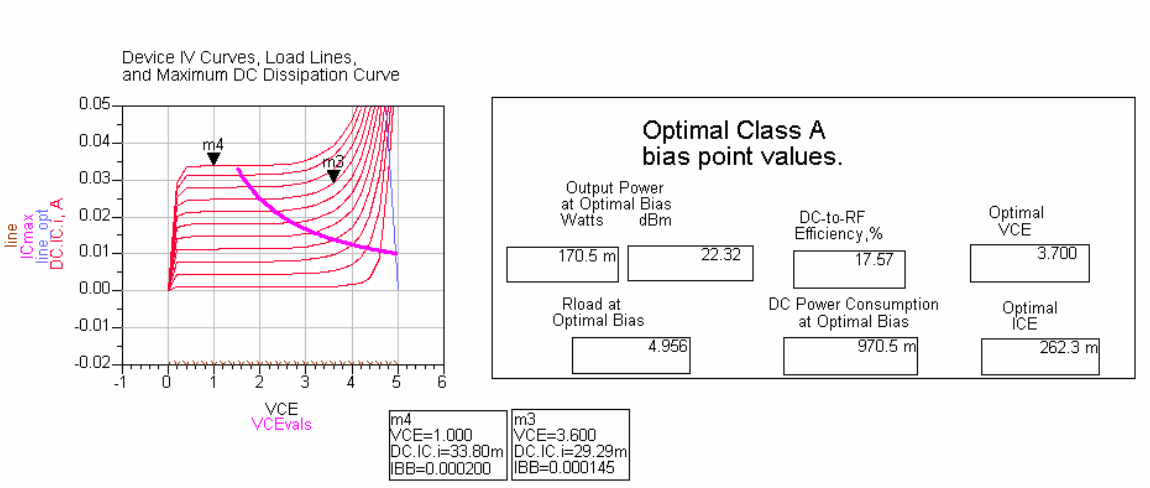


Figure 3.3 Bias simulation results of six-transistor amplifier

It can be seen that optimal Class A bias point values are given in the figure. According to these values, the amplifier will dissipate too much current to be biased properly. Hence, it will have very low power added efficiency. In addition, the input signal is connected directly to the base of the transistors. Parallel connection of many transistors will decrease the base resistance dramatically and matching will be very hard to implement.

After some trials and simulations, it is decided that using three transistors in parallel will be appropriate. The total transistor area is obtained as 288µm with this decision. This approach gives approximately 50mA output current in the power amplifier. It will be analyzed detailly in following chapters.

3.2 Matching

In many amplifier types, matching networks are used to avoid standing wave problem [12]. Matching networks can be built from passive components like striplines, inductors, and capacitors.The source impedance is generally 50Ω and to make a proper transformation, matching network is needed between this source and power amplifier input. Similarly, another matching network is needed between the output and the load impedance. With the help of matching networks, maximum gain and output power can be achieved.

In this thesis, "Load Pull" technique is used to obtain a proper matching. In load pull technique, the output impedance seen by the amplifier is swept and the amplifier performance is measured. Similarly in source pull, the input impedance is swept while the performance of the amplifier is measured. From the results of these two simulations, desired source and load impedances are found. These desired impedances are illustrated in Figure 3.4. The designer may need to choose an optimum impedance value to reach optimum efficiency, power and gain levels. If these desired impedances are obtained, power amplifier will give the best performance. The load impedance value found by load pull is required to have the maximum efficiency. In the other hand, source pull is helpful to suppress the second harmonic effects.

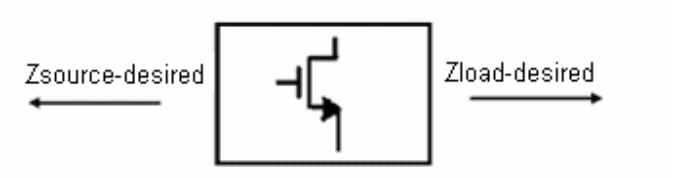


Figure 3.4 Load and Source Impedance for maximum efficiency

3.2.1 Load-Pull

Load pull matching technique gives the optimal output load impedance to achieve optimum efficiency and output power values by sweeping the impedance. Classically, the measurement method can be explained as follows. As shown in Figure 3.5, a two-port load-pull system measures the transistor under test by fixing the dc bias and ac input signal. The input tuner is adjusted for zero reflected power and this is read at power meter B. In this condition, output tuner is adjusted until the power meter C measures a given power level. The incident power can be seen in power meter A. Power gain is calculated from these power meters. Also PAE and output power contours can be obtained on Smith chart in terms of output load [3].

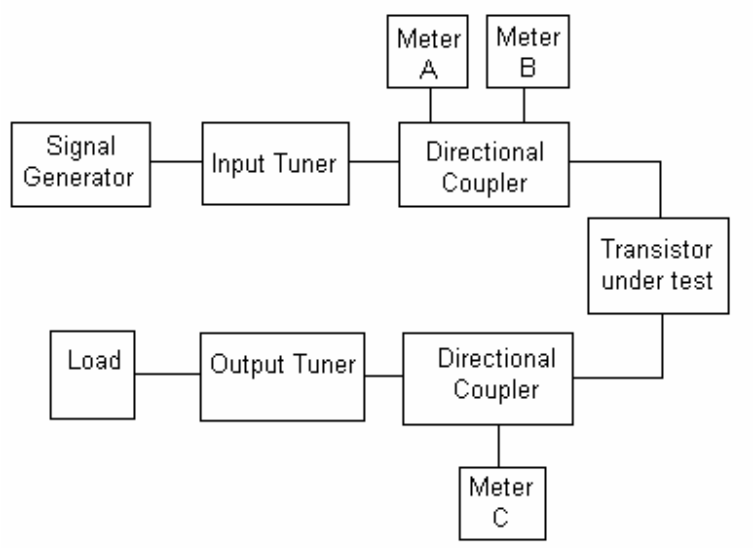


Figure 3.5 Two-port load-pull measurement system

Today, with the help of different advanced CAD tools, this measurement is simulated on computer. Their operation concept is the same. Source and load reflection coefficients are calculated as a function of gain and output power. The power and efficiency contours can be generated empirically by connecting various loads to the amplifier and by measuring the gain and the output power at each value of the load impedance. Maximum output power is

more concerned than the gain. The simulation setups and results will be examined in following chapters.

In power amplifier, the output impedance is very important to reach the maximum output power. The impedances seen from the output node must be conjugating the decrease the loss. Figure 3.6 shows the circuit that uses parametric analysis to give the optimum load impedance. At the output of the circuit, load-tuner is used. In load pull analysis the output impedance is swept and the suitable one is found. Also, linearity is an important issue for Class A amplifier. The maximum power delivered will decrease if there is a nonlinear distortion.

As seen from the figure, "SweepVar" and "Parameter Sweep" simulations are done. In the simulations, S_{11} amplitude R and phase θ are swept to find the load reflection coefficient and hence optimum load value.

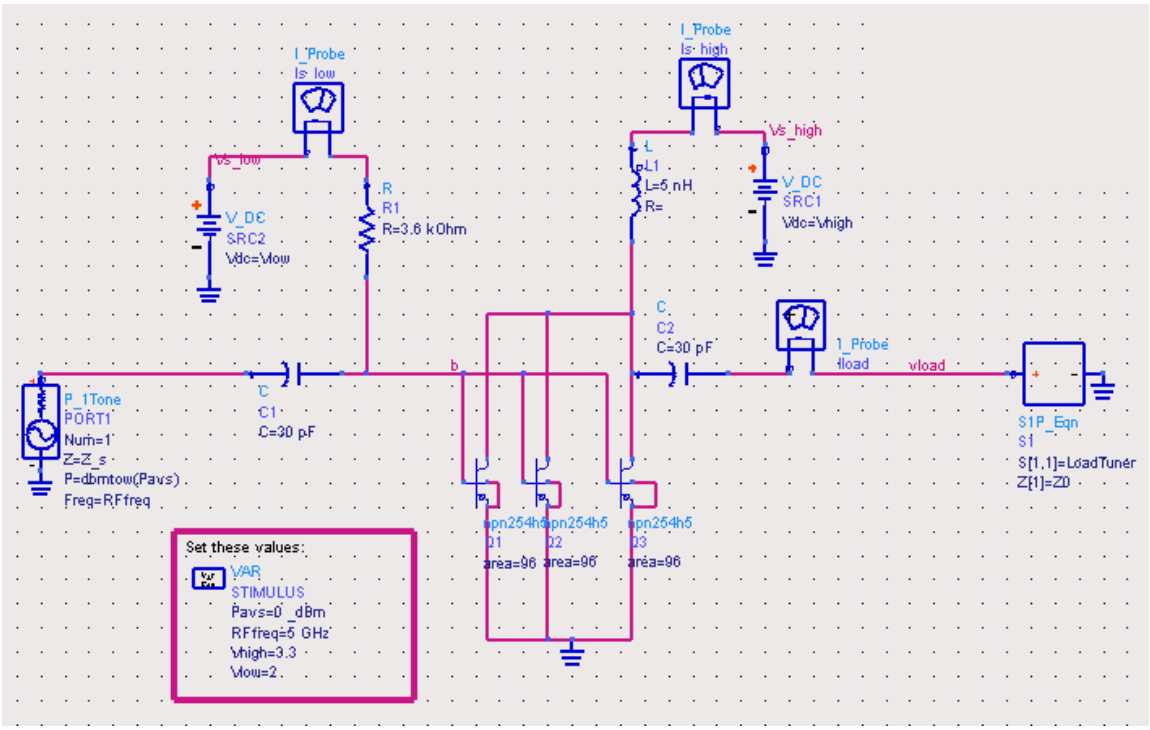


Figure 3.6 Load-pull simulation setup

Figure 3.7 shows the results of parametric analysis in the Smith Chart. PAE contours are shown in red circuits and power contours are shown in blue circles. The maximum PAE and output power delivered from this circuit are shown in these results. Also another Smith Chart shows the output impedance where these maximum values can be delivered. The impedance found from this simulation is 23.1+j*3.65.

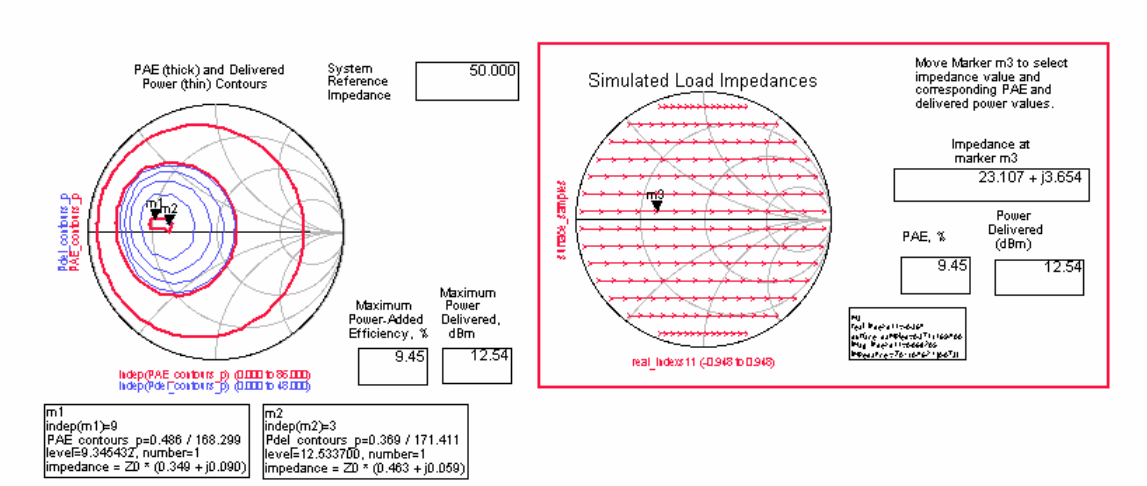


Figure 3.7 Load-pull simulation results

As a second option, the circiut is simulated as a six-transistor amplifier and load pull results are obtained as shown in Figure 3.8. This circuit is biased according to the results of previous bias simulations. It is seen that the maximum PAE of this circuit can only reach 0.56% where the maximum output power is 7.7dBm. It is seen that increasing the total area of the transistor will not give better results. Designer should find an optimum device area to reach maximum output power.

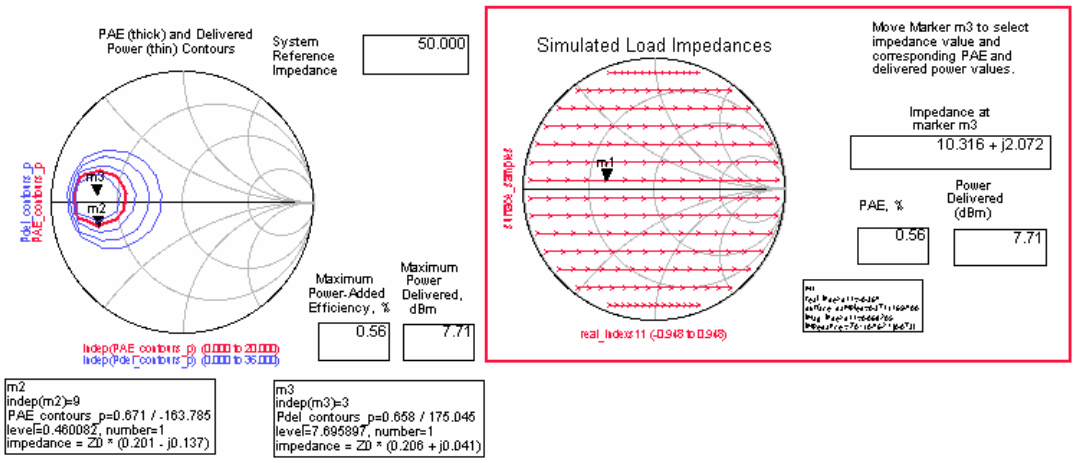


Figure 3.8 Load-pull simulation results of 6-transistor amplifier

Turning back to current three-transistor design, the next step is to match this value to the circuit after finding the desired output impedance from load pull analysis. In the transceiver, power amplifier output sees 50Ω output impedance. The circuit needs to see the desired output power when 50Ω is at the output. So there must be a matching circuit at the output. Figure 3.9 shows the matching simulation setup in ADS. The simulation frequency is 5GHz. Desired output impedance 23.1+j*3.65 will be obtained. Four different matching circuits are simulated and the most suitable ones will be shown at the s-parameter simulation output.

In Figure 3.10, the matching simulation results obtained from ADS are shown. Two matching circuit choices are available for this output matching. The below circuit is more suitable for our power amplifier because DC blocking capacitance must be in series with the output node. In this type of matching, the inductor is parallel. The values of the components are 1.49pF and 1.47nH accordingly.

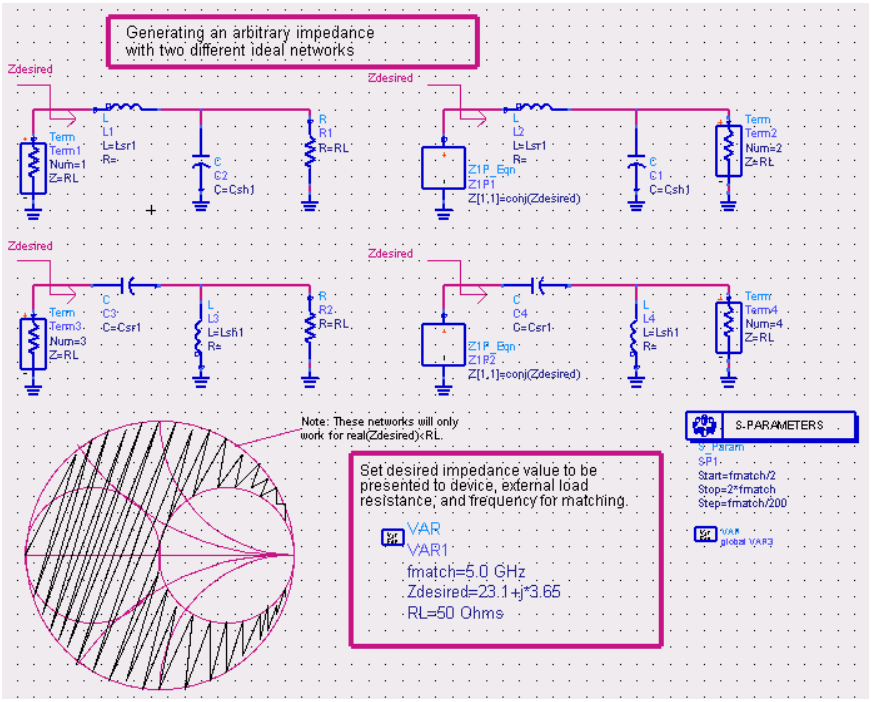


Figure 3.9 Setup for matching simulation

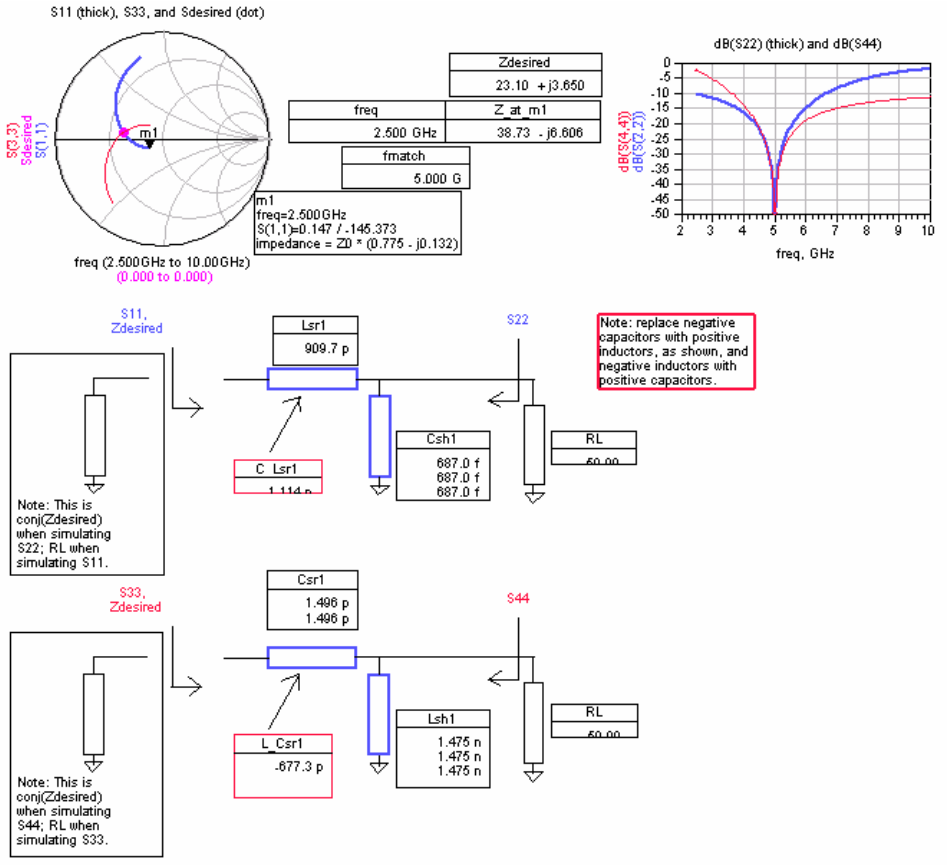


Figure 3.10 Two kinds of matching circuits found from simulation

3.2.2 Source-Pull

After the output matching, the same steps have to be taken for the input node of the circuit. Figure 3.11 is the source pull setup for the power amplifier. As seen in this figure, output matching is used at the output node. The same parametric sweep simulation is run for source pull and the result is shown in Figure 3.12. Maximum PAE is 26% and maximum output power is 16.4dBm. The desired input impedance that gives these values is 3.69+j*6.32.

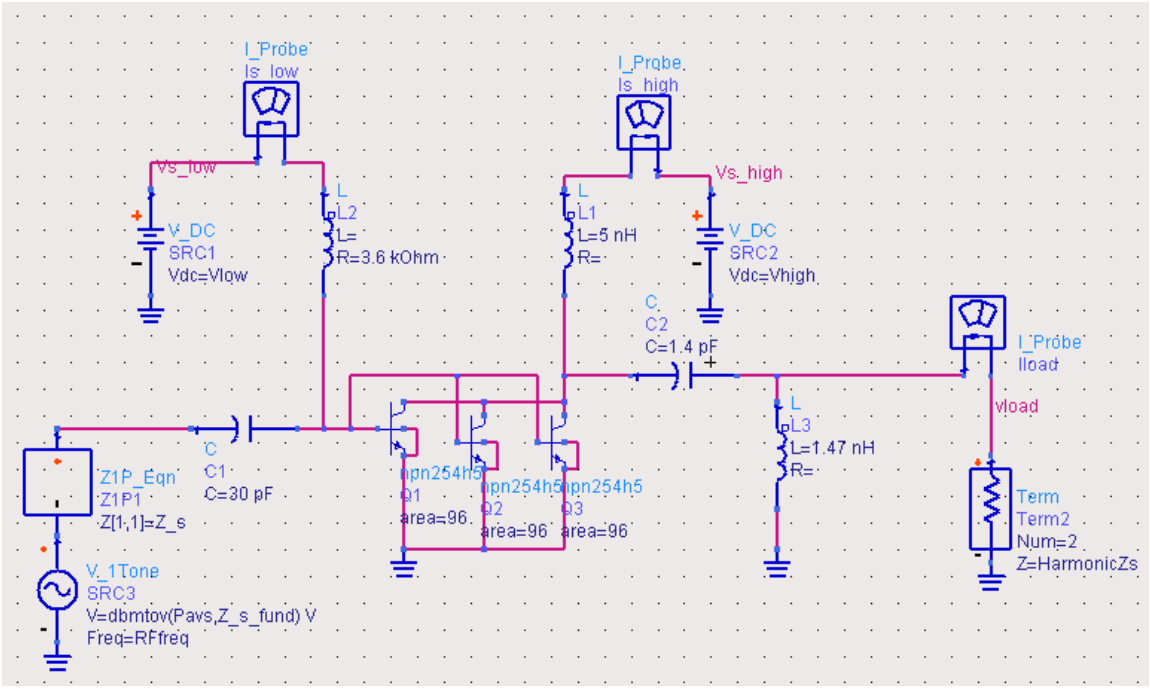


Figure 3.11 Source-pull simulation setup

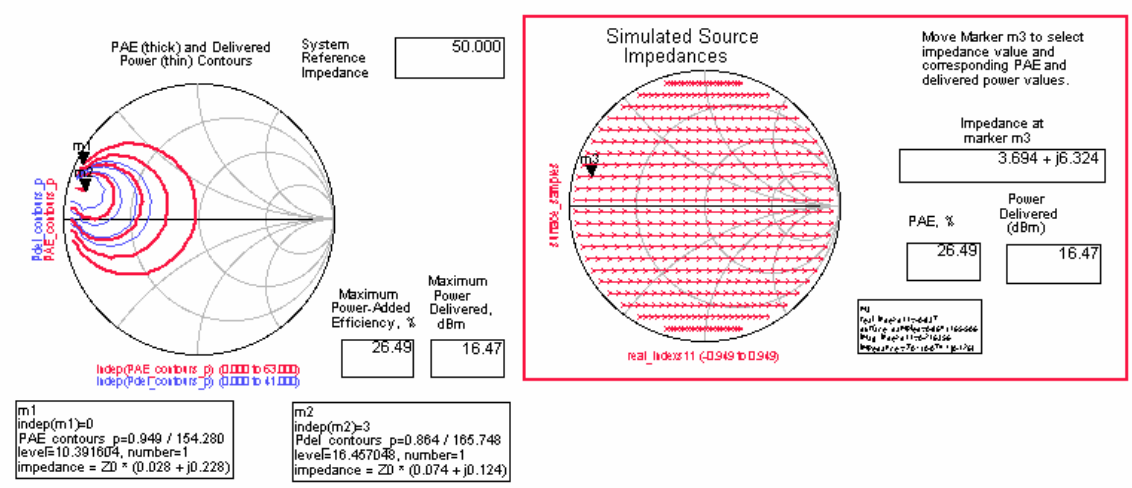


Figure 3.12 Source pull simulation results

Just like the output matching, matching simulations are done in ADS for input node. Figure 3.13 shows the setup circuit to find the proper input matching circuit. This time desired Z value to be seen from the input node is 3.69+j*6.32. In Figure 3.14, simulation results are given. S33 is our desired Z value and the same type of matching circuit is obtained with C=1.64pF, L=450pH.

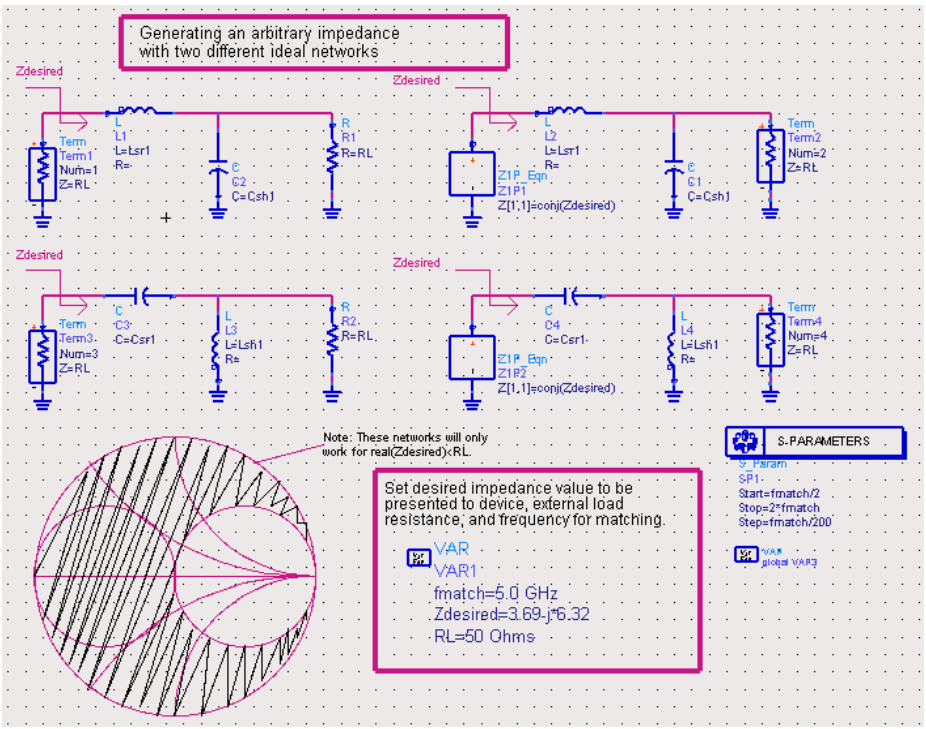


Figure 3.13 Setup for input matching simulation

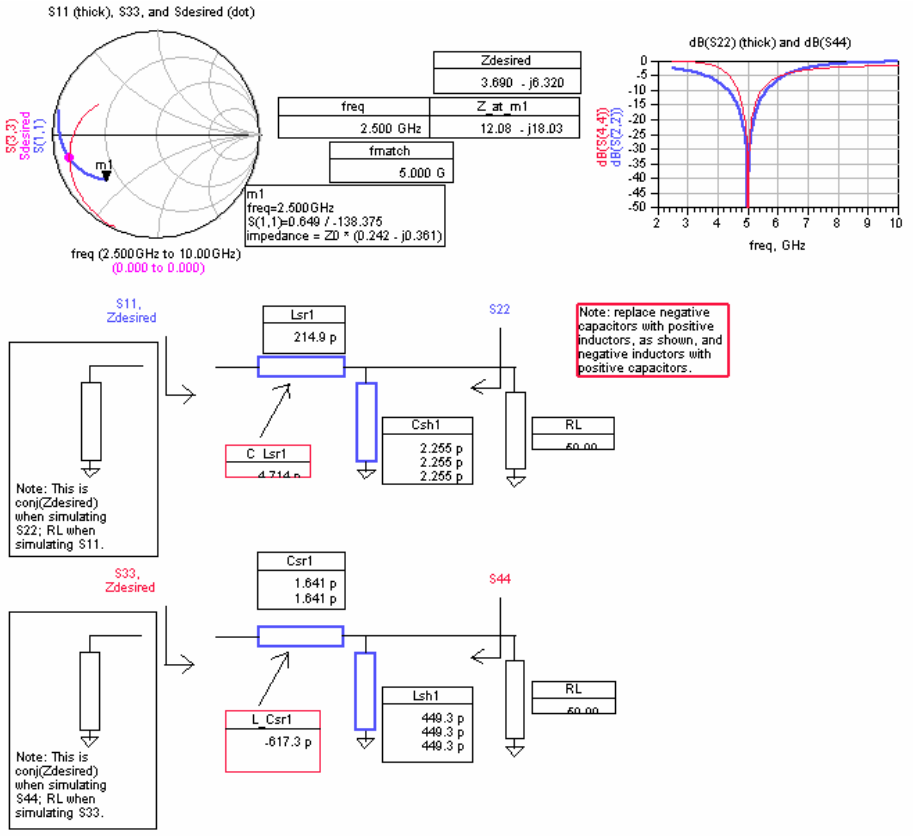


Figure 3.14 Input matching circuits found from the simulation

There is a trade-off in matching for single-stage PA's. The input matching is connected to the base of the power transistor where the output matching is connected to the collector node. So, these two nodes are not isolated from each other. As a result of this, output matching is changed after input matching circuit is applied. In this step, matching adjustment is done to reach the optimum capacitance and inductance values. So, the values found from the above simulations are not constant. In the next chapter, the final values of matching components are mentioned after some adjustments.

3.3 Single-Stage Power Amplifier Design

In the previous source pull and load pull simulation circuits, a single-stage power amplifier is shown. After the input and output matching circuits are found, the single-stage PA is

obtained (Figure 3.15). As shown in the figure, input and output ports have 50Ω impedance. The desired impedances are obtained with the help of matching circuits.

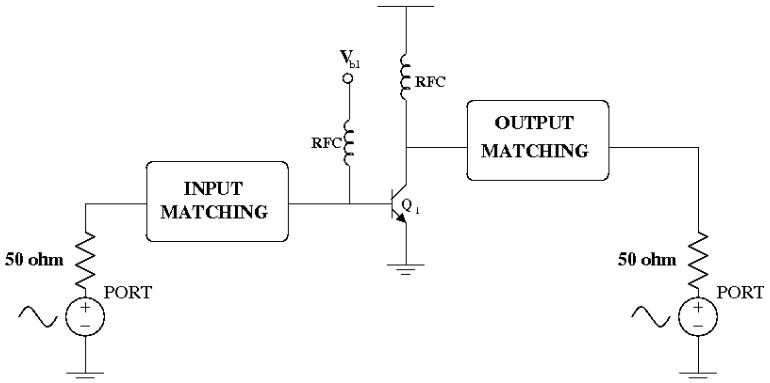


Figure 3.15 Single-stage PA with matching circuits

Figure 3.16 is the final single-stage PA circuit to be simulated in ADS. In the input matching, parallel inductance is 500pH and series capacitance is 2.12pF. At the output, capacitance is 2.21pF where inductance value is 4.77nH. These values are found after several matching simulations mentioned in previous chapter.

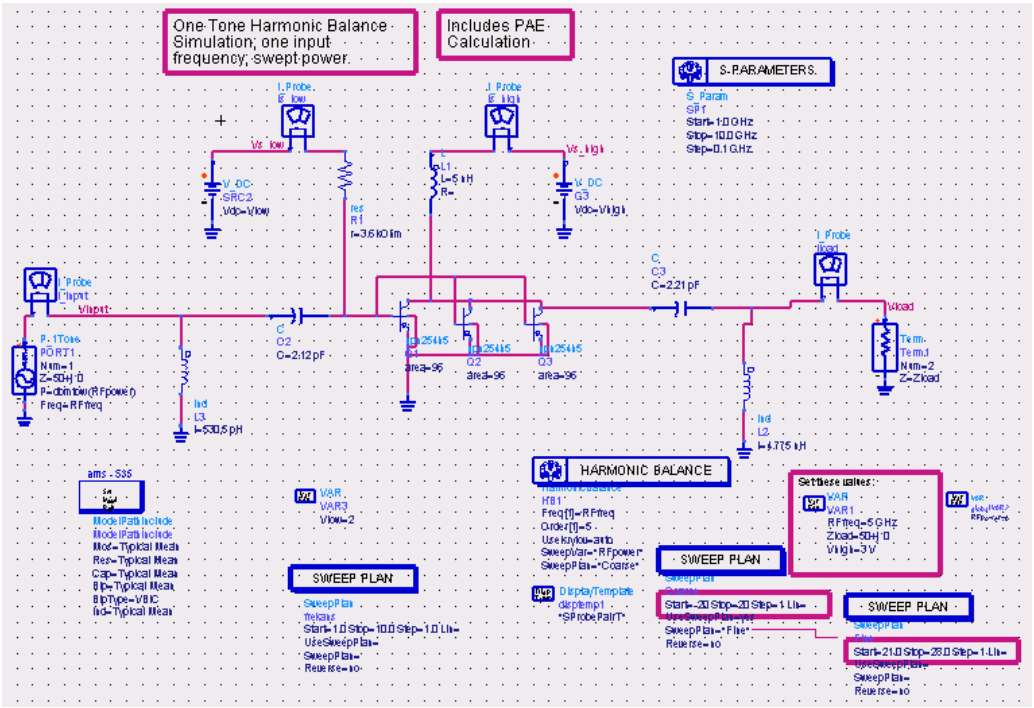


Figure 3.16 Single-stage PA with proper matching

The simulation results in ADS are shown in Figure 3.17 and 3.18. At the 1dB compression point, output power is 15.2dBm and gain is 17.4dB. At this compression point, input power is -3dBm. Also Power Added Efficiency (PAE) is 20% in this circuit. Some other simulation results are also seen in Figure 3.17. At the operating frequency (5GHz) S11 is obtained at the minimum value, -5.3dBm. S22 is -6dBm at this frequency. The gain of the circuit is also calculated as a different name, P_gain_transducer. Also 1dB compression point is found with two markers and output power value is 15.2dBm which is seen with marker m2.

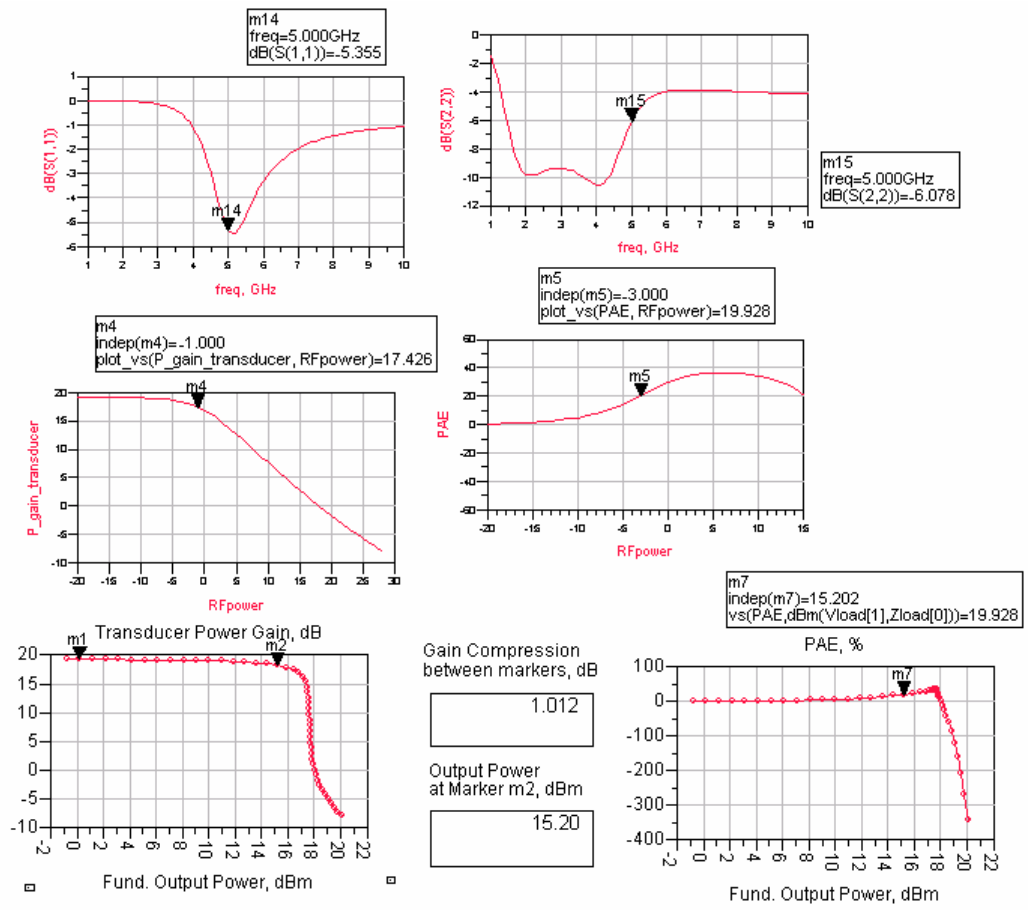


Figure 3.17 Simulation results of single-stage PA

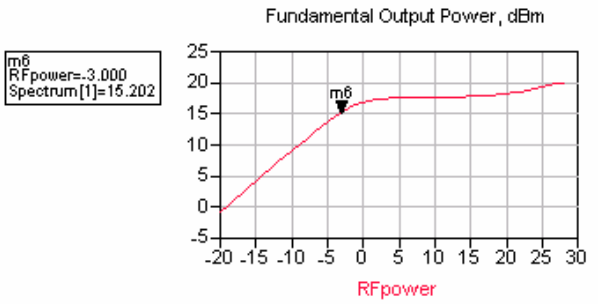


Figure 3.18 Input-output power characteristic

Figure 3.19 shows the simulation setup of the circuit in Cadence environment. Inside of the component "PA" is the same single-stage circuit which will be simulated using Cadence. It is shown in Figure 3.20. It can be seen that the schematic is the same as Figure 3.16. In Cadence environment, parametric sweep will be applied to the circuit to find the compression point, output power and PAE. But before the simulations, the real components are included instead of ideal ones. Inductors, capacitors and resistances are replaced with the ones with ideal behaviour in Figure 3.21. With this kind of simulation, the real behaviour of the circuit will be obtained. As an inductor, spiral is used which is defined in the library of AMS. The inductance of the spiral changes according to the number of turns, width, length, and the degree of the metal. Naturally one node of the spiral is connected to ground. In AMS technology file, some certain inductances are defined as spiral. So, if we want to use spirals instead of ideal inductor, we have to choose the most adequate spiral from the library. Similarly, capacitance is used as CMIM (Metal-Insulator-Metal) which shows the real capacitance that AMS produce. It is the capacitance between the second and the third layer of metals. In AMS technology, maximum CMIM is 1.1pF. So, for higher values, more than one CMIM are connected in parallel.

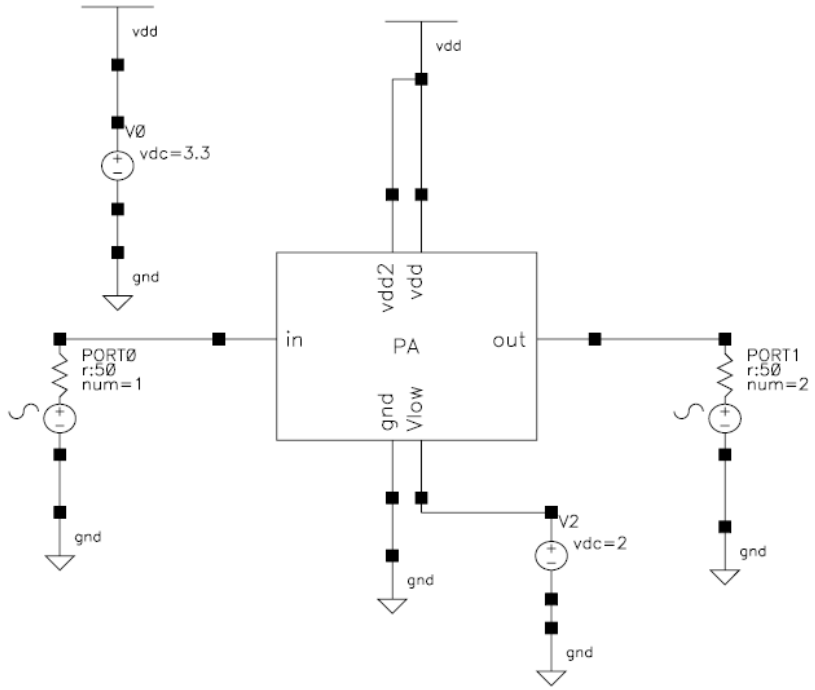


Figure 3.19 PA circuit in Cadence environment

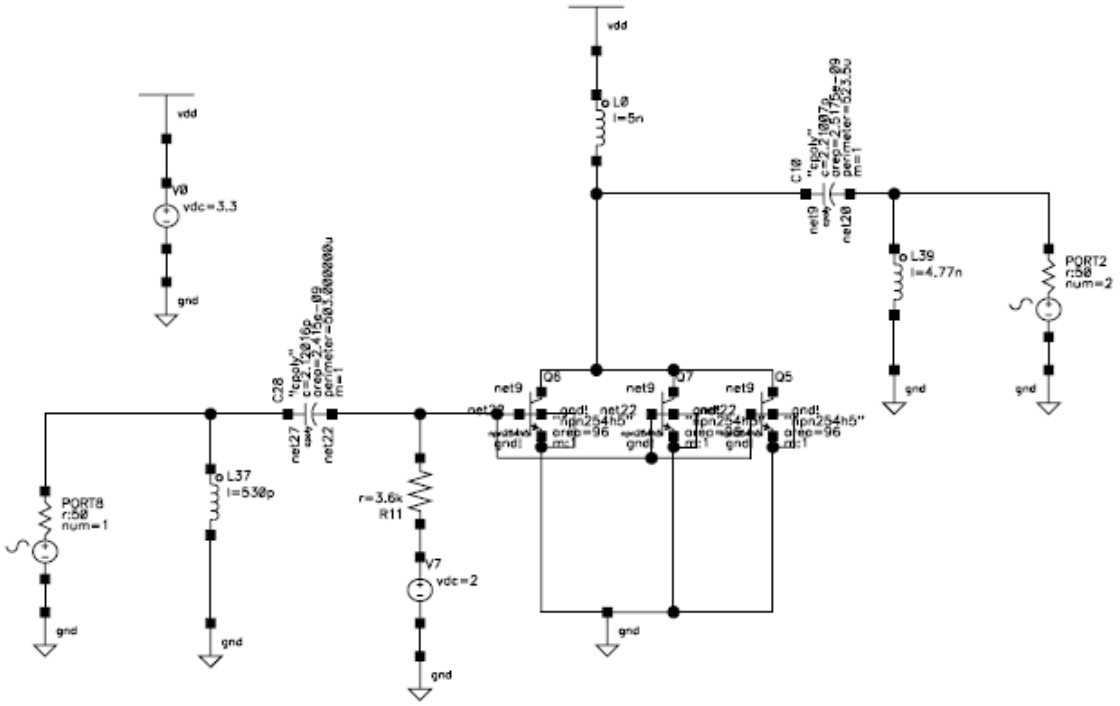


Figure 3.20 Single-stage PA in Cadence

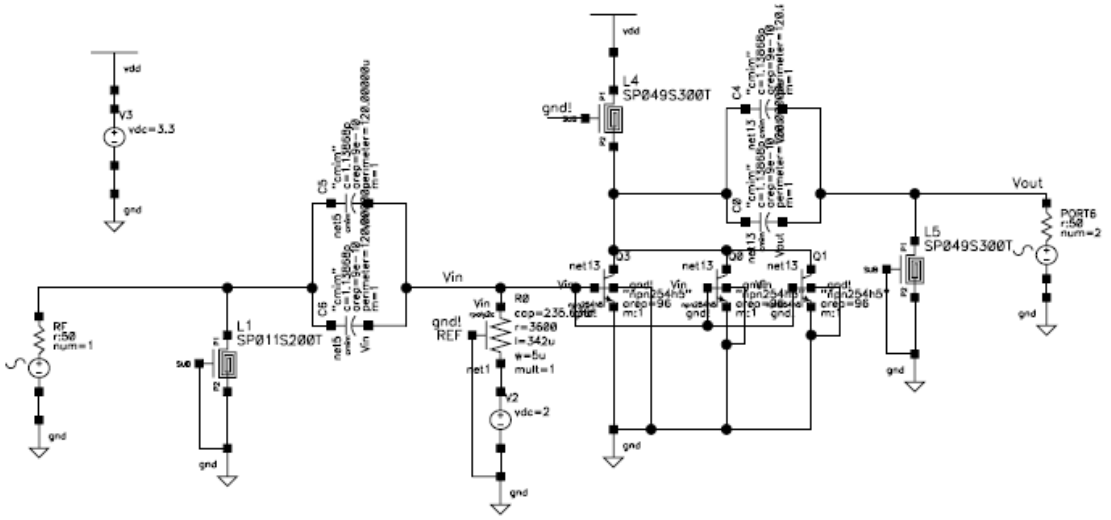


Figure 3.21 PA circuit with real components

The simulations are performed on the circuit shown in Figure 3.21. Parametric sweep simulation has to be performed to see the power values of the circuit. Figure 3.22 shows the Pin-Pout graph. In this figure "prf" is the input power and it is swept during the simulation. It can be seen that the 1dB compression point is obtained at around 1.6dBm input power. The linear line shows the 1st order line while the curve shows the real behaviour of the circuit. 1dB compression point is the one that these two lines are crossed. The output power stops increasing after Pin=1.6dBm point. It is shown on the same diagram. At 1dB compression point Pout=15dBm.

PAE is another important value in power amplifier. Figure 3.23 shows the PAE of the circuit which is found from parametric sweep simulation. In the 1dB compression point, Pin=1.6dBm and PAE=18%. These values are close to the ones we found in ADS simulations but they are slightly smaller. This is due to the real components used in the simulation. In Cadence environment, to get more realistic results, real component models are used. In this situation, some parasitic effects are taken into account and the results show some deviations which are expected.

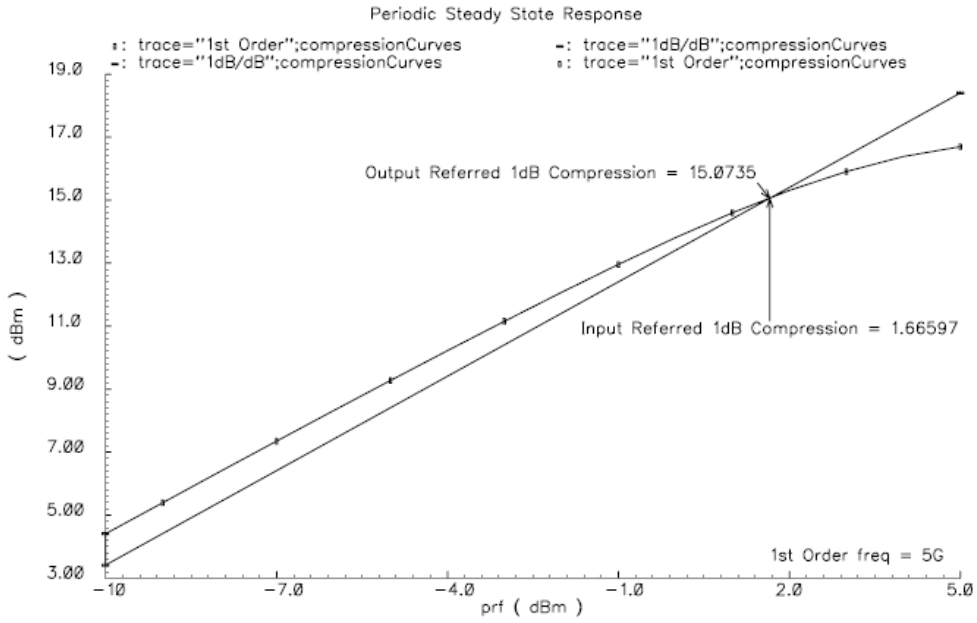


Figure 3.22 Pin-Pout graph

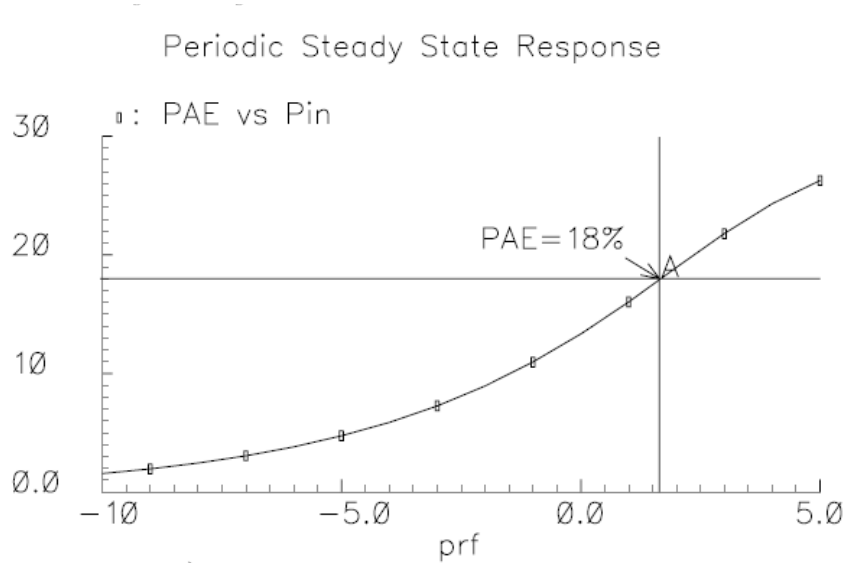


Figure 3.23 PAE

Figure 3.24 and 3.25 show the available voltage gain and power gain circles for the PA in the Smith Chart. In Figure 3.24, circles are drawn from 10dB to 20 dB at 5GHz while the circles are getting smaller. This result is found from s-parameter simulation, where the gain is calculated using s-parameters of the circuit. Similarly in Figure 3.25, the power gain

circles are shown with 2dB steps from 10dB to 20 dB while they are getting smaller. It can be seen that for two different type of gain, the center of the circles are nearly the same. That is because of the relation between the voltage and power. If high gain is desired, the s-parameters of the circuit must be located near the high gain circle.

At this point, if Figure 3.25 and Figure 3.7 are compared, the trade-off in PA design can be seen clearly. Figure 3.7 shows the power circles of the amplifier and they are converging to a point near the line where the imagenary part is zero. That means for maximum output power, desired load impedance is near the real Z line. However, in Figure 3.25, maximum gain point is in the middle of the yellow circle and it is far away the real Z line. These results show that designer has to decide the operating point according to the fuction of the power amplifier. If high output power is desired, the gain will stay in low values. In this design, maximum output power is observed and the matching circuits are designed according to the maximum Pout. So, the gain of the circuit will be low. Figure 3.26 shows the Total Harmonic Distortion (THD) of PA. It is seen that at the 1dB compression point, its value is 6.3%.

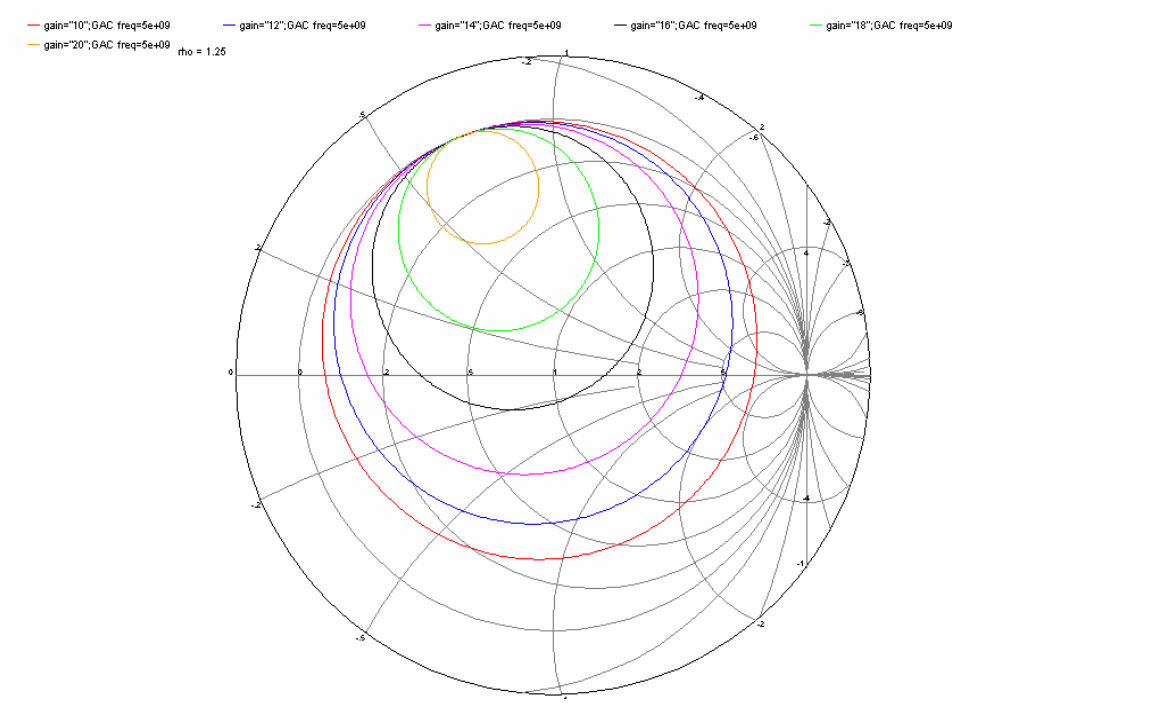


Figure 3.24 Available gain circles

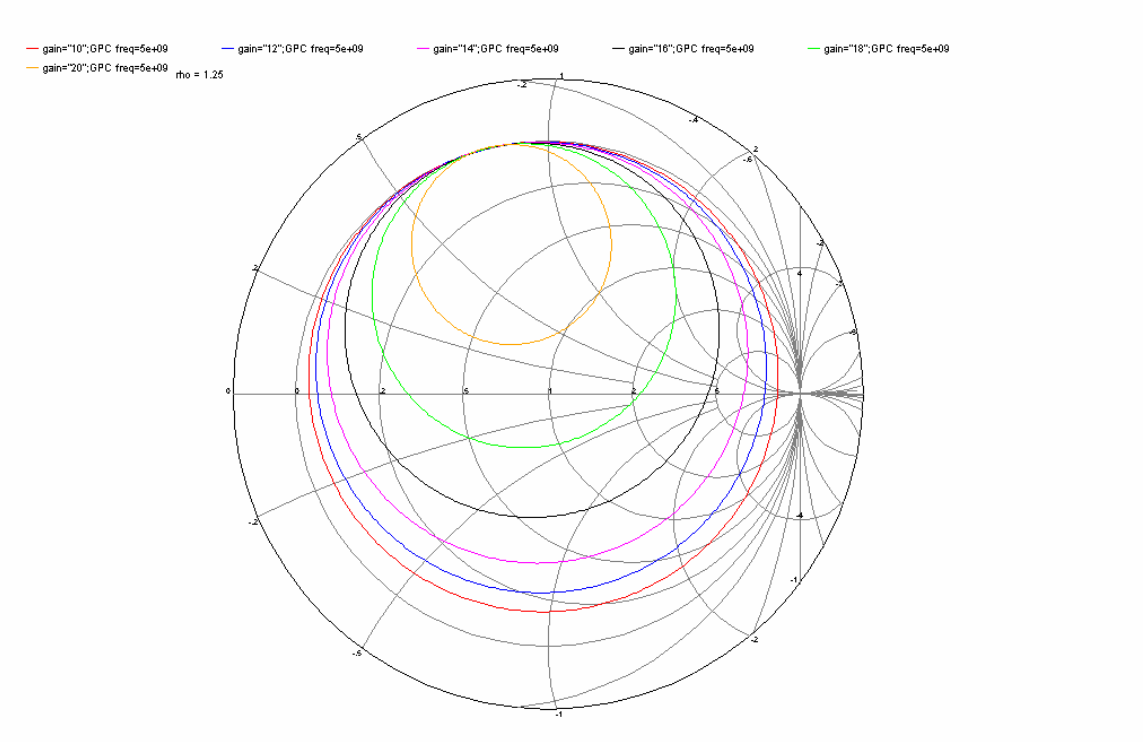


Figure 3.25 Available power gain circles

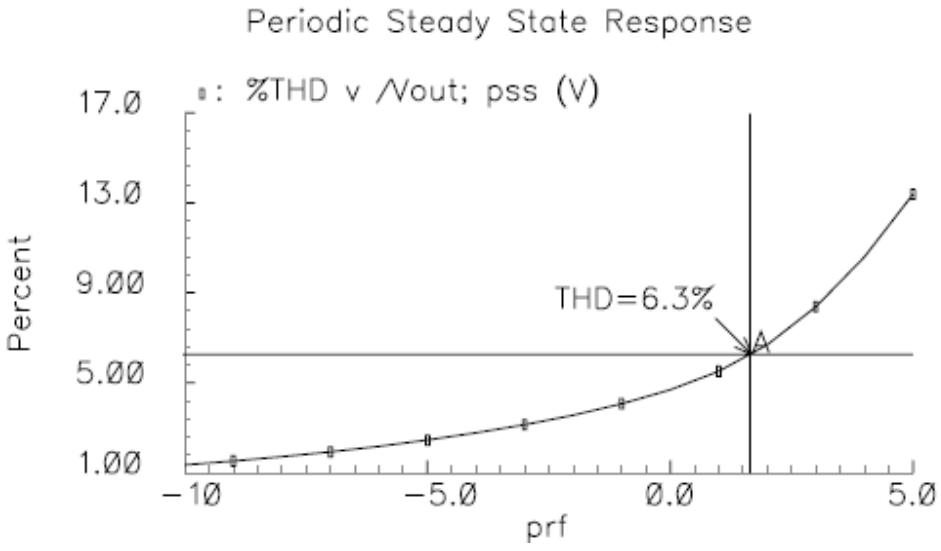


Figure 3.26 THD

3.4 Power Combining

3.4.1 Introduction

In order to obtain the required output power levels of IEEE 802.11a standard, the power combining technique will be utilized. The desired transmitter output is generally achieved by combining the outputs of individual power amplifiers. Combining smaller PAs instead of one single larger PA offers higher gain, wider bandwidth, beter linearity and lower cost. In addition to these advantages, heat dissipation is easier with smaller devices.

Two main power combining techniques can bementioned [18]. As a first combiner type, quadrature-hybrid combiner can be stated. There is a 90° phase shift at the input of one power amplifier and at the output of the other one. In this combining technique, the input impedance is constant which suppresses the odd harmonics. The effect of load impedance is also reduced. A two-terminal quadrature combiner architecture can be seen in Figure 3.27.

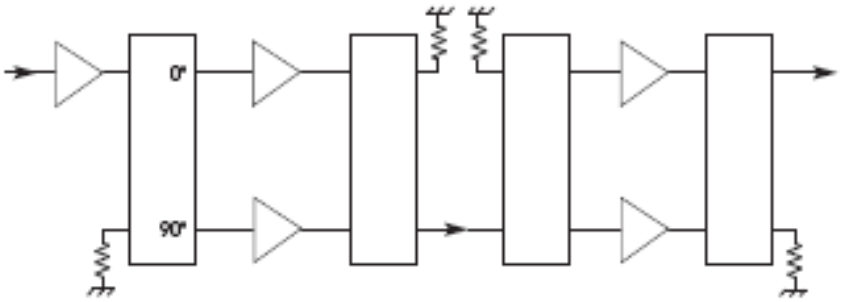


Figure 3.27 Amplifier stages with quadrature combiners

The other combining technique which is also used in this thesis is Wilkinson power combiner. It is easier to fabricate than a quadrature combiner. Also greater bandwitdh can be obtained by increasing the number of amplifier stages. Like other power combining techniques, this one also suffers from circuit and mismatch losses. If the number of stages

increase, the losses also increase. General combining type microstrip line is more lossy than the other implementation techniques if open microstrip line is used. Due to this disadvantage, suspended microstrip line is preferred which offers good performance and cost. Of course microstrip line is implemented on board which is not possible in the technology we use.

In Wilkinson power combining technique, first the RF signal is splitted into two paths with a "1:2 lumped element Wilkinson power divider" and two RF amplifiers are fed with the splitted RF signal. The output stages of each amplifier are then combined with an "output 2:1 lumped element Wilkinson power combiner" [13].

At the output stage, higher levels of output power are produced compared to that obtained in the single amplifier case. This method also improves the linearity of the power amplifier since the linearity decreases as the operating input RF power increases. Generally, 2^n power amplifiers are combined to achieve high output power [14]. Figure 3.28 shows a classical microstrip Wilkinson power divider.

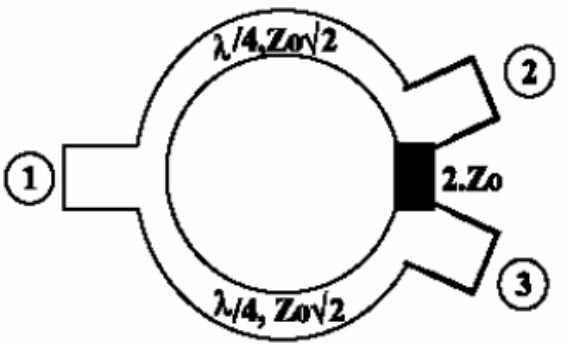
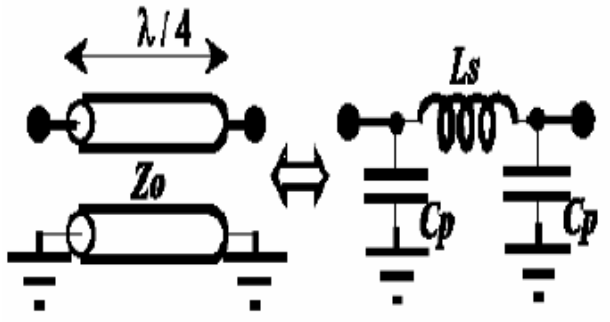


Figure 3.28 Microstrip Wilkinson power divider

A λ/4 transmission line can be modeled with a lumped element pi equivalent network as shown in Figure 3.29. Using this equivalent circuit, four power amplifiers are combined like the one in Figure 3.30.



$$L_S = \frac{Z_O}{2 * \pi * f_O}$$

$$C_P = \frac{1}{2 * \pi * f_O * Z_O}$$

Figure 3.29 Equivalent power divider network

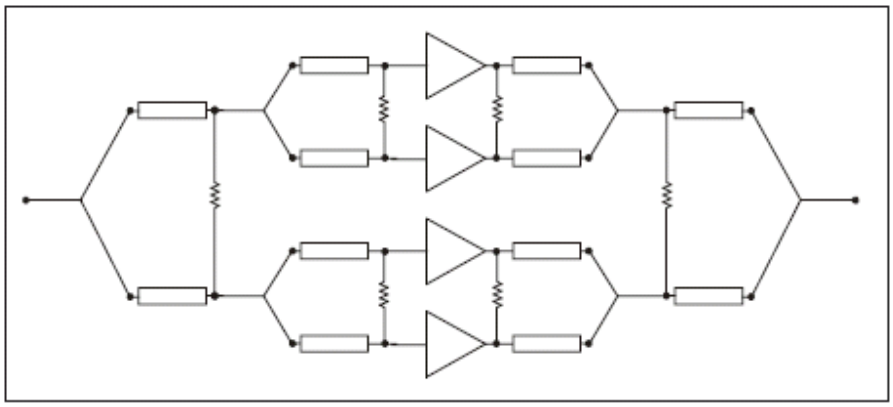


Figure 3.30 Multi-section Wilkinson combining architecture

3.4.2 Combined Power Amplifier Design

A lumped component Wilkinson power splitter is designed and used in power amplifier in ADS which operates at 5 GHz. Figure 3.31 shows how the values of components in Wilkonson divider are simulated. The terminal in the left hand side represents the input source. Three capacitors, two inductors, and a resistor are used to divide the input power. Terminals 2 and 3 are representing the inputs of two single-stage power amplifiers designed. The power obtained from the input source is divided into two amplifiers by using the components with proper values. For example, if the input power is 0dBm, the inputs of the other PA's are -3dBm.

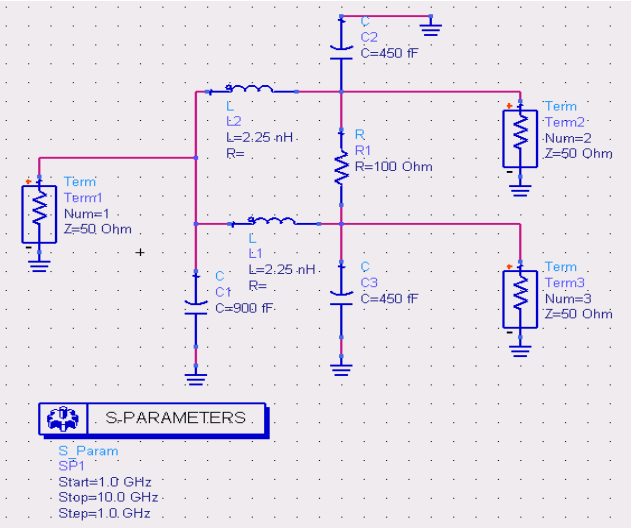


Figure 3.31 Power divider in ADS

The power splitter is also used as power combiner in the whole circuit. The output powers of two amplifiers are summed up at the output and the combined PA is simulated like the single-stage amplifier.

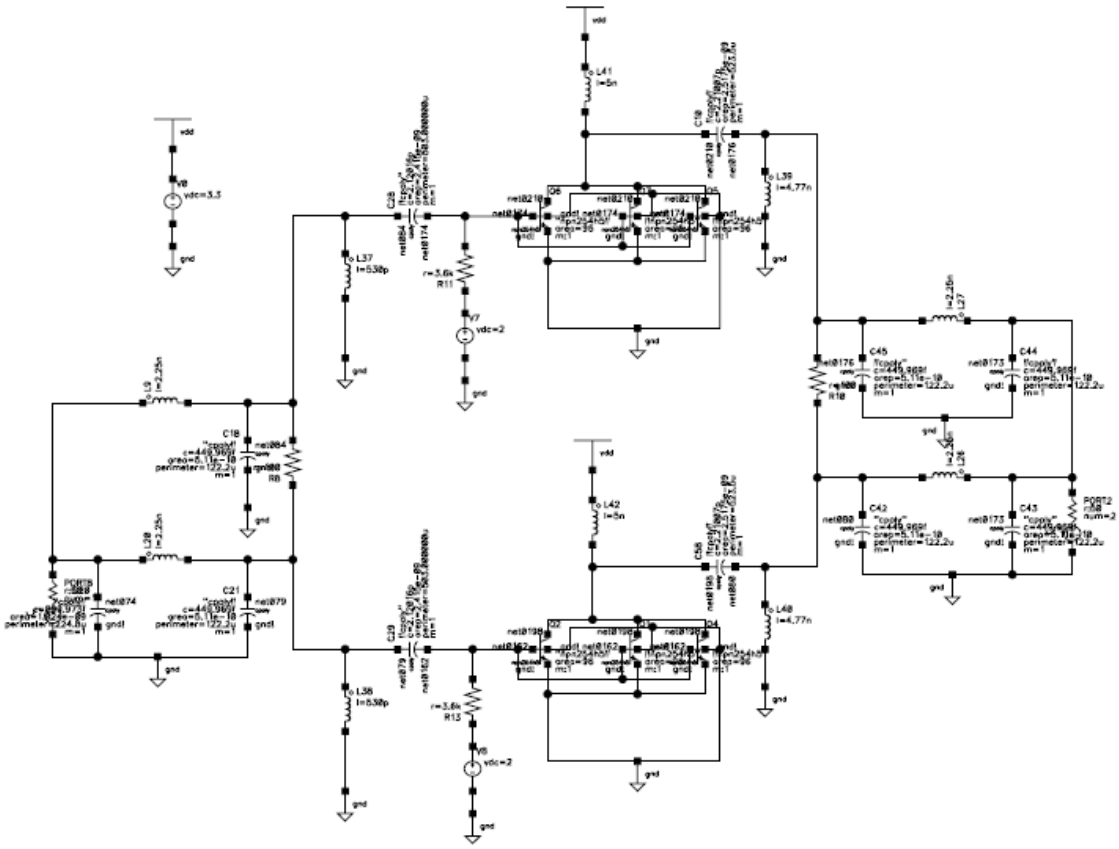


Figure 3.32 Combined Power Amplifier with Wilkinson technique

Figure 3.32 shows combined two single-stage power amplifiers. As a first step, ideal components are used in simulations. After the parametric sweep simulation, input-output power relation is obtained which is shown in Figure 3.33. 1dB compression point in the input is around 0dBm and the output is 17dBm. This means the maximum input power of one single-stage is -3dBm and the maximum output power is 14dBm. The gain of the total combined power amplifier is about 20dB.

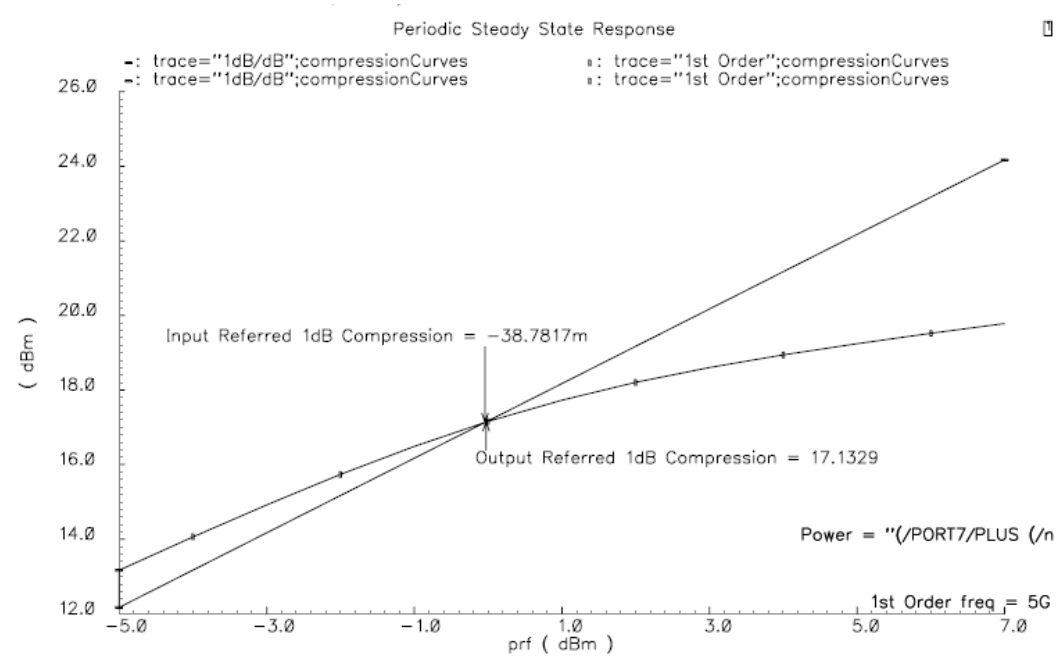


Figure 3.33 Pin-Pout graph (input and output referred)

Figure 3.34 shows the PAE of the ideal combined power amplifier. At 1dB compression point, PAE is 14%.

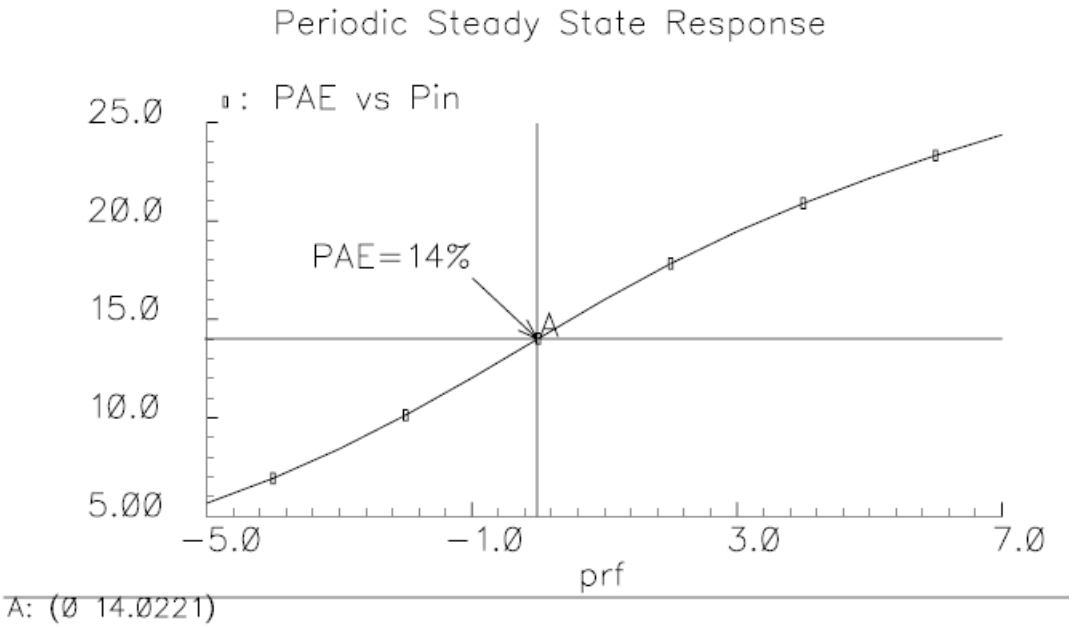


Figure 3.34 PAE

After parametric sweep simulations, s-parameter simulation is also done in power combined amplifier. As shown in Figure 3.35, available power gain circles are drawn on the Smith Chart. Like the one in single-stage power amplifier, the centers of two kinds of circles are nearly the same. While the power gain values are getting bigger, the circles are getting smaller. It is seen that the center of the circles is different from the single-stage amplifier. So, combining two PAs creates a different amplifier with different bias.

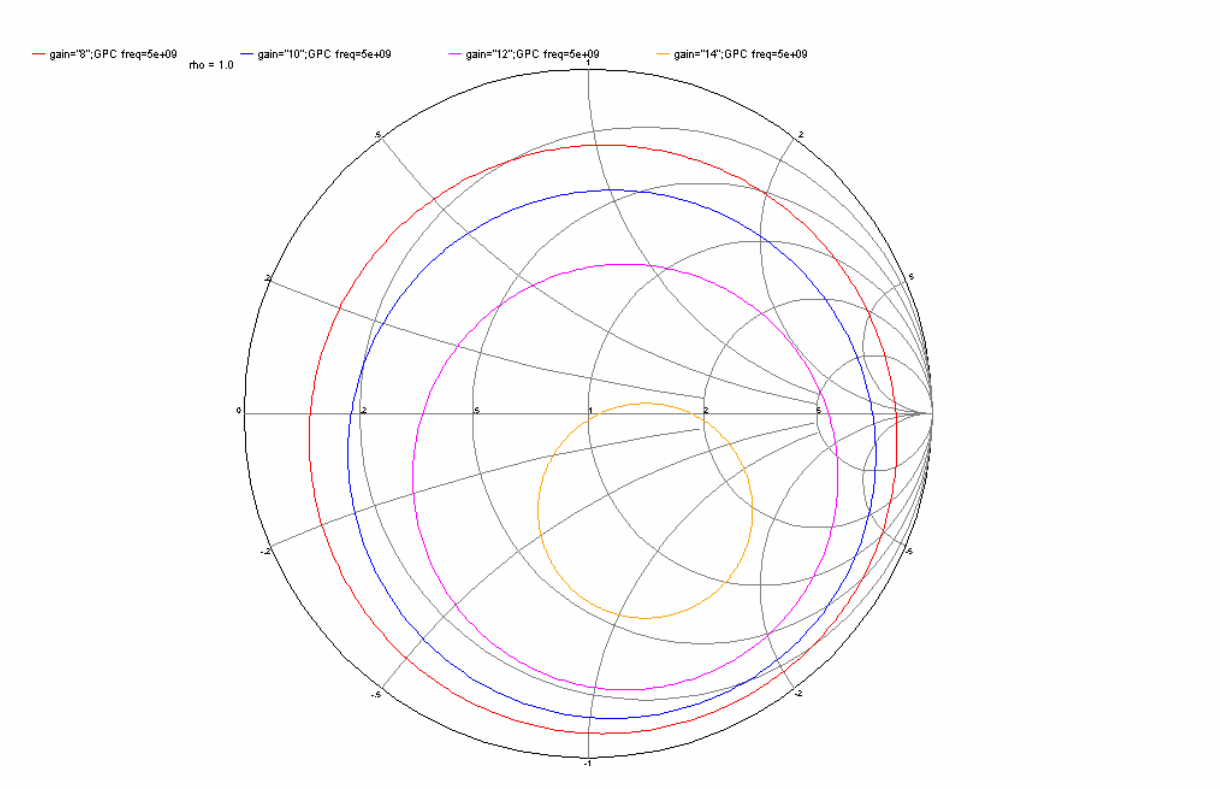


Figure 3.35 Available power gain circles

As a final simulation result, THD is shown in Figure 3.36 for combined PA. At the 1dB compression point, its value is 2.5%.

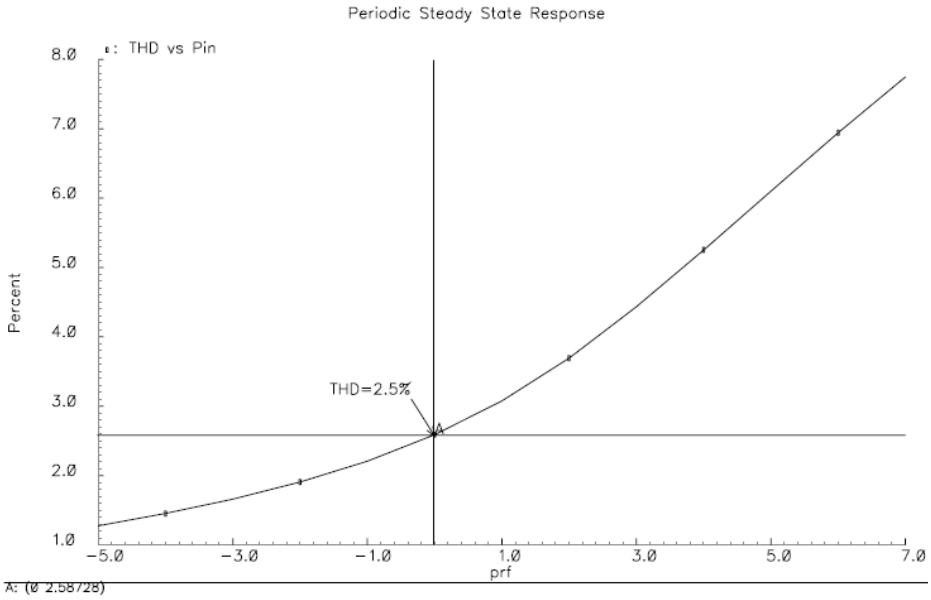


Figure 3.36 THD

If we want to compare these simulations with other works, there are some studies about combined power amplifiers. As an example, Perkons [15] implemented the Wilkinson power combining technique with microstrip delay lines to focus the guided waves. The output power of Transverse Magnetic (TM) spatial power combiner is 16dBm at the 1dB compression point. This result is obtained at 8.25GHz and input power is around 6dBm. In the same study, compression output power for Transverse Electric (TE) surface wave combiners is 14dBm at 5GHz.

In another scientific work, four-amplifier combiner is presented. Hang [16] used microstrip combiner to reach optimum efficiency. At 2.2GHz frequency, output power is 28.8dBm when input is 19.5dBm. When this thesis is compared with these works, the input-output power relationship is reasonable for 5GHz integrated power amplifier.

The second step in the schematic design is using real models of components. Figure 3.37 shows the schematic of the circuit with real component models. For example, Cmim is used as capacitance and two of them are used in parallel to obtain 2.2pF which was also mentioned in previous chapter. The inductors (spirals) and resistors have a node to be connected to the ground. These changes make a slight difference in the simulation results.

Some parasitics come from the real models. The simulation results can be seen in below figures.

Figure 3.38 shows the Pin-Pout relation in this circuit. It is seen that at 1dB compression point, Pin=5.9dBm and Pout=17.2dBm. These results are nearly the same as the previous circuit. At this compression point, gain is around 13dB as shown in Figure 3.39. When input power of the combined PA circuit is 5.9dBm, the input power of a single-stage becomes around 3dBm. According to the previous simulations, 1dB compression point of the single-stage circuit is found as 1.5dBm. So, the amplifier can not work at the maximum compression point, it is limited at 1.5dBm. Calculating from this point of view, the output of the single-stage becomes 15dBm maximum. At the output, we could receive 17dBm which shows that there are some losses coming from the real models of combiner and splitter components. Other simulation results for PAE and THD are shown in Figure 3.40 and 3.41 resulting 14% and 1.3% respectively.

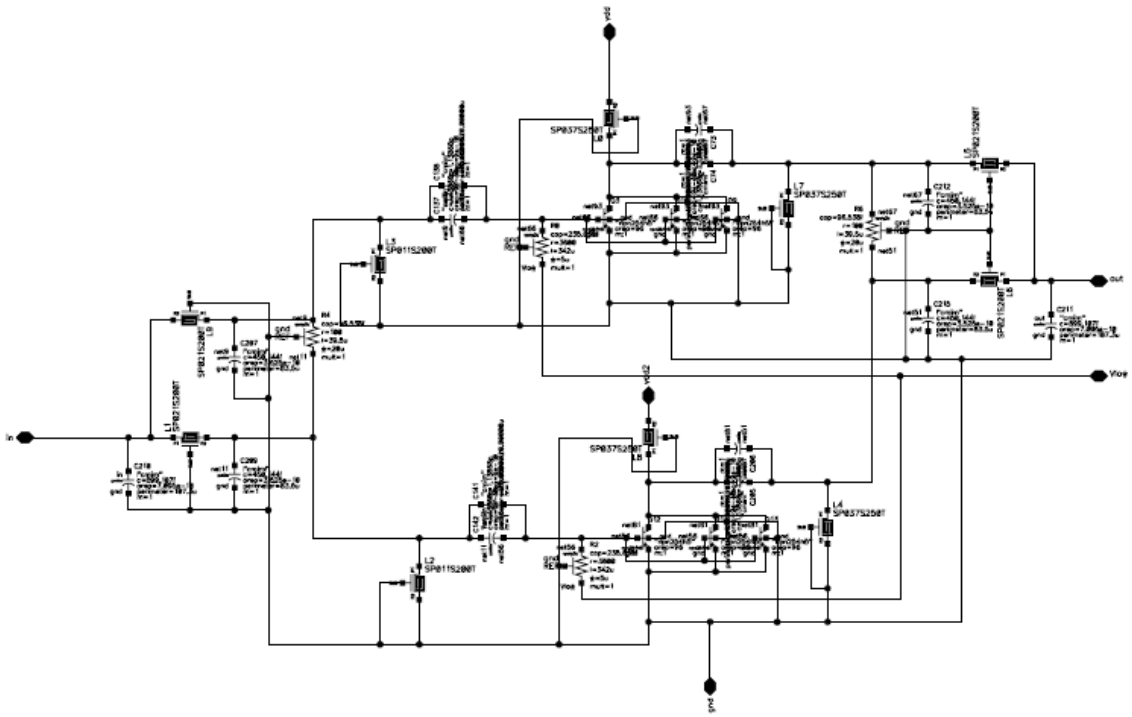


Figure 3.37 Combined Power Amplifier with real components

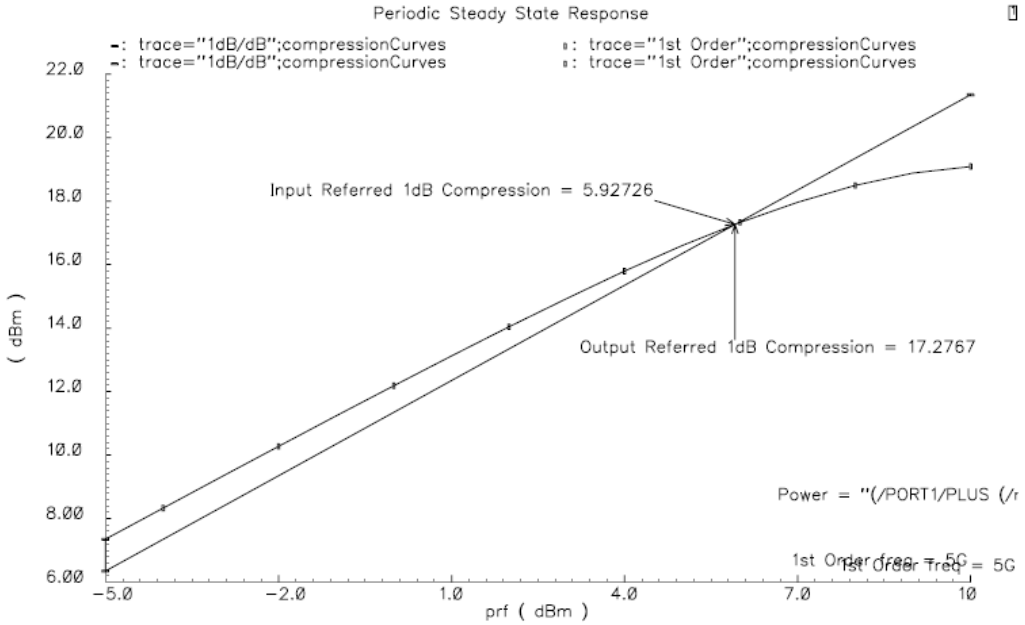


Figure 3.38 Pin-Pout Graph for schematic design with real components

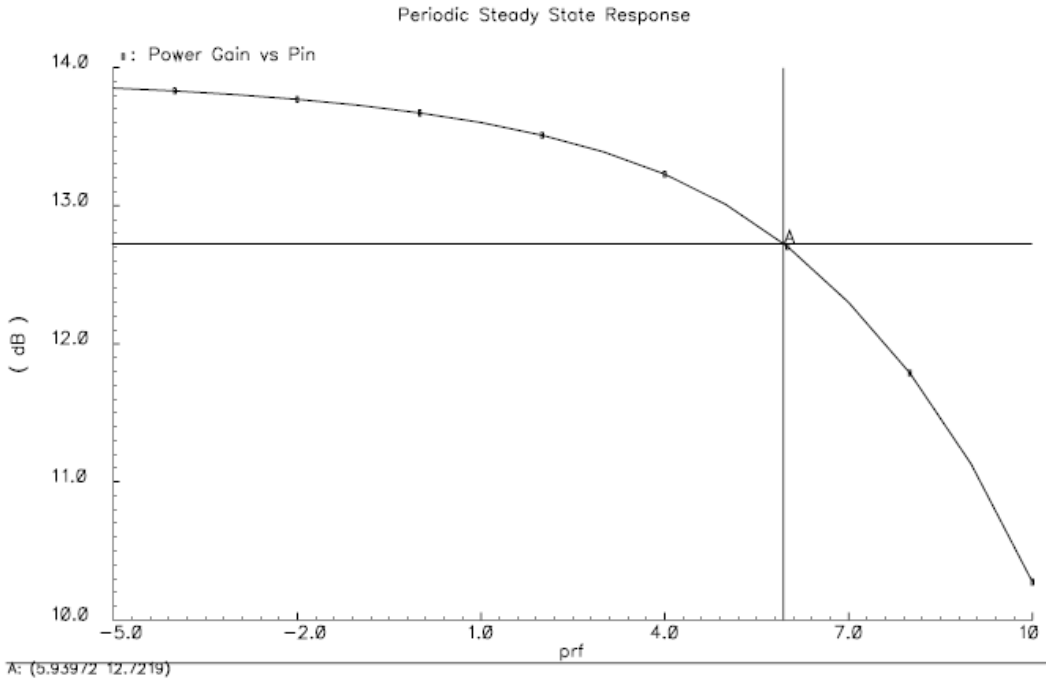


Figure 3.39 Gain of the schematic circuit

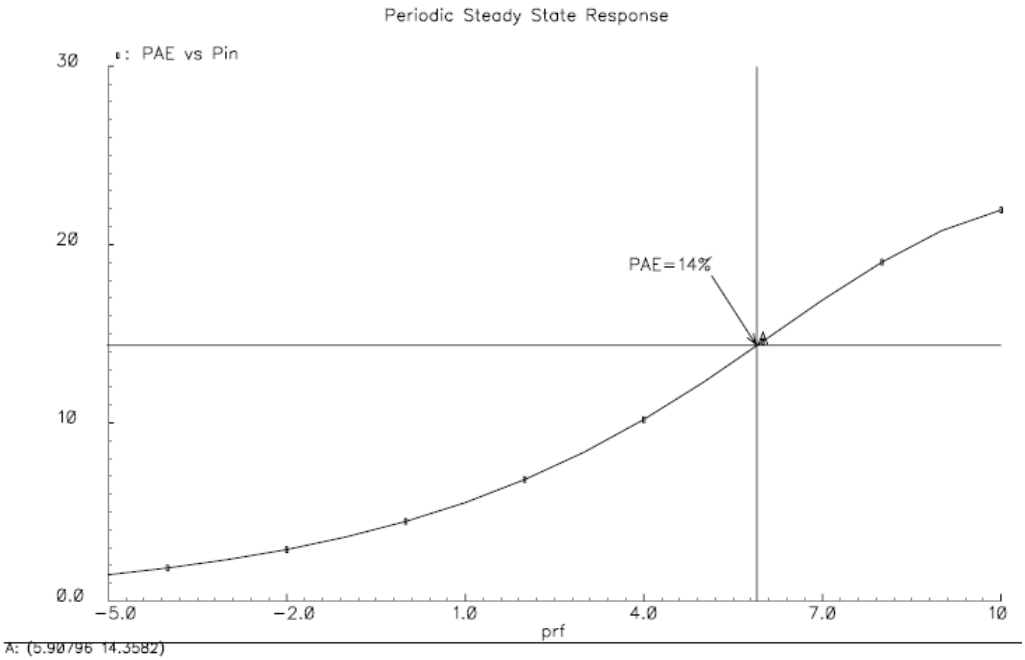


Figure 3.40 PAE

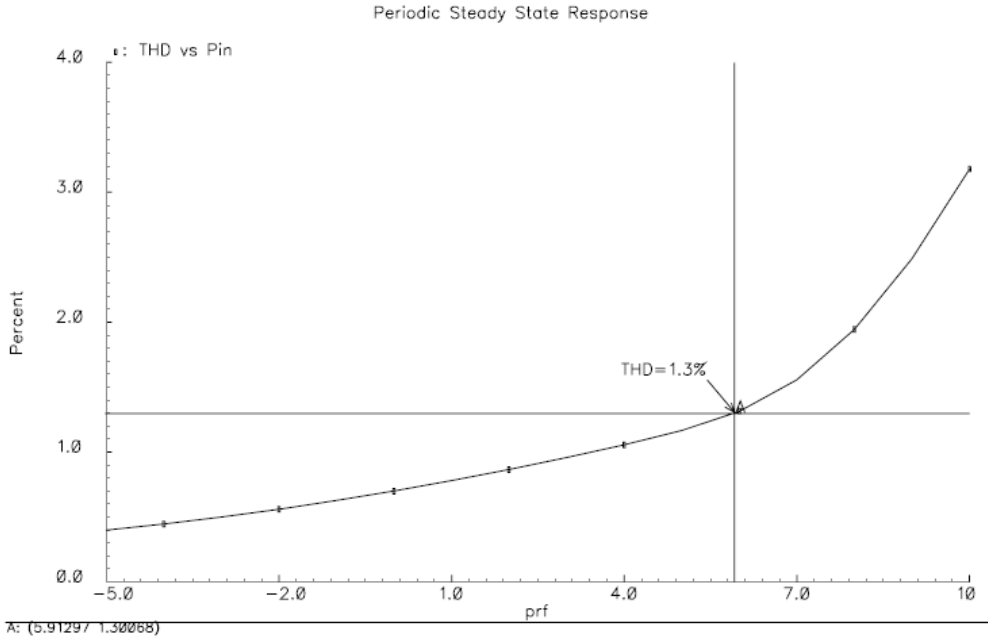


Figure 3.41 THD

3.5 Layout Design

The last step of design of power amplifier is creating the layout of the circuit. Figure 3.37 will be the reference for the layout. For example the ground pins have to be taken into account for the passive components like the ones in the schematic.

The layout can be seen in Figure 3.42. Spirals are chosen to get the closer value to the inductors in the circuit. In the layout, from the lower to higher metal layers, Metal1 is seen in blue, Metal2 is white, Metal3 is yellow and Metal4 is green. The spirals are defined in the highest layer Metal4 to get the most accurate inductance values. But the connectors of these components are in Metal3.

In the layout, the biggest components are the spirals as seen in the figure. So, the components are located according to the placing of spirals. Three parallel transistors are used in one stage and two parallel capacitors are used in the matching circuits near the transistors. The combiner and divider are made from two inductors each. So, these sub-circuits make the layout wider.

The Cmim capacitances are the components defined between Metal2 and 3. Additional capacitances in the layout are used to get the healthy grounding of the circuit. The circuit is open to parasitics in the dc bias nodes. So, as many as possible capacitances are connected between these points and ground. As shown in the layout, they are put on the empty places in the die.

It is important to create the layout as compact as possible. As shown in Figure 3.42, the layout is a square shaped. This is important not to loose any space in the die. The other important point is grounding of the layout. The white frames around the spirals, resistors and capacitances are already defined in the components from the library. These frames have many P-poly diffusion to make the grounding accurately. In the transistor part, this kind of grounding is added manually and as much as possible grounding is obtained. Also most of

the pins in the die are used as a ground pin. The ground frames of the components are connected to some pins directly and they are connected to each other via other pins. While operating, all these pins will be grounded.

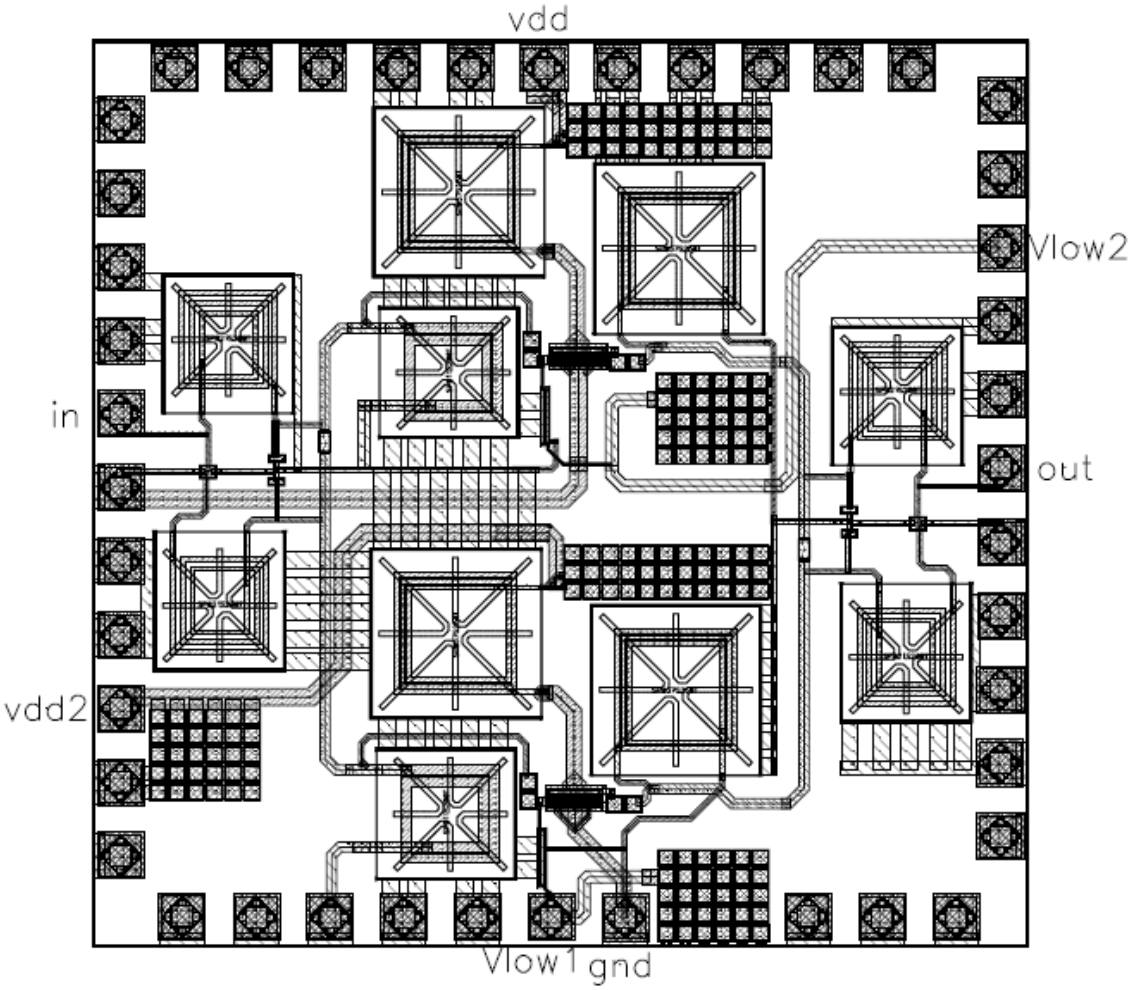


Figure 3.42 Layout of combined power amplifier

According to the schematic simulations done before the layout, the currents in the nodes of the components are known. The amount of the current is the most important thing when the designer decides the thickness of the metal lines. When big amount of current is passing through a line, it must be thick enough not to be damaged during the operation. In addition to this, higher metal layer has a more current capability in the layout. So, Metal4 is used in the high current points in the circuit. For example, in the collector node of the transistor, 17mA is flowing and the thicker Metal4 line is used at this node.

Figure 3.43 shows the exact schematic of the layout of the circuit. Additional capacitances between the bias points and the ground are added in this figure. In Cadence, LVS (Layout vs. Schematic) is needed to be sure that the layout is the circuit that we want, and to pass the LVS, schematic and layout must be exactly the same.

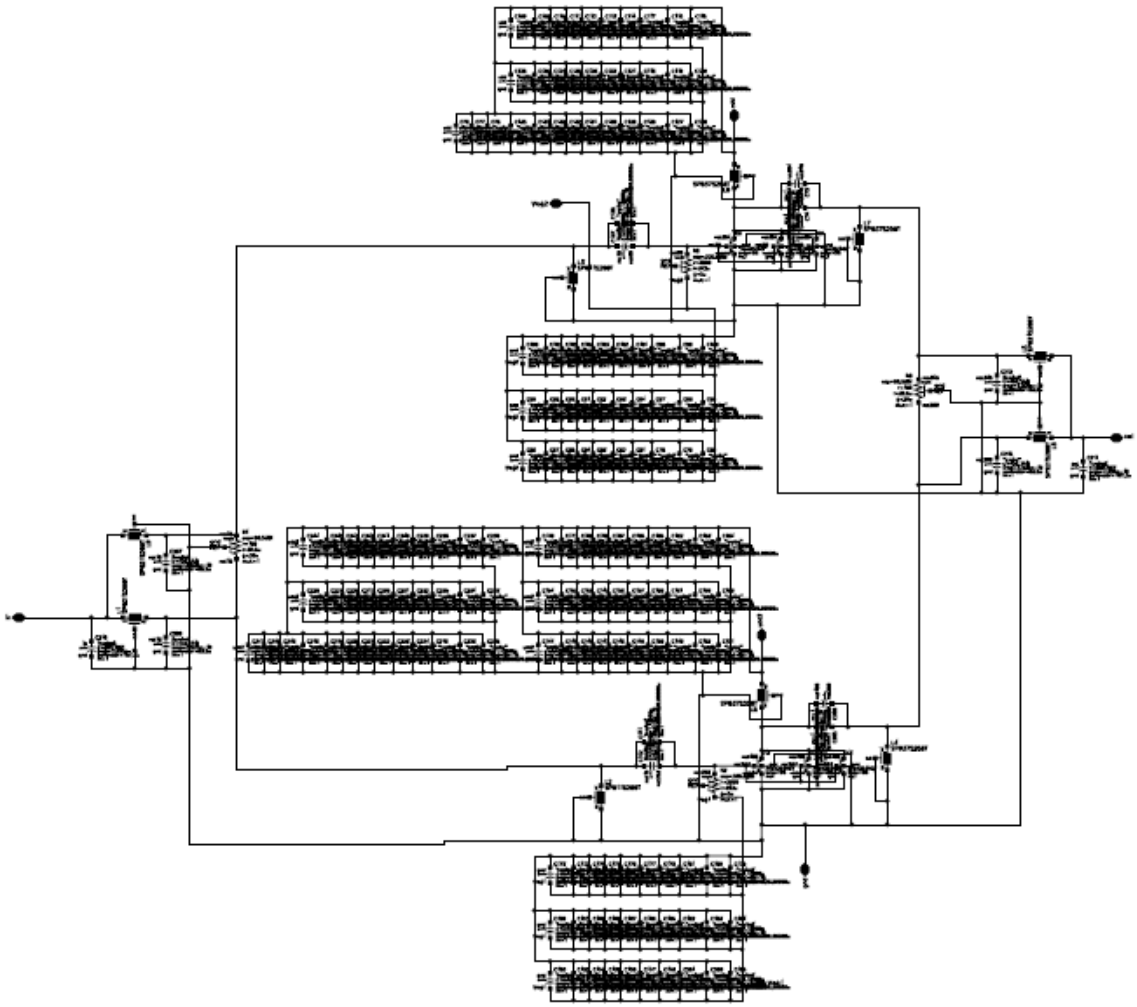


Figure 3.43 Schematic of the layout

After completing the layout, the circuit is extracted to define the additional parasitic capacitances and resistances come from the layout. When the simulations are done with this extracted layout, more realistic behavior of the circuit is obtained. Figure 3.44 is the schematic of the test circuit. The inside of the box component “pa_test” can be chosen from the environment of the simulator in Cadence. The extracted layout is defined and chosen in

this component and post-layout simulations are obtained. These simulation results are the most realistic ones according to the masked, produced and measured die.

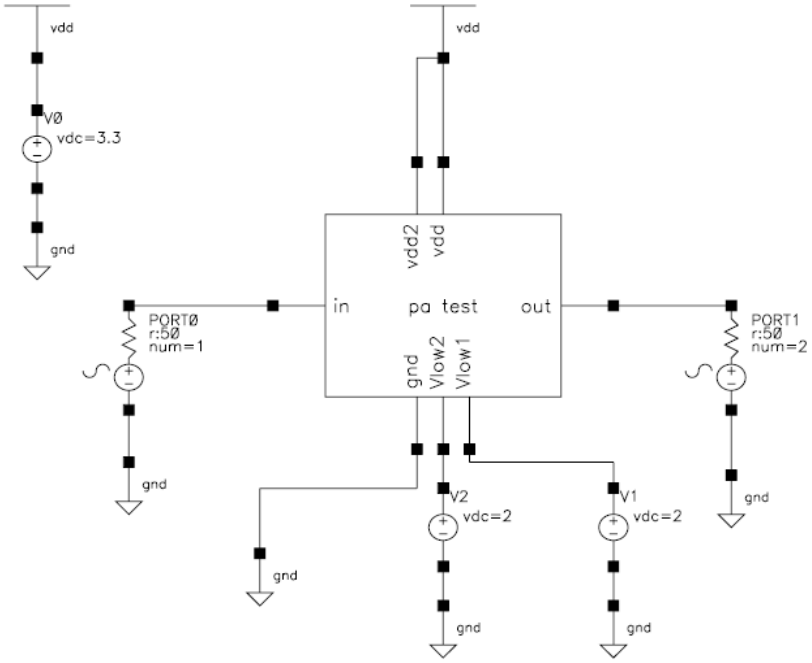


Figure 3.44 Schematic test circuit

Post-layout simulation results are shown between Figure 3.45 - 3.48. In Figure 3.45, input-output power graph is shown. It is simulated at 5GHz. The first order line and the real behaviour of the circuit cross at the 1dB compression point. At the intercept point, input power is 6.7dBm and output power is 17dBm. As explained before, the input power is divided into two (decrease 3dBm) and at the output of the circuit, they are added (increase 3dBm). The power gain in Figure 3.46 is 11.3dB at the compression point which can be also calculated from the previous graph.

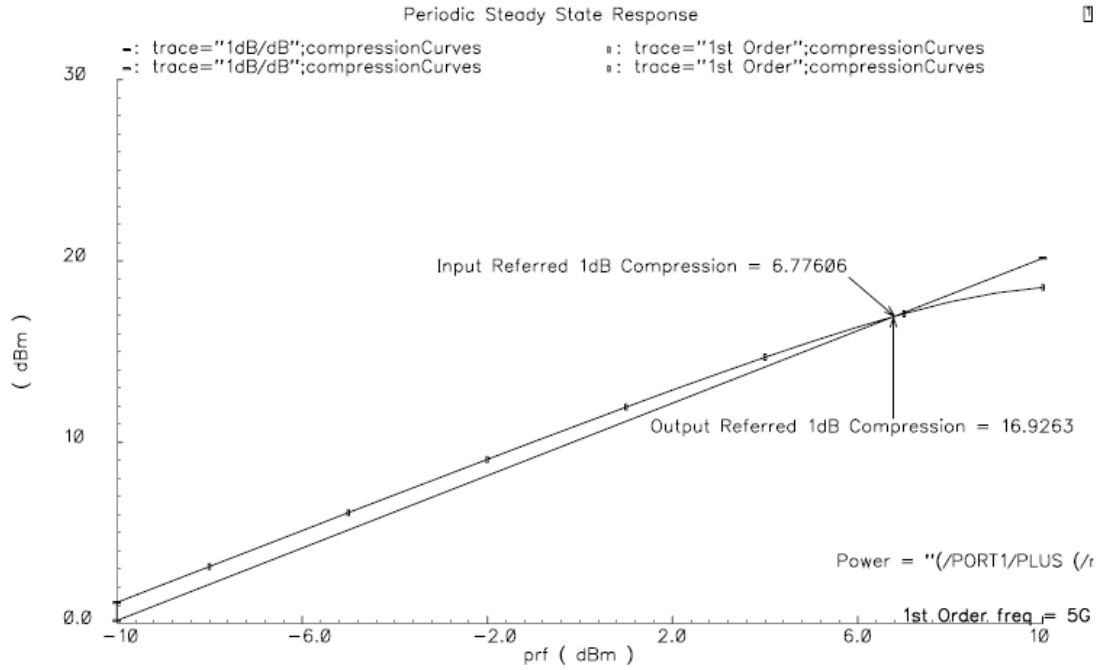


Figure 3.45 Pin-Pout graph of layout

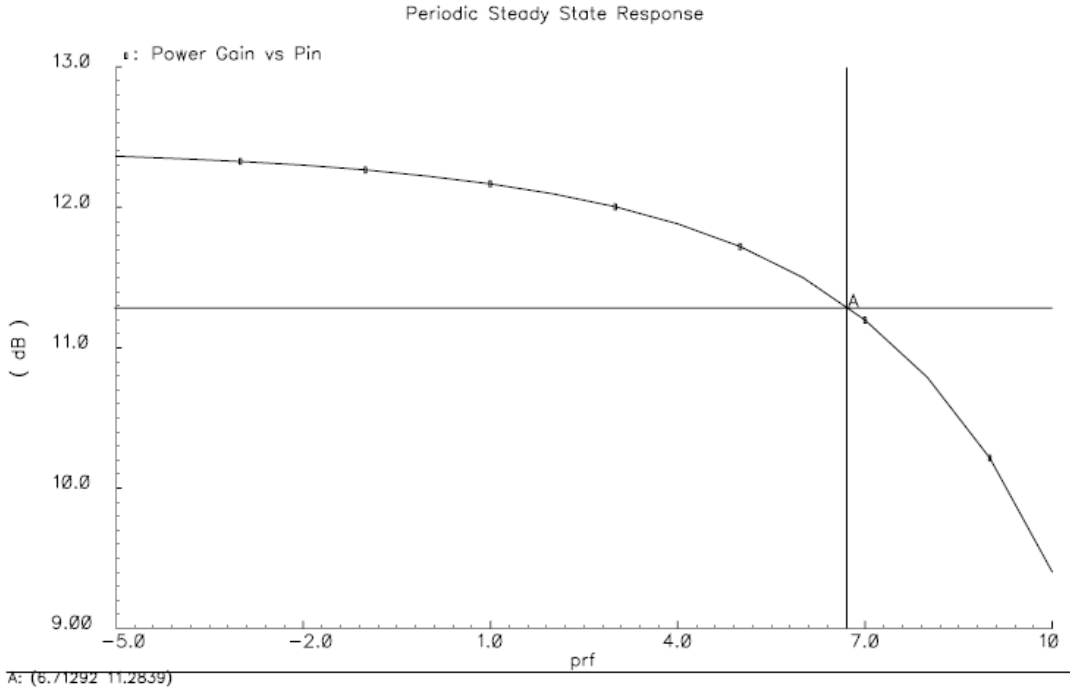


Figure 3.46 Power Gain of layout

Figure 3.47 shows the PAE graph for the amplifier. It is seen that the efficiency is decreased too much according to the single-stage amplifier. At the 1dB compression point, PAE is 13%. It is known that Class-A amplifier is the one that has the lowest efficiency and that is one reason of this result.

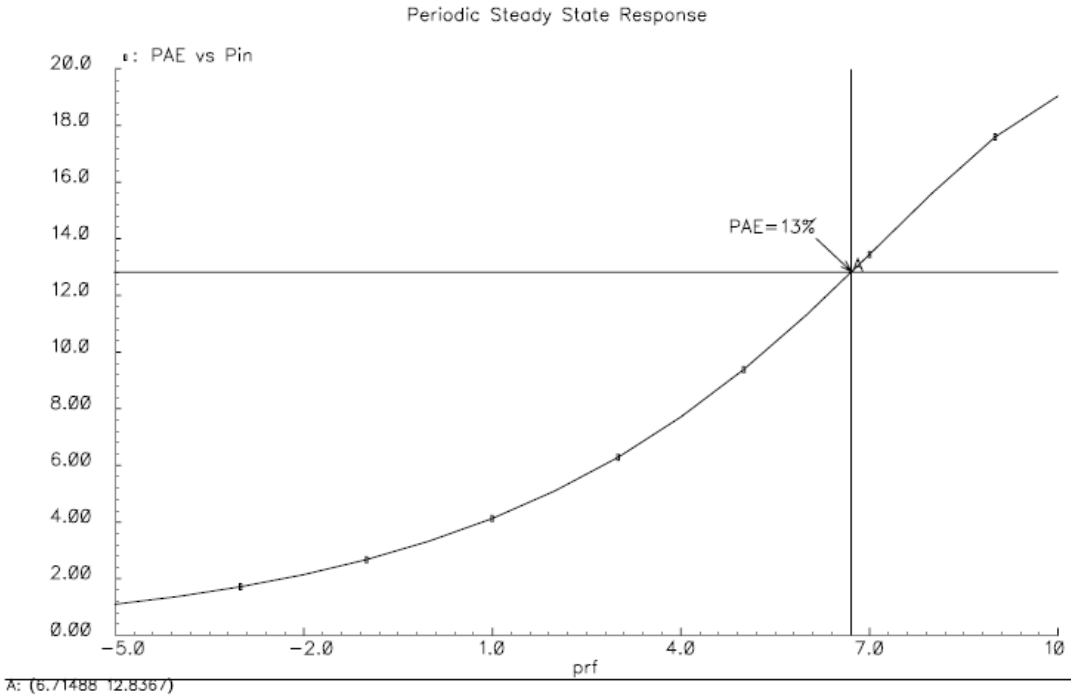


Figure 3.47 PAE

The last simulation result of the circuit is THD vs. Input power shown in Figure 3.48. It is seen that the value is 0.9% at the compression point. In the schematic simulations, its value was higher. This means THD is one of the advantages of a combined power amplifier compared to single-stage amplifier.

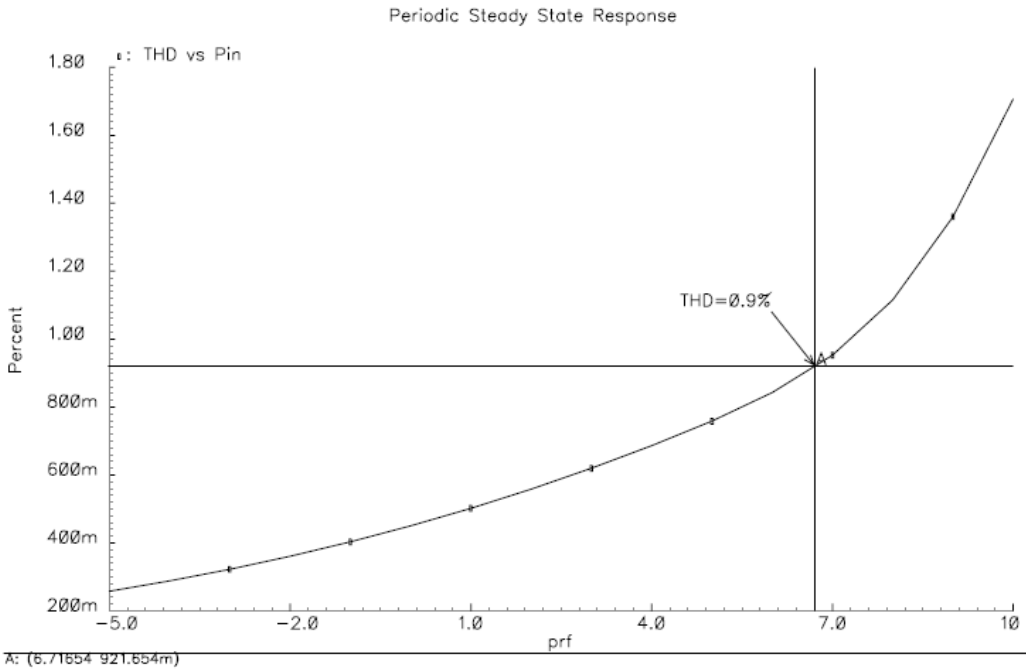


Figure 3.48 THD

As another lumped-element power combining study, Martin [17] used GaAs technology based on an extended resonance technique. In inductively coupled two-device amplifier, Pout is around 20dBm when Pin is 9dBm at 0,8-1MHz range. In a four-device amplifier, the performance of PA is more dependent to Q of the inductor.

Finally, all the simulation results can be summed up in the below table.

	Single-Stage PA with real models	Combined PA	Combined PA with real models	Post-Layout Combined PA
Pin [dBm]	1,6	0	5,9	6,7
Pout [dBm]	15	17	17	16,9
PAE [%]	18	14	14	13
THD [%]	6,3	2,5	1,3	0,9

Chapter 4

4 Conclusion

In this thesis, two single-stage power amplifiers are combined using AMS 0.35μm SiGe BiCMOS technology. The design is based on IEEE 802.11a standard which means 5GHz operating frequency. In ADS simulations, 15dBm output power is obtained from the single-stage amplifier when 1dB compression point for input is -3dBm. PAE is 20% and gain is 18dB. When the simulations are performed in Cadence environment with real components, the results are slightly different. 1dB compression point increases to 1.5dBm value and output power at this point is again 15dBm. The linear region that the circuit can work properly has decreased. But PAE remains the same in this simulation. This means designer obtains different results frojm these two simulators.

As a next step, power combiner is used in the PA. The total input power of the circuit at 1dB compression point is 5.9dBm and Pout is 17dBm. The disadvantage of this circuit is PAE which decreases to 14%. If two kinds of circuits are compared, THD is improved in the combined one. It decreases from 6.3% to 2.5% according to parametric sweep simulations.

The layout is also drawn for the combined amplifier. Schematic simulations are repeated with real models of components and post-layout simulations are performed. Two of them are also compared. Fine grounding of the layout prevent the decrease in post-layout. The simulation results are slightly different from each other.

It is seen that combining two power amplifiers can have some advantages. The linear operation region is increased which is an advantage for the designer. Higher output power can be obtained in the combined circuit. In single-stage amplifier, it is limited and high Pout can not be obtained although input power is increased. Also THD value is decreased according to the single-stage one. The simulation results show that combining technique with passive components can be used in the power amplifier design.

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