REALIZATION of READOUT INTEGRATED CIRCUIT (ROIC) for an ARRAY of 288x4, N-on-P type HgCdTe LONG WAVE INFRARED DETECTORS

by

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Abstract

Infrared (IR) imaging systems are used in a variety of applications from biomedical to astronomic and strategic imaging. Modern military missile guidance and surveillance systems also incorporate infrared imaging systems. The most critical component of an infrared imaging system is the focal plane array (FPA), a key assembly of detectors and readout electronics to carry out the function of infrared to electrical signal conversion. As in all sensor networks, extraordinary care must be given to both the detector design and readout integrated circuits, to obtain a high performance and durable system. In IRFPAs, detectors set the operation wavelength, readout circuit area and operation temperature. However many of the system performance parameters such as signal to noise ratio (SNR), linearity, input referred noise level, dynamic range, are set by the readout integrated circuit (ROIC).

First generation of IR imaging systems incorporated single detector, or a fewer number of detectors. Higher frame rate and resolution requirements brought up the scanning type of FPAs where a scene is scanned constantly to create a 2D electronic image by a single array of detectors. Scanning type FPAs, with higher frame rates, started to replace staring arrays, with the maturing of detector processing technology and allowing integration of thousands of

functioning detectors (pixels) on a single substrate, with smaller pitches. However, scanning type arrays are attractive due to their lower cost.

In this thesis, design of a CMOS readout integrated circuit for an array of 288x4, n-on-p type HgCdTe long wave infrared detectors is presented. ROIC input preamplifier is current mirroring integration type due to low input impedance requirement. In order to increase SNR, time delay integration (TDI) on 4 detectors is applied with a super sampling rate of 3. ROIC has additional features of bidirectional TDI scanning, dead pixel deselection, automatic gain adjustment in response to pixel deselection, in addition to programmable four gain settings (up to 2.58pC storage), and programmable integration time. ROIC has four outputs with a dynamic range of 2.8V (from 1.7V to 4.5V) and input referred noise of 2989 electrons for an area of 13mm^2. Two clocks: master clock and integration clock are required in order to operate the ROIC. Integration clock sets the integration time and adjust frame rate. Master clock maintains synchronization and can be adjusted up to 5MHz. ROIC can be programmed through both serial and parallel interface with full functionality but pixel deselection being allowed only in serial interface mode.

288x4, P üzeri N türü HgCdTe UZUN DALGA BOYU KIZILÖTESİ DEDEKTÖR DİZİNİ için ENTEGRE OKUMA DEVRESİNİN GERÇEKLEŞTİRİLMESİ

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Özet

Kızılötesi görüntüleme sistemleri biomedikal uygulamalardan, astronomik uygulamalara ve stratejik görüntüleme sistemlerine kadar geniş bir uygulama alanına sahiptir. Modern askeri füze güdüm sistemleri ve gözetleme sistemleri de kızılötesi görüntüleme sistemleri içermektedir. Kızılötesi sistemlerin en önemli bileşeni, kızılötesi ışımayı elektriksel işarete dönüştüren, dedektör ve dedektöre ait okuma devresinden oluşan odaksal düzlem dizileridir (FPA). Bütün sensor devrelerinde olduğuu gibi işlevsel, dayanıklı bir system tasarımı için, hem dedektör hem de okuma devresinin tasarımına özel dikkat gösterilmelidir. Bu sistemlerde, dedektörler çalışma dalga boyunu, okuma devresi alanını ve çalışma sıcaklığını belirlerken, okuma devreleri de gürültü işaret oranı (SNR), doğrusallık, girişe yansıtılmış gürültü seviyesi, dinamik aralık gibi performans parametrelerini belirlerler.

Birinci nesil kızılötesi görüntüleme sistemleri tek ya da sınırlı sayıda dedektör içermekteydi. Yüksek çerçeve hızı ve çözünürlük gereksinimleri iki boyutlu görüntü oluşturmak için bir dizi dedektörün kullanıldığı taramalı sistemleri ortaya çıkarmıştır. Dedektör işleme teknolojilerinin gelişmesi ile daha çok sayıda çalışır dedektör aynı substrata daha küçük pixel alanlarıyla üretilebilmiştir ve böylece taramalı diziler, daha yüksek çerçeve hızına sahip

hareketsiz dizilerle değiştirilmeye başlanmıştır. Bununla birlikte taramalı diziler halen daha ucuz olmaları itibariyle cazip bir tercih olmayı sürdürmektedir.

Bu tezde p katman üzerine n tabakayla oluşturulmuş, yüksek dalgaboyunda çalışan, 288x4 HgCdTe kızılötesi dedektör dizisi için CMOS okuma devresi (ROIC) tasarımı gösterilmektedir. Tasarlanan okuma devresi dört eleman üzerinde üçlü örnekleme ile zaman geciktirmeli toplama (TDI), hatalı piksel ayırma ve bu ayırma işlemine göre otomatik kazanç ayarlama, dört ayarlanabilir giriş kazanç ayarı ve ayarlanabilir entegrasyon süresi özelliklerine sahiptir. Okuma devresinin dinamik aralığı 2.8 volttur (1.7-4.5V), toplam kırmık alanı 13mm^2 dir ve girişe yansıtılmış gürültü seviyesi 2989 elektrondur. Okuma devresinin çalışması ana saat işareti ve entegrasyon saat işareti gerekmektedir. Entegrasyon saati çerçeve hızını ve entegrasyon süresini belirler. Ana saat ise senkronizasyonu sağlar ve 5MHz'e kadar çıkabilir. Okuma devresi seri ya da parallel modda programlanabilir.

Acknowledgements

I have started to work on this project in 2006 as an undergraduate student. I had neither a prior tape-out experience nor the vision to see how vast designing a circuit like this one was. Today, while ending my MSc study in Sabanci University, I feel technically confident, experienced and ready to face upcoming challenges. All these are possible today with the help of my professors, co-workers on this project and friends aside from the hard work and late nights across the stationary view of a workstation. I would like to thank to those people here.

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CHAPTER 1 INTRODUCTION

1.1 Introduction

Infrared (IR) imaging systems find a variety of applications in civil and military applications such as medical imaging, space and astronomy applications, surveillance, infrared search and track systems, missile guidance and forward looking infrared systems (FLIR). An infrared imaging system in general, is composed of optics, a scanner, a detector and readout electronics that may be enclosed in a cooler, to carry out IR generated signals, and further signal processing blocks as shown in Figure 1.1.

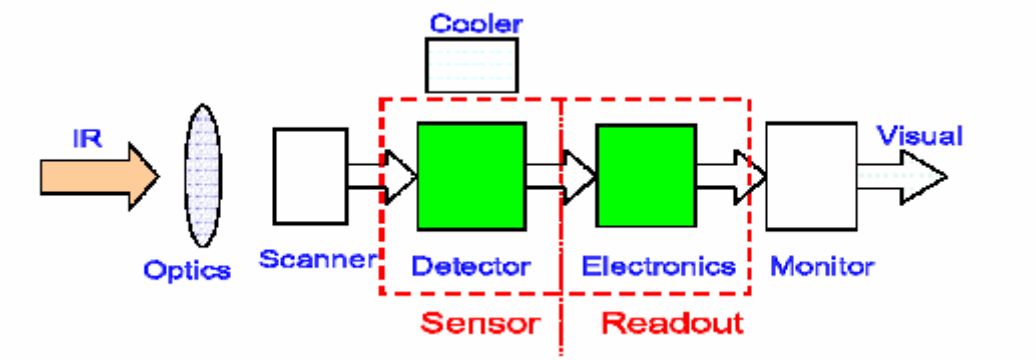

Figure 1.1: General architecture of an infrared imaging system

In applications where high resolution and sensitivity is demanded, large integrated set of detectors are required. Since 1970, research on highly integrated set of detectors and their multiplexers produced infrared focal plane arrays (IRFPA); an array of detectors and its readout electronics. Compared to the conventional discrete infrared detector configurations, IRFPAs has two major advantages: they provide an economical method for high density packaging of detectors and they allow signal processing to take place on the focal plane. Both of these advantages permit design tradeoffs of system parameters such as smaller optical apertures, reduced spectral bandwidths, and faster frame rates [1].

Readout electronics and detectors are in general built on different substrates and are flip chip bonded through indium bumps, in order to select optimum substrate for both, as shown in Figure 1.2 [2]. Usually an off package ADC, is involved before further signal processing. Majority of the detectors used in FPAs are mostly mercury cadmium telluride alloys (HgCdTe or MCT) and readout integrated circuits are charge coupled devices or CMOS circuits, with trend moving towards CMOS ROICs.

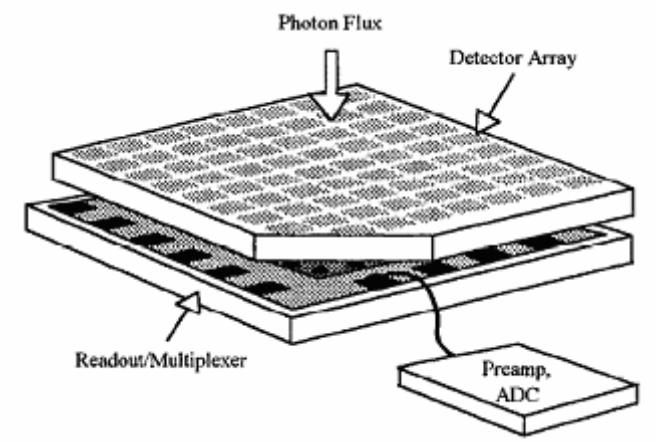

Figure 1.2: Representation of FPA, detector array and multiplexer [2]

Focal Plane Arrays (FPA) can be classified according to their substrate and readout circuits being on the same substrates as monolithic and hybrid. Monolithic approach involves some of the signal processing on the detector substrate, however mature applications of this approach are limited to silicon based Schottky-barrier detectors [3]. Hybrid approach, as shown in Figure 1.3 involves that detectors and readout are fabricated on their optimum, different substrates and are than connected together by use of indium bumps with flip chip bonding method or loophole method (also called via-hole method). In both methods, Aside from optimum substrates selection, larger signal processing area can be obtained with the hybrid approach.

In the flip chip bonding method, a planar readout multiplexer is aligned with the detector array; a single contact from every detector to the readout is formed as in Figure 1.3.(a). Contacts can be formed in two ways; either indium bumps are formed on both detectors and readout chip or indium bumps are only formed on readout chip. Finally, connection is achieved by heating or by applying mechanical force. Loophole method differs from flip chip bonding by the detectors being processed after readout chip and detector substrate are connected by a glue as in Figure 1.3.(b). Following detector processing holes are created by ion milling, and indium bumps are inserted for connection with readout array.

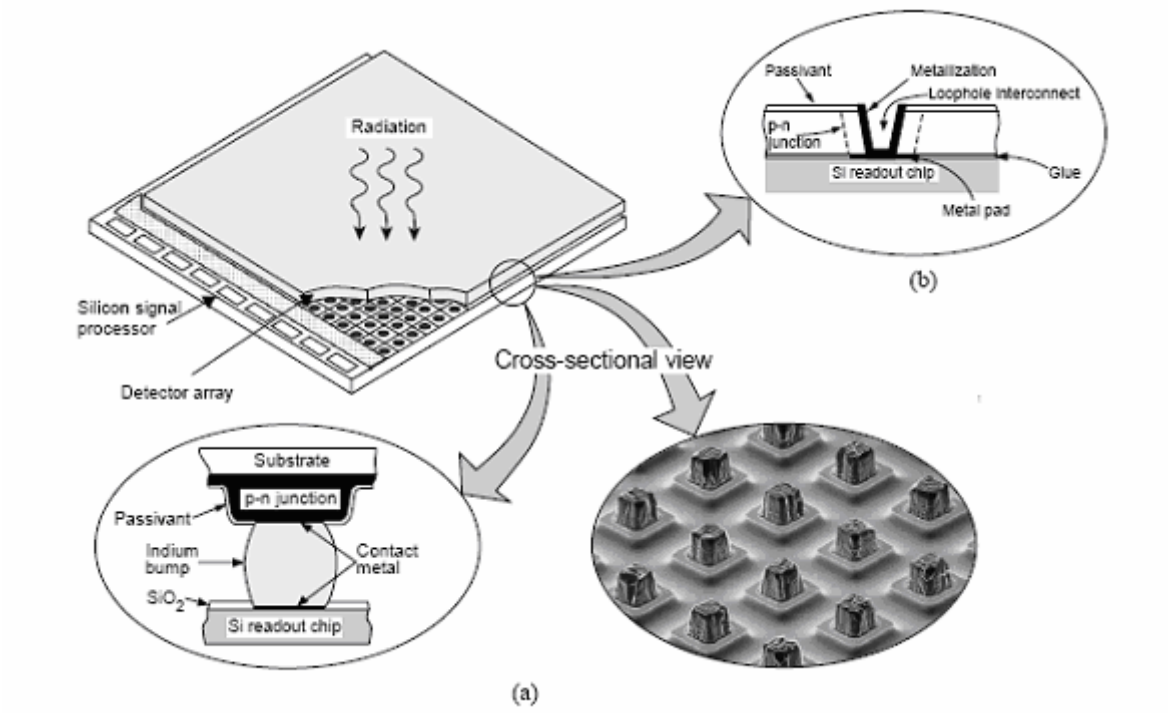

Figure 1.3: Hybrid IRFPA with independently optimized detector and readout (a) indium bump technique, (b) loophole technique [4]

IR detectors mainly focus on the spectrum range in terms of wavelength as 3-5 μm (mid wave infrared, MWIR) and 8-14 μm (long wave infrared LWIR) due to the high atmospheric transmission and maximum emissivity of objects is achieved around 10 μm [4]. Detectors are classified in two as their mode of detection, as thermal detectors and photon detectors. Further classification can be done according to the detection schemes; thermal detector types can be given as pyroelectric, bolometers and thermoelectric effect devices; intrinsic, extrinsic and quantum well, Schottky barrier devices, can be listed as photon detector types.

Region (abbreviation)	Wavelength range (μm)
Near infrared (NIR)	0.78–1
Short wavelength IR (SWIR)	1–3
Medium wavelength IR (MWIR)	3–6
Long wavelength IR (LWIR)	6–15
Very long wavelength IR (VLWIR)	15–1000

Table 1.1: Division of infrared radiation [5]

Thermal detectors rely on the change of device temperature under IR illumination. Change in device temperature causes device's physical or electrical properties to change, forming the

detection mechanism. In theory, these devices are not wavelength selective; rather they depend on the power of the radiation. Thermal detectors operate at room temperature and easy to make and cheap however, they have average sensitivity and slow response times due to the time required for heating of the device [3].

Photon detectors are semiconductor devices that create an output signal in response to the change of electric energy distribution in case of a radiation contact with an electron at the device [3]. These devices operate wavelength selective, has very good sensitivity (high signal to noise ratio) and has very fast response times. However these advantages come with a cost of cryogenic cooling requirement, mostly down to 77K, in order to prevent thermal generation of charges in the device. Uncooled detectors are quite noisy, and the cooling requirement makes the use of photon detectors expensive.

A comparison of IR detector types, both thermal and photon, is represented in [3] and also shown in Table 1.2. For infrared detection, the most suitable and preferred photon detector material is HgCdTe, even its disadvantages of harsh processing issues as its toxiticity and high vapor pressure at melting point [4]. However certain advantages of HgCdTe detectors make their use inevitable as the primary material for photon detectors. First by properly selecting the amount of CdTe and HgTe, spectral response of detector can be set to a range of 1-25 μm. HgCdTe detectors, are direct bandgap materials and being relatively thin, can absorb high amount of energy. A thin substrate generates lower noise. Finally lattice matched substrates for epitaxial growth is available for HgCdTe detectors for total range of IR spectral range, posing a major advantage over other detector materials [3] [4].

Detector type			Advantages	Disadvantages
Thermal (thermopile, bolometers, pyroelectric)			Light, rugged, reliable, and low cost Room temperature operation	Low detectivity at high frequency Slow response (ms order)
Photon	Intrinsic	IV–VI (PbS, PbSe, PbSnTe)	Easier to prepare More stable materials	Very high thermal expansion coefficient Large permittivity
		II–VI (HgCdTe)	Easy bandgap tailoring Well developed theory & exp. Multicolour detectors	Non-uniformity over large area High cost in growth and processing Surface instability
		III–V (InGaAs, InAs, InSb, InAsSb)	Good material & dopants Advanced technology Possible monolithic integration	Heteroepitaxy with large lattice mismatch Long wavelength cutoff limited to 7 μm (at 77 K)
	Extrinsic (Si:Ga, Si:As, Ge:Cu, Ge:Hg)		Very long wavelength operation Relatively simple technology	High thermal generation Extremely low temperature operation
	Free carriers (PtSi, Pt_2Si, IrSi)		Low-cost, high yields Large & close packed 2-D arrays	Low quantum efficiency Low temperature operation
	Quantum wells	Type I (GaAs/AlGaAs, InGaAs/AlGaAs)	Matured material growth Good uniformity over large area Multicolour detectors	High thermal generation Complicated design and growth
		Type II (InAs/InGaSb, InAs/InAsSb)	Low Auger recombination rate Easy wavelength control	Complicated design and growth Sensitive to the interfaces
	Quantum dots	InAs/GaAs, InGaAs/InGaP, Ge/Si	Normal incidence of light Low thermal generation	Complicated design and growth

Table 1.2: Comparison of detectors [4]

Photovoltaic and photoconductive HgCdTe detectors are available and applied successfully to ROICs. Photovoltaic (PV) detectors are basically pn junction devices, producing current of an incident photon with energy higher than the band gap of the junction. In most ROICs in order to benefit from the large shunt impedance, and reduce power consumption, PV detectors are operated at almost zero bias. Photovoltaic detector process is a challenging, but due low power advantage, is a quite attractive one. Today, IRFPAs are dominated by photovoltaic detectors, most of which are HgCdTe alloys.

Photoconductive (PC) detectors are semiconductor devices with a detection mechanism of changing conductance under IR illumination. In case of an incident photon, either an electro-hole pair is generated (intrinsic semiconductor) or majority carriers are activated (extrinsic semiconductors) [6]. PC detectors are operated through a constant bias thus; power consumption is a problem, compared to PV detectors, making PC detectors not favorable for large array applications.

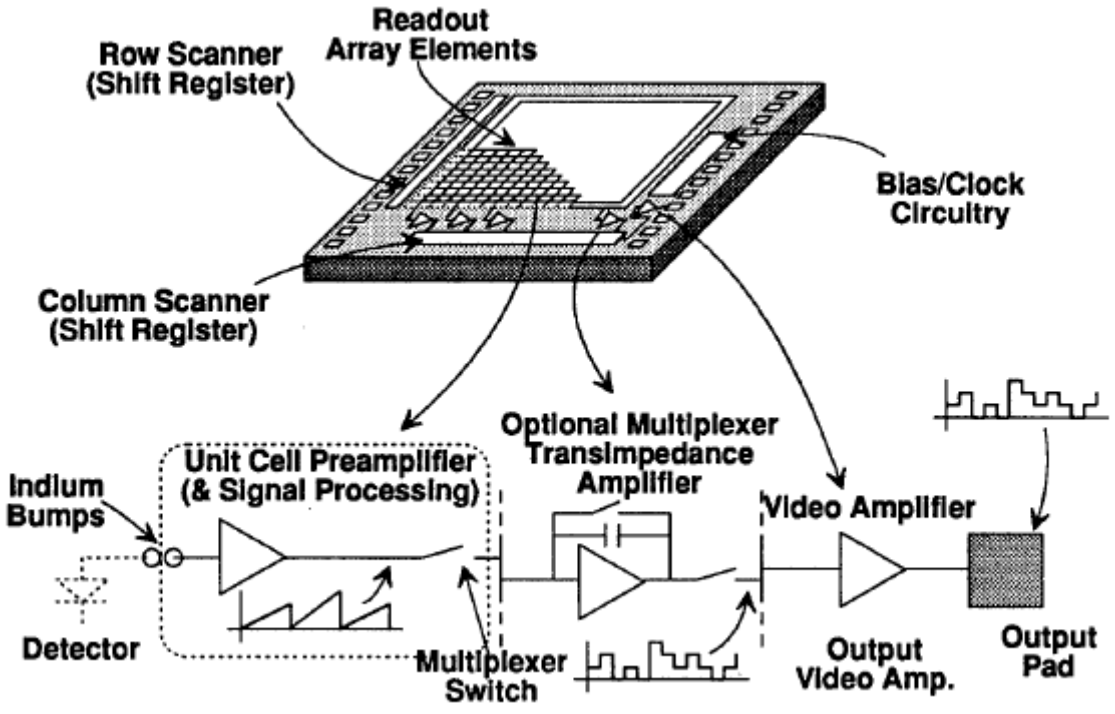

Figure 1.4: Generic staring type ROIC. ROIC includes amplification and signal processing. [7]

ROICs are sensor interface blocks where photocurrent to immediate voltage conversion on an integration capacitor for a certain integration time is held. In Figure 1.4, a generic view of ROICs is represented. Detectors are connected to the ROIC by indium bumps with flip chip bonding method. For every single element in FPA there is a unit cell preamplifier. Unit cell

can be direct injection, buffered direct injection, current mirroring direct injection, or any other topology, selected according to the detector's shunt impedance, noise, linearity, and power consumption requirements of the readout circuit. A transimpedance amplifier may be required according to signal processing used. Finally, a video amplifier or output buffer is employed. Additionally, ROICs can have on chip analog to digital converters (ADC) and on chip clock generators.

Most important parameter of an ROIC is the signal to noise ratio. Most ROICs have input referred noise levels less than the detector itself. Largest possible dynamic range is desired in order to maximize the saturation level of the signal. Since photon detectors operate at cryogenic temperature, power consumption of the circuit should be minimized in order to reduce cooling requirements. A careful input preamplifier selection must be made according to the detector properties (shunt impedance, capacitance) as well as aimed radiation conditions of the detector array (flux level), since input preamplifier sets linearity and efficiency of ROIC along with dynamic range. These requirements are discussed in [7] as shown in Table 1.3.

Major Readout Performance Parameters	Related System Parameter or Interface Impact	Comments
NEC (noise equivalent charge)	Sensitivity	Minimized to enhance SNR
Power dissipation	Cooldown time Life Weight	Limited cryogen/cooler life Cryogen weight/cooler size
Dynamic range	Maximum saturation signal	Loss of signal
Crosstalk	System MTF (resolution) Blooming of saturated elements	Element to element
Frequency response	System MTF (resolution) Latent images	Often related to crosstalk
Input impedance	Signal linearity Noise	Detector bias changes with signal Loss of optimum detector bias
Linearity reliability	Calibration Instrument life	Proper identification Confidence of success
Gain	Sensitivity	Signal amplified above system noise floor
Output video driver impedance	Sensitivity MTF	EMI from environment crosstalk between multiplexed elements

Table 1.3: Relationship between readout performance parameters and system requirements [7]

Circuit architecture of ROICs also depends on the type of FPA. FPAs can be staring or scanning type. Scanning arrays are first generation FPAs incorporating a single column of

detectors. Four or seven columns of detectors are also developed with time delay integration functionality. The bottle neck of developing huge number of functioning devices led to the first generation FPAs to be linear, scanning type arrays. In scanning type arrays, only a single column of image is produced at a single frame. An optic scanner scans the scene continuously to create a full image output. ROICs for scanning type arrays operate at lower frame rates and lower spatial resolution; super sampling is incorporated for increasing the spatial resolution.

The second generation of FPAs is the staring arrays incorporating thousands of elements up to 2048x2048. Having higher number of elements, these FPAs have much higher field of view than scanning ones. These arrays operate at higher frame rates and have better spatial resolution. Also as in [8], trend is to operate FPA at higher temperature as 110K, for a better performance.

Finally it is important to mention the process technologies ROICs are built. First IRFPA readouts were made by CCD technology. Until that, only way to create a sensitive, high resolution system is through configuring a large set of detectors with each detector being connected to a single wire (and probably an individual preamplifier). Also these detectors and readout elements are all required to be packaged in a small dewar [1]. This would be a difficult task with dewar being quite large, as well as harsh cooling requirements, due to higher power consumption.

Although CCD technology enabled high integration, IRFPAs benefited from the mature CMOS technology. Advantages of CMOS IRFPAs are based on versatility and compactness. CMOS based readouts can cover operating ranges down to 10 Kelvin. High performance low noise amplifiers are available through CMOS technology. Finally, through low voltage operation compared to CCD technology, CMOS technology has proven very successful for designing readout integrated circuits.

1.2 Motivation

As mentioned in the previous section, first generation of IR imaging systems incorporated single detector, or a limited number of detectors. High frame rate and resolution requirements brought up the scanning type of FPAs where a scene is scanned constantly to create a 2D image by a single array of detectors. Staring arrays allow high frame rates and better resolution. However staring arrays are expensive and it is hard to integrate large set of detectors. Hence scanning type arrays are attractive choices due to the above mentioned

advantages. It is easier to build scanning arrays due less number of elements being incorporated. Scanning arrays are also cheap with all advantages of integrated array technology.

In this thesis, design of a CMOS readout integrated circuit for a scanning array of 288x4 elements of n-on-p type HgCdTe detectors for long wave infrared spectrum is represented. Designed readout ROIC structure includes four elements time delay integration (TDI) functioning with a super sampling rate of 3, bidirectional TDI scanning, dead pixel deselection, automatic gain adjustment in response to pixel deselection, besides programmable four gain settings (up to 2.58pC storage), and programmable integration time. ROIC has four outputs with a dynamic range of 2.8V (from 1.7V to 4.5V) and input referred noise of 2989 electrons for an area of 13mm^2. Organization of the thesis is given in the next section.

1.3 Organization of Thesis

In Chapter 2, scanning type ROIC building blocks are discussed. First, most of the preamplifiers already discussed in the literature, are explained and compared in terms of their injection efficiency, linearity, input referred noise level and power consumption. Specific applications of each preamplifier are discussed. Next a noise reduction technique, widely known and applied to scanning type of ROICs, time delay integration (TDI) is announced. Application of TDI with super sampling rate of three on four detectors is shown. Possible implementation methods are also addressed and compared in terms of trade offs between area and power consumption. In the last section of the chapter additional ROIC features such as pixel deselecting in case of a malfunctioning detector, automatic gain adjustments and test mode operations are explained.

In Chapter 3, implementation of individual blocks discussed in Chapter 2 is explained. First requirements for the specific ROIC 288x4 HgCdTe array are given as well as the detector properties. Next, input preamplifier selection as current mirroring integration is introduced. Implementation of preamplifier together with input capacitor selection and variable gain application is discussed. In the next section, implementation of the TDI according to the chosen topology is shown. Implementation of TDI amplifier is represented as well. Due to TDI implementation some offset is added to the output. Following section illustrates implementation of an offset cancellation block, which also reduces charge injection and clock

feedthrough effects. Output buffer is also defined. Finally control block design to operate the ROIC, as well as required user interface is explained.

Chapter four includes simulation and experimental results. First, measurement results from a 1x4 ROIC is given. Then simulation results of 288x4 ROIC are represented by a 72x4 sub block. Results are shown for minimum, nominal and maximum input current levels for voltage levels at the integration capacitors, at the TDI amplifier output, at the output of offset cancellation stage and at the output buffer.

Finally, in chapter five, conclusions of this study are provided, problems are addressed and future study is discussed.

CHAPTER 2 LINEAR ROIC BUILDING BLOCKS

2.1 Introduction

All ROICs, scanning or staring type, involves use of a preamplifier, also named the unit cell as the immediate interface circuit. As in all sensor readouts, most of the performance parameters are strictly dependent on this input preamplifier, especially; input referred noise, injection efficiency, dynamic range and linearity are key performance parameters of ROIC are set through unit cell.

Second, all linear ROICs employ signal processing such as correlated double sampling or time delay integration. Correlated double sampling (CDS), is used in sample and hold circuits in order to store an amplifier noise, and subtract it from another set of results. Time delay integration (TDI) is another method used to increase signal to noise ratio (SNR) through creating an output by adding multiple measurements from a set o detectors.

Most linear ROICs apply super sampling with TDI, to effectively increase spatial resolution of the image, without increasing the number of elements on the FPA. Super sampling is realized by setting certain scanning steps for a single detector on a row. For example an image is passed through a detector with three steps, results with three data from a single detector, hence a super sampling rate of three.

ROICs employ additional functionalities such as dead pixel deselection, automatic gain adjustment or bypass (test) mode. These functionalities are correlated. By test mode malfunctioning detectors are determined. ROIC is then programmed according to data obtained. During read phase, in case of one or more defected detectors, gain is adjusted so that the effect is not observed at the output.

In this section above mentioned building blocks and signal processing methods are discussed in detail with possible circuit or implementation types. Focus is given to set the key parameters, advantages and disadvantages of each circuit or method and application types each circuit or method is applicable.

2.2 Preamplifiers

Initial conversion from photocurrent to voltage takes place at the preamplifier (unit cell) and. further processing of signal is held in voltage domain. In order this conversion to be accurate, stringent requirements are met by different types of preamplifiers.

First, preamplifiers should have low noise, but in return should not loose the advantage of having low input impedance (hence high injection efficiency) or linearity, which is not the case most of the types. Also these cells must be operable at very low current levels, such as 1nA, in cryogenic temperatures most of the time, due to the cooling requirement of the FPAs. Moreover, since they are the most repeated building block (every detector has one dedicated unit cell) preamplifiers should consume minimal power. Finally, most ROIC incorporates unit cells just under the detector itself; in this case, preamplifiers must fit in area determined by the size of the detector.

There are various different types of preamplifiers in the literature. Most common ones are discussed in this section. In the end, advantages and disadvantages of each topology is given.

2.2.1 Self Integration Preamplifier

Among all ROIC preamplifiers self integration (SI) is the unit cell with the least number of components and has an advantage of being implemented in the minimum area. However SI unit cell is subject to limited dynamic range and causes nonlinearity as the detector bias is varied with the stored charge on the integration capacitor.

The operation of SI unit cell is simple, for a certain IR radiation, photocurrent is accumulated on the stray capacitance as well as parasitics from the line to the multiplexer bus. Additional capacitance to widen the dynamic range is also applicable [7]. For a given frame time integration is done over the stray capacitances and then the multiplexer connects the detector to the transimpedance amplifier where conversion from charge to voltage domain takes place. Depending on the transimpedence amplifier used a reset bus may be required to reset the detector (integrated) voltage to its initial value. The operation type discussed is represented in the following Figure 2.1.

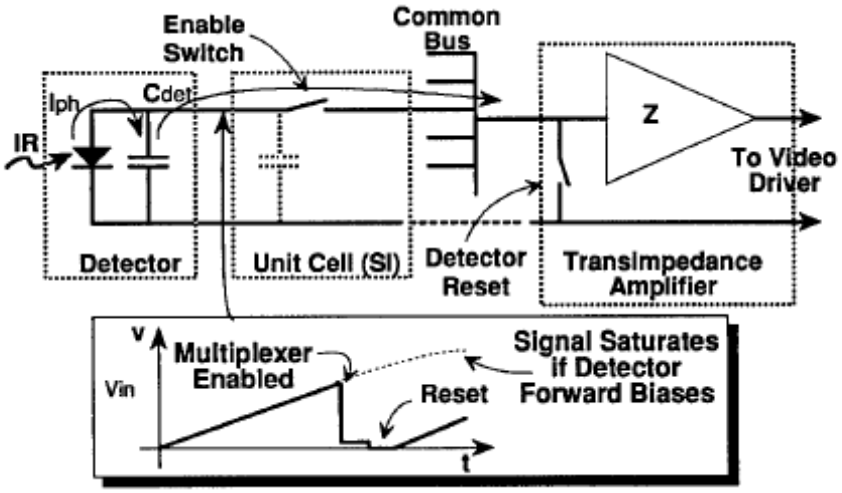

Figure 2.1: Self integrator readout [7]

As seen from the integrated voltage curve, there are two important issues to mention in terms of linearity and dynamic range of SI type preamplifiers. First the voltage over the PV diode is evaluated as:

$$Vout = Z\int I_{ph}xdt + ZQr\,, \qquad \textbf{(2.1)}$$

with Z, being the charge to voltage gain of the preamplifier, I_{ph} is the photocurrent and Qr being the initial charge remained following the reset operation of the PV detector [7]. As the voltage increases the dark current associated with the detector will change resulting nonlinearity for different radiation levels. Further increase of the integrated voltage will forward bias the PV detector limiting the voltage level to the PV detectors on voltage. Hence, the dynamic range of SI is limited to the flat back bias signal excursion of the detector [7].

Finally, in terms of noise contribution, SI unit cell suffers from kTC noise as all switched capacitor circuits as well as detector thermal noise and photon noise. The column multiplexer is also a major contributor to the noise generated although it is outside the unit cell [7]. However, SI is along with direct injection unit cell, is the lowest noise contributing preamplifier. Aside this advantage, its limited dynamic range and nonlinearity limits its applications.

2.2.2 Source Follower per Detector Preamplifier

The source follower per detector (SFD) preamplifier is similar to the SI preamplifier, aside from having a source follower instead of the transimpedance amplifier. SFD unit cell is

subject to limited dynamic range and causes nonlinearity with the detector bias varied with the stored charge on the integration capacitor. However, with the reset bus, the detector bias can be initialized better than the SI unit cell. The SFD is typically utilized in low background applications where long integration times accumulate sufficient charge for readout.

The unit cell is again simple with having only three transistors, one to reset the detector voltage and two as the source follower amplifier, as in Figure 2.2.

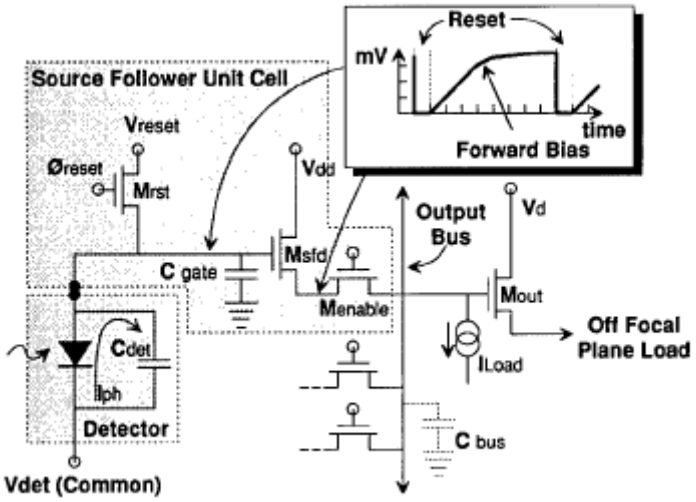

Figure 2.2: Source follower per detector readout [7]

As in the SI unit cell, the stray capacitance of the detector and the routing capacitances in addition to the gate capacitance of the source follower, form the integration capacitance. Since voltage conversion is handled by the source follower no additional bus amplifiers are required. Following the read operation, the detector is reinitialized by the reset switch and integration begins again.

The noise sources of the SFD are again kTC, MOSFET 1/f noise and MOSFET thermal noise. SFD having moderate noise has limited dynamic range and poor linearity at high background fluxes.

2.2.3 Direct Injection

Following the SI unit cell, direct injection preamplifier (DI) is the smallest unit cell which can also achieve very good results for IR imaging with PV type detectors, especially for SWIR and MWIR with high irradiance applications. Formed of only a single transistor, DI has very low noise. Compared to SI and SFD preamplifiers, it results with quite better detector bias

stability. Also gain is not dependent on detector capacitance and parasitic capacitances. Using an integrated capacitor, ROICs with DI preamplifier can achieve variable gains. However, for low background applications the injection efficiency drops significantly, resulting in a poor SNR. Use of DI circuits for low impedance detectors, especially LWIR PV detectors, is also limited due to the decrease in the injection efficiency.

The working principle of DI is simple. As in the Figure 2.3, the source of a MOSFET, controlling the integration of the photocurrent to the integration capacitor, follows the reverse biased PV detector. The injected charge is accumulated at the integration capacitor where the immediate change to charge to voltage domain takes place. Then the stored charge can be read through the use of a multiplexer to the output. Following the read of the integrated voltage, a reset switch initializes the integration capacitor for the following frame.

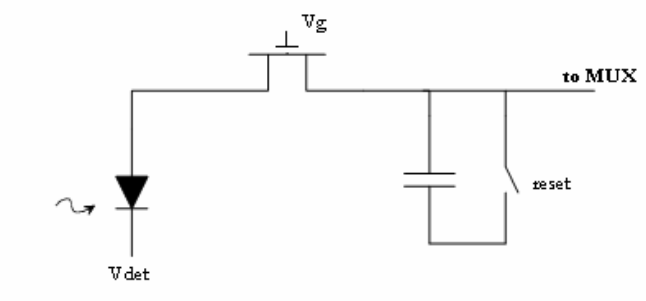

Figure 2.3: Direct injection preamplifier

In DI preamplifier, the detector bias is obtained by a stable voltage source (V_{det}) and the source of the MOSFET which is, ignoring the low overdrive voltage, the gate voltage plus the threshold voltage of the device. However this would not create a constant bias for all the PV detectors in the FPA since not all detectors are radiated by the same flux. Hence not driven by the same current source, the source voltages of the integration MOSFETs will differ over the FPA. This variation can be on the order of 10 – 50 mV and can result higher 1/f noise and dark current values, decreasing the SNR and linearity [7].

Another issue about the DI unit cell arises in terms of its injection efficiency. Injection efficiency is defined as the ratio of the integrated photon current I_{int} to the generated photocurrent I_{ph} is

$$Injection\_efficiency = \frac{I_{\text{int}}}{I_{ph}} = \frac{r_{\text{det}} g_m}{1 + r_{\text{det}} g_m} \qquad \textbf{(2.2)}$$

Where r_{det} is the detector impedance and g_m is the transconductance of the MOSFET. For low flux applications g_m is strongly dependent to the photocurrent since the MOSFET will be in weak inversion (sub threshold region). MOSFET will then operate with the equation as stated in [9]

$$I_d = \frac{W}{L}\mu_n C_{ox} \exp(V_g - \frac{mkT}{q}) \quad \textbf{(2.3)}$$

Then, g_m will be:

$$g_m = \frac{I_d q}{mkT} \quad \textbf{(2.4)}$$

G_m is independent of the device geometry parameters and dependent to the photocurrent. This results with DI being a poor choice for the low flux or low detector impedance applications reducing the linearity of ROICs significantly due to poor injection efficiency.

The noise sources for DI are again kTC, MOSFET 1/f and thermal noises. However with MOSFET noise contribution in terms of current being as given in [7]

$$i_0 \approx \frac{e_n g_m}{1 + r_{\det} g_m} = injection\_efficiency \frac{e_n}{r_{\det}}, \quad \textbf{(2.5)}$$

where i_o is the noise current integrated to the capacitor and e_n is the input referred rms noise voltage of the MOSFET device, MOSFET noise becomes insignificant.

In brief, DI is a small, low noise, compact preamplifier creating a relatively good detector bias stability compared to SI and SDF. However its applications lack to cover low flux applications and LWIR PV detector type ROICs where the detector impedances are small.

2.2.4 Buffered Direct Injection

Buffered direct injection (BDI) lowers the input impedance of the preamplifier by using a feed forward amplifier. It has all the advantages similar to DI, with lower input impedance. However its drawback is the use of amplifier which is hard to build in small pixel area, and consumes power which heats the ROIC which is a problem increasing noise and complicating the cooling process.

BDI is represented in Figure 2.4. Its operation is same as in DI. As in the figure the source of a MOSFET, controlling the integration of the photocurrent to the integration capacitor follows the reverse biased PV detector. Then the stored charge can be read through the use of a multiplexer to the output. Following the read of the integrated voltage, a reset switch initializes the integration capacitor for the following frame.

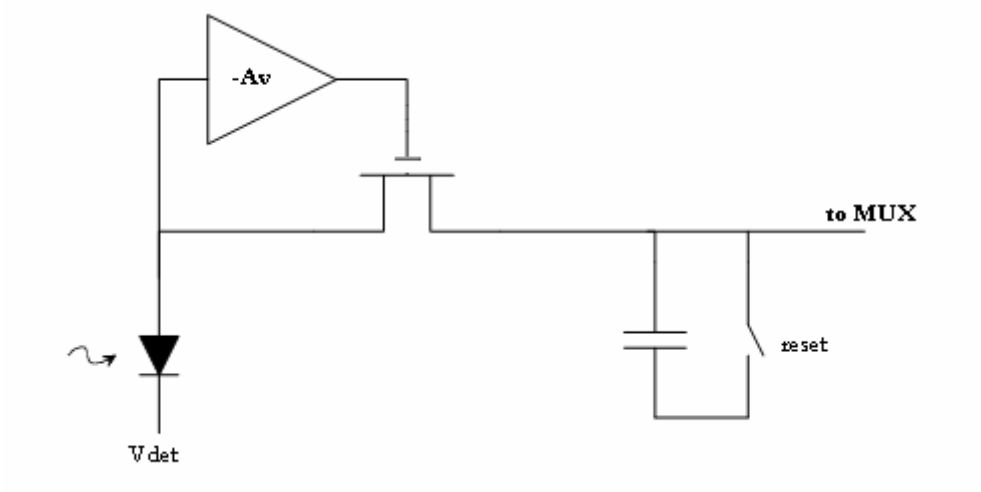

Figure 2.4: Buffered direct injection preamplifier

The feed forward amplifier provides an increase of g_m by a factor of $1+A_v$; hence the input impedance of the unit cell is reduced by a factor of $1+A_v$.

In addition to the noise sources of kTC, MOSFET 1/f, thermal noises, input noise of the inverting amplifier will be an additional noise source, representing the linearity vs. noise tradeoff.

BDI is a unit cell with all the advantages of DI with lower input impedance. However the amplifier will cause additional noise and increase power consumption. Also it is important to mention that it is a difficult task to get high gain and low noise, low power amplifier in a small area.

2.2.5 Capacitive Feedback Transimpedance Amplifier

The Capacitor feedback transimpedance amplifier (CTIA) unit cell is a reset integrator and addresses a broad range of detector interfaces for many applications [10]. It is mostly employed in ROICs with correlated double sampling, with having 3 transistors and a feedback capacitor.

The CTIA preamplifier in figure functions as follows. The photocurrent increases the voltage at the negative input of the amplifier. This change in the input reduces the output voltage, which in return pulls the photocurrent to the feedback capacitor. Hence a decreasing ramp at the output is observed. Following the read operation the feedback capacitor is initialized through the reset switch.

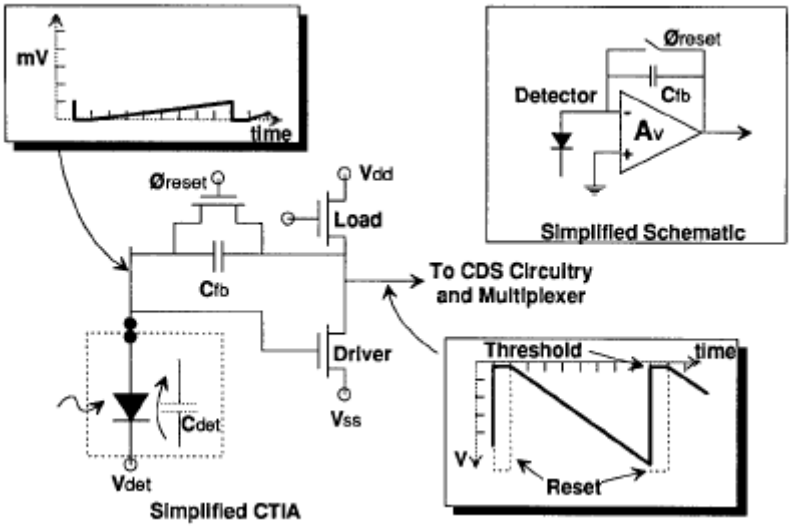

Figure 2.5: Capacitive feedback transimpedance preamplifier. Only a small change at the input is observed for a high change at the output [7]

CTIA as seen in the above graphs has little voltage variation at its input compared to the ramp at the output; hence it has good detector voltage bias stability. However its noise is affected by the amplifier input transistors, introducing its drawback.

2.2.6 Resistor Gate Modulation

Resistor gate modulation input cell is the only preamplifier that has nonlinear operation. Lacking the linearity, its advantage is that is appropriate for high flux background applications where with proper design of the resistor value, some level of background suppression can be achieved.

The RL circuit in figure operates as follows. Radiation caused photocurrent and dark current passes through the RL creates the voltage V_{in}. This voltage than induces a current that will pas through the MOSFET which operates in the sub threshold region. The integrated device current I_{int} will be an exponential according to the formula [7]:

$$I_{\text{int}} = I_d = \frac{W}{L}\mu_{\text{n}} C_{ox} \exp(V_{in} - \frac{mkT}{q}) \approx K \exp(V_{in}), \quad \textbf{(2.6)}$$

where K is dependent on resistor bias, geometry parameters and threshold voltage.

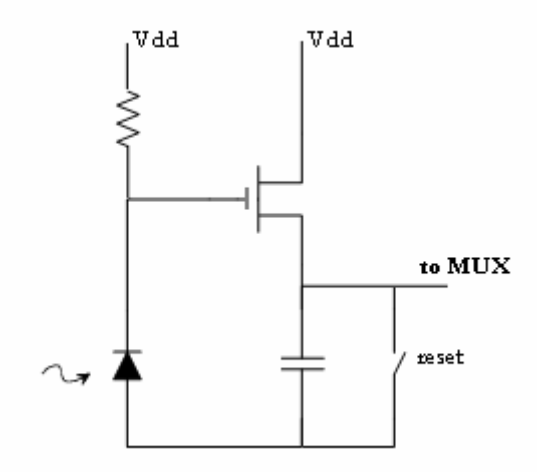

Figure 2.6: Resistor gate modulation preamplifier

With proper design of the resistor value, I_{int} can be reduced close to zero for a determined value of background irradiance. Aside this advantage, RL preamplifier has fixed pattern noise due to variations of transistor geometry and threshold voltages over the FPA which limits its applications to high background irradiance applications. Also the resistance creates additional noise.

2.2.7 Current Mirror Gate Modulation

Current mirror gate modulation (CM) preamplifier is similar to RL unit cell with the resistor being replaced by a diode connected MOSFET. It has better linearity compared to RL type unit cell, similar injection efficiency compared to DI unit cell. As in RL preamplifier, CM suffers from threshold voltage variations and geometry variations over the FPA.

The operation of CM unit cell in Figure 2.7 is as follows. The photo generated current creates a bias that is mirrored to the transistor whose drain is connected to the integration capacitor. After being connected to the output multiplexers a reset switch initializes the integration capacitor.

The CM preamplifier, although having better performance in terms of linearity, lacks the low input impedance since the input impedance will be strictly dependent on g_m as in the DI

preamplifier. Also it has the same noise issues of RL preamplifier as fixed pattern noise due to variations of transistor geometry and threshold voltages over the FPA.

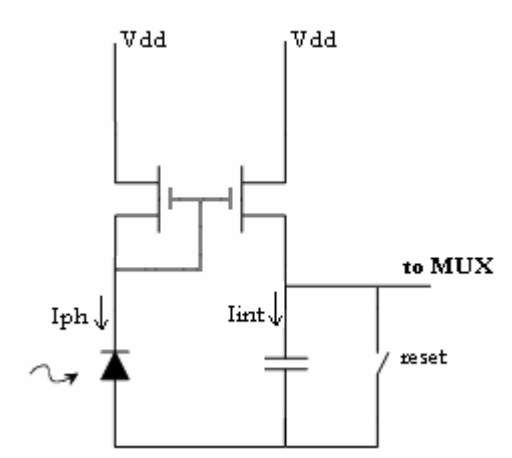

Figure 2.7: Current mirror gate modulation preamplifier

2.2.8 Current Mirroring Direct Injection

Current mirroring direct injection (CMDI) achieves 100% injection efficiency even for very low input impedances with a little extra power consumption compared to BDI and creates a very stable detector bias compared to the DI preamplifiers. Its disadvantage is the moderate noise it introduces compared to above mentioned preamplifiers.

As in Figure 2.8, by the use of current mirrors, the photo current I_{ph} is mirrored to the transistors to the left. Since the drain currents of two NMOS devices are equal with same gate voltage the source of MN2 will be zero, creating a zero bias on the PV detector. A zero bias will also result a zero dark current, creating the measured integrated voltage to be only as a result of IR radiation. However, due to transistor threshold voltage mismatches, the PV diode can move slightly from zero bias to a 1 mV of reverse bias as stated in [11].

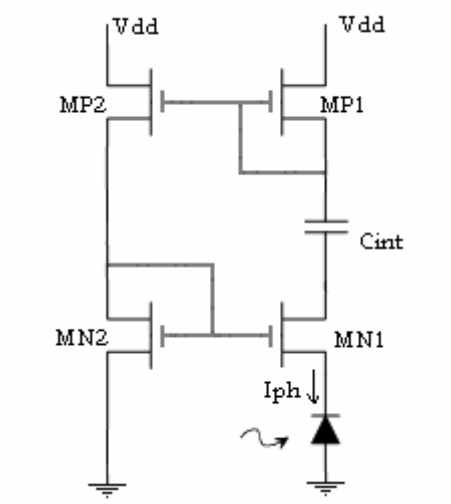

Figure 2.8: Current mirror direct injection preamplifier

The injection efficiency of CMDI preamplifier is also evaluated in detail as well as its comparison with widely used preamplifiers of DI and BDI in [11] and given as:

$$injection\_efficiency = \frac{R_D}{R_D + R_{IN}} = \frac{g_{mn2}R_D}{g_{mn2}R_D + (1-\gamma_{gm})}, \quad \textbf{(2.7)}$$

where γ_{gm} is given as:

$$\gamma_{gm} = \frac{g_{mp1}}{g_{mp2}} x \frac{g_{mn2}}{g_{mn1}} \quad \textbf{(2.8)}$$

And the reverse bias voltage over the detector is given as:

$$V_{DET} = \frac{K_P}{K_N}\Delta V_{TP} + \Delta V_{TN}, \quad \textbf{(2.9)}$$

where K_P and K_N are geometry constants, ΔV_{TP} and ΔV_{TN} are threshold variations between two mirroring transistors of PMOS and PNMOS devices respectively [12].

The comparison with DI and BDI as in table shows that for a cost of little power consumption. However this work ignores that CMDI together with its benefits stated has higher noise level than DI.

	DI	BDI	CMDI
ΔI_D (when ΔI_{ph} = 20nA	1.17nA	8.92nA	10.15nA
Injection efficiency ($\Delta I_D/\Delta I_{ph}$)	11.7%	89.2%	101.5%
Unit cell power consumption	~ $V_{DD} \cdot I_{ph}$	~ $V_{DD} \cdot I_{ph}$ + amplifier power	~ $2V_{DD} \cdot I_{ph}$
Cell to cell detector bias variation	Within ~ 50mV over FPA	Within ~ 2.5mV over FPA	Within ~ 0.5mV over FPA

Table 2.1: Comparison of DI, BDI and CMDI preamplifiers [11]

2.2.9 Current Mirroring Integration

Current Mirroring Integration (CMI) operates very similarly to CMDI but has the integration capacitor off-pixel, increasing the dynamic range and charge storage capacity. It has, as in CMDI, 100% injection efficiency and very stable detector bias over the FPA to a cost of higher power consumption, larger size and moderate noise.

The operation of CMI unit cell as represented in Figure 2.9 is as follows. The photo generated current passes through MN1 and is mirrored to MN2 with high swing cascade current mirror through transistors MP1 and MP4. Similar to the CMDI preamplifier MN1 and MN2 being connected as current mirror, the PV detector bias is forced to be zero. By use of MP5 and MP6 the photocurrent is mirrored to the integration capacitor [12]. Following the read operation, a reset switch initializes the integration capacitor voltage.

Injection efficiency of the CMI unit cell is identical to that of CMDI, almost 100%. However for very low photocurrents (less than 1nA) the devices operating in the weak inversion may have significantly low transconductance values, decreasing the 100% injection efficiency. In terms of the detector bias stability, CMDI is identical to CMI. Its drawback is that CMI has significantly higher noise than DI or BDI type preamplifiers.

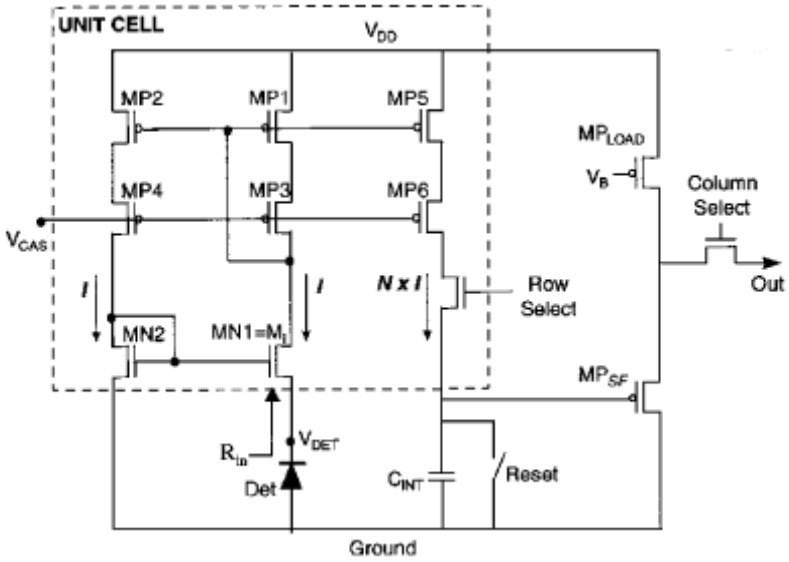

Figure 2.9: Current mirroring integration readout [12]

2.2.10 Comparison of ROIC Preamplifiers

Preamplifiers are the first circuit parts where photo generated charge to voltage conversion occur. In general, for user specified integration time charge is stored on a capacitor, multiplexed to the output and before a subsequent read operation a reset switch initializes the capacitor voltage. As discussed in the previous sections there are different types of input circuits varied with their properties as size, power consumption, input referred noise and dynamic range. The preamplifier choice is a designer decision according to the application specifications such as detector type, detector impedance and capacitance and application's radiation levels.

Among all preamplifiers, SI is the smallest unit cell, with minimum noise contribution. However using only detectors stray capacitance and detector getting in to forward bias region as the integrated voltage increases, results a limited dynamic range. A bus amplifier is required for charge to voltage conversion following the multiplexing of a detector to be read. SFD also uses the stray capacitance for same reasons as in SI, has a limited dynamic range. With three transistors, one for reset operation and two for source follower per detector, it is larger than SI unit cell, but ROICs with SFD does not require a bus amplifier due voltage conversion before multiplexing is handled by the source followers. Due the source follower, noise in SFD is higher than noise in SI preamplifiers.

Direct injection preamplifier is also a very compact input cell, which has higher dynamic range than SI and SFD due to the integrated capacitor. Compared to SI and SFD it has good detector voltage stability. DI preamplifier has also low noise due it has only one MOSFET device as the noise source. However, its only, but significant drawback is that for low IR irradiances DI unit cell shows poor injection efficiency due having high impedances. Hence DI unit cell is an inappropriate choice for low impedance detector arrays such as LWIR PV FPAs.

The injection efficiency problem is solved by using a feed forward inverting amplifier at the input as in BDI preamplifier. Injection efficiency is increased by a factor of the amplifier gain. However, input noise of the amplifier is another noise source. In addition, obtaining a high gain, low power amplifier at a small pixel area is a difficult task.

Capacitive transimpedance amplifier unit cell is widely used in many different ROICs as the preamplifier. It also uses an amplifier at the input as in the BDI which creates a wide output voltage change for a little change at the input. Hence for the integration period detector bias is quite stable. However as in BDI, the amplifier creates additional noise.

Resistive gate modulation circuit is used in high background applications due its nonlinear operation. Its size is also dependent on the resistor. Its drawback is that it creates a fixed pattern noise due to the device mismatches over the FPA.

Resistor is replaced by a mirroring MOSFET in current mirror gate modulation (CM) unit cell, making it operating linearly. It has only two transistors making it compact. However it also suffers from threshold voltage variations and geometry variations of MOSFETs creating noise.

Current mirroring direct injection unit cell is another preamplifier using current mirrors to stabilize the detector bias and reducing the input impedance. Very low input impedances can be achieved increasing the injection efficiency to 100%. Detector bias variations over the FPA can be as low as 2.5 mV which suppresses dark current variations. Its drawback is that integration capacitor is used in pixel, reducing the dynamic range in small pixel area. It also has high noise due to current mirrors.

Current mirroring injection (CMI) is similar to CMDI preamplifier, but it uses a high swing cascade current mirror structure to mirror the photo generated current to the off pixel

integration capacitor. Using off-pixel integration capacitor increases charge handling capacity. CMI injection efficiency and noise issues are same as in CMDI preamplifier.

Preamplifier	Input Impedance	Detector Bias Stability	Size	Input Referred Noise
SI	Self integrator	Not stable, changes during integration	Small	Low, detector noise only
SFD		Not stable, changes during integration	Small, 3 transistors	Moderate, Depends on source follower
DI	$1/g_m$	Not stable, changes during integration (10-50mV)	Small, only 1 transistor	Low, depends on single MOS
BDI	$1/g_m x (1+A_v)$	Stable, controlled by op-amp feedback	Large, due to in pixel amplifier and integration capacitor	Moderate, Depends on amplifier noise
CTIA	Self integrator	Stable, controlled by op-amp feedback	Large, due to in pixel amplifier and integration capacitor	Moderate, Depends on amplifier noise
RL	Load resistor	Not stable, depends on photocurrent	Large due to in pixel resistor	Moderate, Depends on

			and capacitor	resistor
CM	$1/g_m$	Stable, controlled by current mirrors	Large due in pixel capacitor	Moderate, depends on current mirrors
CMDI	$1-\gamma / g_m$	Stable (1-2.5mV)	Large due to in pixel integration capacitor and four transistors	High due to current mirrors
CMI	$1-\gamma / g_m$	Stable (1-2.5mV)	Small,9 transistors but off-pixel integration capacitor	High due to current mirrors

Table 2.2: A comparison of preamplifiers in terms of input impedance, detector bias stability, size and input referred noise, where A_v is the amplifier gain, γ is as given in equation 2.8 and g_m is the transconductance

2.3 Time Delay Integration

There are different signal processing techniques associated with ROICs such as time delay integration (TDI), sample and hold and correlated double sampling (CDS). ROICs, as well as these techniques, may have features such as variable gains, pixel selection-deselection in case of a malfunctioning pixel, automatic gain adjustments and etc. Thanks to the high integration capacity of CMOS technology, on chip digital quantization is also possible.

A sample and hold technique can be employed in a ROIC in order to obtain continuous integration. The integrated charge can be sampled to a storage capacitor and read while a new integration continues during the read from the hold capacitor.

Another technique, correlated double sampling (CDS) is widely used in sampled data circuits especially in switch capacitor circuits [13]. In switch capacitor circuits, CDS is used to store the noise of an amplifier in one phase and to subtract it from a new set of amplifier noise on a

subsequent phase creating a DC zero in the frequency domain, which eliminates flicker noise [14].

TDI is another signal processing techniques applied on ROICs to reduce noise, hence increase the SNR. SNR in infrared detectors is proportional to the square root of the integration time; TDI is used as a method to effectively increase the integration time without changing frame rate and resolution. By implementing TDI technique, diodes on the same row are used to detect the same image and the signal is integrated from these photo-diodes [3]. Hence, TDI realized on N detectors, results in an improvement of $\sqrt{N}$ in SNR, effectively increasing integration time by N.

A mathematical formulation is presented in [4] as follows. Radiation is received by the first pixel and following a time delay Δt, same radiation is received by the subsequent pixel on the array. The output is the sum of charge stored by n pixels, n being the number TDI pixels used. Hence total voltage summed at the output is given as:

$$V_{total} = \sum_{i=1}^{n} v_i(t1 + (i-1) * \Delta t), \tag{2.10}$$

Where v_i is the voltage corresponding to the charge accumulated by detector i.

However, noise is added by power, given as:

$$V^2_{noise\_total} = \sum_{i=1}^{n} v^2_{noise\_i}(t1 + (i-1) * \Delta t) \tag{2.11}$$

Where v_{noise_i} is the voltage corresponding to the noise accumulated by detector i.

Since all pixels will be illuminated by same radiation with a time delay, all pixels will add same amount of voltage and noise power. Hence the output voltage will be four times a single detectors output and output noise will be four times a single detectors noise power, resulting an SNR improvement of $\sqrt{N}$.

$$S/N = \frac{v_{total}}{v_{noise\_total}} = \sqrt{N}(S/N) \tag{2.12}$$

Device for reading line arrays with TDI effect consists of assembly of detectors and each detector integrates its own contribution during integration time. Then a summing device carries out sum of these contributions of detectors that are time-delayed versions of current image in order to create a TDI effect on detectors. The structure for TDI, described is represented in Figure 2.10 where TDI is applied with four detectors.

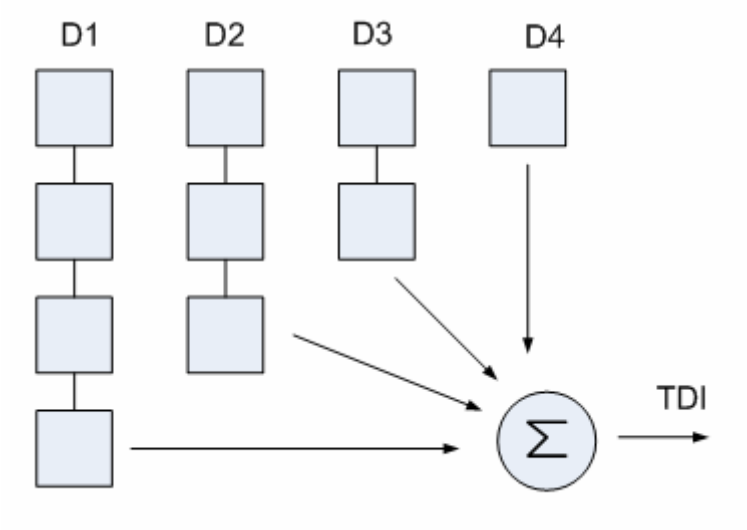

Figure 2.10: Block diagram of TDI operation on four detectors

In order to create a TDI effect on detectors optical scanning of the image is required. As can be seen from Figure 2.11, the image is scanned through detectors starting from the left. The pixel data obtained from TDI can be achieved by adding the contributions of the detectors of same pixel for different times.

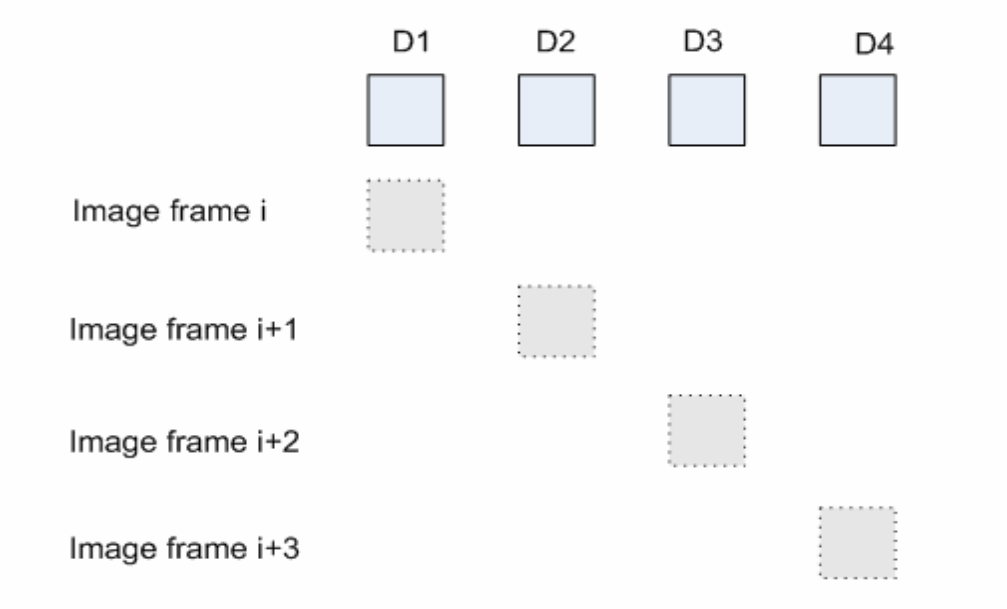

Figure 2.11: TDI scanning on four detectors

According to the diagram above the data for an image I_1 is generated as following:

I_1 = D1 (image frame i) + D2 (image frame i+1) + D3 (image frame i+2) + D4 (image frame i+3) [16]

Also spatial resolution of the image can be improved by implementing an optical super sampling, a method used to create more than one data (hence more than a single column at video output) from a single detector by moving the image from one detector to another with more than one step. The diagram representing optical super sampling rate of 3 is presented in Figure 2.12. This time, the sequence for obtaining pixel I_1 can be described as:

Pixel I_1= D1 (image frame i) + D2 (image frame i+4) + D3 (image frame i+7) + D4 (image frame i+10) [16]

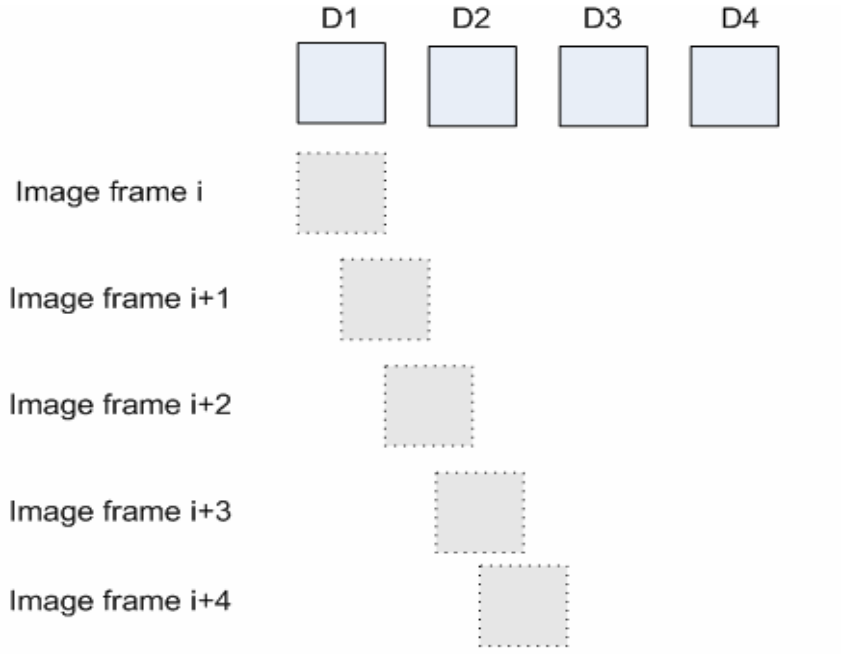

Figure 2.12: TDI scanning on four detectors with super sampling rate of three

TDI functionality can be implemented in two ways. Either a single storage (capacitor) handles the charge generated by different detectors of same image or multiple storages are used to add the charge generated by different detectors of same image, with a given time delay depending on the frame rate. Both approaches have certain advantages and disadvantages. The first approach requires that there are more devices to add signals generated from different

detectors. The second approach however uses more analog memory (storage capacitors) and can be implemented by the use of a single adding device.

In Figure 2.13, represented is architecture of TDI implemented on four detectors with super sampling rate of three in line with the first approach. Since TDI is realized on four detectors with super sampling rate of three, an image that drops on first detector is received by the fourth detector after a 10 frame rate delay. Hence, if TDI is implemented with this architecture as represented in figure, ROIC in order to have the simultaneous integrate and read options, must have 12 storage and adder devices; 10 to be used for storage during the delay, one to realize integration while read operation, and one to be used for storage during resetting. With this kind of architecture, at frame i, D1 is integrating, at frame i+3 D1 and D2 are added, at frame i+6 D1, D2 and D3 are added and at frame i+9 D1, D2, D3 and D4 are all summed. I +10 is when read operation is done. At frame i+11 resetting of the integrator occurs [16]. The process is continuously repeated for every integrator.

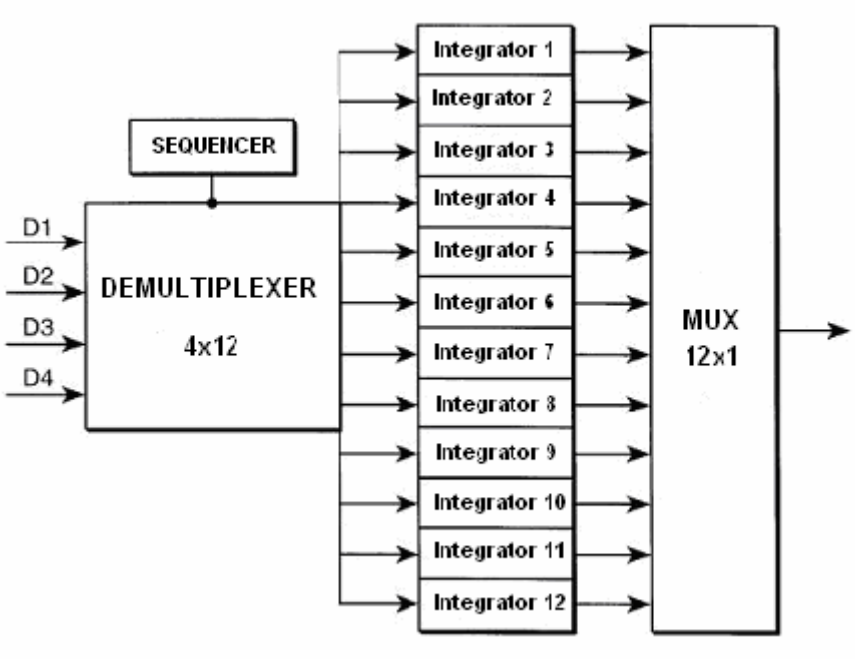

Figure 2.13: TDI architecture with use of 12 integrators [16]

Integrators used in above architecture as represented in the figure employs amplifiers (op-amp) creating drawbacks. Here C1 is the integration capacitor. With proper biasing through switches integrated charge is transferred to C_s. The voltage added is read through the rising ramp at the output. A reset switch initializes the output (sampling) capacitor to zero state. ROICs with this kind of TDI architecture usually integrate the stored charge over a DC value.

The above explained TDI architecture benefits from the minimum number of storage elements. Since in a CMOS technology storage elements are capacitors and capacitors are area consuming, this architecture has a convincing advantage. However, it also has certain drawbacks. First, using twelve integrators may cause significant power consumption, which also brings up the heating issue as a by product. Second there may be mismatches between the integrators, such as threshold mismatches between transistors or geometry mismatches causing non-linearity. Hence another approach employing a single integrator to a cost of more storage memory, may be a better choice depending on the application in terms of number of detectors TDI is implemented, as well as super sampling rate.

A second approach lies on the idea of reducing the number of integrators, through increasing the number of analog memory. The architecture is represented in Figure 2.14. As in the previous architecture of TDI being implemented on four detectors with super sampling rate of three, D1 must have 11, D2 must have 8, D3 must have 5 and D4 must have 2 storage elements. The storage elements are capacitors, or a set of switches and capacitors to realize variable gains, where the switches are MOSFET devices. In this architecture, switches connect the two terminals of the capacitors to same potential forcing the integrated charge to move to output (sampling) capacitor. A rising ramp is observed at the output, as the charge is transferred. Following every charge transfer, a reset operation is required to initialize the storage capacitor to its initial DC value.

ROICs employing TDI in line with this architecture, has the advantage of low power and linear operation compared to the previous architecture. However, the cost is higher area due to usage of twenty six total storage elements compared to 12 storage elements. The circuit type to implement TDI is hence designer's trade of between area, linearity and power consumption. The second approach is a good choice for linear ROICs such as 288x4 with TDI implemented on 4 detectors with super sampling rate of three. However due to the greatly increased area corresponding to the increase of TDI elements, first approach is a better choice for ROICs such as 576x7 TDI implemented on 4 detectors with super sampling rate of three.

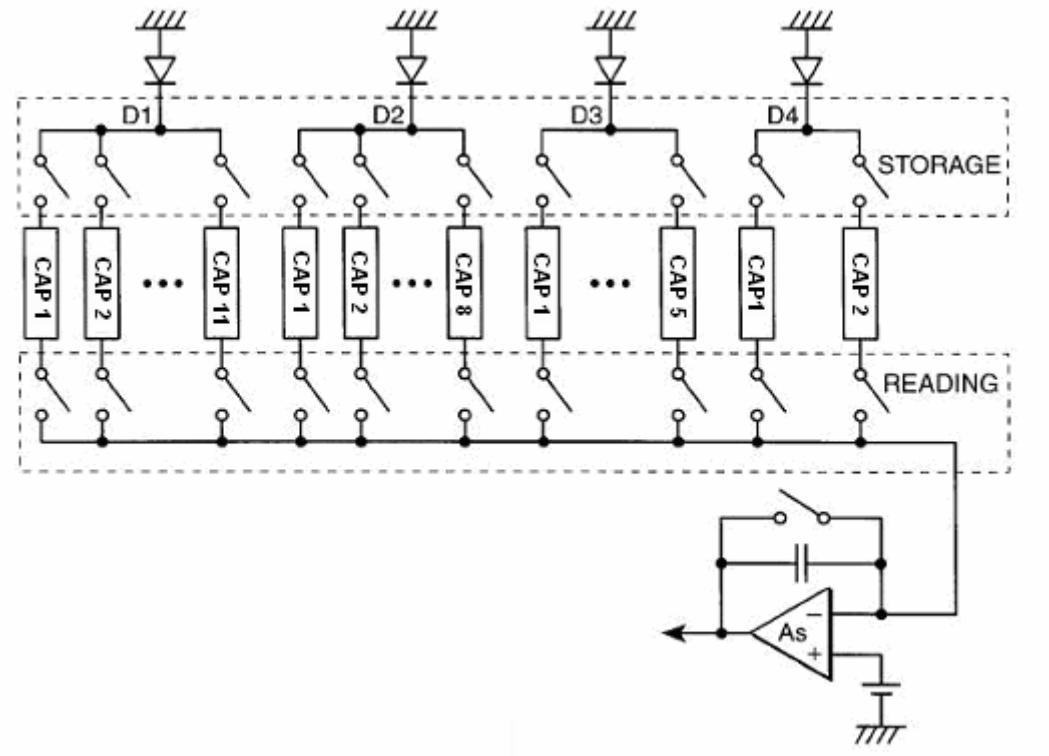

Figure 2.14: TDI architecture with use of single integrator to a cost of more storage elements [16]

2.4 Additional ROIC Features

As discussed in the previous section TDI is a very common signal processing employed in ROICs to increase SNR by suppressing detector noise. Aside from the TDI property, linear ROICs may have additional features of variable gains, adjustable integration times, bidirectional scan, and pixel bypass for test mode, pixel deselection and automatic gain adjustment. ROICs also include interface circuits serial, parallel or both in order to program the ROIC according to user preferences. In this section, these features of ROICs and their possible implementations are pointed out in brief.

Variable gain functionality is very common in ROICs as represented in [17][18]. An efficient way to realize variable gains is with the use of switches, increasing the integration capacitance at their on state. For such integration capacitor sets, output (sampling) capacitors must be switched accordingly for proper operation.

Most ROICs have adjustable integration times, as represented in [19][20]. ROICs may have two clocks, one master clock to drive digital control circuits and another to set the integration time, i.e. integration takes place during an integration signals high. In this way, setting

integration signals duty cycle, with its period, allows adjustable integration times. Another way to achieve variable integration time is through a single master clock, with user programming by digital data entry, setting the number of cycle the integration to take place.

Bidirectional scan property is used to give flexibility to the imaging system, by allowing the optics to change scanning direction. Bidirectionality can be realized by either adding additional memory to every detector group to realize TDI as discussed in previous sections or switching the detectors through a fixed set of integration capacitors.

FPAs may have defective elements, such as high noise detectors or detectors not functioning at all. If these detectors are to be used as valid data carriers, erroneous outputs results. Hence first an ROIC must be tested for every pixel's operation at a certain radiation level. At this point every element can be read at the output alone. Hence a bypass property must be added in ROICs. This can be implemented by carrying the integrated charge of a single detector to the TDI stage. According to the data of pixel functionality, the output data is used to program the ROIC for proper operation.

Pixels known to be malfunctioning by test mode are removed from the summing at TDI stages. ROICs hence involve automatic gain adjustment functionality, creating a valid output from a less number detectors. This functionality can be implemented at the TDI stages through capacitive switching as in the case of variable gains or can be implemented at the output stage through the use of an amplifier, with gain depending on the number of detectors malfunctioning.

Finally all ROICs involve a user interface to program the ROIC. ROIC functionalities such as gain settings, integration time settings, working mode (TDI or test), scanning direction and pixel programming that are controlled by the user are inputs through a parallel or serial interface. Main ROIC functionalities such as scan direction or gain setting can be set through parallel interface while programming can be handled by serial interface. In this way, control pads are reduced that would result lots of addressing pads otherwise (i.e. programming done by parallel interface).

CHAPTER 3 288x4 ROIC IMPLEMENTATION

3.1 ROIC Definition and Requirements

A 288x4 ROIC is designed using Austria Microsystems' (AMS) 0.35-µm 4 metal 2 poly CMOS process technology for a 288x4 linear FPA of photo voltaic type, n on p HgCdTe detectors sensitive to long wave infrared radiation within the wavelength range of 7.7 to 10.3µm. Detector pixel sizes are 25x28µm. FPA, consisting of four groups of 72 channels is as represented in figure. The length and width of the FPA is 8064µm and 383µm with a separation between the left and right blocks of 100µm.

ROIC has four outputs, each being generated from a 72x4 sub block, operates at a frequency up to 5MHz, including TDI on four elements with a super sampling rate of three. ROIC requirements are as listed below.

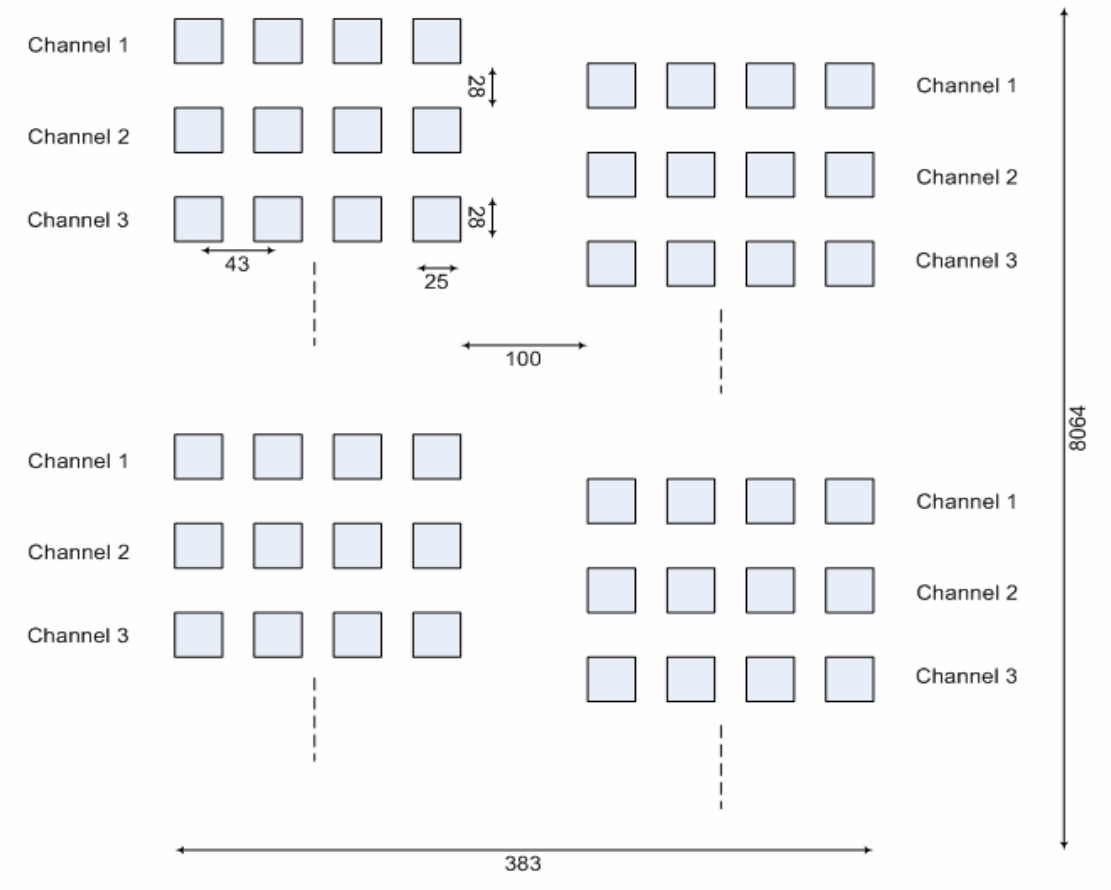

Figure 3.1: Detector distribution and size over the FPA

Input Requirements

Minimum detector input impedance is 1MΩ. Input current range is 1.2 – 55nA with 12.3 being the nominal current level

Operation Modes

The readout integrated circuit has the following features:

- Integration period adjustment
- Variable gain adjustment
- Bidirectional TDI scanning
- Bypass property for test mode
- Pixel deselection / automatic gain adjustment accordingly

Programming Modes

The readout integrated circuit can be programmed through serial interface or parallel interface. In parallel mode, no pixel deselection property is allowed, hence all detectors are considered as functioning devices. Variable gains and scanning direction properties can be programmed through parallel mode operation.

Serial mode is used to program the chip for the malfunctioning detectors. In the serial mode, ROIC can also be controlled to change gain setting and scan direction. Whether the chip operates in serial mode or parallel mode is realized by user input SERIAL_BAR.

Output Requirements

Dynamic range of the ROIC at the output is 2.8V. A zero radiation causes an output voltage of 1.7V; hence maximum observable output is limited to 4.5V. The output should be ready to be sampled by an off-chip ADC in 100nsec considering the maximum clock frequency of 5 MHz. ROIC should drive an output load of a 10pF capacitor with a 1MΩ shunt resistor.

Noise Requirements

Input referred noise of the ROIC should be less than 2100e^-.

Power Consumption

Total power consumption of ROIC is limited to 50mW.

3.2 ROIC Architecture

288x4 ROIC is constituted of for 72x4 sub-blocks, each operating as a single 72x4 ROIC having single output. All blocks together, create four parallel, outputs. Hence 288x4 ROIC architecture is as in Figure 3.2.

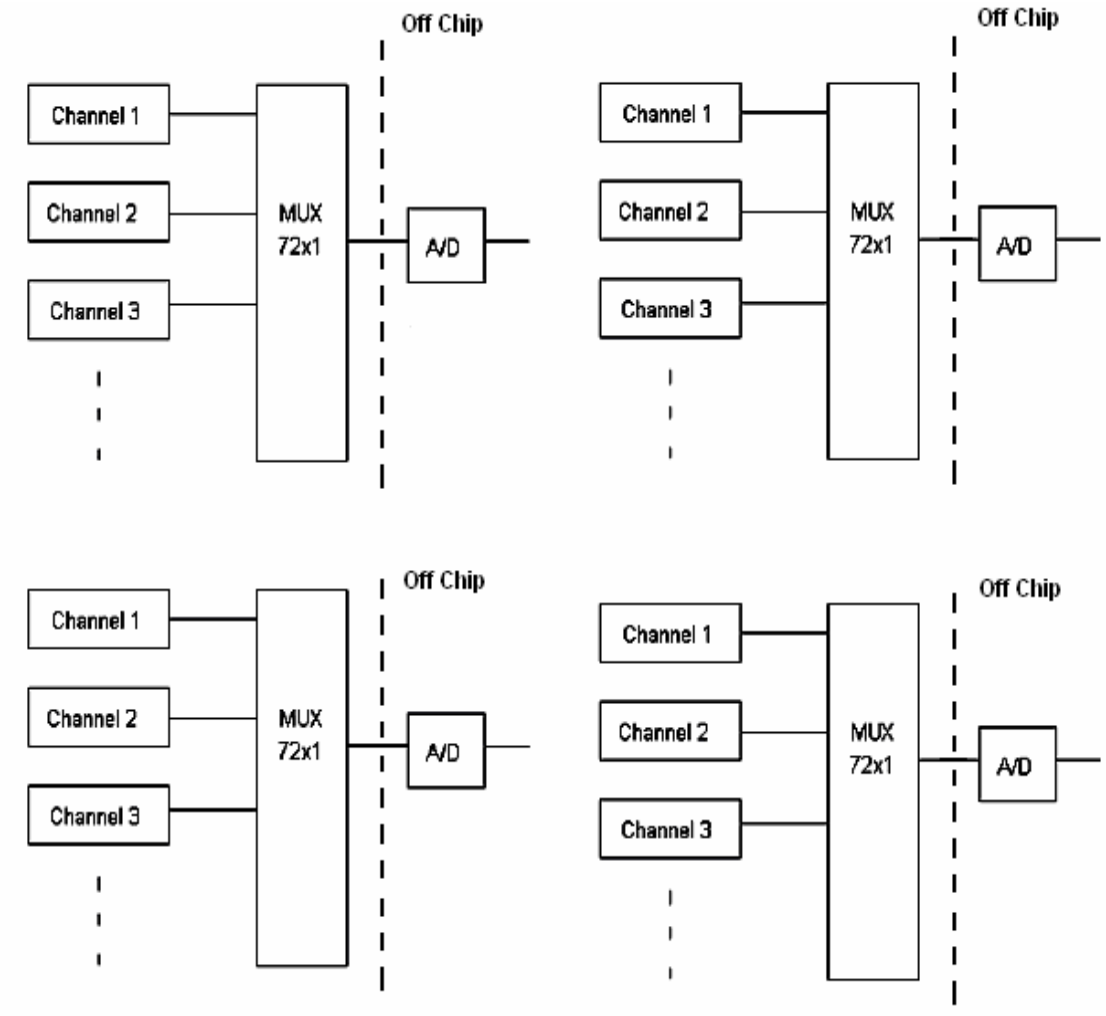

Figure 3.2: Block diagram of 288x4 ROIC with off-chip ADC

72 channels form the 72x4 ROIC as represented in Figure 3.3.

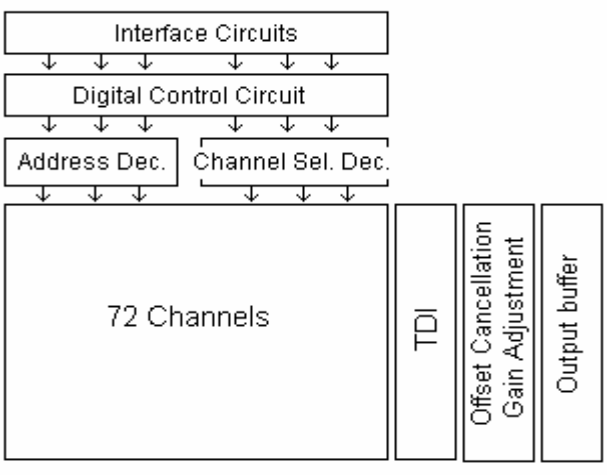

Figure 3.3: Block diagram of 72x4 ROIC

A channel is constituted of four preamplifiers, twenty six capacitor sets (integrated charge storage), according to the TDI approach with single amplifier, with TDI being implemented on four detectors with super sampling rate of three, four latches to store pixel functionality data, a channel select circuit to connect the channel to output at required time, a four input NAND gate to signal automatic gain adjustment and bidirectionality switches. Channel architecture is represented in Figure 3.4.

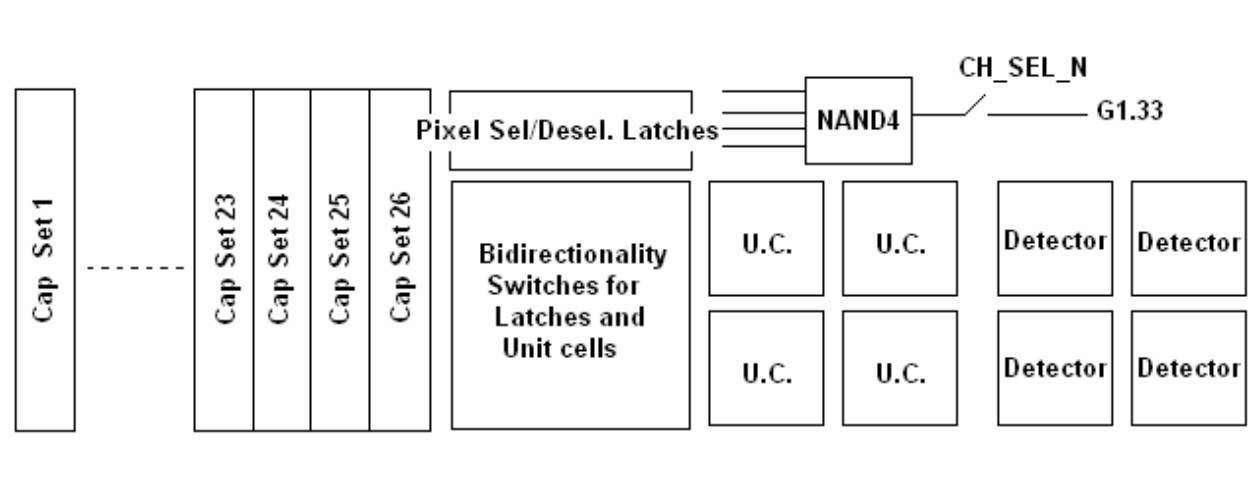

Figure 3.4: Block diagram of a channel constituted of 26 storage elements, four unit cells for four detectors, bidirectionality switches and a NAND gate to drive automatic gain adjustment control signal

3.3 ROIC Implementation

3.3.1 Input Stages

3.3.1.1 Preamplifier Design

Various input cells are discussed in previous sections and compared according to their linearity, output noise, power consumption and detector bias stability. It is designers decision between various trade-offs. In this, 288x4 ROIC, CMI preamplifier is used. The reason to choose CMI preamplifier is due to the requirements specified in section 3.2. First detectors impedance is as low as 1MΩ, requiring a low input impedance input stage in order to keep injection efficiency and linearity high. Second, CMI has excellent detector bias stability, almost zero, eliminating dark current effects.

Conventional CMI circuits as in figure of section 2 includes 9 transistors in-pixel, photocurrent as input and photocurrent as the output, stored on of-pixel integration capacitor. However carrying the photocurrent precisely to the integration capacitor is a difficult task, due to the unavoidable parasitics. These parasitics' effects become significantly important, especially when the integration capacitors are becoming large.

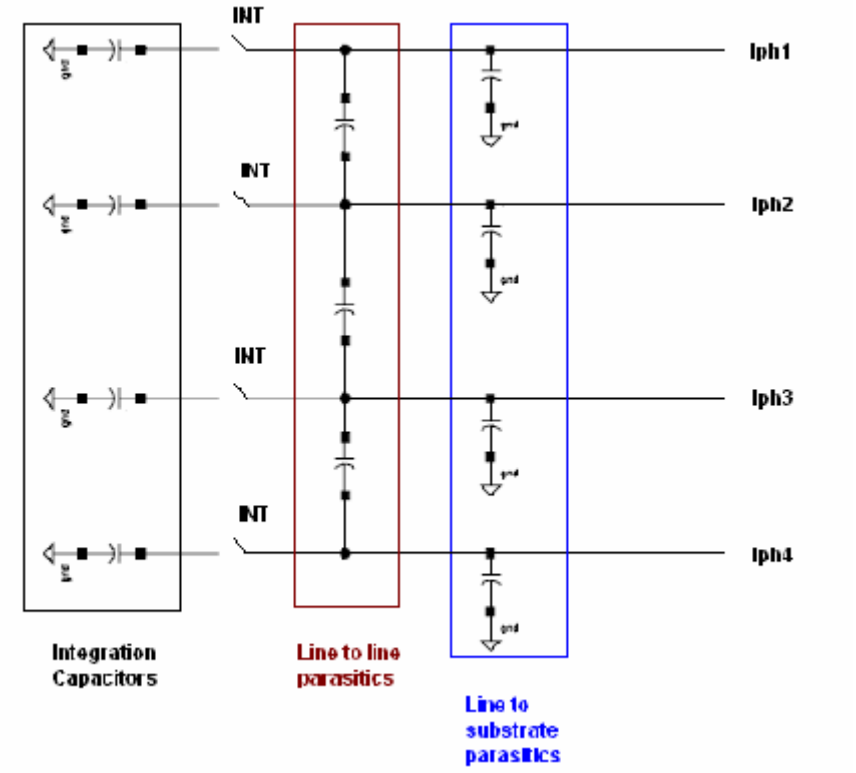

Figure 3.5: Parasitics associated with lines to carry photocurrent

Parasitics associated with current carrying lines are represented in the figure. Coupling parasitics to ground can be decreased by using a higher level metal, such as metal3, proper layout techniques can also eliminate path mismatches, hence parasitics can be matched at some extend. However line to line parasitics associated are only avoidable through spacing the lines distantly. In this application, channel height is fixed to 56μm due to the FPA requirements. If, integration capacitors' top plates are as well avoided for routing, as a keep out to prevent nonlinearities, distant spacing of lines is not possible. In sum, carrying photocurrent precisely to integration capacitors is not possible, especially when ROICs becomes large.

In order to overcome the above discussed problem, the last stage of conventional CMI can be removed from the pixel area, and moved near to the integration capacitors. Hence instead of current voltage is carried, and a copy of photocurrent is created and integrated.

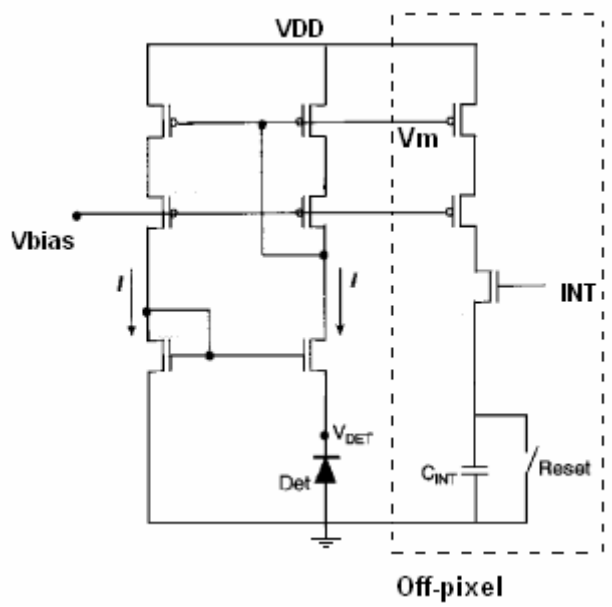

Figure 3.6: Schematic of CMI unit cell. The last stage is off-pixel, Vm and Vbias is carried through the ROIC to regenerate photocurrent near the integration capacitors

It is also important to mention some simulation results, in comparison with DI preamplifier in order to express why CMI is an appropriate choice as input cell. A DI unit cell is built with the same technology. It is observed that for the input current range, impedance of DI circuit varies between 250KΩ to 2.5MΩ. In comparison, input impedance of CMI varies between 1.2KΩ to 64KΩ. Considering that PV detectors for this specific application can have input impedances as low as 1MΩ, results that DI will show an injection efficiency of %25 for low fluxes, while CMI shows an injection efficiency of %95 in worst case.

Also, bias stability of the two preamplifiers is compared in Table 3.1:

Current	**DI - Detector Bias**	**CMI – Detector Bias**
1nA	112.8mV	477µV
10nA	79.5mV	562µV
30nA	47.8mV	752µV
50nA	32.4mV	867µV
70nA	22mV	940µV
100nA	10.75mV	1004µV

Table 3.1: performance comparison of designed DI and CMDI unit cells

Aside these advantages, it is also important to mention the drawback of higher noise. Designed CMI unit cell has a noise level of 414e^-, while DI unit cell has a significant lower noise level of 69e^-.

3.3.1.2 Input Capacitors

It is common to use MOS capacitors, due to the availability of thin gate oxides. However, MOS capacitors are quite nonlinear, or linear at a very limited dynamic range. For this reason already available poly-capacitors are used at the input stages. There are four gain settings of ROIC as given in Table 3.2. For a dynamic range of 2.8V, stored charge is given as well.

Gain state	Equivalent Capacitance (pF)	Storage Capacitance (pC)	Gain Ratio
0	0.35	0.98	1.30
1	0.46	1.29	1.00
2	0.70	1.96	0.66
3	0.92	2.58	0.50

Table 3.2: Gain settings and ratios

To obtain capacitance values as in above table, 0.35, 0.22, 0.24 and 0.11 pF poly capacitors are added by switches which are implemented by NMOS devices. Circuit implementation is given in Figure 3.7.

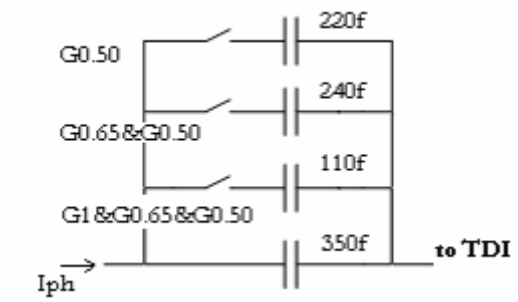

Figure 3.7: Input Capacitors

3.3.2 Implementation of TDI stages

As explained in the previous section, TDI is implemented by using a single amplifier and 26 analog memories. According to this principle, D1 has 11, D2 has 8, D3 has 5 and D4 has 2 capacitors. For bidirectional scanning, either D1, D2, D3, D4 should have 11, 8, 8, 11 capacitors respectively, or unit cells should be switched in between the capacitor sets of 11, 8, 5, 2. The second approach is used in implementing TDI in order to operate with low power consumption.

At each frame, an integration switch between a detector and one of the storage capacitors is on while all others are off, enabling integration of all detectors, simultaneously to one of its memory. Following the charge transfer on a storage capacitor, charge is saved for its addition to three other detectors stored charge at its required frame.

There are four switches associated with charge transfer from detector to TDI amplifier: INT, RESET, S1 and S2. RESET and INT are used to transfer the charge from detector to integration capacitor. RESET initializes capacitor voltage, while INT enables photocurrent to transfer to storage capacitor.

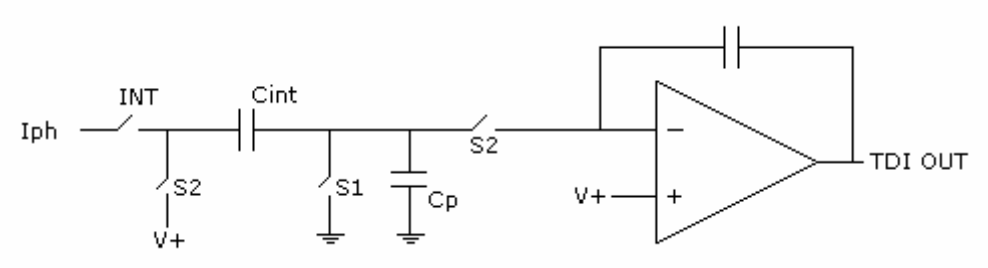

Figure 3.8: Circuit used for realization of TDI

Charge transfer to TDI register is realized with the use of an op-amp. Together with S1 and S2 switches, this circuit forms a switch capacitor integrator, as represented in Figure 3.8. S1 is on during integration, connecting the bottom plate of integration capacitor to ground level and off during charge transfer to TDI stage. S2 is off during integration and on during charge transfer to TDI stage, forcing zero voltage drop between the plates of capacitor. Since there is no path but the bottom plate of the sampling capacitor between the negative input and output of the amplifier, all the stored charge on C_{int} is transferred to output stage.

However there is one remaining issue related to this charge transfer process. As stated before, poly capacitors are used as integration capacitors which have significant parasitics associated with their bottom plates. In the process ROIC is designed poly1-poly2 area capacitance is 0.86 fF/μm^2, whereas poly1 to substrate area capacitance is 0.119 fF/μm^2 which can result in significant additional charge movement to the output. As in figure, bottom plate is connected to ground level during integration. However, in order charge to be transferred to TDI sampling capacitor, its both plates are connected to V+ which is the voltage applied to the amplifier's positive input. Since the voltage at the bottom plate is changing from ground level to V+, which is set to 1.2V for this design, the parasitic capacitance, C_p is being charged to V+, hence results an additional erroneous charge transfer to the output.

The above issue is quantitively analyzed as follows. At an instant of time, a total charge of $Q_{int} = V_{int}*C_{int}$ is stored at the top plate of the integration capacitor. When S2 switches are closed, voltage on the integration capacitor is forced to be zero which results a discharge over CTDI. At this instant, a charge movement of $Q_p = V_+ \times C_p$ results an additional increase at the output. Following the end of integration, at bottom plate of integration capacitor, charges on the bottom plate of C_{int} and top plate of C_p plates are as;

$$Q_{\text{int},bottom} = -V_{\text{int}} \times C_{\text{int}} \quad , \quad Q_{p,top} = 0 \qquad \textbf{(3.1)}$$

When this charge is transferred to TDI stage, with S2 on and S1 is off, charges on the bottom plate of Cint and top plate of Cp plates are as;

$$Q_{\text{int},bottom} = 0 \quad , \quad Q_{p,top} = V_{+} \times C_{p} \tag{3.2}$$

Hence at the output, there is a total charge movement of;

$$Q_{out} = V_{+} \times C_{p} + V_{\text{int}} \times C_{\text{int}} \quad , \tag{3.3}$$

results an output voltage of;

$$V_{TDI} = V_{+} + \frac{V_{+} \times C_{p}}{C_{TDI}} + \frac{C_{\text{int}} \times V_{\text{int}}}{C_{TDI}} \tag{3.4}$$

It is important to eliminate the term associated with C_p; V+ can be set according to output requirement which is in this case 1.2V. In order to cancel the offset associated with C_p term, a subtract circuit involving an op-amp and a zero input current channel to create the offset is realized. This circuit will be explained in the following section.

Since issues related to the TDI design are pointed out designed TDI amplifier is to be clarified. There are two important issues about the TDI amplifier used. First, it should have moderate gain, in order to connect the bottom plate of the amplifier to exactly 1.2V and it should have good slew rate, with an acceptable phase margin, in order not to allow too much ringing, since the amplifier must be fast enough to settle in less than 100ns. The amplifier should have as large as possible output voltage swing and minimal power consumption.

Chosen topology for the op-amp is two stage, differential NMOS input stage followed by a common source output stage with nulling resistor compensation. A cascade amplifier is not appropriate since it tends to limit the output voltage swing and resistive compensation is preferred instead of capacitive compensation in order to eliminate the effect of right plane zero with lesser power consumption. Designed amplifier is shown in Figure 3.9.

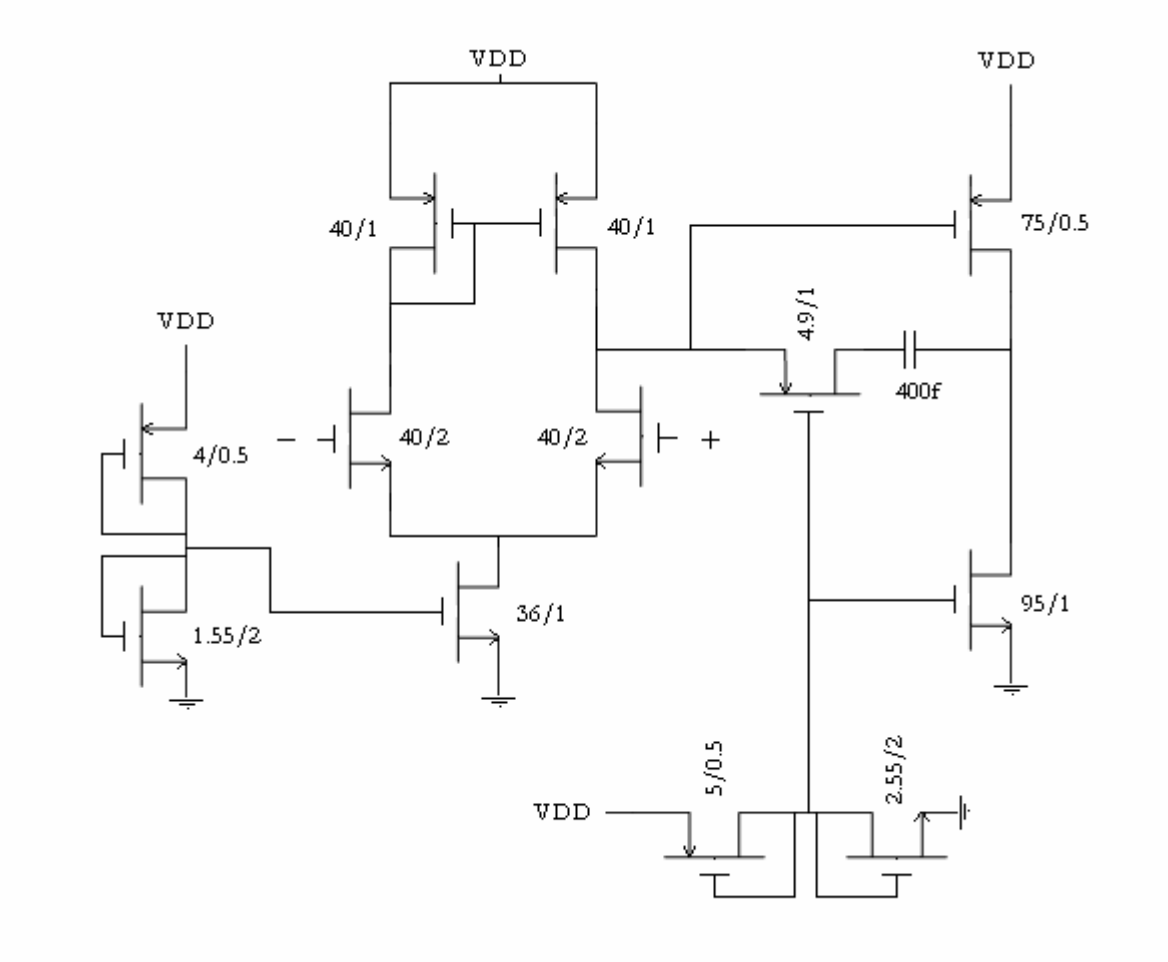

Figure 3.9: Schematic of TDI amplifier

Amplifiers gain is 66dB, with a power consumption of 1.82mW. The amplifier has a phase margin of 61 degree. Amplifiers slew rate is larger than 100V/μsec.

3.3.3 Offset Cancellation and Automatic Gain Adjustment

Throughout the implementation section, although they were taken care for during the design, two important phenomenas related to switch capacitor circuits namely charge injection and clock feedthrough are not discussed. It is important to describe these effects here first.

Clock feedthrough effect is due to the capacitive coupling from the gate to both source and drain, allowing charge to be transferred from the gate signal (generally clock) to the drain and source nodes [21]. In [22] this effect's error voltage is given as:

$$\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H}, \qquad \textbf{(3.5)}$$

where C_{ov} is the overlap capacitance per unit length, C_H is the hold capacitor the switch is connected and V_{CK} is the peak to peak value of the gate signal. Clearly all the integration capacitors, which are controlled by INT and RESET switches experience this error. However since it is a constant value, it can be removed from the output easily.

The second effect, charge injection, is due to the charge in the channel being injected to the source or drain regions, when a switch is closed. Consider a switch where the clock, CK is high enough, hence input, V_{in} is tracking output, V_{out}. In this case the charge in the channel of NMOS device, Q_{ch} is given as:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}), \quad \textbf{(3.6)}$$

where W and L are width and length respectively, with C_{ox} being oxide capacitance. V_{DD} is the supply voltage (also high level of CK) and V_{TH} is the threshold voltage. When the switch is closed, this charge will split between source and the drain, creating an error at the output. However this error is not constant in terms of fraction. How this charge will split in between drain and source regions is dependent on many parameters such as the impedance to the ground in both terminals, the level of the voltage being sampled and even to the transition time of the CK [21][22].

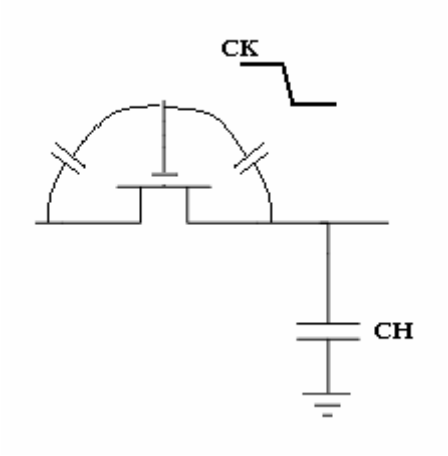

Figure 3.10: Parasitic capacitances that cause clock feed through effect

Using complementary switches is a way to overcome charge injection errors. In this case as in Figure 3.11, a pair of MOS devices is driven by two different phases of CK. The idea is that since one device's channel is opening the other one will be closing. If the charge the opening channel absorbs is equal to that of the closing channel produces then no error is presented to

the output. However this is valid at only one voltage level and in reality either PMOS or NMOS device's error is dominating.

Another approach is to use a dummy switch to eliminate the error. In this case as in figure, a dummy switch is driven with the inverse phase of CK. Considering the charge will split up equally between the source and drain (which is not correct), the dummy transistors size can be set to half of the sampling switch. This way the charge one transistor introduces will be eliminated by the other one, since they operate with different phases.

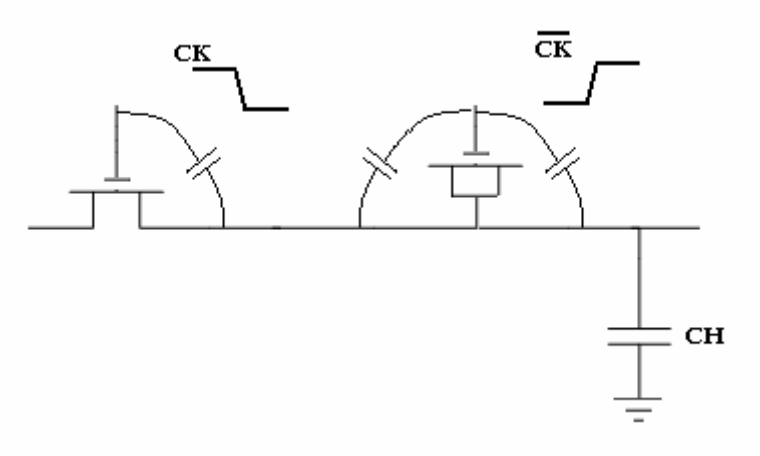

Figure 3.11: Schematic of dummy switch method

Another approach named bottom plate sampling eliminates both clock feedthrough and charge injection quite better than the above mentioned ones, however, it requires that the input is a voltage, that can be sampled twice, which in the case of a current input is not applicable, as in this case.

Thus, a nulling switch added to the input, which is operating in inverse phase of INT signal, to suppress the effect of charge injection. Also since error is dependent on the transistors aspect ratio, minimum size devices are used which have aspect ratios as 0.4 / 0.5 μm. Clock feedthrough effects are removed through differential operation.

In the previous section the necessity to remove the offset due to the parasitics associated with TDI were explained. As in all cases where a constant is unavoidable, employing a differential stage is a convenient solution. At this point first the error must be recreated, and then must be removed from the TDI output, before the output buffer receives it for ADC sampling. The error, aside one related to C_p, includes the constant clock feedthrough effects at the input.

The offset cancellation circuit consists of an amplifier and a whole channel with a dedicated TDI stage to create the switching and parasitic errors. TDI voltage is the input to the circuit, while error is created in. The error is generated through four input cells (four storages of four detectors) with zero input current. Hence only the switching errors and the bottom plate parasitics are created and subtracted. The circuit is shown in Figure 3.12.

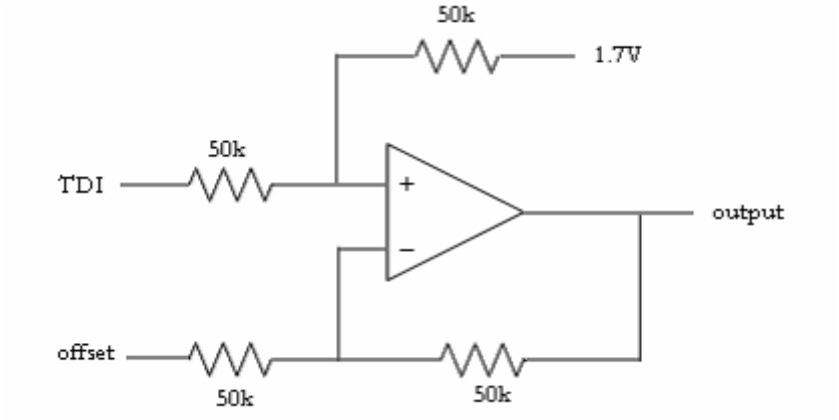

Figure 3.12: Offset cancellation circuit

Both signal and Offset are asserted on 1.2 V, as the positive input of TDI amplifier is set. When offset is removed in order to shift the output voltage to 1.7 V – 4.5 V range, as an output requirement, 1.7 V is also added. The output voltage can be calculated as below;

$$V_{-} = (V_{TDI} + 1.7) / 2 \quad \textbf{(3.7)}$$

$$V_{out} = 2V_{-} - V_{offset} \quad \rightarrow \quad Vout = V_{TDI} - V_{offset} + 1.7 \quad \textbf{(3.8)}$$

The op-amp schematic is as in Figure. The topology is same as in the op-amp used in TDI stage, a differential stage followed by common source stage. The op-amp operates with supplies 0 V and 5 V, with a total current of 400uA, results a power consumption of 2mW. Gain of the op-amp is 60.4 dB with a phase margin of 71 degree. Slew rate is 100V/μsec for a load of 1pF.

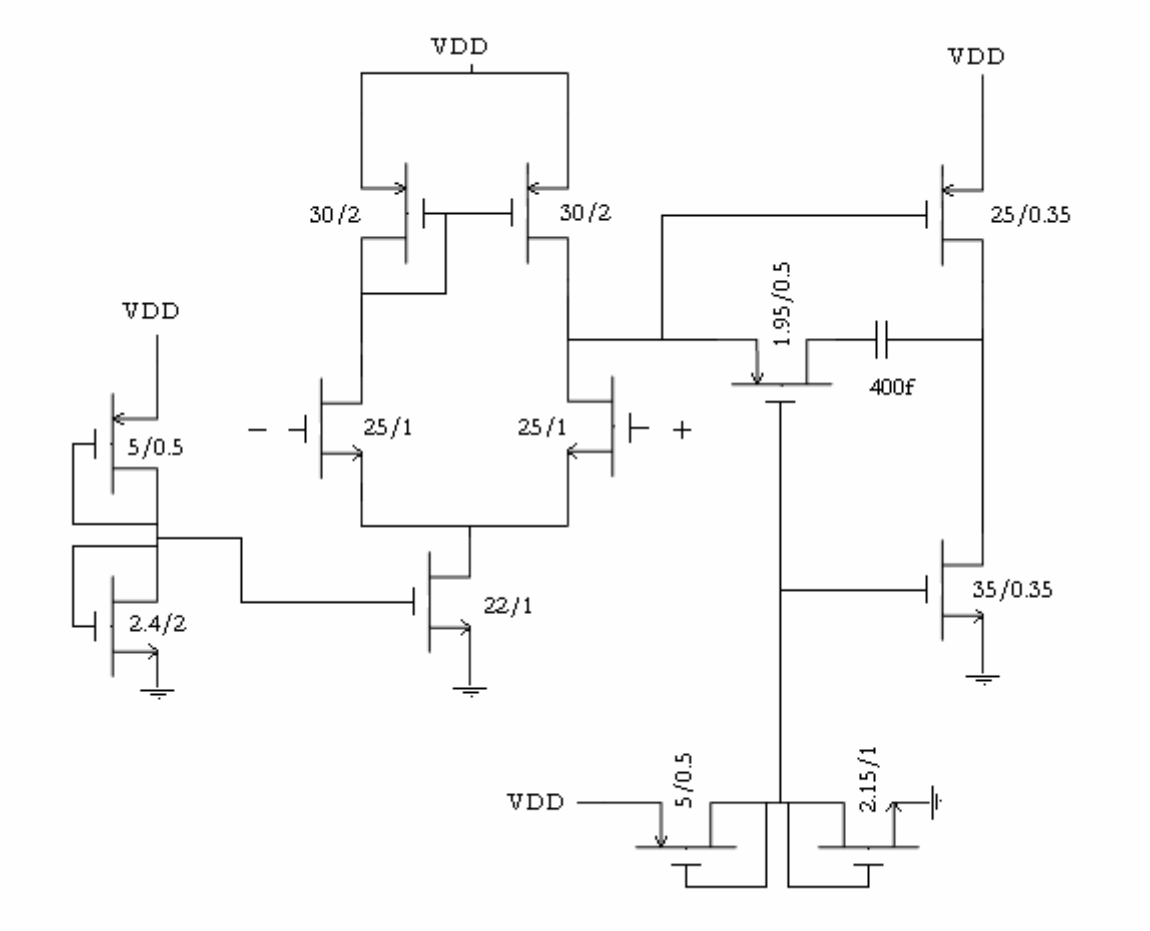

Figure 3.13: Schematic of amplifier used in offset cancellation circuit

One of the ROIC requirements is automatic gain adjustment in case of a dead pixel. For this design, only a single malfunctioning device is considered. Then, when one or more pixels are malfunctioning on a channel to be read, output is multiplied by 4/3, 1.33 without those pixels being connected to the output automatically. This situation is handled by varying the resistors used at the adder-subtracter circuit through a complementary switch changing the resistor ratios as 1.33 as shown in Figure 3.14.

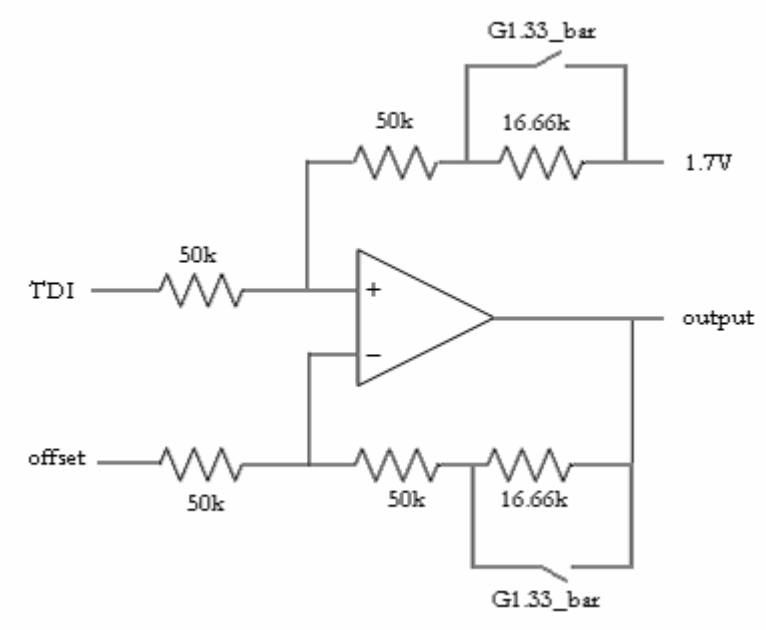

Figure 3.14: Circuit that removes offset as well as performs automatic gain adjustment

G1.33 signal is a bus, driven by a NAND gate according to the data of pixel functionality. The NAND gate is as represented in figure a building block of every channel. At every clock cycle during a read operation, one of the NAND gates, belonging to the channel to be read drives G1.33 bus. If any of the detectors is malfunctioning, (i.e. a zero appears in one of the inputs of the NAND gate) G1.33 is set to high, 5V. The circuit implementation is shown in figure. The transistors enabled through channel select signal determine the channel being read drives the bus.

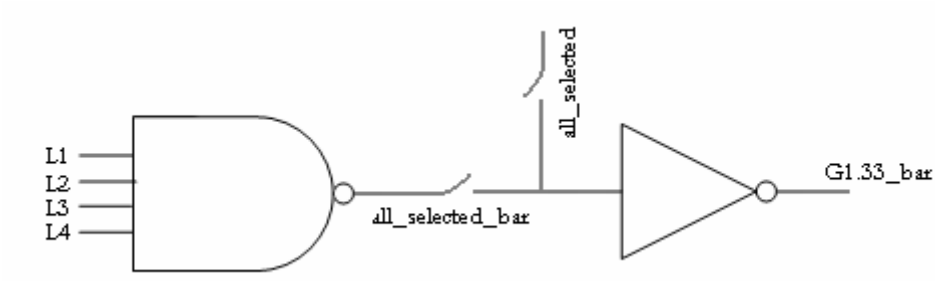

Figure 3.15: Digital logic to set automatic gain adjustment control signal, G1.33_bar

Whenever G1.33 is high, output voltage can be calculated as below.

$$V_{-} = (4V_{TDI} + 3x1.7) / 7 \qquad \textbf{(3.9)}$$

$$V_{out} = 7/3V_{-} - 1.33xV_{offset} \quad \rightarrow \quad Vout = (V_{TDI} - V_{offset})\ x1.33 + 1.7 \qquad \textbf{(3.10)}$$

Resistors are selected as 50K in order to minimize power consumption at this stage, however it is a trade of between noise performance and power consumption. If more power consumption is allowed, smaller resistors can be used, which will decrease noise contribution of this stage.

3.3.4 Output Buffer Design

Output buffer is designed for a load of 10pF with a shunt resistance of 1MΩ. Required ROIC output response is given in figure. From Figure 3.16, it is known that a 1mV settling error is allowed in 100ns rise time. Again high slew rate and good phase margin are required to meet the specifications.

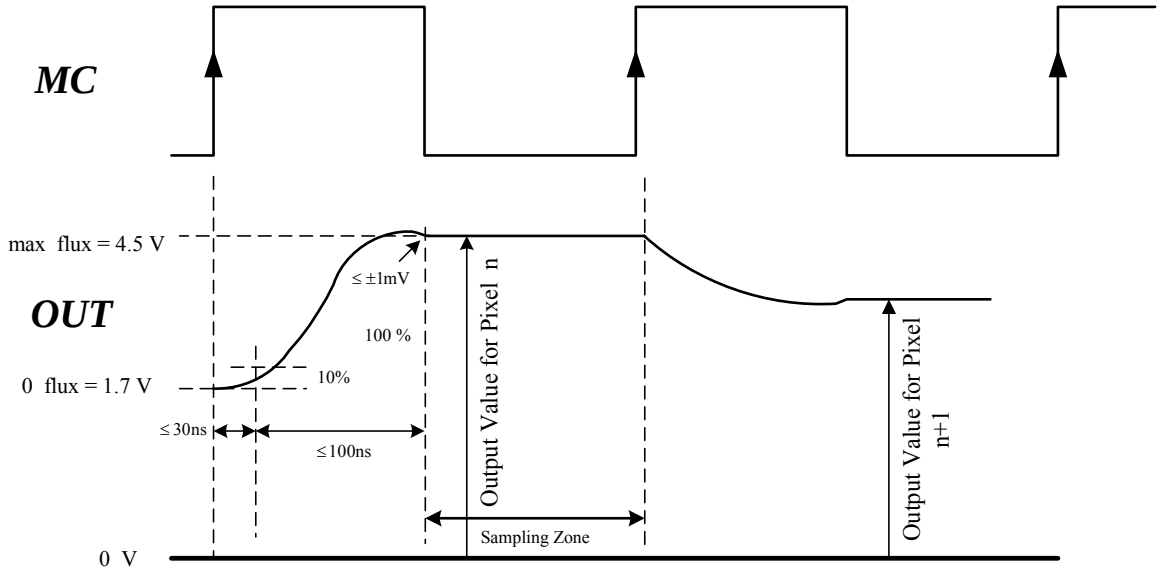

Figure 3.16: Output waveform

As the output buffer, a two stage op-amp with a differential stage followed by a common source stage is used, with its output connected to its negative input. Designed amplifier has a gain of 68.7 dB with a phase margin of 45 degree. Its power consumption is 5.9 mW. Slew rate is 65V/μsec. with the load being 10pF with a shunt resistance of 1MΩ as stated above.

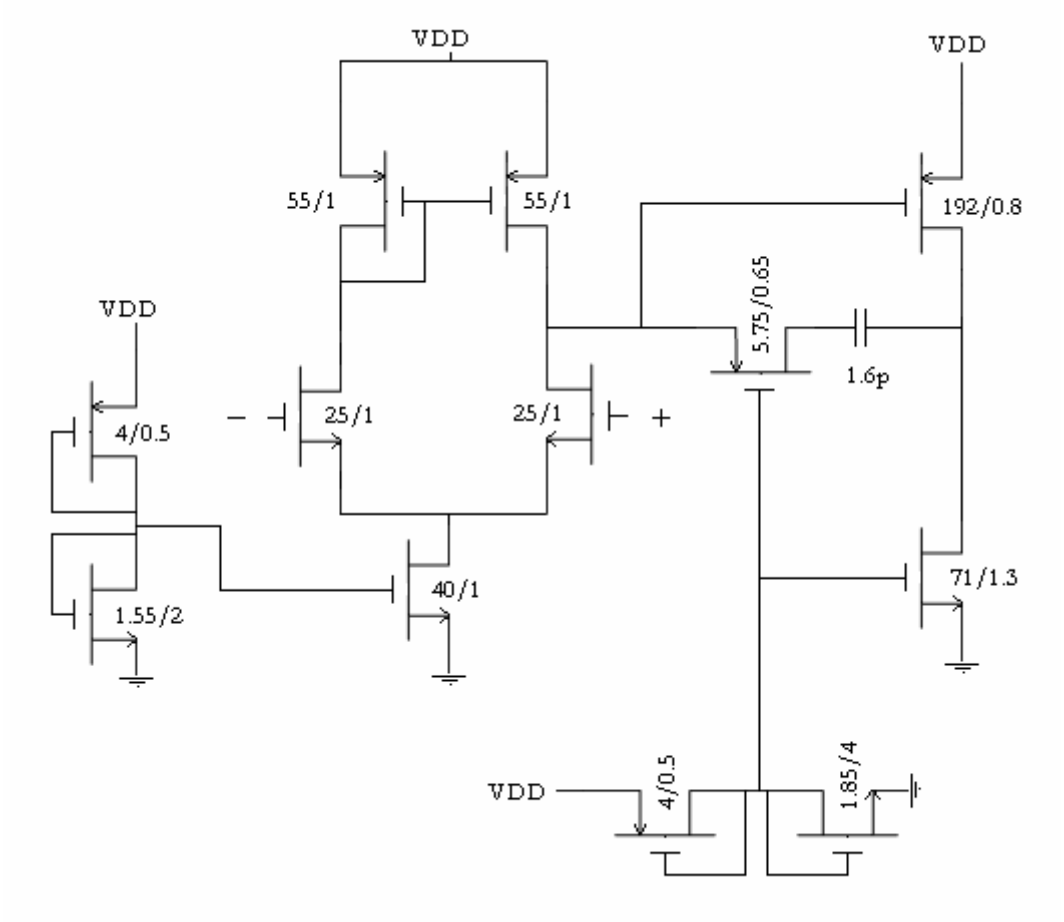

Figure 3.17: Schematics of amplifier used as buffer

3.3.5 Digital Circuit Design

Digital circuits consist of three main blocks. A main control block generates required INT, RESET, S1, and S2 signals for every channel and offset cancellation circuit, in addition to 7 bit channel select signal. An interface block programs the ROIC through serial and parallel interface. Finally, a block of decoders carries out the selection of signals generated from the control logic to be activated at the ROIC.

Digital control circuit functions by the help of two 3.3V clock signals. The first is the master clock signal CLK, which can set up to 5 MHz. All the control signals used in the ROIC are synchronized with this clock. The second is the integration clock INT, setting the integration time.

Main control block and interface circuits are designed through automatic synthesis. Logic is designed by Verilog programming language. Following the verification in code level, design is synthesized by using Synopsys design compiler and the netlist generated is mapped to AMS

CORELIB 3.3V standard cell library elements. Following design verification at the schematics level, physical design is created using Silicon Ensemble tool. Decoders and level shifters (3.3 V to 5 V digital converters) are designed with full custom methodology.

3.3.5.1 Main Control Circuit Design

As explained above, main control block generates S1, S2, INT and RESET signals. Every detector in a channel has its own data path (logic creator). Since detector 1 includes 11 storages, detector 2 includes 8 storages, detector 3 includes 5 and detector 4 includes 2 storages, control signals generated are 4, 4, 3 and 2 bits for detector 1, detector 2, detector 3 and detector 4. Also data paths have 4, 4, 3 and 2 bits frame counters to generate control signals. Aside from these blocks, main control block has a data path to create same control signals for offset cancellation stage. A block diagram of the circuits is shown in Figure 3.18.

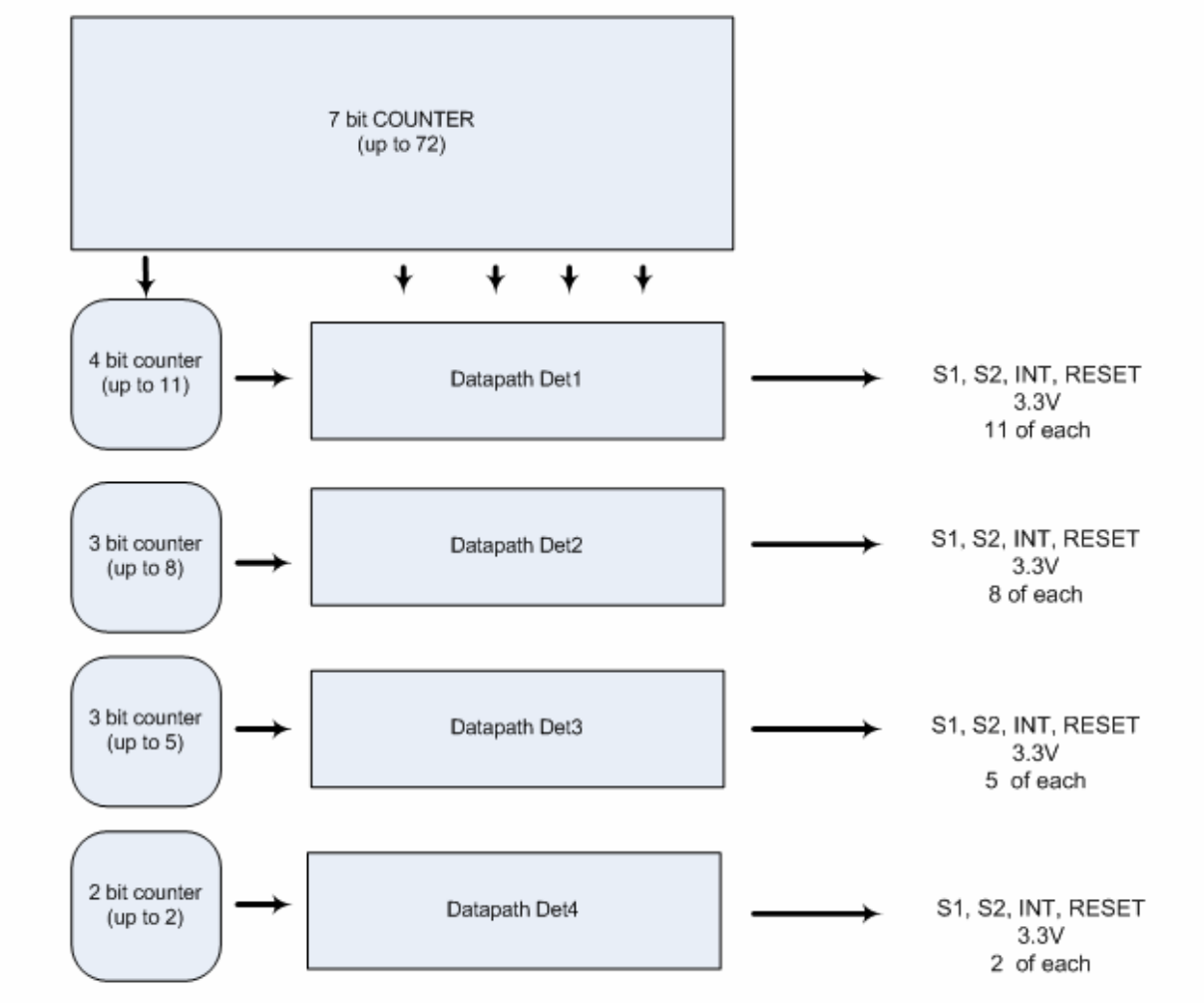

Figure 3.18: Block diagram of main control block

This circuit is designed at the RTL level, using Verilog programming language. Following verification in this level, circuit is synthesized using Synopsys and mapped to standard cell library elements of AMS CORELIB. Physical design is generated by Silicon Ensemble for AMS C35B4 (four metal, 2 poly) process.

3.3.5.2 Interface Circuit Design

The second digital block is an interface circuit which is used to program the ROIC. Programming can be achieved through serial or parallel interface. In parallel mode gain settings, bypass or TDI mode can be programmed. Pixel deselection as well as pixel functionality programming is achieved through serial interface only.

Parallel Interface

Operation through parallel interface is determined by the input SERIAL_bar. When this signal is low, circuit operates in the parallel mode. For operation in the parallel mode five inputs are required: GAIN2, GAIN1, DIR, BYPASS1 and BYPASS2. Values of these inputs set the gain setting, TDI direction and bypass mode as in tables.

GAIN2	GAIN1	Cint (pF)	Cint (pC)	Gain Ratio
0	0	0.36	1.00	1.29
0	1	0.46	1.29	1
1	0	0.70	1.96	0.66
1	1	0.92	2.58	0.50

Table 3.3: Gain settings according to gain bits

DIR	BYPAS2	BYPAS1	MODE
0	0	0	TDI along +Y (default)
0	0	1	BYPASS on diode n°1
0	1	0	BYPASS on diode n°2
1	0	0	TDI along –Y
1	0	1	BYPASS on diode n°4
1	1	0	BYPASS on diode n°3

Table 3.4: TDI and test mode settings according to programming bits

With user inputs, four gain settings can be achieved; 1.30, 1, 0.66 and 0.50. Also bidirectional scanning is possible in parallel mode. There are four test modes four each detector in the channel. Control signals for bypass mode according to user input are generated in this block.

However realization of bypass mode is held through S2 signal described in the decoders section.

Serial Interface

Whenever SERIAL_bar is low, the circuit operates in the serial mode. In the serial mode, serial data is input to the circuit through SERIAL_DATA input. Frames are defined between two low edges of INT clock. Data must be available in SERIAL_DATA input following the ¼ CLK period of CLK's low edge. This data is first stored in a shift register, following the next INT fall edge; data in the shift register is transferred to the control register. Both interfaces program the ROIC by use of a control register as shown in figure. With the first cycle being discarded, totally 25 cycles are required to program the ROIC in serial mode.

SIGNAL	CNT	GAIN2	GAIN1	DIR	BYPAS2	BYPAS1	SELECT	PGM	8 bit data for selection/deselection of pixel								8 bit pixel program address							
bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	WORD CONTROL : 8 BITS								DATA WORD : 8 BITS								ADDRESS WORD : 8 BITS							

CNT, at high level, enables data writing to bits 1 to 6, setting values for GAIN2, GAIN1, DIR, BYPASS2, BYPASS1 and SELECT. At low level of CNT, these bits remained unchanged.

- GAIN2 and GAIN1 bits control the gain settings as shown in Table 3.3.
- DIR, BYPASS2 and BYPASS1 control bypass mode and TDI direction as shown in Table 3.4.
- SELECT at high level enables the selection of all pixels (i.e. all detectors are assumed to be functional). At low level, pixels operate according to their programmed data.
- PGM at high level operates the ROIC in programming mode and pixel functionality data is written to the latches in the channel. At low level, no programming is done and pixel functionality data is kept as is.

Bits 8 to 15 include the pixel functionality data. A high value sets a pixel as functional while a low value sets the pixel to be not functional. The first 4 bits (8 to 11), include the functionality data for the left four detectors and the last 4 bits (12 to 15) include the functionality data for the right four detectors.

- Bits 16 to 23 include the programming address. Bit 16 represents that address is being at the upper or lower part of the array. If high, top part of the FPA is being programmed and if low bottom part of FPA is being programmed. Remaining 7 bits represent addresses from 1 to 72 for every channel. Remaining possible addresses at this register are considered as non-valid.

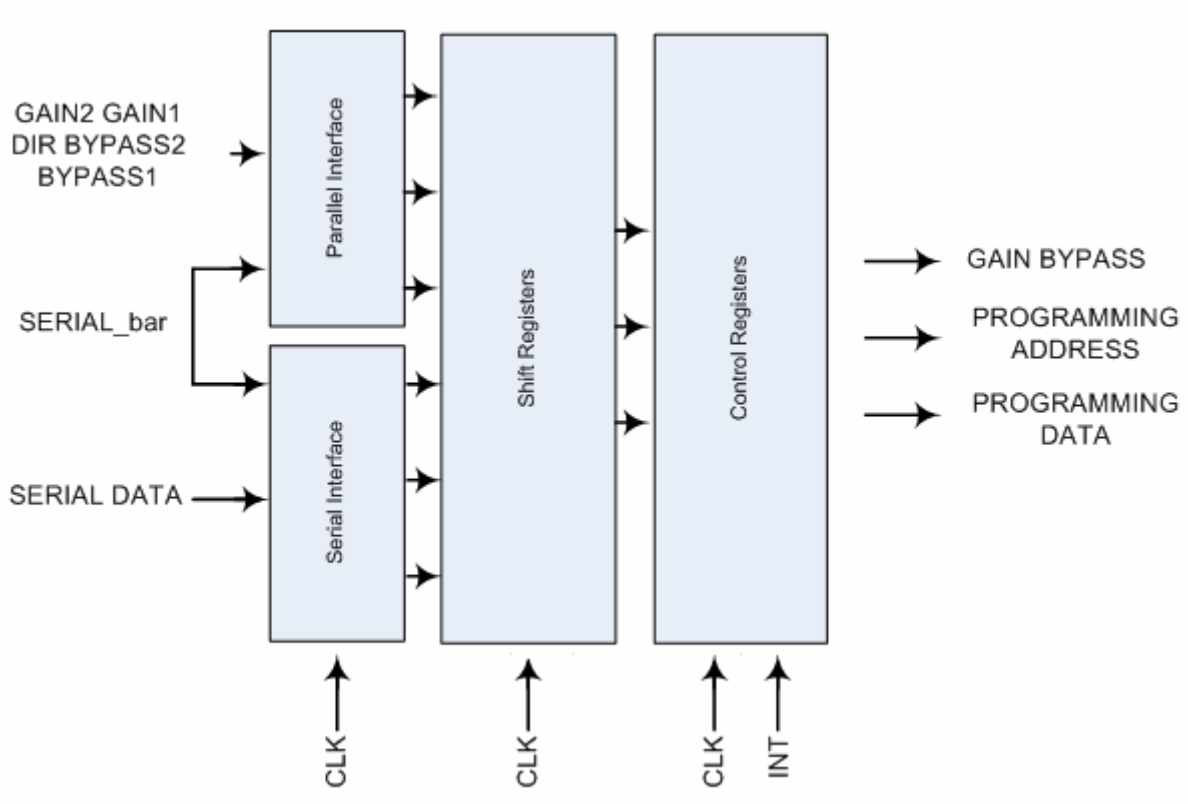

Figure 3.19: Block diagram of interface circuits

Block diagram of the mentioned circuit is as given in figure. This circuit is designed at the RTL level, using Verilog programming language. Following verification in this level, circuit is synthesized using Synopsys and mapped to standard cell library elements of AMS CORELIB. Physical design is generated by Silicon Ensemble for AMS C35B4 (four metal, 2 poly) process.

3.3.4.3 Decoder and Level Shifter Design

ROIC analog blocks operate at 5V, hence control signals must be at 5V as well. Due to the signals generated from standard cell library which operate at 3.3 V a block to convert voltage from 3.3V to 5V is designed.

Signals from the main digital control circuit come to this level shifters first and than passed through a decoder sized according to their respected bit size. For example S1, S2, INT and RESET signals of first detector are 11 bits; hence a 4x16 decoder is used with 5 outputs set as invalid. In all cases, zero outputs of detectors are considered invalid as well.

It is common to observe glitches in combinational digital circuits due to clock feedthrough effects and substrate noise during state change of signals. Glitches does not result an error in the digital domain, however for precise operation as in this case, analog blocks should have control signals with minimal glitches. This is especially critical for S2 signal in this case. Consider a 1ns glitch is received to S2 signal of a detector that is not to be connected to the output at an instant of time. 1 ns pulse width would not be enough to discharge the capacitor to output but it will connect to bottom plates of the capacitors and may result significant charge sharing between two. In order to prevent this, a flip flop is added right after the digital circuits. Employing a flip flop greatly reduces the glitches at the output.

Finally, in order to drive paths with parasitic loads in the order of 500fF, digital buffers (series of inverters with sizes increasing to the output as in design of a super buffer) are used. Circuit architecture is represented in Figure 3.20.

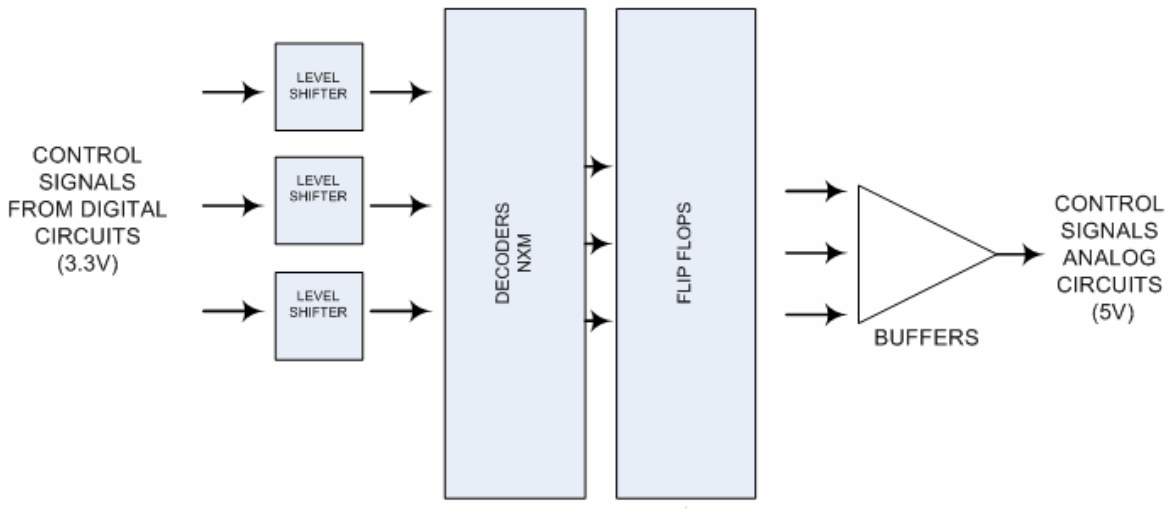

Figure 3.20: Block diagram of final digital stage, including level shifters, decoders, flip flops and buffers

BYPASS (test) mode

In order to deselect malfunctioning detectors along the array, ROIC is to be operated in test mode. This is handled by bypassing one detector to output for a determined radiation level. Observing single detectors voltage at the output, detector is known to be functioning or not.

The operation of the bypass mode is handled through S2 switch. All the channels in a 72x4 ROIC are operated by same INT,S1,S2 and RESET signals, however they are connected to the output through a channel select signal, which is passed through an AND gate with S2. Hence all storage capacitors having S2 are ready to transfer their charge to the output when channel select is activated together with S2. Bypass property limits the number of detectors added to the output to one through disabling S2 signal for those detectors that should not add to the output according to user programmed data. ROIC has four bypass modes, each one corresponding to connection of one detector in the channel to the output. The logic is as in figure. This logic takes place between the level shifters and decoders Figure 3.21.

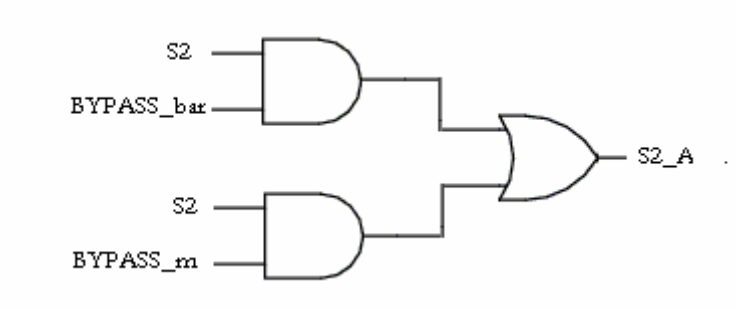

Figure 3.21: Logic to realize bypass control through S2 switch

3.4 Physical Design

Physical designs of digital circuits operating at 3.3V are done by automatic layout generation with Silicon Ensemble tool. Layouts of all remaining blocks are done by full custom.

288x4 ROIC is not submitted for fabrication yet. However physical design of all ROIC blocks except the digital circuits are finished and are all connected together. In this section layout of important analog sub blocks are shown and their sizes are given. Finally a previously submitted 72x4 ROIC's layout is shown as representative to the 288x4 ROIC.

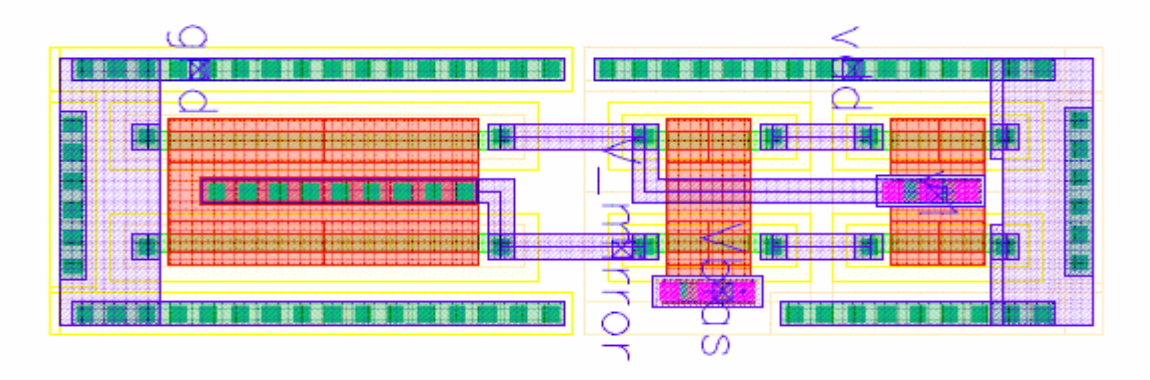

Figure 3.22: Layout of CMDI unit cell, size 8.10µm x 27.15µm

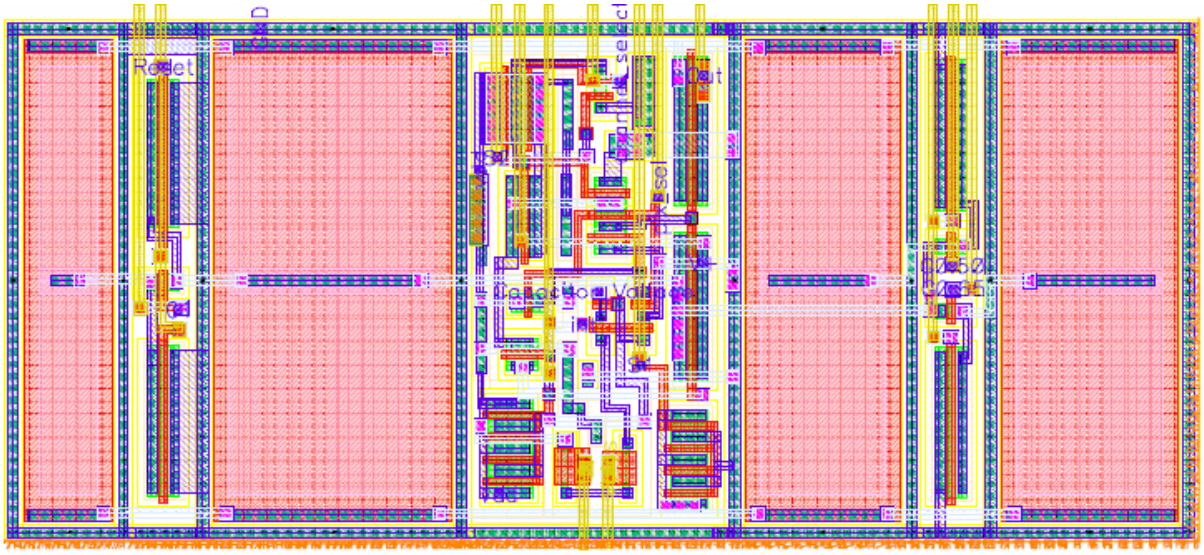

Figure 3.23: Layout of Input capacitor set, four capacitors for four gain settings together with S1,S2 INT and RESET switches, size 34.85µm x 79.55 µm

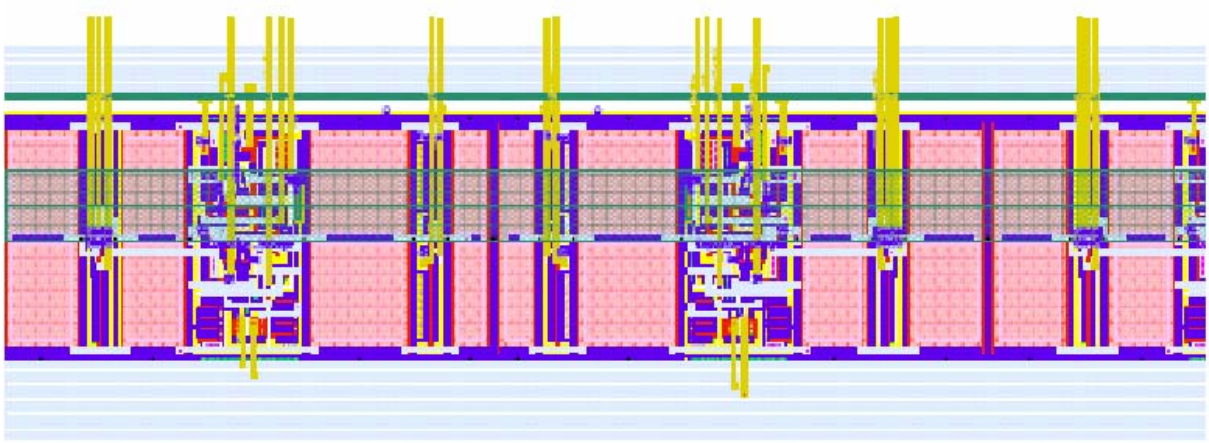

Figure 3.24: Part of layout of a channel, input capacitor sets are repeated with totally 26 in one channel, total size 56µm x 2.810mm including the routing and current sources (400µm). Channel height is dictated by pixel size.

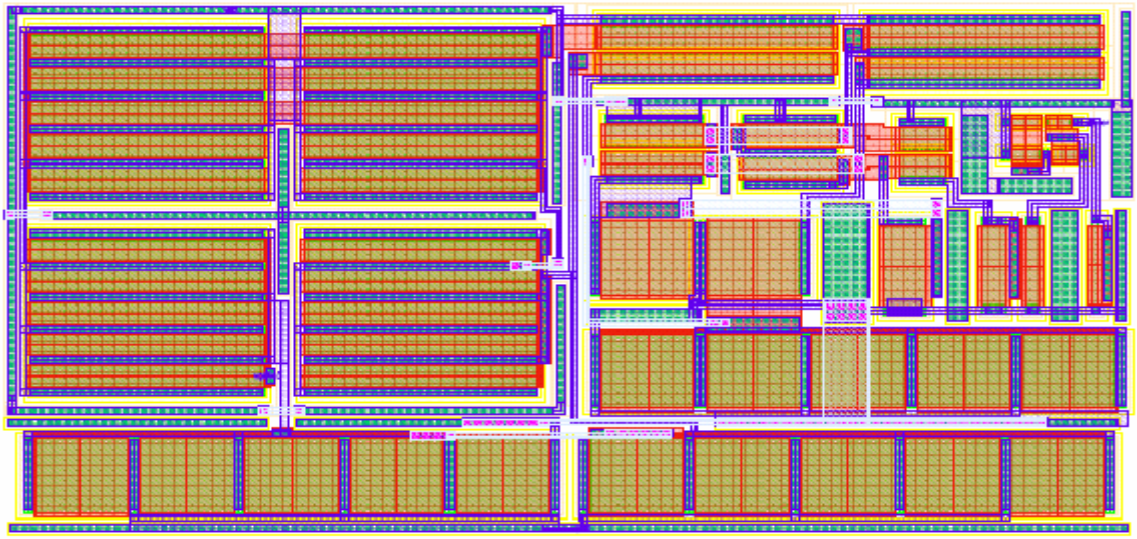

Figure 3.25: Layout of current sources that are designed solely for test purposes, size 97µm x 54 µm

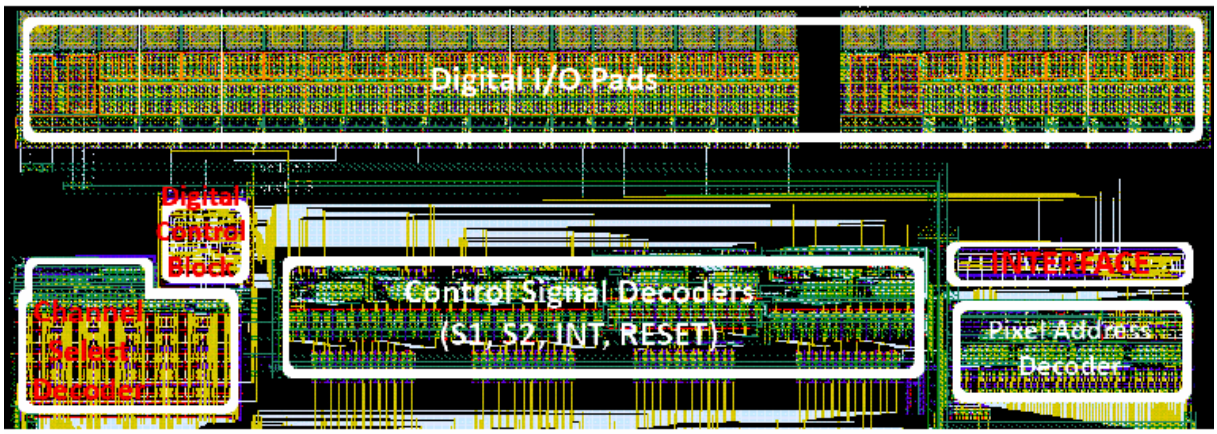

Figure 3.26: Layout of the complete digital blocks with I/O pads. Digital circuit size is 2.810mm x 510µm

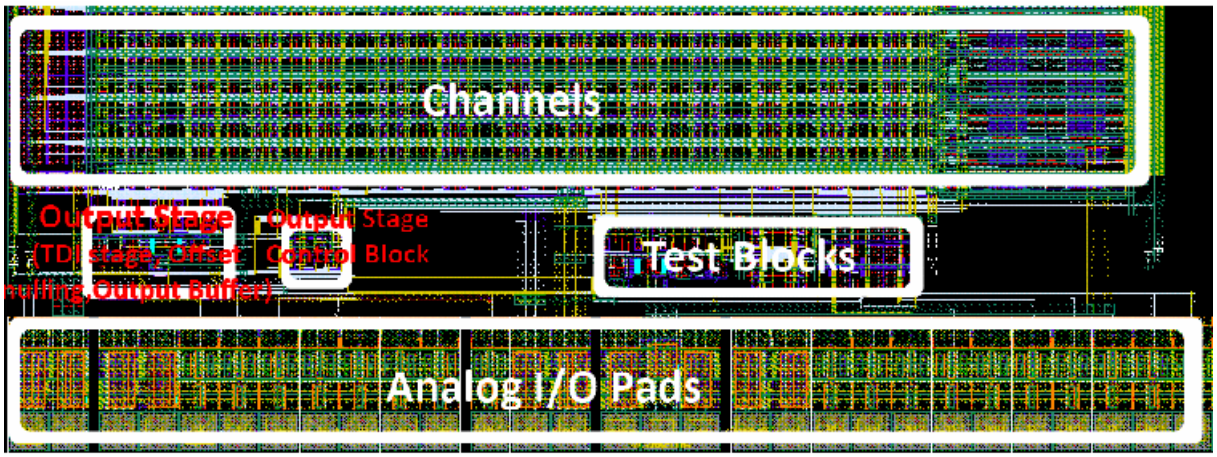

Figure 3.27: Layout of the output stage with I/O pads. Size is 643µm x 200µm, including control logic and excluding channel used for error generation.

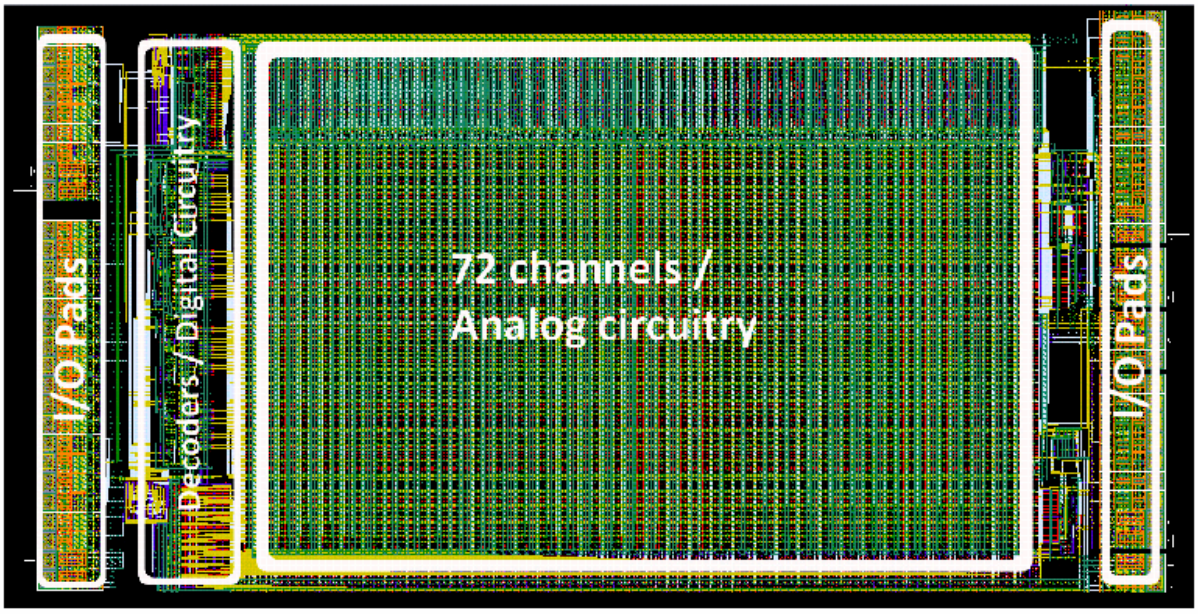

Figure 3.28: Layout of the 72x4 ROIC, size 5.8mm x 3mm.

CHAPTER 4 RESULTS

In this section first simulation results of designed 288x4 ROIC is given. Results are given both on schematics level and extracted level in order to show the effect of bottom plate parasitics. Simulation time of ROIC is extremely long, by long what is meant is more than a week (with a machine of 8 processors and 64G ram) even with a hierarchical set up with the digital control circuits that work at 3.3 V are simulated at the code level. This is due to the amount of the devices that exist in the design (100.000 elements in a block of 72x4 ROIC and 400.000 in 288x4 ROIC). Moreover above mentioned setup is simulated with SPECTRE, and settings as liberal, which is not to be further degraded for analog block performance simulation. Finally RC extraction of the design increases the simulation time dramatically, since not only the elements increase, but the nodes the simulator solves increases too.

Hence best performance analysis of ROIC can be obtained through dividing each circuit assuming the possible loads and simulating with a smaller part. In this sense ROIC digital blocks are separated from the ROIC. Since no simulation tool assuming different models for devices on the same die, four 72x4 blocks are unnecessary and increasing the simulation time. So, for simulation all digital blocks are removed from layout as well as all channels but first three. Hence simulated ROIC has all routing same as 288x4 ROIC's respected 72x4 block, but with 3 channels only in order to minimize simulation time. All digital signals are given to the circuit with appropriate rise fall times.

In the next section noise analysis of the ROIC is given over a single channel. Noise contribution of each block is given as well as calculation methodology.

Finally measurement results from a 1x4 ROIC, the first tape out of this work is represented. Although not much of the functionalities are included in that design, results are still representative.

4.1 Simulation Results of Minimum Input Current

4.1.1 Schematics Results

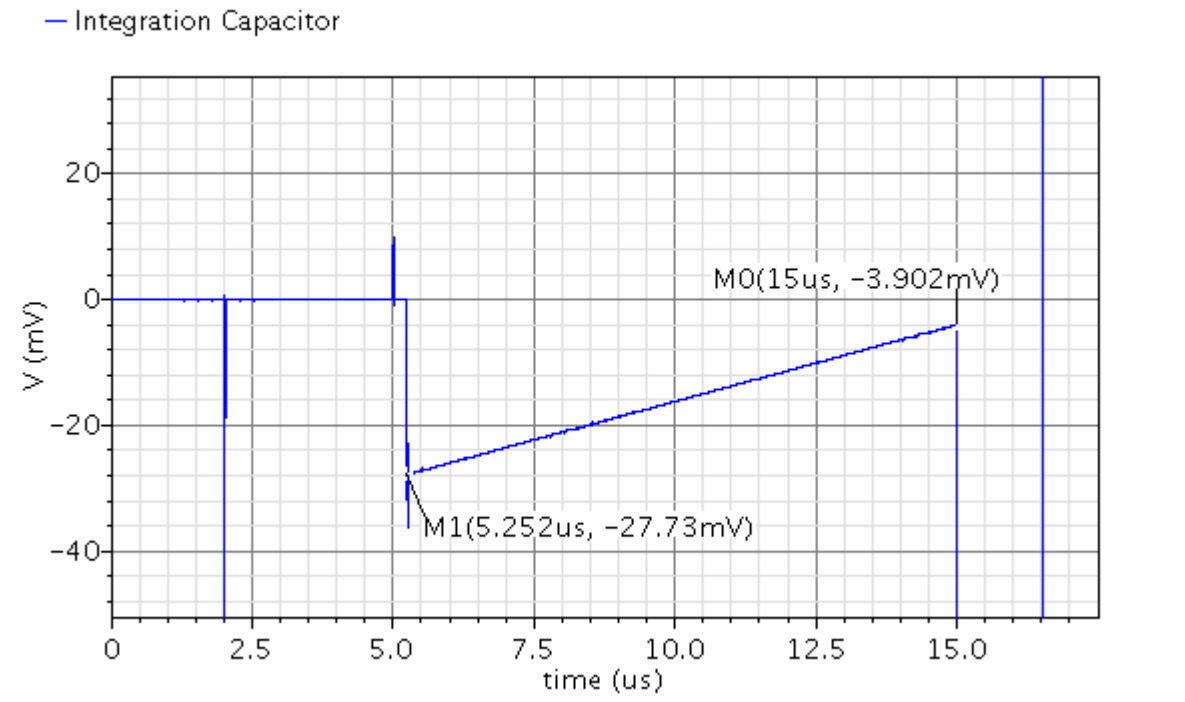

Figure 4.1: Schematic level simulation result at the input, for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

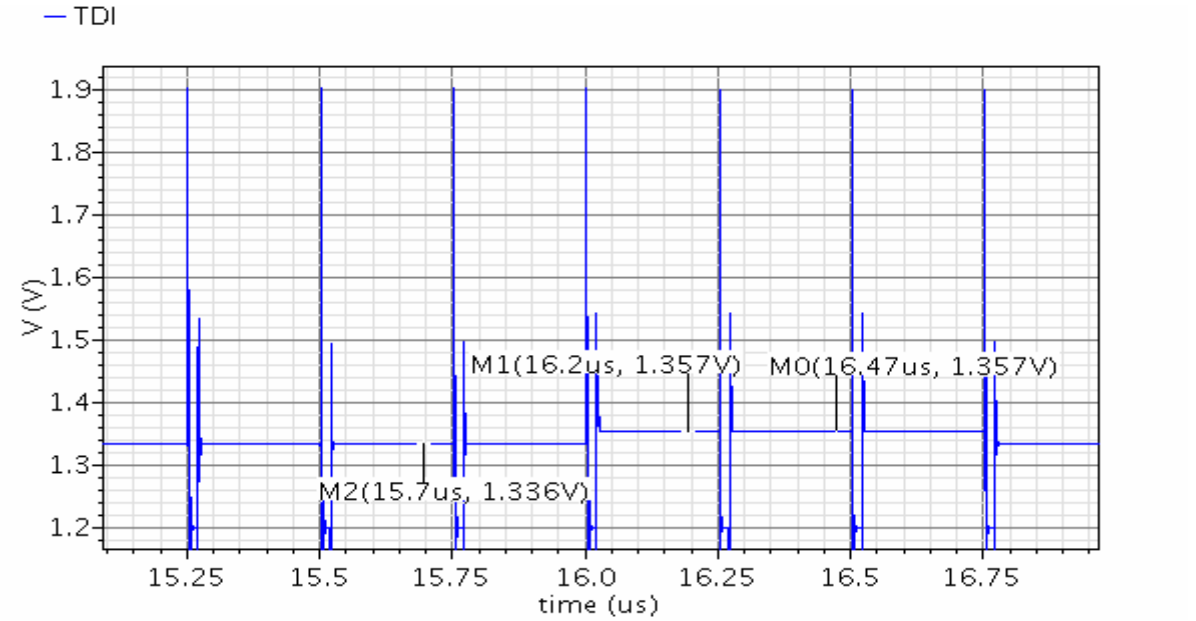

Figure 4.2: Schematic level simulation result at the TDI stage, for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

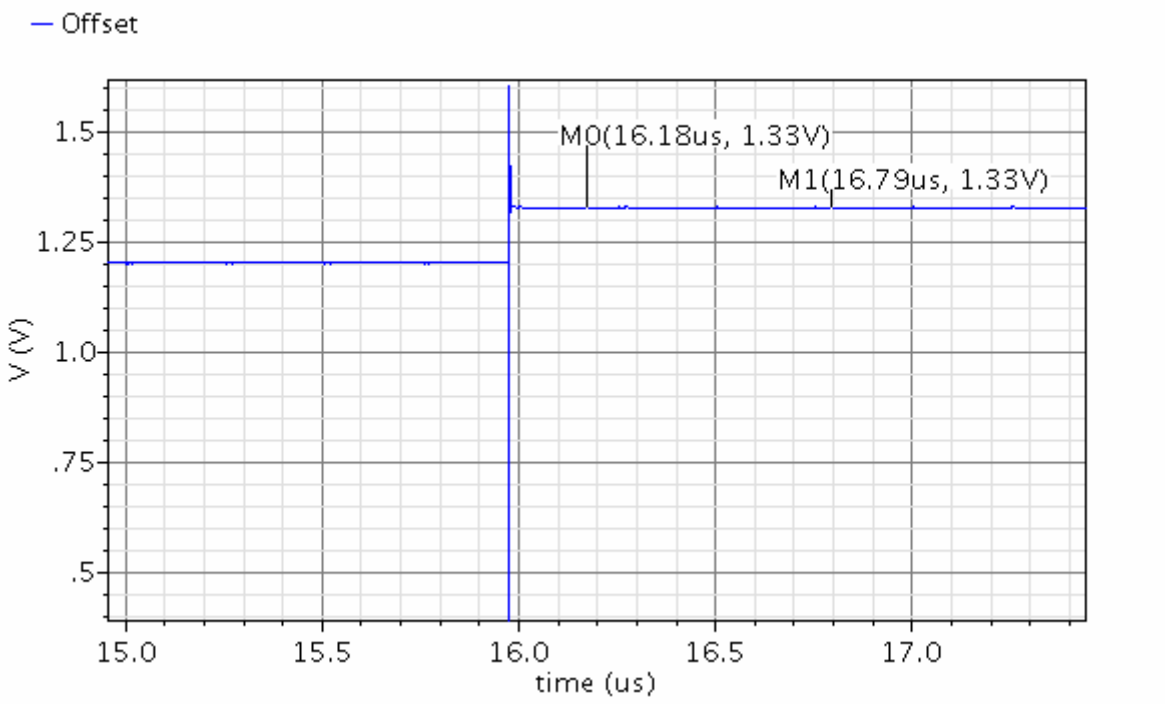

Figure 4.3: Schematic level simulation result at the offset stage, for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

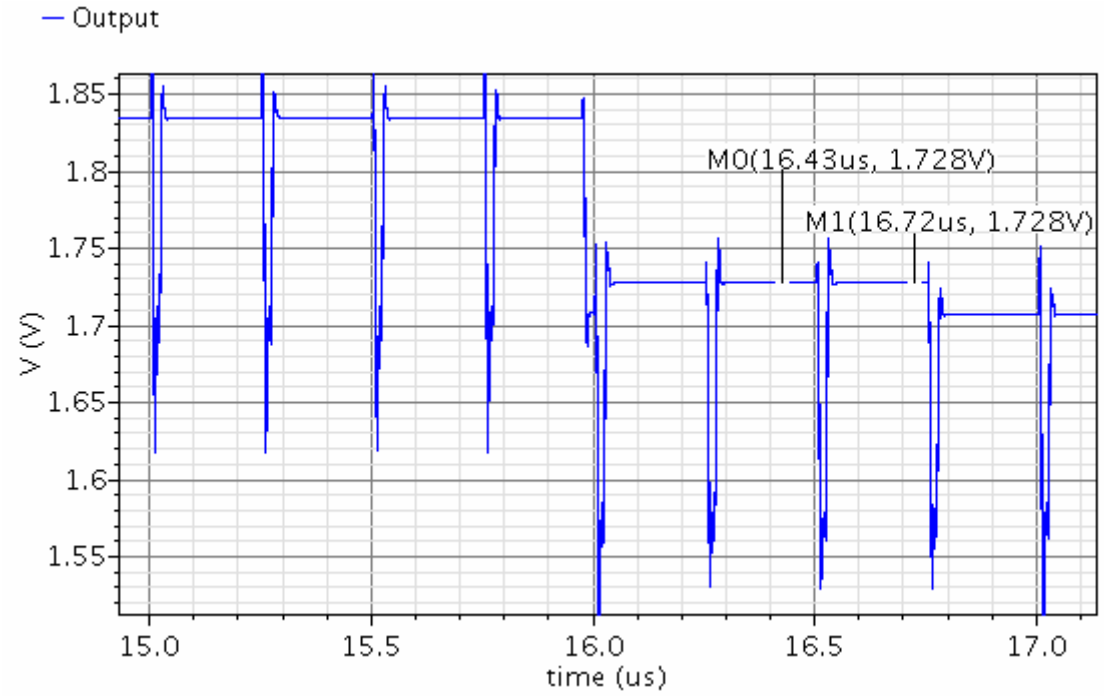

Figure 4.4: Schematic level simulation result at the output , for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 24mV is integrated at the input. At TDI stage 157mV is added (errors exist), at the offset 130mV is observed. Hence at the output 28mV is added.

4.1.2 Extracted Results

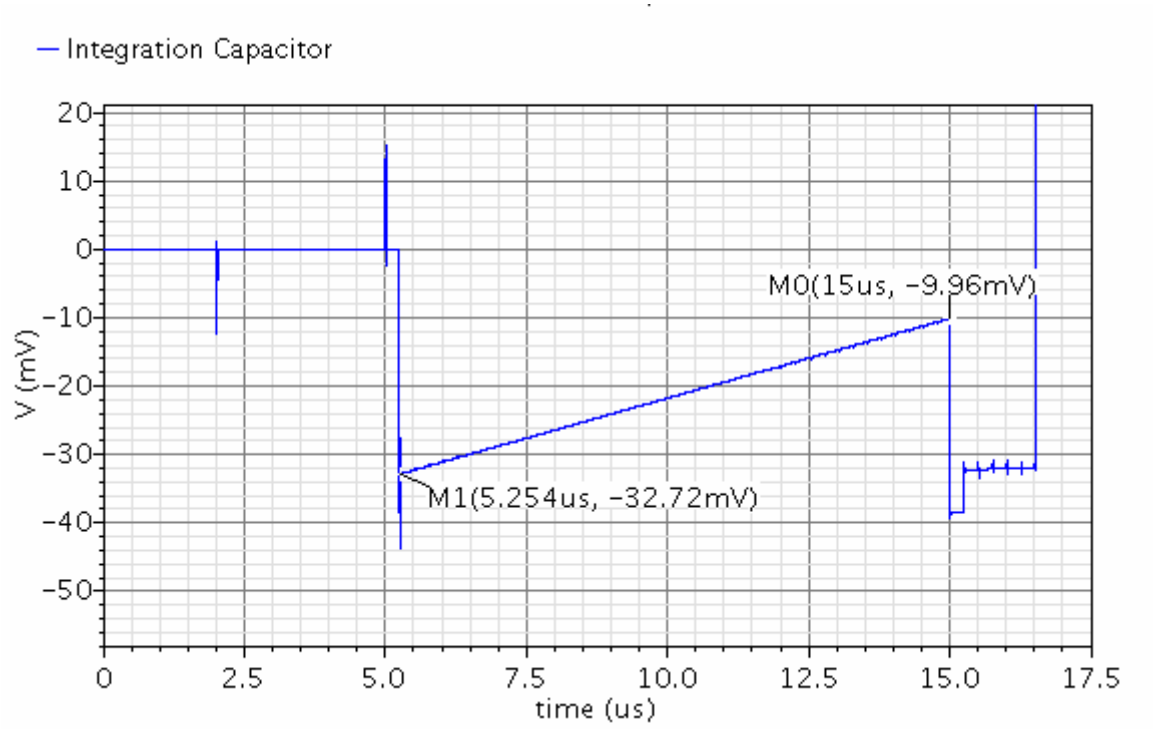

Figure 4.5: Extracted level simulation result at the input, for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

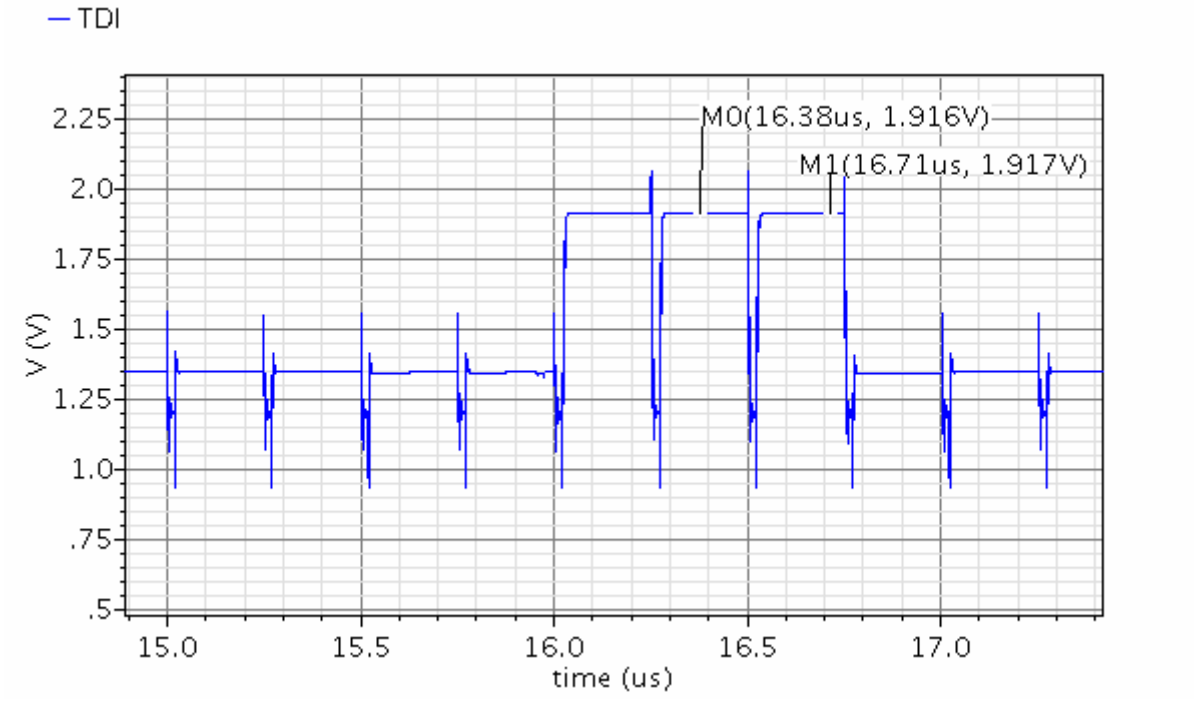

Figure 4.6: Extracted level simulation result at the TDI stage, for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

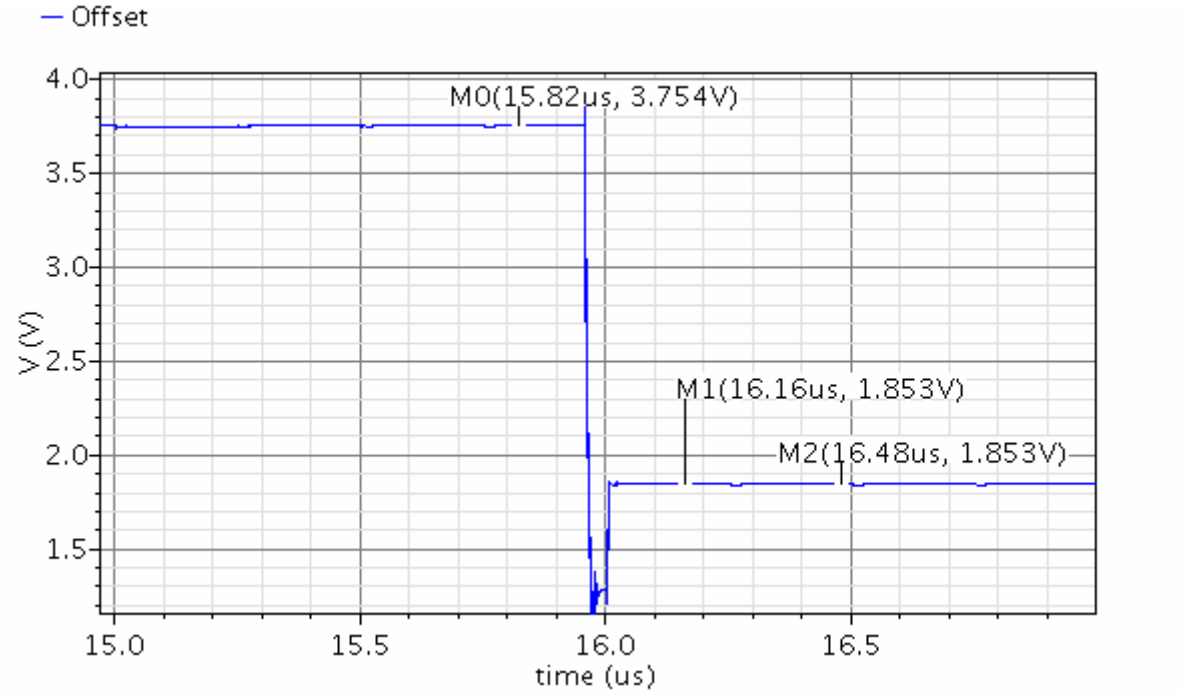

Figure 4.7: Extracted level simulation result at the offset stage, for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

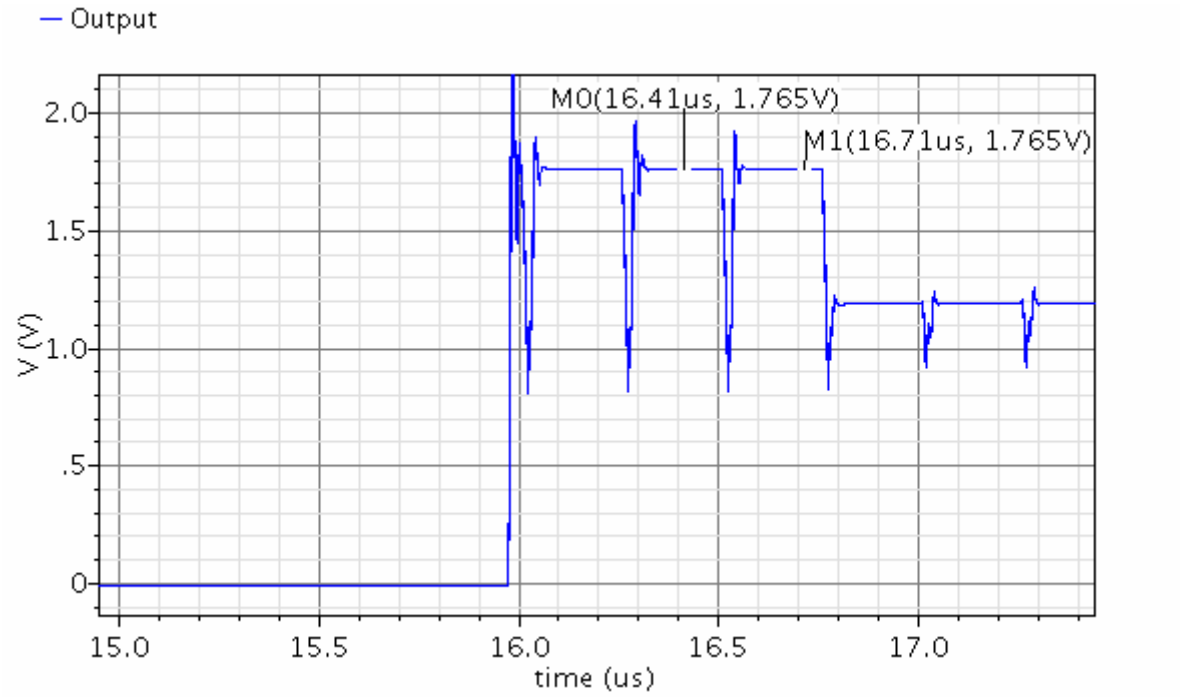

Figure 4.8: Extracted level simulation result at the output stage, for input current of 1.2nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 234mV is integrated at the input. At TDI stage 716mV is added (more errors exist), at the offset 653mV is observed. Hence at the output 65mV is added (There is constant offset of 42mV).

4.2 Simulation Results of Nominal Input Current

4.2.1 Schematics Results

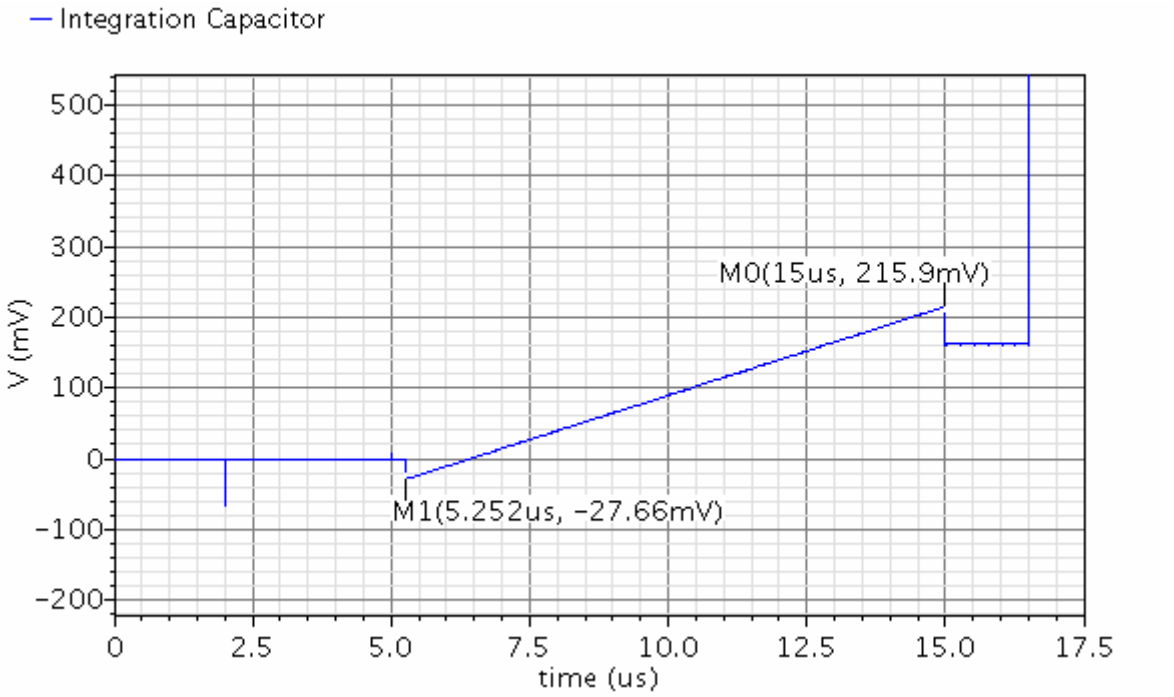

Figure 4.9: Schematic level simulation result at the input, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

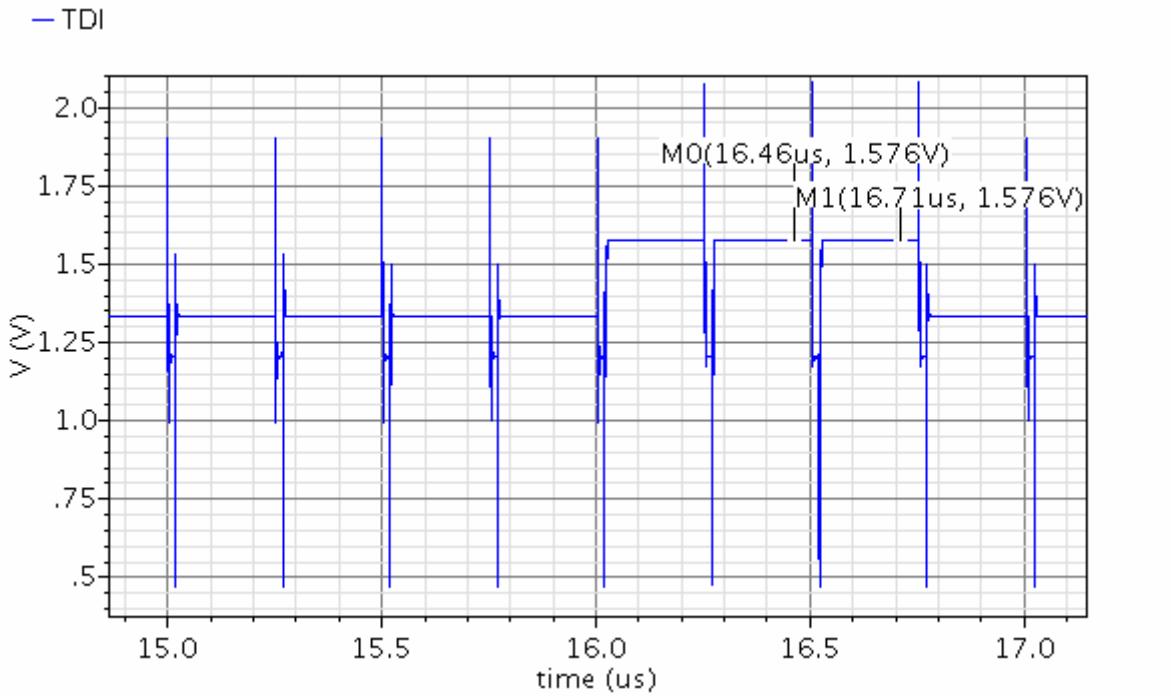

Figure 4.10: Schematic level simulation result at the TDI stage, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

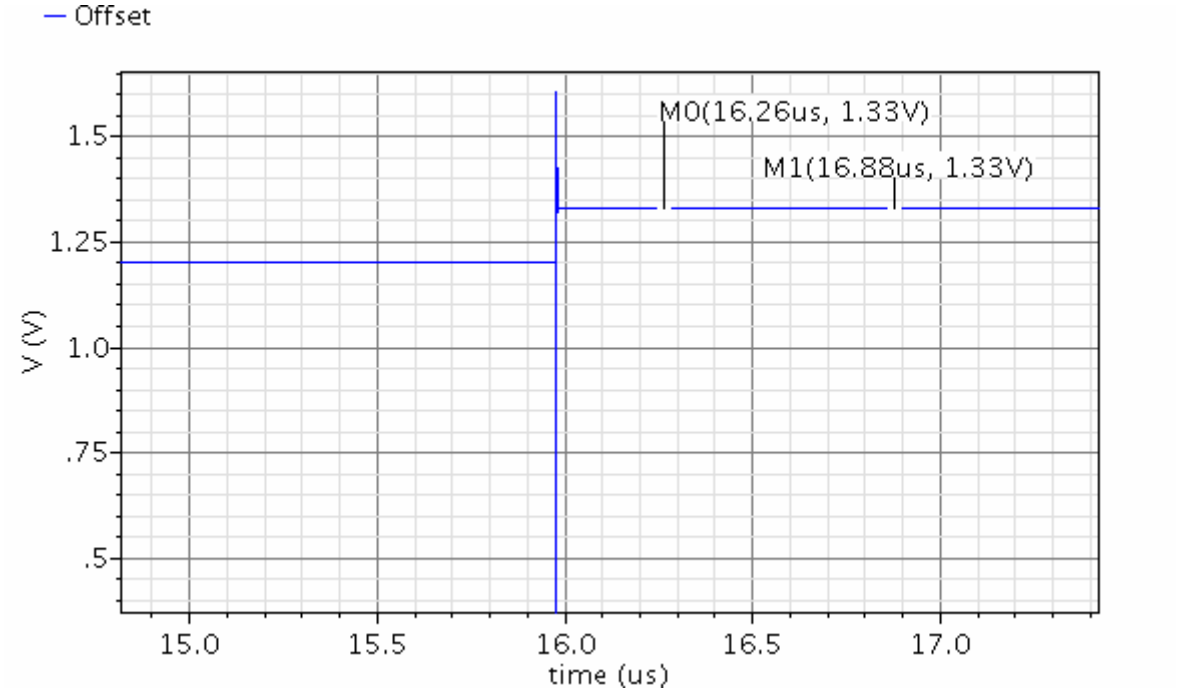

Figure 4.11: Schematic level simulation result at the offset stage, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

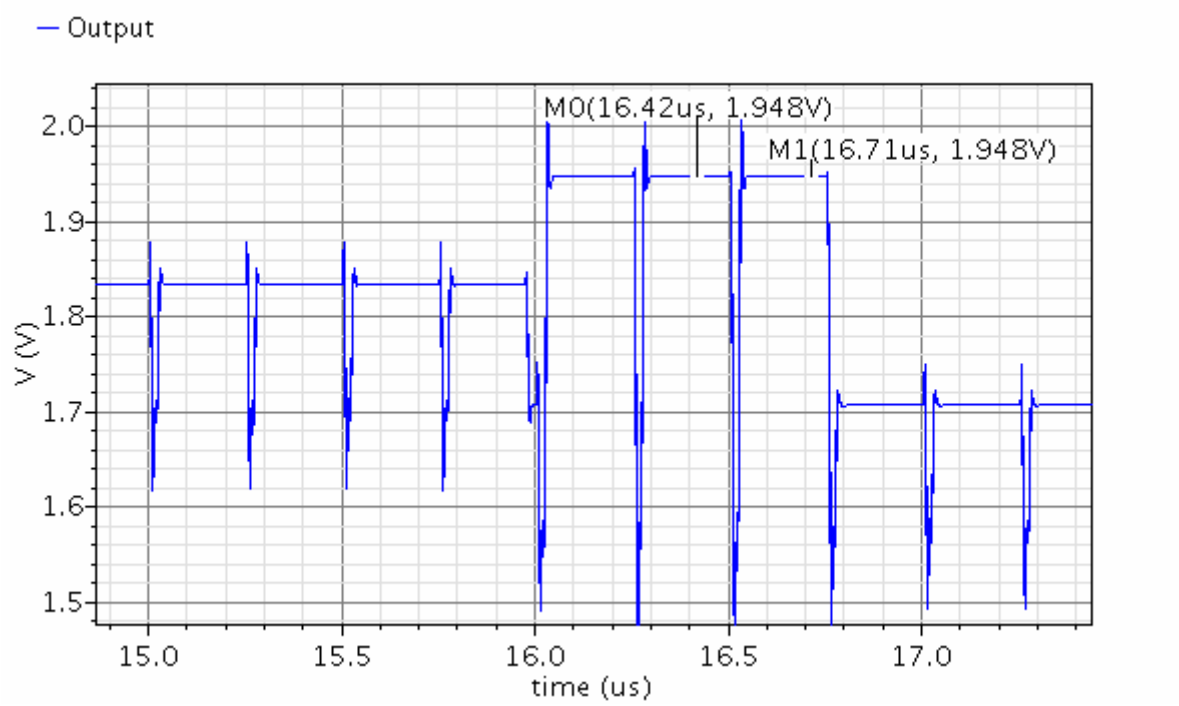

Figure 4.12: Schematic level simulation result at the output, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 243mV is integrated at the input. At TDI stage 376mV is added (errors exist), at the offset 130mV is observed. Hence at the output 248mV is added.

4.2.2 Extracted Results

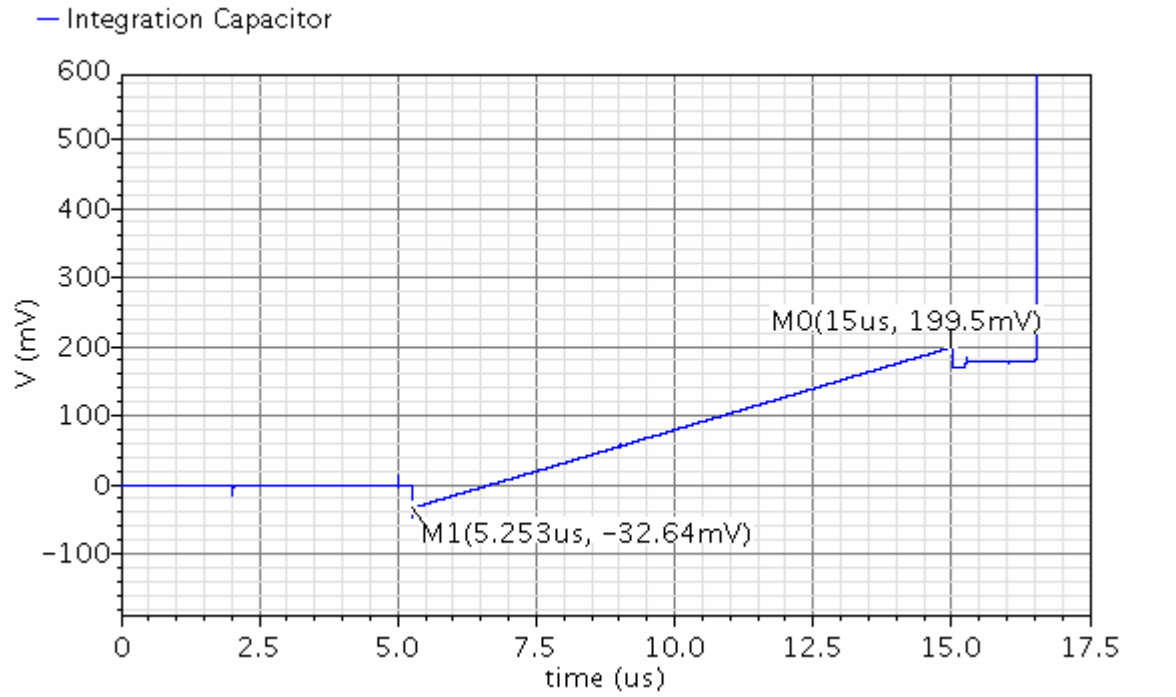

Figure 4.13: Extracted level simulation result at the input, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

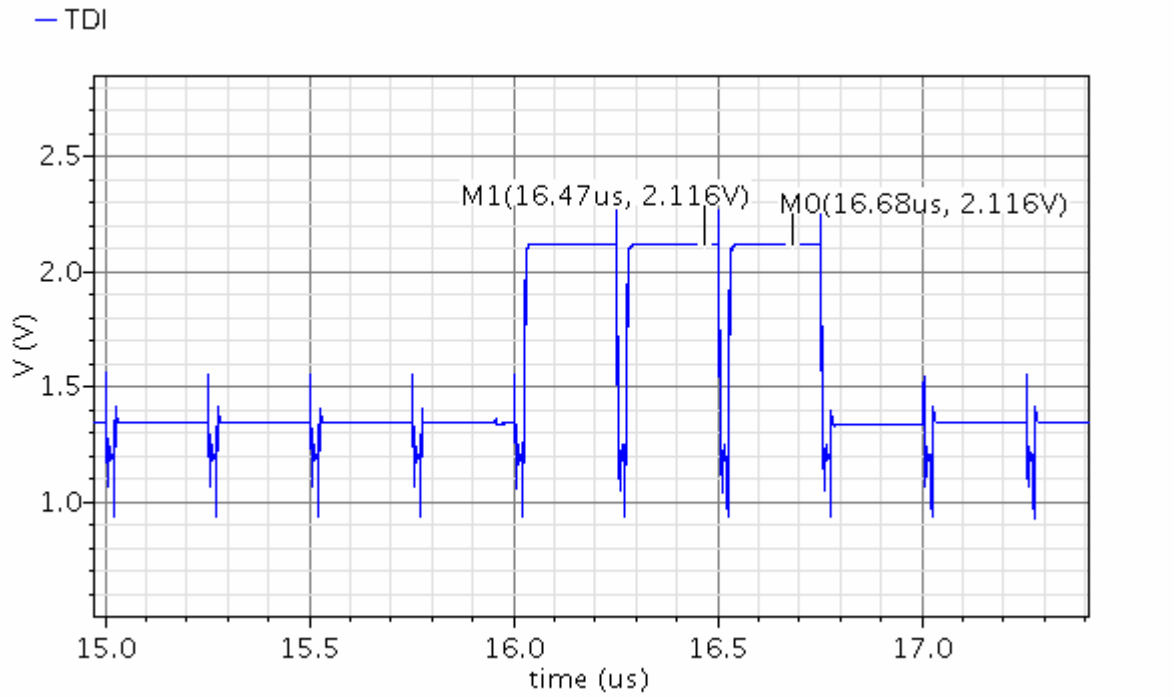

Figure 4.14: Extracted level simulation result at the TDI stage, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

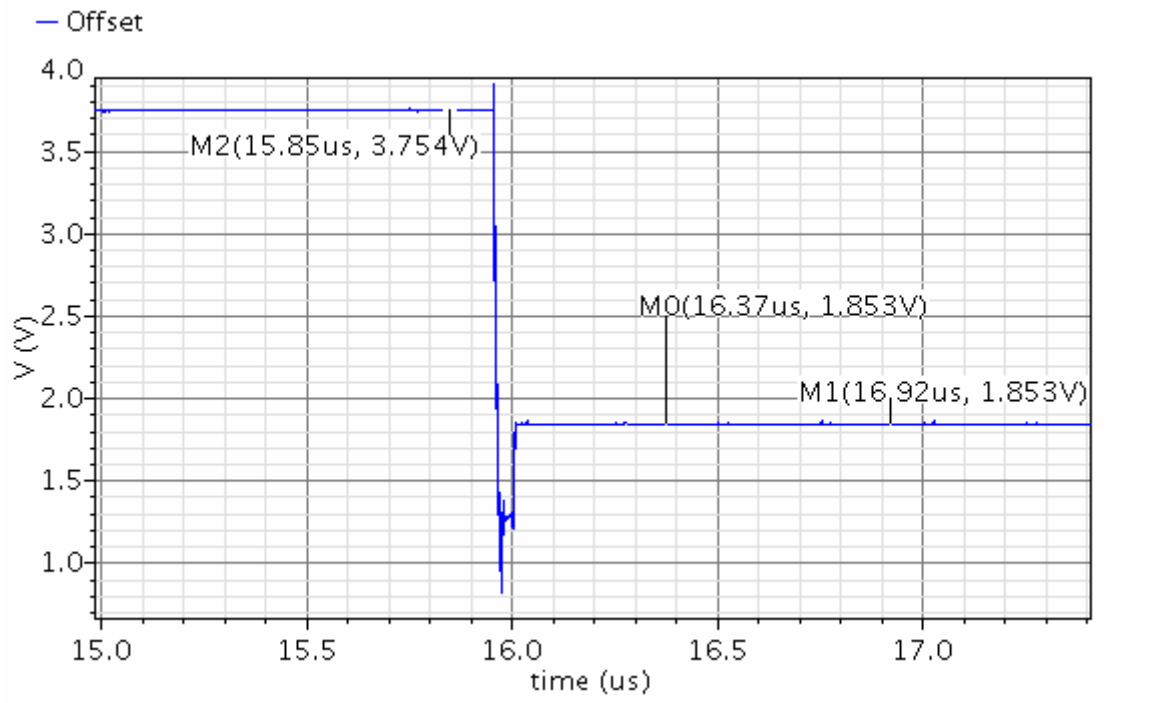

Figure 4.15: Extracted level simulation result at the offset stage, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

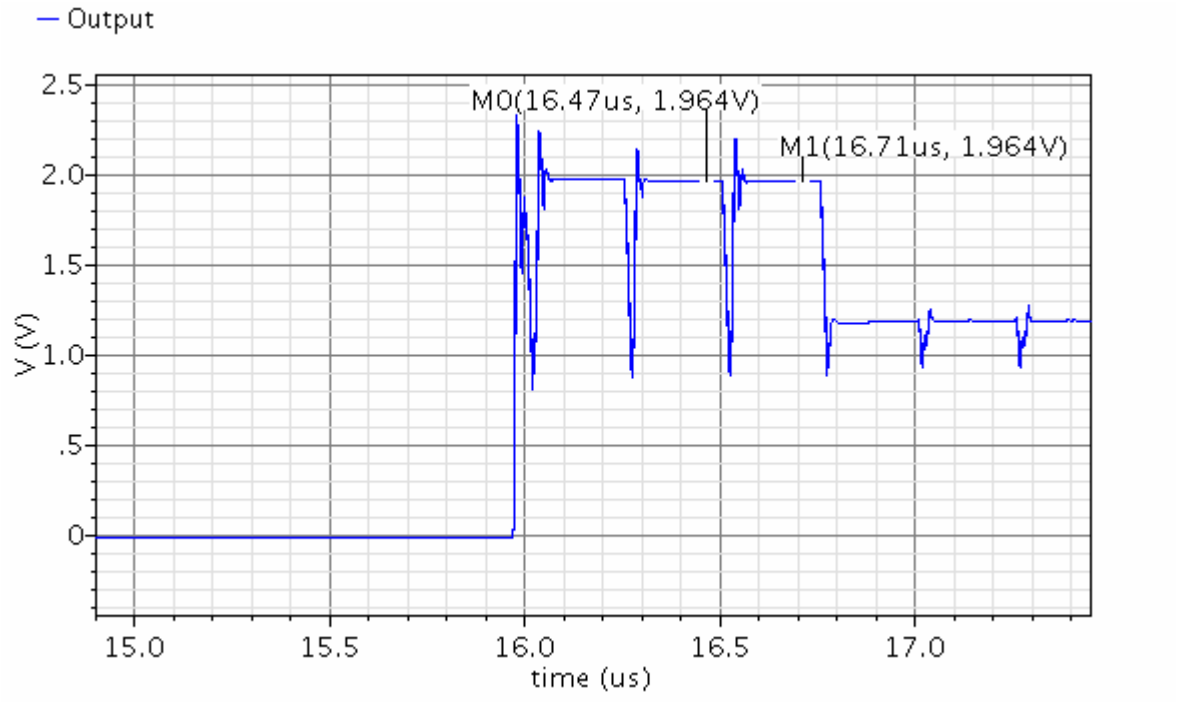

Figure 4.16: Extracted level simulation result at the output stage, for input current of 12.3nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 232mV is integrated at the input. At TDI stage 916mV is added (more errors exist), at the offset 653mV is observed. Hence at the output 264mV is added (There is constant offset of 42mV).

4.3 Simulation Results of 25nA Input Current

4.3.1 Schematics Results

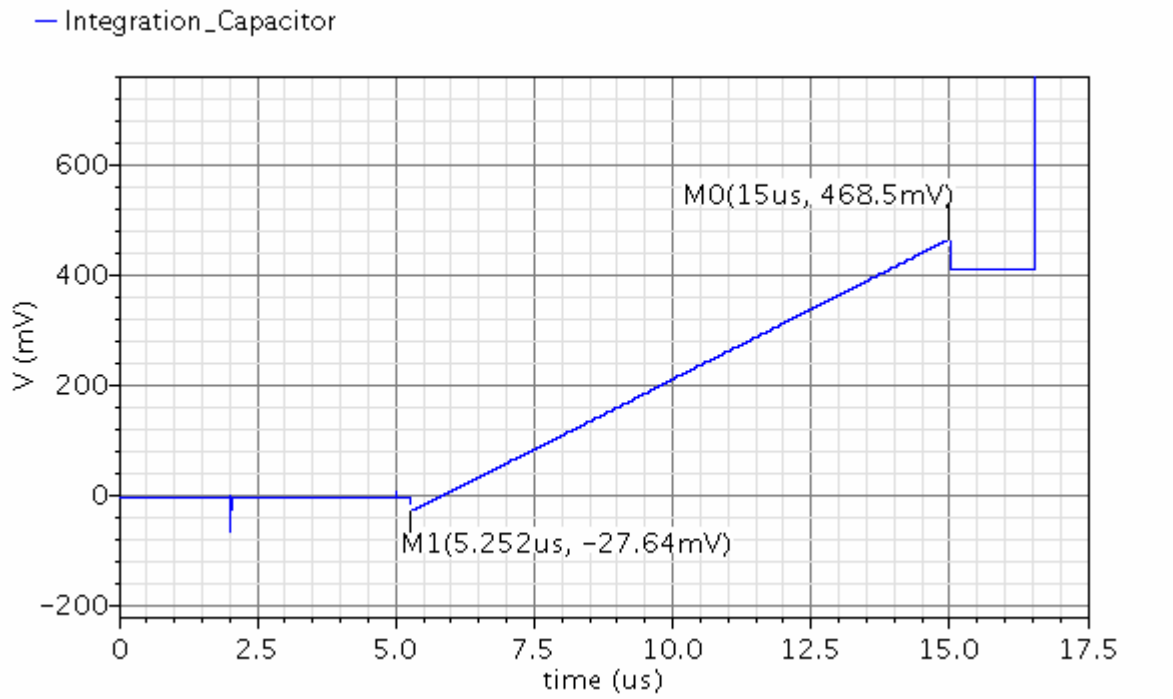

Figure 4.17: Schematic level simulation result at the input, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

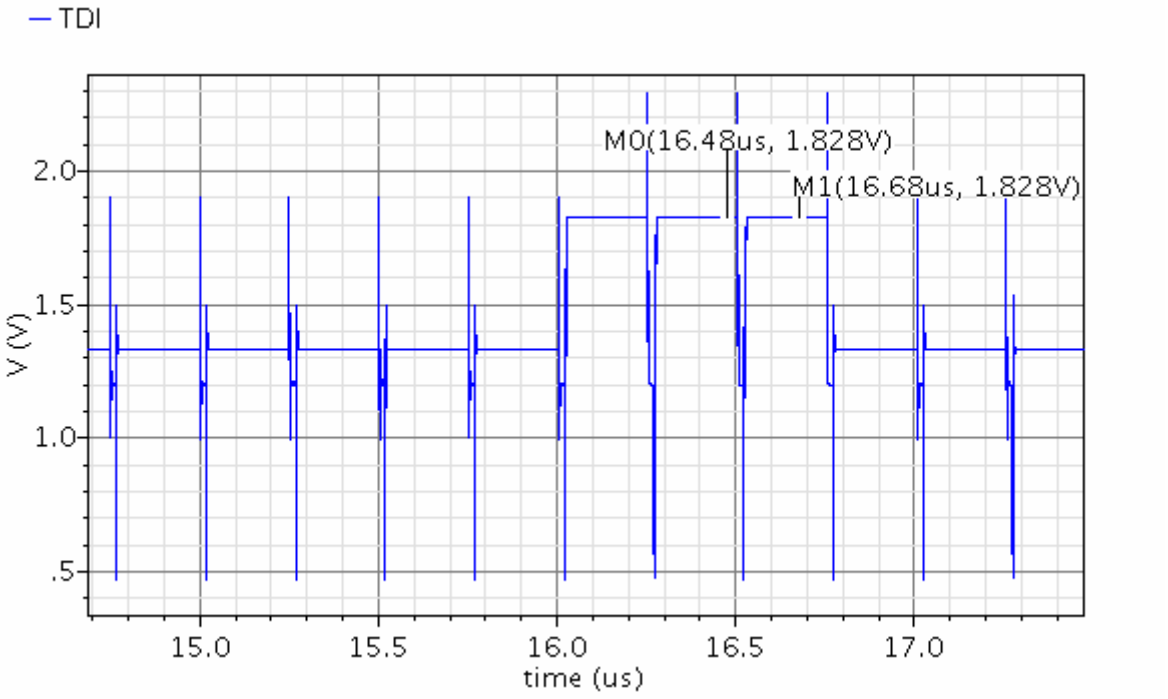

Figure 4.18: Schematic level simulation result at the TDI stage, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

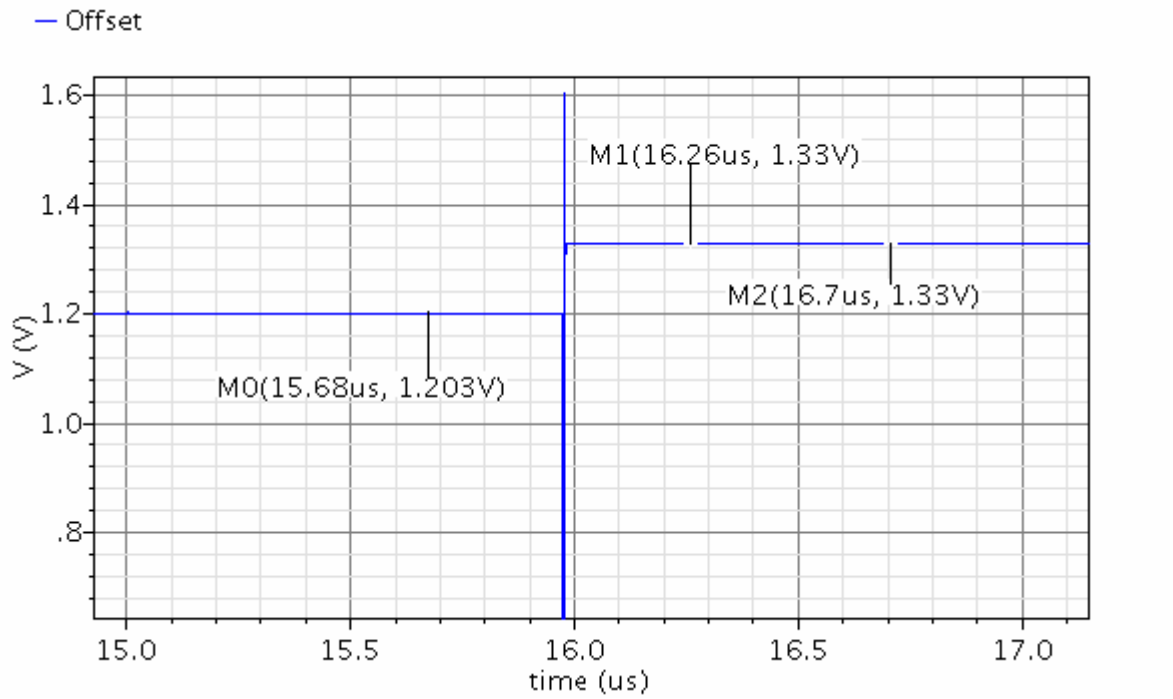

Figure 4.19: Schematic level simulation result at the offset stage, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

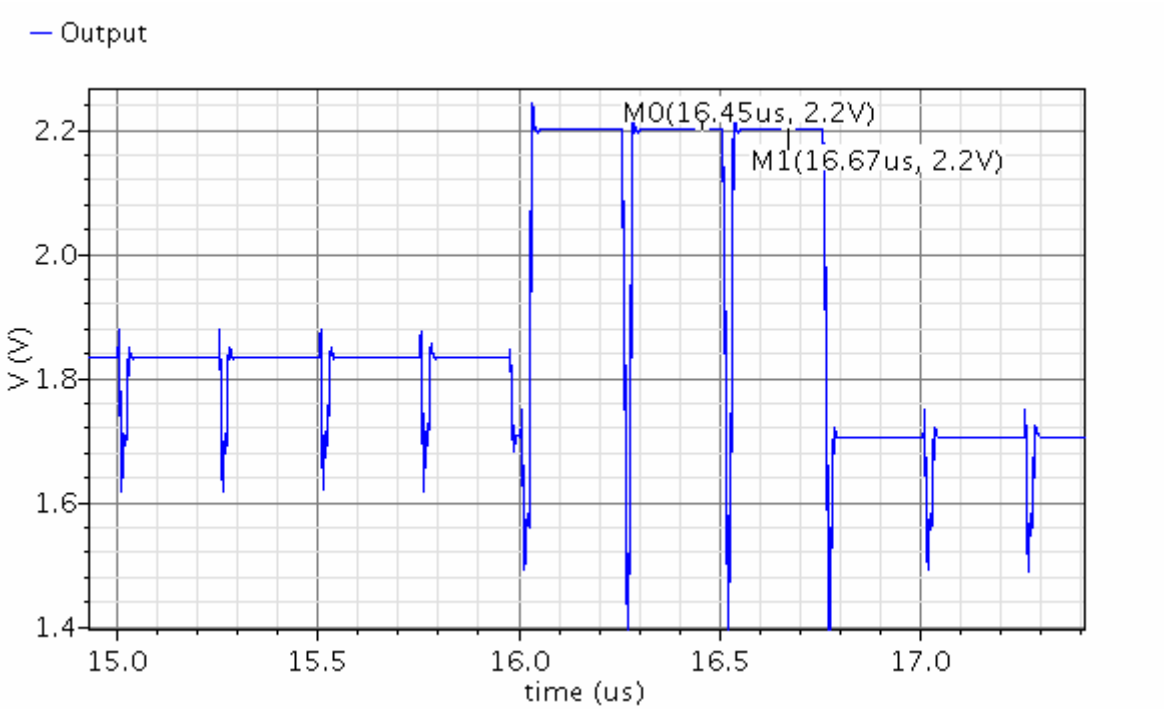

Figure 4.20: Schematic level simulation result at the output, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 496mV is integrated at the input. At TDI stage 628mV is added (errors exist), at the offset 130mV is observed. Hence at the output 500mV is added.

4.3.2 Extracted Results

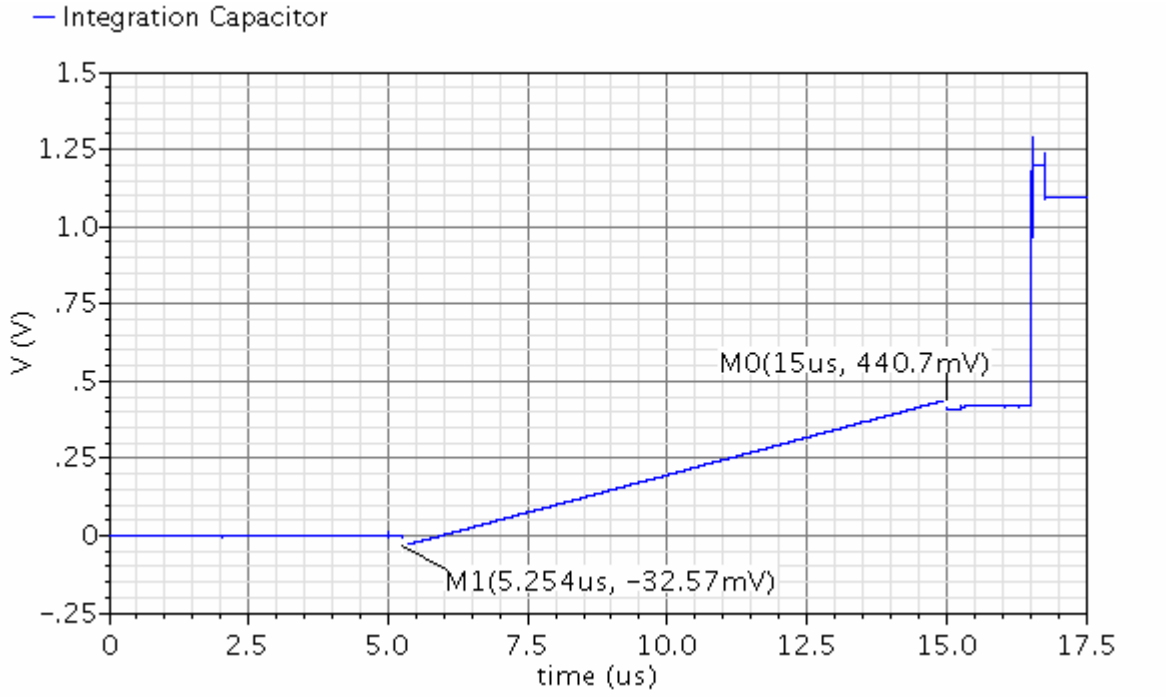

Figure 4.21: Extracted level simulation result at the input, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

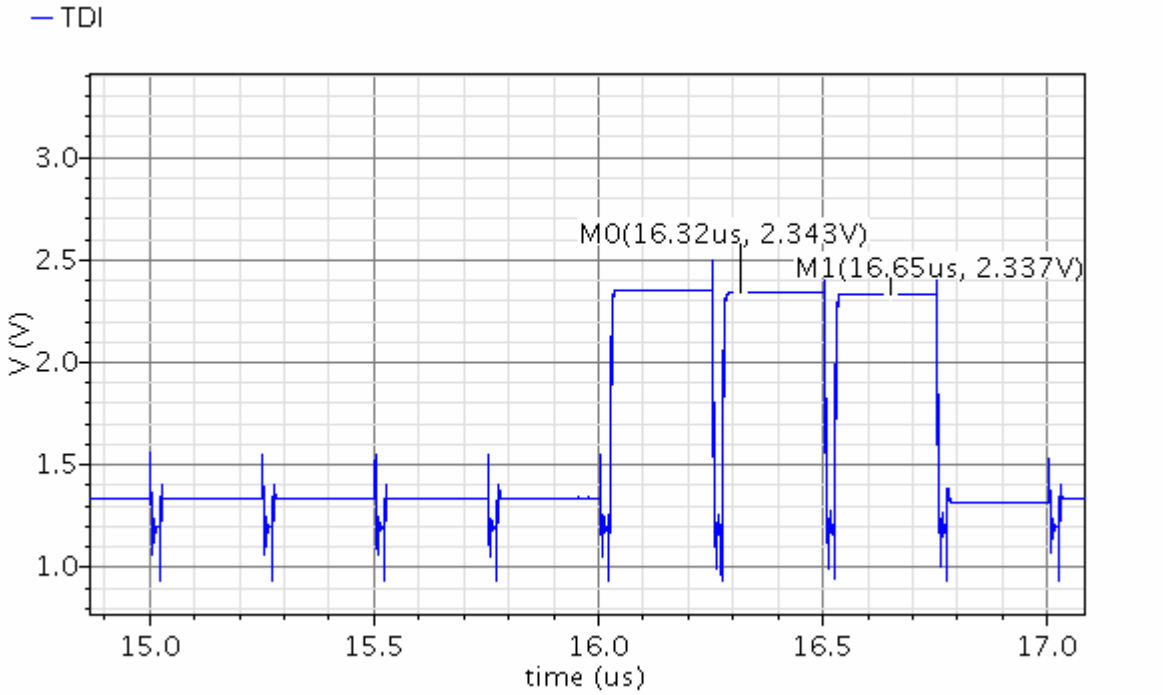

Figure 4.22: Extracted level simulation result at the TDI stage, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

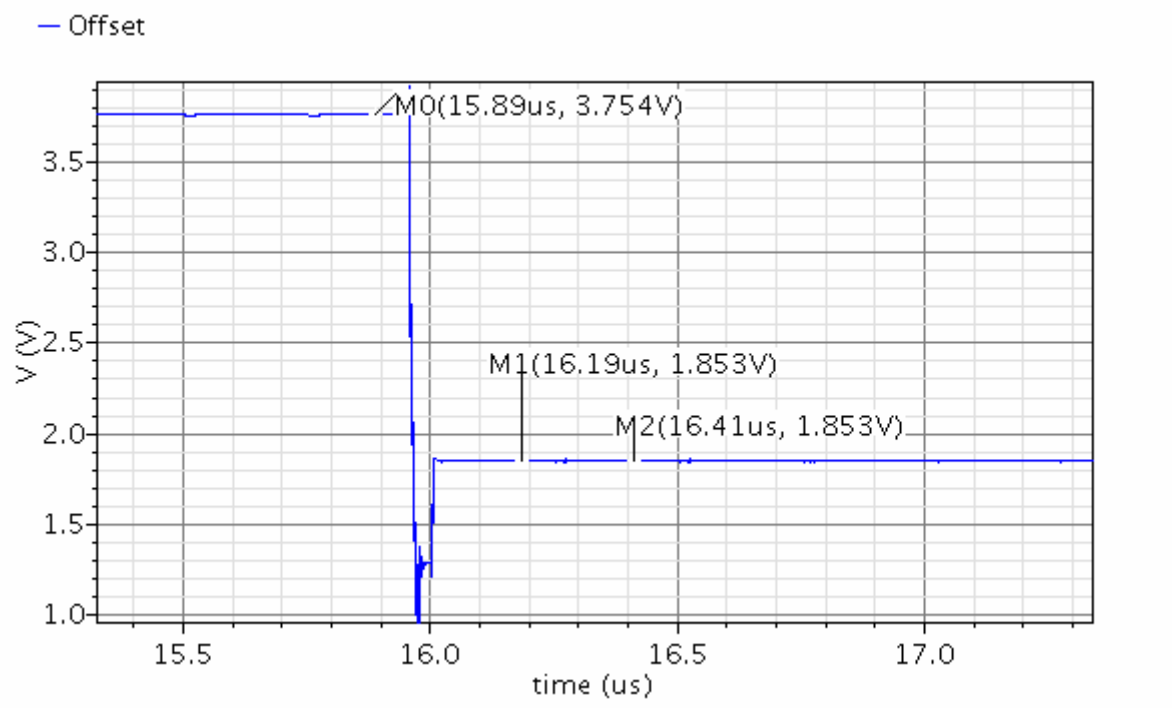

Figure 4.23: Extracted level simulation result at the offset stage, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

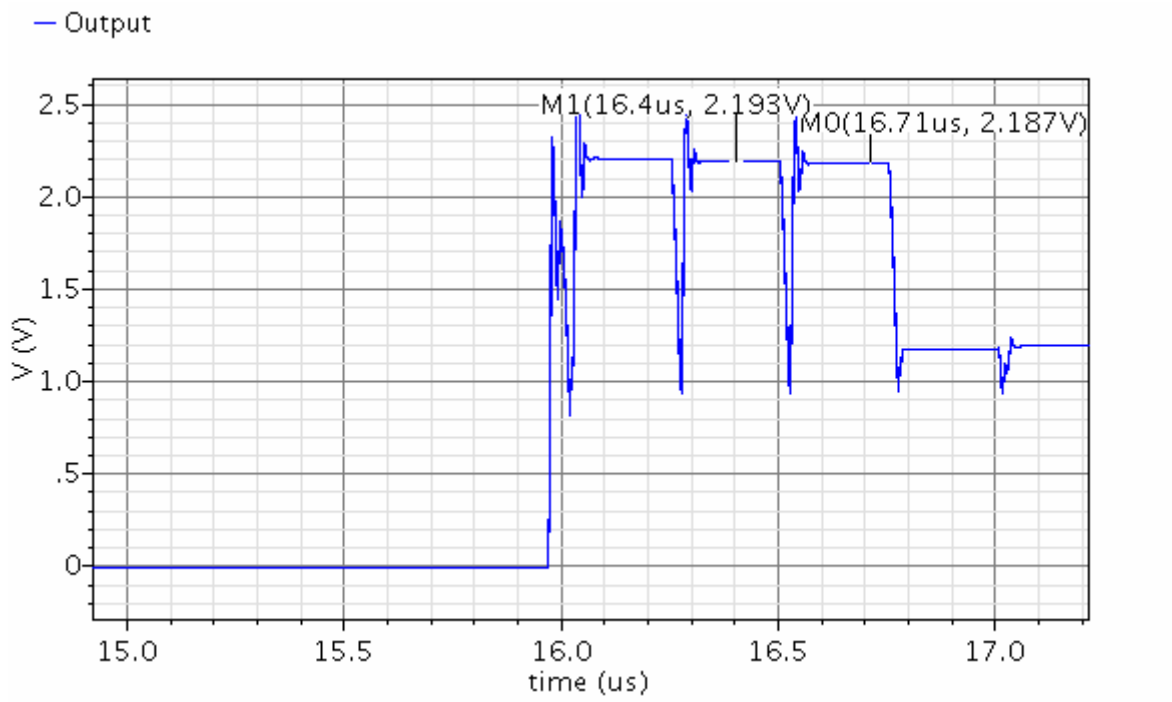

Figure 4.24: Extracted level simulation result at the output, for input current of 25nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 473mV is integrated at the input. At TDI stage 1143mV is added (more errors exist), at the offset 653mV is observed. Hence at the output 493mV is added (There is constant offset of 42mV).

4.4 Simulation Results of 55nA Input Current

4.4.1 Schematics Results

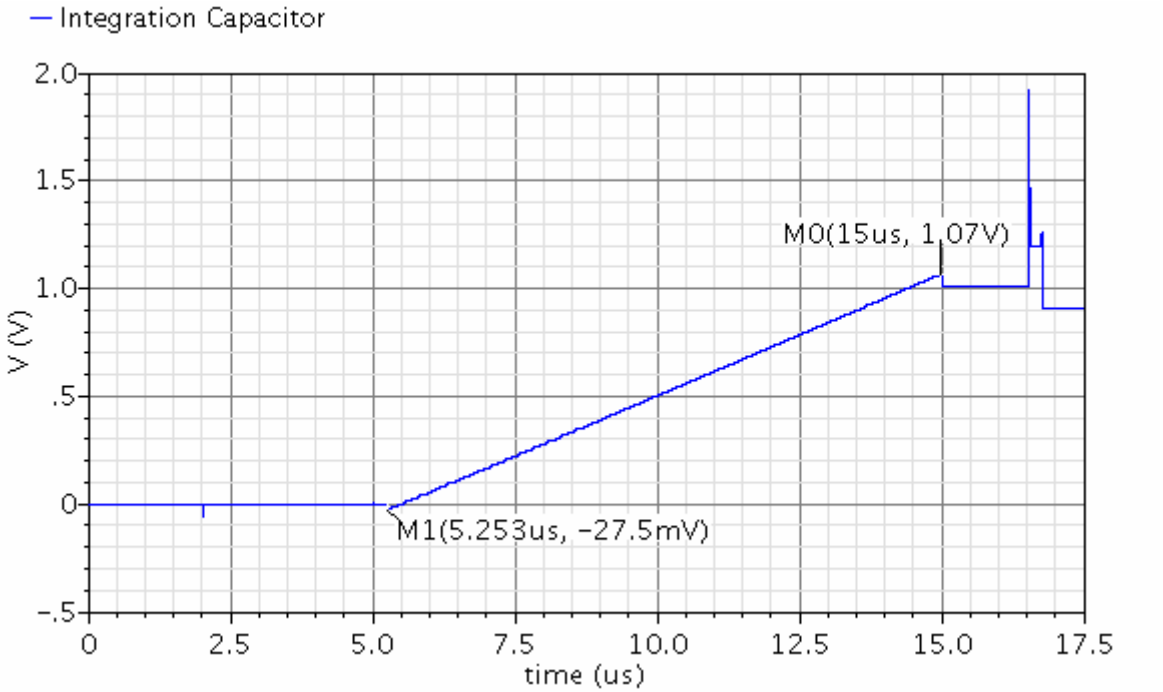

Figure 4.25: Schematic level simulation result at the input, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

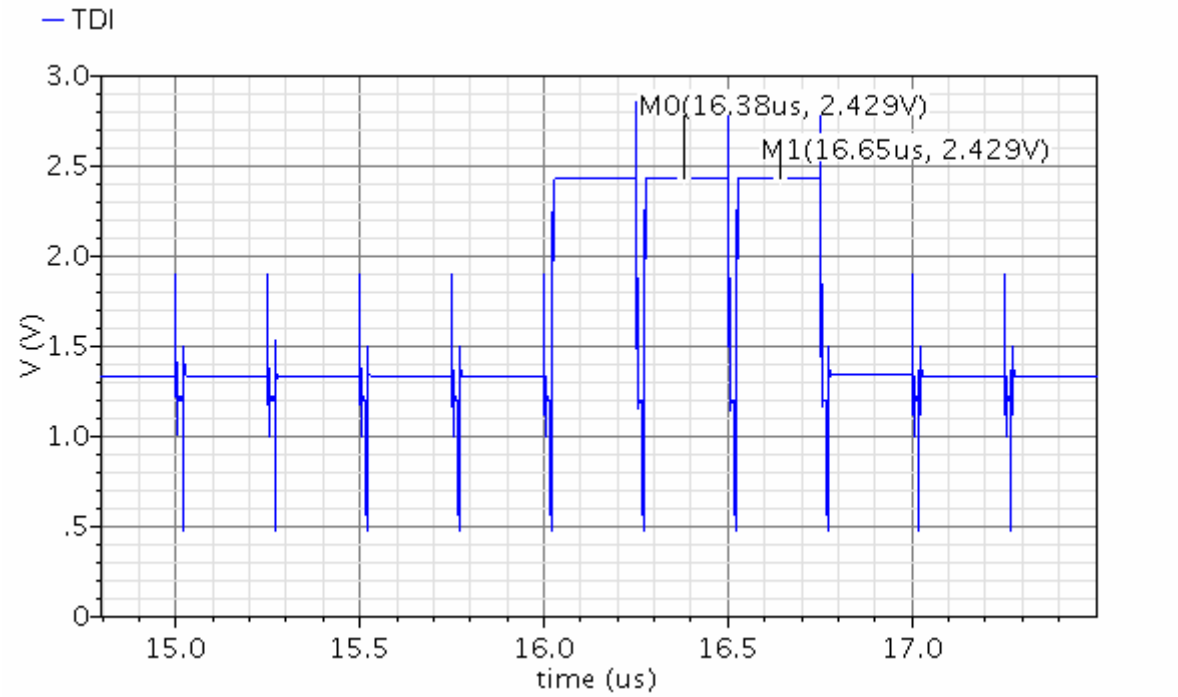

Figure 4.26: Schematic level simulation result at the TDI stage, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

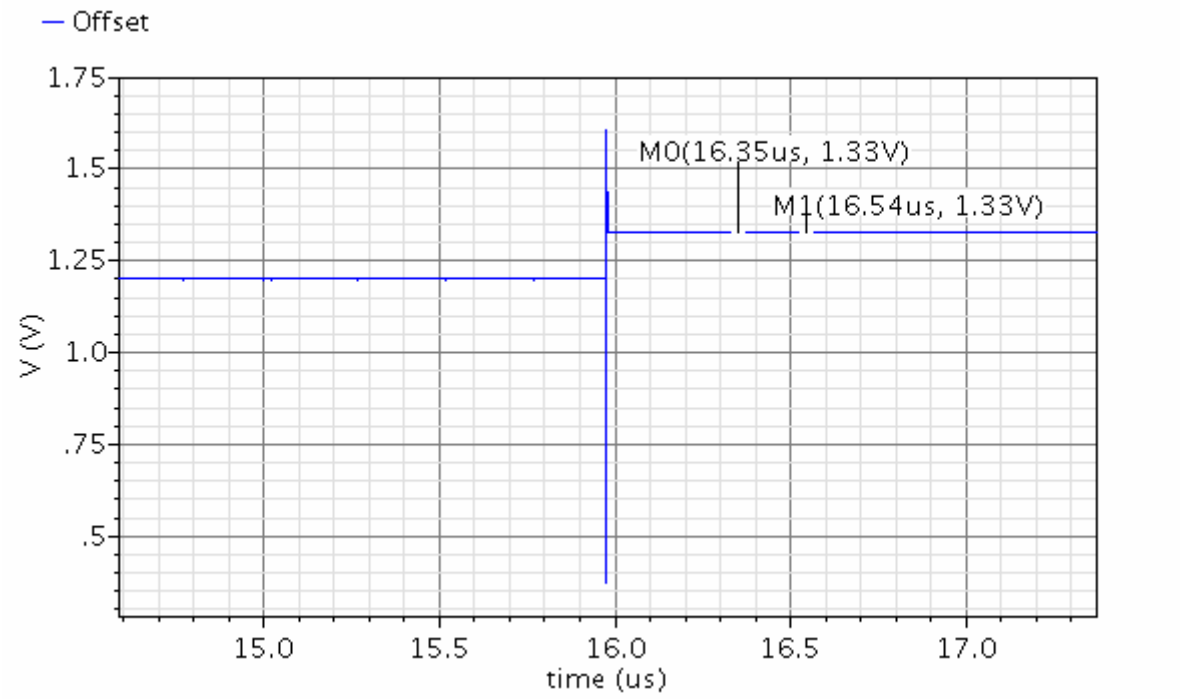

Figure 4.27: Schematic level simulation result at the offset stage, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

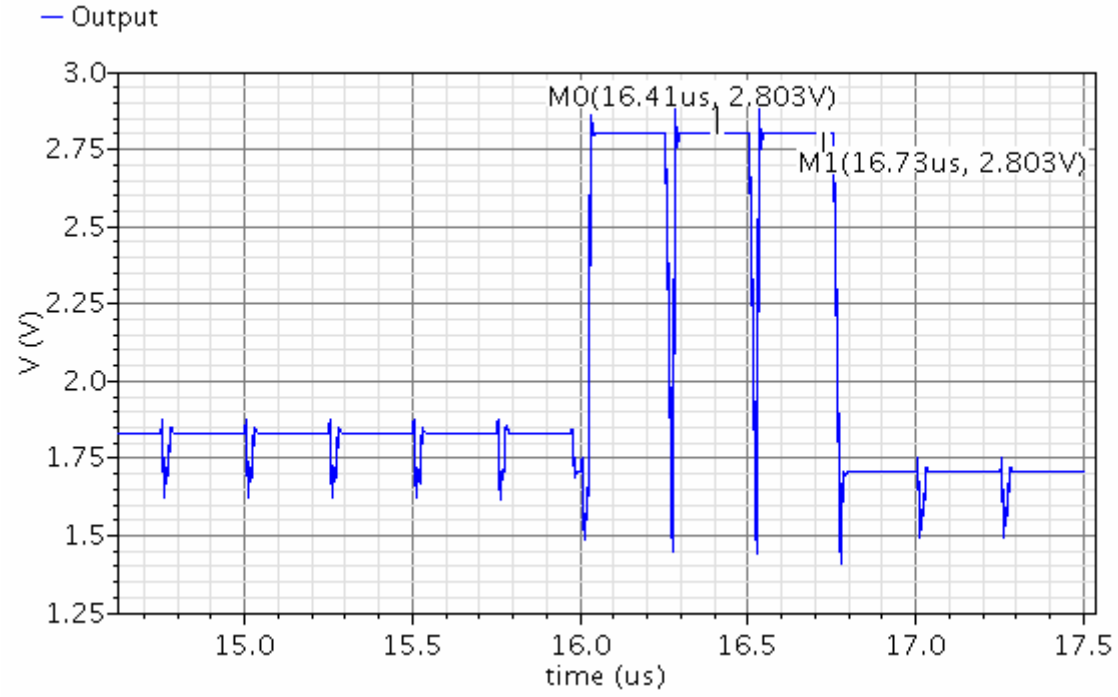

Figure 4.28: Schematic level simulation result at the output, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 1098mV is integrated at the input. At TDI stage 1229mV is added (errors exist), at the offset 130mV is observed. Hence at the output 1103mV is added.

4.4.2 Extracted Results

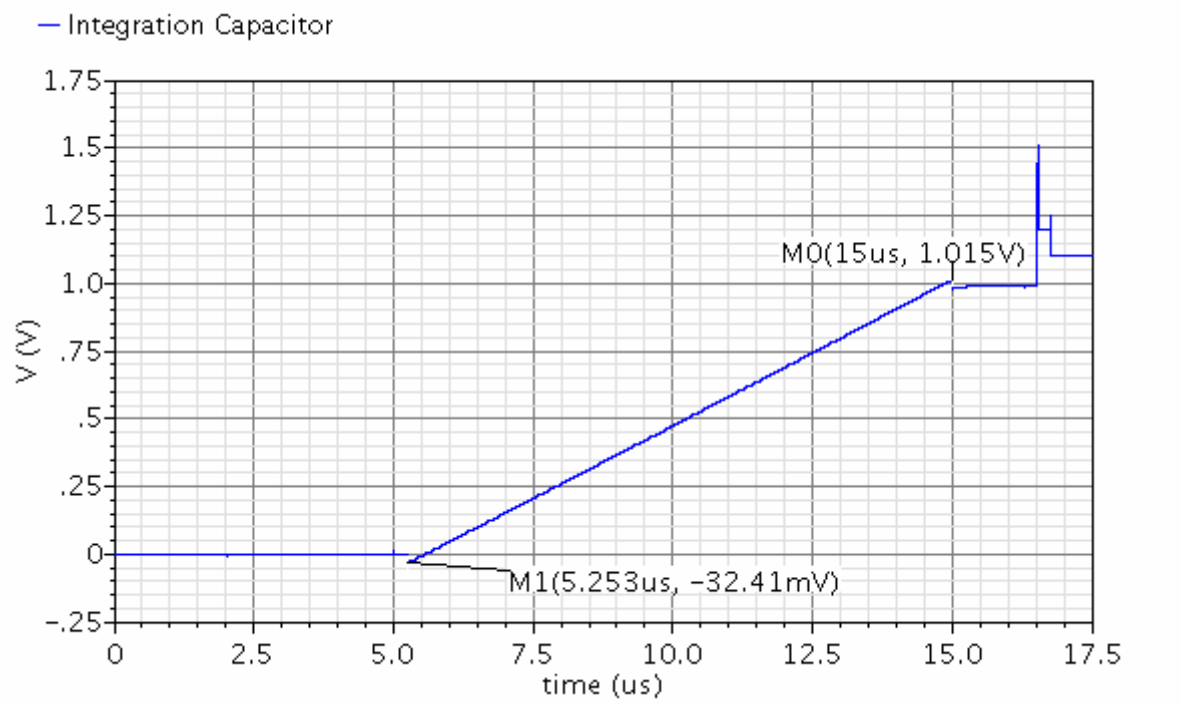

Figure 4.29: Extracted level simulation result at the input, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

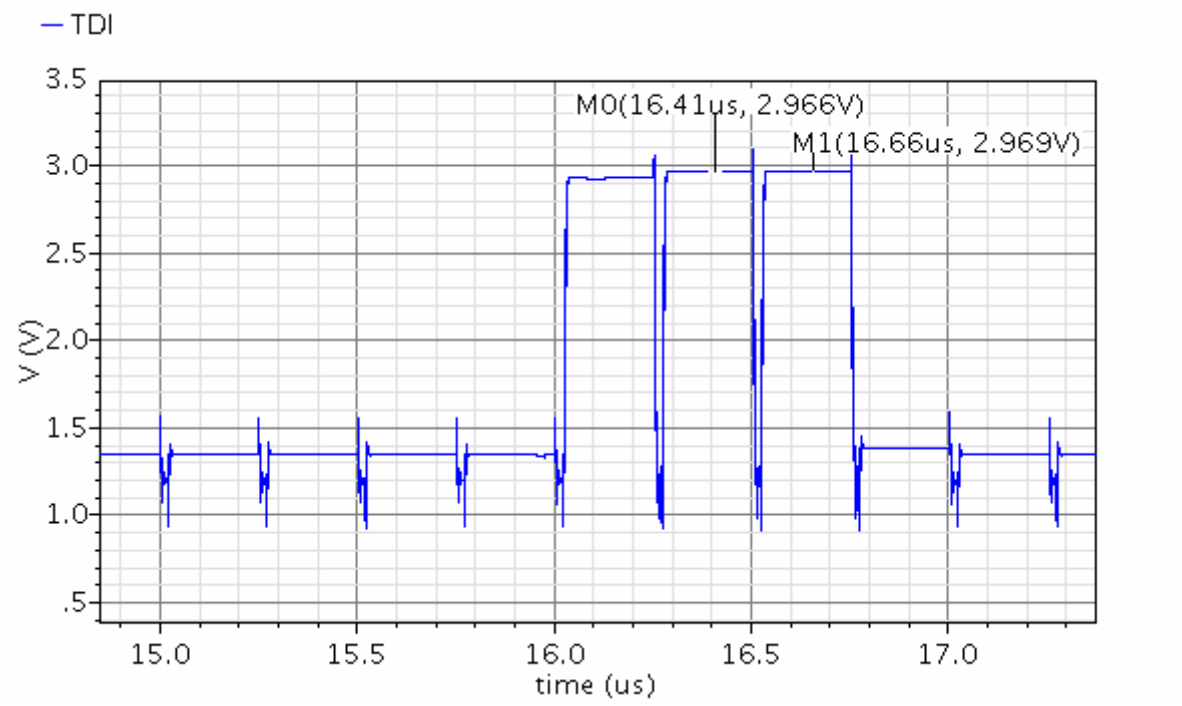

Figure 4.30: Extracted level simulation result at the TDI stage, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

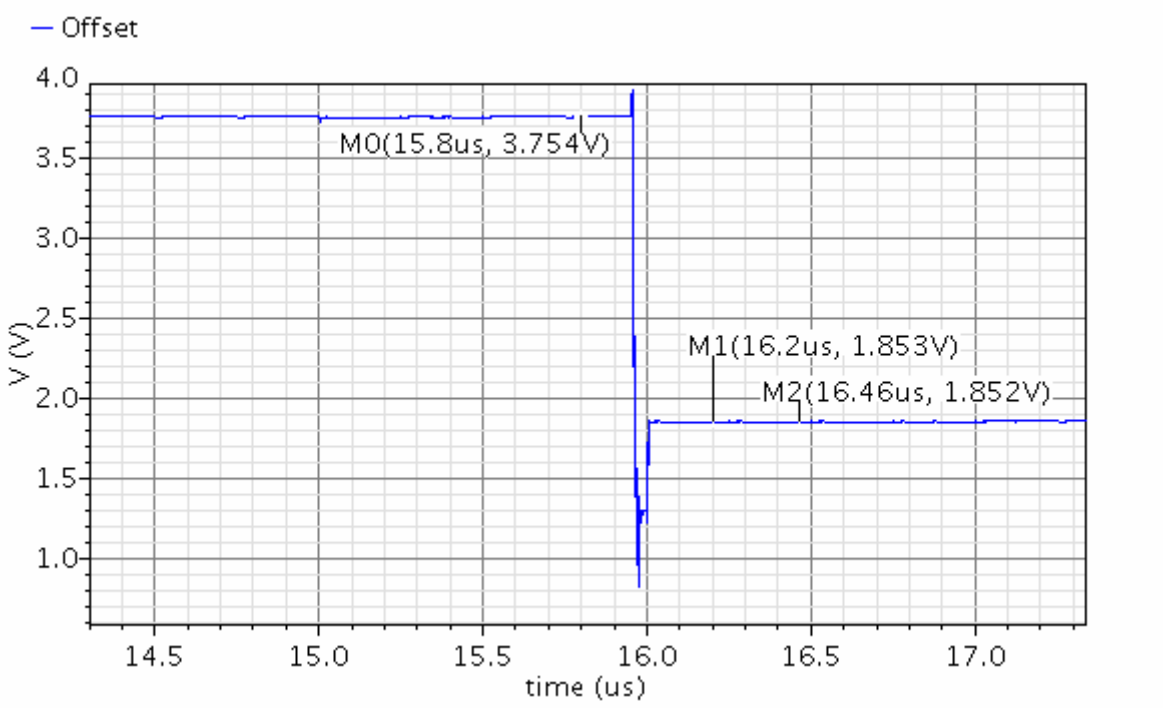

Figure 4.31: Extracted level simulation result at the offset stage, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

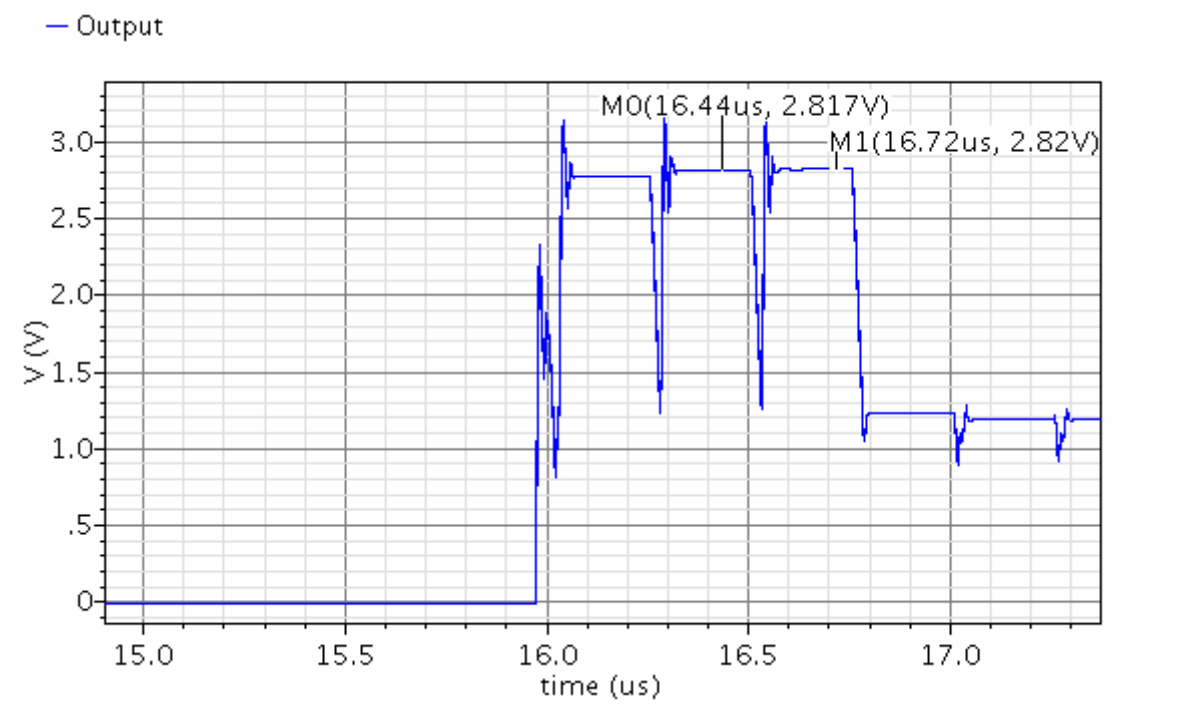

Figure 4.32: Extracted level simulation result at the output, for input current of 55nA, integration time 10µsec. and gain setting 1 (460fF)

Results show that 1047mV is integrated at the input. At TDI stage 1766mV is added (more errors exist), at the offset 653mV is observed. Hence at the output 1117mV is added (There is constant offset of 42mV).

4.5 Simulation Results with G0.50 setting

4.5.1 Schematics Results

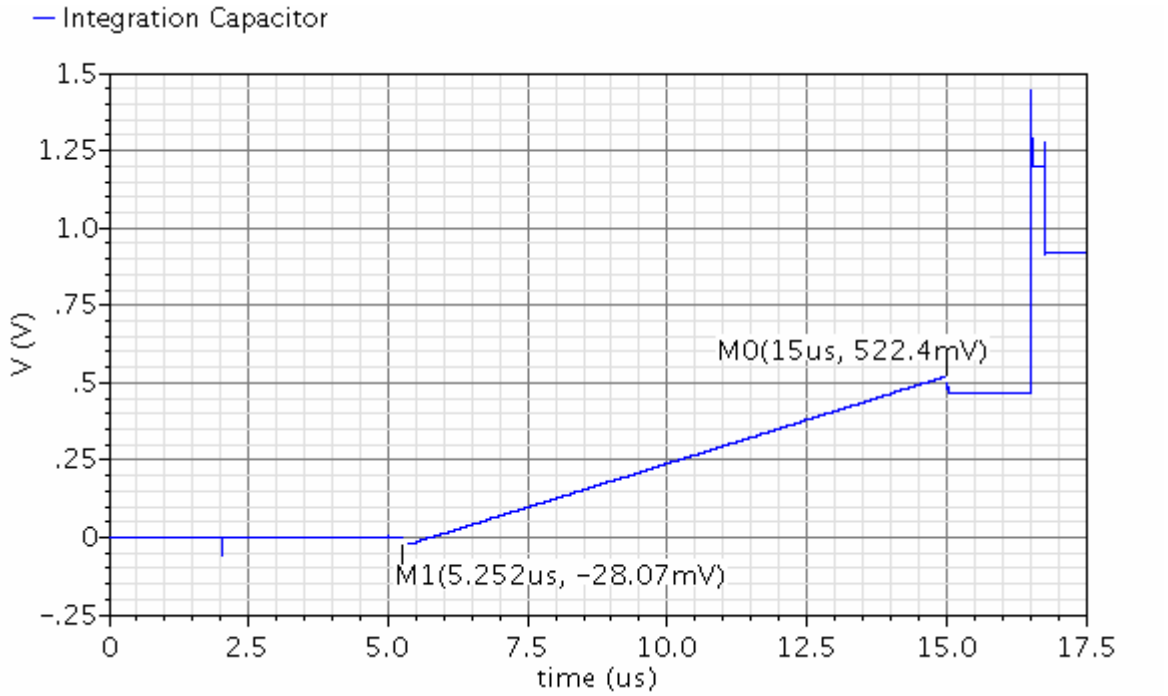

Figure 4.33: Schematic level simulation result at the input, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF)

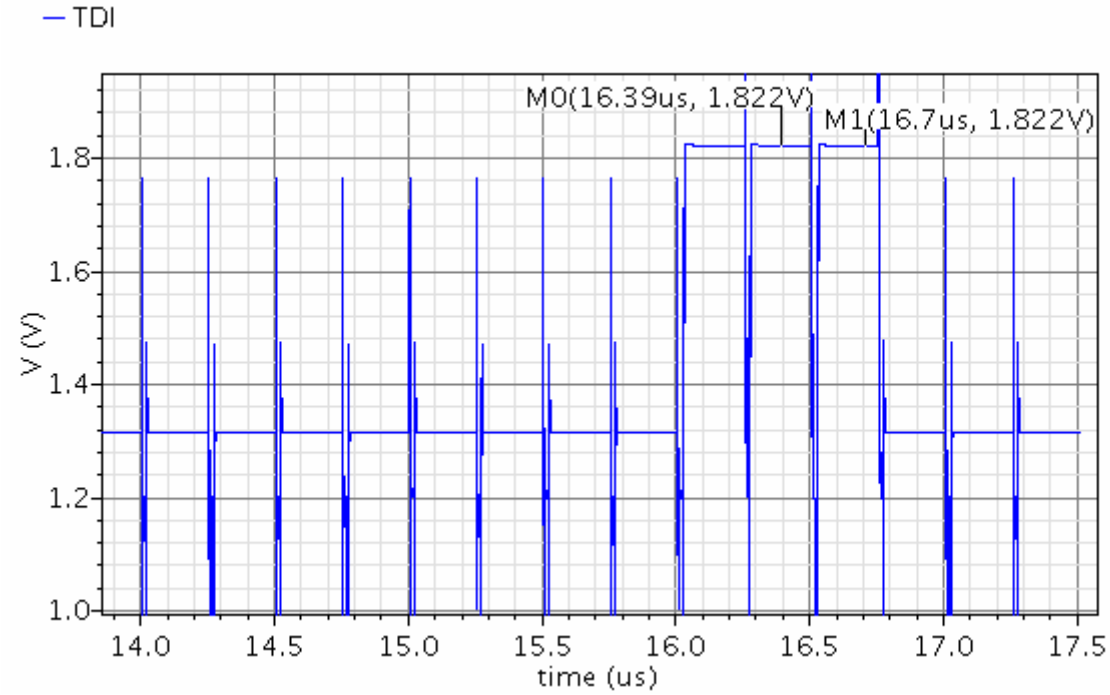

Figure 4.34: Schematic level simulation result at the TDI stage, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF)

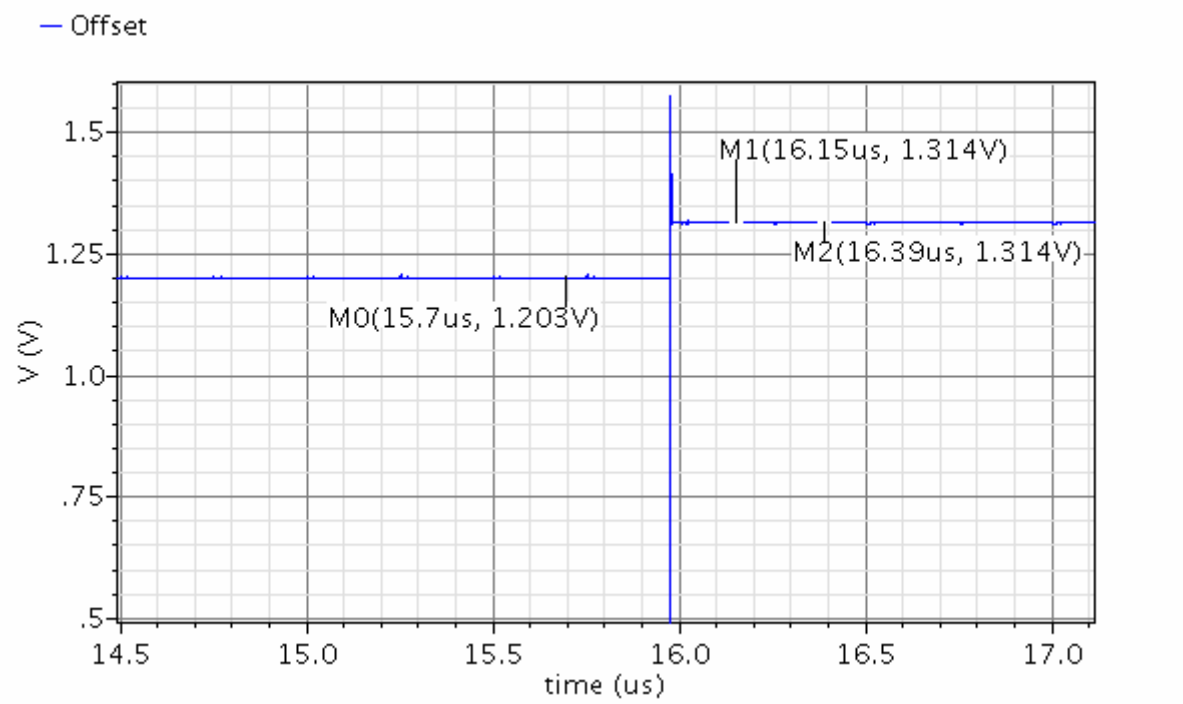

Figure 4.35: Schematic level simulation result at the offset stage, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF)

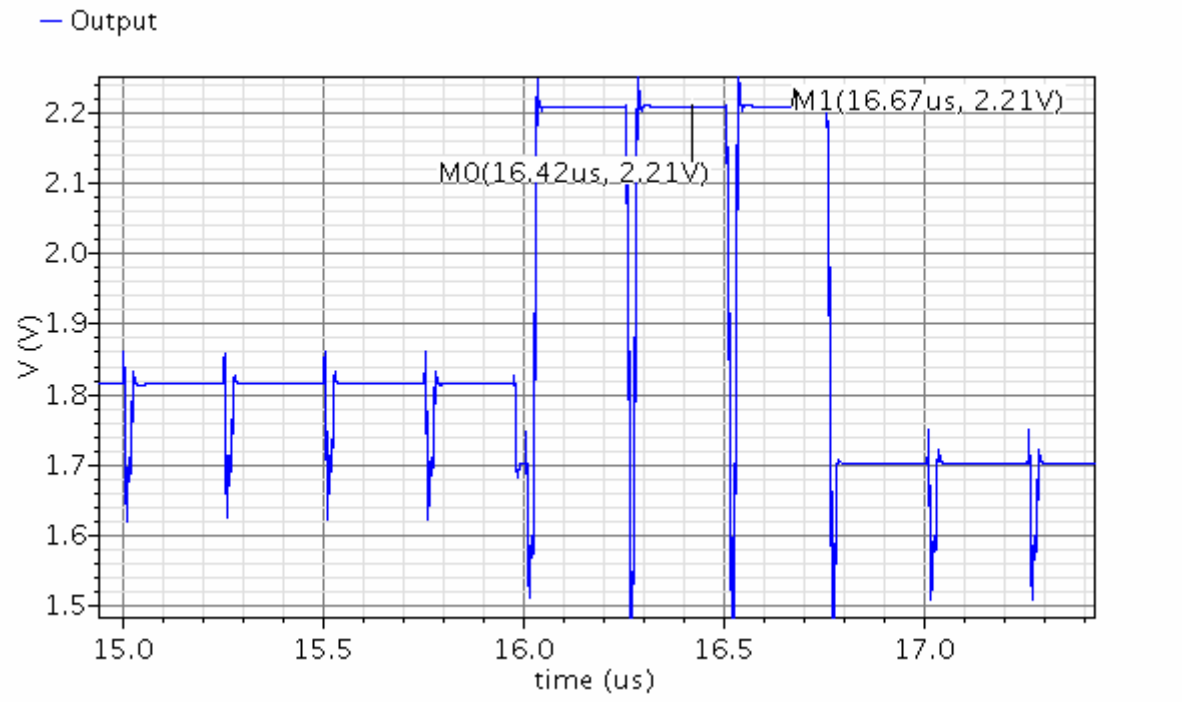

Figure 4.36: Schematic level simulation result at the output, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF)

Results show that 550mV is integrated at the input. At TDI stage 622mV is added (errors exist), at the offset 114mV is observed. Hence at the output 510mV is added.

4.5.2 Extracted Results

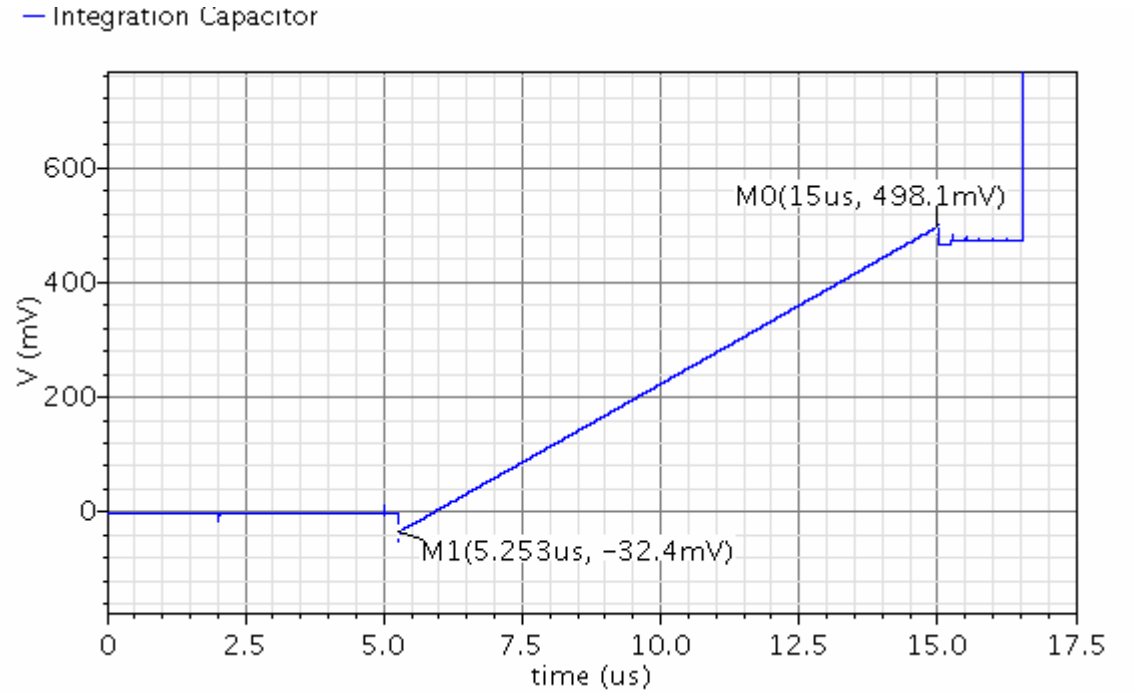

Figure 4.37: Extracted level simulation result at the input, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF).

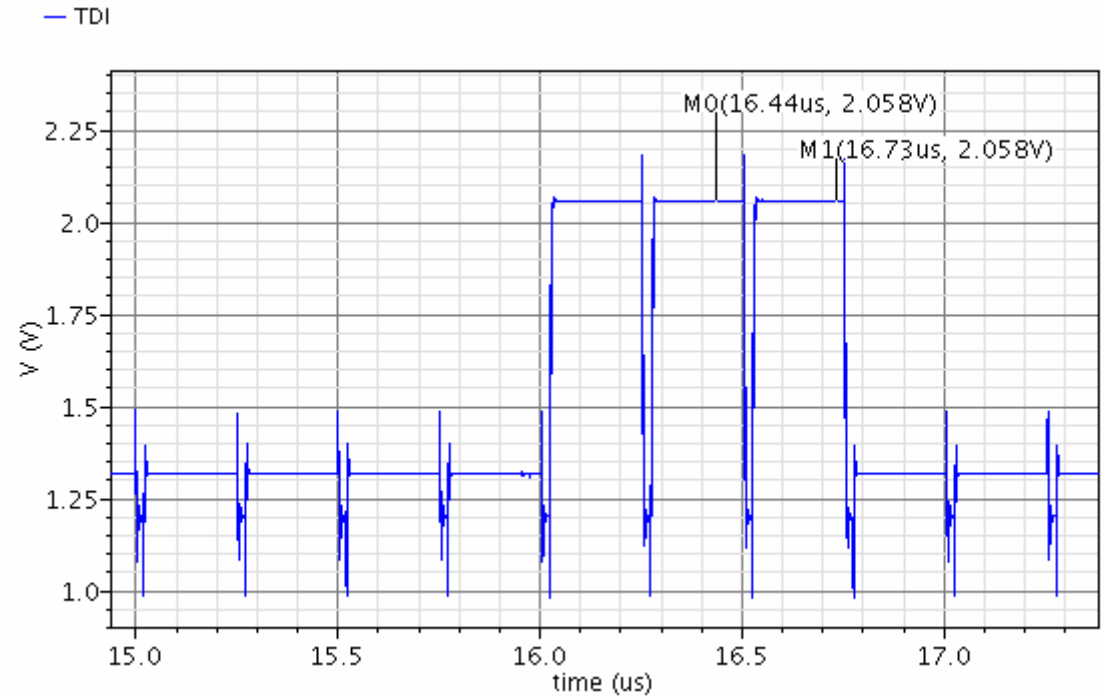

Figure 4.38: Extracted level simulation result at the TDI stage, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF).

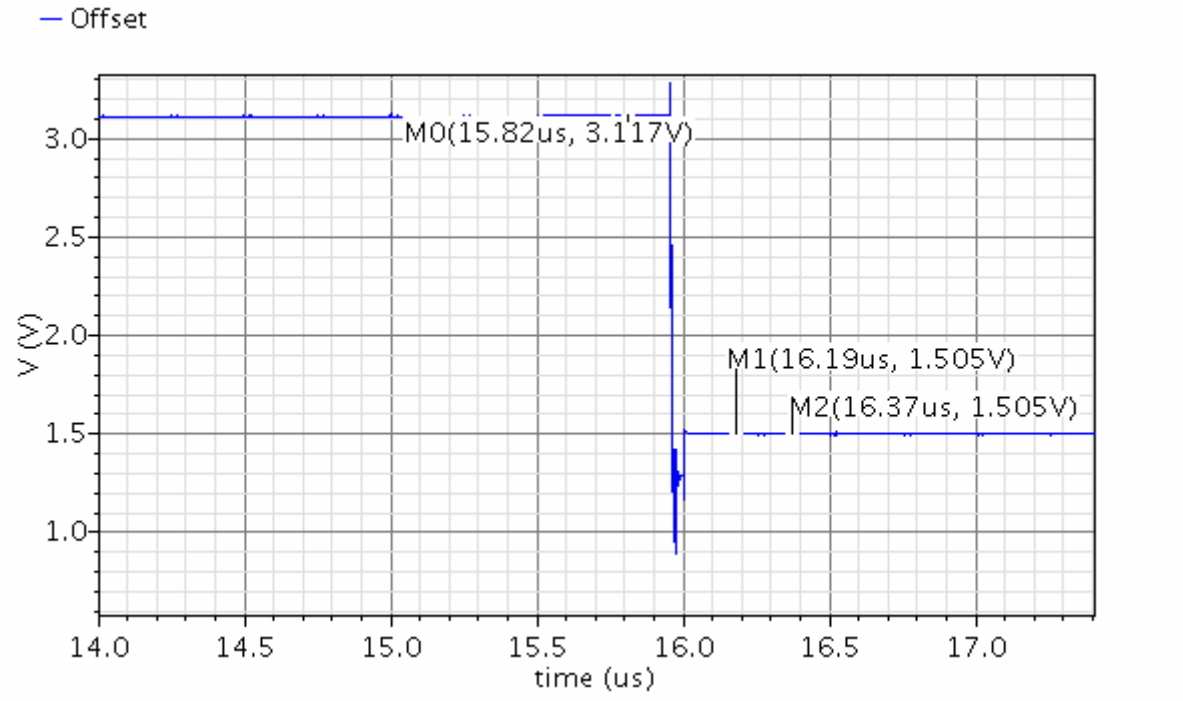

Figure 4.39: Extracted level simulation result at the offset stage, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF).

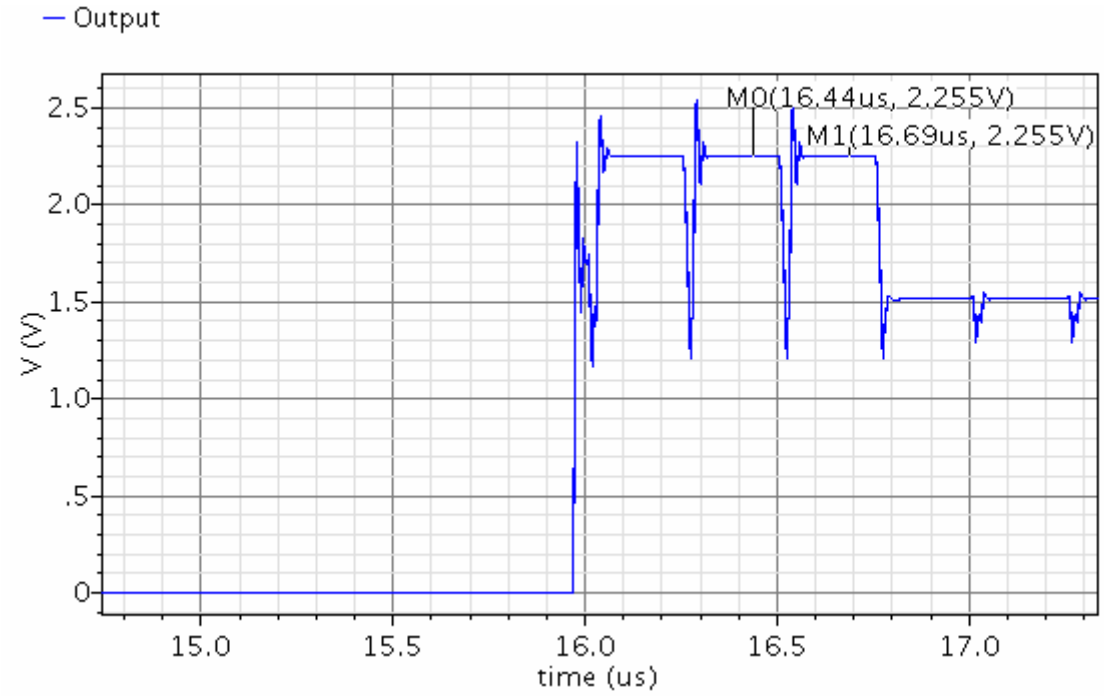

Figure 4.40: Extracted level simulation result at the output, for input current of 55nA, integration time 10µsec. and gain setting 0.50 (920fF).

Results show that 530mV is integrated at the input. At TDI stage 858mV is added (more errors exist), at the offset 305mV is observed. Hence at the output 555mV is added (There is constant offset of 42mV).

4.6 Comments on Simulation Results

It is observed from above graphs that extracted offset is always higher than the simulated schematic offset as expected. There is some amount of constant offset around 40mV remained at the output. This is due to the capacitive mismatch between the TDI stage input that creates the TDI effect and the TDI amplifier used at the differential block. Further layout optimization for this stage is possible. However, aside this offset and ±15 mV range nonlinearity, operation of ROIC is verified. If parasitics in both stages are to be matched, offset and nonlinearity can be decreased further. Extracted results shown in previous sections are represented in table.

	Integration Capacitor	**TDI**	**Offset**	**Output Simulated**	**Output Ideal**
1.2nA / G1	23mV	1916mV	1853mV	1765mV	1723mV
12.3nA / G1	233mV	2116mV	1853mV	1964mV	1933mV
25nA / G1	473mV	2343mV	1853mV	2193mV	2173mV
55nA / G1	1047mV	2966mV	1853mV	2820mV	2847mV
55nA / G0.50	530mV	2058mV	1505mV	2255mV	2230mV

Table 4.1 Simulation results of 288x4 ROIC

4.7 NOISE ANALYSIS

Noise analysis is realized by Cadence Spectre CAD tool with transient noise analysis on single channel. Transient noise analysis evaluates possible noise contributions of every circuit element. Multiple runs for an average output noise power is done in order to calculate the equivalent output referred rms noise voltage. First rms values of each noise from different

simulation results are obtained. Than rms values of each simulation are summed according to formulas below.

For a continuous function *f(t)*, rms value is obtained by,

$$f_{\text{rms}} = \sqrt{\frac{1}{T_2 - T_1}\int_{T_1}^{T_2} [f(t)]^2\, dt} \tag{4.1}$$

Rms values of each noise run are evaluated first and than the rms values of N collection of data are obtained by:

$$x_{\text{rms}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \cdots + x_N^2}{N}} \tag{4.2}$$

Rms value of noise is obtained from the formulas are put in equation in order to convert to charge domain hence represent the noise as number of electrons.

$$Q = CxV \tag{4.3}$$

Number of electrons is found by Q / q where q is the charge of an electron.

A simulation with three iterations and gain setting 1 (460fF integration capacitor) is held. Using above equations noise at the output of each stage is obtained. At the input capacitor Input referred noise is found to be 286 μV corresponding to 821 electrons. Input referred noise is found to be 449 μV at TDI stage which corresponds to 1289 electrons. Following the offset cancellation stage, input referred noise is 1034 μV corresponding to 2969 electrons. Finally at the output of the buffer input referred noise is 1037 μV which corresponds to 2989 electrons. As expected preamplifier and the offset cancellation circuit are two major noise contributors.

4.8 MEASUREMENT RESULTS of 1x4 ROIC

First design submission for this project was done in June 2006. With AMS C35B4C3 process (2 poly, 3 metal layers), a single channel with similar architecture was submitted for manufacturing. The single channel design was not fully functional; it could only be programmed for variable gain settings and integration times. However it was quite successful in terms of the results it gave for verification of the designed sub blocks of the system. In this section some results of the 1x4 ROIC (single channel) is represented and more results are given in tabular form.

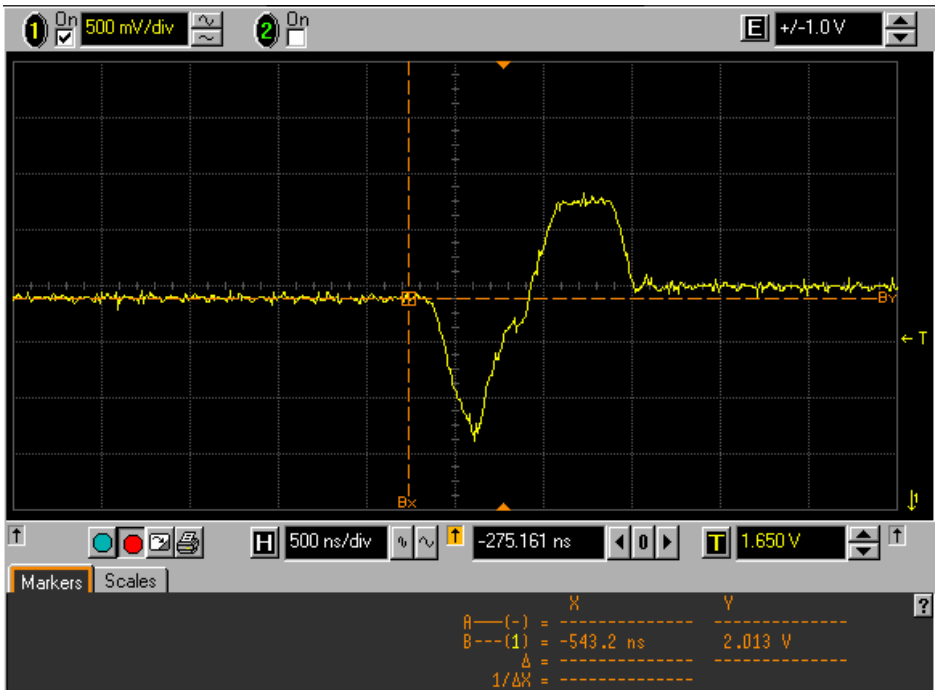

Figure 4.41: Measurement of 1x4 ROIC with input current 1nA, integration time 32 us, gain setting 1, output voltage is 2013mV, 313mV added to output

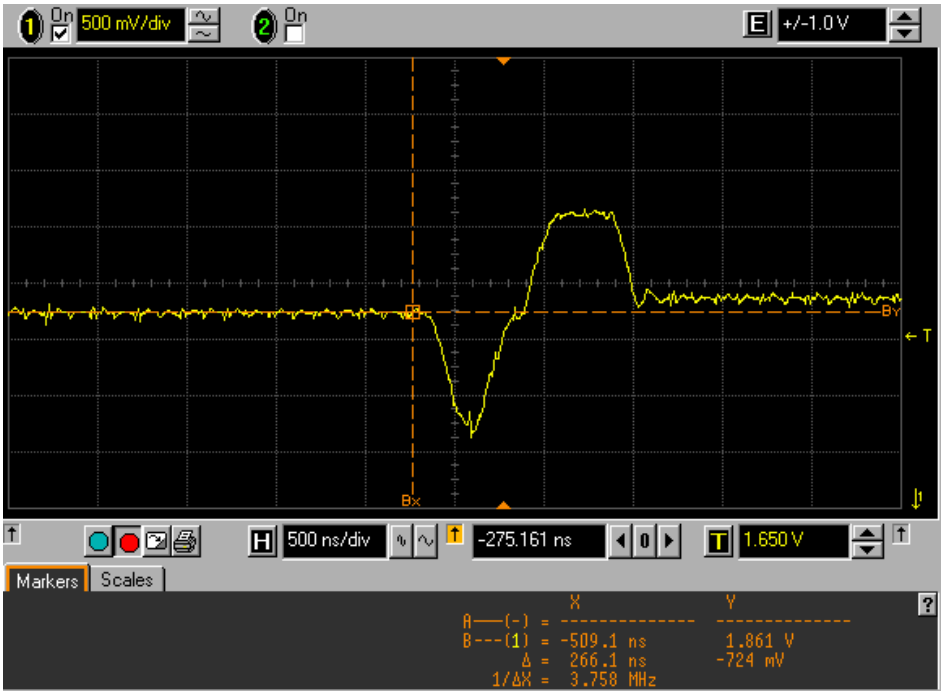

Figure 4.42: Measurement of 1x4 ROIC with input current 1nA, integration time 16 us, gain setting 1, output voltage is 1861mV, 161mV added to output

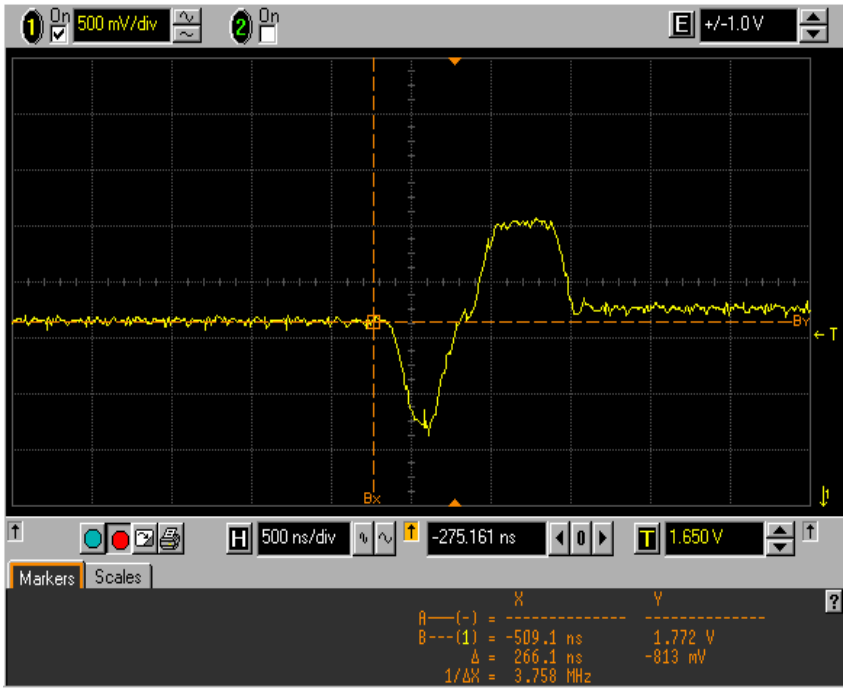

Figure 4.43: Measurement of 1x4 ROIC with input current 1nA, integration time 8 us, gain setting 1, output voltage is 1772mV, 72mV added to output

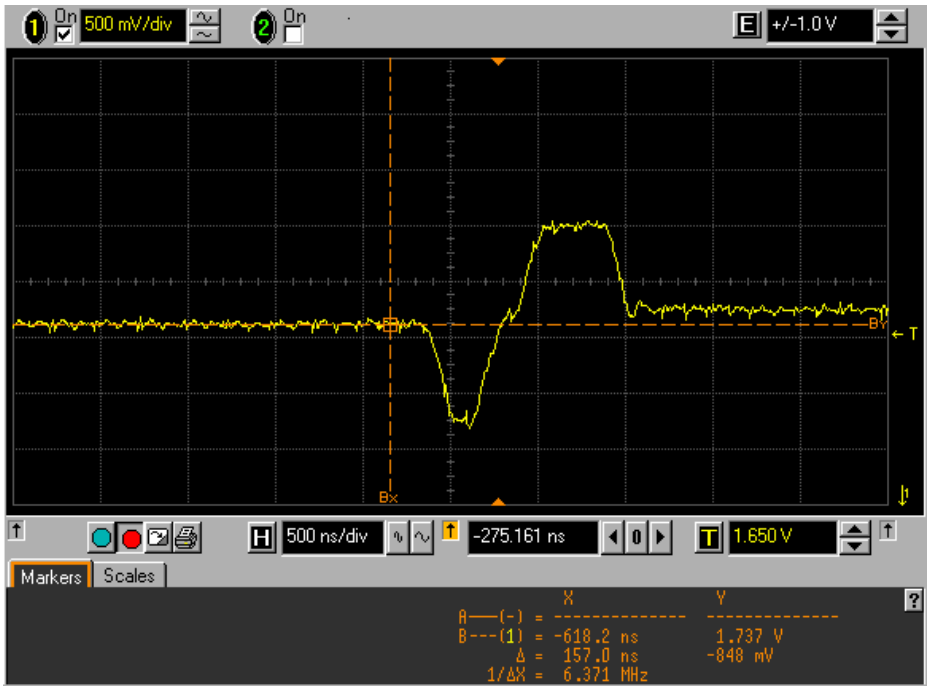

Figure 4.44: Measurement of 1x4 ROIC with input current 1nA, integration time 4 us, gain setting 1, output voltage is 1.737V, 37mV added to output

Further measurement results from 1x4 ROIC is given in table as voltage added to output.

	Gain Setting 1.30		Gain Setting 1		Gain Setting 0.65		Gain Setting 0.5	
	32u	16u	32u	16u	32u	16u	32u	16u
1nA	347	174	313	156	208	104	154	78
5nA	944	472	734	374	538	261	409	206
10nA	-	671	-	515	769	379	593	294
50nA	-	-	-	1391	-	967	-	749
100nA	-	-	-	-	-	1404	-	-

Table 4.2: Output voltage increase (mV) for integration times 32us and 16us

	Gain Setting 1.30		Gain Setting 1		Gain Setting 0.65		Gain Setting 0.5	
	8u	4u	8u	4u	8u	4u	8u	4u
1nA	84	43	72	36	53	-	38	-
5nA	238	119	181	97	130	-	105	-
10nA	335	165	255	128	193	-	149	-

50nA	899	446	690	344	486	243	376	189
100nA	1366	684	1075	531	725	359	565	280

Table 4.3: Output voltage increase (mV) for integration times 8us and 4us

In 2007 a 4x4 n-on-p ROIC is submitted with same functionalities of 1x4 ROIC in order to observe the effects of integrating more channels experimentally. Due to a resetting error at the offset cancellation circuit, measurement results of this ROIC is not represented in this work. Also a 72x4 ROIC is manufactured in March 2008 layout of which is shown in Figure 3.28. This chip has recently arrived from manufacturing and measurements of this ROIC are not done yet. At this moment its test board is to be manufactured.

Chapter 5 CONCLUSIONS

In this thesis, design of a CMOS readout integrated circuit for an array of 288x4 elements of n-on-p type HgCdTe detectors for long wave infrared spectrum is represented. Previous chapters include information, literature survey and detailed design procedure as well as simulations and measurement results towards achieving a functioning 288x4 ROIC.

As the input preamplifier selection, current mirroring integration type unit cells are used due to the detectors to be used in the focal plane array exhibits moderate shunt impedance of 1 MΩ. This unit cell has the drawback of high noise due to the current mirror nature. However requirement for a very low input impedance pointed out the choice of CMI unit cell. The unit cell's worst case input impedance is simulated to be 64KΩ. Hence, CMI shows an injection efficiency of %95 in worst case. In contrast, with the same technology DI preamplifier has a worst case impedance of 2.5MΩ, causing the injection efficiency to drop to %25.

In this ROIC time delay integration is applied on four detectors with a super sampling rate of three. Super sampling effectively increases the spatial resolution, while TDI increases SNR. In order to realize this, TDI is implemented by using a single amplifier and 26 analog memories. According to this principle, D1 has 11, D2 has 8, D3 has 5 and D4 has 2 capacitors. For bidirectional scanning, detectors' unit cells are switched instead of increasing the number of storage elements.

At each frame, an integration switch between a detector and one of the storage capacitors is on while all others are off, enabling integration of all detectors, simultaneously to one of its memory. Following the charge transfer on a storage capacitor, charge is saved for its addition to three other detectors stored charge at its required frame.

There are four switches associated with charge transfer from detector to TDI amplifier: INT, RESET, S1 and S2. Charge transfer to TDI stage is controlled by use of S1 and S2 switch that are generated from a digital control block. Charge transfer to TDI register is realized with the use of an op-amp. Together with S1 and S2 switches, this circuit forms a switch capacitor integrator. With an amplifier that has moderate gain of 66dB, but good slew rate of 100V/μsec, this circuit performs successful as shown in the simulations. However it suffers

from the parasitics associated with the bottom plates of the capacitors which results an additional offset.

In order to eliminate the offset, differential operation is used. This way, not only the error due to bottom plate parasitics but also charge injection and clock feedthrough effects are greatly reduced. This circuit is composed of an op-amp adder subtracter. Again, amplifier used in this circuit had a moderate gain of 60dB and good slew rate of 100 V/μsec. One of the requirements of ROIC is pixel deselection and automatic gain adjustments. Pixel deselection is handled by the digital programming functions. However, automatic gain adjustment according to programming data is handled at this stage as well through switching the resistors at the feedback network of the amplifier.

Output load of ROIC is 10pF in parallel with 1MΩ and requirement is that the output settles within 100nsec at every clock edge when a read operation is to be done. In order to achieve this, an op-amp buffer is used with slew rate 65V/μsec.

ROIC functionality is controlled by three, digital circuits. A main control block generates required INT, RESET, S1, and S2 signals for every channel and offset cancellation circuit, in addition to 7 bit channel select signal. An interface block programs the ROIC through serial and parallel interface. Finally, a block of decoders carries out the selection of signals generated from the control logic to be activated at the ROIC.

Digital control circuit functions by the help of two 3.3V clock signals. The first is the master clock signal CLK, which can set up to 5 MHz. All the control signals used in the ROIC are synchronized with this clock. The second is the integration clock INT, setting the integration time.

Main control block and interface circuits are designed through automatic synthesis. Logic is designed by Verilog programming language. Following the verification in code level, design is synthesized by using Synopsys design compiler and the netlist generated is mapped to AMS CORELIB 3.3V standard cell library elements. Following design verification at the schematics level, physical design is created using Silicon Ensemble tool. Decoders and level shifters (3.3 V to 5 V digital converters) are designed with full custom methodology.

Functionality of 288x4 ROIC is evaluated through simulation results given in previous chapters as well as measurement results of formerly designed 1x4 ROIC. In sum, designed

readout ROIC structure includes four elements time delay integration (TDI) functioning with a super sampling rate of 3, bidirectional TDI scanning, dead pixel deselection, automatic gain adjustment in response to pixel deselection, besides programmable four gain settings (up to 2.58pC storage), and programmable integration time. ROIC has four outputs with a dynamic range of 2.8V (from 1.7V to 4.5V) and input referred noise of 2989 electrons for an area of $13mm^2$.

All ROIC requirements are met but noise level. For future study noise level of ROIC is to be lowered, which is possible by using lower impedance values at the offset cancellation stage for a cost of higher power consumption. Also according to the experimental data obtained from 72x4 ROIC, any necessary modifications on 288x4 ROIC is to be finalized and 288x4 ROIC will be sent to manufacturing. Finally thanks to the success of this work, a new project, 576x7 ROIC in collaboration with ASELSAN is to be started in Sabanci University.

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