A 5.2 GHz RF COMBINED POWER AMPLIFIER WITH FULLY INTEGRATED ON-CHIP IMPEDANCE MATCHING WILKINSON POWER COMBINER AND SPLITTER

by

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Ercan Kaymaksüt

Electronics Engineering, Master of Science Thesis

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Keywords: IEEE, 802.11a, WLAN, RF IC, SiGe, BiCMOS, HBT, power amplifier,

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Abstract

In this thesis a 5.2 GHz combined power amplifier is designed for Wireless Local Area Network (WLAN) application. A new on-chip power combining technique by using impedance matching Wilkinson power divider circuits will be presented. Two impedance matching Wilkinson power dividers are employed for matching the input and output impedances of the amplifier to 50 Ω as well as splitting the input power into two amplifiers and combining their output powers. A 5.2 GHz fully integrated class-A mode combined power amplifier is designed in 0.35μ SiGE BiCMOS technology to asses the power combining technique for WLAN applications. The power amplifier with the on-chip lumped element impedance matching Wilkinson power divider circuits has a measured small signal gain of 5.21 dB. The output power at 1 dB compression point is measured as 22.4 dBm and the power added efficiency of 17% is achieved at 1 dB compression point. The chip area is significantly reduced by using lumped element impedance matching Wilkinson power dividers; the total die size is 1.2mm x 1.25mm, including RF and bias pads. The simulated (Cadence) and measured performance of Combined Power Amplifier are well matched. Thus the RF power amplifier and combiner/splitter circuits can be used for 5.2 GHz WLAN applications.

EMPEDANS UYUMLU WILKINSON GÜÇ BÖLÜCÜ İLE 5.2 GHz BİRLEŞTİRİLMİŞ GÜÇ KUVVETLENDİRİCİSİ TASARIMI

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Anahtar Kelimeler: IEEE, 802.11a, WLAN, RF IC, SiGe, BiCMOS, HBT, Güç

Kuvvetlendiricisi, Wilkinson Güç Bölücü

Özet

Bu tezde 5.2 GHz Kablosuz Yerel Ağ uygulamaları için bir birleştirilmiş güç kuvvetlendiricisi tasarlanmıştır. Empedans uyumlu Wilkinson güç kuvvetlendiricileri kullanılarak yeni bir güç birleştirme yöntemi ortaya konmuştur. İki tane empedans uyumlu Wilkinson Güç kuvvetlendiricisi kullanılarak hem kuvvetlendirici katının giriş çıkış empedansı 50 Ω'a uyumlaştırılmıştır hem de giriş gücü iki kuvvetlendiriciye bölünmüş ve iki kuvvetlendiricinin çıkış gücü toplanmıştır. Bu güç birleştirme tekniğini sınamak için 5.2 GHz de A sınıfı çalışan tamamen entegre bir güç kuvvetlendiricisi gerçeklenmiştir. Entegre edilmiş güç bölücü ve güç toplayıcı devreler ile güç kuvvetlendiricisinin kazancı 5.2 GHz de 5.21 dB olarak ölçülmüştür. 1 dB bastırma noktasında 22.4 dBm çıkış gücü ölçülmüş ve bu çıkış gücünde %17 katılmış güç verimliliği elde edilmiştir. Kırmığın toplam alanı yapılan ayrık eleman tasarımı sayesinde önemli oranda küçültülmüş ve 1.2mm x 1.25mm olarak gerçeklenmiştir. Similasyon sonuçları(Cadence) ile ölçüm sonuçları uyum içerisindedir. Tasarlanan güç kuvvetlendiricisi ve güç birleştirici/güç toplayıcı devreleri 5.2 GHz Kablosuz yerel ağ uygulamaları için uygundur.

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Chapter 1

1. Introduction

Wireless Local Area Networks (WLAN) connects two or more computers without using wire. This gives the users the mobility to move around within the coverage of the network. WLAN applications generally use the 83.5 MHz bandwidth in the 2.4 GHz band. The WLAN gains popularity mostly because of replacing personal computers with portable laptops. WLAN attracts home users with its ease of installation and location freedom. The growing interest in the WLAN market motivated for the new technologies that can enable higher data rates and capacity. Therefore the IEEE 802.11a WLAN standards have associated 5 GHz band for WLAN applications. The 200 MHz bandwidth available in the 5 GHz band enables high data rate, increased system capacity and low interference [1]. WLAN utilizes orthogonal time division multiplexing modulation scheme in order to achieve high data rates. The IEEE 802.11g standards offers 5 to 10 times more data rates at 5 GHz band than the conventional IEEE 802.11b systems [2].

The output power of the devices has an important effect on the coverage of the wireless network. Standards arranges the maximum allowable output power for each frequency band. Each of the standards requires a power amplifier for the final amplification.

Traditionally, III-V heterojunction bipolar technologies (HBT) such as Ga-As is preferred for high power applications at high frequencies. Integrating the power amplifier is the most challenging part in the single chip transceiver design. However, SiGe BiCMOS technology

has a unique opportunity in the wireless marketplace because it can provide the performance of III-V HBTs and the cost benefits of silicon bipolar technology. Therefore a higher level integration can be accomplished by using CMOS for digital processor and HBT's in the high frequency design[3]. Silicon Germanium (SiGe) HBTs have proven themselves as cheaper, viable replacements for GaAs in many different applications.

This thesis describes the design of a fully integrated SiGe BiCMOS combined power amplifier. We address the design of a 5 GHz PA for WLAN 802.11a applications. SiGe devices capable of 5 GHz operation have a low collector-emitter breakdown voltage. Therefore low load impedance is needed to achieve high output power. Matching a few ohms to 50 Ω results in very high losses due to low resistivity silicon substrate. Therefore, the solution could be to use power combining techniques. To overcome this restriction various power combining techniques have been developed over years. These different power combining techniques are summarized and discussed in [8]. In recent works distributed amplifier topology [9-11] are used to combine multiple amplifiers output power. However this technique is used for achieving high gain bandwidth product. Therefore this topology is not suitable for high power applications. On the other hand, transformer based power combining techniques [12-15] are the most common on-chip method for achieving high powers. Main drawback of this power combining technique is the large size and high insertion loss of the on-chip transformers. Another high combining efficiency power combining technique is spatial combining technique [16], [17]. But integrating spatial combiners is very challenging because of the size limitations of the antennas. For circuit level combining, Wilkinson power divider based power combining techniques are widely used in the industry. This technique can also be applied to chip level combining [19]. In this thesis two integrated Wilkinson power dividers are used to combine output powers of the two amplifiers. The power combining techniques are discussed in detail in chapter 4.

In this thesis, impedance matching Wilkinson power dividers are used to combine two amplifier blocks so that higher output power is obtained. In addition, impedance matching Wilkinson power dividers accomplishes the matching duty so that no additional impedance matching is needed. The power combining technique increases the linearity of the power amplifier therefore higher output power can be obtained with respect to single amplifier for a given technology.

Two impedance matching Wilkinson power dividers are employed for matching the input and output impedances of the amplifier to 50 Ω as well as splitting the input power into two amplifiers and combining their output powers. A 5.2 GHz fully integrated class-A mode combined power amplifier is designed in 0.35µ SiGE BiCMOS technology to asses the power combining technique for WLAN applications. The impedance matching Wilkinson power dividers and power amplifier are designed and simulated by using Cadence and Advanced System Design (ADS). The impedance matching Wilkinson power dividers and PA are fabricated and measured separately in order to classify their performance individually. Two fabricated IMWPD circuits (splitter and combiner) have insertion losses better than 1.4dB, and return losses less than -13dB and port-to-port isolation > 12 dB at 5.2GHz. The power amplifier with the on-chip lumped element impedance matching Wilkinson power divider circuits has a measured small signal gain of 5.21 dB. The output power at 1 dB compression point is measured as 22.4 dBm and the power added efficiency of 17% is achieved at 1 dB compression point. The chip area is significantly reduced by using lumped element impedance matching Wilkinson power dividers; the total die size is 1.2mm x 1.25mm, including RF and bias pads. The simulated (Cadence) and measured performance of Combined Power Amplifier are well matched. Thus the RF power amplifier and combiner/splitter circuits can be used for 5.2 GHz WLAN applications.

The material in this thesis is organized as follows:
Chapter 2 contains basic information about power amplifiers. Design parameters for power amplifier is described in this chapter. In addition power amplifier classes and different power amplifier topologies are discussed in this chapter.

In Chapter 3, basic design procedure of a 5 GHz Class A single stage power amplifier is given in detail. The device I-V characteristics, load pull simulations and input/output matching network design are all presented as part of the PA design roadmap.

In Chapter 4, some common power combining techniques will be described and the proposed power combining technique will be presented. The theoretical background of the impedance matching Wilkinson power dividers are supported with simulation and measurement results of the two manufactured impedance matching Wilkinson power dividers in 0.35µ AMS SiGe HBT technology.

In Chapter 5, the simulation and measurement results for the overall combined power amplifier will be given.

And finally in Chapter 6, the thesis will be concluded with comments on the performance of both impedance matching Wilkinson power divider and the overall power amplifier.

Chapter 2

2. Power Amplifier Basics

Power amplifiers (PA) are being used in many diverse applications. Power amplifiers are the last stage of the transmitter chain where highest RF power is generated and highest DC power is consumed. A schematic of a basic RF power amplifier is given in Fig. 2.1. Schematic of the RF power amplifiers is very similar to an ordinary RF amplifier. The PA consists of RF choke and DC bias circuits for biasing the RF transistor and input/output matching circuits are used for matching the optimum source and load impedances to 50Ω as in all RF devices.

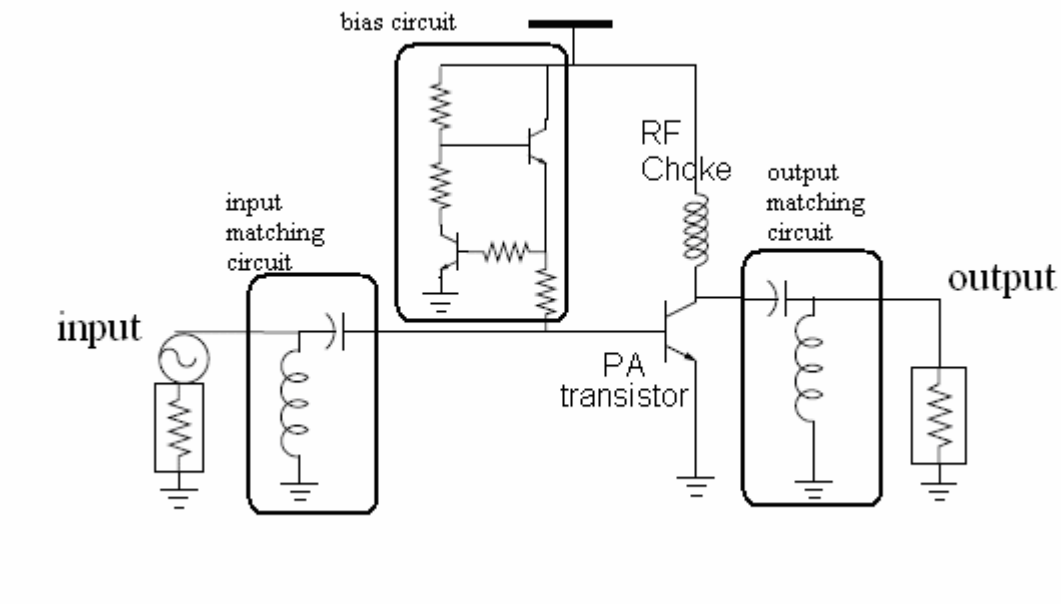

Fig. 2-1 Schematic view of a single stage RF power Amplifier

The main difference of the power amplifiers with respect to the small signal amplifiers are mainly the output matching circuit. In power amplifier designs, the output matching circuit is configured such that the maximum voltage and current swing occurs in the load of the transistor. The requirements of PA vary depending on application. For characterizing the power amplifiers, some criteria are developed. In this chapter firstly some of the major figures of merit of Power Amplifiers will be explained, then power amplifier classes will be mentioned.

2.1 Power Amplifier Performance Parameters

2.1.1 Output Power

The output power of a power amplifier is the main design parameter for a power amplifier. The power level needed to be delivered to the transmitted antenna is defined by the communication standards of the system. The combined PA is designed for 5.2 GHz WLAN applications and the maximum allowed effective radiated power for this system is 200 mW (23 dBm). The effective radiated power is the multiplication of driven power to the antenna and antenna gain. Therefore 21 dBm maximum output power is needed assuming the antenna gain is 2 dBi (antenna is approximately omni directional)

2.1.2 Gain

An amplifier's gain can be described as voltage gain, current gain, or power gain. The gain of power amplifiers are generally described in power gain. The small signal power gain can be described by three definitions; transducer gain (G_T), operating gain (G_P), available gain (G_a). Transducer gain is defined by:

$$G_T = \frac{Power\_Delivered\_to\_the\_Load}{Power\_Available\_From\_Source} \qquad (2.1)$$

In this power definition the reflection losses at the input and output ports are taken into account. The transducer gain is the most widely used gain definition for power amplifiers. The gain of the amplifier is constant in the low power region. Amplifiers generally operate linearly in this region. The transducer gain of an amplifier can be given as by using scattering parameters as:

$$G_T[dB] = 10 \log \left| S_{21} \right|^2 \qquad (2.2)$$

In the operating power gain definition, only the reflections at the output are taken into account. So the power input to the amplifier is considered instead of power available from source. The operating power gain is defined as:

$$G_P = \frac{Power\_Delivered\_to\_the\_Load}{Power\_input\_to\_the\_Amplifier} \qquad (2.3)$$

The available power gain considers the reflections at the input so the input power defines as the power available from the source but the reflections at the output is not considered. The available gain is defined as:

$$G_a = \frac{Power\_Available\_From\_the\_Amplifier}{Power\_Available\_From\_Source} \qquad (2.4)$$

According to the power definitions given above we can conclude that $G_P \geq G_T$ and $G_a \geq G_T$. In the conjugate matched condition the gain of the amplifier should be the same according to all three gain definitions.($G_T = G_P = G_a$)

The gain of the amplifiers starts to drop in the high power region. The saturated gain is the power gain when the maximum output power is obtained from the amplifier. The saturated gain can be defined as:

$$G\ [dB] = P_{out}(sat)[dB] - P_{in}(sat)[dB] \qquad (2.5)$$

The required gain of the power amplifiers varies from application to application but generally by using high gain amplifiers the number of amplifier stages can be reduced which gives an important cost reduction. In addition to high gain, generally the gain of the amplifier is required to be flat over the operating frequency band.

2.1.3 Linearity

In the linear region of an amplifier, gain is constant for a given frequency. As the input power is increased, the gain of the amplifier starts to drop. Linearity is a measure of how much linear power can be delivered to the load. Linearity is the most important criteria for power amplifiers for WLAN applications because of the higher order modulation shames used in this system. There are two important parameters that can be measured for evaluating the linearity performance of the amplifier: 1 dB compression point and third order intercept point.

a) 1 dB compression point

1dB compression point is defined as the power level for which the gain of the amplifier drops down 1 dB with respect to the linear gain for a specific frequency. 1 dB compression point can be expressed as input or output referred. This power level can be interpreted as the end of the linear operation. The 1 dB compression point for an amplifier is given in Fig. 2.2. 1dB compression point can be found by intersecting the actual gain and (small signal gain-1 dB) curves.

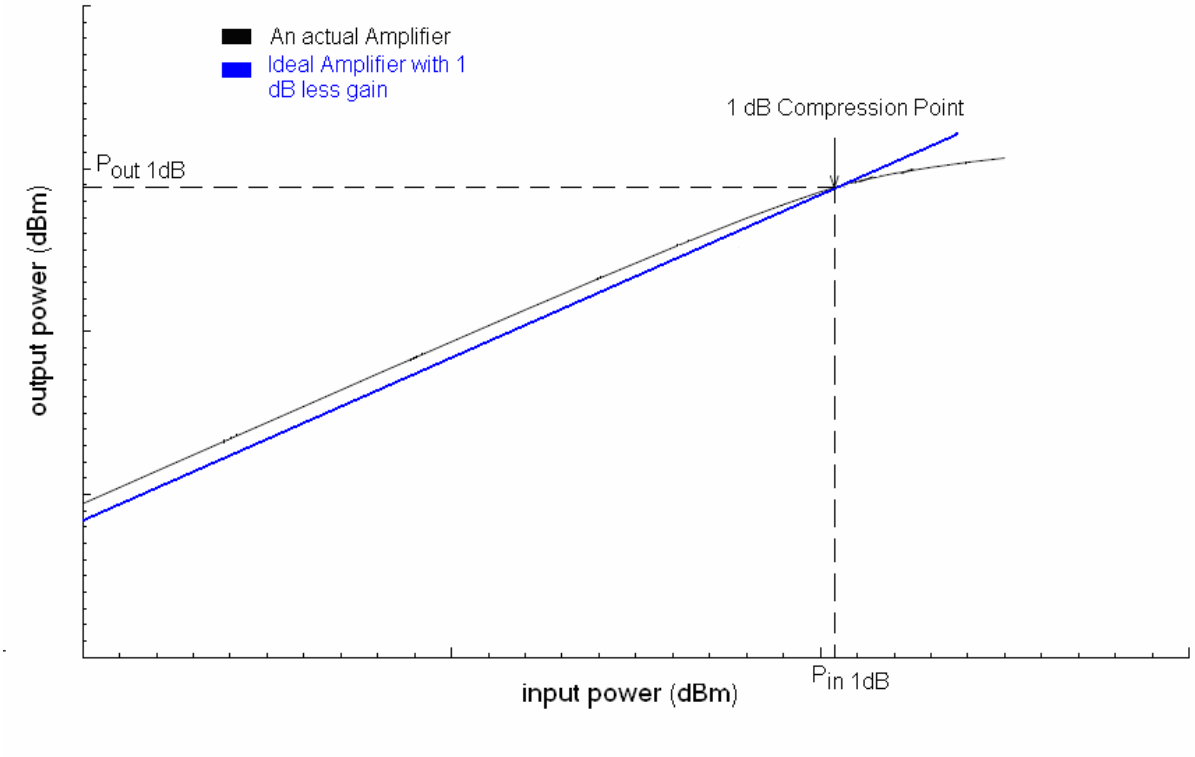

Fig. 2.2 1 dB compression point characteristics

b) Nth order intercept point

In the high power region, an amplifier introduces distortions into the output signal. For a BJT amplifier the relationship between collector current and base emitter voltage can be given as in (2.6) where K_1 is the Tranconductance of the amplifier and K_2, K_3 … are the square ,cubic, etc. nonlinearity coefficients.

$$I_C = K_1 v_{BE} + K_2 v_{BE} + K_3 v_{BE} + \ldots \qquad (2.6)$$

Assuming an input signal consisting of two very close tones ω_1 and ω_2 both in amplitudes of A_1, Base- Emitter voltage v_{BE} can be written as,

$$v_{BE} = A_1 \cos(w_1 t) + A_1 \cos(w_2 t) \qquad (2.7)$$

Where

$$w_1 - w_2 << w_1, w_2 \qquad (2.8)$$

These input signals create outputs with intermodulation products at the frequencies:

$$w_{out} = nw_1 \mp mw_2 \qquad (2.9)$$

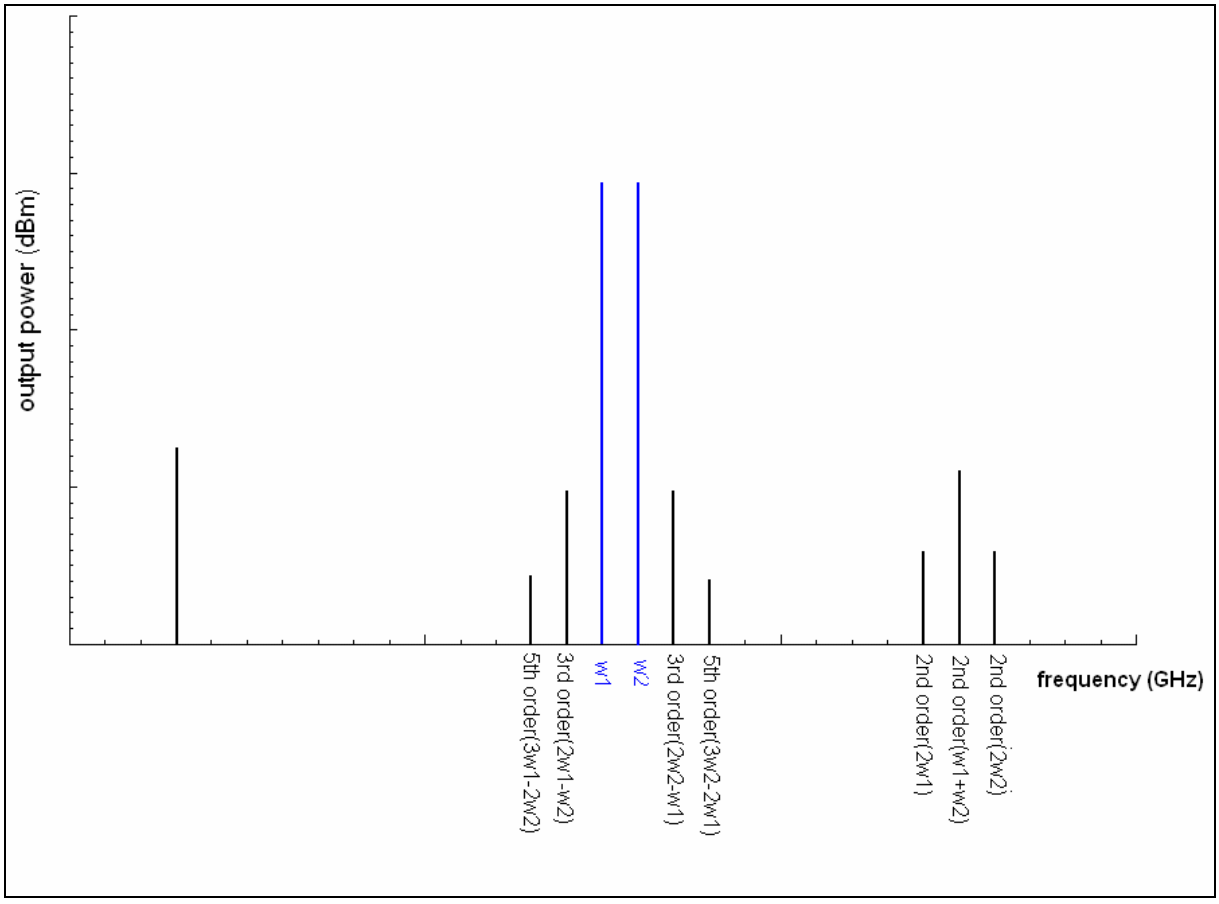

Fig. 2.3 Output Power spectrum for a PA with intermodulation products

The orders of intermodulation products are given as (n+m). The power of these intermodulation products can be given as,

$$P_{IMP} = (K_{IMP} P_{in})^{(n+m)} \qquad (2.10)$$

Where K_{IMP} is the coefficient for that intermodulation product.

The output frequency spectrum of an amplifier with intermodulation products is given in Fig. 2.3.

The third order intermodulation products (at frequencies 2w1-w2 and 2w2-w1) are typically the most critical ones because they are the closest products to the fundamental and it is hard to filter them out from the pass band. (see Fig.2.3). The power of the third order intermodulation products has a cubic relationship given in (2.10) so as the power increases the intermodulation products increases more rapidly than the fundamental products.
In the dB scale, power of third order intermodulation products increase by 3dB when the fundamental tones increase by only 1dB.

Minor harmonic distortion occurs when power amplifiers are operating with small input power, in the linear region. However with the increase of the input power nonlinearities and intermodulation products start to be visible on the output as nonlinear effects increase. The 3rd order intercept point, IP3, is defined by the crossing of the fundamental frequency and the 3rd order intermodulation curve. As the transistors saturate at the higher power region, (2.10) is not valid beyond some power range. The 3rd order intercept point can be found by extrapolating the fundamental frequency term and 3rd order intermodulation term as given in Fig.2.4. The other order intercept points are defined the same way as the 3rd order intercept point.

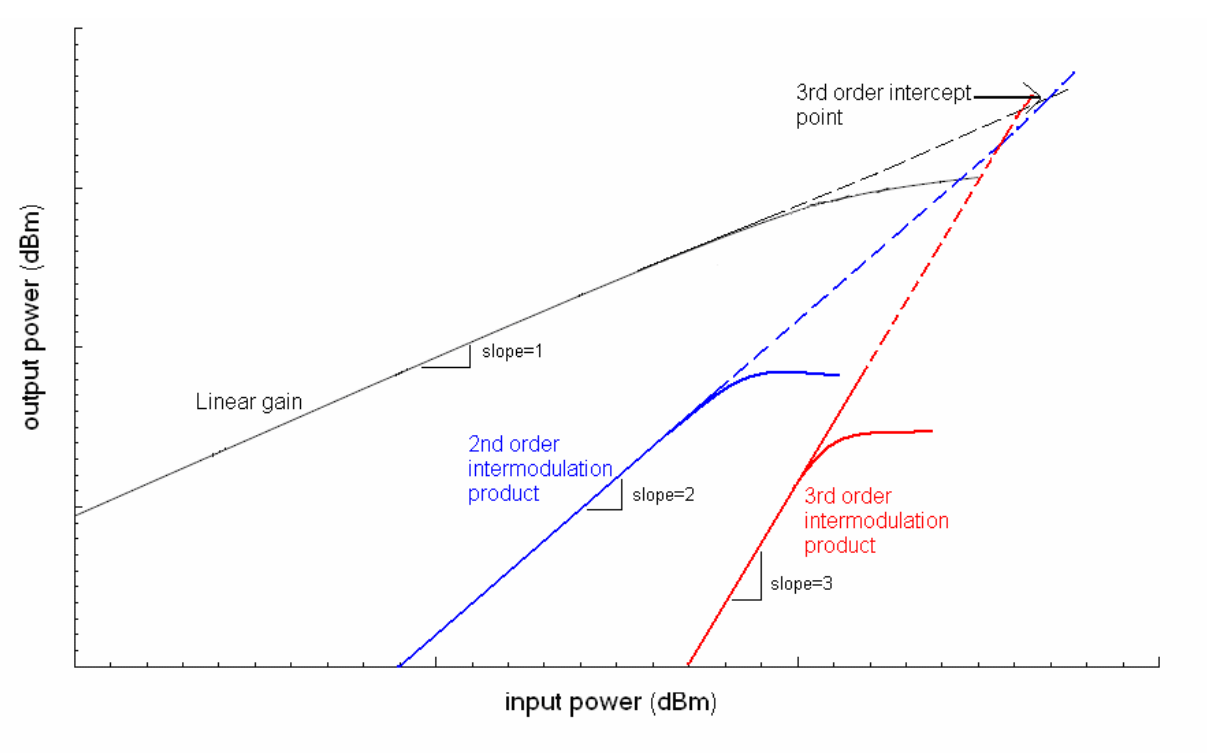

Fig. 2.4 Graphical explanations of the intercept points

It can be seen in Fig.2.4 that 3rd order intercept point can be determined geometrically from the output power spectrum for any given power level when the intermodulation terms are presented.

The output referred 3rd order intercept point OIP3 can be given as,

$$OIP3[dBm] = P(f1) + \frac{P(f1) - P(IMP)}{2} \qquad (2.10)$$

2.1.4 Efficiency

The efficiency is very important figure of merit for a power amplifier. Power amplifiers are generally the most power consuming block of the transmitter. For this reason the overall efficiency of the transmitter is pretty much determined by the efficiency of the power amplifier. There are two commonly used definitions available for this key parameter of the power amplifier: drain efficiency, power added efficiency.

a) Drain efficiency

Drain efficiency is the ratio of the output power to the DC power consumption:

$$Eff_{drain} = \frac{P_{RFout}}{P_{DC}} \qquad (2.11)$$

Drain efficiency is a measure of how much of the DC power is converted to RF power. This efficiency definition does not take into account the input RF power.

b) 2.4.2 Power Added Efficiency

Power added efficiency takes into account the input RF power to drive the amplifier. The power added efficiency is defined as the ratio of the RF power added by the amplifier to the DC power consumption:

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \qquad (2.12)$$

The power added efficiency is less than the drain efficiency for finite gain amplifiers. The difference between these two efficiency definitions extends as the gain of the amplifier increases.

2.1.5 Error Vector Magnitude (EVM)

The nonlinearities in power amplifiers cause also degradation in the digitally modulated systems. The digital data transferred onto and RF carrier by changing the RF carrier's amplitude and phase by the help of modulators. The carrier occupies a point in I versus Q plane and can be treated as a vector starting from the origin. The nonlinearities introduced by the PA can produce distortion in of phase and amplitude, which results in a distorted constellation diagram, as shown in Fig. 2.5.

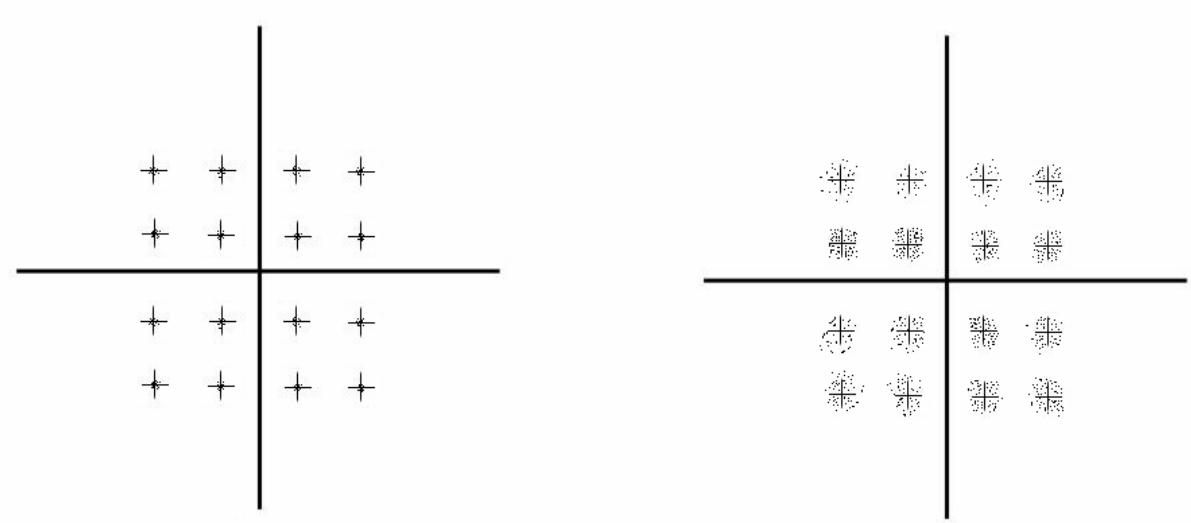

Figure 2.5 Non-distorted 16-QAM input signal (left) and the same signal after a nonlinear distortion (right).

Error vector magnitude (EVM) is a measure of degradation of the digitally modulated signals. The EVM is a direct function of Bit Error Rate which is an important measure in digital communication systems [4]

Assuming that the ideal signal is known, it is possible to calculate the error between the distorted signal and the ideal signal. The modulation schemes decide the ideal transmitted signal. EVM is defined by the scalar distance between two signal vector end points as shown in Fig. 2.6. It is common that EVM is reported as a percentage of the peak signal level.

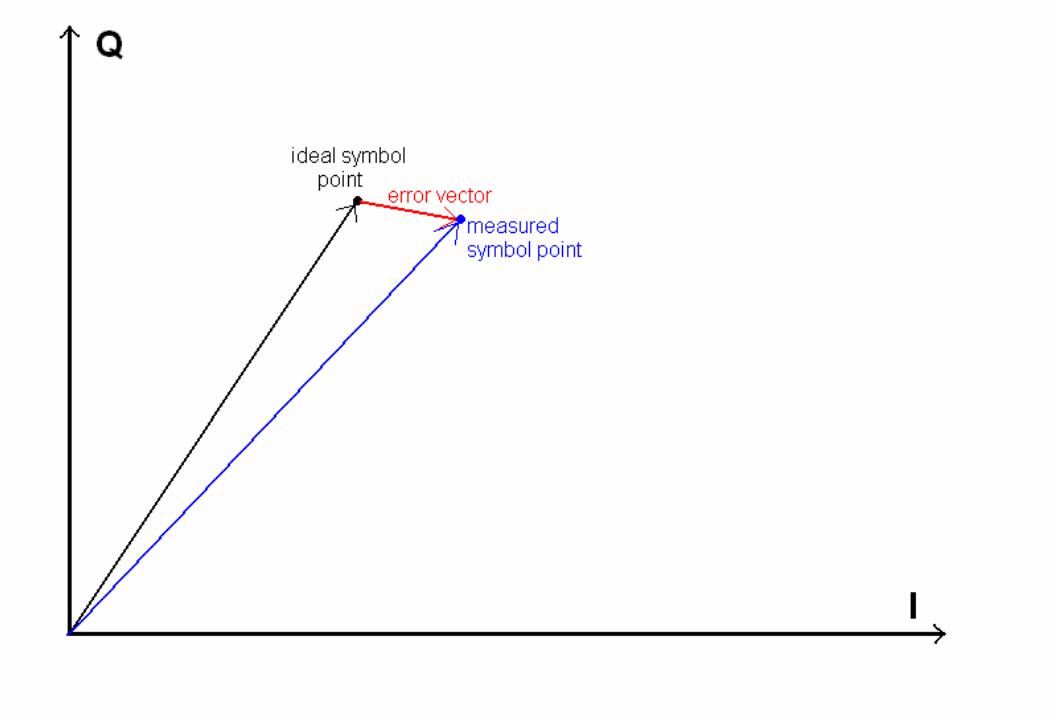

Fig. 2.6 Error vector is shown in IQ plot for a digitally modulated signal

2.2 Power Amplifier Classes

Efficiency is very important parameter in a power amplifier design, therefore many different power amplifier topologies are developed for improving efficiency. Power Amplifiers can be categorized by their operating mode into two groups as linear power amplifiers and non-linear (switching-mode) power amplifiers. The class of the amplifier is determined by the topology, bias condition for the active device and the driving input signal. Class A, AB, B and C can be classified in linear mode power amplifiers as the output signal is a linear multiplication of the input signal for all or some portion of the input signal. For the linear power amplifiers efficiency drops drastically as the amplified fraction of the input signal increases.

Class D, E and F are some of the non-linear power amplifiers. The active device works as a switch for these topologies. The efficiency improves in these non-linear classes but the output signal is no longer a linear function of the input signal level. Therefore switching mode power amplifiers are not suitable for amplitude modulated signals.

Brief background information about different classes of PA's will be presented in the next subsections. However, Class A will be emphasized more than other classes.

2.2.1. Class A

The linear amplifiers are classified by their bias conditions. Every small signal amplifier is biased in the middle of its active region, and it stays in the active region for the complete period of the input signal. The conduction angle is defined as the angle of the input signal oven which the transistor stays in the active region-"conducts". Class A amplifiers are used to amplify with high linearity which means minimum distortion. So the class A amplifiers are biased as small signal amplifiers. Class A amplifier can be defined as the transistor is always biased on. The conduction angle for a Class A amplifier is 360°. Commonly Class A power amplifiers are built by using the general topology for linear power amplifiers given in Fig.2.7. This topology is called inductively loaded class A power amplifier as RF choke is used for achieving two times more voltage swing as the resistor loaded case.

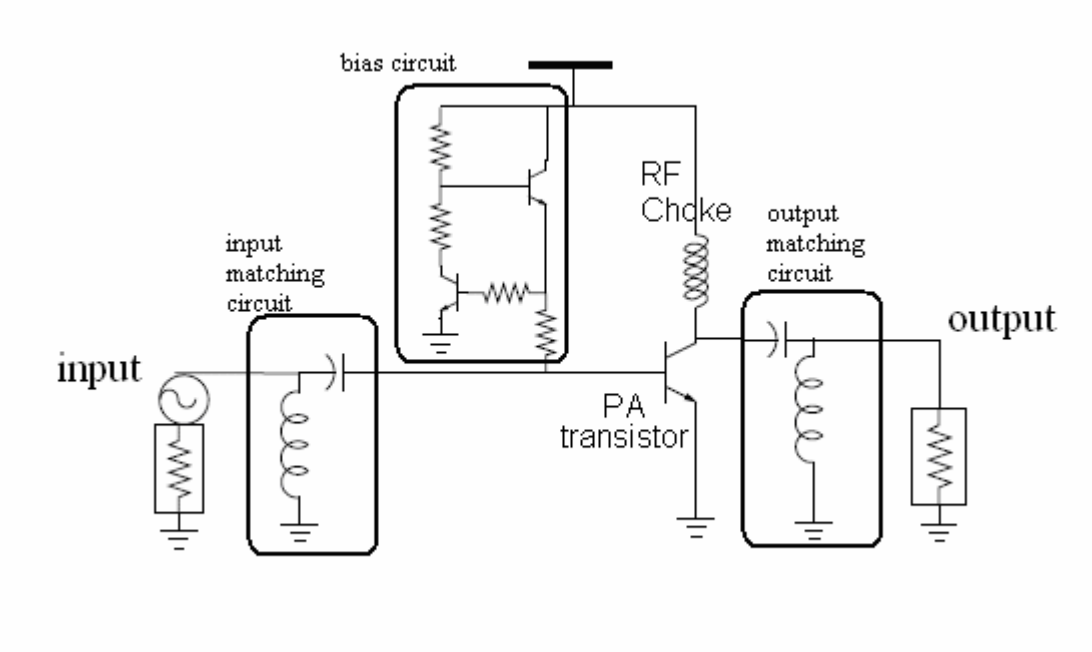

Fig. 2.7 Topology for linear Power Amplifiers

Assuming the input signal is sinusoidal (this assumption is valid for most of the modern communication systems), we can write the total amplifier current as:

$$I_C = I_Q + I_{Peak} \cos wt \qquad (2.13)$$

Where I_Q is the bias current and I_{Peak} is the peak value of AC current.

The total current swing should be less than the maximum allowed current for the transistor:

$$I_Q + I_{Peak} \leq I_{MAX} \qquad (2.14)$$

The maximum allowed current for a given transistor is generally based on thermal considerations for a BJT transistor. For the FET case in addition to thermal conditions saturation condition is also considered [5].

As the device designed to be always biased on in the class A topology:

$$I_{Peak} \leq I_Q \qquad (2.15)$$

For Class A, choosing $I_Q = I_{MAX} / 2$ gives the maximum RF current swing where

$$I_{Peak} = I_{MAX} / 2 \qquad (2.16)$$

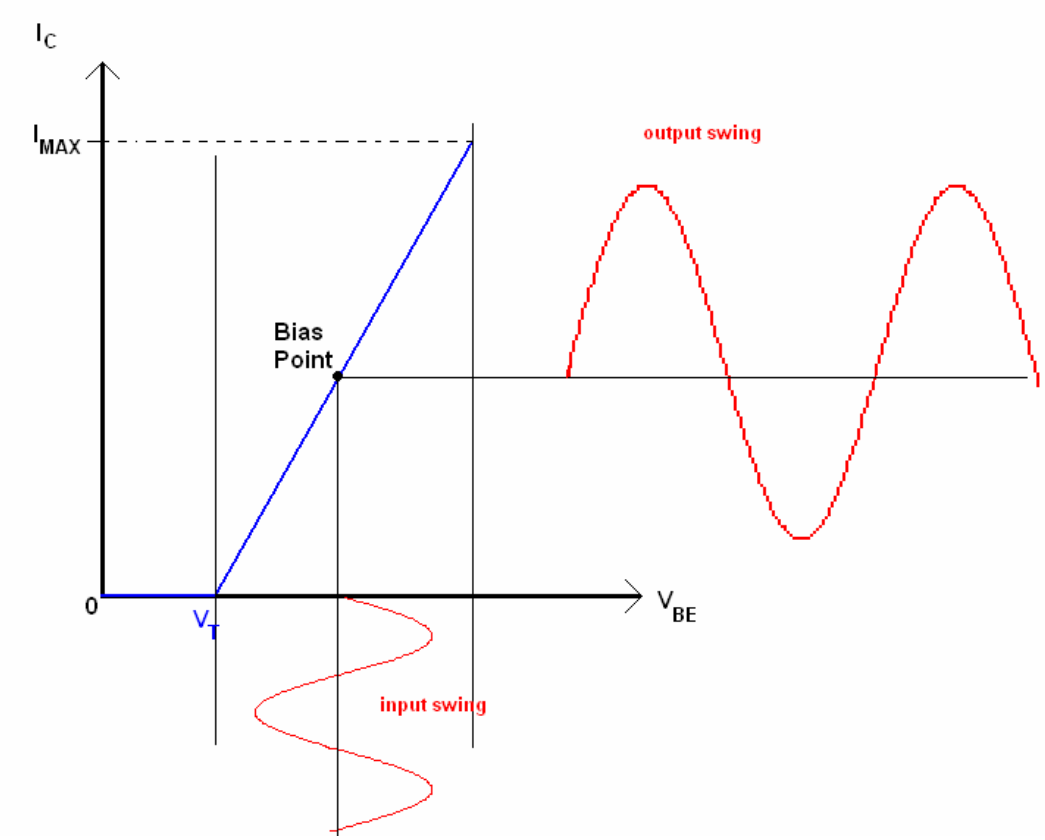

Fig. 2.8 Class A power amplifier Bias Point and input/output swings

The bias point for the class A condition is given in Fig 2.8 with corresponding input voltage swing and output current swing.

The peak Voltage can be represented by the multiplication of peak current and load resistor and for the inductively loaded class A PA peak voltage can be represented as:

$$V_{Peak} = I_{Peak} R_L \leq V_{CC} - V_{SAT} \qquad (2.17)$$

The DC power consumption can be calculated as:

$$P_{DC} = I_Q V_{CC} \qquad (2.18)$$

Then the output RF power is :

$$P_{RF} = \frac{I_{Peak}{}^2 R_L}{2} \qquad (2.19)$$

Therefore the efficiency can be calculated as:

$$\eta = \frac{I_{Peak}{}^2 R_L}{2 I_Q V_{CC}} \qquad (2.20)$$

The efficiency expression given in (2.20) stated that as the drive increases the efficiency also increases with the square of the output current or voltage swing. The maximum efficiency occurs when the current and voltage swings take on their maximum values. ($I_{Peak}=I_Q$, $V_{Peak}=V_{CC}-V_{SAT}$) . This condition can be satisfied by choosing a proper load impedance.

$$P_{RFMAX} = \frac{I_Q (V_{CC} - V_{SAT})}{2} \qquad (2.21)$$

$$\eta_{MAX} = \frac{V_{CC} - V_{SAT}}{2 V_{CC}} \qquad (2.22)$$

Therefore the maximum efficiency from a class-A amplifier cannot exceed 50% This efficiency is a theoretic value assuming $V_{SAT}=0$.

The collector voltage swing versus efficiency is plotted in Fig 2.9. The efficiency for a class A amplifier drops rapidly as the output voltage swing decreases. When the amplitude modulated signals are applied to the power amplifier, the overall efficiency will drop drastically as the overall output power decreases.

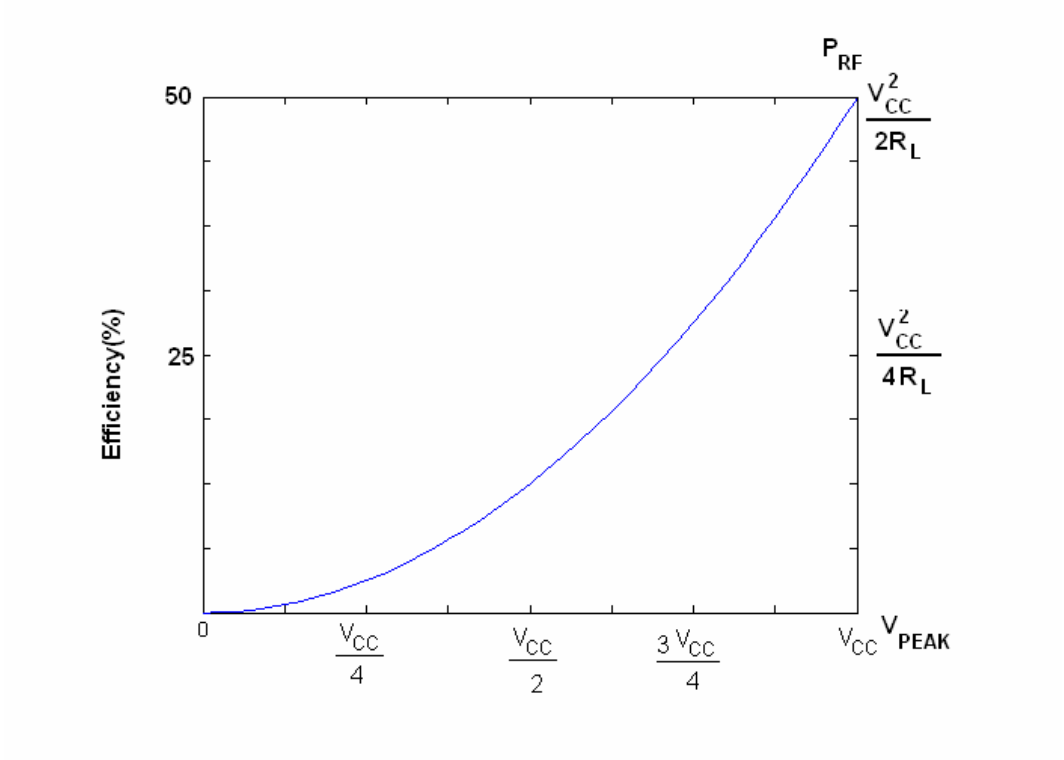

Fig. 2.9 Collector Voltage swing versus efficiency and Output power for Class A PA

2.2.2 Class B

Class B is another linear amplifier class. Therefore the output voltage amplitude is a constant multiplication of the input voltage amplitude. The difference between Class A and Class B amplifiers are the conduction angle. The conduction angle of a Class B amplifier remains 180°, independent of the input drive level. The conduction angle of class B amplifier is given schematically in Fig. 2.10. In Fig. 2.10 the transfer function of the transistor is given with tranconductance G and threshold voltage V_T.

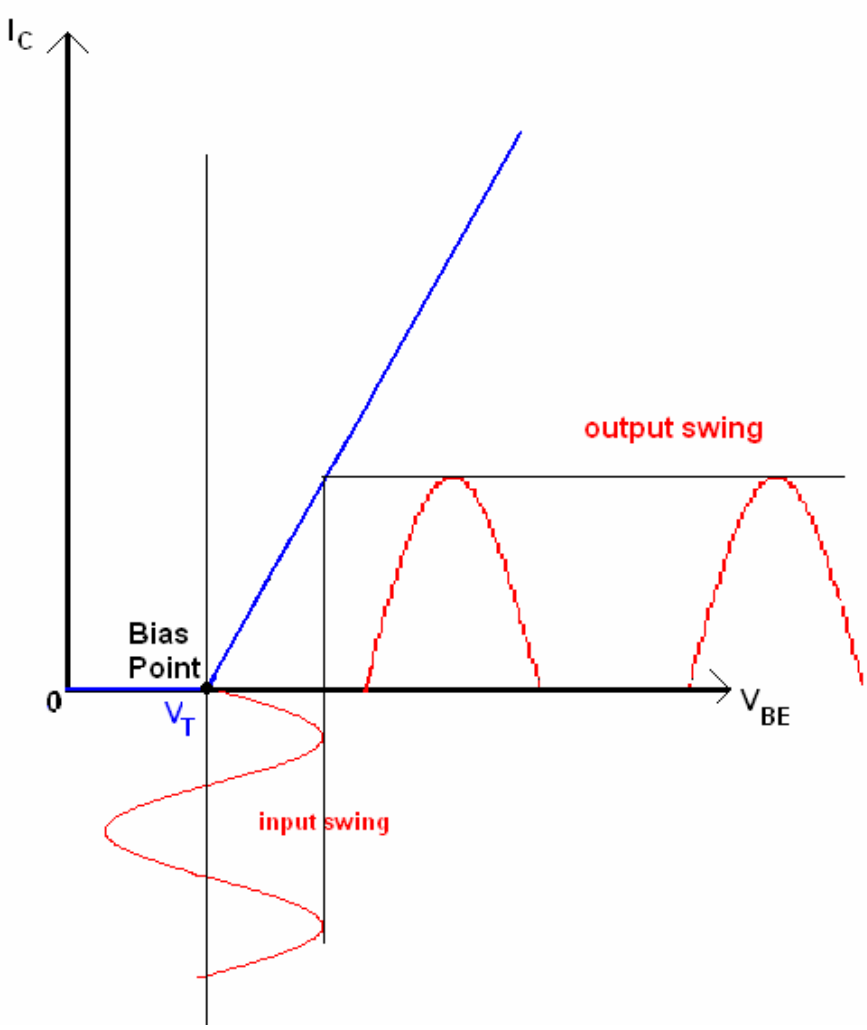

Fig. 2.10 Class B power amplifier Bias Point and input/output swings

Class B power amplifiers are commonly realized by using push-pull topology given in Fig.2.11. In this topology two transistors are used and each of them biased at the threshold points. Therefore each of them conducts only half of the period. The output is the combination of two class B amplifiers so full sinusoidal waveform can be obtained [6].

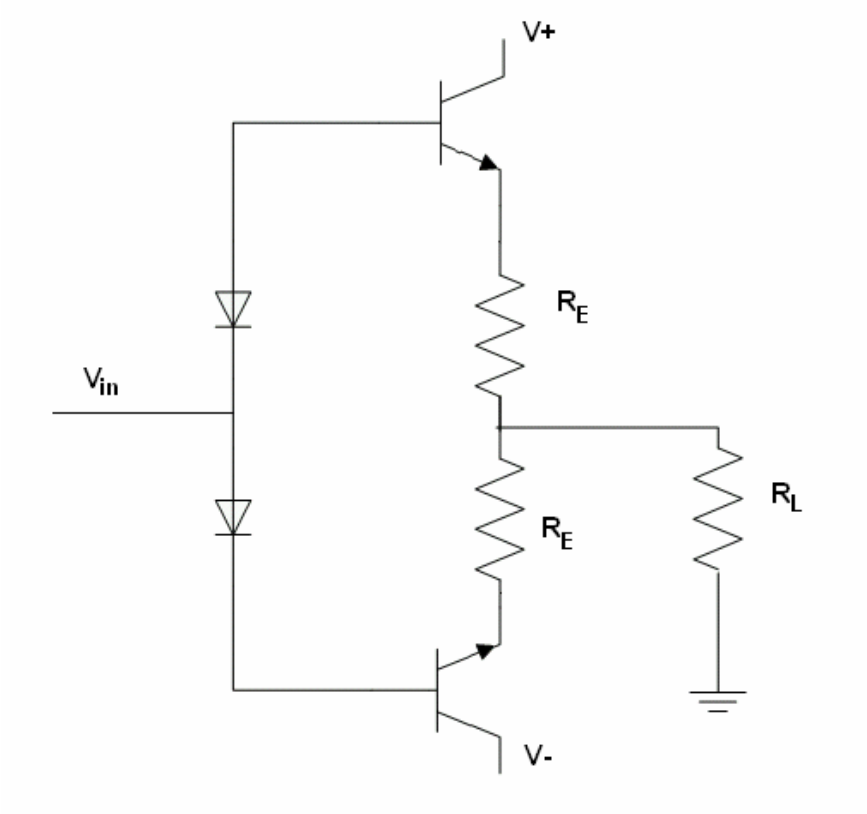

Fig. 2.11 Push-Pull Amplifier Topology

When the applied voltage Vin exceeds the threshold voltage, the output voltage can be calculated as Io=G(Vin-Vt) for the given basic transfer fuction. And the current is zero when the input voltage falls below the threshold. To satisfy the 180° conduction angle, the bias voltage should be choosen exactly as the threshold voltage. The output current is simply half wave sinusoids given in Fig. 2.10 . This time domain output can be expanded as Fourier series

$$I_0(t) = \frac{I_P}{\pi} + \frac{I_P}{2}\cos wt + \frac{2I_P}{3\pi}\cos w2t - \frac{2I_P}{15\pi}\cos w4t.... \qquad (2.23)$$

Low Pass or bandpass filters can be used to eliminate the higher order harmonics [6]. Therefore output would be full sinusoid with zero DC offset. The peak voltage of the output after filtering can be given as:

$$V_{PEAK} = \frac{V_{in}GR_L}{2} \qquad (2.24)$$

Note that (2.24) shows a linear relation ship between the input and output as expected. The DC current consumption can be calculated from equation (2.23) as $\frac{I_P}{\pi}$, Therefore the DC power consumption can be calculated as

$$P_{DC} = \frac{V_{CC} I_P}{\pi} \qquad (2.25)$$

$$P_{RF} = \frac{{I_P}^2 R_L}{8} \qquad (2.26)$$

$$\eta = \frac{I_P R_L \pi}{8 V_{CC}} \qquad (2.27)$$

The maximum output RF power of Class B amplifier is the same as the class A amplifier, as both topologies can have an RF current swing of $I_{MAX}/2$ at the desired frequency. See (2.23). (2.27) states that efficiency rises linearly with input drive. Maximum efficiency can be achieved by choosing load impedance to generate maximum current and voltage swing at the same time. The maximum output current swing for class B amplifier is I_{MAX} and maximum output voltage swing is (V_{CC}-V_{sat}) Therefore maximum efficiency can be calculated as

$$\eta_{MAX} = \left(\frac{V_{CC} - V_{SAT}}{V_{CC}} \right) \frac{\pi}{4} \qquad (2.28)$$

In (2.28)assuming V_{sat}=0 the efficiency can be achieve as high as $\frac{\pi}{4} \approx 78\%$

2.2.3 CLASS AB

The assumption of constant G_m for the entire active region is not valid for practical transistors. Especially near the threshold region the reduction of G_m causes distortions. The most linear G_m can be obtained at the middle of the active region. This is the reason that class A amplifiers are the most linear out of all classes [5].

The conduction angles of class AB amplifiers are between 360°-180°. The transistors generally biased at a little bit higher voltage than threshold voltage. Therefore the transistor operates in a more linear Gm region. The bias point and conduction angle can be seen in Fig. 2.12.

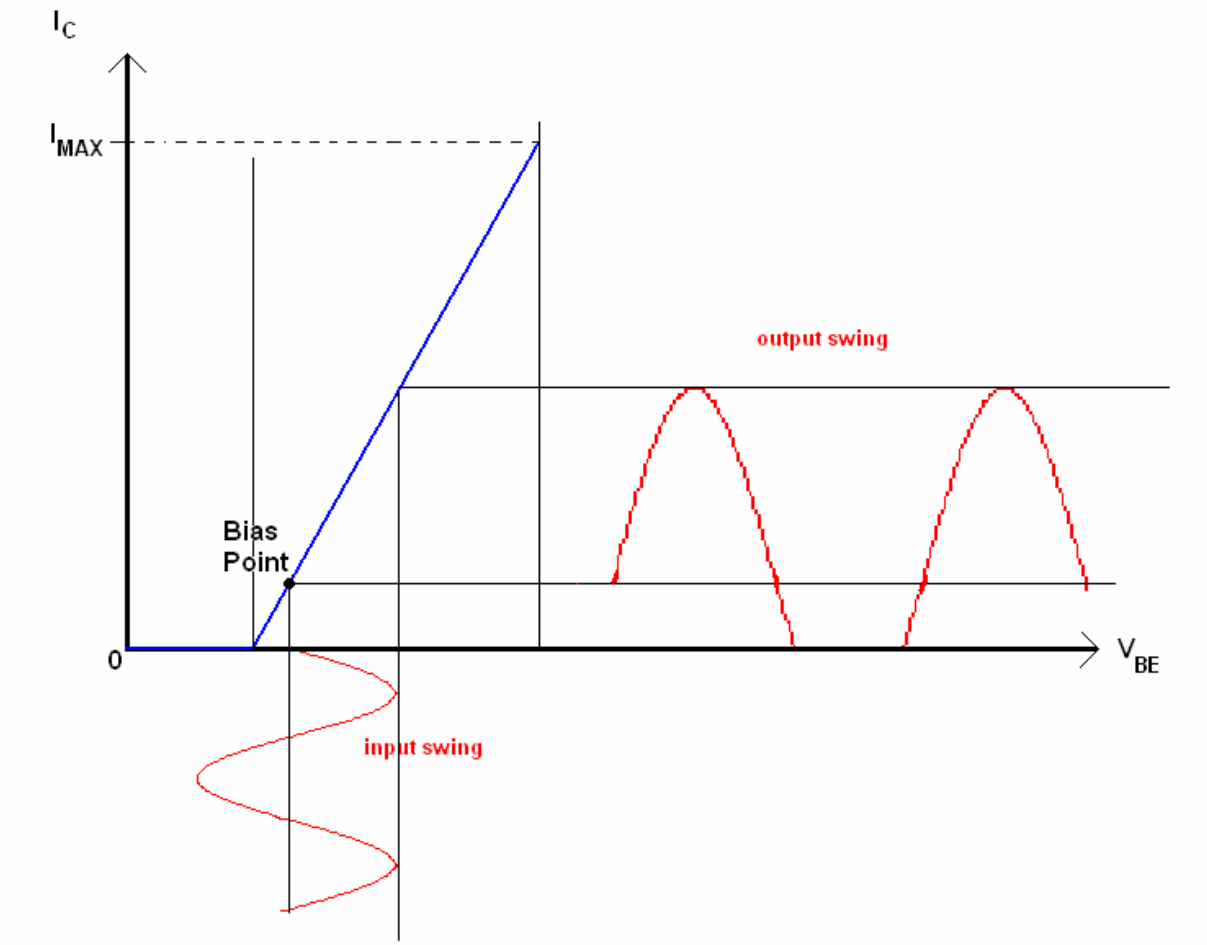

Fig. 2.12 Class AB power amplifier Bias Point and input/output swings

Class AB is a trade-off between class A and Class B in terms of linearity and efficiency. Generally push pull topology is used for class AB amplifiers (see Fig.2.11)

2.2.4 CLASS C

The efficiency of the power amplifier can be further increased by decreasing the conduction angle. Class C amplifier is biased below the threshold voltage of the transistors so the transistor is biased on less than half of the period. The efficiency increases because the turn on time of the transistor decreases. In Fig 2.13 the bias point and input/output voltage swings are given.

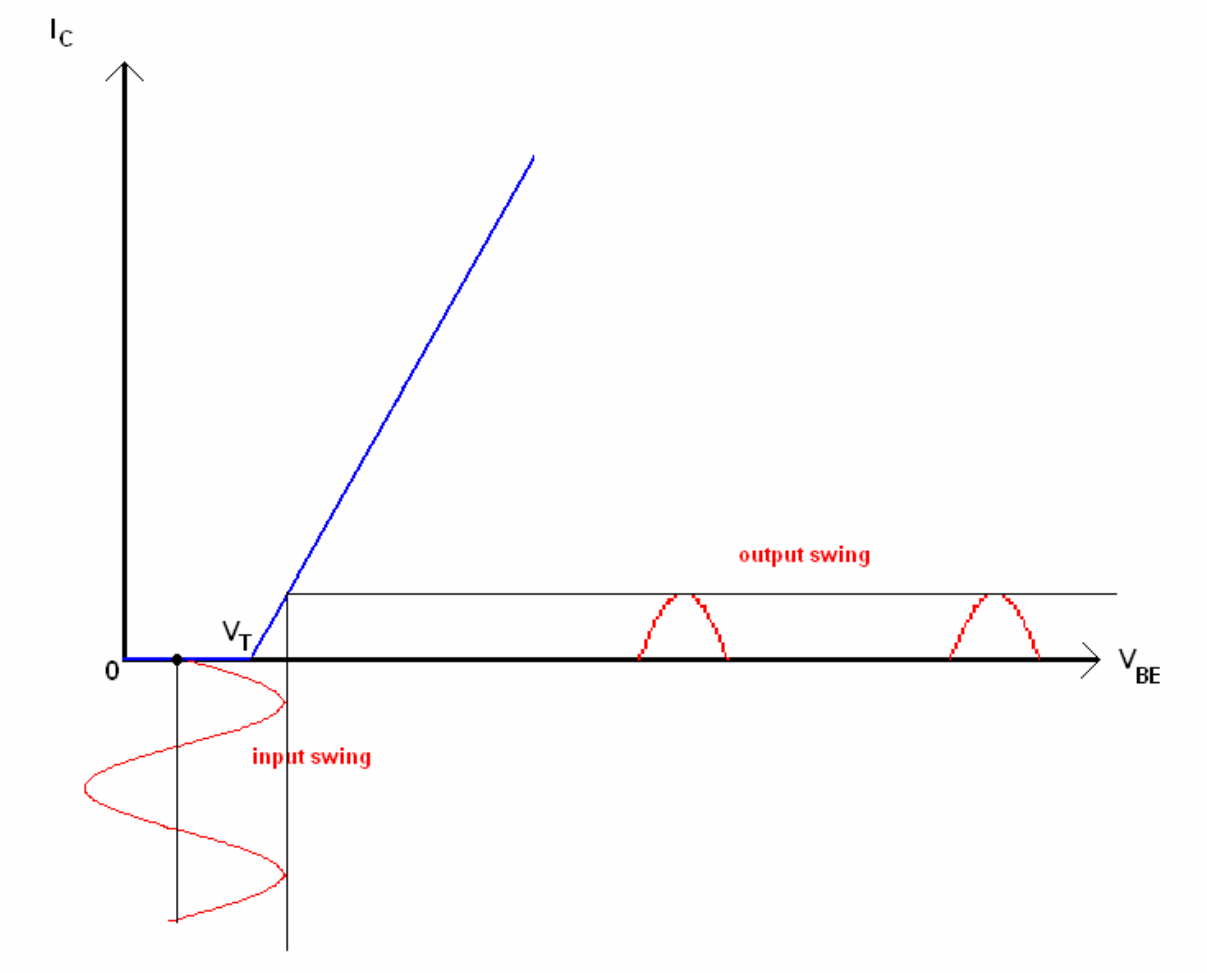

Fig. 2.13 Class C power amplifier Bias Point and input/output swings

The conduction angle of class C amplifiers is a function of input drive. The efficiency increases as the conduction angle decreases. The efficiency achieves 100% when conduction angle is zero. In other words, the efficiency is 100% when the amplifier generates no RF power.

The main drawback of the class C power amplifier is the decease in power handling capability and the power gain. As the conduction angle drops below 180° the output power can be obtained from the transistor decreases because of the increased harmonic distortions. Also power gain starts to drop down as the conduction angle goes to 0 from 180. The approximate output power and efficiency curves with respect to conduction angle are plotted in Fig. 2.14.

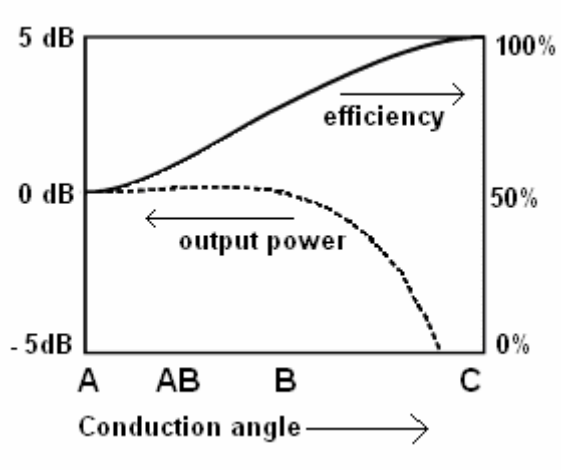

Fig. 2.14 Approximate output power and efficiency curves with respect to conduction angle

In class C amplifiers the fundamental component of the output current is no longer a linear function of the input drive. Therefore best used of Class C amplifiers are constant envelope modulation schemes, such as FM or filtered FSK [6].

2.2.5 Switching Mode Power Amplifiers

In switching mode amplifiers the transistor works as a switch which means that it is either in "on" state or "off" state. In the on state transistor acts as a short circuit. In the off state it acts as open circuit. Assuming the circuit exhibits ideal switching characteristics, voltage and current do not exists on the transistors simultaneously. Therefore, the theoretical peak efficiency of switching mode PA's are 100%. Therefore ideally the device operates at 100% efficiency. Analog changes in the input amplitude will disappear in the switching mode amplifiers as the device does not have analog states. Therefore switching mode amplifiers can be used in frequency modulation, pulse width modulation, Gaussian minimum shift keying modulation, as there is no information on the amplitude in these modulation schemes. The phase and zero crossing of the input are preserved in the switching mode amplifiers. Most common switching mode power amplifiers are class D and class E. As the transistors works as a switch in these topologies generally field effect transistors preferred.

2.25.5 a) Class D

In Fig 2.15 basic class D power amplifier topology is given. Complimentary transistors used as in inverter topology therefore the output would be 180° phase shifted version of the input. Assume that the input is at the voltage of V_{dd} initially. Therefore top switch acts as open circuit and bottom switch acts as short circuit and the output is zero. For the next half circle

the input instantly goes to zero so top switch is switched to short circuit and bottom switch acts as an open circuit.

The output waveform is shaped by the output band pass filter which is tuned to the input signal frequency. This causes the output current to be a continuous sinusoid at the input frequency.

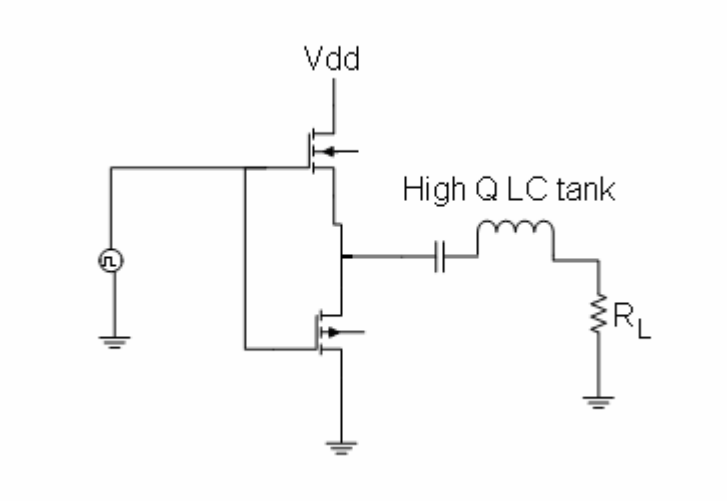

Fig. 2.15 Class D power amplifier topology

In practice, there are several sources of power dissipation that cause the Class D topology to have less than 100 % efficiency. Instant switching between the states could not be realized because of the output capacitances of the transistors. Finite switching time causes the efficiency to reduce. In addition, the transistors dissipate power since a finite resistance exists across its terminals during conduction, they can not act as an ideal short circuit [7].

2.2.5 b) CLASS E

In Fig. 2.16 schematic view of shunt capacitor class E power amplifier is given. The shunt capacitor configuration employs the transistors parasitic output capacitor as a part of output matching circuit. Therefore the parasitic effects caused by the transistors output capacitance decreased by this configuration.

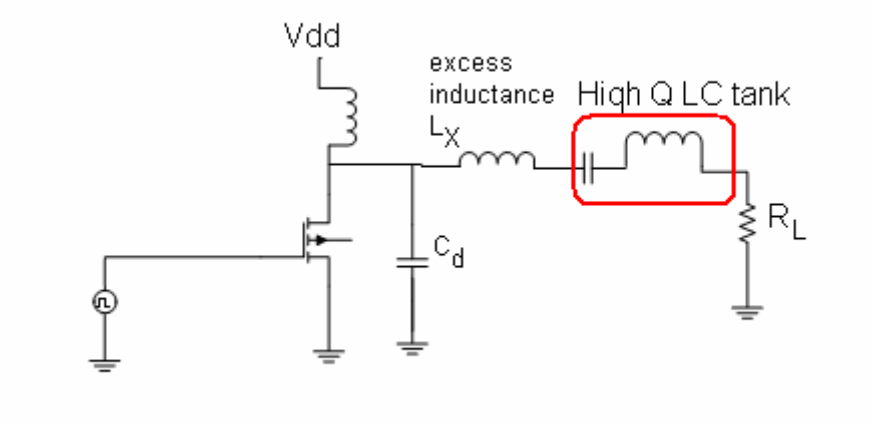

Fig. 2.16 Class E power amplifier topology

Unlike the Class D configuration, no power is lost due to the shunt capacitor in the ideal Class E power amplifier. Because, in the shunt capacitor Class E configuration, C_d provides an AC current path while the device is cut-of. The excess inductance is purposefully included in the output network to insure that C_d is completely discharged before the device begins conducting current [7].

Chapter 3

3. Power Amplifier Design Fundamentals

In this section general Power amplifier design fundamentals will be discussed. First the design road map for a RF power amplifier design will be introduced and design details will be explained in the subsections.

The design of a power amplifier starts with the device selection. Then the device area is determined by the power requirement. The IV curve of the transistor has a key importance in the PA design. The DC operating points can be determined by the IV curves. In addition, approximate load lines and linear output power can be determined by using the IV curves. Optimum input and output impedances are determined by using parametric simulations including load pull technique. The matching network designed by using optimum source and load impedance values. If the simulation results do not meet the requirements, the device area and impedance matching networks should be changed. After completing these states the layout phase of the design starts. According to the parasitic extraction due to layout, design should be modified. The final design should be achieved in an iterative manner. A simple road map for PA design can be given in Fig. 3.1

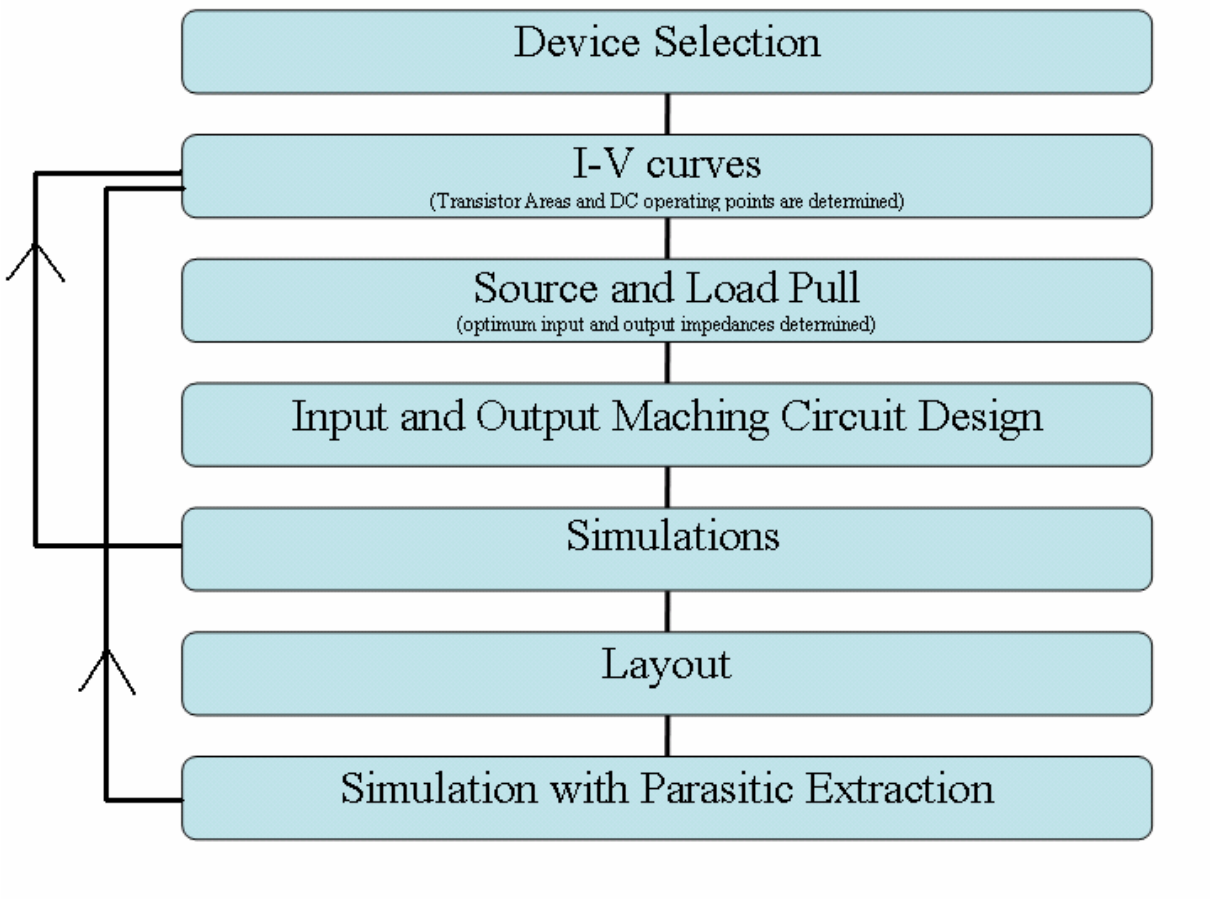

Fig. 3.1 Power Amplifier Design Road Map

3.1 Device Selection

In this thesis, the PA is designed by using AMS 0.35μm SiGe BiCMOS HBT technology. High voltage HBT transistors are used for the design. The transistors are symbolized as npn <2><5><4>h5 HBT and the numbers refer to the number of collector, base and emitter contacts, respectively. The transistor is preferred for the PA applications because of its high breakdown voltage and relatively high transition frequency.

3.2 Plotting the I-V characteristics

The next step for the PA design is plotting the I-V curves for the selected transistor. By this way the device area for the required power and the corresponding DC operating point can be determined. The base current (I_B) and collector voltage (V_C) is swept and collector voltage and current is plotted for determining the maximum linear output operation for the transistor. The schematic view for plotting the I-V curves is given in Fig.3.2. The emitter degeneration is applied with an inductor for increasing the linearity of the amplifier.

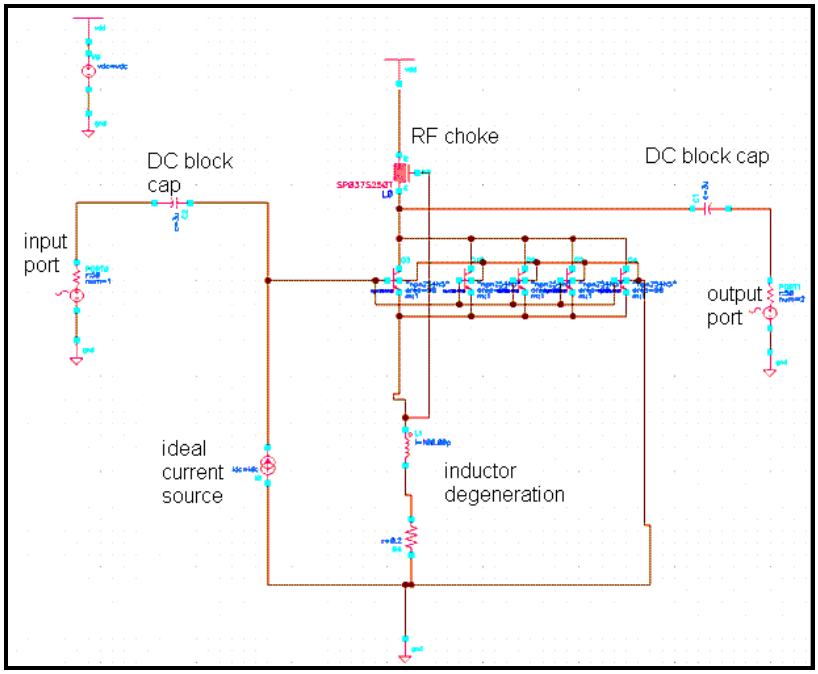

Fig. 3.2 Schematic View of the test setup for I-V curve simulations

A general I-V curve is given in Fig.3.3. We can determine the transistors maximum voltage and current swings by using I-V curves. The upper limit for the voltage swing is determined by the collector emitter breakdown voltage of the transistor. The breakdown voltage of the transistor is specified by the foundries. The selected transistor has a breakdown voltage of 6V. The lower limit of the voltage swing is the knee voltage. On the other hand, the output current swings between zero and the bias current.

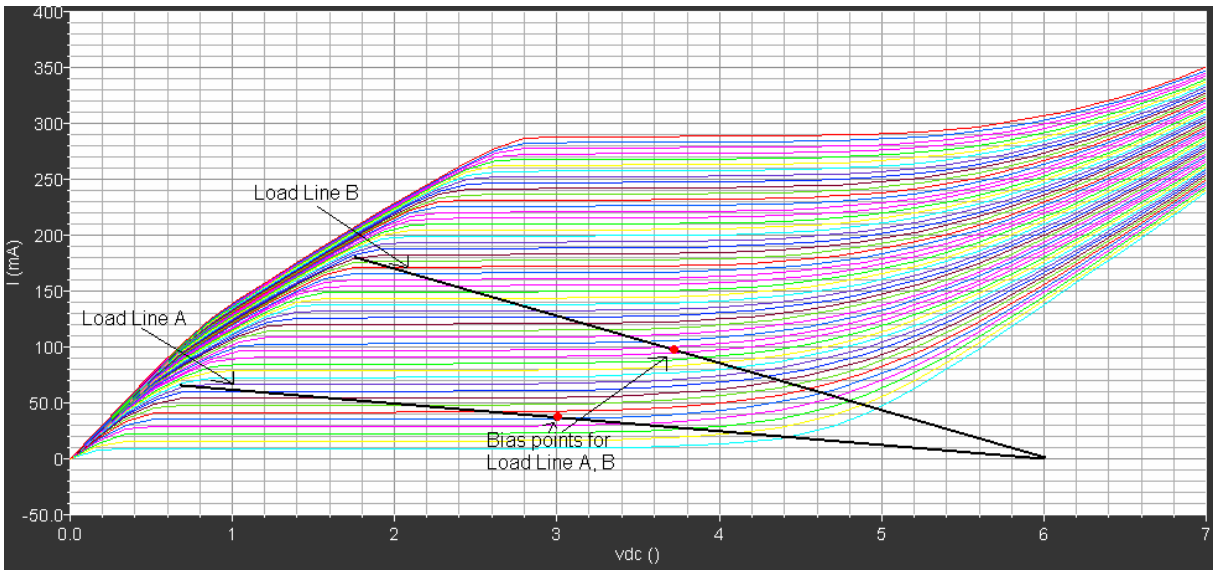

Fig. 3.3 Load Lines for a power amplifier on the IV curve

In Fig 3.3 two possible load lines are given for a fixed transistor size. Load line A symbolizes the low current operation whereas the load line B points out the high current density operation. Increasing the current density has a negative effect on the voltage swing as the knee voltage for the transistor increases in the high current region. Therefore the voltage swing decreases. The decrease in the voltage swing has a negative effect on the efficiency of the amplifier as the DC power consumption is linearly increasing with the bias current but the output RF power does not grow linearly because of the decrease in the voltage swing. The bias point for a power amplifier is very critical. The bias voltage of the amplifier should be the middle point of the knee voltage and threshold voltage. The bias current should be chosen as the maximum current level for the selected load line. The maximum current level is determined by using the maximum allowed current for the metal layers of the process and thermal considerations.

The collector current given in Fig 3.3 can be approximately scaled by the transistor area. Therefore increasing the transistor area increases the available current swing without degrading the efficiency. However increasing the transistor size, adding more transistors in parallel, reduces the impedance levels so that matching the input/output of the transistor impedances to 50 Ω becomes challenging. The difficulty in matching will also limit the power obtained for a given technology.

3.3 Load Pull Technique

Input and output matching is very important for an RF amplifier design. The method of obtaining the optimum source and load impedance for a transistor changes from application to application. The optimum source and load impedances for a given transistor are different for maximum gain and maximum power cases. For obtaining the highest gain, the source and load impedances should be the complex conjugate of the input and output impedances of the transistor. However in power amplifier design the transistor should be "power matched" for maximum available power and efficiency, resulting in reduced gain. Maximum power and gain can not be obtained simultaneously for a given transistor. In Fig. 3.4 the input power versus output power is plotted for the same transistor for small-signal gain match and power match cases.

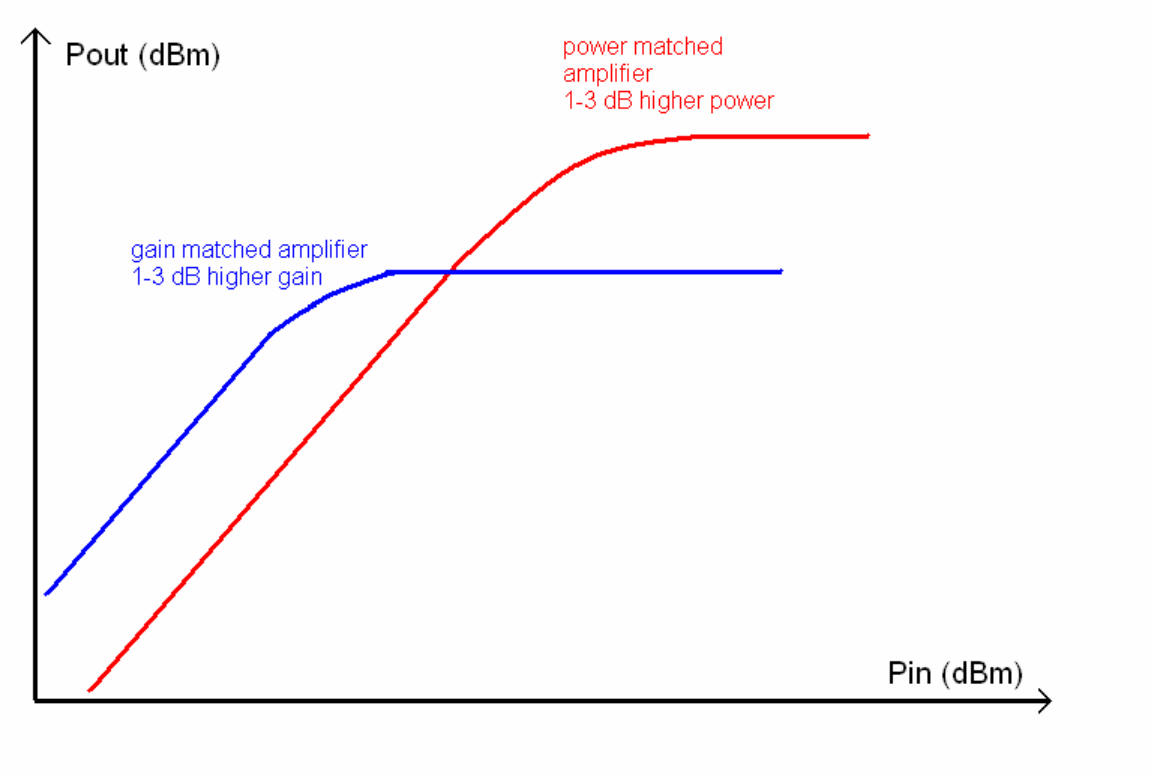

Fig. 3.4 Output Power-Input Power curves for power matched and gain matched cases

Choosing the proper load impedance is very important for obtaining the highest available power for a given transistor. The load resistor can be optimized for maximum power after the transistor area and bias point determined. The optimum load should be a resistor for the internal transistor satisfying the maximum voltage and current swing at the same time.[mavi kitap]. Therefore the load resistor can be given as:

$$R_L = \frac{V_{\max} - V_{\min}}{I_{\max}} \qquad (3.1)$$

The effect of load impedance is shown in Fig 3.5 in the I-V curve of the transistor. All of the load lines for the different load impedances pass through the bias point. The bias point corresponds the zero crossing of the AC signal. Three different load resistances are given in Fig 3.5. The optimum load resistance satisfies the maximum voltage and current swing condition. For the condition the load resistances lower than the optimum load resistance the transistor could not achieve the maximum voltage swing as the current swing run out. On the other hand the load resistances greater than the optimum load resistance complete the current swing while using only a portion of the available voltage swing.

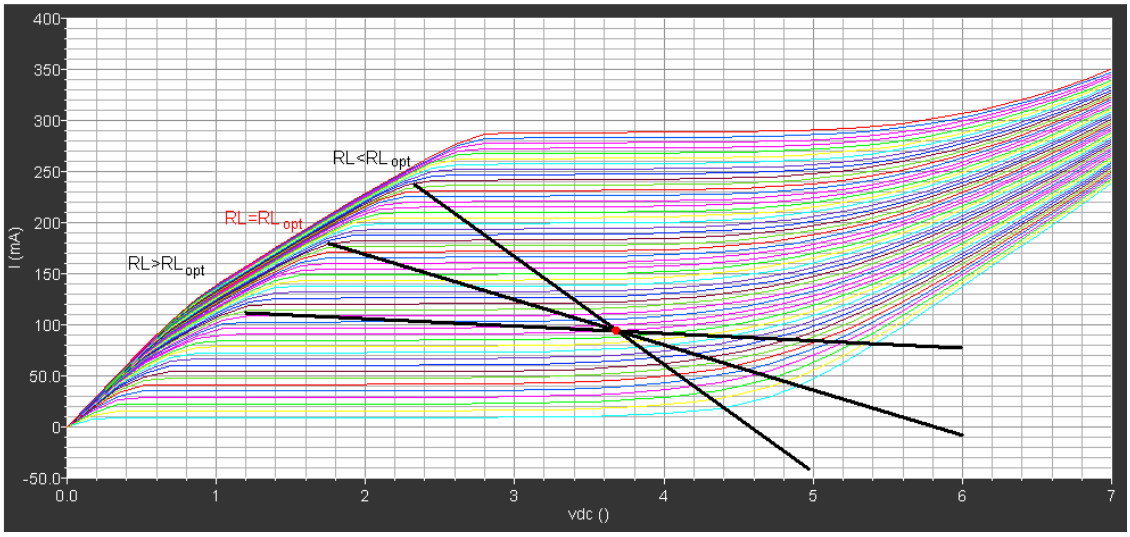

Fig 3.5 Optimum Load impedance shown on the IV curves

The device parasitic transforms the optimum load resistor (R_L) to optimum load impedance (Z_L). The optimum load impedance which gives the maximum power can be found by parametric simulations. For a given load impedance the output power can be calculated. (The load impedances yield the same output power contours in the Smith chart.) The power contour simulation results of the 5x96 μm^2 254h5 transistors are given in Fig. 3.6.

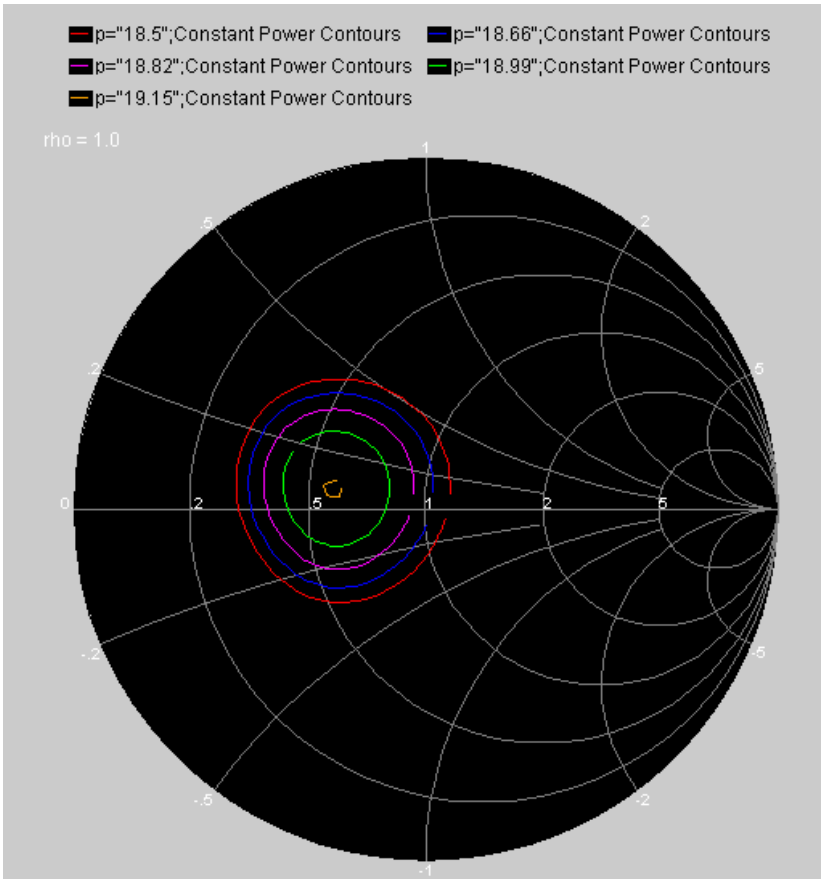

Fig 3.6 Power Contours for different Load impedances

3.4 Input and Output Matching Circuit design

In an RF system all the discrete components are designed for 50 Ω so there is no reflection between them. For this reason the input (Z_{in}) and the output (Z_{out}) impedance of the amplifier should be 50 Ω. Therefore the optimum load (Z_L) and source (Z_S) impedance obtained in the previous step should be transformed to 50 Ω. A power amplifier view is given in Fig. 3.7 showing optimum source and load impedances.

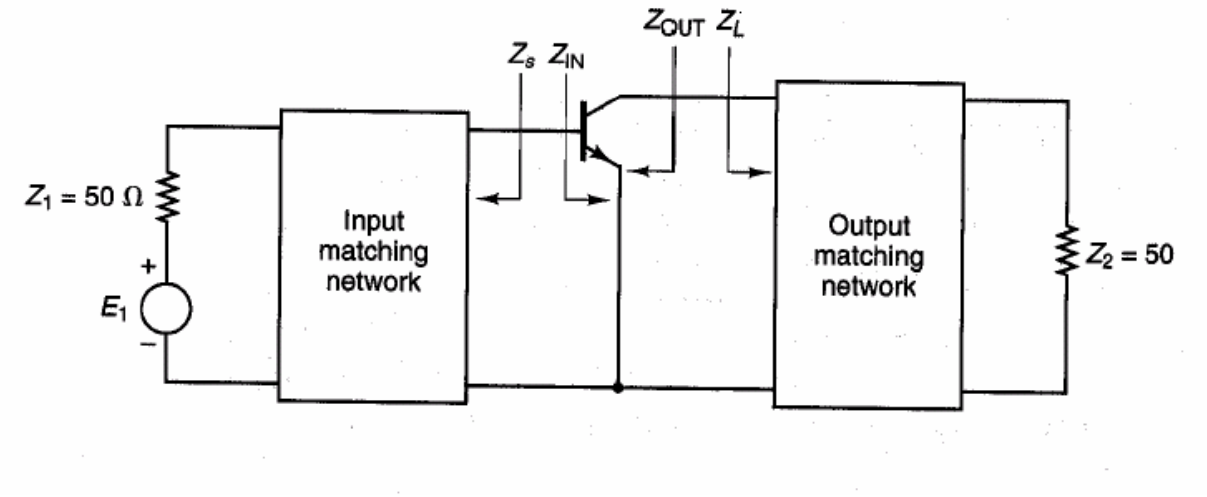

Fig. 3.7 An amplifier schematic showing Z_{in}, Z_{out}, Z_L and Z_S

In the RF systems generally distributed transmission lines are used for matching. But transmission lines can not implemented on-chip, due to size limitations below certain frequency of operation. The most common impedance matching method for on-chip matching is using L-type matching networks. The schematic of some L-type matching networks consisting of just an inductor and a capacitor is given in Fig. 3.8.

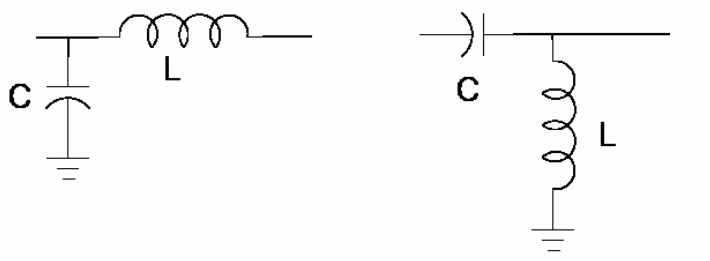

Fig. 3.8 Schematic view of L-type matching networks

The ideal L-type matching network can transform every impedance value to 50 Ω without loss. But considering the losses of the passive elements the insertion loss of the matching

network grows extensively with decreasing matched impedance. So, matching low impedances to 50 Ω causes extensive losses.

After the matching networks are designed the performance of the Power amplifier can be tested. The main parameter for defining the performance of a power amplifier is the 1 dB compression point, efficiency and gain. If these parameters meet the requirements the designer can go forward to the layout step. If these parameters do not meet the requirements the designer should go through the previous steps. The layout, simulation and measurement results for the combined power amplifier will be given in chapter 5.

Chapter 4

4. Power Combining Techniques

Designing high power devices at high frequencies is very challenging because of the trade off between high breakdown voltage and high mobility in solid-state devices. Various power combining techniques are developed over many years to overcome this restriction. However most of these techniques are circuit level combining techniques and can not be applied to chip-level combining [8]. In this section some of the widely used power combining techniques will be presented and their compatibility to chip-level combining will be discussed.

Chip level power combining techniques are required for high power single chip transmitter architectures. Chip-level power combining techniques offers size, cost and weight reduction and very high reproductivity, but suffers from increased losses due to low quality factor of integrated passives, especially inductors.

Usually, an impedance matching network is used to transform the 50Ω input/output impedance to lower equivalent source/load impedance seen by the PA (Fig.3.7). Because of the low supply voltage in silicon based technologies, the required load impedance could be extremely low when high power is required. Lower the value of load resistor (Z_L), the higher the output power. However, matching a lower value of Z_L to 50Ω will result in excessive losses in the matching network and it will degrade the overall efficiency of the amplifier. Some of the powers combining techniques have an impedance matching capability in addition to power combining. Usually these techniques offer less loss with respect to independent

designs of power combining and impedance matching circuits. In this manner the impedance matching capabilities of the power combining techniques will also be discussed.

Some of the most common power combining techniques can be classified as distributed amplifier, transformer based power combiners, spatial power combiners and Wilkinson power divider based power combiners.

Brief background information about these power combining techniques will be presented in the next subsection. In this thesis an improvement on the Wilkinson power divider architecture will be presented. For this reason Wilkinson power divider based power combining techniques will be emphasized more than other techniques. The proposed power combining technique will be presented in the Wilkinson power divider based power combining techniques subsection with the simulation and measurement results.

4.1 Distributed Amplifier Design

Distributed amplifiers can be considered as a power combining technique as many transistors are used in the design and output powers of these transistors added. A distributed amplifier consists of two transmission lines and multiple transistors providing gain through multiple signal paths. One of the transmission lines carries the input wave; the other carries the output wave. Transistors are placed between these transmission lines and supplies gain between input and output. Each transistor's output power adds in phase with the output wave so the output powers of the amplifiers are combined at the end of the transmission line. Transmission lines are terminated by resistors from one end to prevent reflections. General schematic representation of distributed amplifier topology is given in Fig. 4.1.

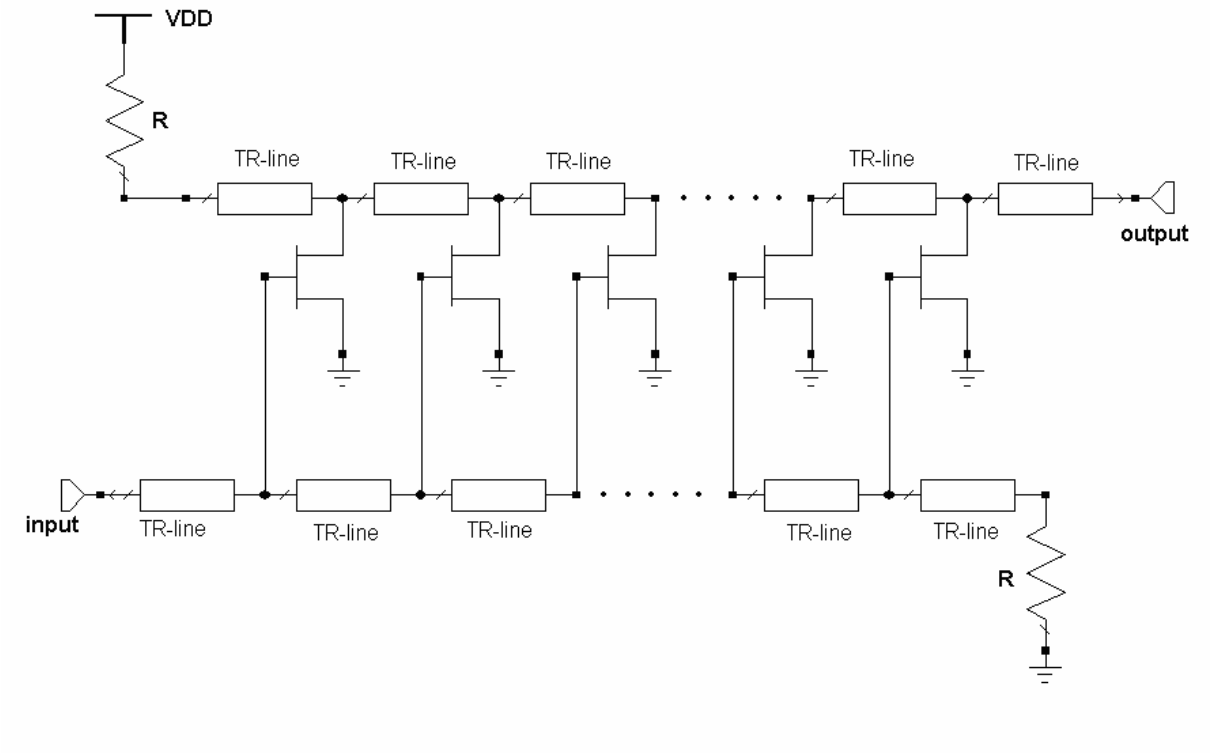

Fig 4.1 Schematic view of Distributed Amplifier Topology

FET based transistors are preferred for this topology for their high input impedance. FET device will not load the input transmission line. The distributed amplifier topology can be modified by using distributed transmission lines. The artificial transmission lines consist of series inductance and shunt capacitance can act like actual transmission lines. By this way parasitic gate and drain capacitances of the FET device taken into account for better frequency response. Using transistors parasitic capacitances as a transmission line, the frequency limitations of FET device can be avoided. The distribute amplifier idea is proposed for circuit level combining. But the idea can be applied for chip level combining, as the integration became the major motivation for the RF industry.

The main advantage of this technique is not achieving high power but increasing the bandwidth [9]. In [11], 12.5 dBm output power at 1 dB compression point is obtained in the 2-25 GHz frequency bandwidth. Both the transmission line [10], [11] and artificial transmission line [9] versions of this technique are applied for building single chip broad-band amplifiers.

4.2 Transformer Based Power Combining Techniques

Transformer is a well known impedance matching element. For the ideal transformer the impedance matching ratio is $1/N^2$ where N is the ratio of number of windings in each side of the coil namely primary and secondary coil. On-chip transformers can be realized by placing metal layers on top of each others. Therefore, signal will couple the adjacent metal layer. On-chip transformers can be used for power combining by driving one of the coils with more than one amplifier. Different on-chip transformer topologies developed for accomplishing power combining and impedance matching duty at the same time[12-15]. In Fig 4.2 general principle of power combining transformer is described.

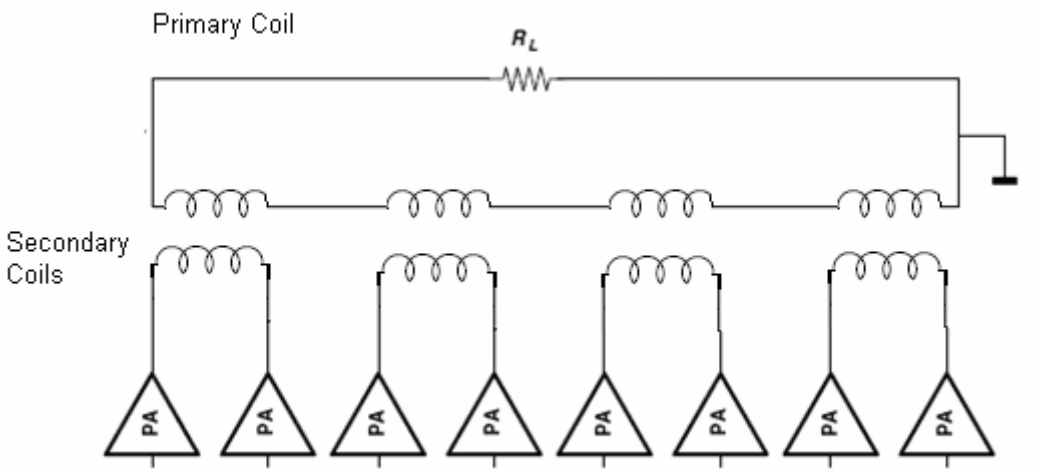

Fig. 4.2 Transformer Based power combining topology

For impedance matching, primary coil of the transformer should be more than one winding. However, increasing the number of windings to satisfy the matching condition increases the insertion losses dramatically.

In [13] this technique is applied for 5.8 GHz WLAN applications and 20.5 dBm output power is obtained at 1dB compression point with a drain efficiency of 15%.

Power combining transformers can be used for on-chip power combining and impedance matching at the same time but low resistivity substrate degrade the performance of the amplifier greatly [13].1

4.3 Spatial Power Combining Techniques

In this technique the output power of several solid state circuits are combined in free-space as opposed to in a lossy substrate. In this approach, the output of each amplifier is connected to an antenna [16]. Antennas are placed to form an array configuration so that the radiated power is added in a specific direction. This technique was first demonstrated in [17] by using

100 element array. General representation of the spatial power combining technique is given in Fig.4.3.

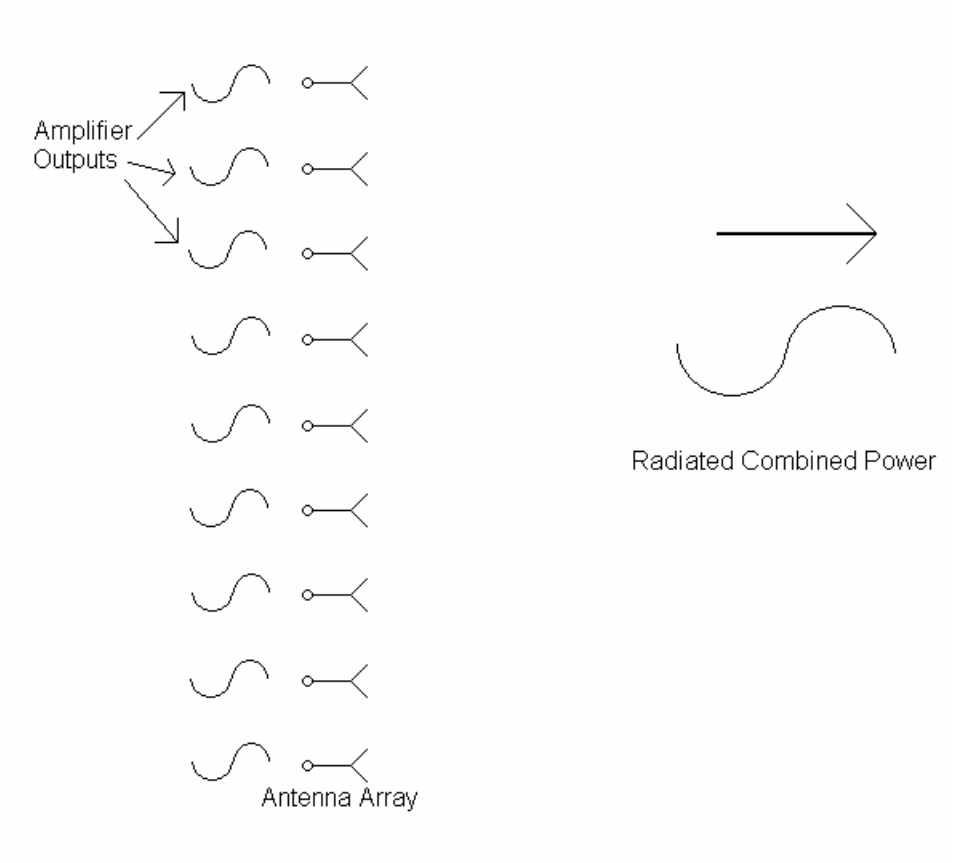

Fig. 4.3 General Representation of Spatial Power Combining Technique

The efficiency of spatial combiners are not effected by the number of combined devices. Therefore, larger number of elements can be combined efficiently by using this technique. The elements can be fed by using circuit level splitting techniques or spatially by using another antenna. This combining technique is not approperate for chip level combining for WLAN frequencies because of the extensive chip area of the antenna arrays.

4.4 Wilkinson Power Divider Based Power Combining

The Wilkinson power divider was invented in 1960's. In this early topology, quarter wave transmission lines and a resistor used to match 3 ports in a lossless manner as shown in Fig. 4.4.

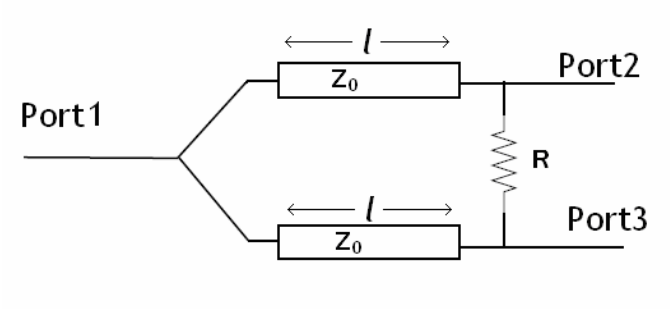

Fig. 4.4. A transmission line two-way Wilkinson power combiner

Wilkinson power dividers are generally designed for all three ports are matched to the same impedance. As all the ports have the same impedance values (Z_1) the design parameters for the transmission line of the Wilkinson Power divider is:

$$Z_0 = \sqrt{2}Z_1 \quad (4.1)$$

$$l = \lambda / 4 \quad (4.2)$$

And

$$R=2\ Z_1 \quad (4.3)$$

for the isolation resistor.

Wilkinson power divider circuit can be analyzed by using even and odd mode excitation method [18]. This method allows us to use symmetry in the 3 port device and decrease the effort to analyze. The Wilkinson power divider given in Fig. 4.4 can be depicted in a symmetrical manner including the port impedances as given in Fig. 4.5. The network given in Fig. 4.5 is drawn symmetric to the mid-plane.

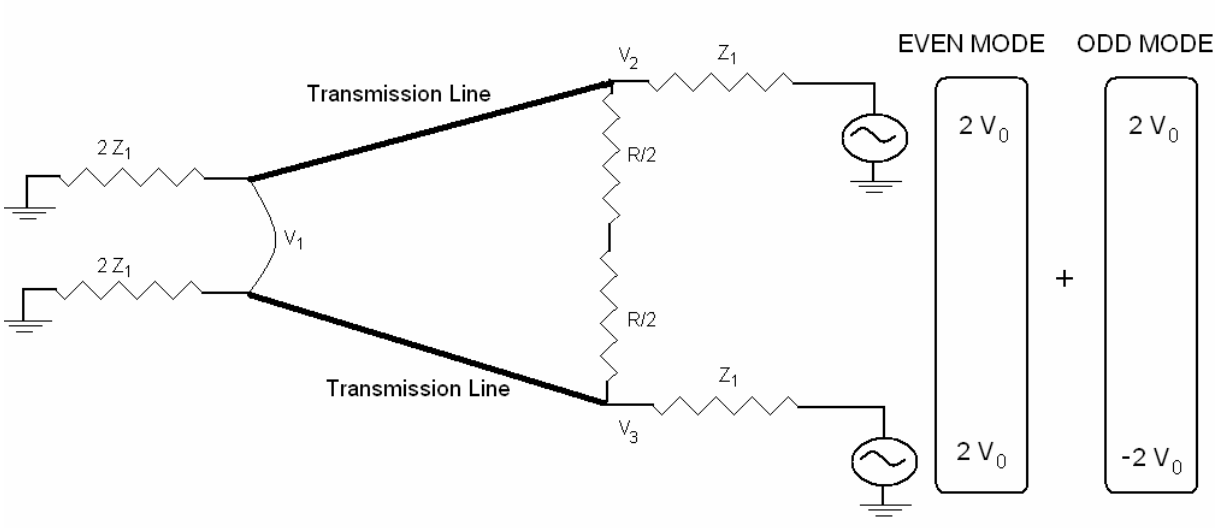

Fig 4.5 Wilkinson Power Divider in symmetric form

For the even mode excitation Ports 2 and 3 are excited by a voltage 2 V0. As the impedances of the port 2 and 3 are the same there is no current flow through the R/2 resistors due to symmetry with respect to mid plane. Therefore the network in Fig. 4.5 can be analyzed as two symmetric half circuits given in Fig. 4.6.

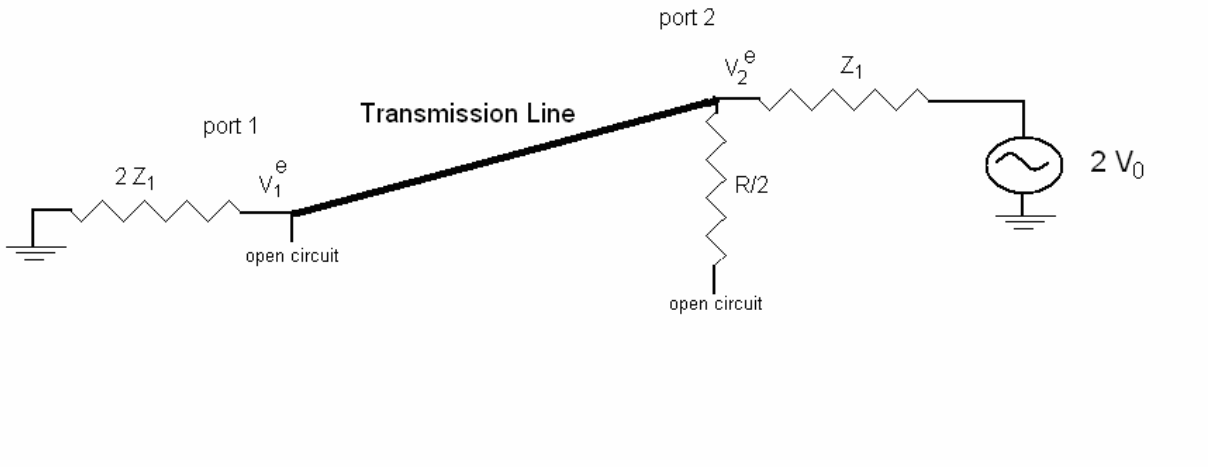

Fig. 4.6 Even Mode half circuit representation for the Wilkinson Power Divider

In Fig. 4.6 the input impedance of the port 2 can be found by using λ/4 transformation:

$$Z_{in2}^{e} = \frac{Z_0^2}{2Z_1}, \qquad (4.4)$$

Therefore if Z0=$\sqrt{2}Z_1$,

Z_{in2}^{e} can be calculated as Z_1 from Equation 4.1.

Therefore, the Port 2 is matched for the even mode excitation.

The V_1^e in Fig.5 can be found by using the voltage on transmission line as:

$$V_2^e = V_0 \qquad (4.5)$$

$$V_1^e = -jV_0\sqrt{2} \qquad (4.6)$$

For the odd mode excitation, Ports 2 is excited with 2 V0 and Port 3 is excited with – 2V0 therefore there is a voltage null across the mid plane of the circuit given Fig. 4.5. We can use the half circuit method by grounding the mid plane for the odd mode excitation. The half circuit for the odd mode excitation is given in Fig. 4.7.

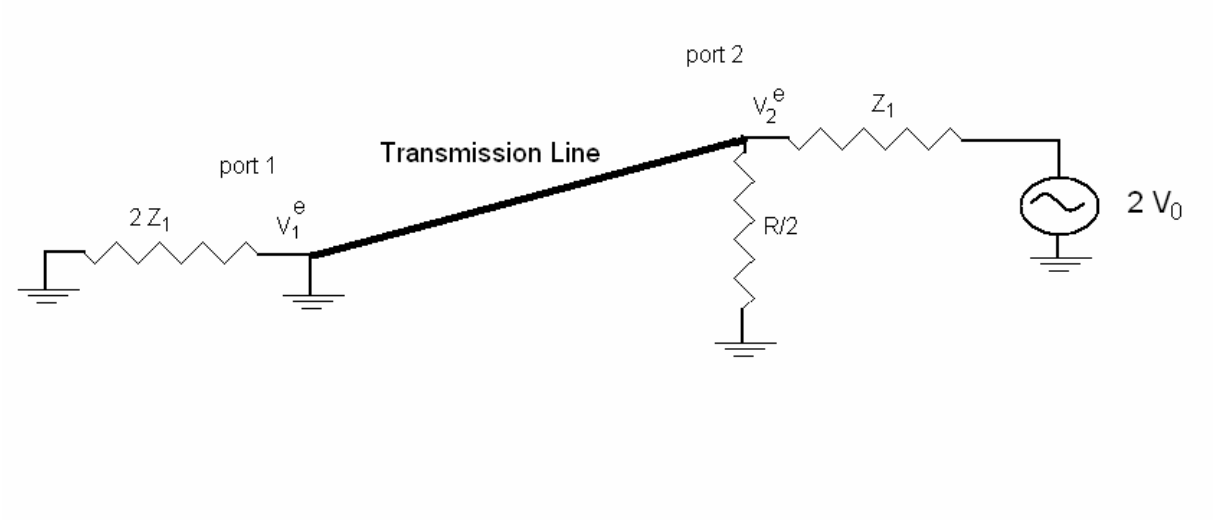

Fig. 4.7 Odd Mode half circuit representation for the Wilkinson Power Divider

The input impedance seen from port 2 is the parallel of the impedance seen from the transmission line and R/2 resistor. As the λ/4 transmission line is grounded at one end the impedance seen from port 2 is infinity and overall input impedance of the port 2 is R/2. Therefore, choosing R=2* Z1 satisfies the matching condition for the port 2 in the odd mode excitation. Then V_2^o and V_1^o can be calculated as:

$$V_2^o = V_0\,, \tag{4.7}$$

$$V_1^o = 0 \tag{4.8}$$

With these even-odd mode method we can calculate

$$S_{22} = S_{33} = 0 \tag{4.9}$$

because port 2 and 3 are matched for both even and odd mode excitation and

$$S_{21} = S_{12} = \frac{V_1^e + V_1^o}{V_2^e + V_2^o} = \frac{-j}{\sqrt{2}} \tag{4.10}$$

$S_{31} = S_{13}$ would be equal to $S_{21} = S_{12}$ due to symmetry of Port 2 and Port 3.

And

$$S_{32} = S_{23} = 0 \tag{4.11}$$

Because the mid plane of the network is grounded for the odd mode excitation and open circuit for the even mode excitation.

For determining the input impedance of the Port 1, a signal should applied to that port. As Ports 2 and 3 are symmetric, no current flows on the isolation resistor. The simplified schematic of the network for this condition is given in Fig. 4.8.

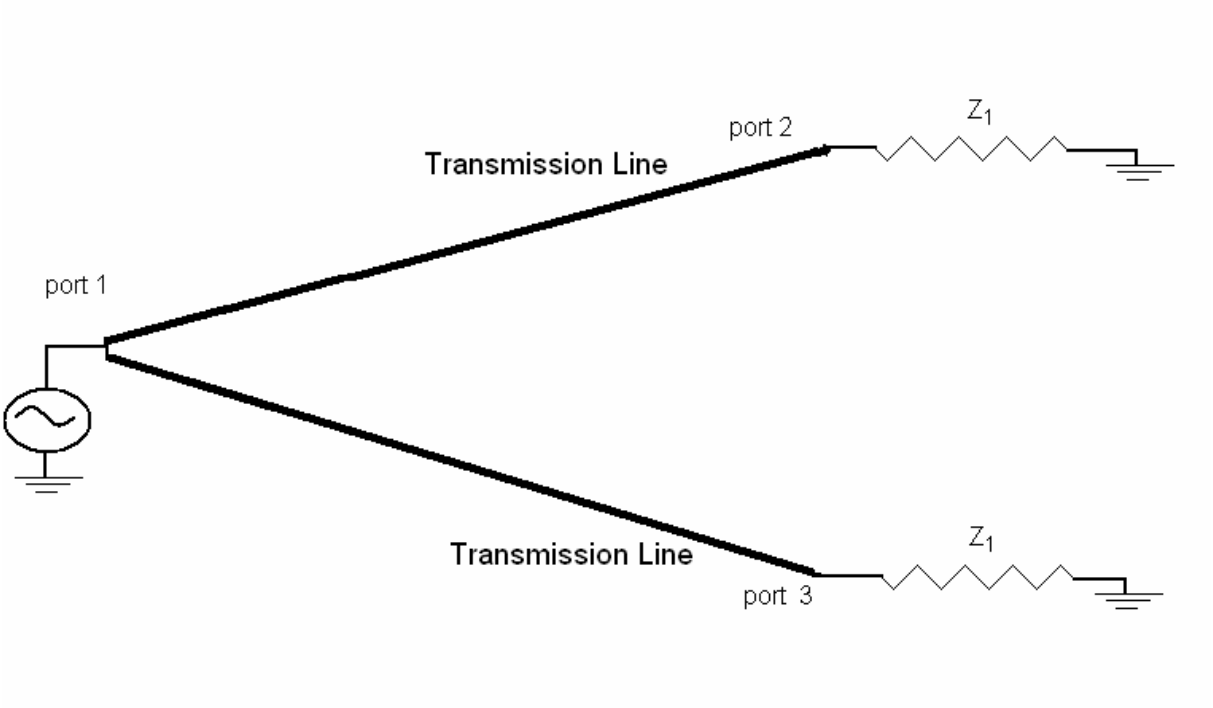

Fig. 4.8 Representation of Wilkinson Power Divider with port 1 excitation

As the Ports 2 and 3 are terminated with matched loads (Z_1) the input impedance of the Port 1 can be calculated as the parallel of the impedances seen from the transmission line.

As the Z_0 of the λ/4 transmission line is $\sqrt{Z_1}$:

$$Z_{in1} = \frac{(\sqrt{2}Z_1)^2}{2} = Z_1 \qquad (4.12)$$

Therefore Port 1 is also matched and the S-parameters of the Wilkinson Power divider are calculated as follows:

$$S = \frac{-j}{\sqrt{2}} \begin{vmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{vmatrix} \qquad (4.13)$$

The Wilkinson power dividers are used for power combining over many years in the RF industry. The schematic view of power combining circuit by using Wilkinson power divider is given in Fig. 4.9.

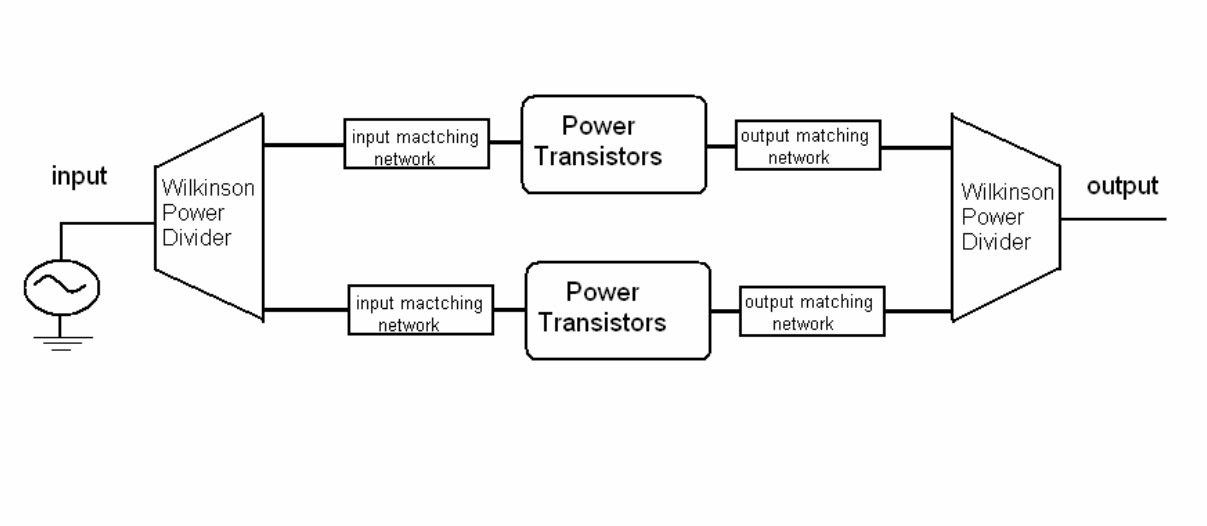

Fig . 4.9 Conventional Power combining schematic by Using Wilkinson power dividers

In common power combining method, the dividers are built that all of its ports are matched to 50 Ω. Therefore, input and output matching circuits are needed to match power transistors input and output impedance to 50 Ω. The power combining method generally used for circuit level combining by using distributed transmission line elements. However in [19] the idea is applied for on-chip combining at 24 GHz by using on-chip transmission line elements. The proposed power combining method is an improvement of the conventional Wilkinson power divider based power combining method. The proposed power combining method by using impedance matching Wilkinson power dividers are mentioned in the next subsection.

4.4.1 Proposed Power Combining Technique by Using Impedance Mathcing Wilkinson Power Dividers

The novel idea in this thesis is designing the Wilkinson power divider not for 50 Ω but for the input and output impedances of the power transistors. Therefore the input and output matching circuits can be eliminated. The overall schematic of the proposed power combining technique is given in Fig. 4.10.

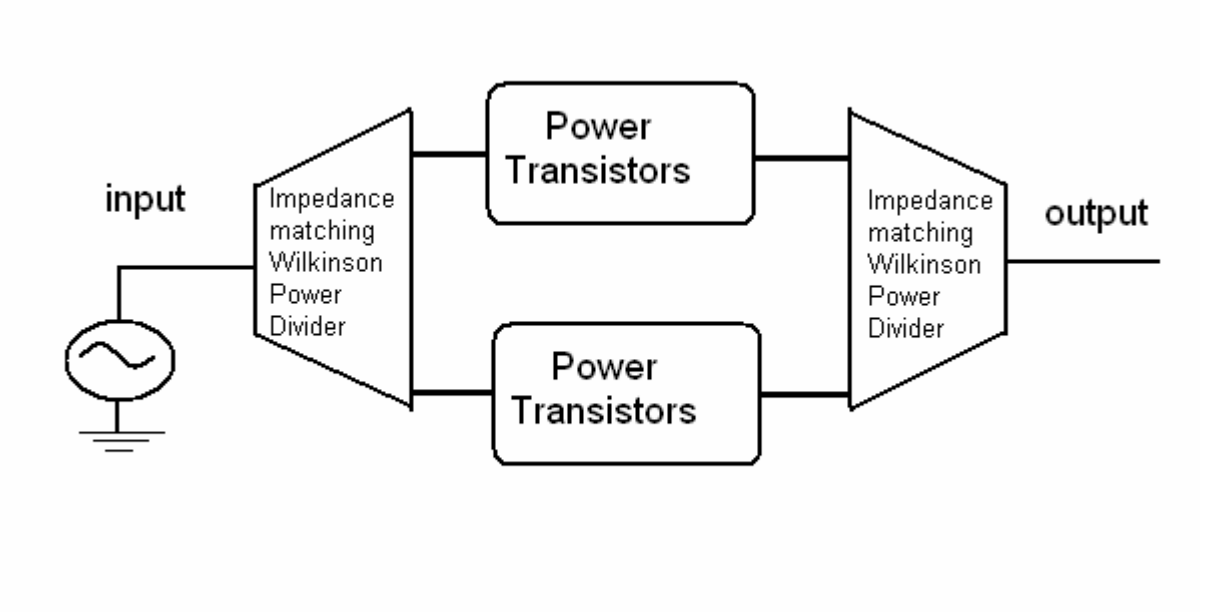

Fig. 4.10 Proposed Power Combining Technique using Impedance Matching Wilkinson Power Dividers

Eliminating the input and output matching circuits decreases the matching losses therefore higher gain and higher power can be achieved with respect to conventional power combining method. In addition, the area of the circuit is reduced by eliminating the matching circuits and replacing conventional 50 Ω matched Wilkinson power divider with approximately the same sized impedance matching Wilkinson power dividers.

4.4.2 Impedance Matching Wilkinson Power Divider Design

The analyses of Wilkinson power divider given in chapter "4.3 Wilkinson Power divider based power combining" can be extended by choosing the impedances of Port 2 and 3 differ from Port 1(common port). As the impedances of the Port 2 and 3 are still the same even-odd mode analyses is also valid for this situation.

Assume that Port 1 is terminated with impedance Z_1, and Ports 2 and 3 are terminated with impedance Z_2 where Z_1 and Z_2 are purely resistive (Fig. 4.4). For perfect match condition at all ports, the following equations should be satisfied.

$$\begin{aligned} l &= \lambda / 4 \\ Z_0 &= \sqrt{2Z_1 Z_2} \\ R &= 2Z_2 \end{aligned} \qquad (4.14)$$

The characteristic impedance for the λ/4 transformer of the impedance matching Wilkinson power divider is now $Z_0 = \sqrt{2Z_1Z_2}$ to match 2 Z_1 to Z_2. Therefore the matching conditions for the even mode excitation (Fig. 4.6) and common port excitation (Fig. 4.8) are satisfied. Choosing the value of the isolation resistor as $2Z_2$ satisfies the matching condition for the odd mode excitation (Fig.4.7) so the same S parameters (Equation 4.13) can be obtained for the different impedance case.

The design equation given in (4.14) is an extension for the Wilkinson power divider design and the author does not meet this extension in any other published book or paper. As the new design equations allow us to choose different impedances for port 1 and the ports 2 and 3 the Wilkinson power divider can also be used for impedance matching duty. Therefore, it can be called "impedance matching Wilkinson power divider".

This extension has also the restriction of choosing the impedances of Port 2 and 3 the same as in the common Wilkinson power divider. This restriction does not limit the usage of the Wilkinson power dividers for the combined power amplifier application. Because the port impedances of Port 2 and Port 3 should be the same as the transistor blocks connected to these ports are identical.

A quarter-wavelength transformer can be easily realized on PCB's by using distributed transmission line structures for microwave frequencies. However, for frequencies below 10 GHz, transmission line structures become too long to be placed in a reasonably small-sized chip. The designs can be miniaturized by using lumped element equivalent circuits [20], [21]. In this way the lumped element Wilkinson dividers can be realized in standard CMOS technology and 1.4 dB insertion loss is already reported at 24 GHz [22]. The lumped equivalent of the circuit in Fig. 4.4 is given in Fig. 4.11 where the transmission lines are replaced by a π-network of L-C elements.

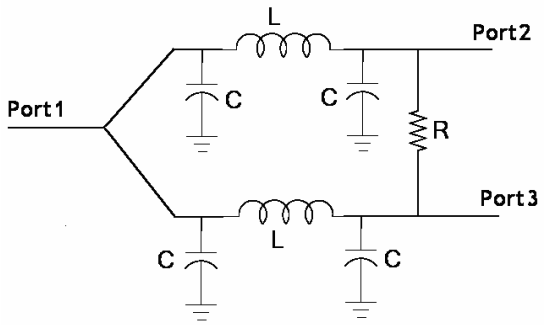

Fig. 4.11 π-network lumped equivalent two-way Wilkinson power divider

The values of inductance L and capacitance C are given by

$$L = \frac{Z_0}{2\pi f}$$

$$C = \frac{1}{2\pi f Z_0} \qquad (4.15)$$

The π-network accomplishes the 90° phase shift and matching duty at the same time but suffers from high insertion loss when realized with low quality factor inductors which are generally less than 15 in silicon based technologies. On the other hand, the L-type matching network offers better insertion loss but does not satisfy the 90° phase shift; so degraded isolation is expected by the L-network realization. The π-type and L-type matching networks are designed to match $2Z_1$ to Z_2 (Port 1 to Ports 2 and 3); therefore, very low return loss is obtained at all three ports of impedance matching Wilkinson power divider circuits.

In our case, Z_1 is 50 Ω, so matching networks should match 100 Ω ($2Z_1$) to the desired impedance levels at the Ports 2 and 3. The insertion loss of the impedance matching Wilkinson power divider directly relates with the insertion loss of matching networks. The insertion loss and phase shift for π-type and L-type matching networks are studied as a function of their inductor unloaded quality factor and the desired impedance levels at Ports 2 and 3. As the quality factors of the on-chip capacitors are significantly higher than the inductors, their losses are not considered here. The insertion loss of π-type and L-type matching network with respect to matched impedance is given in Fig.4.12.

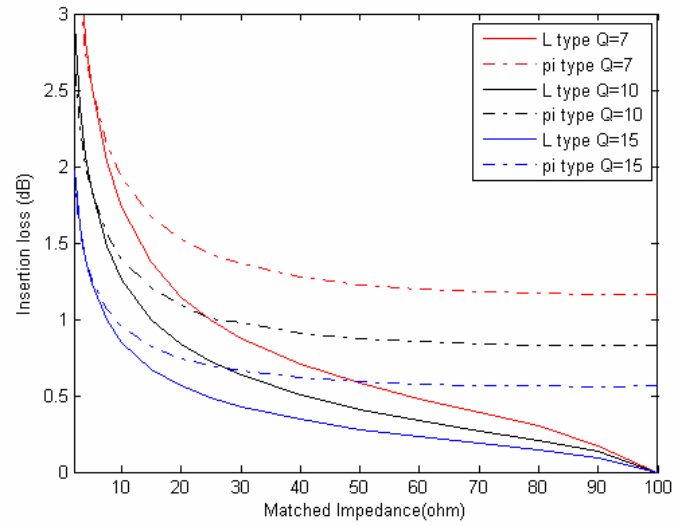

Fig. 4.12 Insertion loss for π-type and L-type matching networks for various quality factors

Fig. 4.12 shows that the insertion loss for L-type network is smaller than pi-type network for the simulated values of impedances ranging between 2-100 Ω. For the higher matched impedances, difference between the two matching networks increases.

The π-type matching network offers a 90° phase shift which is needed for the isolation between Port 2 and Port 3. On the other hand, L-type matching network does not exactly satisfy this 90° phase shift condition. The phase difference for the L-type matching network which is designed to match 100 Ω to different impedances is plotted in Fig. 4.13.

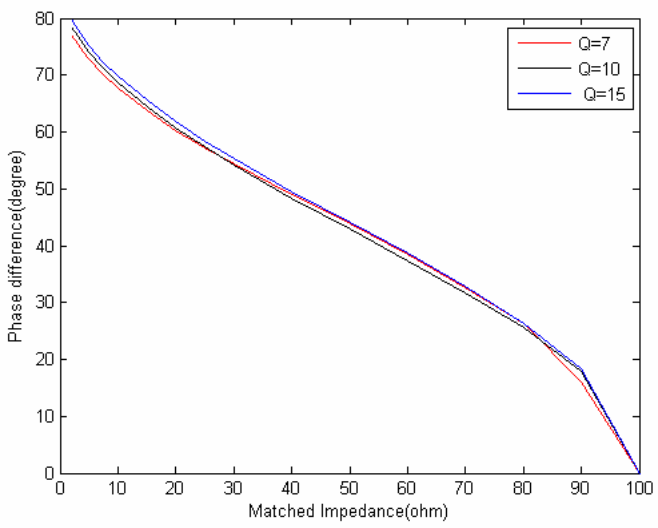

Fig. 4.13 Phase difference for L-type matching network for various quality factor inductors

The desired 90° phase shift can be obtained in high matching ratios; for example, while matching 100 Ω to few ohms. However, this condition will not be satisfied if the matching impedance level increases. If the matched impedance level is 100 Ω, L and C values of the L-type network become zero, so both the insertion loss and phase shift is zero.

For the combined power amplifier application, insertion loss of the combiner is more important than the isolation performance; so impedance matching Wilkinson power divider circuits are realized by using L-type matching networks. It should be noted that by using L-type matching networks, the restriction of choosing Z_1 and Z_2 purely resistive is cancelled out. The schematic view of proposed L-network lumped element impedance matching Wilkinson power divider circuit is given in Fig. 4.14.

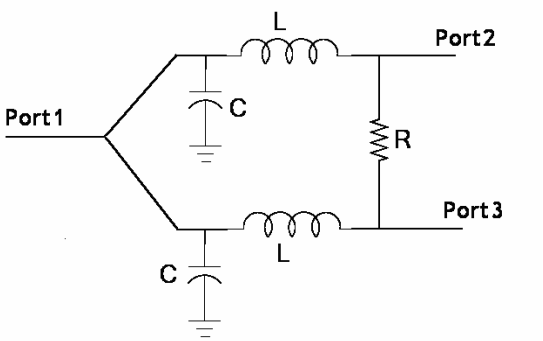

Fig. 4.14 L-network lumped element impedance matching Wilkinson power divider circuit

Two impedance matching Wilkinson power divider circuits are designed for the combined power amplifier application. One of these circuits is used as a splitter and the other circuit is used as combiner. Impedance matching Wilkinson power dividers are designed and optimized in SpectreRF Cadence programs. The splitter is designed so that Port 1 matches 50 Ω and ports 2 and 3 match input impedances of the power amplifier, 9.5+ j3.5 Ω at 5.2 GHz (see Fig. 4.14). The design of the splitter results in values of L = 0.9 nH, 2C = 1.9 pF (including pads and trace capacitances) and R=18.6Ω (Fig. 4.14). DC block capacitances are used before ports 2 and 3 for DC isolation of the base terminals of the amplifiers. The combiner is designed such that Port 1 matches 50 Ω and ports 2 and 3 are matches the optimum output load impedance of the amplifier, 28.5-j3 Ω. The design results in L=1.4 nH, 2C=0.9 pF and R=57 Ω (Fig. 4.14). DC block capacitances are used before Port1 for the combiner. The layouts of splitter/combiner are designed such that two amplifiers with on-chip RF choke inductors can be placed in between these circuits. The layout of impedance matching Wilkinson power divider used as splitter/combiner is given in Fig. 4.15a and b.

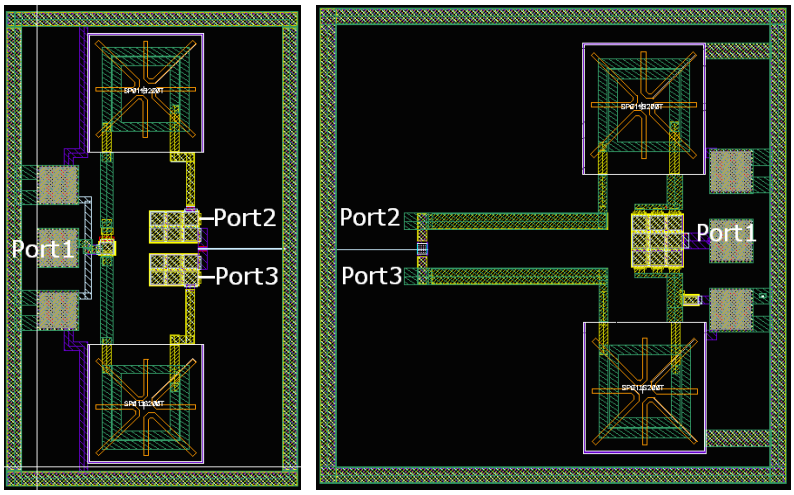

Fig. 4.15. Layout of impedance matching Wilkinson power dividers used as a) Splitter (left) b) Combiner (right)

The post layout simulation results for the splitter are shown in Fig. 4.16. Port1 is terminated with 50Ω and Port2 and Port3 are terminated with 9.5+j3.5Ω for this simulation.

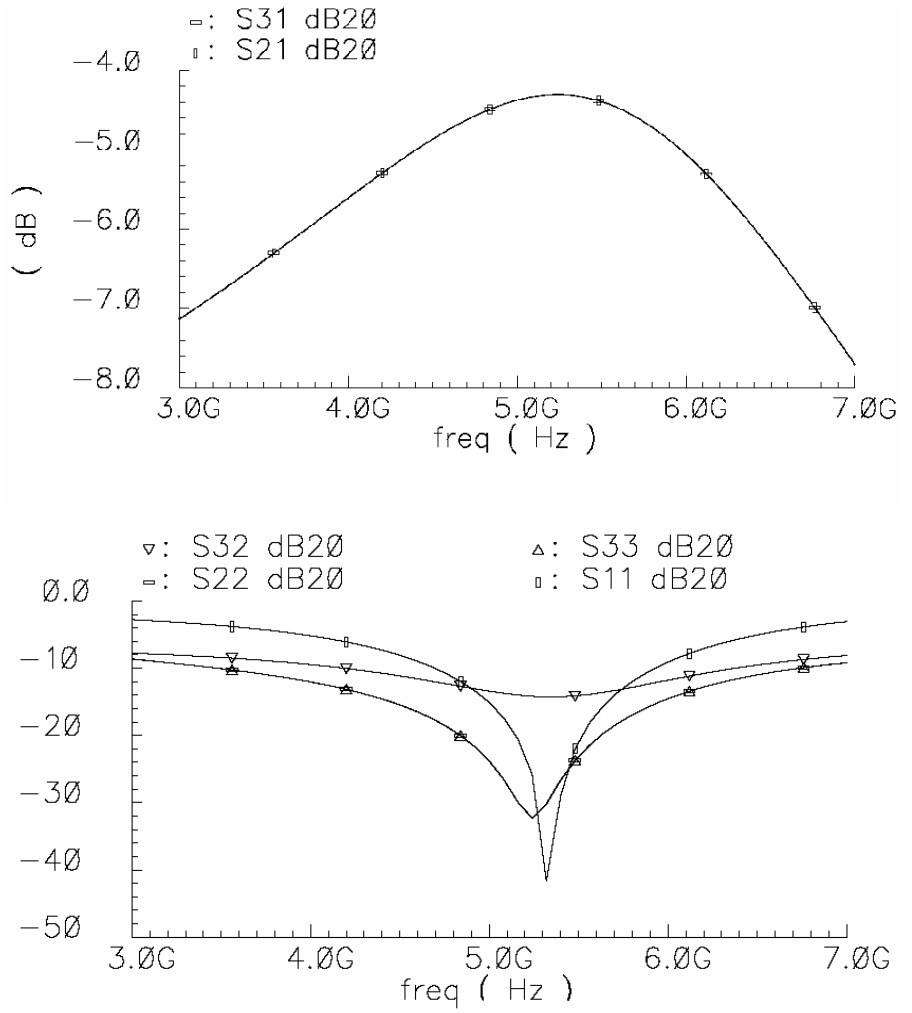

Fig.4.16. S-Parameter Simulation Results for impedance matching Wilkinson power dividers used as Splitter

Insertion loss of 1.4 dB is achieved at 5.2 GHz with all ports matched to the desired impedances (S11, S22, S33< -20dB) and good isolation (S23<-14 dB) is obtained as shown in Fig. 4.16. Low source impedances needed by the amplifier stage degrade the insertion loss performance of the splitter. The post layout simulation results for the combiner are given in Fig. 4.17. Port1 is terminated with 50 Ω; ports 2 and 3 are terminated with 28.5-j3 Ω for the simulation of the output impedance of the amplifier obtained from load-pull analysis.

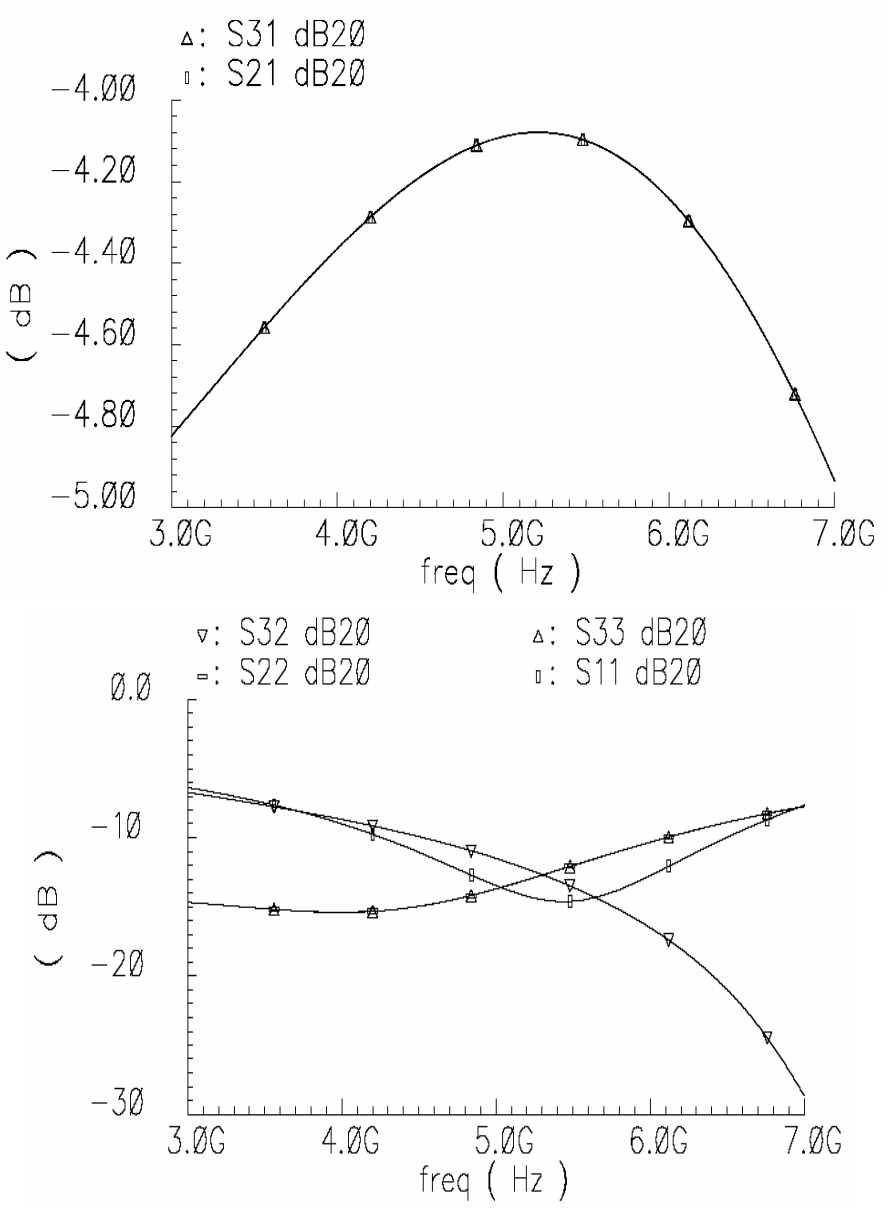

Fig.4.17 S-Parameter Simulation Results of impedance matching Wilkinson power dividers used as Combiner

An insertion loss of 1.1 dB is achieved at 5.2 GHz with all ports matched to the desired impedances (S11, S22, S33 <-13dB) and reasonable isolation level (S23<-12 dB) is also obtained as shown in Fig.4.17. The S21 and S31 curves are very flat with respect to the splitter case because the impedance matching ratio for the combiner is lower than the splitter.

For measurement purposes, Port 2 of the splitter/combiner is internally terminated with the port impedances of 9.5+j3.5 Ω (9.5 Ω resistor, 100 pH inductor) for the splitter and 28.5-j3 Ω (28.5 Ω resistor, 10pF capacitor) for the combiner. Additional pads are placed for

Port 3 of the combiner/splitter. The microphotograph of the fabricated splitter and combiner are given in Fig. 4.18.a, b respectively.

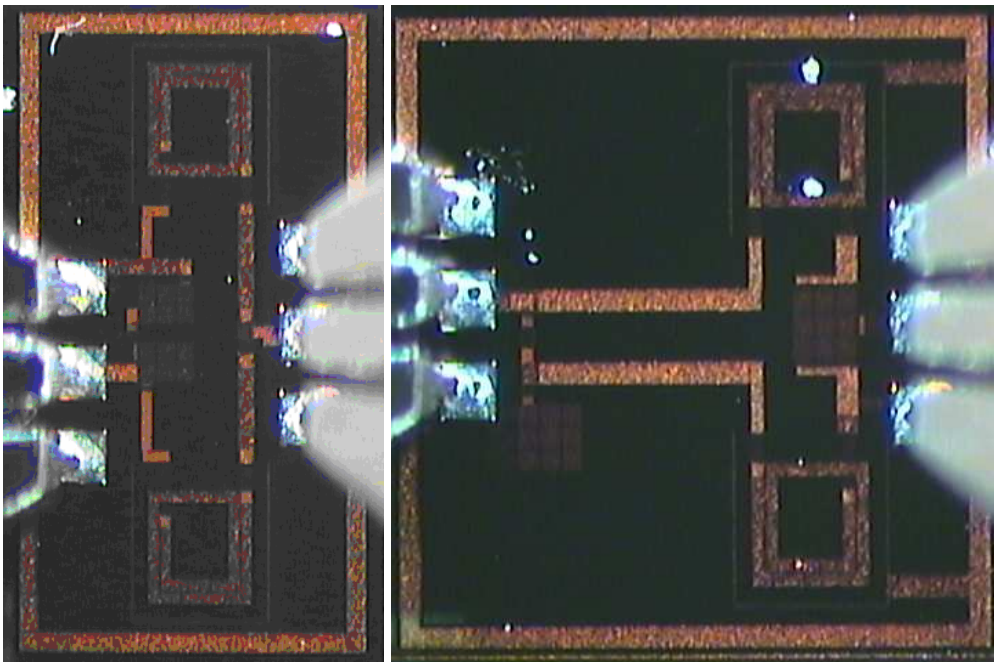

Fig. 4.18 Microphotograph. of a) Splitter (left) b) Combiner (right)

4.4.3 Experimental Results For Impedance Matching Wilkinson Power Divider

The measurements are done using Agilent 8720ES Network Analyser with a 50 Ω measurement setup. The SOLT calibration is done with the calibration kit and port extension calibration is applied for the proper measurement of the input impedance. The reference plane is defined as the pads of the measured port. The effects of the pads are not de-embedded during the calibration. The S-parameter measurements of the splitter are given in Fig. 4.19 in comparison to post layout simulation results with 50 Ω measurement system.

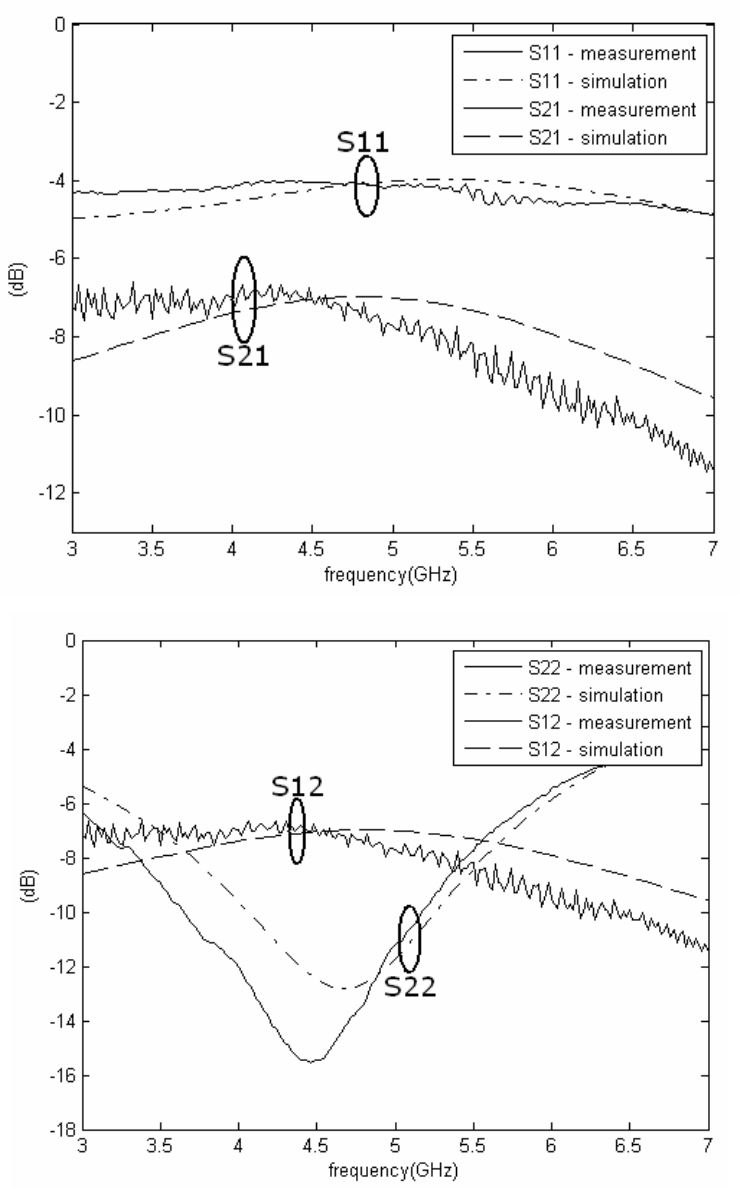

Fig. 4.19 Measured and Simulated S-Parameters of the Splitter with 50 Ω measurement setup

Around 5 GHz, measured results are in-line with the simulated results. The measurement results seemed to be shifted to the lower frequencies which could be caused by the extra capacitances of the pads added for measurement purposes. Note that S11 which is the return loss for Port 3 in Fig. 4.19 is approximately -4.5 dB. This should not be considered as a bad return loss since this circuit is meant to be used with a low impedance amplifier. The measured S21 and S12's are very close to the post-layout simulated curves which show that the circuit does not demonstrate additional loss other than simulations.

As Port1 and Port2 are terminated with optimum port impedances (50 Ω and 9.5+j3.5 Ω), the input impedance of Port 3 shows the impedance matching performance of the splitter. The measured and simulated input impedance from Port 3 of splitter is given in Fig. 4.20.

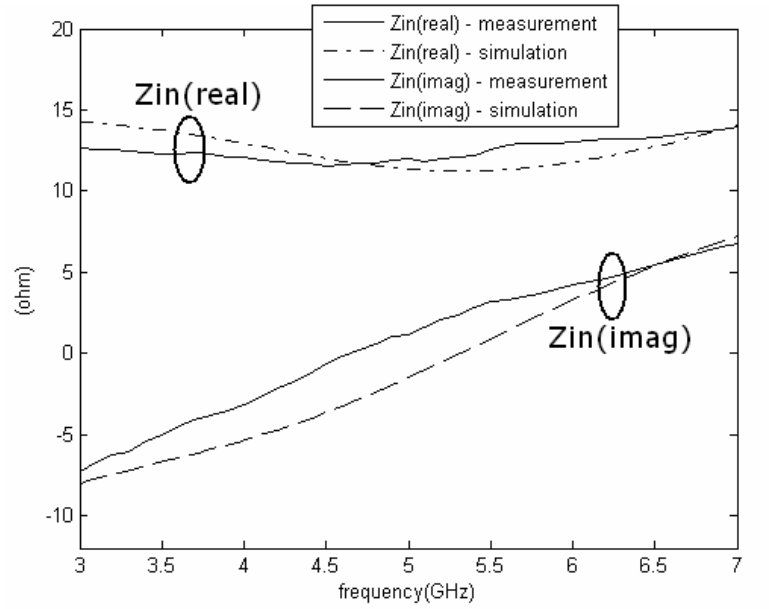

Fig. 4.20 Measured input impedance seen from Port3 of splitter

The measured input impedance of Port 3 of the splitter is in close agreement with simulations. Note that this measurement result does not show the exact input impedance of the splitter given in Fig. 4.20 because of the added pads for measurement purposes. The input impedance is measured as 12+j2 Ω at 5.2 GHz which is close to (9.5+j3.5)* Ω.

The S-parameter measurement results of the combiner are given in Fig. 4.21 compared with post-layout simulation results with the 50 Ω measurement system. The measurement results seem to be slightly shifted to the lower frequencies; as in the splitter case. The measured S21 and S12's are very close to simulated curves up to 4.5 GHz. Hence, it can be assumed that the circuit does not demonstrate additional loss other than the components considered in simulations. The measured and simulated input impedance seen from Port 3 of combiner is given in Fig. 4.22.

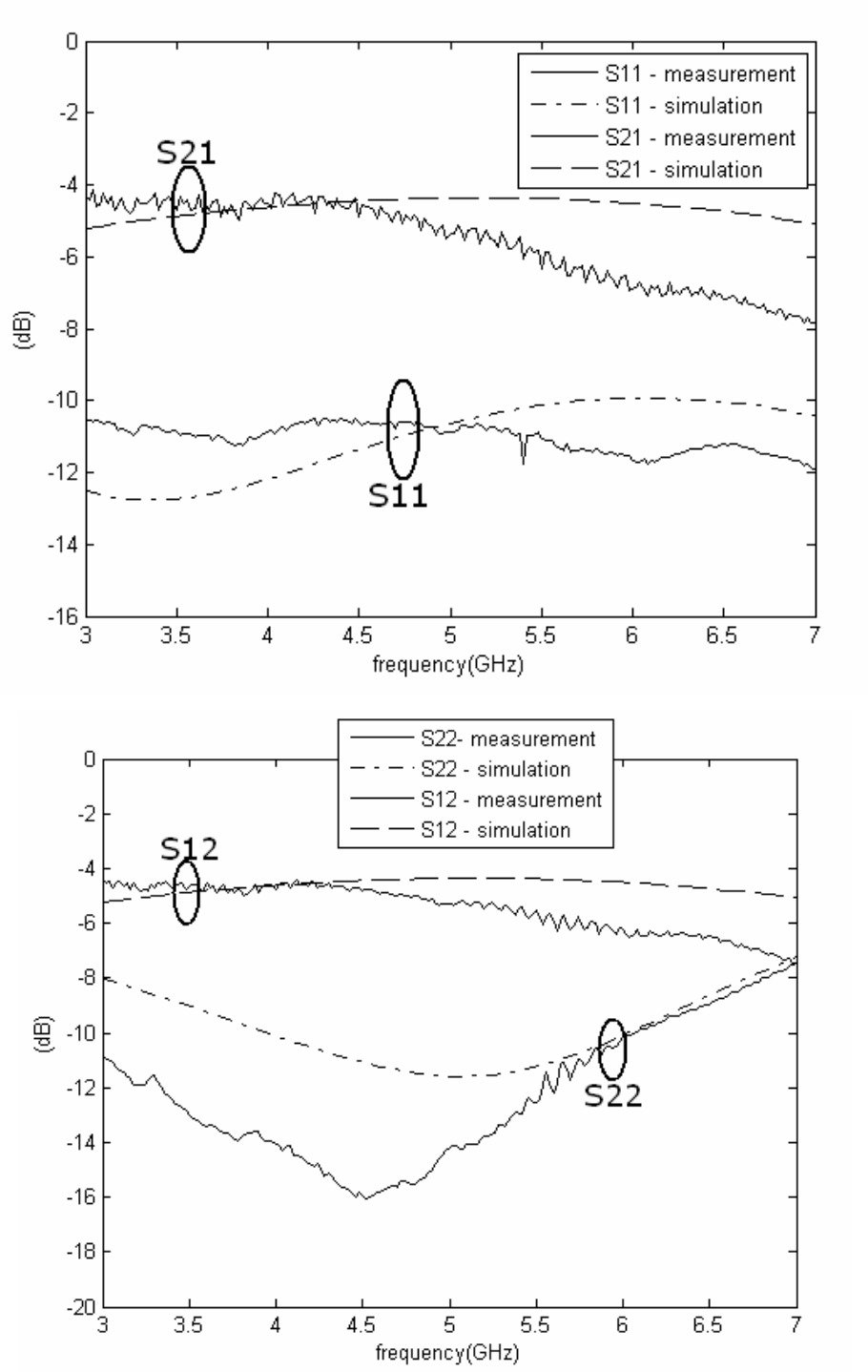

Fig. 4.21 Measured and Simulated S-Parameter Results of Combiner with 50Ω measurement setup

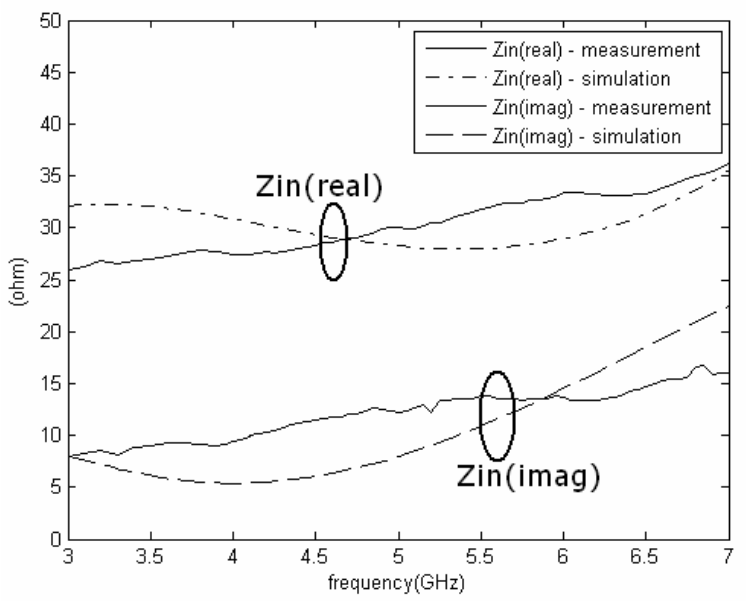

Fig. 4.22 Measured input impedance seen from Port3 of combiner

The measured input impedance of Port 3 of combiner is in-line with simulations. Although the pads are added for measurement purposes, the input impedance of combiner is measured as 31+j13 Ω at 5.2 GHz; which is close to (28.5-j3)* Ω.

The power gain/loss of a two port network excluding the reflection losses can be calculated by the following equation

$$G = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \qquad (4.15)$$

where Sij are the scattering parameters of the two port network. The gain excluding the reflection losses is very meaningful as the circuit is measured with 50 Ω measurement setup. For ideal equal split of the RF signal (two-way Wilkinson power divider with ideal transmission lines), the insertion loss is 3 dB between the input and the output ports. This can be regarded as splitting loss. However, if the elements are lossy, the insertion loss will be higher. The measured loss of the splitter/combiner are calculated by (4.15) and plotted in Fig. 4.23 and Fig. 4.24 respectively in comparison with lossy (layout extracted) simulated results and lossless (with ideal components) simulated results.

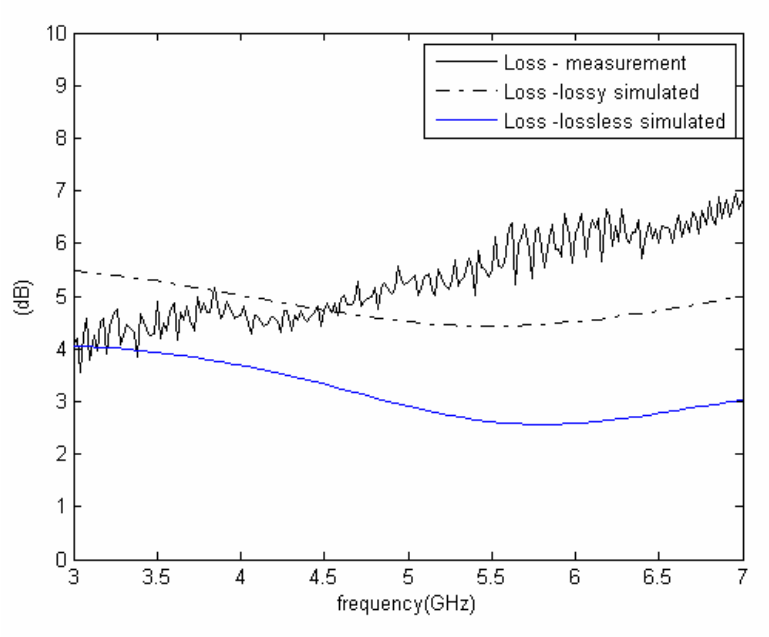

Fig. 4.23 Measured loss of Splitter

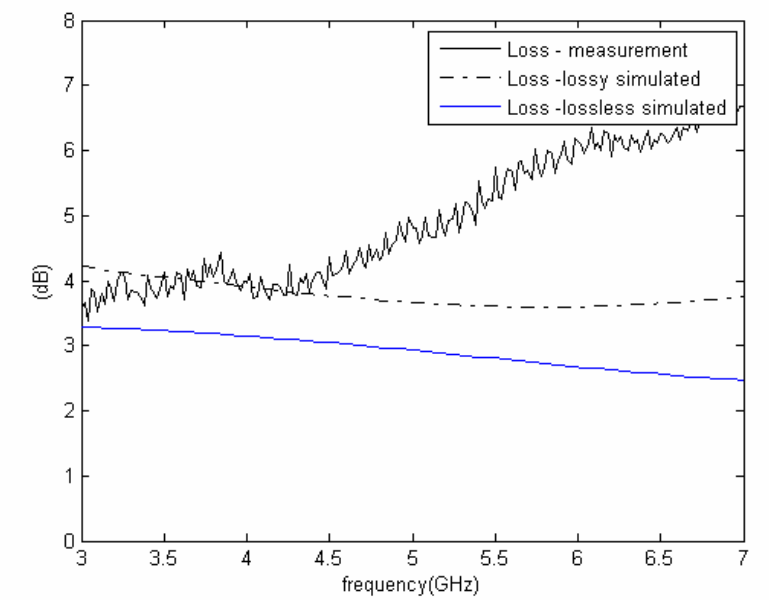

Fig. 4.24 Measured loss of Combiner

Measured results are in-line with the simulated results for both combiner and splitter up to 4.5 GHz. The measurement results seemed to be shifted to the lower frequencies which could be caused by the extra capacitances of the pads added for measurement purposes. Note that additional loss introduced by the splitter and combiner is around 2 dB and 1.5 dB respectively at 5 GHz with respect to the equal split two-way Wilkinson power divider. The total insertion loss for an isolated design of a splitter and combiner circuits and the matching circuits for the amplifier will be higher than the losses measured in this thesis.

Chapter 5

5. Combined Power Amplifier Design

For the design of 5.2 GHz single stage Class A power amplifier, 0.35 μm SiGe BiCMOS technology is used. Five of the 96μm^2 transistors are connected parallel to one another for the amplification which gives 480 μm^2 total size. First, the bias voltage and current values are chosen to satisfy the maximum linear operation due to stringent linearity requirements for higher order modulation schemes. Bias voltage and currents are chosen as 3.3V and 105mA respectively. Optimum source and load impedances are then obtained by parametric analysis, which include the load pull technique. Optimum source impedance satisfies the conjugate match condition, (9.5- j3.5) Ω; and optimum load impedance is obtained from load pull simulations (the available highest power) which is (28.5 + j3) Ω.

To increase the output power, a greater number of transistors can be connected in parallel. However, this will reduce the impedance levels so that matching the input/output of the transistor impedances to 50 ohm becomes challenging. The difficulty in matching will also limit the power obtained for a given technology. To further increase the output power, therefore, combining techniques can be applied. In this study, on-chip lumped element Wilkinson power splitter/divider is investigated for combined power amplifier applications.
Output power of two groups of 5x96μm2 SiGe HBT blocks are combined by Wilkinson power splitter/divider which are matched to the transistor's source and load impedances respectively so that no additional impedance matching is needed. The individual designs of impedance matching Wilkinson power dividers are presented in chapter 4. In this chapter the performance of the combined power amplifier will be examined.

The splitter, two RF power amplifiers and the combiner are connected as shown in Fig 5.1 to obtain higher power. Note that the splitter and combiner circuits contain DC block capacitors for proper RF operation of the power amplifiers. The input signal is fed to the splitter which has two outputs that are matched to the power amplifiers. After amplification, the signals are combined at the power combiner to produce higher power.

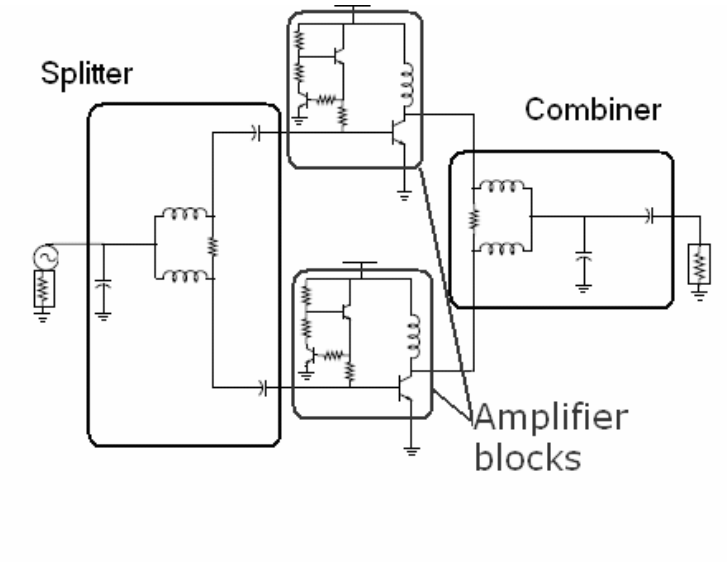

Fig. 5.1 Schematic view of the combined power amplifier

The microphotograph of the proposed combined PA with on-chip combiner and splitter is given in Fig. 5.2. The combined power amplifier includes 3 DC pads for each of the power amplifier block (total 6) and input/output RF pads. Total die size is 1.25mm x 1.2mm including DC and RF pads. Note that using lumped element design significantly reduces the chip area. The transmission line equivalent of the Wilkinson power dividers would occupy approximately 10 mm die size for each.

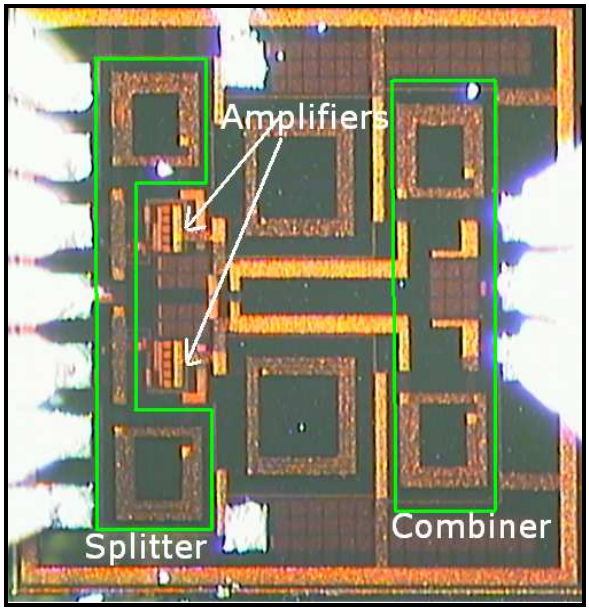

Fig.5.2. Microphotograph of the fabricated PA with on-chip combining circuits

5.1 Comparison with Single Stage Power Amplifier

In this subsection the performance of the power combining technique will be discussed by comparing the performance of single amplifier block and combined power amplifier. The design of single amplifier block is mentioned in chapter 3. The amplifier block used for single PA is identical with the amplifier block used in the combined PA. Therefore the effect of combining technique can be obtained. Single amplifier block's optimum source and load impedances are (9.5- j3.5) Ω and (28.5 + j3) Ω which was discussed in detail in chapter 3. The optimum source and load impedance of the single amplifier block matched to 50 Ω by using L-type matching networks. The schematic view for the single PA is given in Fig. 5.3

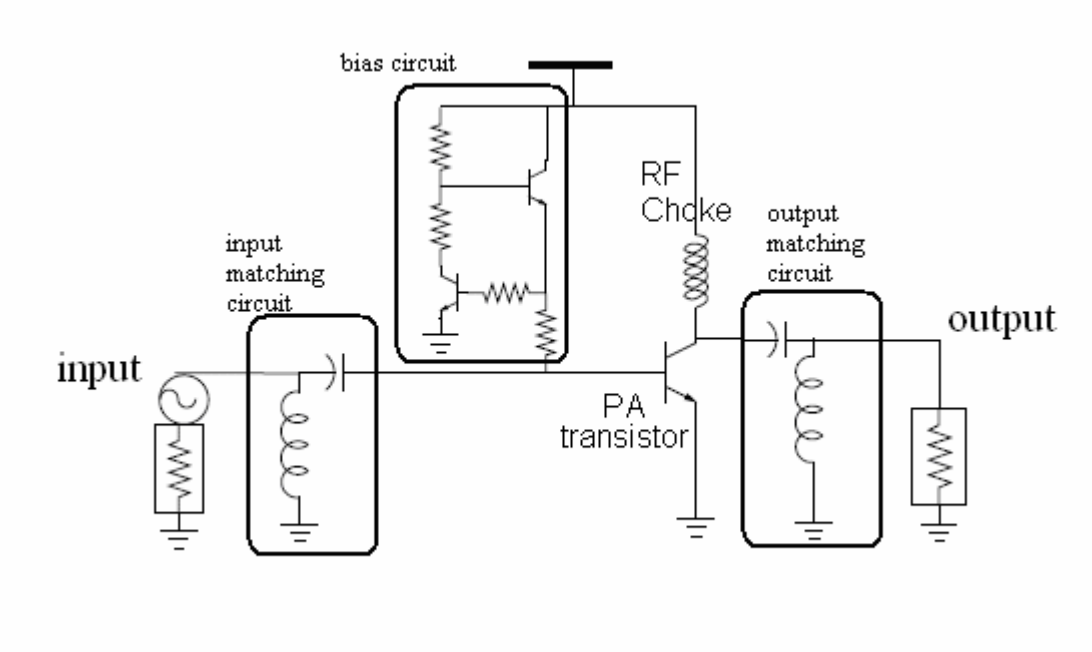

Fig. 5.3 Schematic view of Single PA

The S- parameter simulation results for single PA and combined PA are given in Fig. 5.4-5.8. Schematic level simulations are done for the comparison purpose.

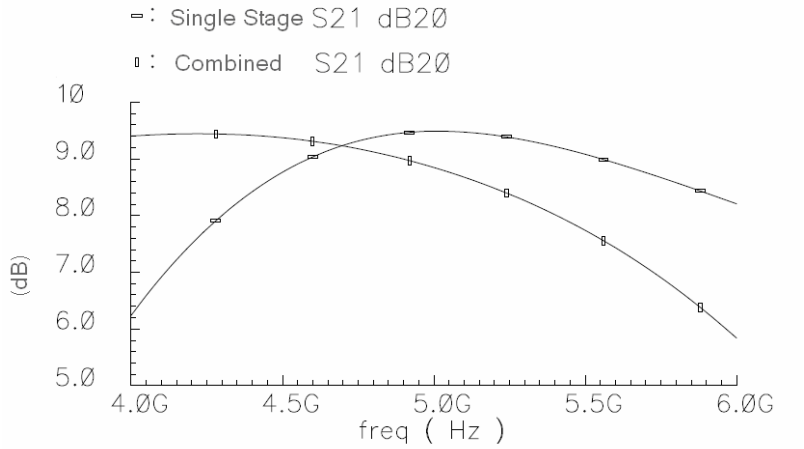

Fig. 5.4 S21 simulation results for Single PA and Combined PA

In Fig. 5.4, gain of 9.41 dB is obtained for the single PA whereas the gain of the combined PA dropped to 8.48 dB due to additional loss of the combiner and the splitter.

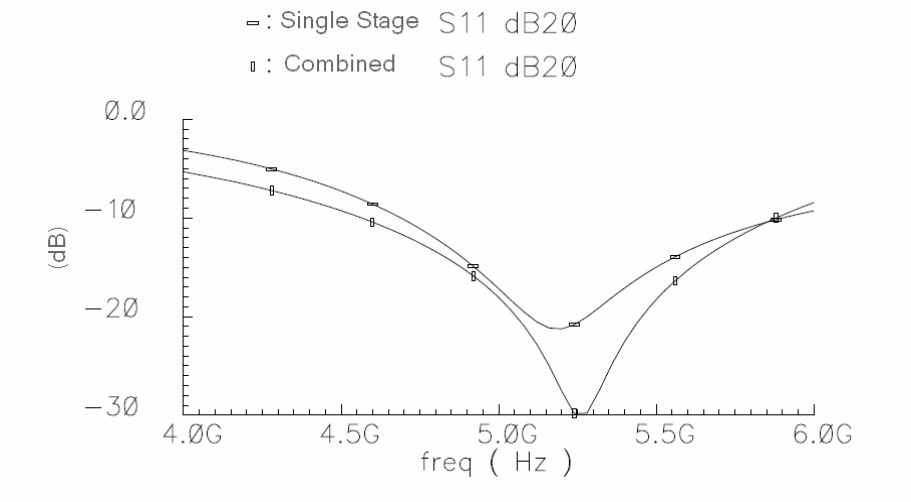

Fig. 5.5 S11 simulation results for Single PA and Combined PA

In Fig. 5.5, S11 of the both single PA and the combined PA are given for 5 GHz frequency band. The input return loss of -21.20 dB is obtained for the single PA and the S11 of the combined PA is -27.71 dB.

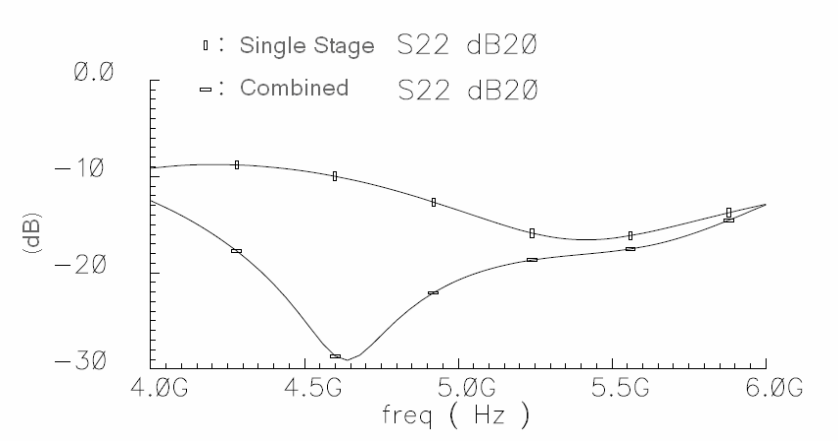

Fig. 5.6 S22 simulation results for Single PA and Combined PA

In Fig. 5.6, S22 of the both single PA and the combined PA are given. The output return loss of -15.55 dB is obtained for the single PA and the S22 of the combined PA is -18.90 dB. As it is seen from the figure, Wilkinson power combiner protects the transistor from reflecting power while showing the same load impedance with the single PA.

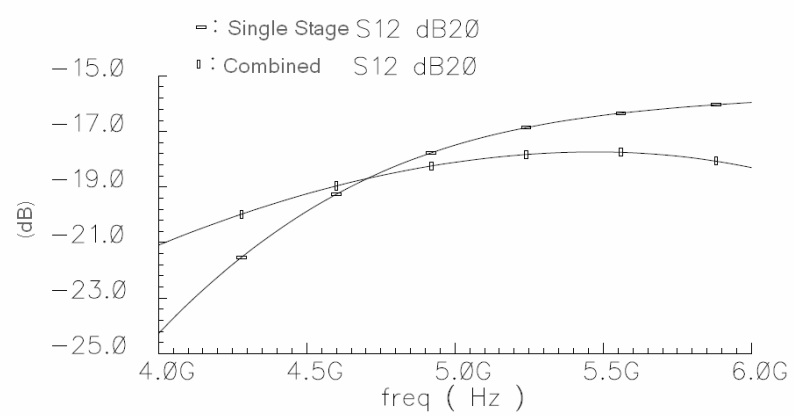

Fig. 5.7 S12 simulation results for Single PA and Combined PA

In Fig. 5.7, S12 of the both single PA and the combined PA are shown. The isolation of -16.93 dB and 17.86 dB is obtained for the single PA and combined PA respectively. As it is seen from the figure, the isolations of single PA and combined PA are approximately identical.

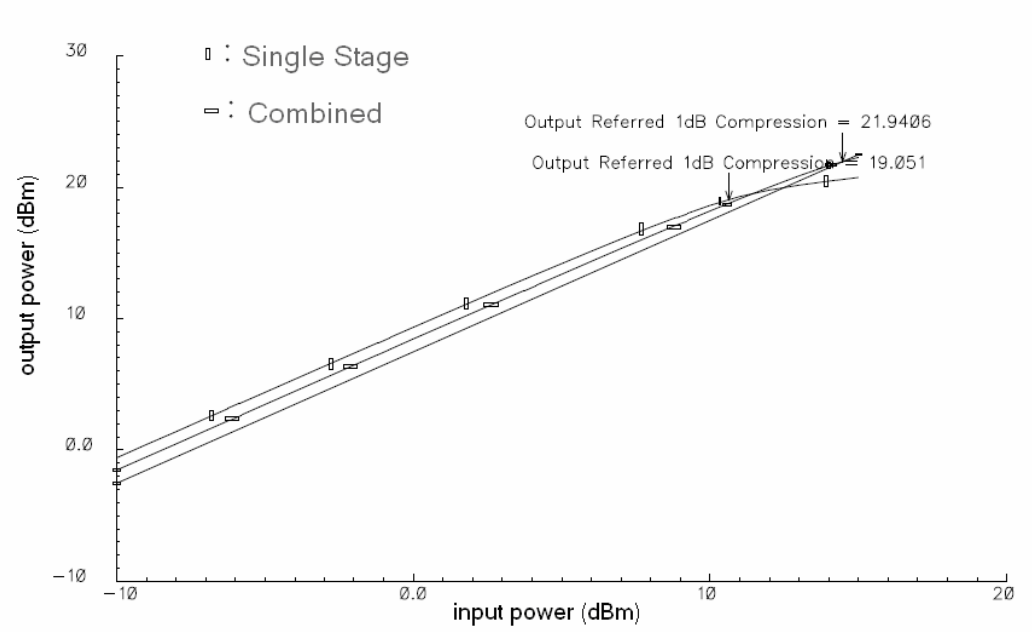

Fig. 5.8 1 dB compression point simulations for Single PA and Combined PA

In Fig. 5.8, input power swept from -10 dBm to 15 dBm for both single PA and combined PA. 1 dB compression point for single PA is found as 19.05 dBm whereas combined PA's 1 dB compression point is 21.94 dBm. 2.9 dB increases in 1 dB compression point verify the power combining idea mentioned in section IV. 0.1 dB additional loss is coming from the combiner's additional loss with respect to single PA's output matching circuit.

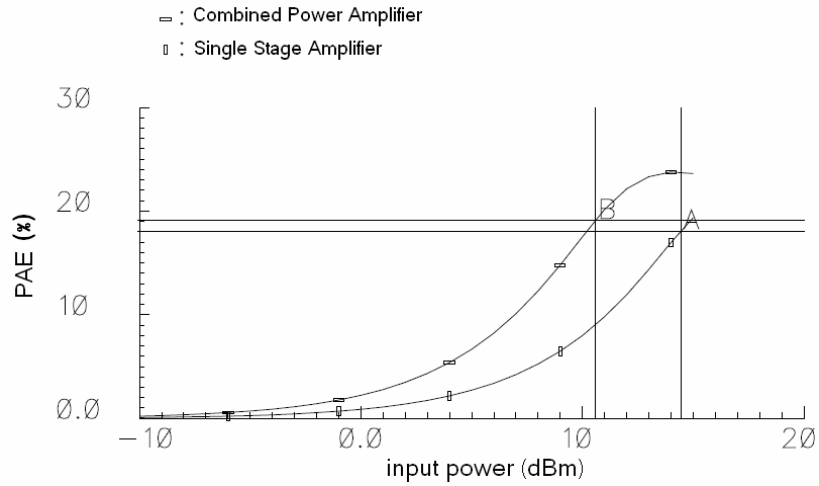

Fig. 5.9 PAE simulation results for Single PA and Combined PA

In Fig. 5.9, Power Added Efficiency (PAE) with respect to input power for single PA and combined PA are given. %19.05 (PAE) is obtained for single PA at 1dB compression point while PAE drops to %18.57 at 1dB compression point for combined PA. The reason of this slight decrease is mainly the additional loss of the combiner.

The simulation results obtained for the single PA, combined PA and another work with the same technology is summarized in table 5.1. The table summarizes that the power combining technique enables to achieve higher power levels in a cost of gain reduction.

	Single Stage	Combined PA	PA in [23]	Unit
S_{21}	9,41	8,48	15.5	dB
S_{11}	-21,20	-27,71	-18.6	dB
S_{22}	-15,55	-18,90	-5.8	dB
S_{12}	-16,93	-17,86	----	dB
P1dB	19,05	21,94	14.3	dBm
PAE @ P1dB	19,16	18,57	17	%

Table 5.1: Comparison of the Single PA, Combined PA and PA in [23]

5.2 Experimental Results for Combined Power Amplifier

The S-parameter measurements of the combined power amplifier are done using Agilent 8720ES Network Analyzer with a 50Ω measurement setup. The SOLT calibration is accomplished with the calibration kit and the effects of pads are not de-embedded. The S-parameter measurements of the combined power amplifier are given in Fig. 5.10 and 5.11 in comparison to post layout simulation results with 50 Ω measurement system.

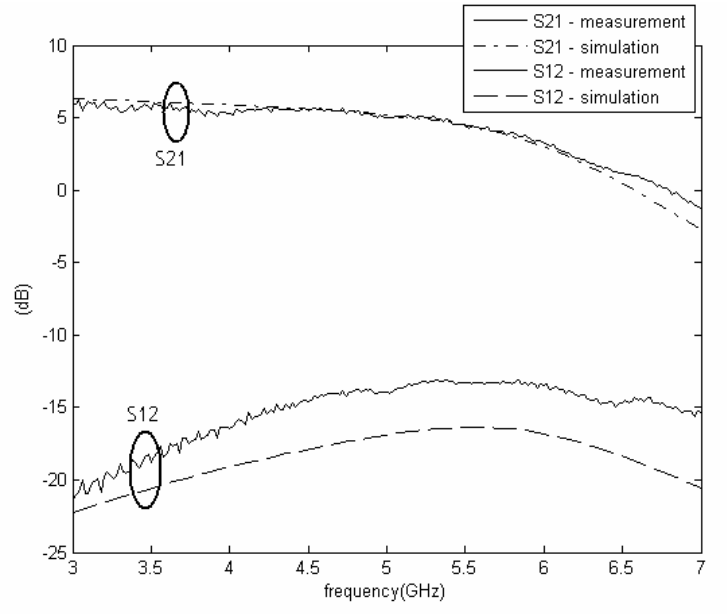

Fig.5.10 Measured and Simulated S21, S12 (dB) of combined PA

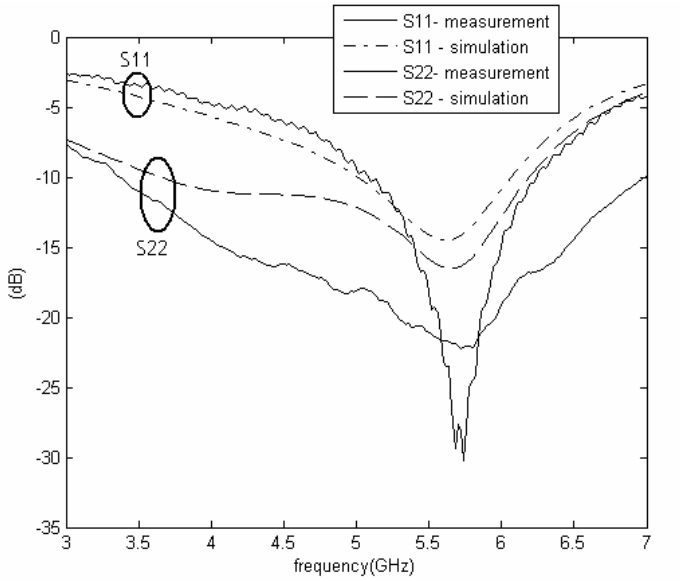

Fig.5.11 Measured and Simulated S11, S22 of combined PA

As it can be seen in Fig. 5.10, gain of 5.2 dB is obtained at 5.2 GHz. The simulated and measured gains are closely matched which means the simulated insertion loss of the impedance matching Wilkinson power divider circuits are well matched with the measurements. Note that any additional losses occur in the splitter/combiner, can be seen directly in the gain of combined PA. The isolation of combined PA is also in close agreement with simulations which is given in Fig. 5.10.

Fig. 5.11 provides input and output return losses of the Combined PA. Input return loss, S11, is measured to be below 10 dB in the 5.1-6.2 GHz frequency range. The S11 measurement results are in close agreement with simulations Note that the measurement result is very close to the splitters input return loss given in Fig. 4.16. Output return loss of the combined PA is measured to be below 10 dB in the 3.5-7 GHz frequency range. The measurement and simulated S22 is in close agreement. Note that the output return loss simulation results of the combiner given in Fig. 4.17 do not have to match those of the simulated and measured S22 of the combined amplifier. Since the combiner is designed to have 28.5+j3 Ω (optimum load impedance found by the load pull simulations). However, the amplifiers output impedance might be slightly different than the combiner input impedance. Different loading of the combiner can cause different output return loss.

Input power of the combined power amplifier swept from -14 dBm to 19 dBm to obtain 1 dB compression point of combined power amplifier at 5.2 GHz using Agilent 8267D RF signal generator and E4407B Spectrum analyzer.
In Fig. 5.12 1 dB compression point and power added efficiency measurement results are plotted in comparison with simulation results. 1 dB compression point is measured as 22.4 dBm which was calculated as 21.6dBm in post-layout simulation results.

Power added efficiency of 17% is obtained at 1 dB compression point while drawing 196 mA from 3.3 V supply.

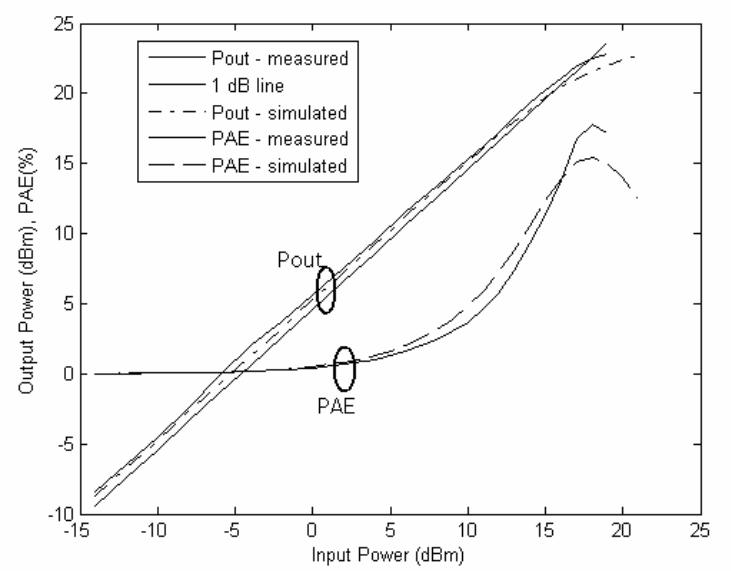

Fig.5.12 1 dB compression point and PAE of combined PA

Chapter 6

6. Conclusions and Future Works

In this thesis a 5.2 GHz fully integrated class-A RF power amplifier is implemented in 0.35μm SiGe BiCMOS technology. On-chip Wilkinson power combiner/splitter is designed with optimum load and source impedance for an RF power amplifier block so that no additional impedance matching elements are needed.

L-network lumped element impedance matching Wilkinson power dividers fabricated and measured individually to validate their performance. Measurement results show that the impedance values required for the combining technique can be obtained and the loss introduced by the substrate is within reasonable tolerances. Both of the implemented circuit's measurement results are in-line with the post-layout simulated results. The impedance matching Wilkinson power divider circuits can be used in various applications where dividing and matching is needed.

The impedance matching Wilkinson power dividers are used for combined power amplifier application. Total chip area is 1.2mm x 1.25mm including RF and bias pads. The output power at 1 dB compression point is measured as 22.4 dBm and the power added efficiency of 17% is achieved at 1 dB compression point while drawing 196 mA from 3.3V supply. The RF PA and combining circuit achieve a total gain of 5.2dB at 5.2 GHz frequency, input and

output return losses (S11, S22) are below -10 dB and output to input isolation is 14 dB. Therefore, the combined power amplifier can be used for 5.2 GHz WLAN applications.

As a future work, the on-chip Wilkinson power combining technique can be extended. In this thesis we concentrated on combining only two single stage power amplifiers, but this method can be modified to 2^N numbers of power amplifiers easily. The gain of the PA can be increased by increasing the number of stages. In addition to these extensions, a digital control scheme can be added to the combined power amplifier for power adjustment. It is well known that a PA can only achieve maximum efficiency at peak output power. As output power decreases, efficiency drops rapidly. However, for WLAN applications, the transmit power level could be well below the maximum power to control the interference to other users. The proposed power combining technique also offers a simple power control technique for achieving high efficiency even at the low power region. The technique is simply to turn off the bias current for some of the amplifier blocks when less power is required. As impedance matching Wilkinson power dividers provide enough isolation between the amplifier blocks, the operating amplifiers does not effected from this operation. Therefore the PA can work efficiently in a wide power range.

REFERENCES

[1] IEEE Draft Supplement to IEEE Standard 802.11: "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High speed Physical Layer in the 5 GHz Band", September 1999

[2] C.F. Jou, Cheng Kuo-Hua, Lin Chia-Min, Chen Jia-Liang, "Dual Band CMOS Power Amplifiers for WLAN applications", 46th IEEE International Midwest Symposium, Dec. 2003, Vol. 3, Pages 1227-1230.

[3] John D. Cressler, "Silicon-germanium heterojunction bipolar transistors", Boston, Artech House, 2003.

[4] R. Ahmed Shafik, Md. S. Rahman, AHM R. Islam and N. S. Ashraf, "On the error vector magnitude as a performance metric and comparative analysis", Emerging Technologies, 2006. ICET '06, Nov. 2006, Pages 27-31.

[5] Steve C. Cripps**,** "Advanced techniques in RF power amplifier design", Boston: Artech House, 2002.

[6] Rowan Gilmore, Les Besser,, "Practical RF circuit design for modern wireless Systems", Artech House Inc., 2003

[7] David K. Choi, "High Efficiency Switched Mode Power Amplifiers for Wireless Communications", Ph.D Thesis, 2001.

[8] Chang Kai, Sun Cheng, "Millimeter-Wave Power-Combining Techniques", IEEE Transactions on Microwave theory and Techniques, Vol: 31, No: 2, Feb. 1983

[9] J.B. Beyer, S.N. Prasad, R.C. Becker, J.E. Nordman, G.K Hohenwarter, "MESFET Distributed Amplifier Design Guidelines", Microwave Theory and Techniques, IEEE Transactions on, Volume 32, Issue 3, Mar. 1984, Pages:268 – 275.

[10] P. Abele, M. Zeuner, I. Kallfass, J. Muller, H. Laban Hiwilepo, T. Hackbarth, D. Chrastina, H. von Kaonel, U. Kounig and H. Schumacher, "32GHz MMIC distributed amplifier based on N-channel SiGe MODFETs", ELECTRONICS LETTERS 2nd October 2003 Vol. 39 No. 20.

[11] Kuo-Liang Deng, Huei Wang, C. Glaser, M. G. Stubbs, "A Miniature High Gain and Broadband MMIC Distributed Amplifier", European Microwave Conference, 2003. Oct. 2003 Pages:615 – 618.

[12] D. Gruner, G. Boeck, “6 GHz SiGe power amplifier with on-chip transformer combining”, Microwave and Optoelectronics Conference, Oct. 29 2007-Nov. 1 2007 Pages :790 – 794.

[13] P. Haldi, D. Chowdhury, P. Reynaert, Liu Gang, A.M. Niknejad, “A 5.8 GHz 1 V Linear Power Amplifier Using a Novel On-Chip Transformer Power Combiner in Standard 90 nm CMOS”, Solid-State Circuits, IEEE Journal, Volume 43, Issue 5, May 2008 Page(s):1054 - 1063.

[14] Tak S. D. Cheung and John R. Long, “A 21–26-GHz SiGe Bipolar Power Amplifier MMIC”, IEEE Journal of Solid-State Circuits, Mar. 2002, Vol.: 37, No:3, Pages: 371-383.

[15] I. Aoki, S. D. Kee, D. B. Rutledge and A. Hajimiri, “Fully Integrated CMOS Power Amplifier Design Using the Distributed Active-Transformer Architecture” , IEEE Journal of Solid-State Circuits, Dec. 2005, Vol. 40, No:12, Pages: 2583-2597.

[16] E. W. Bryerton, M. D. Weiss and Z. Popovic, “Efficiency of Chip-Level Versus External Power Combining”, IEEE Transactions on Microwave theory and Techniques, August 1999, Vol. 47, No: 8, Pages: 1482-1485.

[17] D. Staiman, M. E. Breese, W. T. Patton, “New Technique for Combining Solid-State Sources”, Journal of Solid-State Circuits, Sep.1968, Vol. 3, No:3, Pages: 238-243.

[18] David Pozar, “Microwave Engineering”, Addison-Wesley, 1993

[19] P. J. Riemer, J.S. Humble, J.F. Prairie, J.D. Coker, B.A. Randall, B.K. Gilbert, E.S. Daniel, ”Ka-Band SiGe HBT Power Amplifier for Single-Chip T/R Module Applications” Microwave Symposium IEEE/MTT-S International, pp. 1071-1074, June 2007.

[20] G. Carchon, K. Vaesen, S. Brebels, P. Pieters, W. De Raedt, B. Nauwelaers “Integrated Wilkinson Power Dividers in C-, Ku- and Ka- Band in Multi-Layer Thin-Film MCM-D”, European Microwave Conference, pp. 1-4, Oct. 2000.

[21] H. S. Nagi, ”Miniature lumped element 180/spl deg/ Wilkinson divider”, IEEE MTT-S International Microwave Symposium Digest, Volume 1, pp. 55-58, June 2003.

[22] Jeong Geun Kim, G. M. Rebeiz, “Miniature Four-Way and Two-Way 24 GHz Wilkinson Power Dividers in 0.13 _m CMOS” IEEE Microwave and Wireless Components Letters, Vol. 17, Issue 9, pp. 558-560., Sept. 2007.

[23] Canan Kavlak, “Power Amplifier Improvement Techniques/Circuits in 0.35 μm SiGe HBT Technology For 5 GHz Wireless Lan Band”, Master Thesis, 2006