REALIZATION of LOW POWER, HIGHLY LINEAR ROIC with CURRENT MODE TDI for LONG WAVE INFRARED DETECTORS

by

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Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of

Master of Science

Sabancı University

Summer, 2010

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Keywords: Readout integrated circuit (ROIC), focal plane array (FPA), scanning FPA, time delay integration (TDI), current mode.

Abstract

Infrared (IR) imaging systems can be used for variety of civil and military applications such as medical imaging, surveillance, night vision and astronomy applications. In IR systems, readout electronic is a key element between detector and signal processing units. System performance parameters of readout electronic can be enumerated as follows: signal-to-noise ratio (SNR), linearity, input referred noise level and dynamic range.

In this thesis, design of a CMOS readout integrated circuit (ROIC) for an array of 6x7 as a part of 576x7 full ROIC system, p-on-n type mercury cadmium telluride (HgCdTe) long wave infrared (LWIR) detectors is presented. AMS 0.35μm, 4-metal 2-poly CMOS process is used in the design of ROIC. Preamplifier of ROIC is direct injection(DI) type due to noise performance. In order to increase SNR, time delay integration (TDI) on 7 detectors is applied with a supersampling rate of three. TDI stage implemented as current mode with current memories rather than capacitances to store integrated charges. This particular novel current mode TDI design in this thesis brings superior features over other topologies like high linearity, low area and very low power consumption in comparison with capacitor based topologies. 99.9% linearity is achieved with 2.5 times smaller area with very low power consumption (28μW per channel) compared to other topologies. ROIC has additional

features of bidirectional TDI scanning, programmable five gain settings, and programmable integration time by serial/parallel interface. ROIC operated at 1 MHz with an output dynamic range of 3.75V and input referred noise of 1000 rms electrons.

UZUN DALGA BOYU KIZILÖTESİ DEDEKTÖR için AKIM MODLU TDI ile DÜŞÜK GÜÇLÜ YÜKSEK DOĞRUSALLIKTA ENTEGRE OKUMA DEVRESİNİN GERÇEKLEŞTİRİLMESİ

Melik YAZICI

EE, Master Tezi, 2010

Tez Danışmanı: Prof. Dr. Yaşar GÜRBÜZ

Anahtar kelimeler: Entegre okuma devresi (ROIC), odaksal düzlem dizileri (FPA), taramalı FPA, zaman geciktirmeli toplama (TDI)

Özet

Kızılötesi görüntüleme sistemleri biomedikal görüntüleme, gözetleme sistemleri, gece görüşü ve astronomi gibi çok çeşitli sivil ve askeri alanlarda uygulamalarda kullanılmaktadırlar. Okuma devresinin dizaynı çok kritiktir, çünkü dedektörden gelen bilgi sinyal işleme bölümüne yüksek hassasiyette ulaştırılmalıdır. Okuma devresinin sistem performansını belirleyen parametreler şu şekilde sıralanabilir; gürültü işaret oranı (SNR), doğrusallık, girişe yansıtılmış gürültü seviyesi ve dinamik aralık.

Bu tezde, 6x7 lik merkür kadmiyum tellür uzun dalga boylu kızılötesi dedektör dizini için CMOS entegre okuma devresi (ROIC) tasarımı sunulmuştur. Dizayn edilen 6x7 ROIC 576x7 lik tüm sistemin temel parçasıdır. ROIC dizaynında AMS 0.35µm, 4-metal 2-poli CMOS teknolojisi kullanılmıştır. Dizaynda önyükselteç olarak direk enjeksiyon topolojisi gürültü performansı açısından tercih edilmiştir. SNR seviyesini arttırmak için yedi dedektör üzerinde üçlü örnekleme ile zaman geciktirmeli toplama (TDI) kullanılmıştır. TDI bölümü kapasitör kullanan topolojilerin aksine toplanan akımları saklamada akım bazlı hafızalar

kullanmaktadır. Bu özel tasarım diğer topolojilere göre yüksek doğrusallık, düşük alan ve düşük güç tüketimi sağlanmaktadır. Diğer topolojilerle karşılaştırıldığı zaman, %99.9 doğrulsallık 2.5 kat daha küçük alan ve kanal başına 28 μW'lık çok düşük güç tüketimine sahiptir. ROIC bunun dışında TDI'da iki yönlü tarama, programlanabilir kazanç ayarları ve programlanabilir entegrasyon süresi gibi özellikleri seri ve paralel arayüz üzerinden sunmaktadır. ROIC 1 MHz'de 3.75 V'luk dinamik aralıkta ve 1000 rms elektron girişe yansıtılmış gürültü seviyesi ile çalışmaktadır.

Acknowledgements

First of all, I would like to thank my advisor Prof. Yaşar Gürbüz not only for giving me the opportunity to carry out my Master's Thesis, but also for his endless, patient guidance and his support throughout my MSc. I am also thankful to Ayhan Bozkurt, Meriç Özcan, Cem Öztürk and Erkay Savaş for their valuable comments and presences in my thesis defence. This thesis was sponsored financially by ASELSAN Inc. I would like to thank Mrs. Hacer Selamoğlu, Manager of the Electronics Design Group, at ASELSAN-MGEO, for their great support and this opportunity to work on this project. Also, I am thankful for valuable technical discussions through my thesis work with ASELSAN team under supervision of Ümid Tümkaya.

Hüseyin Kayahan and Ömer Ceylan deserve extra special thanks as a team member in this project for their everlasting supports and friendships. Moreover, I want to thank all my friends in Sabancı University for their technical and motivational supports. Specifically, I am grateful to Muharrem Bayraktar and Emre Özeren for friendship and support in my first graduate year. Then, I would like to share my appreciation to Samet Zihir and Ferhat Taşdemir as lab partners and very good friends. Besides, I would like to thank to Aydın Aysu, Onur Can Ulusel and Abdulkadir Akın for their friendship in my undergraduate and graduate year in Sabancı University, and in particular to Gülperi Özsema for her support and for best friendship. And many more thanks to all of my friends that I forget to mention in Sabancı University and any other parts of the World.

Finally I would like to thank to my family; My parents Fatma and Mehmet for their love and support.

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1 INTRODUCTION

1.1 Introduction

Infrared radiation (IR) is non-visible electromagnetic radiation with a wavelength between 0.7 and 300 micrometers (µm). Discovery of IR went over to 1800s; Sir William Herschel observed higher temperatures with regular lead thermometer beyond the red end of the visible spectrum by passing sunlight through a glass prism.

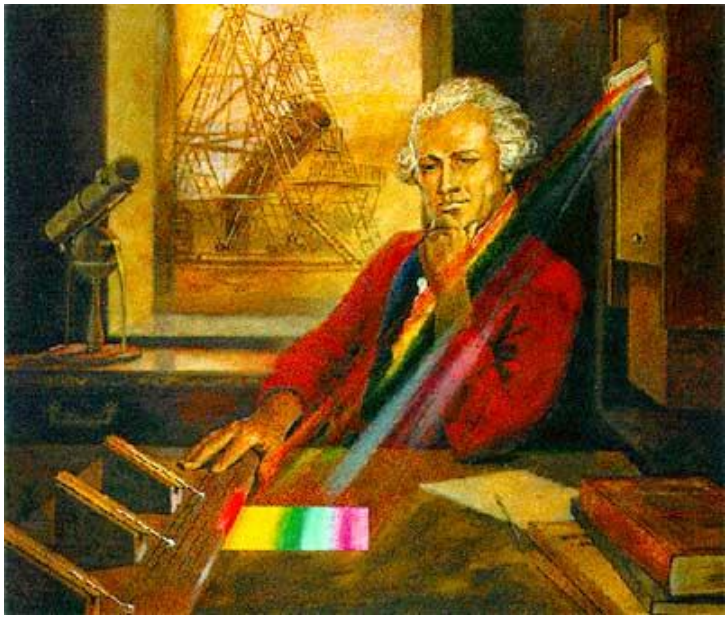


Figure 1.1: Herschel's experiment with light [1].

In modern day, infrared imaging systems can be used for variety of civil and military applications such as medical imaging, surveillance, tracking and night vision, missile guidance, space and astronomy applications, meteorology, climatology and forward looking infrared systems (FLIR). An infrared imaging system composed of three main elements; optics, detector and readout electronics. Depending on a system, a scanner and cooler can be needed as well.

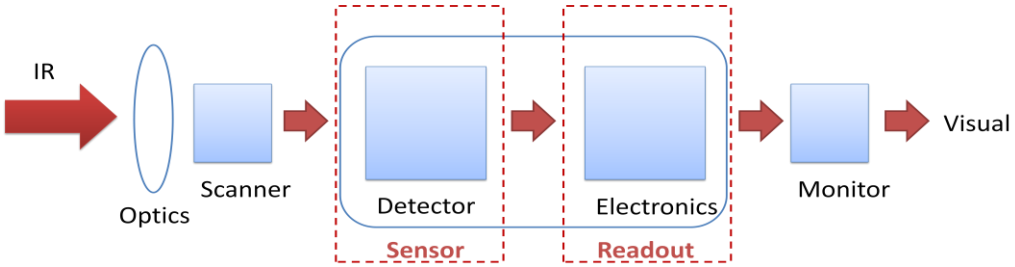


Figure 1.2: General architecture of scanning array IR imaging system.

Optical part of the system is responsible for focusing infrared light on the detector. If the detector is formed as single array rather than two dimensional array, scanner is needed for focusing portions of light to form 2D image from 1D array. Moreover, some types of infrared detectors are needed to be cooled in order to capture infrared radiation with lower noise and wide ranges. Finally, electronic part of system is responsible for capturing detector information and processing it to improve signal to noise ratio and amplifying signal for digital signal processing part of the system.

In infrared system, array of IR detectors and its readout part of the system referred as Infrared Focal Plane Arrays (IRFPA). In these systems, generally readout electronics and detectors are built on different substrates. By using flip chip bonding method these two different substrates are bonded together to form complete IRFPA. This type of structure is called as hybrid array structure. In flip chip method, two different substrates are aligned and connected through solder or indium bumps, or loophole interconnection as shown in Fig. 1.3 [2]. Flip chip bonding method developed by IBM in 1960s is cheapest, area saver, flexible and reliable post processing method [3].

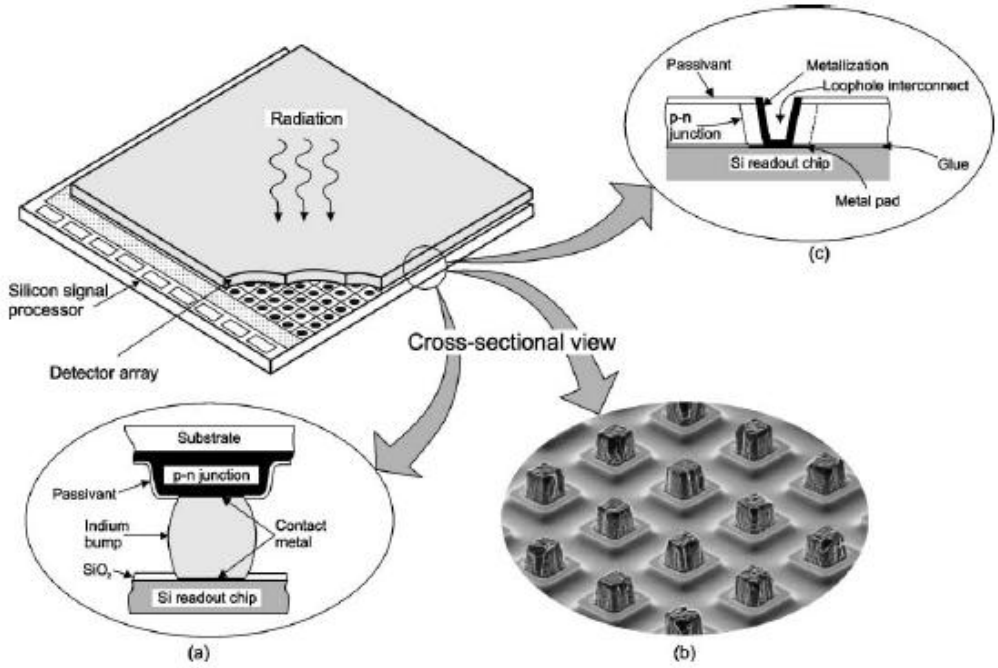


Figure 1.3: Hybrid detector array with indium bump connection technique [2].

Other type of structure is monolithic array structure. In this structure both the detector and multiplexing part are on the same silicon substrate. Monolithic array is not as flexible as

hybrid array structure because of limitations of silicon process compatible detectors, their radiation spectrum and sensitivity performance is very limited [3]. Hence hybrid structures are more preferable than monolithic structure for high performance systems, because detector materials can be optimized and developed independently from silicon process.

FPAs also classified for their image capturing system; scanning arrays and staring arrays. In scanning array systems, there is one column of detector to capture the radiation. So it's one dimensional array (1D). By scanning, from 1D detector array 2D image can be obtained. Also due to losing time by scanning, frame rates of these systems are slower than staring array systems. In order to suppress noise and improve SNR of image, there can be four or seven detectors for each column instead of just one detector to form 1D array. These detectors that are on the same column get same information. Integration of these currents with some analog techniques results in improved SNR of image in scanning array system.

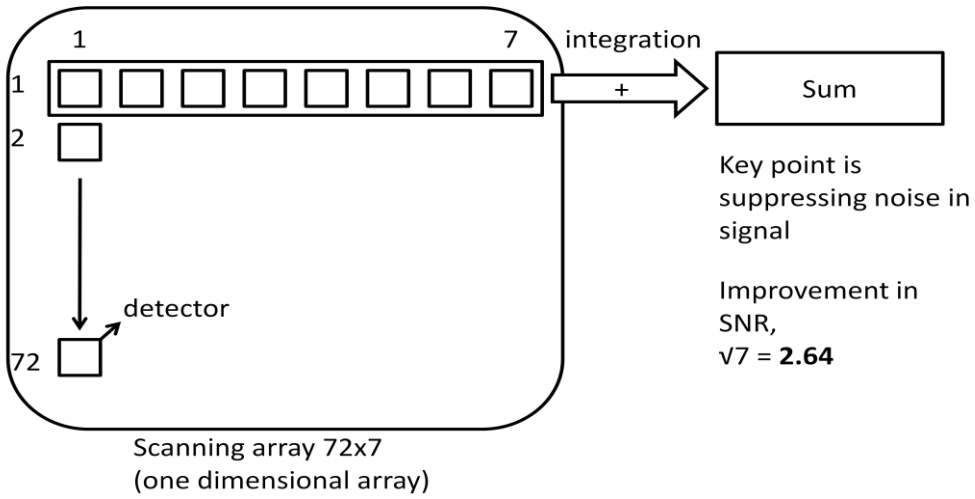


Figure 1.4: Integration of photocurrent to improve SNR in scanning type 1D arrays.

Staring type of FPAs do not use optical scanner, because all detector arrays are already fabricated as two dimensional array (2D). In recent days, 4096 x 4096 is the highest resolution fabricated infrared detector array size. This is size called as limit for 2D systems because in recent technology larger than this size is inefficient for production. If larger resolution is required array of this detectors can be used together in a single system [4].

Latest classification method is based on detector type. There are two main detector types one is photodetectors, other one is thermal detectors. Photodetectors are also classified in two parts; photoconductive and photodiode. Quantum well infrared photodetector (QWIP) is

photoconductive type infrared photodetector which contain one or more quantum wells. A quantum well is thin layer with small band gap that confines particles (electrons or holes), sandwiched between two layers of semiconductors with large energy gap. Gallium Arsenide (GaAs) is typical type of QWIP example. Advantages of QWIP are their low cost, high yield, high uniformity and narrow spectral response that allow multi-color devices. Main disadvantages are low quantum efficiency (10%) and low operating temperature requirement [4]. Quantum efficiency can be defined as percentage of photons that hit the detector that produces electron-hole pair.

Photovoltaic detectors are basically semiconductor pn junction diodes, that directly produce current from incident photon with higher energy than band gap of pn junction. Unlike photoconductive devices, photovoltaics can be operated at almost zero bias that will reduce power consumption. Some photodiodes are Indium Antimonide (InSb), Mercury Cadmium Telluride (HgCdTe or MCT) and Type II Strained Layer Superlattice (InAs/GaInSb, Type II SLS). Depending on application and desired wavelength these materials are used to developed detector. As seen from Fig. 1.5 MCT detector covers most of the wavelength band from Short Wave to Long Wave. Moreover, pn junction can be used in photoconductive mode by reverse biasing the junction. But in this mode junction tends to produce more electric noise.

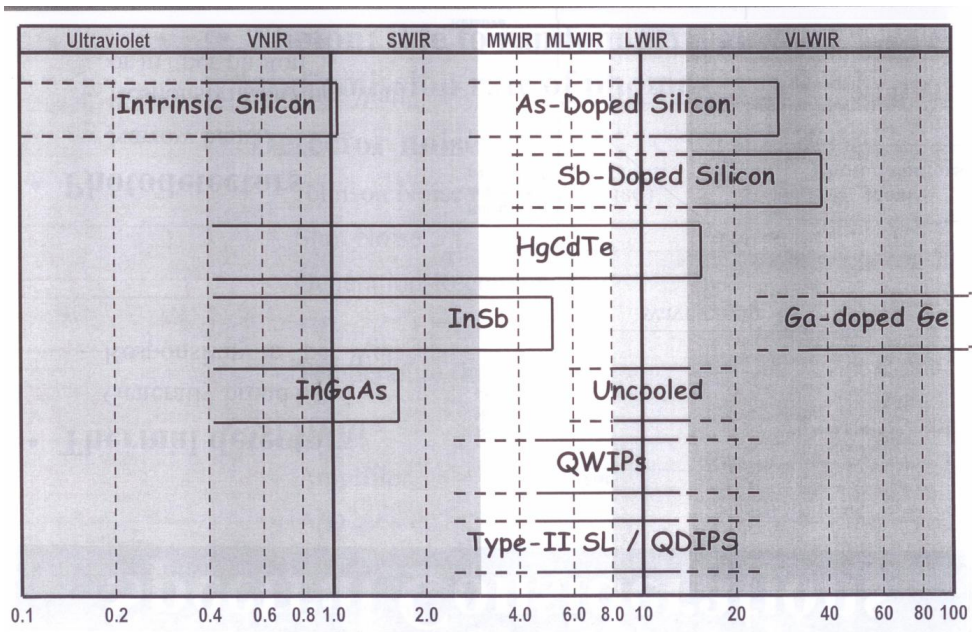


Figure 1.5: Spectral ranges for leading visible and infrared detector materials [4].

Due to coverage of most of infrared band and some other advantages, MCT is most popular detector for all ranges. Its quantum efficiency is superior to other materials, dielectric constant is low, electron mobility is high and it has some other advantages over other materials. Most crucial disadvantages are cost, low yield and increased non-uniformity of response for large area [5]. Table 1.1 below shows clearly main differences between detector types for LWIR range at 77 °K temperature.

Parameter	**HgCdTe**	**QWIP**	**Type-II SLS**
IR Absorption	Normal Incidence	None @ Normal Incidence	Normal Incidence
Quantum Efficiency	≥ 70 %	≤ 10 %	≈ 30 - 40 %
Spectral Sensitivity	Wide-Band	Narrow-Band FWHM ≈ 1-2 μM	Wide-Band
Optical Gain	1	0.2 (30-50 wells)	1
Thermal Generation Lifetime	≈ 1 μs	≈ 10 ps	≈ 0.1 μs
R0A Product	300 Ω-cm^2	10^4 Ω-cm^2	100 Ω-cm^2
Detectivity (FOV=0)	2 x 10^{12} cm-Hz^{½}/W	2 x 10^{10} cm-Hz^{½}/W	5 x 10^{11} cm-Hz^{½}/W

Table 1.1: Typical properties of LWIR detectors at 77 °K [4].

As observed from table above Type II SLS are not superior to HgCdTe detectors for LWIR but as predicted they have strong potential for superior performance over MCT detectors and will replace MCT detectors in next 20 years [4]. But today's dominant and superior detectors are MCT detectors [4].

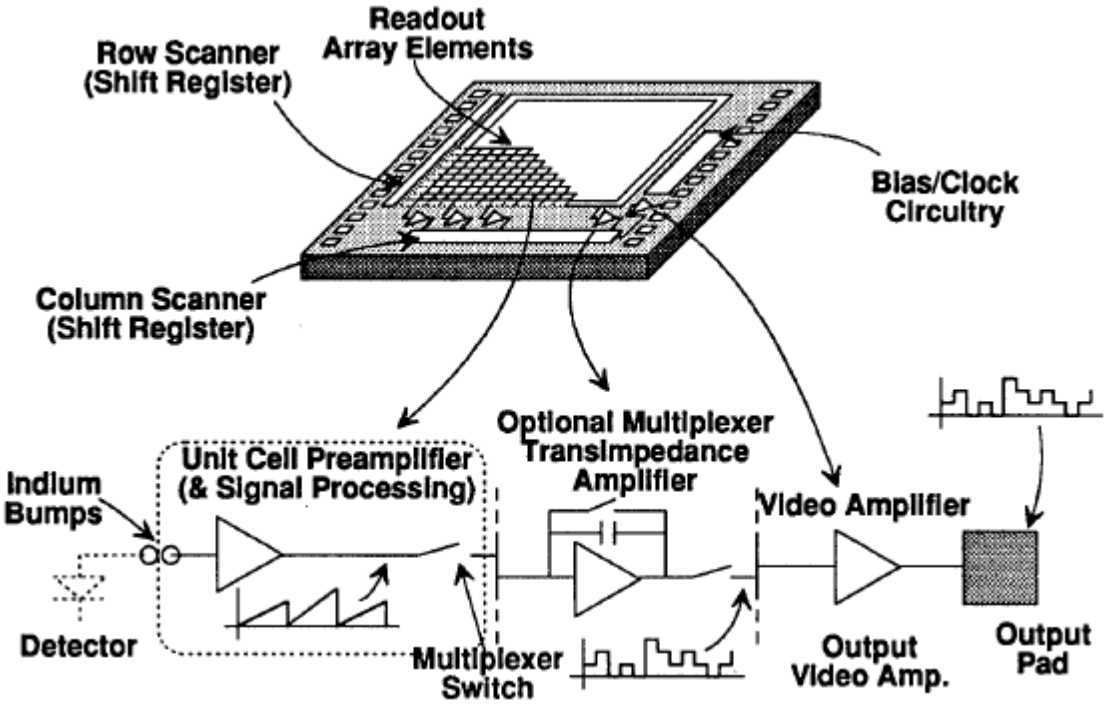


Figure 1.6: General ROIC architecture [5].

Fig. 1.6 demonstrates basic view of staring type FPA with readout integrated electronic circuit (ROIC) and detector. Detector is bonded on ROIC with flip chip method via indium bumps. For each detector element, unit cell preamplifier is dedicated. There are several unit cell topologies available such as source follower per detector, direct injection, buffered direct injection and capacitive transimpedance amplifier. Following block is amplifier and noise suppression stage. Some analog algorithms are applied in this stage to increase signal to noise ratio. Finally buffer stage drives analog output through output pad. Further signal processing can be applied off-chip after digitalization of analog output.

1.2 Motivation

Infrared FPAs can be used wide range of high-tech applications which are used medical imaging, missile guidance, and surveillance systems. These systems composed of many blocks such as optic, detector, electronic and digital signal processing. One of the very crucial blocks is ROIC, which is the interface between detector and digital signal processing of the IRFPA, and performance of ROIC directly affects overall system. Therefore, design of ROIC is very essential part of the IRFPA system, all building blocks should be carefully chosen and

designed according to many parameters such as detector type, operating conditions and process technology.

In this thesis, a CMOS ROIC is designed and implemented for scanning type of 72×7 P-on-N HgCdTe detector array as a building block of 576x7 system using 0.35 μm, 4 metal 2 poly AMS CMOS process named C35B4. Direct Injection preamplifier (DI) is used as the unit cell of the ROIC. For the analog signal processing, Time Delay Integration (TDI) over 7 elements with a supersampling rate of three is used for improved Signal-to-Noise Ration (SNR). In TDI algorithm MOSFET based current mode memories used instead of poly capacitors for storage of integrated photocurrent. This particular approach and design significantly reduces both area and power consumption by increasing linearity of output. Output of circuit has a dynamic range of 3.75V from 1.25V to 5V. The organization of thesis is given in section 1.3.

1.3 Thesis organization

In Chapter 2, ROIC building blocks are explained and discussed in detail. First, most of the preamplifiers already discussed in the literature, are explained and compared in terms of their injection efficiency, linearity, input referred noise level and power consumption. Next a noise reduction techniques are explained, main focus is time delay integration (TDI) for scanning type of ROICs. TDI architecture methods compared and explained in terms of tradeoffs between area and power consumption with examples.

In Chapter 3, implementation of chosen individual blocks that is discussed in Chapter 2 is explained. First requirements for the specific ROIC 576x7 HgCdTe array are given as well as the detector properties. Next, input preamplifier selection as direct injection is introduced. Implementation of preamplifier together with input capacitor selection and variable gain application is discussed. In the next section, implementation of the TDI according to the chosen topology is shown. Together with as a requirement of selection topology voltage to current converter is discussed on the following section. As a final stage of analog channel, output buffer is also defined. Digital control block design to operate the ROIC, as well as required user interface is explained. Finally, ring oscillator based temperature sensor is designed for measuring cryogenic temperatures.

Chapter four includes simulation and experimental results of building blocks of ROIC and overall system.

Finally, in chapter five, conclusions of this study are provided, problems are addressed and future study is discussed.

2 LINEAR ROIC BUILDING BLOCKS

2.1 Introduction

ROICs are crucial interface element of IRFPAs between detector and digital signal processing unit. Performance of ROIC has a great effect on overall performance of IRFPA. Because, well designed ROIC captures very small (1-50nA) photocurrent from detector precisely, processes it to improve its signal to noise ratio and produces high level output. All ROICs composed of preamplifier stage, noise reduction stage and output stage with digital control circuitry.

First stage of ROIC is preamplifier, it is immediate interface circuit between detector and ROIC. Careful design and topology selection is important for preamplifiers. Most of the performance parameters are strictly dependent on this input preamplifier, especially; input referred noise, injection efficiency, dynamic range and linearity are key performance parameters of ROIC.

Noise reduction techniques are employed all type of ROICs. For staring and scanning type of arrays, correlated double sampling (CDS) and time delay integration (TDI) techniques is used respectively. Correlated double sampling (CDS), is used in sample and hold circuits in order to store an amplifier noise, and subtract it from another set of results. Time delay integration (TDI) is another method used to increase signal to noise ratio (SNR) through creating an output by adding multiple measurements with a time difference from a set o detectors.

Moreover, supersampling is further SNR improvement techniques used together with TDI, to effectively increase spatial resolution of the image, without increasing the number of elements on the FPA. Super sampling is realized by setting more scanning steps for a single detector on a row. For instance, an image is passed through a detector with three steps, results with three data from a single detector, in other words, a super sampling rate of three.

In this section above mentioned building blocks of ROIC and signal processing methods are explained and discussed in detail with advantages and disadvantages of methods with examples.

2.2 Preamplifiers

In ROIC, most important and crucial part of the block is the preamplifier (unit cell stage). Because, in order to transfer accurately detector information to electronic circuitry, careful design of unit cell is very essential part of ROIC design.

First of all, an unit cell should have low noise and high injection efficiency. Injection efficiency refers to how many percentage of detector current transferred from input stage. Another crucial parameter is linearity, while transferring detector information same amount of change should be observed at the output of unit cell. Non-linear transfer of detector information can cause wrong coloration of information in the final infrared image. At least, this non-linearity should be compensated in the signal processing part of the system. Moreover, occasionally unit cells transfers very low currents from detectors, hence preamplifier design should be take care of very low currents.

Other clichéd and inherent design parameters are power consumption and area. Power consumption is critical since for each detector pixel there should be unit cell. To save area ideally each unit cell should fit the area determined by pixel size of detector.

In this section, most common and popular ones are individually discussed and other not so popular topologies will be mentioned separately. At the end of section, comparison of topologies are given.

2.2.1 Source Follower per Detector

The source follower per detector (SFD) preamplifier is composed of three transistors, thus it covers very small area. Two of transistor composed of source follower stage, other transistor is responsible for resetting detector information as shown in Fig. 2.1.

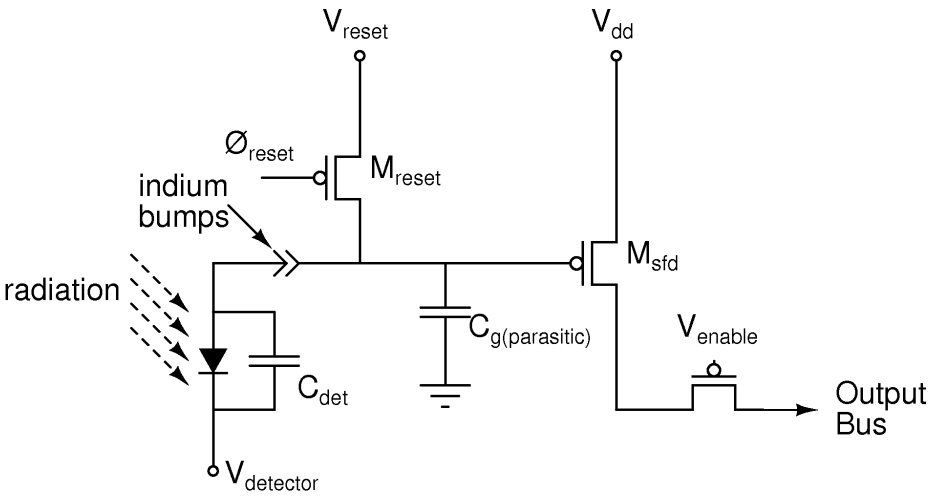


Figure 2.1: SFD preamplifier topology.

C_g in the figure forms integration capacitance of unit cell. Detector information is stored in this capacitance. C_g contains gate capacitance of source follower stage and metal routing capacitances. Charge stored in integration capacitance is converter into voltage at the output of source follower stage. After read operation is done reset switch zeros integration capacitance.

Gain of unit cell is determined by source follower stage and it is almost unity gain by topology. Also dynamic range is limited by voltage at the input of source follower stage caused by integrated charges. If this voltage exceeds detector forward bias nonlinearities and extra shot noise are unpreventable.

SFD is typically used for low background applications such as telescopes. For instance, it's being used in SPITZER Space Telescope and WISE Space Telescope with very long wave infrared radiation (VLWIR) sensitive detectors [4]. In this applications long integration times are required for accumulate adequate charges.

Noise sources of SFD can be addressed as 1/f in the input, kTC and MOSFET channel thermal noise. 1/f MOSFET noise can be overcome by increasing simply product of width and length of a transistor (W, L). In the process, increase of gate oxide capacitance (C_{ox}) can also reduce 1/f noise. Moreover, noise in SFD can be handled by optimizing the noise equivalent bandwidth of the unit cell [6].

2.2.2 Direct Injection

Direct Injection (DI) topology is smaller than three transistor SFD topology. DI composed of only two transistors, one is directly connected to detector other one is reset switch. If we ignore reset transistor, we can count DI as one transistor because reset is obligatory transistor for each preamplifier circuit. Since it is formed of only one transistor, DI has very low noise. Using integrated capacitor (C_{int}) rather than parasitic that is in the case of SFP, DI unit cell is capable of variable gains.

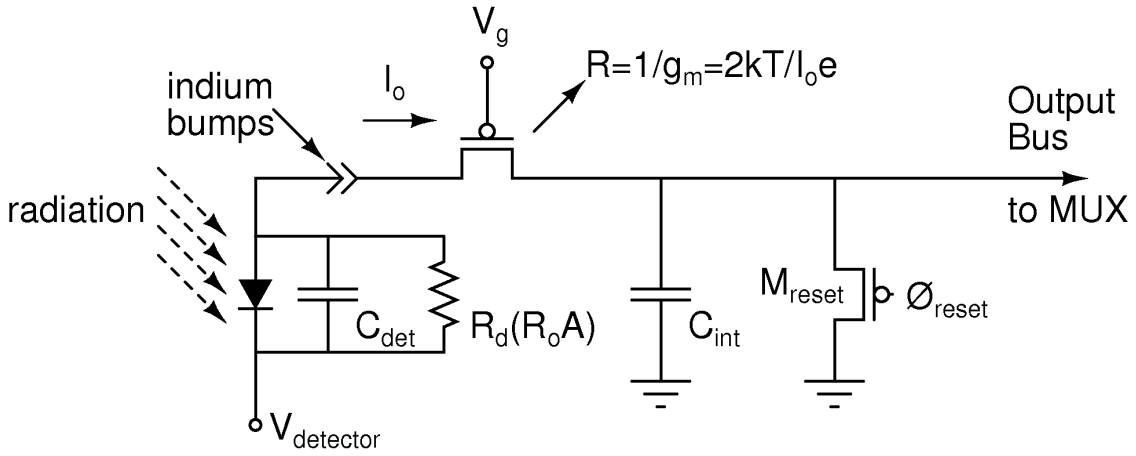


Figure 2.2: Direct injection preamplifier topology.

Injection efficiency of DI is very high if properties of detector is correctly chosen. Firstly, in order to achieve high injection efficiency with DI, detector impedance (R_d) should be high. Additionally, in low photon irradiance condition, performance of efficiency of DI reduced. Fig. 2.3 clearly shows injection efficiency of DI with different detector impedances.

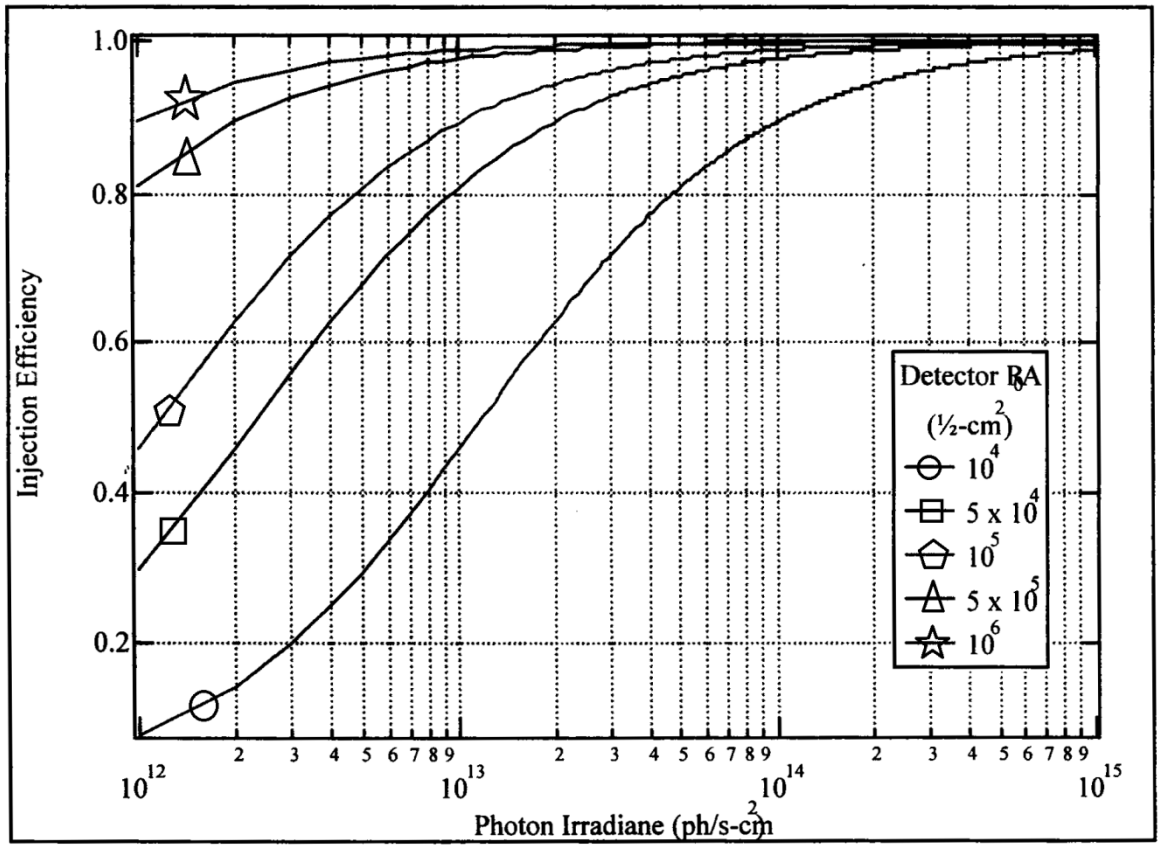


Figure 2.3: Injection efficiency vs Photon irradiance of MCT detector in LWIR range [4].

Injection efficiency η can be calculated with formula below. I_d refers to detector current and I_0 defines as integrated photo current (output of DI).

$$\eta = \frac{I_0}{I_d} = \frac{g_m R_d}{1 + g_m R_d} \tag{2.1}$$

Integrated currents are generally so low, hence DI transistor operates in weak inversion, also known as subthreshold region. Subtreshold current through DI transistor and its transconductance value of g_m are calculated as follows [7].

$$I_d = \frac{W}{L} \mu_n C_{ox} e^{\left(V_g - \frac{mkT}{q}\right)} \tag{2.2}$$

$$g_m = \frac{I_d q}{mkT} \tag{2.3}$$

g_m is simply derived from I_d formula by taking derivative with respect to drain current and gate voltage. As observed from derived formula, it is independent from detector properties. This means that DI as a poor choice for the low flux or low detector impedance applications. Reduced linearity due to low injection efficiency is inescapable.

Moreover g_m has a contribution on bandwidth of the detector. It can cause frame to frame crosstalk if g_m is the dominant impedance on the node. Calculation of frequency of detector is given as following, C_{det} is detector capacitance and C_{gs} is gate to source capacitance of MOS device [6].

$$f\left(-3dB\right)=\frac{g_m}{\pi\left(C_{det}+C_{gs}\right)} \tag{2.4}$$

The noise contributors for DI unit cell are MOSFET, 1/f noise and kTC thermal noise. MOSFET noise results in output current (i_o) as a function of detector resistance. As a result, MOSFET noise (e_n) is negligible in the output current when detector impedance (R_d) is high.

$$i_0 \approx \frac{e_n g_m}{1+R_d g_m} \tag{2.5}$$

High detector impedance is essential in case of DI unit cell since it positively affects noise performance and injection efficiency.

2.2.3 Buffered Direct Injection (BDI)

In this configuration, unlike DI feed-forward inverting amplifier with a gain of A is connected between the detector and the gate of injection transistor. This configuration keeps advantages of DI and has extra advantages over DI because of inverting amplifier. This amplifier increases gm by a factor of 1+AV, therefore input impedance reduces 1+AV times.

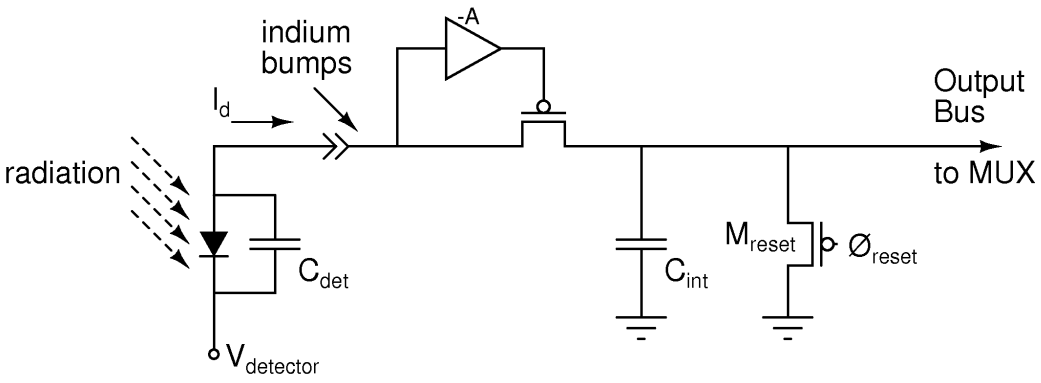


Figure 2.4: Buffered direct injection topology.

$$g_i = g_m\left(1+A_V\right) \quad \left[A/V\right] \tag{2.6}$$

However There are significant drawbacks of this configuration more than the advantages. This buffer configuration increases complexity and enlarges area of unit cell thus it will be challenging to fit unit cell inside pixel area. Furthermore, power consumption increases significantly. Due to extra components (buffer) and heat caused by high power consumption, overall noise of unit cell increases. Output referred MOSFET unit cell noise for BDI is,

$$i_0 \approx \frac{e'_n\, g'_m\, A_V}{(1+A_V)(1+R_d g'_m)} \approx \eta\frac{e'_n}{R_d} \quad [\mathrm{A}/\sqrt{Hz}] \tag{2.7}$$

in which input referred noise of inverting amplifier e'_n dominates other noises. The noise component comes from injection transistor is negligible due to inverting amplifier which reduces by A_V[6].

To sum up, BDI is not so favorable topology due to significant drawbacks such as large area, high power consumption and high noise contribution.

2.2.4 Capacitive Feedback Transimpedance Amplifier

Capacitive feedback transimpedance amplifier (CTIA) unit cell can be for used many applications and various detector interfaces since it provides highly stable detector bias, wide dynamic range, high gain and low noise [8]. It is mostly used with correlated double sampling (CDS) technique to further improve noise performance. CTIA and CDS structure generally can be fit inside pixel area [9].

Detector current increases the voltage level at the negative input of the amplifier. Increase in negative input of amplifier causes voltage drop at the output of amplifier. This drop pulls detector current to the feedback capacitor. After read operation is done, parallel connected reset transistor with respect to feedback capacitor initializes feedback capacitor.

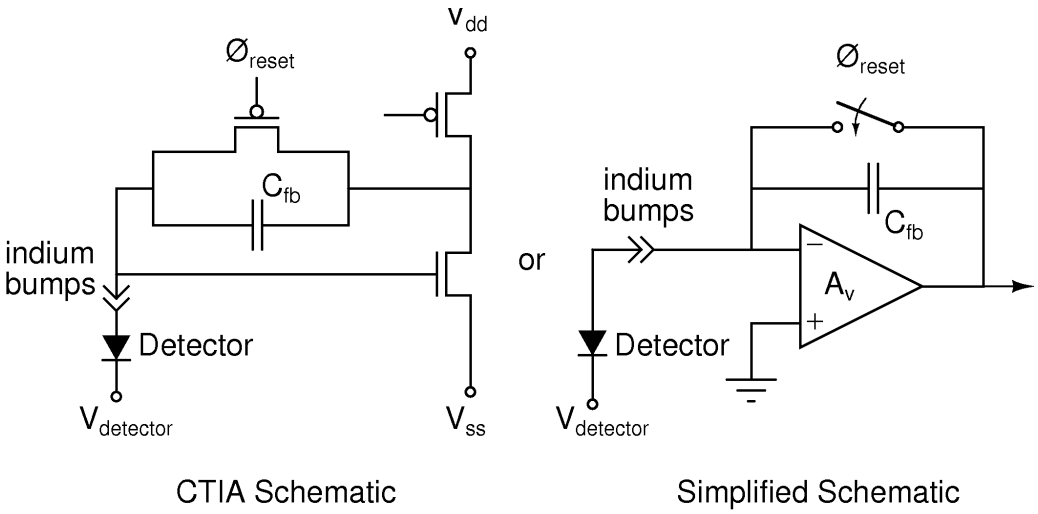


Figure 2.5: Capacitive feedback transimpedance amplifier topology.

CTIA gain and transimpedance can be expressed as follows,

$$V_{out} = \frac{I_d t_{int}}{C_{fb}} \tag{2.8}$$

$$z_t = \frac{V_{out}}{I_d} = \frac{t_{int}}{C_{fb}} \tag{2.9}$$

In this equations C_{fb} is the feedback capacitor, I_d is detector current and t_{int} is the integration time.

Main noise sources of CTIA unit cell is input transistors of differential amplifier. To eliminate this noise in most applications in-pixel CDS is used. CDS reduces low frequency (1/f) noise and eliminate kTC noise caused by reset transistor [8].

2.2.5 Other Preamplifier Topologies

Besides these four most popular topologies there are some other unit cell topologies that addressed more specific applications and detector types.

2.2.5.1 Resistor Gate Modulation

Resistor load gate modulation (RL) unit cell in Fig. 2.6 is suitable for high flux background applications. In other words, proper designing of the resistor value I_{int} can be close to zero for determined value of background level. In this way, signal of interest can be purified from background.

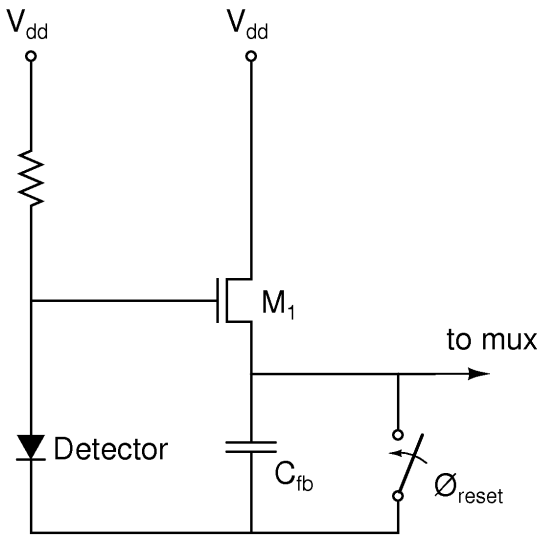


Figure 2.6: Resistor gate modulation topology.

2.2.5.2 Current Mirror Gate Modulation

Current mirror gate modulation configuration in Fig. 2.7 is very similar to RL unit cell but in this case resistor in there replaced with a MOSFET with current mirror configuration. If two transistor is matched detector current directly transferred to output because those transistors both have same gate and source voltages. With different geometries output current can be scaled by desired value. In reality it not possible to transfer current perfectly, transistor and threshold voltage variations of the process causes pixel to pixel differences. This process variations also affects noise performance and injection efficiency of the circuit.

Other than, It has better linearity performance than RL unit cell and comparable injection efficiency with DI unit cell except process variations.

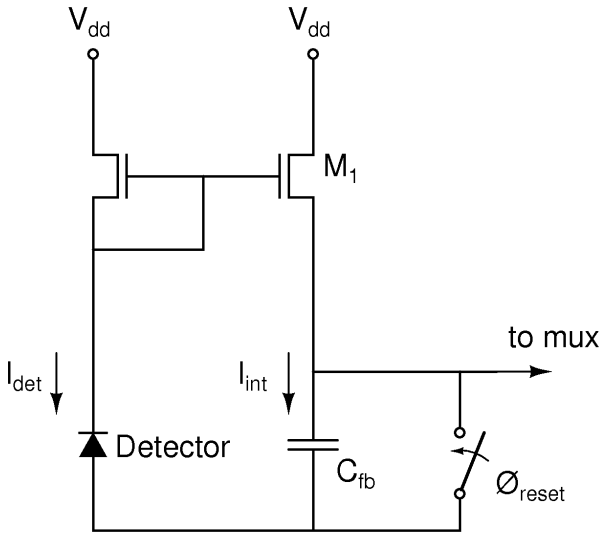


Figure 2.7: Current mirror gate modulation topology.

2.2.5.3 Current Mirroring Direct Injection

Current mirroring direct injection (CMDI) achieves perfect (100%) injection efficiency even in case of very low input impedances with a cost of extra power consumption. Also, it creates a very stable detector bias compared to the DI unit cell. As a disadvantage, it introduces poor noise performance compared to other preamplifiers [10].

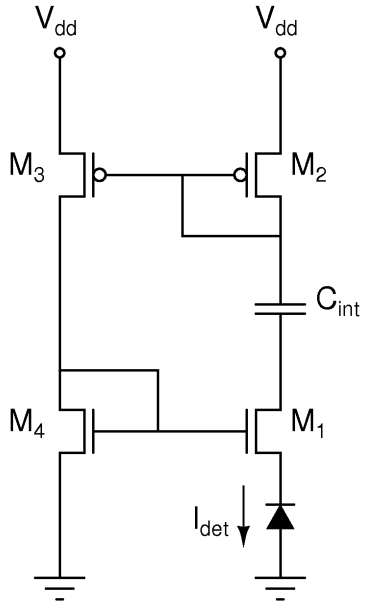


Figure 2.8: Current mirroring direct injection topology.

2.2.5.4 Current Mirroring Integration

Current mirroring integration (CMI) unit cell has off pixel integration capacitor unlike CMDI unit cell. Also CMI has even better injection efficiency along with almost rail to rail dynamic range than CMDI unit cell.

Unfortunately, the noise performance of the CMI unit cell is not superior to CMDI unit cell, it serves even poor performance than CMDI because of effects of current mirrors.

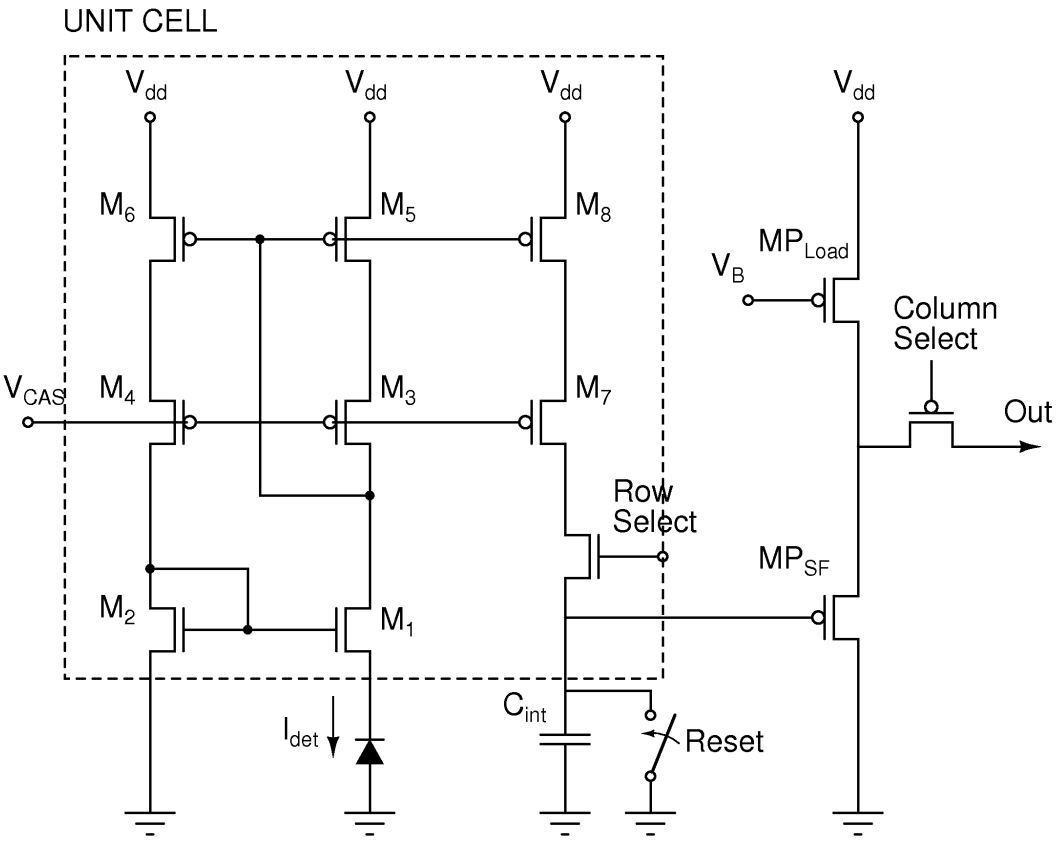


Figure 2.9: Current mirroring integration topology.

2.2.6 Comparison of Preamplifiers

Preamplifiers are most essential part of ROICs, it converts integrated input photocurrent to voltage. There are a lot of topologies available in literature. Their usage and selection in ROICs depends on some parameters such as application and detector properties (impedance,

type, capacitance). Also, their properties such as size, power consumption, dynamic range, bias stability and noise determine their application areas.

Inside discussed preamplifiers DI has smallest area and lowest power consumption. DI can be used with in pixel integration capacitor. Also, DI provides best choice for noise performance along with good detector voltage stability. Its injection efficiency is high but only for high impedance detectors. When detector impedance is high and noise is very critical for application DI is the best choice. Due to small area and low power it is also best choice for big arrays with small pixel sizes.

BDI preamplifier provides solution for injection efficiency of DI unit cell by adding feed forward inverting amplifier at the input. With this topology, designer suffer from high power consumption, large area and additional noise components come from inverting amplifier.

CTIA is very popular widely used preamplifier topology and it has wide range of application area. This topology provides highly stable detector bias, wide dynamic range, high gain and moderate power. Noise performance is not better than DI but it is comparable. CTIA within pixel CDS usage further improves noise performance.

RL unit cell is used in high background applications due to its nonlinear operation characteristics. Its drawback is noise due to the device mismatches over the FPA.

In CM unit cell resistor is replaced by MOSFET to make it linear. However it is also suffers process variations like RL unit cell. Threshold voltage variations and geometry variations of MOSFETs creates additional noise and reduces injection efficiency.

CMDI unit cell achieves 100% injection efficiency along with stable detector bias and reduced input impedance. It achieves this performance by using current mirrors. Again due to current mirrors this topology suffers from high noise.

CMI is similar to CMDI preamplifier, but it uses off pixel integration capacitor and cascade current mirror structures. Its efficiency even better than CMI and it has rail to rail dynamic range as opposed to CMDI but noise issues remain same as in CMDI preamplifier.

Cell	Input Impedance	Detector Bias Stability	Size	Input Referred Noise	Applications
SFD	Self integrator	Not stable, changes during integration	Small, 3 transistors	Moderate, Depends on source follower	Astronomy and Visible Spectrum
DI	$1/g_m$	Not stable, changes during integration (10-50mV)	Small, only 1 transistor	Low, depends on single MOS	Terrestrial IR Applications
BDI	$1/g_m x (1+A_v)$	Stable, controlled by op-amp feedback	Large, due to in pixel amplifier and integration capacitor	Moderate, Depends on amplifier noise	Space IR Applications, Replaced by CTIA
CTIA	Self integrator	Stable, controlled by op-amp feedback	Large, due to in pixel amplifier and integration capacitor	Moderate, Depends on amplifier noise	Space IR Applications

Table 2.1: A comparison of leading preamplifiers in terms of input impedance, detector bias stability, size and input referred noise with applications, where A_v is the amplifier gain, γ is as given in equation 2.8 and g_m is the transconductance [4].

Cell	Input Impedance	Detector Bias Stability	Size	Input Referred Noise
RL	Load resistor	Not stable, depends on photocurrent	Large due to in pixel resistor and capacitor	Moderate, Depends on resistor
CM	$1/g_m$	Stable, controlled by current mirrors	Large due in pixel capacitor	Moderate, depends on current mirrors
CMDI	$1-\gamma / g_m$	Stable (1-2.5mV)	Large due to in pixel integration capacitor and four transistors	High due to current mirrors
CMI	$1-\gamma / g_m$	Stable (1-2.5mV)	Small,9 transistors but off-pixel integration capacitor	High due to current mirrors

Table 2.2: A comparison of other preamplifiers in terms of input impedance, detector bias stability, size and input referred noise, where A_v is the amplifier gain, γ is as given in equation 2.8 and g_m is the transconductance [11].

2.3 Noise Suppression Methods

Correlated double sampling and time delay integration methods will be examined in this section.

2.3.1 Correlated Double Sampling

Correlated Double Sampling (CDS) is a analog circuit method used in focal plane arrays for reducing noise components. Idea behind technique is sampling the output twice. First right after reset and second with integrated signal, and taking difference between two values offset and noise are eliminated. Eliminated noise components are low frequency noises such as 1/f, and drift noise in expense high frequency noise components are increased [12].

Following circuit in Fig. 2.10 shows CDS implementation after source follower per detector (SFD) preamplifier stage. After read operation is done M_{reset} switch initializes C_g node. During switching activity of reset switch, kTC switching noise is created. This noise stored in the C_{clamp} capacitor. After reset following operation is read operation. In this mode, integrated charges transferred to sample and hold circuit without noise components that are already captured by clamp capacitor (C_{clamp}) in reset operation. Also offset can be subtracted by adjusting V_{clamp} value.

CDS can be implemented not only in chip but also in digitally outside of the chip. This requires sampling of noise of reset switch and integrated photocurrent. After sampling these two samples are subtracted digitally.

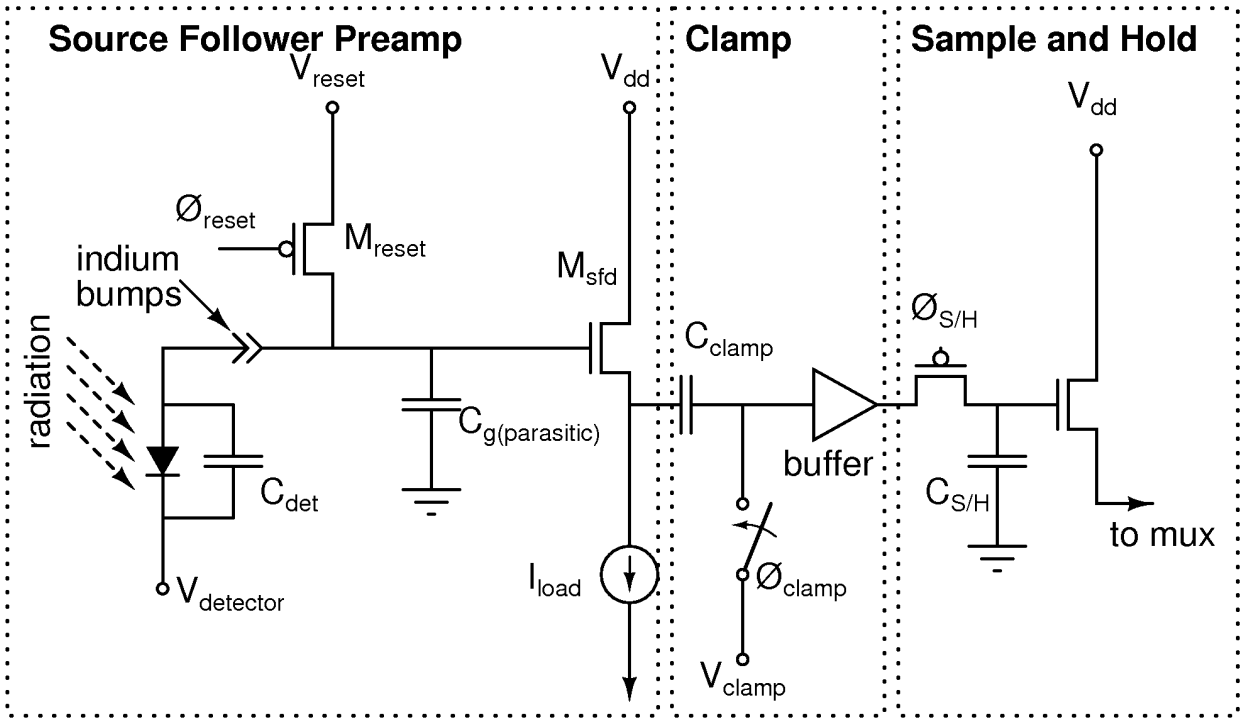


Figure 2.10: Source follower preamplifier with correlated double sampling [9].

2.3.2 Time Delay Integration

Like CDS, time delay integration (TDI) is another analog circuit method for reducing noise and improving signal level, in other words TDI improves SNR of the signal. In ROIC, TDI technique is used for scanning type of detectors. In scanning type of FPA, there is only one column of detector element. In order to construct full scene, array is scanned optically from one side to other side of the field of view.

If another column of detector array establishes next to first array, this new array will also construct full image with a time difference Δt with respect to first array. If these two signals combined together to construct same full scene, it results SNR improvement on the constructed image. In other words, TDI means getting and integrating same exact information from different pixels with a time difference. For N detector array SNR improvement becomes $\sqrt{N}$ because noise is added by power unlike signal [2].

TDI technique can be explained by following formulations. There will be a Δt time delay between subsequent pixel arrays. If there is n subsequent pixels arrays, n represents number of TDI pixel element. Total voltage signal of N pixels is calculated as given in equation [5].

$$V_{total} = \sum_{i=1}^{n} v_i (t1 + (i-1) * \Delta t) \tag{2.10}$$

In which V_i is the voltage corresponding to the charge accumulated by detector i.

Unlike signal, noise is added by power, given as:

$$V^2{}_{noise\_total} = \sum_{i=1}^{n} v^2{}_{noise\_i} (t1 + (i-1) * \Delta t) \tag{2.11}$$

Where V_{noise_i} is the voltage corresponding to the noise accumulated by detector i.

As a result total SNR improvement is calculated as given,

$$S/N = \frac{v_{total}}{v_{noise\_total}} = \sqrt{N}(S/N) \tag{2.12}$$

N represents pixel elements in each row. For instance, if there is a 7 detector element in each row, TDI algorithm improves SNR ratio to $\sqrt{7} \approx 2.64$ times.

TDI can be implemented off FPA and on the ROIC. Off chip implementation can be realized combining all detector information digitally. For on chip implementation CCD is most common way of implementation platform for TDI. CDD transports charge from one to next element by accumulation. Then accumulated signal transferred to output buffer.

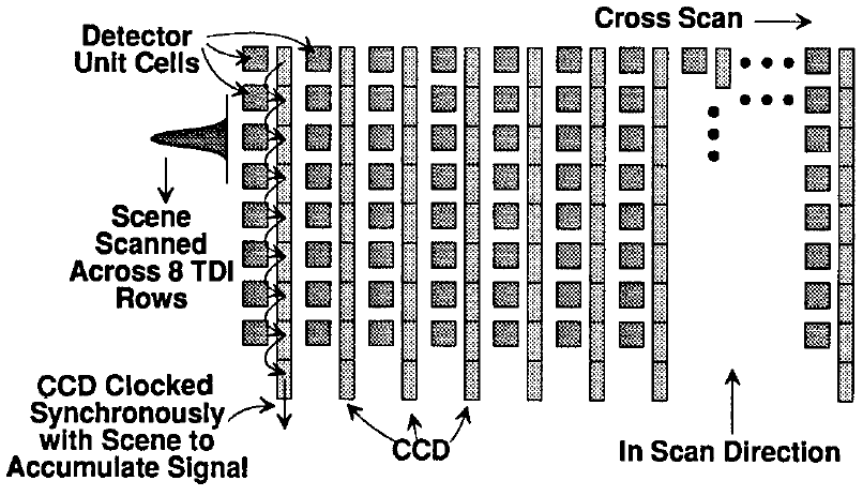


Figure 2.11: TDI implementation on CCD array [6].

For CMOS case, it is not easy task to perform TDI because on the fly integration and accumulation is not possible like CCD. In order to apply TDI, each pixel information is to be stored on separately then it is accumulated. At the same time it is also essential to keep next incoming information and store it separately from previous one. As observed from figure below in a case of 7 detectors for basic TDI implementation at least 28 storage is needed.

In the Fig. 2.12 object (O_1) is scanning from D1 to D7 direction. D1 is the first detector encounter with object, D7 is the last detector. D7 is associated with just one storage element because after D7 all information that obtained from 7 detectors will be accumulated. Likewise, D1 has 7 storage elements and all the way down to D7, D1 will be encounter 6 new objects. Thus, in order to store 6 new information and information of O_1 D1 has to have 7 storage elements.

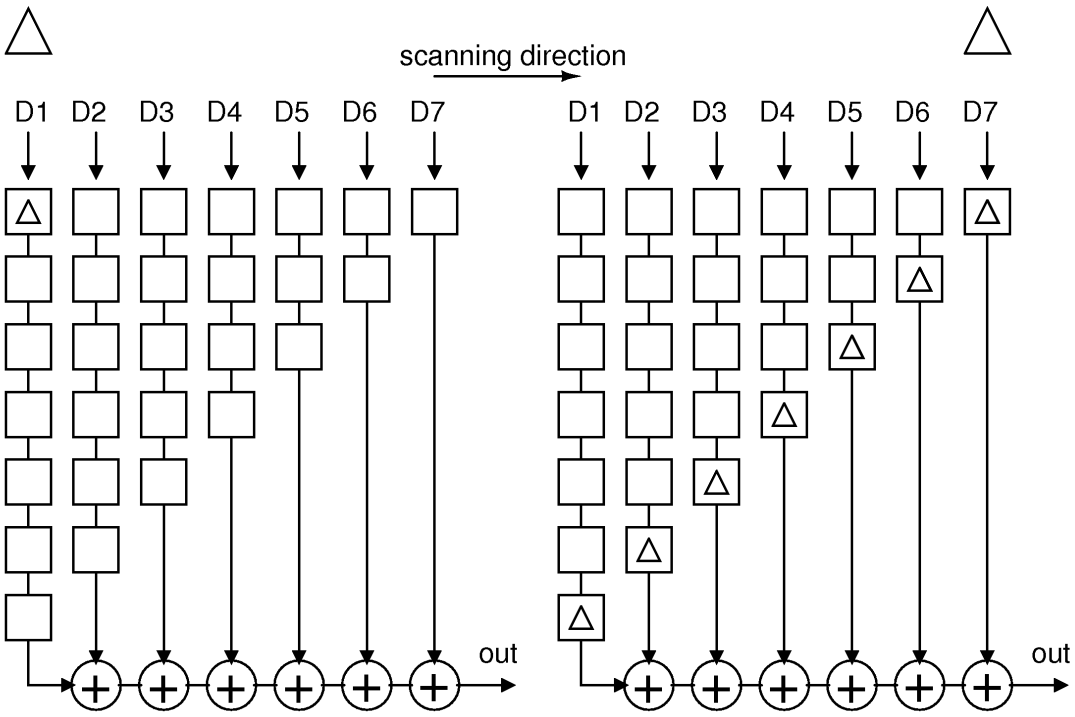


Figure 2.12: Storing information to apply TDI when object is moving from D1 to D7 [13].

Another property associated with TDI is supersampling. In this ROIC and TDI concept, supersampling means to obtain extra information from detector when object is located at intermediate nodes. Object moves only in one step from one detector to another in the case of TDI with no supersampling. If there is a supersampling, when object is moving from one to another detector, more than one information is captured. These information need to be stored separately. The main purpose of using sumpersampling is to increase the spatial resolution of the image.

Fig. 2.13 shows example of differences between supersampled TDI and non-supersampled TDI. This example shows the case of TDI over 3 elements and sumpersampling rate of 3 with TDI over 3 elements.

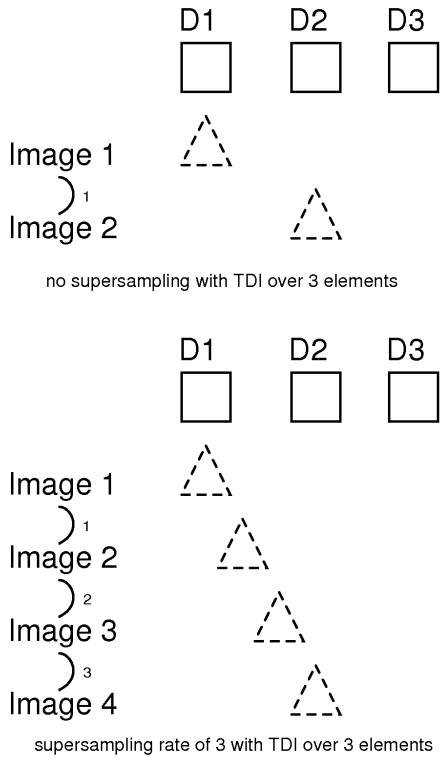


Figure 2.13: TDI with no supersampling vs TDI with supersampling rate of three.

As it is shown in top figure above, for the first image data the stored data at frame 1 of first detector, the stored data at frame 2 of second detector, the stored data at frame 3 of third detector should be summed up. The formula showing this is given in equation 2.13 [13].

$$I1 = D1 \text{ (image frame } i) + D2 \text{ (image frame } i+1) + D3 \text{ (image frame } i+2) \quad (2.13)$$

For instance, if the supersampling rate of three applied to TDI. The formula of first image with TDI over three elements with an optical supersampling rate of three is given in equation 2.14 [13].

$$I1 = D1 \text{ (image frame } i) + D2 \text{ (image frame } i+3) + D3 \text{ (image frame } i+6) \quad (2.14)$$

Because of supersampling more storage elements needed in the ROIC. In order to apply TDI over 7 elements with supersampling rate of 3, 77 storage elements needed as seen from Fig. 2.14.

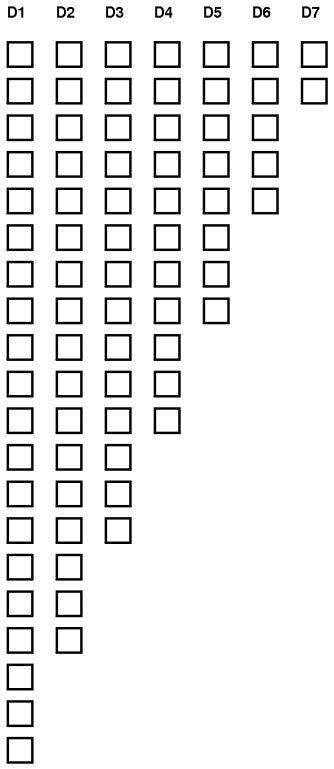


Figure 2.14: Number of TDI capacitors for TDI over seven 7 elements.

In CMOS architecture there are two common methods to implement TDI functionality. First method is using single big capaity storage to handle integrated charges by detectors and second method is using a lot of small storages than integrate charges. Both method have some advantages and disadvantages, First method requires lots of integrators and this means high power consumption. Second method requires lots of storages like stated before for TDI over 7 elements and supersampling rate of 3 requires 77 storage devices. These storage devices are capacitors. Capacitors cover a lot of area, for typical process unit capacitance per area is $0.96 fF/\mu m^2$. Thus, ROIC with TDI design turns out to be capacitor dominated circuit.

In Fig. 2.15, TDI with four detectors and supersampling rate of three based on first architecture is shown. As observed from figure, there are 12 integrators which have capable of store and add feature at the same time. Because, first design approach requires simultaneous read and integration options. 10 of these storages are store during the delay, one is needed for integration while read operation and one is used for storage during resetting. At frame i, D1 is integrating, at frame i+3 D1 and D2 are added, at frame i+6 D1, D2 and D3 are added and at frame i+9 D1, D2, D3 and D4 are all summed. I +10 is when read operation is

done. At frame i+11 resetting of the integrator occurs [16]. The process is continuously repeated for every integrator.

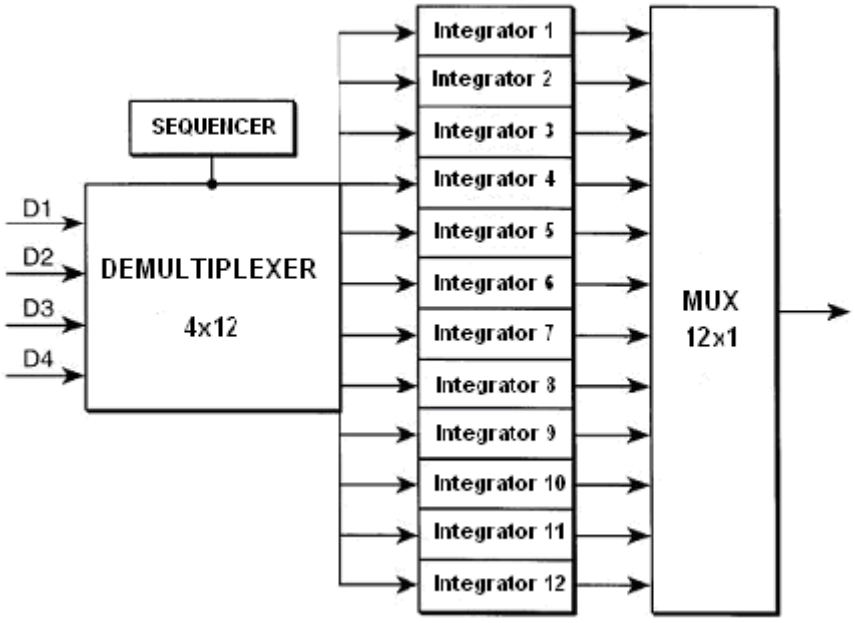


Figure 2.15: TDI architecture with use of 12 integrators [13].

Power consumption hungry part of this topology is integrators. Generally, integrators implemented based on op-amp architecture that requires a lot of power to operate and they produce heat. Also, it is most likely to have mismatches between integrators based on threshold variations or geometrical variations. These mismatches effect linearity of read out circuit since there will be variations between outputs of different integrator even they integrate same charges.

Second architectural approach requires mores capacitors than integrators. Unlike first one, this approach requires only one integrator. This reduces power consumption and increases linearity of TDI process. On the other hand, this architecture requires more capacitors. In CMOS process more capacitor means more area. There are MOS capacitors that have more capacitance density but MOS capacitors are not linear in operation. There will be 26 capacitors required for TDI over 4 elements with supersampling rate of 3. Architecture of second approach can be found in Fig. 2.16.

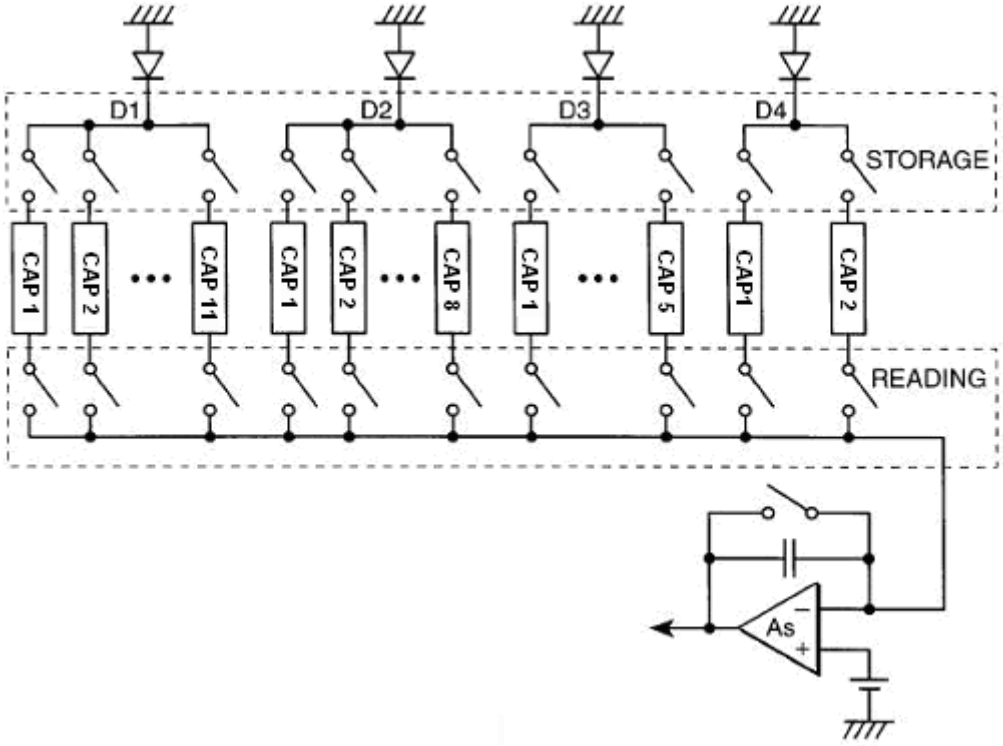


Figure 2.16: TDI architecture of second approach [13].

Capacitors that have a set of switches to realize variable gains, in which the switches are transmission gates. In this architecture, switches connect the two terminals of the capacitors to same potential forcing the integrated charge to move to output capacitor. A rising ramp is observed at the output, as the charge is transferred. Following every charge transfer, a reset operation is required to initialize the storage capacitor. This one integrator solution brings low power and linear operation for advantage over first approach. The cost of second approach is 26 storage capacitors compared to 12 storage capacitors. Choice of topology is depended on trade off between area linearity and power consumption.

Alternative to these methods another third TDI approach to integrating and storing photo current is using current memories. Current memory structures composed of only transistors. Thus it requires much less area than capacitors. Also integration operation doesn't need power hungry op-amps, it can be achieved with simple switching's. Integration operation is also very linear. To sum up, this method requires less area and consumes low power by linearly integrating and storing photo currents.

Basic current memory cell shown in Fig. 2.17 first reported at [14]. It consists of pair of MOSFETs connected as current mirrors with a switch between the gates. The current is

sampled by charge stored in the gate-source capacitance of M2. Current sources are needed to keep bias transistors in saturation. Termination circuit required to eliminate sampling errors. Instead of current sources simple transistors can be replaced.

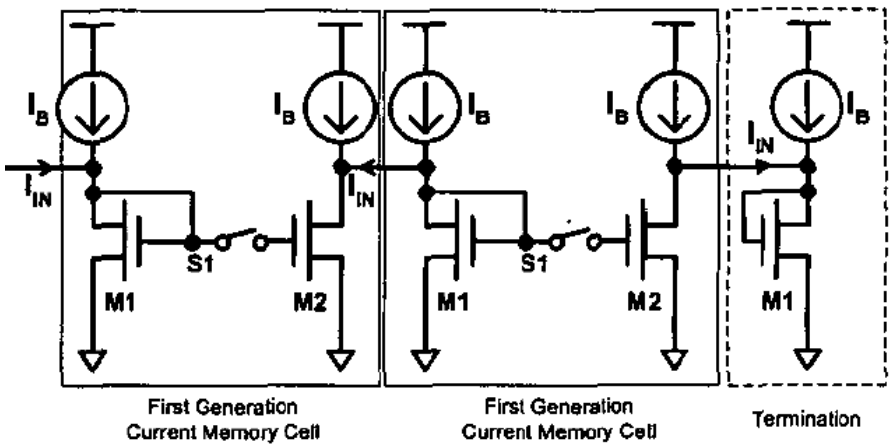


Figure 2.17: Basic current memory architecture [14].

Fig. 2.18 shows core structure of current memory based TDI circuit. This circuit can be divided into two parts one is input stage, other one memory state. Input stage captures input current and stores it inside M_2 transistor, after that captured current will be transferred to memory part. Memory transistors stores current value. If another current comes to circuit, again input stage captures it and transfers it to second memory stage. New current will be added on old current already stored in memory stage.

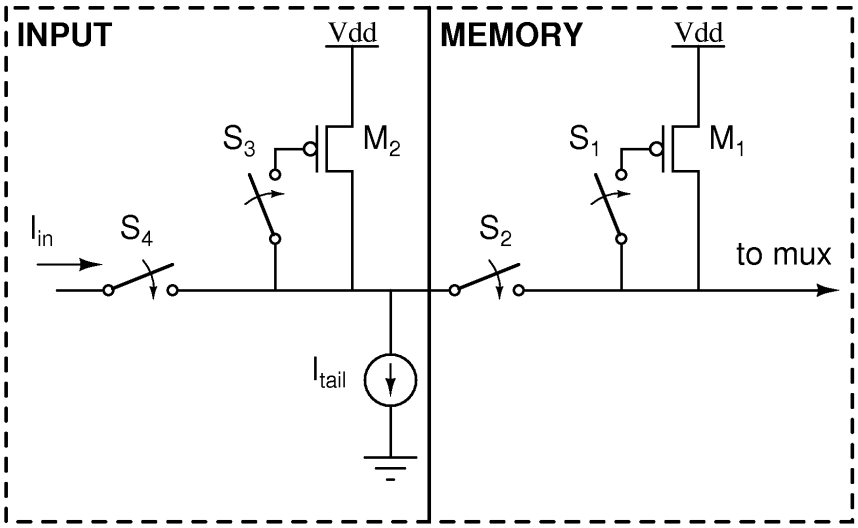


Figure 2.18: Basic TDI elements of third approach.

Fig. 2.19 demonstrates how input and memory stages used to implemented together to make TDI is possible

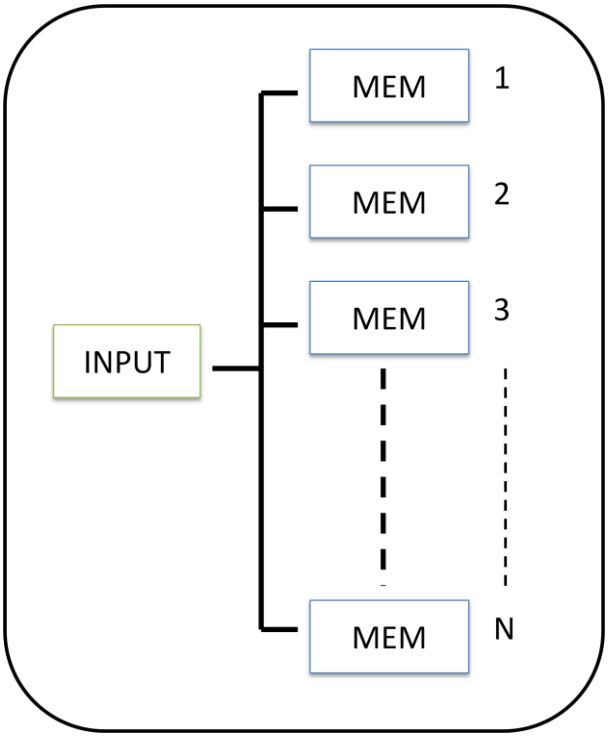


Figure 2.19: TDI architecture of third approach with input and memory elements.

For TDI over seven with supersampling rate of three, 21 memory blocks used. After each frame, detector information will be written on appropriate places according to position of object. This decision is made by digital block, hence digital block controls switches inside TDI.

3 576x7 P-on-N ROIC IMPLEMENTATION

3.1 ROIC Definition and Requirements

As a fundamental step for 576x7 ROIC firstly a 6x7 P-on-N type ROIC is fabricated for testing purposes in Austria Microsystems (AMS) 0.35 µm, 4 metal (1 top metal), 2 poly CMOS process. After measurements will be done 72x7 are going to be designed as a building block of 576x7, by just increasing analog channels of 6x7 ROIC. Because, 576x7 ROIC is composed of eight 72x7 ROICs. Detector is P-on-N type Mercury Cadmium Telluride (HgCdTe - MCT) detectors which are sensitive to long wave infrared radiation (LWIR) between 7.7 and 10.3 µm. In the complete detector system, there are 576 lines, each of them consisting of 7 detectors. These 576 lines consist of 8 blocks (72x7 ROIC) (2x4 matrix) of 72 lines in Fig. 3.1.

Total detector width is 532 µm while length is 11530 µm. Each detector pixel's size is 20 x 30 µm. The separation between the center of the last pixel of first set and first pixel of second set is 108 µm. All measures are shown in shown in Fig. 3.1.

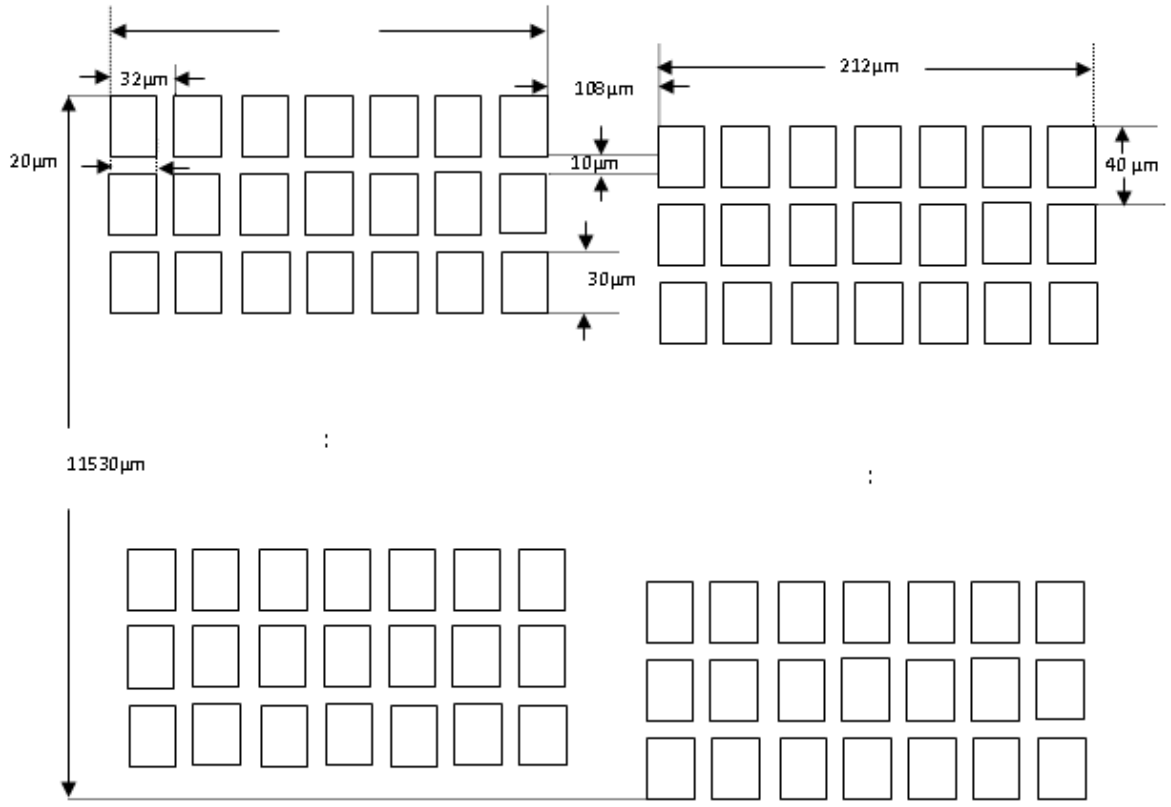


Figure 3.1: Geometry of detector array on FPA.

Output frequency of the ROIC is 1 MHz. The ROIC implements bidirectional TDI scanning over 7 elements for signal processing with an oversampling rate of 3. Detailed additional ROIC requirements and features are listed below. All features will be given based on 72x7 ROIC because it is building block of final 576x7 ROIC.

Input Requirements

Minimum detector input impedance is 1MΩ. Input current range is 1 – 50nA. Nominal current value is 10nA at 293 K background.

ROIC Features

- Integration period adjustment
- Multi-gain adjustment (1, 0.9, 0.5, 0.4, 0.3)
- Bidirectionality of TDI scanning
- Pixel select/deselect option with automatic gain adjustment
- Bypass property
- Parallel/Serial programmability

Output Requirements

Dynamic range of ROIC output is 3.75 V and the output voltage at zero irradiance should be 1.25 V, so that maximum output voltage is 5 V. The output should be ready within first 100 ns of the frame to be sampled by an off-chip ADC. ROIC output should drive a 15 pF capacitance with a 1 MΩ shunt resistance.

Noise Requirements

Maximum allowed input referred noise level is 1000 rms electrons.

Power Consumption Requirements

Maximum allowed power consumption of ROIC is 100 mW.

3.2 ROIC Architecture

The 72x7 P-on-N ROIC consists of 72 channels for 7 detectors in each channel, which are connected to a 72x1 multiplexer. In each cycle, one of the channel outputs is sent to the output

to be received by an off-chip ADC. General architecture of the 72x7 ROIC is shown in Fig.3.2.

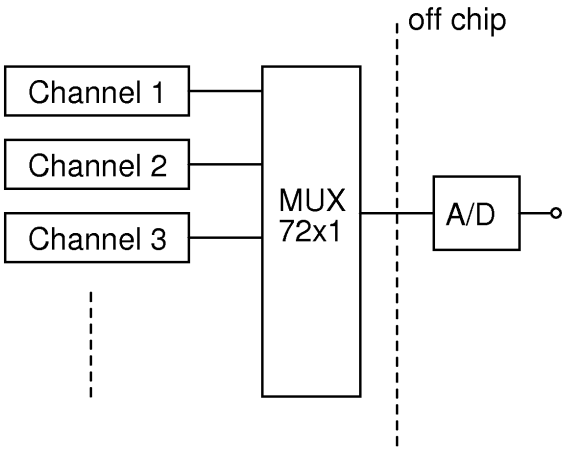


Figure 3.2: ROIC architecture.

The detailed architecture of the 72x7 ROIC is given Fig. 3.3. The interface circuit, digital control block, channel select decoder and address decoder constitute the digital part of the ROIC. Digital part controls the analog part, which consists of input stage, gain controls, TDI stage and output buffer stage inside each channel and total of 72 channels.

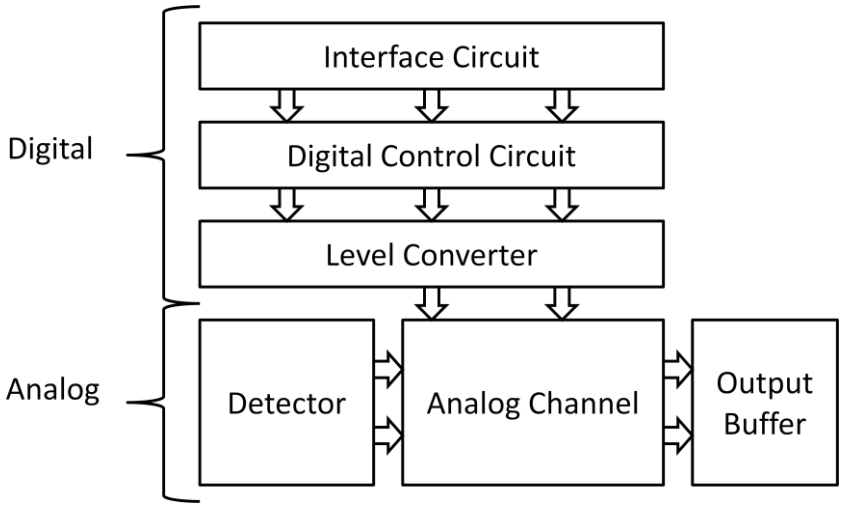


Figure 3.3: Detailed ROIC architecture.

Each of the 72 channels have its own TDI memory, voltage to current converter, and 7 unit cells for 7 detector pixels. The channel architecture is shown in Fig. 3.4.

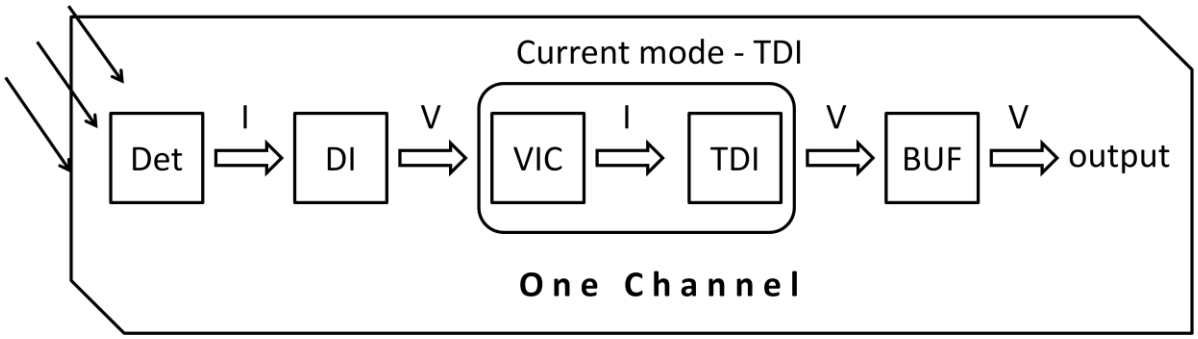


Figure 3.4: Block diagram of analog channel.

In Fig. 3.4 abbreviations are as follows; Det: detector, DI: direct injection, VIC: voltage to current converter, TDI: time delay integration, BUF: buffer, V: voltage domain, I: current domain.

3.3 ROIC Implementation

The ROIC building blocks are unit cell with gain adjustment, voltage to current converter (VIC), TDI stage , and the output buffer stage. The CMI unit cell as the unit cell architecture is implemented for P-on-N type ROIC.

In the input stage direct injection (DI) topology applied with At TDI stage, the third approach mentioned in section 2.3, current mode TDI, is implemented.

3.3.1 Input Stages

Unit cell and integration capacitor stage constitute the input stages of ROIC. DI unit cell is used as the unit cell architecture of the ROIC.

3.3.1.1 Preamplifier Design

Various input cells are discussed in previous sections from most popular ones to other topologies that are designed for specific areas. Preamplifiers were compared according to their linearity, output noise, power consumption and detector bias stability. According to the system and requirements designer should carefully choose one of the topologies.

In this, 72x7 ROIC, DI preamplifier is used. The reason to choose DI preamplifier is based on the requirements specified in section 3.2. First of all, DI has superior noise performance over other preamplifier topologies. Second, DI unit cell consumes very low power and fits very small area that enables to fit just under the detector pixel in order to save area and reduce

parasitic and noise. Only drawback is injection efficiency. If detector with high R_0A is used, efficiency of DI very high (≥95%). If R_0A value of detector is low, efficiency drops significantly. Moreover, efficiency is sensitive with photocurrent value. High photocurrent increases efficiency. For low photocurrents values R_0A is around 10 and efficiency is around 15%. For typical conditions, R_0A is around 100 and efficiency is around 50%. These efficiency changes can be easily compensated off the chip with signal processing. Nevertheless, for this application of FPA, primarily choice of DI unit cell topology is its noise performance. For comparison CMI unit cell has a noise level of $414e^-$, while DI unit cell has a significant lower noise level of $69e^-$. [11]

DI unit cell is composed of only two transistors one is injection transistor other one is reset transistor. Basic DI preamplifier stage which is shown in Fig. 3.5 discussed in detail at section 2.2.2.

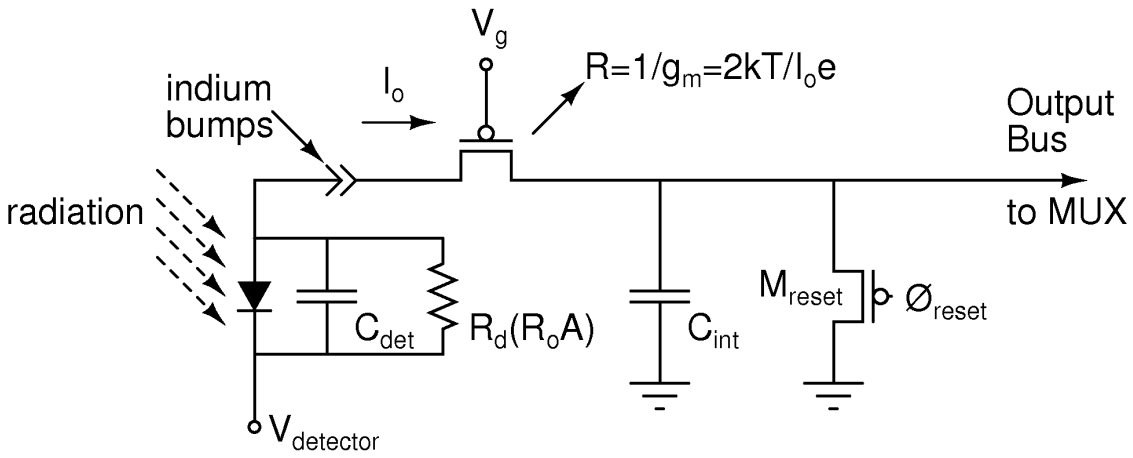


Figure 3.5: Direct injection preamplifier.

Fig. 3.6 demonstrates applied DI unit cell architecture in the ROIC system. DI cell has 4 capacitors to switch between 5 gain modes. Photocurrent charge stored in these capacitors is converted to voltage with simple source follower architecture. Source follower follows its input voltage with threshold difference. Because of its simplicity its noise performance is better than any more complex amplifier.

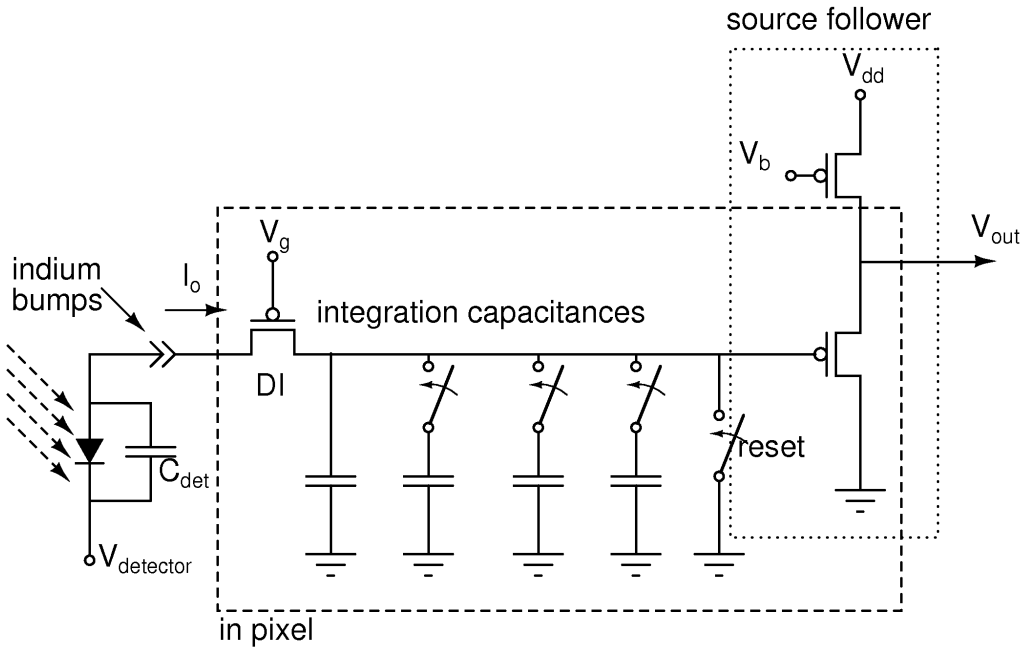


Figure 3.6: Schematic of CMI unit cell. The last stage is off-pixel, V_m and V_{bias} is carried through the ROIC to regenerate photocurrent near the integration capacitors.

3.3.1.2 In pixel Input Capacitors

In CMOS process, it is very common to use MOS capacitor due to high unit capacitance. However, MOS capacitors are nonlinear, or linear at a very limited range. In AMS 0.35µ process, there are available poly capacitors with a 0.96fF/μm^2 capacitance per area. These poly capacitors are very linear with high dynamic range. There are five gain settings of ROIC as given in Table 3.1. For a dynamic range of 3.75V, stored charge is given as well.

GAIN	Equivalent Active Capacitance C_{int} (pF)	Storage Capacitance (pC)	Gain Ratio
0	0.064	0.24	1.00
1	0.072	0.27	0.9

2	0.128	0.48	0.5
3	0.160	0.6	0.4
4	0.213	0.8	0.3

Table 3.1: Gain settings and ratios.

To obtain capacitance values as in the table above 8, 56, 64 and 85fF poly capacitors are added by switches. For unity gain 64fF capacitor is used primarily. Combinations of other capacitors are able to generate other gains. Gain setting switches are controlled by digital circuitry.

3.3.2 Implementation of TDI Stage

In this system, TDI topology that discussed as third topology in section 2.3.2 is used. This topology based on current switches and current memories. Integration of currents is done by switches. Thus, this architecture covers less area and consumes less power than conventional capacitor and integrator OTA based topology. Also, this particular TDI topology brings high linearity in comparison with other topology. Since this TDI topology is based on current domain integration there will be need for a voltage to current converter because after at the end of input stage source follower output is in the voltage domain.

Fig. 3.7 shows core structure of current memory based TDI circuit. As seen from figure there are two parts of the circuit; input stage and memory stage. Input stage captures input current and stores it inside M_2 transistor, captured current will be transferred to memory part. Memory transistors store current value I_{in}. If another current comes to circuit, again input stage captures it and transfers it to second memory stage. New current will be added on old current already stored in memory stage.

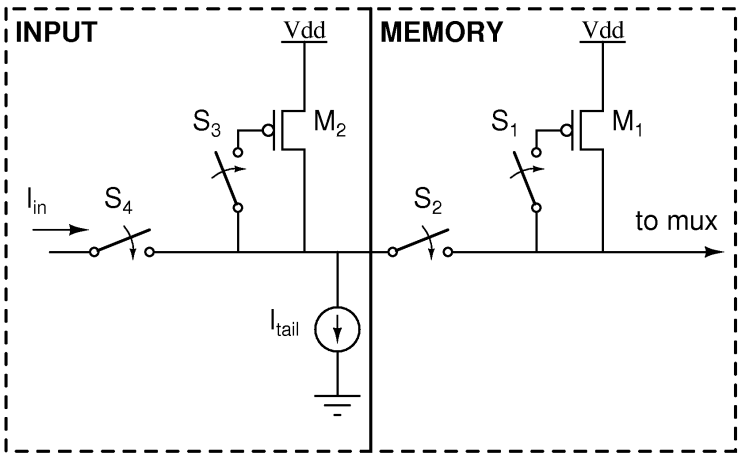


Figure 3.7: Current mode TDI architecture.

Current mode TDI function implemented in this ROIC can be explained in three steps:

First one is reset stage, in this stage S_4, $S_3$and S_1 switches are closed and S_4 is open. There is no incoming current to TDI stage since S4 is open. I_{m2} and I_{m1} equal to each other (M_1 and M_2 are same size) and sum of two is equal to I_{tail} current. This resets I_{m2} and I_{m2} currents to same value.

$$I_{m2(0)} + I_{m1(0)} = I_{tail} \tag{2.15}$$

Secondly, S_4 is closed and S_1 is opened. Since S_1 is opened, I_{m1} current stays same. S_3 is still closed, I_{m2} current lowers as I_{in} current to keep I_{tail} current constant.

$$\begin{aligned} I_{m2(1)} &= I_{m2(0)} - I_{in} \\ I_{m1(0)} &= I_{m1(0)} \end{aligned} \tag{2.16}$$

Finally, I_{in} is captured already by M_2 and this final stage is holding stage. S_3 and S_4 is open, S_1 is closed. I_{m2} couldn't change its value (S3 open). Sum of I_{m2} plus I_{m1} should be I_{tail}. In order to keep total current I_{tail} level, I_{m1} increases I_{in} times since I_{m2} is constant. New I_{in} becomes as formulated below. This explains one cycle of operation.

$$\begin{aligned} I_{m2(1)} &= I_{m2(0)} - I_{in} \\ I_{m1(1)} &= I_{m1(0)} + I_{in} \end{aligned} \tag{2.17}$$

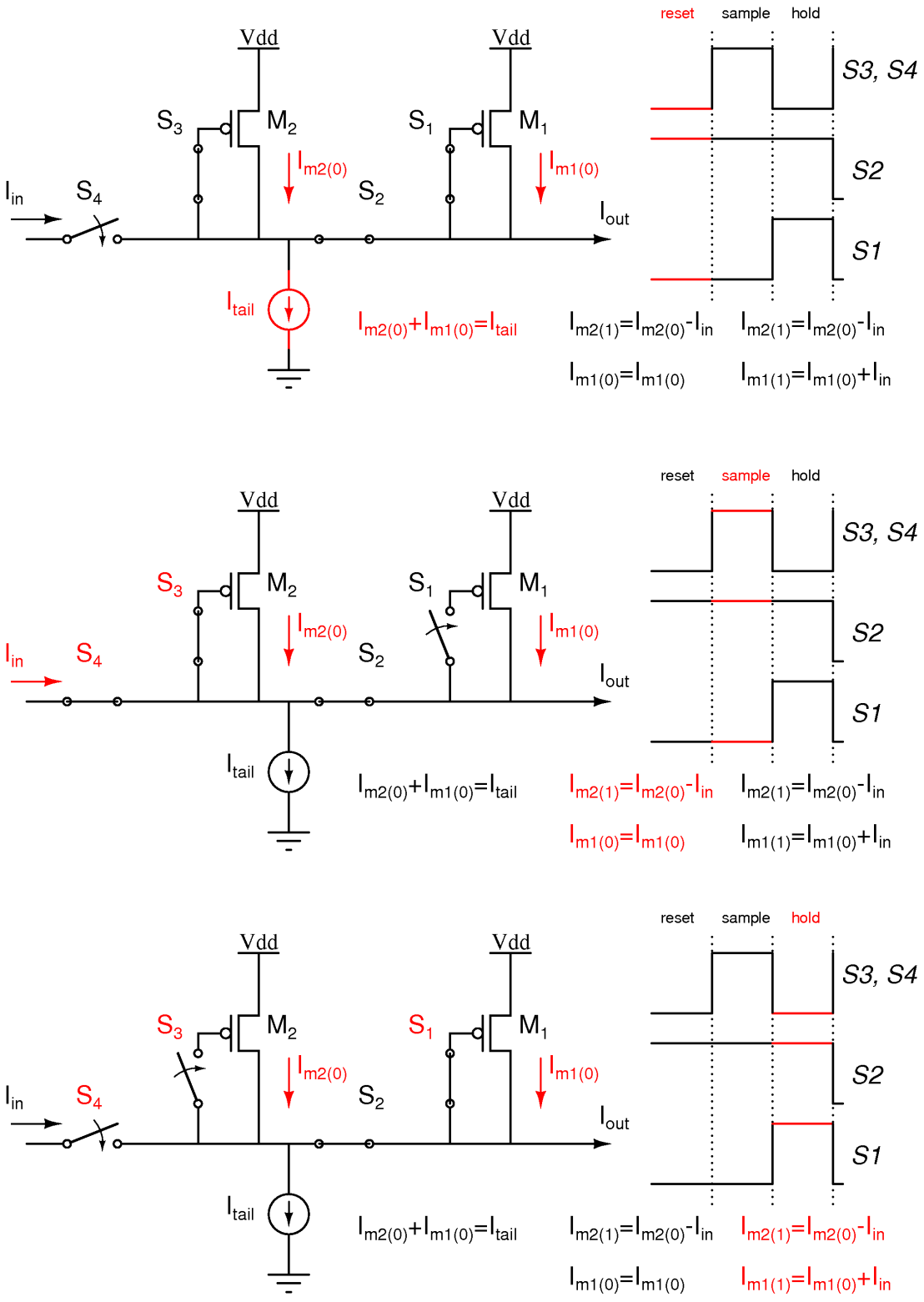


Figure 3.8: Operation of TDI circuit.

After n^{th} cycle, current in the memory becomes;

$$I_{Mn} = I_{M0} + \sum_{k=1}^{n} I_{in(k)} \tag{2.18}$$

This makes integration operation is linear with some offset.

Fig. 3.9 demonstrates how input and memory stages implemented together to make TDI is possible. Only one input stage is used for all memories to save power consumption rather than using input stage for all memories.

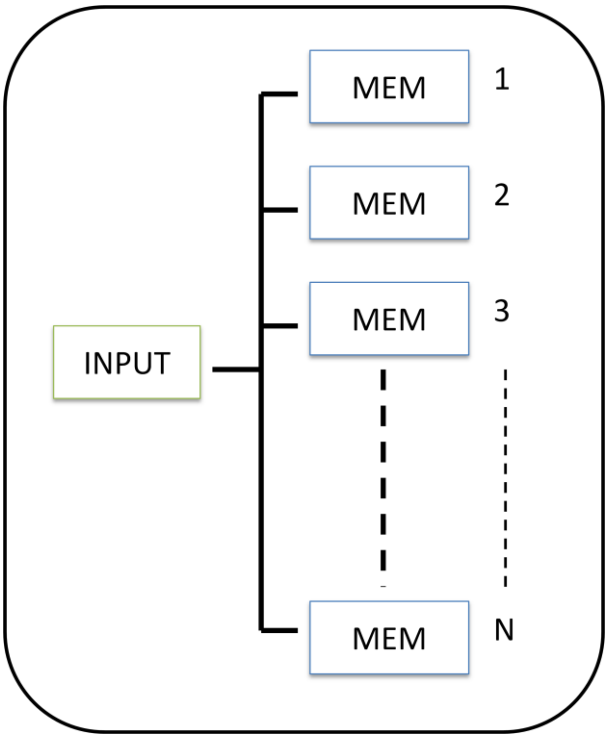


Figure 3.9: Block diagram TDI section.

For TDI over seven element with supersampling rate of three, 21 memory blocks used. After each frame, detector information will be written on appropriate places according to position of object. This decision is made by digital block, hence digital block controls switches inside TDI.

Fig. 3.10 shows how objects written in memory blocks. A-H are different objects, numbers are different positions of objects according to supersampling rate of 3 there is 3 different positions of objects. When object moves from one to another adjacent detector it moves in three steps. Each step is stored in the memory. Figure a) demonstrates detector vs frames. Figure b) shows memories and written information at each frame.

This table filled from t=0 time with empty memory. In the first frame objects are A-G, A will be scanned through by all detectors thus first meaningful information will be acquired from A than H to M. B-G are not going to be meaningful since they won't be scanned from all 7 detectors. Then from B-G these outputs first dummy outputs from this point all outputs are meaningful. As seen from table first meaningful information acquired from MEM1, MEM8 and MEM15 as A objects' supersampled information. Then next output will be from MEM7, MEM14 and MEM21. After that, next output will be read from MEM6, MEM13 and MEM20. As observed from table, output direction is backwards, for 1st supersampled MEM7 to MEM1, for 2nd MEM14 to MEM8 and for 3rd MEM21 to MEM15.

Detectors

	1	2	3	4	5	6	7
D1	A	H	I	J	K	L	M
D2	B	A	H	I	J	K	L
D3	C	B	A	H	I	J	K
D4	D	C	B	A	H	I	J
D5	E	D	C	B	A	H	I
D6	F	E	D	C	B	A	H
D7	G	F	E	D	C	B	A
		G	F	E	D	C	B
			G	F	E	D	C
				G	F	E	D
					G	F	E
						G	F
							G

MEMORY	1	2	3	4	5	6	7
MEM1	A1	A1	A1	A1	A1	A1	A1
MEM2	B1	B1	B1	B1	B1	B1	M1
MEM3	C1	C1	C1	C1	C1	L1	L1
MEM4	D1	D1	D1	D1	K1	K1	K1
MEM5	E1	E1	E1	J1	J1	J1	J1
MEM6	F1	F1	I1	I1	I1	I1	I1
MEM7	G1	H1	H1	H1	H1	H1	H1
MEM8	A2	A2	A2	A2	A2	A2	A2
MEM9	B2	B2	B2	B2	B2	B2	M2
MEM10	C2	C2	C2	C2	C2	L2	L2
MEM11	D2	D2	D2	D2	K2	K2	K2
MEM12	E2	E2	E2	J2	J2	J2	J2
MEM13	F2	F2	I2	I2	I2	I2	I2
MEM14	G2	H2	H2	H2	H2	H2	H2
MEM15	A3	A3	A3	A3	A3	A3	A3
MEM16	B3	B3	B3	B3	B3	B3	M3
MEM17	C3	C3	C3	C3	C3	L3	L3
MEM18	D3	D3	D3	D3	K3	K3	K3
MEM19	E3	E3	E3	J3	J3	J3	J3
MEM20	F3	F3	I3	I3	I3	I3	I3
MEM21	G3	H3	H3	H3	H3	H3	H3

Figure 3.10: Memory locations of object information on third approach TDI.

This particular TDI topology brings low power consumption along with high linearity and small area. Power consumption of TDI block is dominated with I_{tail} current. Because I_{tail}

current defines total current of TDI stage. This current depends on input current that comes from VIC stage. Because If input current is high I_{tail} should be high to compensate input currents. In our design maximum input current that VIC is converted is 550nA. In order to handle this current 8µA tail current is used. Required tail current can be calculated following basic formulation. After reset cycle tail current is divided between input and memory stages. Half of tail current goes to input stage. In order to handle 7 consecutive input current, stored current inside input stage should be at least 7 times of maximum input current. From this calculation stored current input stage should be 3.85µA for 550nA max input current. So, tail current should be at least 7.7µA. Therefore, in this design tail current is selected as 8µA. For one channel simulated dynamic power consumption is 28µW. For 576 channel 16.128mW power consumption can be calculated. If input current is lowered with different design of VIC or another method power consumption can be reduced more. This novel TDI topology can handle as low as 1nA input current. This means power consumption can be reduced even more as compared to 550nA input current.

3.3.3 Voltage to Current Converter

Voltage to current converter (VIC) architecture is an essential part of the current mode TDI system. Because, VIC provides current input for TDI stage. VIC designed with basic flipped voltage follower (FVF) block.

Flipped voltage follower is similar to typical voltage follower configuration but it has some advantageous over it. Basic voltage follower is able to sink large current from the load but sourcing capability is limited. It has less than one gain for large signal voltage. Also, current through transistor is not constant because V_{SG} is not constant [15].

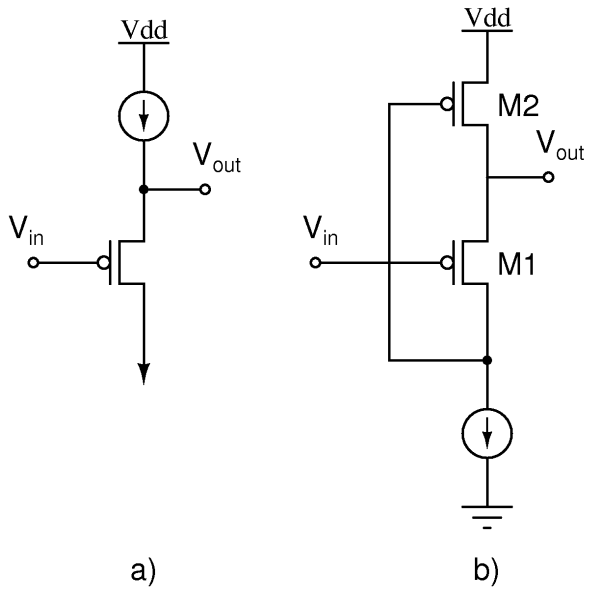


Figure 3.11: a) Conventional source follower, b) flipped voltage follower.

FVF doesn't have this drawbacks of conventional follower. It has high sourcing capability due to low output resistance (r_0) around 20-100Ω. For large signal, it has almost unity gain. Only drawback of this topology is limited dynamic range.

$$r_0 = \frac{1}{g_m{}^{M1} \cdot g_m{}^{M2} \cdot g_m{}^{M2}} \tag{2.19}$$

FVF structure can be used many applications like current mirrors, differential pairs, amplifiers like OTA and output stages. Also, in this system it is used for VIC.

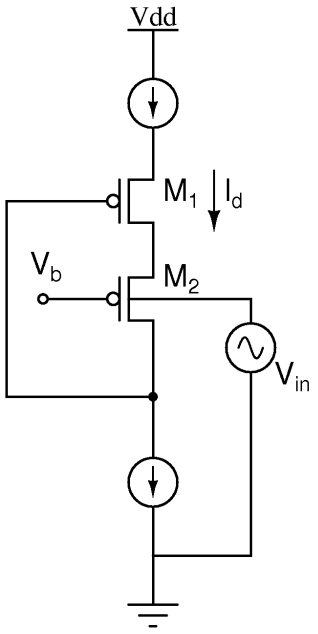


Figure 3.12: FVF based bulk driven linear voltage to current converter.

There is a VIC based on FVF in the literature [16]. In this approach V_{in} applied from source of transistor over R. Unlike this topology in the topology in this system uses bulk-driven approach in Fig. 3.12 [17]. With bulk-driven method linear voltage to current conversion is possible. Bulk driven approach is very ideal than source resistor combination since input current is around 1pA and input capacitance can be around 9fF with bulk driven FVF topology. To further improve VIC performance and its range, circuit can be driven with +5 and -5 symmetric sources.

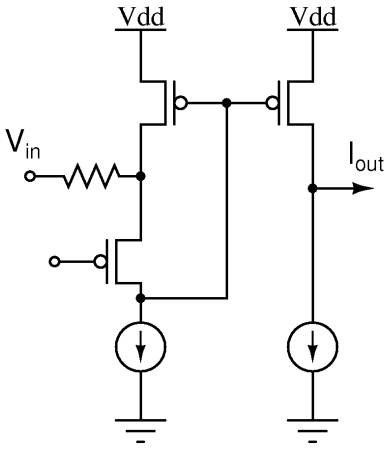


Figure 3.13: Flipped voltage follower based another VIC [16].

3.3.4 Output Buffer Design

Output buffer is designed for a load of 15pF with a shunt resistance of 1MΩ. Required ROIC output response is given in figure. From Figure 3.13, it is known that a 1mV settling error is allowed in 65ns rise time from 1V to 4.8V. High slew rate and good phase margin are required to meet the specifications.

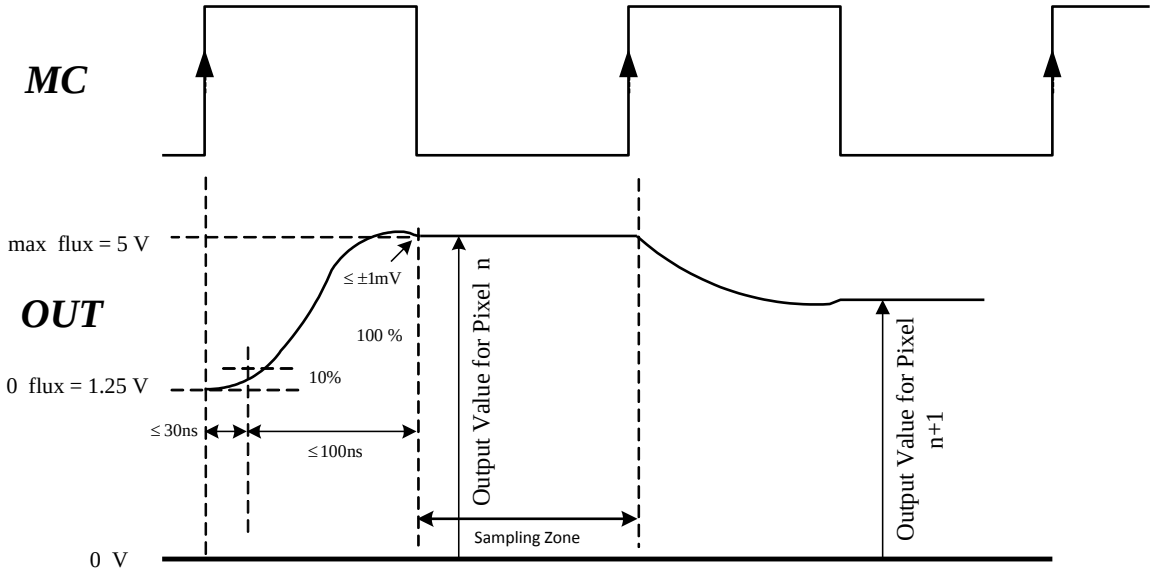


Figure 3.14: Output waveform of buffer.

As the output buffer, a two stage operational transconductance amplifier (OTA) with a differential stage followed by a common source stage is used, with its output connected to its negative input (typical buffer topology for OTA). Designed amplifier has a gain of 49.46 dB with a phase margin of 45 degree. Its power consumption is 6 mW. Slew rate is 60V/μs with the load being 15pF with a shunt resistance of 1MΩ as stated above Fig. 3.14. Each 72x7 block will have one output buffer for 576x7 eight buffer is required and total power consumption will be 24mW.

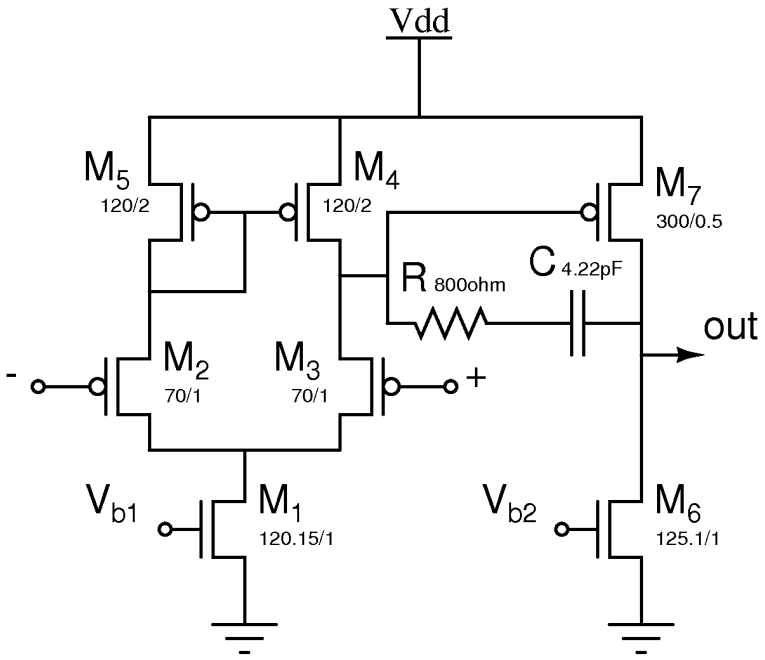


Figure 3.15: Circuit of OTA used as buffer.

3.3.5 Digital Circuit Design

Digital circuits consist of three main blocks. Control block generates required INT, RESET, gain, TDI and output signals for analog channels. An interface block programs digital circuit behavior through serial and parallel interface. Finally, block of decoders that includes level shifters carries out first block's control signals to analog channels of the ROIC.

Digital control circuit functions with two 3.3V clock signals. The first is the master clock signal CLK, which can set up to 1 MHz. All the control signals used in the ROIC are synchronized with this clock. The second is the integration clock INT, setting the integration time.

Main control block, interface circuits and decoders are designed through automatic circuit synthesis. Logic is designed by Verilog® programming language. Following the verification in code level, design is synthesized by using Synopsys® Design Vision® and the generated netlist is mapped to AMS 0.35 CORELIB 3.3V standard cell library elements. Following design verification at the schematics level, physical design is created using Cadence® Encounter® tool. Small decoders and level shifters (3.3V to 5V digital converters) are designed with full custom methodology.

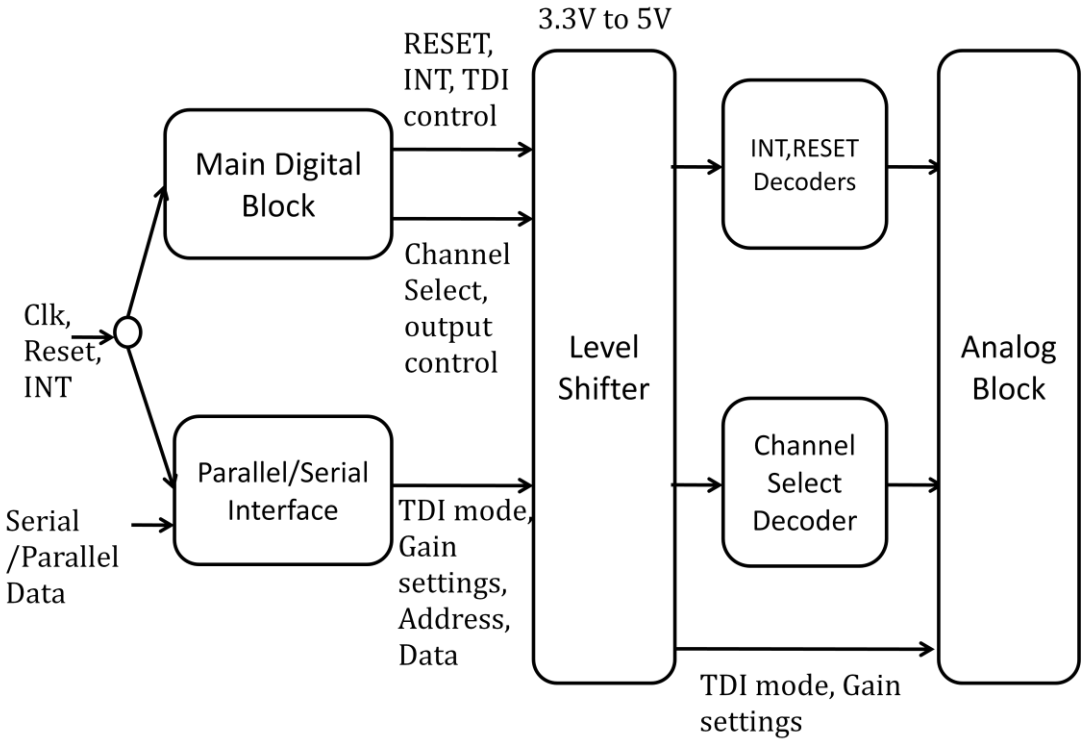


Figure 3.16: Control and interface signals of digital circuitry.

3.3.5.1 Main Control Circuit Design

As explained above, main control block generates gain control, TDI functions, output, INT and RESET signals. These signals are connected analog blocks through level shifters. Level shifters are required since analog block design with 5V MOSFETs.

These control signals are directly connected to switches inside analog channels. Inside input stage, digital circuit controls integration and reset time and, input gain switches (section 3.3.1.2). For TDI stage, digital circuitry directs integrated photocurrent inside unit cells to TDI memory cells according to scanning direction. It also redirects integrated currents inside TDI memory cells to output stage.

Digital circuitry is designed at the RTL level as ASIC by using Verilog® programming language, synthesized using Synopsys® Design Vision® and physical design is generated by Cadence® Encounter® for AMS C35B4 (four metal, 2 poly) process. Mapped Core library uses 3.3V MOSFET digital blocks unlike analog circuitry which is designed with 5V MOSFET library.

3.3.5.2 Interface Circuit Design

3.3.5.3 Level Shifters

Analog channels of the ROIC operate at 5V; hence control signals must be at 5V as well. Due to the signals generated from standard cell library which operate at 3.3V, level shifter to convert voltage from 3.3V to 5V is designed. Designed level shifters also works as buffer to drive long digital paths through 72 channel analog block.

Level Shifters are simply back to back 2 or 3 inverters depending on required signal pattern. These inverters are composed of 5V MOSFETs.

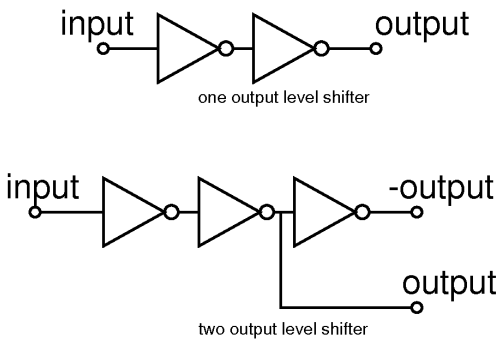


Figure 3.17: Block diagram of level shifters.

3.3.6 Temperature Sensor

Temperature sensor is important for cooled detectors. Because it is essential to know exact temperature of ROIC and detector to adjust optimum working point of detector. Performance of cooled MCT detectors is maximized at some temperatures (77° K). For MCT detector, low temperature brings high performance on IR detection due to low noise.

FPA is cooled by cryogenic temperature coolers called detector dewar cooler assembly (DDCA). Thus temperature information can be used feedback for DDCA. Then DDCA adjust its cooling performance.

Designed temperature sensor is based on ring oscillators. There are 2 ring oscillators, one is changes its frequency linearly with respect to temperature, other one is reference frequency

generator and its value is constant with temperature variations. Proposed topology of temperature sensor is similar to approached used in [18].

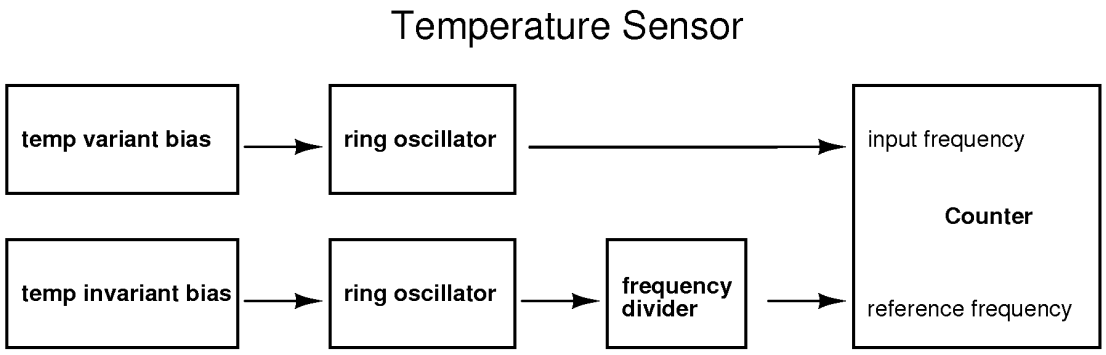


Figure 3.18: Block diagram of temperature sensor.

Reference frequency is constant with respect to temperature; other input frequency changes with temperature. Frequency counter circuit counts input frequency according to reference circuit. Frequency of reference counter is slower than input frequency. Thus, frequency counter circuit counts input frequency between rising edges of reference frequency. Also, frequency divider circuit is used for adjusting reference frequency. Output of frequency counter is 10 bit digital.

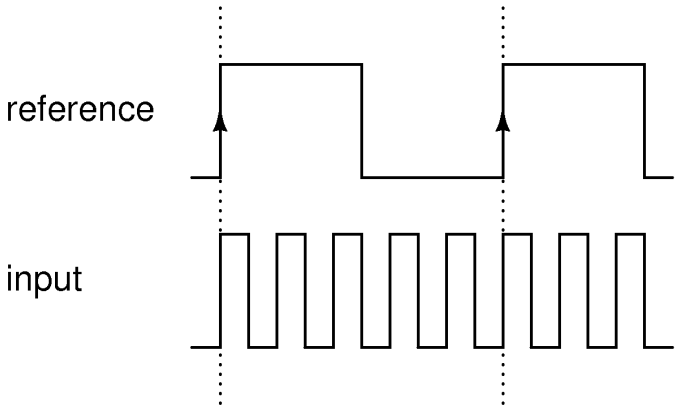


Figure 3.19: Input and reference input signals of frequency counter.

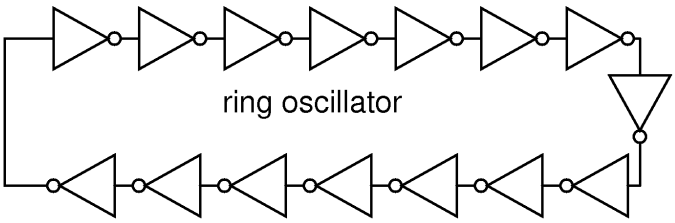


Figure 3.20: Ring oscillator topology.

Ring oscillators are composed of back to back connected odd number of inverters. In this topology 15 current-starved inverters are used. Frequency of ring oscillator can be calculated by rise and fall delays of single inverter. C_{load} represents load capacitance, N is number of inverter stages and I_{source} is inverter bias current.

$$f_{osc} = \frac{1}{N \cdot (t_{rise} + t_{fall})} = \frac{I_{source}}{N \cdot C_{load} \cdot V_{DD}} \tag{2.20}$$

Inverters used in ring oscillators are based on current-starved topology that limits current of inverter. By limiting current, frequency of inverter can be changed by adjusting this current. In this temperature sensor, current-starved inverters in Fig. 3.21 are used for temperature invariant ring oscillator and linear temperature variant ring oscillator. Bias stages are different for these two ring oscillators.

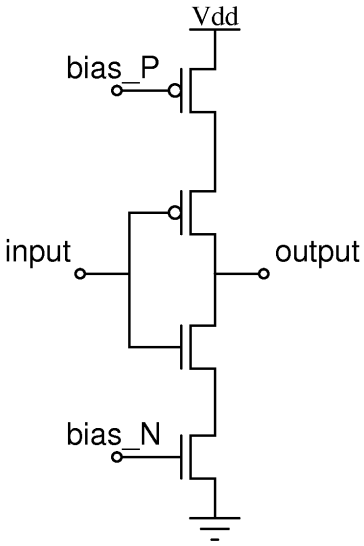


Figure 3.21: Schematic of current starved inverter.

Two different bias circuit is designed for ring oscillators. One is linear temperature variant bias circuit other one is temperature invariant bias circuit. Linear temperature variant bias circuit uses property of resistance at the drain of MOS transistor. Temperature coefficient of poly resistor R is positive, the voltage drop of resistor gets larger as the temperature goes up. Then, current through M3 transistor gets smaller, this behavior transferred ring oscillator through mirror stage. In temperature invariant bias circuit, R gives negative feedback (source degeneration) through source of M2 transistor for temperature variations. Thus, flowing current through this bias circuit doesn't change with respect to temperature variations.

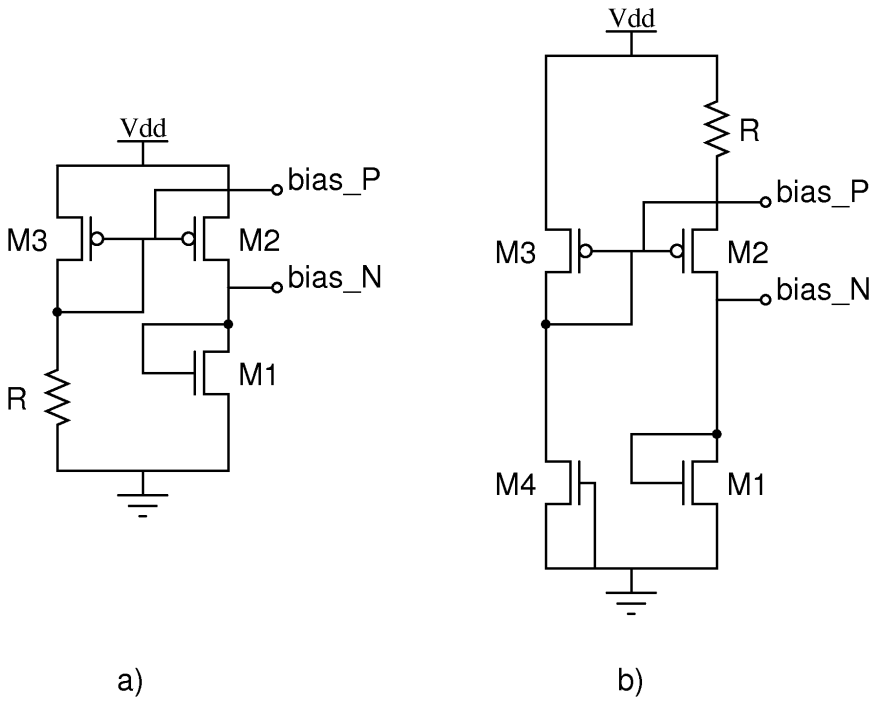


Figure 3.22: Schematics of a) linear temperature dependent and b) temperature invariant, bias circuits of ring oscillators.

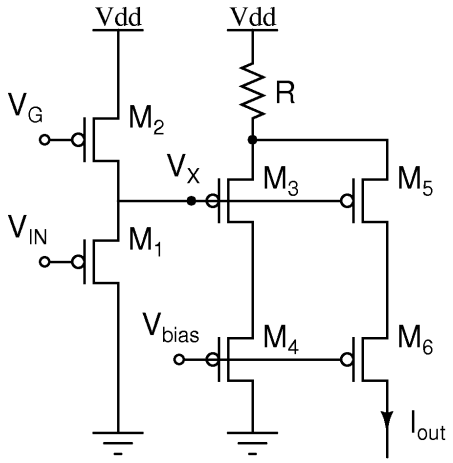
Current-starved inverters, ring oscillators and bias circuits designed fully custom. Frequency counter is designed with Verilog® hardware programming language and synthesized with Cadence® Encounter® software.

3.3.7 Current Source

In order to fully test ROIC, detector needs to be bonded and detector should be exposed controlled IR light sources. But at this time, this is not possible to create this test environment since detectors are not ready. To measure ROIC chip without a detector, currents sources that

represent detector currents are designed. Due to process and mismatches standard current mirror approach to design current sources are not useful. Conventional current sources vary significantly around 55%. Under these conditions measurements will not be reliable. Thus, process and temperature compensated current source is designed.

Process compensation is done by eliminating threshold variation (V_T). In this way, overdrive voltage will be constant. In the schematic Vx node is constant due to process variations. Also, temperature variations are compensated by resistance feedback at the source of M3 and M5 transistors.



3.23: Schematic of temperature and process compensated current reference.

3.4 Physical Design

Physical designs of digital circuits operating at 3.3V are done by automatic layout generation with Cadence® Encounter® tool. Layouts of all remaining blocks are done by full custom.

72x7 ROIC is not submitted for fabrication. Instead 6x7 with fully functional analog block sent fabrication for testing purposes. In this section layout of all analog sub blocks are shown and their sizes are given. Also comparison of analog channels with capacitive based TDI and with current mode TDI will be given.

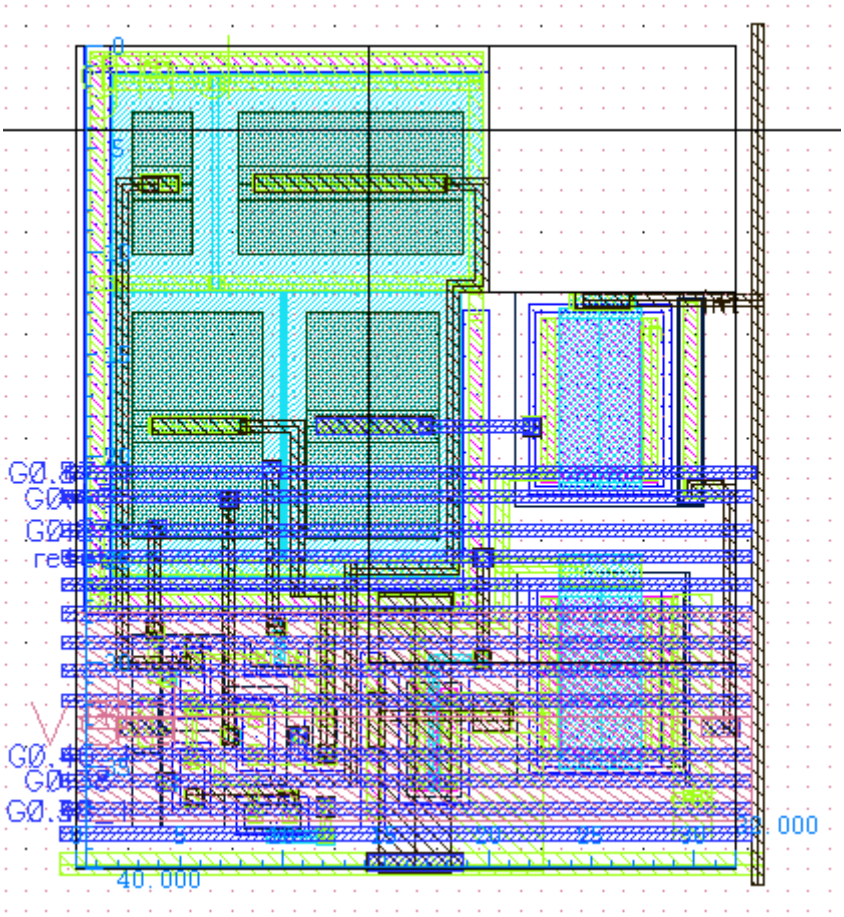


Figure 3.24: Layout of DI input stage.

Fig. 3.24 shows in-pixel implementation of DI input stage. DI input stage gain capacitances and source follower transistor is fit inside detector pixel area. Detector will be bonded via flip chip method and bonding area is right most top area of DI unit cell. Bonding opening is 5µm x 5µm. Total area of DI is 32µm x 40µm.

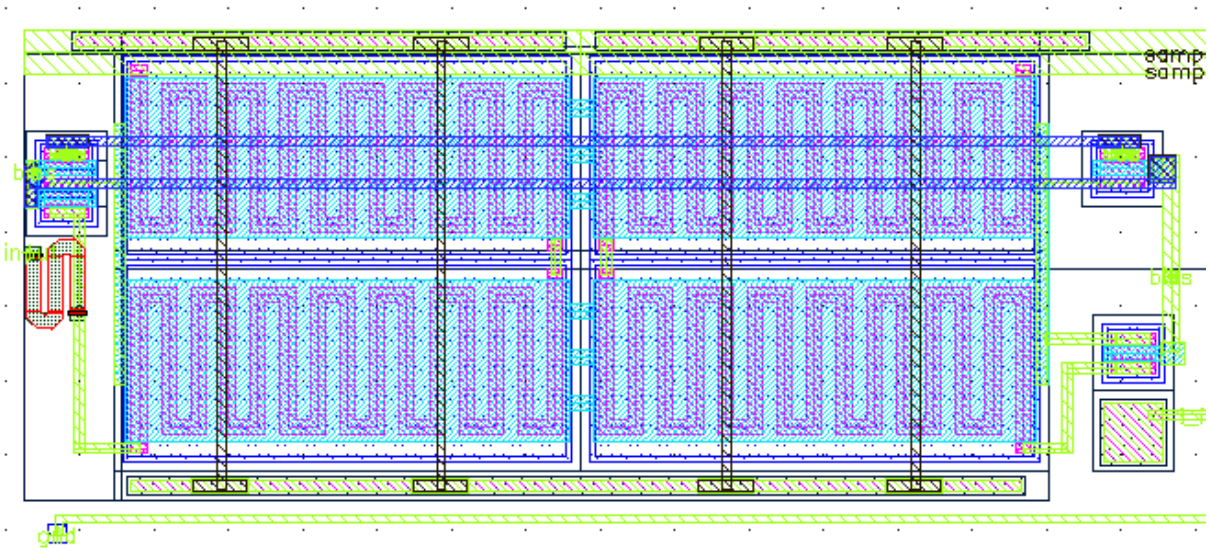


Figure 3.25: Layout of VIC, size 78µm x 30µm.

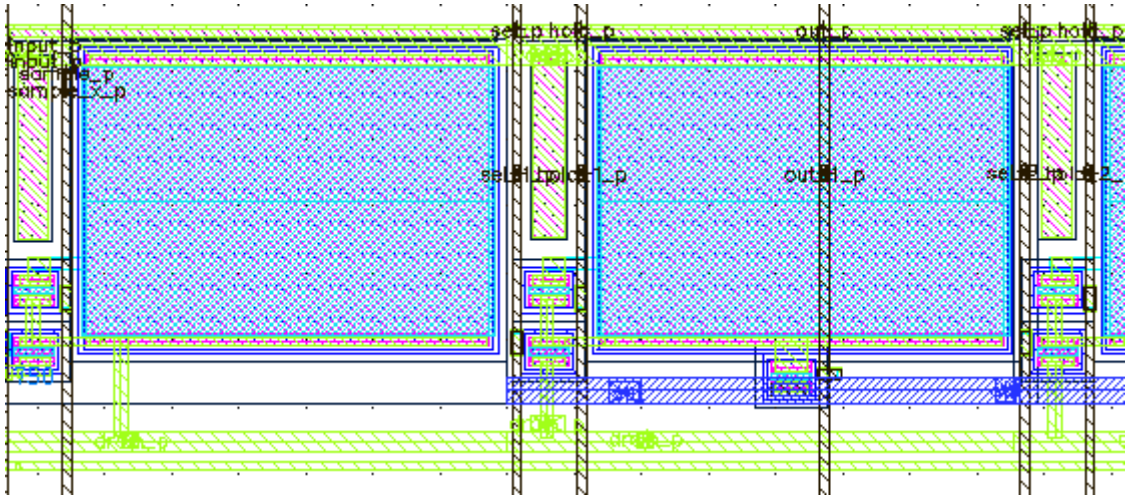


Figure 3.26: Layout of single input cell and memory of TDI stage.

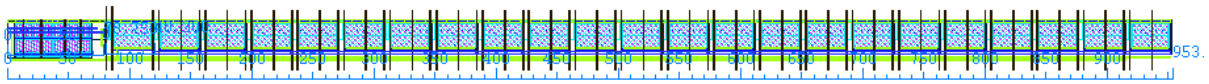


Figure 3.27: Full layout of TDI stage with VIC, size 30µm x 953µm.

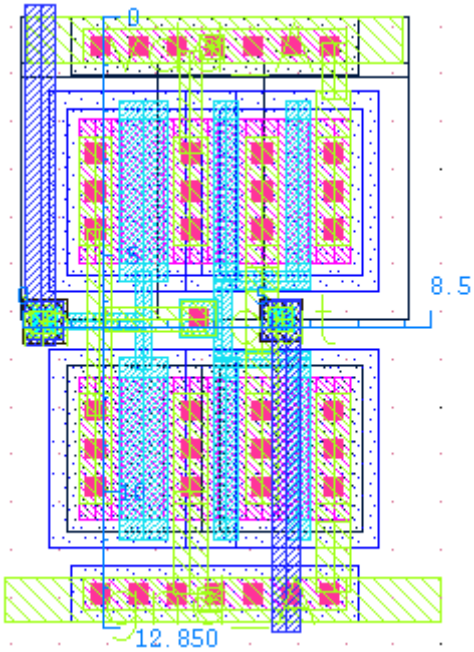


Figure 3.28: Layout of level shifter, size 8.5µm x 12.85µm.

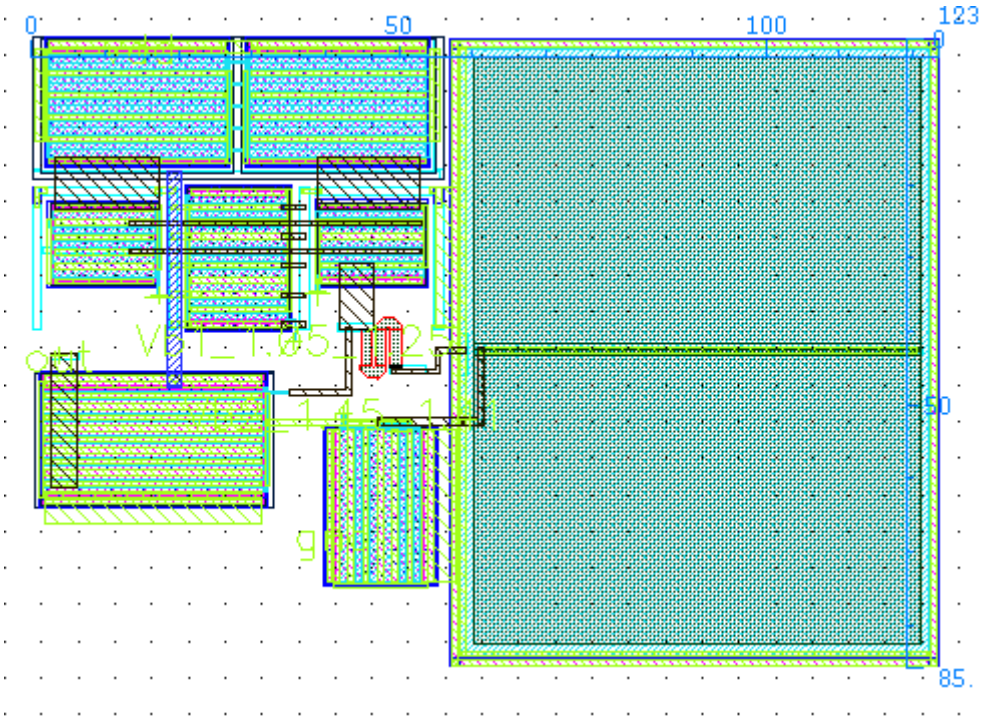


Figure 3.29: Layout of buffer, size 85µm x 123µm.

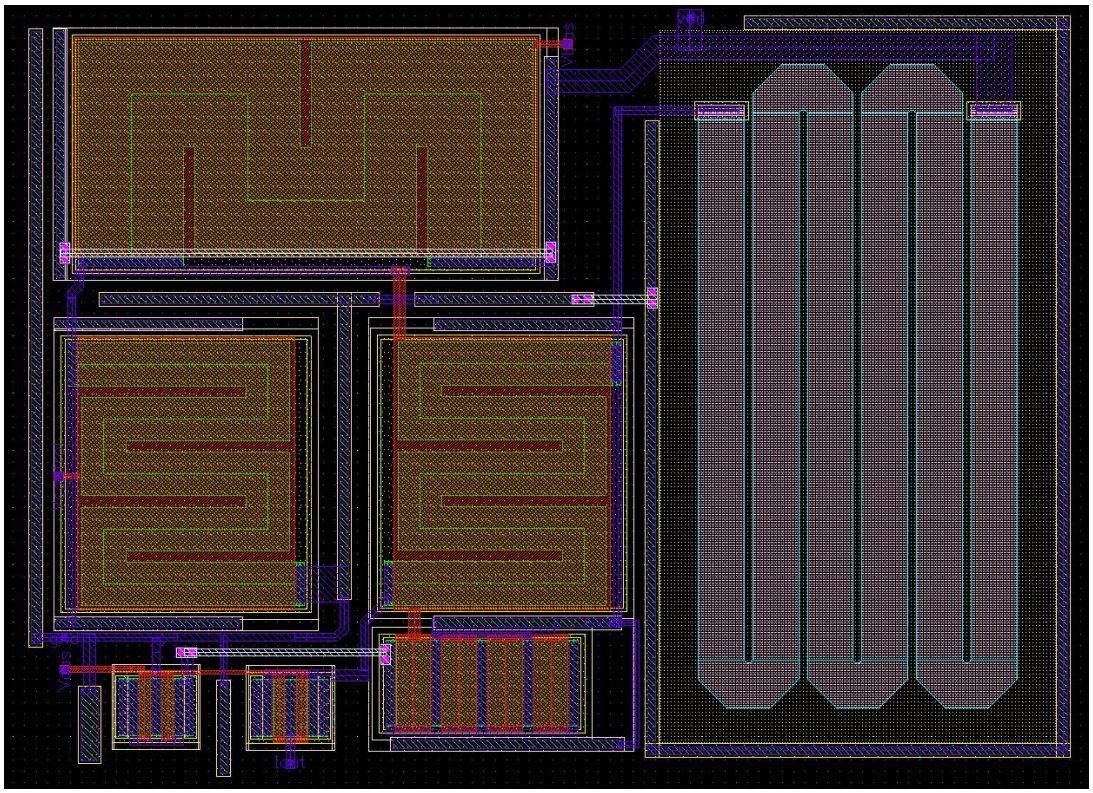


Figure 3.30: Layout of process and temperature compensated current source.

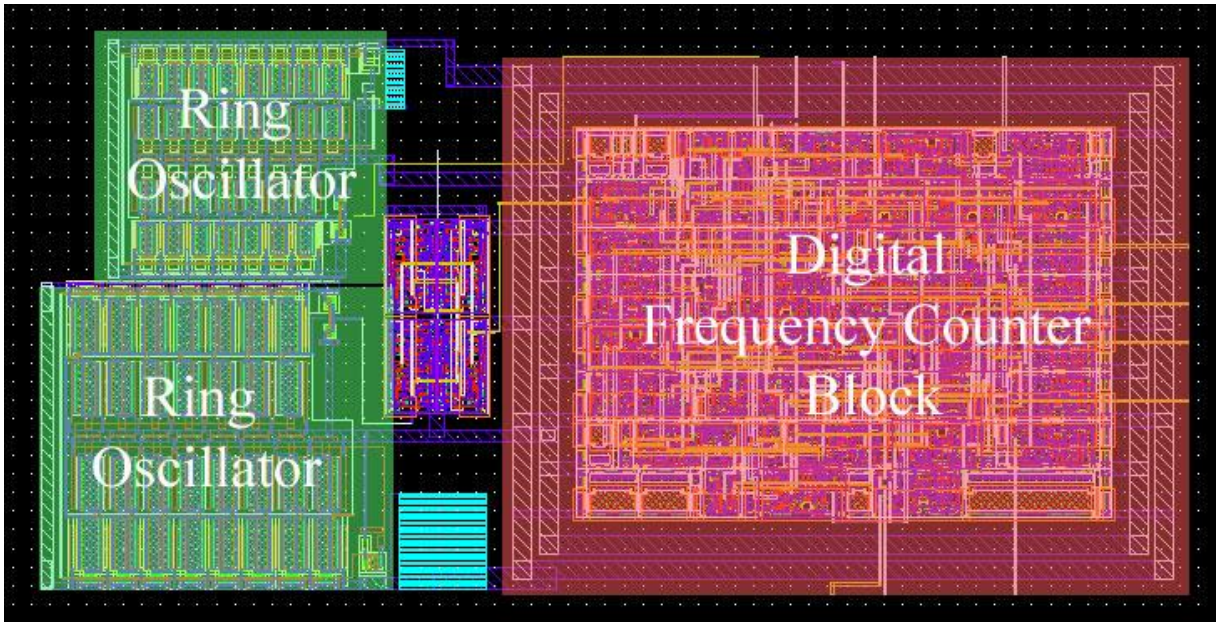


Figure 3.31: Layout of temperature sensor, size 300µm x 140µm.

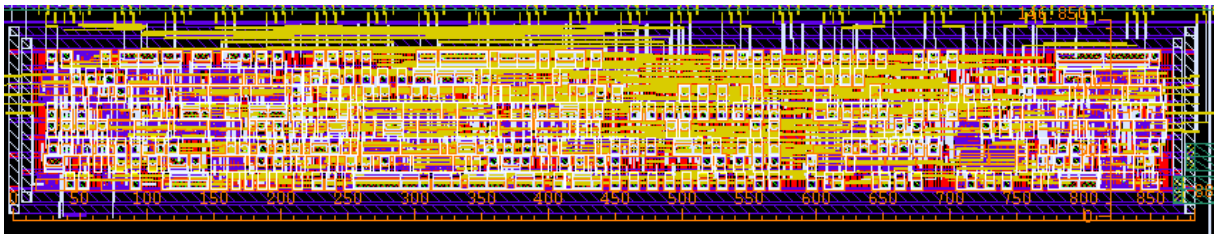


Figure 3.32: Layout of synthesized digital block, size 880µm x 146µm.

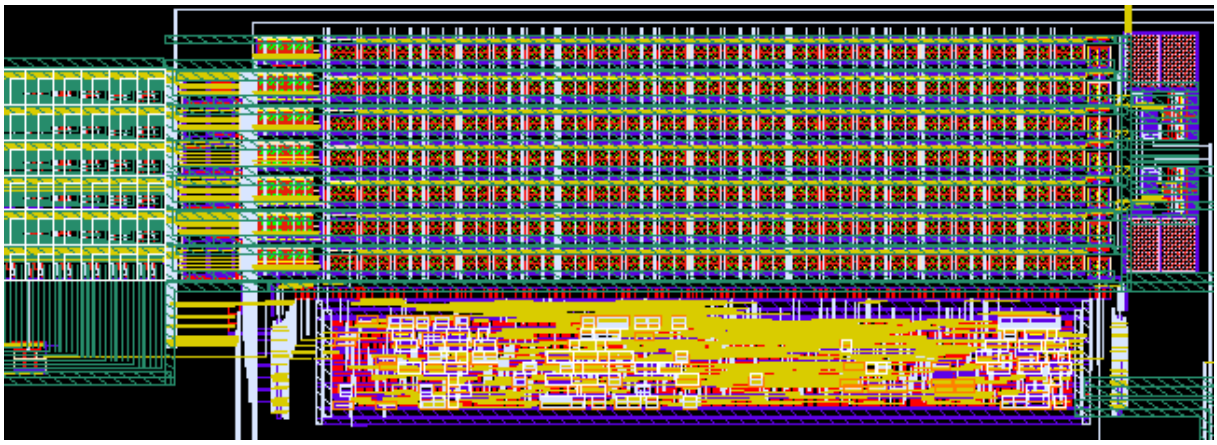


Figure 3.33: Layout of full ROIC 6x7, size 1390µm x 410µm.

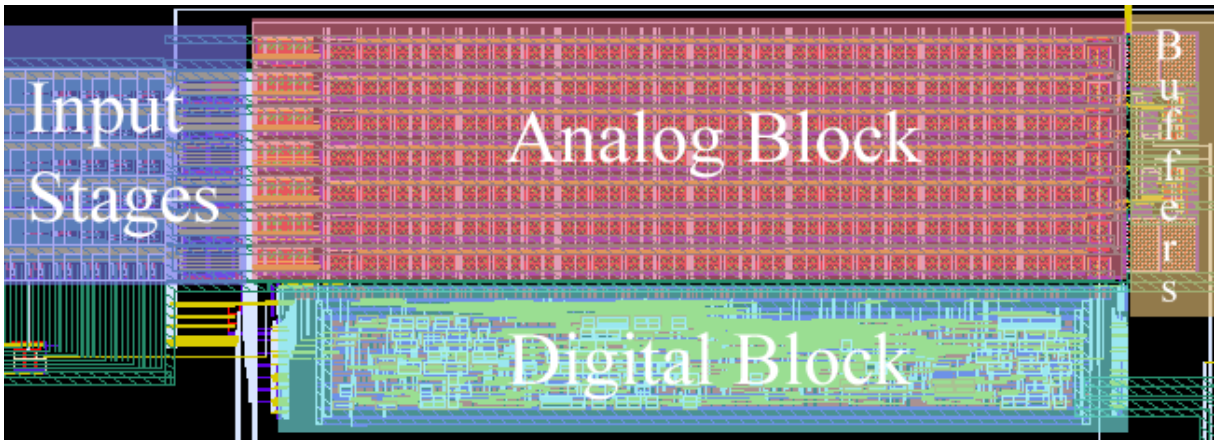


Figure 3.34: Names of blocks of full 6x7 ROIC.

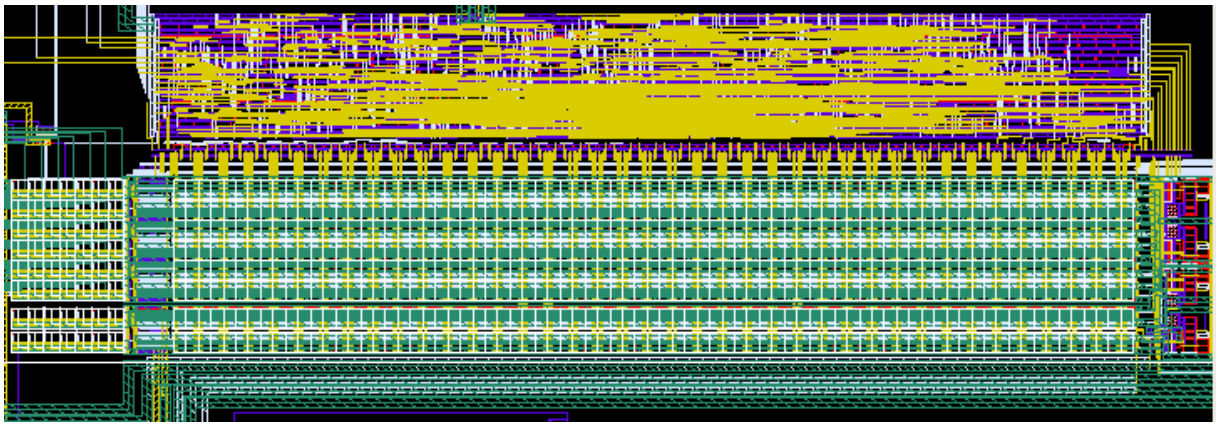


Figure 3.35: Layout of 6x7 ROIC with capacitive TDI approach, size 2520µm x 573µm.

As observed from Fig. 3.33 and Fig. 3.35 areas of layouts are 0,57 mm^2 and 1,44396 mm^2 respectively. Approximately, topology used in this ROIC is 2.5 times smaller than capacitive TDI approach.

4 RESULTS

In this section, simulation results of designed and fabricated 6x7 ROIC is given. It represents 72x7 ROIC performance since 72x7 is replicated version of analog blocks of 6x7 ROIC and digital block is capable to work with 72 channels. Furthermore, simulations are done with accurate SPECTRE simulator based on widely accepted BSIM3V3 transistor models.

Firstly, performance of sub blocks are given one by one, then overall system performance for various input currents is represented. After that, detailed final output results are given.

4.1 Simulation Results of Sub Blocks

4.1.1 Simulation Results of Input Stage

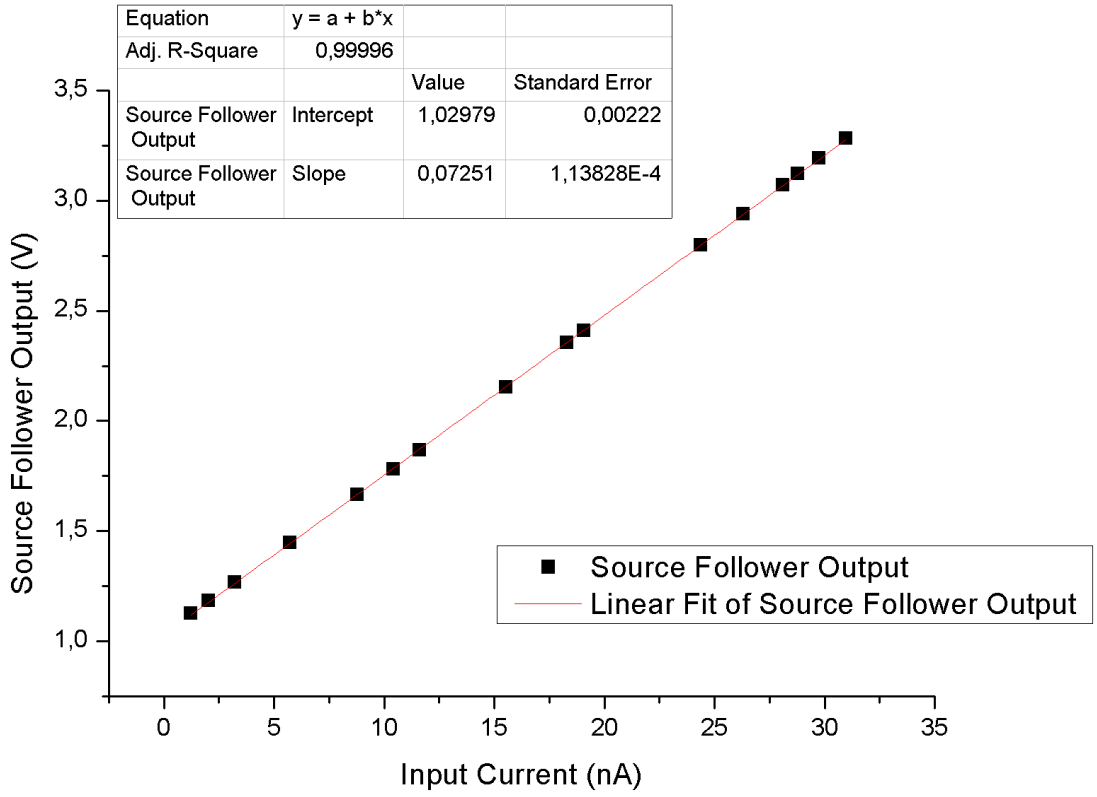


Figure 4.1: Linearity of input stage for different input currents vs source follower output (output of input stage) for 27 °C. Standard error is 0.2%

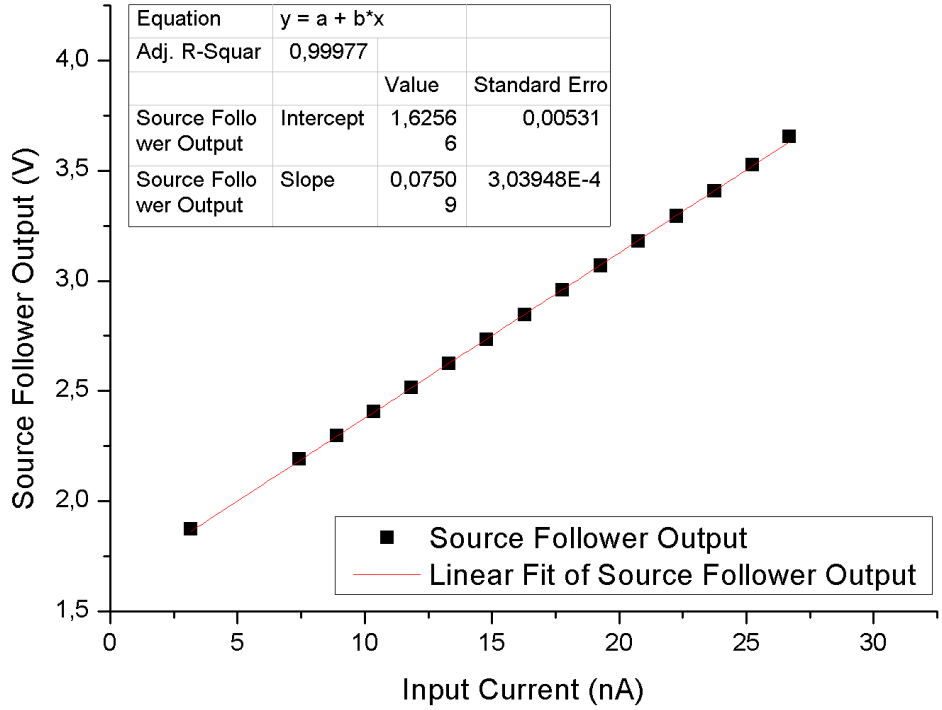


Figure 4.2: Linearity of input stage for different input currents vs source follower output (output of input stage) for 77 °K. Standard error is 0.5%

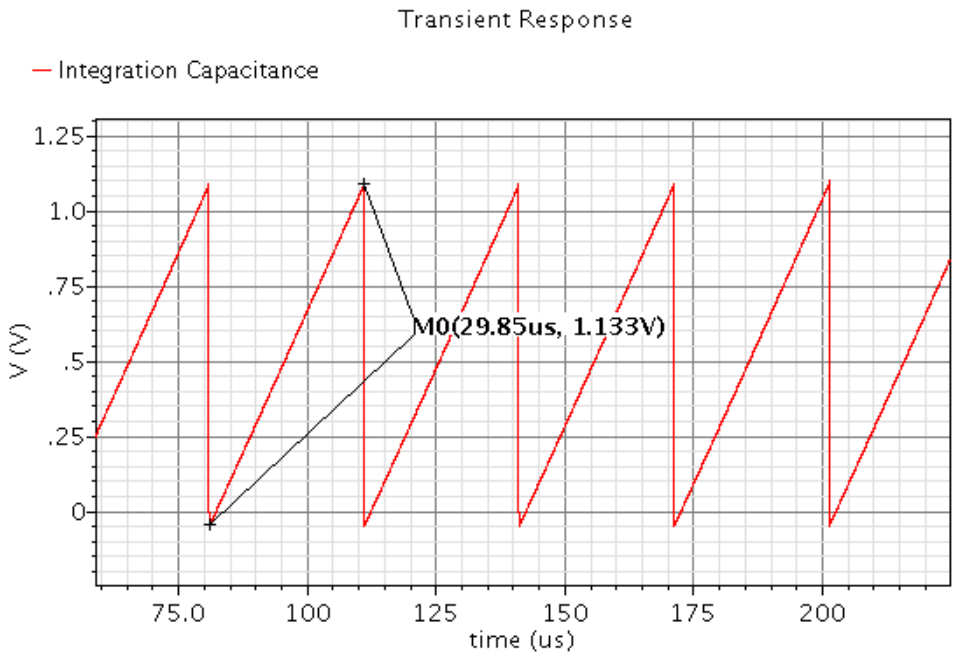


Figure 4.3: Charge at integration capacitance; 29.85u integration time, 1.133V charge is integrated.

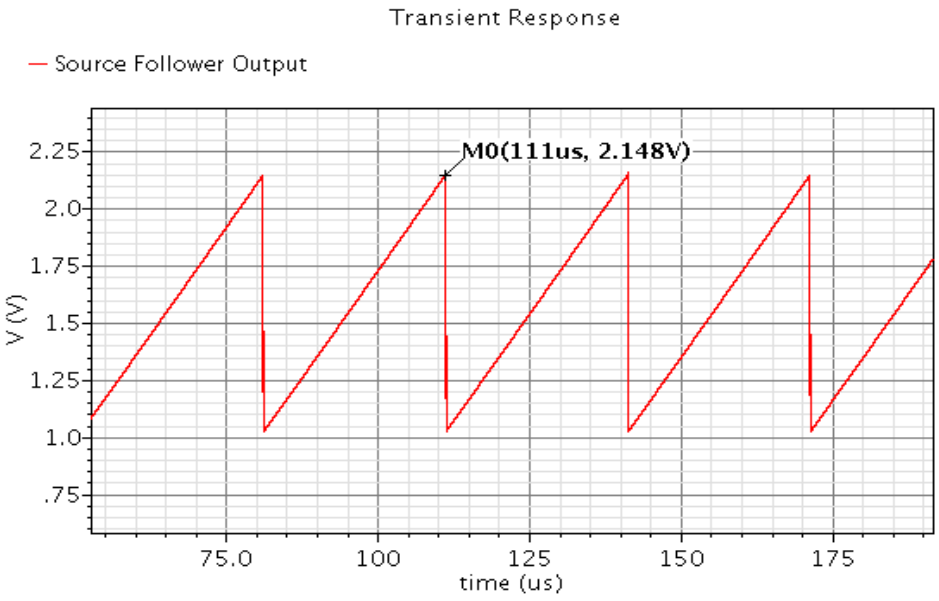


Figure 4.4: Source follower output of integrated charge; 2.148V.

Fig. 4.1 and Fig 4.2 show linearity performance of input stage for different current values. Current is provided by process and temperature invariant current references. Simulation results are obtained for room temperature and cryogenic temperature. Fig 4.3 and Fig 4.4 shows how integrated charge at the input capacitor reflected to output of source follower. There is a offset between results due to threshold voltage of MOSFET.

4.1.2 Simulation Results of VIC Stage

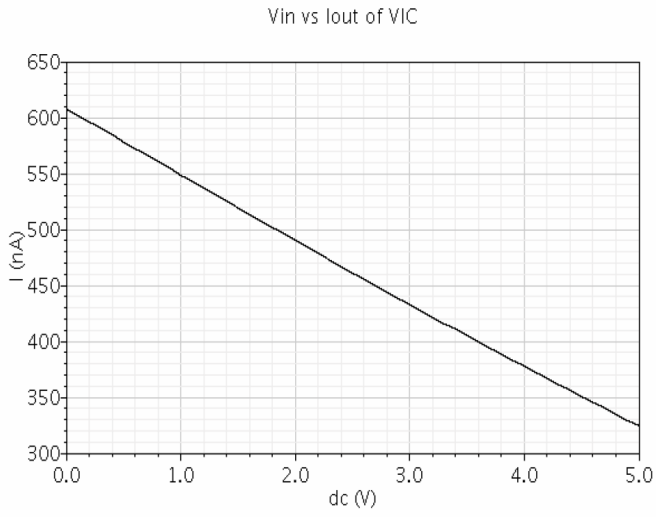


Figure 4.5: DC response of voltage to current converter. Current (nA) vs voltage (V).

4.1.3 Simulation Results of TDI Stage

To simulate performance of TDI stage ideal input currents were given to TDI stage. These currents first pass through input of TDI stage than it is stored at current memory. Same input current integrated 7 times to simulate TDI over 7 element behavior. Output currents are high due to addition on TDI memory stage is done on constant offset current which is 671,094nA in this case. This offset current is depended on tail current inside input of TDI stage. Input currents and results are given in Table 4.1 and Fig. 4.6.

Input Current (nA)	TDI MEM (nA)	Input Current (nA)	TDI MEM (nA)	Input Current (nA)	TDI MEM (nA)	Input Current (nA)	TDI MEM (nA)	Input Current (nA)	TDI MEM (nA)
0	671,094	9	726,018	18	781,001	27	836,021	36	891,071
1	677,197	10	732,082	19	787,116	28	842,138	37	897,192
2	683,297	11	738,195	20	793,233	29	848,241	38	903,305
3	689,395	12	744,306	21	799,352	30	854,358	39	909,419
4	695,497	13	750,421	22	805,434	31	860,478	40	915,533
5	701,598	14	756,535	23	811,55	32	866,597		
6	707,701	15	762,648	24	817,668	33	872,697		
7	713,806	16	768,763	25	823,788	34	878,83		
8	719,91	17	774,882	26	829,903	35	884,95		

Table 4.1: Linearity performance of TDI stage, 7 times integrated input currents and output current as table.

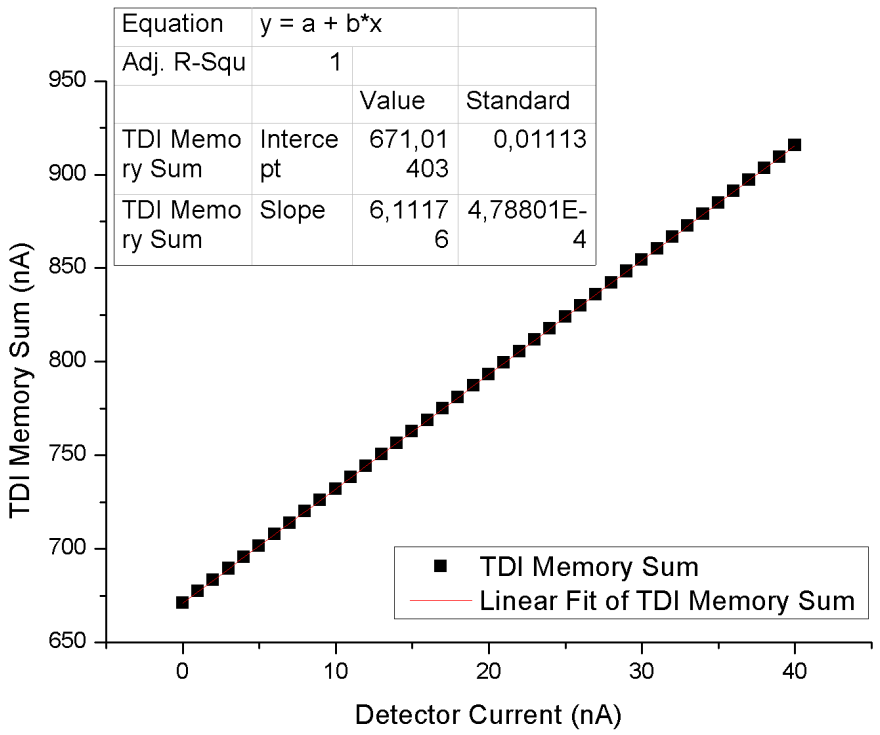


Figure 4.6: Linearity performance of TDI stage, 7 times integrated input currents and output current as graph.

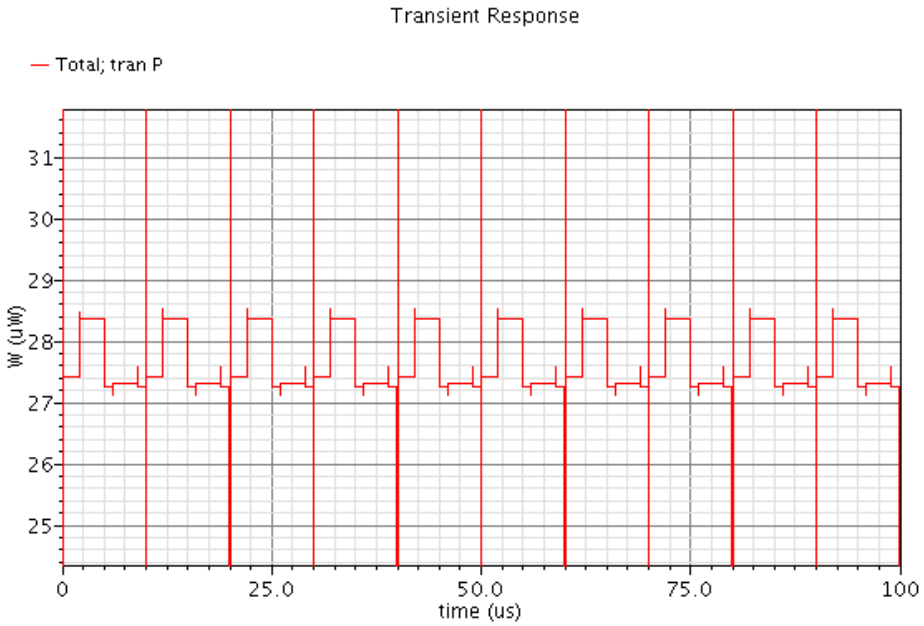


Figure 4.7: Power consumption of single TDI analog channel. Average power consumption is 28µW.

4.1.4 Simulation Results of Output Buffer

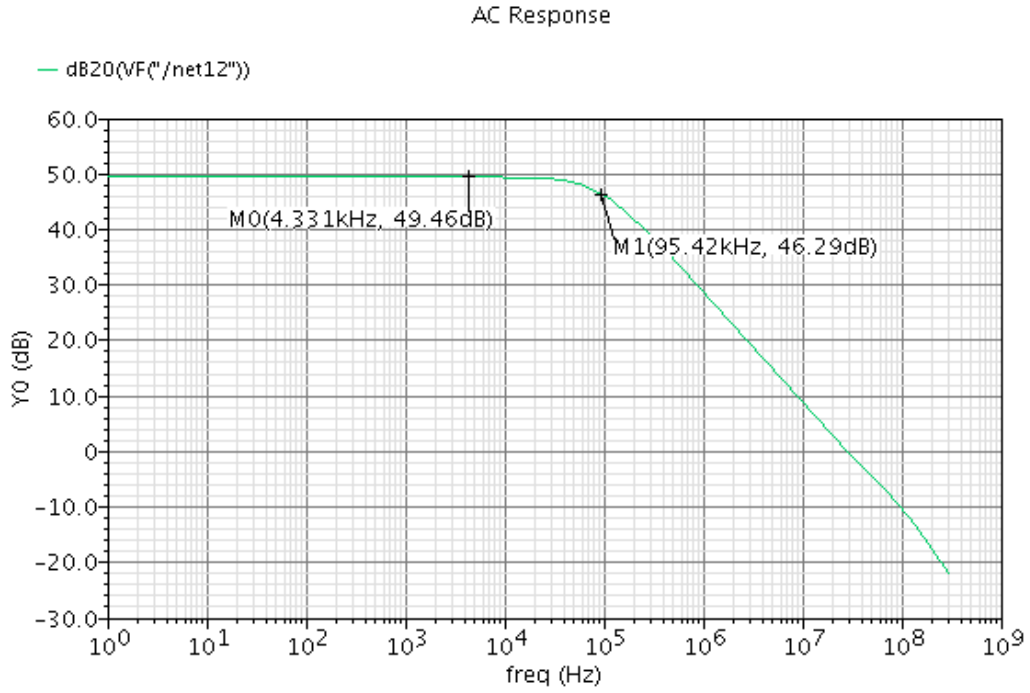


Figure 4.8: Output stage gain vs frequency in dB.

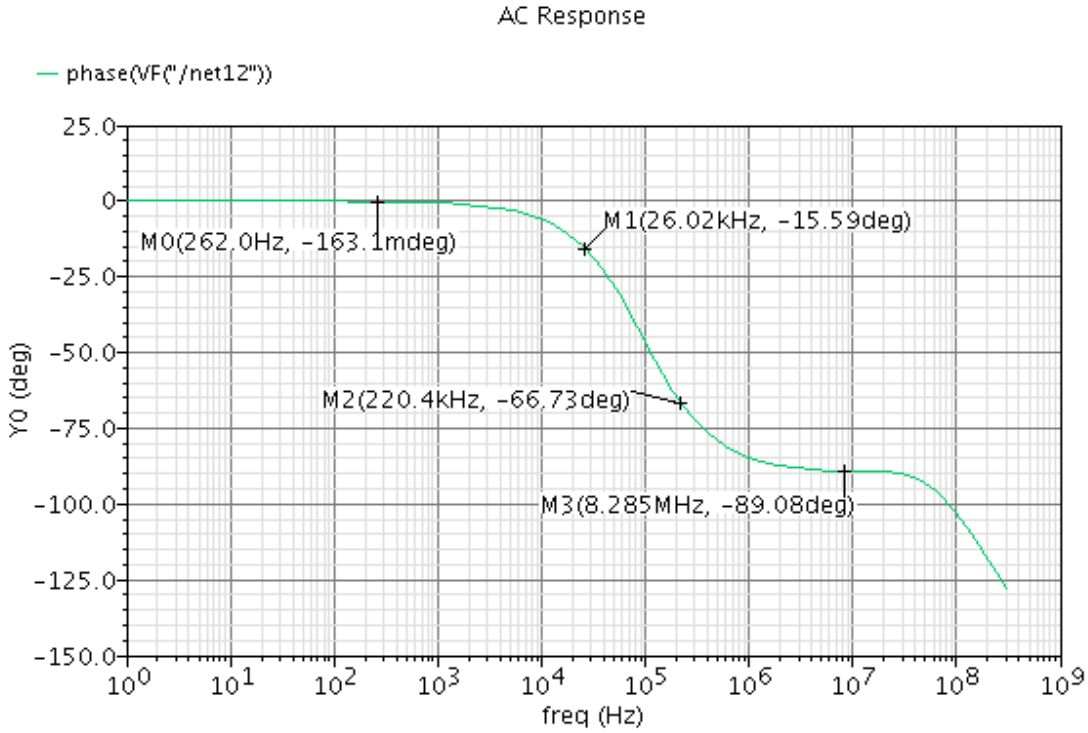


Figure 4.9: Phase graph of output buffer.

4.1.5 Simulation Results of Temperature Sensor

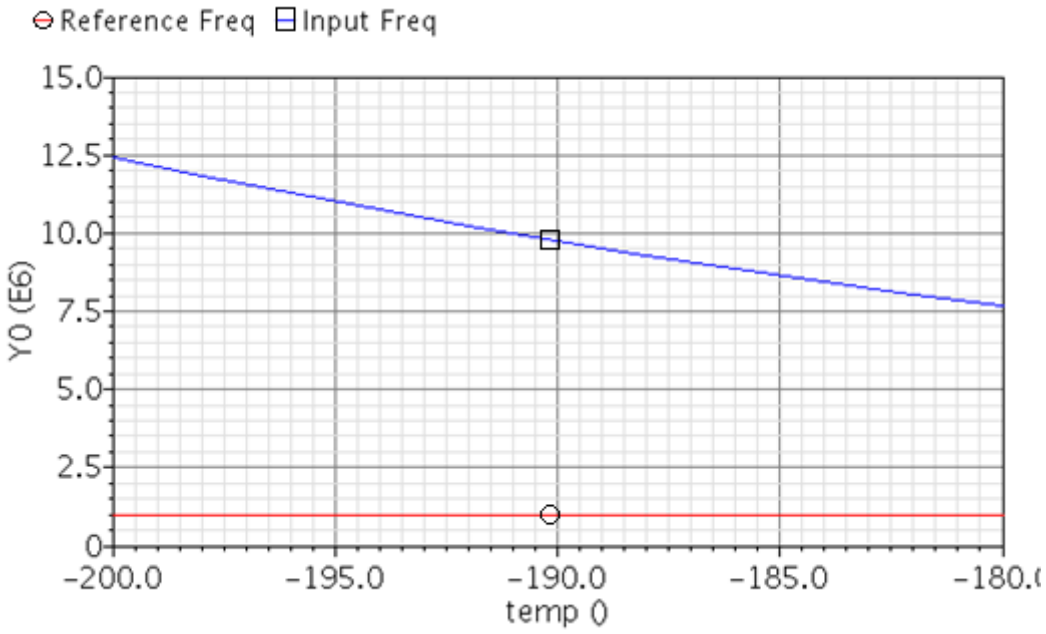


Figure 4.10: Temperature vs frequency for temperature independent ring oscillator (reference freq) and linear temperature variant ring oscillator (input freq).

Fig. 4.10 shows simulation results of temperature sensor input frequency is linearly dependent on temperature. Reference frequency is constant with temperature variation.

4.1.6 Simulation Results of Current Source

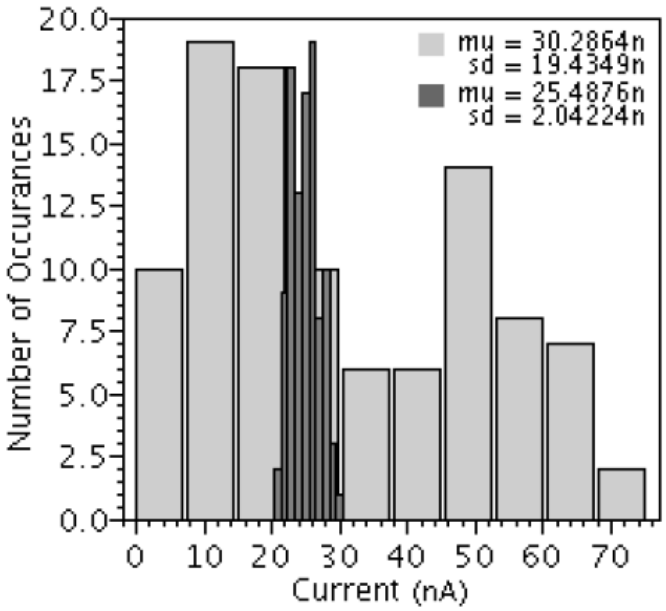


Figure 4.11: Spread of output current as a result of process variations and mismatches. Compensated current (dark colored) has a standard deviation/mean improvement of 8x.

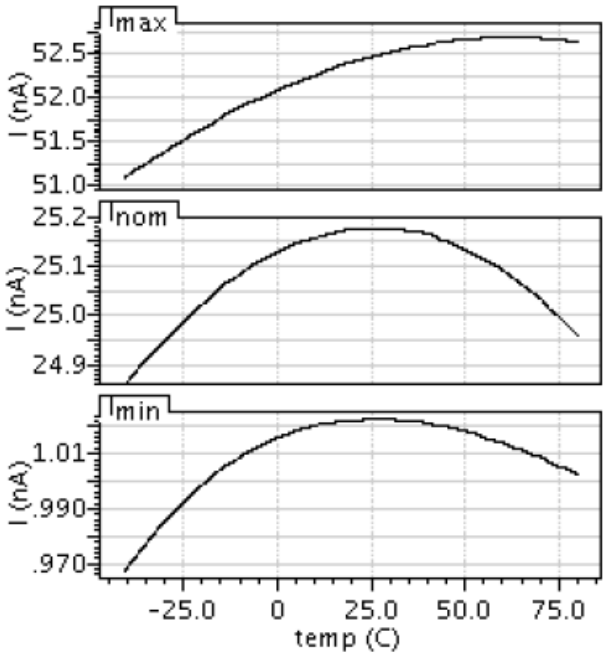


Figure 4.12: Output current vs temperature for maximum, nominal and minimum currents.

Output current (nA)	σ/μ due Process variations (%)				Temperature Drift (ppm/°C)	
	This Work		Uncompansated Current Reference			
	Mismatch only	Process & Mismatch	Mismatch only	Process & Mismatch	-40 - 80 (°C)	10 - 50 (°C)
1	2,8	9,1	1,78	118	443	36
25	1,4	8,0	0,77	64,2	105	14
50	1,1	8,35	0,56	54,5	241	61

Table 4.2: Summary of process and temperature compensated current source results.

4.2 Simulation Results of Overall System

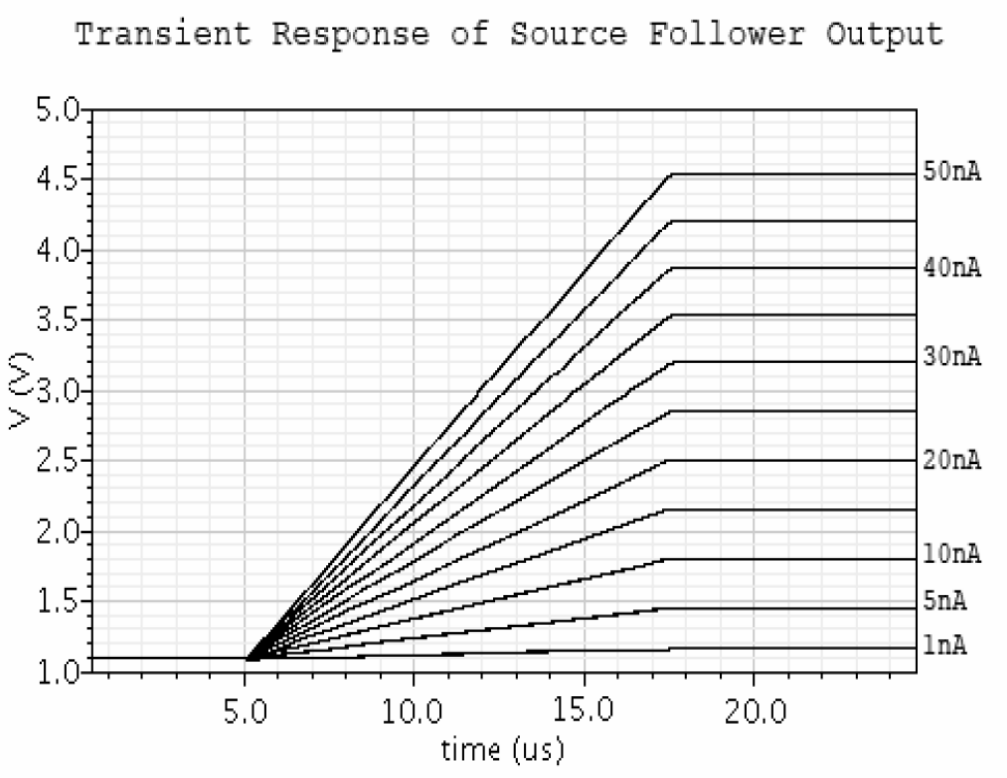


Figure 4.13: Gain setting of 1, integration time of 12.5μs, with an input photocurrent of 1nA, 5nA, 10nA, 20nA, 30nA, 40nA and 50nA

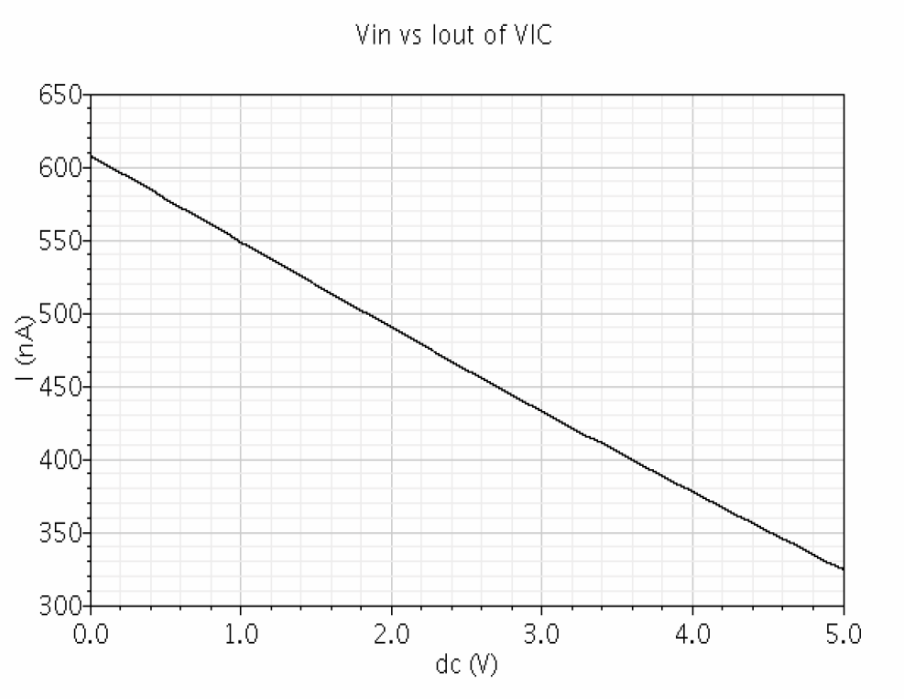


Figure 4.14: DC characteristics of voltage to current converter.

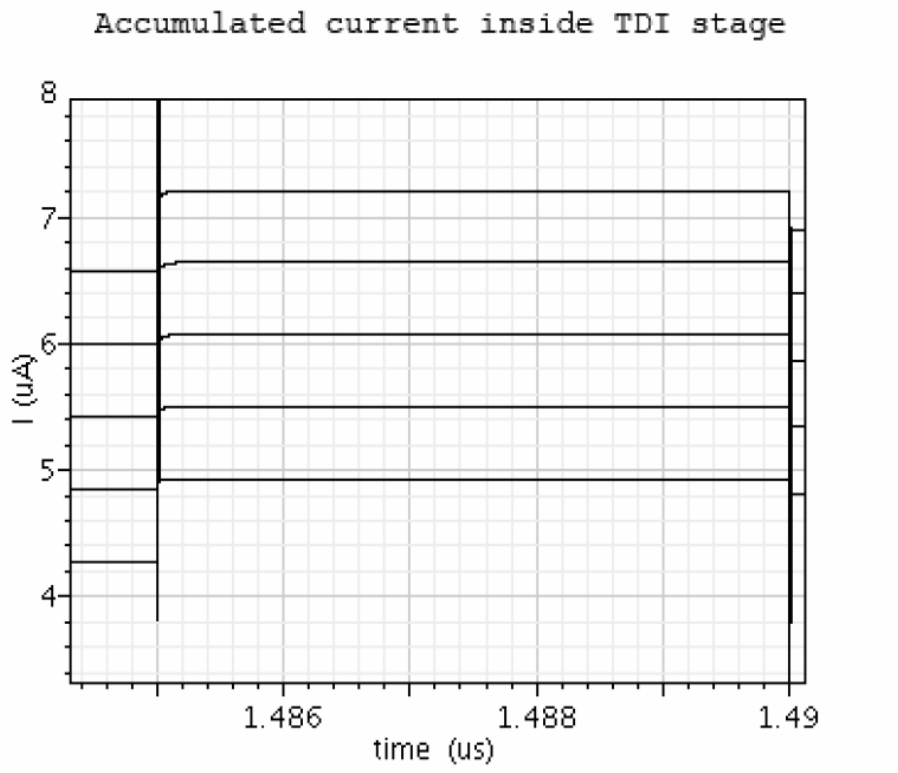


Figure 4.15: 7 element TDI applied result on TDI memory cell for 10nA, 20nA, 30nA, 40nA and 50nA photocurrents.

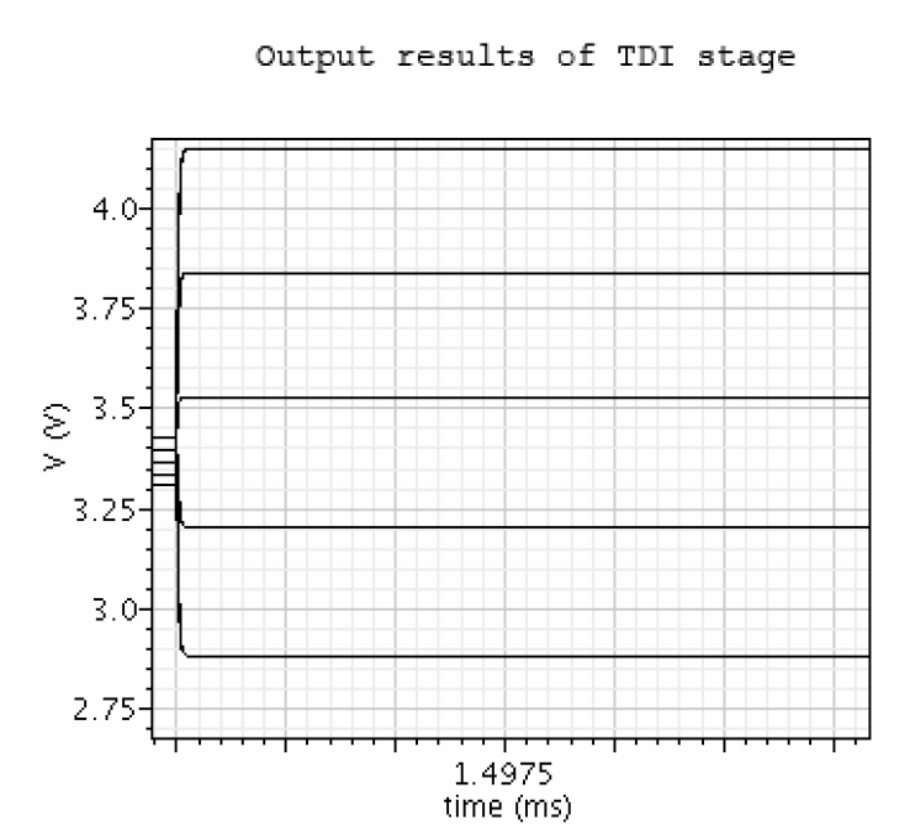


Figure 4.16: Corresponding output results of TDI memory cell for for 10nA, 20nA, 30nA, 40nA and 50nA photocurrents.

5 CONCLUSIONS

In this thesis, design of a CMOS readout integrated circuit for an array of 576x7 elements of P-on-N type MCT detectors for LWIR spectrum is presented. In this system, current mode TDI algorithm applied to improve SNR of photocurrents. This current mode approach brings advantages over capacitor based TDI approach such as small area, low power and high linearity. First chapter includes detailed information about IR imaging systems, detectors and readout electronics. In the second chapter, topologies of main building blocks such as preamplifiers and noise compensation techniques, of ROIC are discussed in detail with advantageous and disadvantageous including possible applications. In the third chapter, proposed ROIC implementation is given in the light of requirements based on application and detector. Fourth chapter contains simulation results of building blocks and overall system with comments.

As a preamplifier of the system, direct injection unit cell topology is selected among many other topologies. Direct injection promises low noise, low power and small area which are essential requirements for the system. 100mW limit for power consumption budget due to chip cooler (dewar) requirements and 1000 rms noise is limit for input referred noise. Also layout should fit under detector pixel to reduce noise and parasitic. Although, DI is not known high injection efficient topology except for detector with high R_0A value. Injection efficiency is on reasonable levels (%50) for typical conditions.

As a noise reduction technique, time delay integration is applied on seven detectors with a super sampling rate of three. TDI increases SNR for $\sqrt{N}$ times (N is number of detectors) and supersampling effectively increases the spatial resolution. Unlike other TDI topologies based on capacitors as analog memory element, the TDI topology applied in this thesis uses current memories. Current memories are composed of just MOSFETs. This reduces area of chip significantly. Both capacitor based TDI and current memory based TDI are implemented for 6x7 ROIC; full 6x7 ROIC with current memory based TDI is 2.5 times smaller than other chip.

Moreover, capacitor based TDI topology requires integrator which is generally based on OTA or op-amp for integration of charges inside capacitors. Unlike this, current memory based TDI approach uses just switches to integrate currents. This reduces power consumption.

Only drawback is requirement of extra stage to implement current mode TDI. Output of DI stage is in the voltage domain which is not suitable for current mode TDI which accepts current as input. Hence, voltage to current converter is required between input stage and TDI stage.

Voltage to current converter is designed with using flipped voltage follower building block. FVF has advantages over conventional voltage followers like low output resistance with high injection capability and almost unity gain for large signal. Additionally, bulk driven approach used in this linear VIC.

Temperature sensor is also realized for ROIC to measure operating temperature of the circuit. Because, this circuit designed to operate at 77 °K due to detector that needs to operate at cryogenic temperatures. Temperature sensor will help to adjust actual temperature of circuit.

Output load of ROIC is 15pF in parallel with 1MΩ. Also output should settle within 60 ns at every clock edge when a read operation is done. In order to achieve this, an op-amp buffer is used with slew rate 60V/μs.

Digital circuit of ROIC can be divided into two parts. A main control block generates required INT, RESET and gain adjustments with switches of TDI circuit. An interface block programs the ROIC through serial and parallel interface.

Digital control circuit operates with two 3.3V clock signals. The first is the master clock signal (CLK) up to 1MHz which all the control signals used in the ROIC are synchronized with this clock. The second is the integration clock (INT), setting the integration time.

All digital main control block and interface circuits are designed through automatic synthesis method using Verilog® hardware programming language. First, verification of synthesizable code checked with ModelSim®. Then, design is synthesized using Synopsys® Design Vision® and generated netlist is mapped to standard cell library (CORELIB 3.3V) elements of AMS. Following design verification is done at the schematics level, physical design is created using Cadence® Encounter® tool. Decoders and level shifters, which up-convert 3.3V digital signals to 5V to match analog circuit level, are designed with full custom methodology.

To sum up, designed readout ROIC structure includes seven elements current mode TDI functioning with a super sampling rate of 3, bidirectional TDI scanning, programmable four gain settings and programmable integration time. Current mode TDI helps to reduce area of analog block and power consumption by improving linearity. ROIC has a dynamic range of 3.75V from 1.25V to 5V and input referred noise of 1000 rms electrons. Functionality of 6x7, to the way for 72x7 and finally 576x7, is evaluated through simulation results given in previous chapters. For the final measurements, current sources will be removed from chip and 576x7 chip will be flip-chip bonded with detector array in dewar system at cryogenic temperature (77 °K).

For the future study, more functionality such as automatic gain adjustment can be added to current mode TDI stage. Also VIC needs to be improved because it limits operating frequency of overall circuit to 1MHz. Direct connection from modified input stage can be considered as well by not sacrificing linearity and noise performance. Also, this helps to even lower power consumption. 6x7 ROIC and one analog test channel circuit is sent to manufacturing. Measurement results of 6x7 ROIC with simulations results help to realize to constitute 72x7 ROIC as a building block of 576x7 ROIC.

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