An X-Band Power Amplifier Design for On-Chip RADAR Applications

by

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Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of
Master of Science

Sabancı University

Summer, 2011

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DATE OF APPROVAL: 07/07/2011

Acknowledgements

This work was supported by Turkish Scientific and Technology Research Institution TUBITAK Grant 110E107, "X-Band Phased-Array Transceiver Module for RADAR Applications Using SiGe-BiCMOS and CMOS Integrated RFMEMS Switch Device Technologies". Additionally, I would like to acknowledge the financial support of TUBITAK-BIDEB during my master program as it provided me with a generous scholarship.

First and foremost, I wish to express my gratitude to Professor Yaşar Gürbüz for his guidance, support, and motivation over my Master study. He has been an advisor in the truest sense of the word and I have benefited his broad vision and perceptive insight. I certainly could not come this far without his assistance.

I would like to thank Assoc. Prof. İbrahim Tekin for taking his time to answer my endless questions about antennas and microwaves. I am also grateful to Assoc. Prof. Meriç Özcan, Assoc. Prof. Ayhan Bozkurt, Assist. Prof. Cem Öztürk, and Dr. Volkan Özgüz for their assistance, helpful comments and serving on my thesis committee.

I am thankful to my friend, Ferhat Taşdemir with whom I started this journey seven years ago, for sticking by me along the way. Moreover, I have been very fortunate in my friends at Sabanci who have made the last two years so enjoyable – Melik Yazici, Hüseyin Kayahan, Emre Özeren, Ömer Ceylan, Burak Baran, and Saravan Kallempudi. Also, thanks to my comrade designer Tolga Dinç for his contribution to this work. I would also like to thank the Sabanci stuff: Bülent Köroğlu, Ali Kasal and Mehmet Doğan, whose support has created a student-friendly environment.

Last, but not the least, to my loving family, my parents Müzeyyen and İbrahim and my sister Çağla for being there when I needed them to be. Their unconditional and pure love has been the greatest source of energy for me.

An X-Band Power Amplifier Design for On-Chip RADAR Applications

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EE, Master's Thesis, 2011
Thesis Supervisor: Prof. Dr. Yaşar GÜRBÜZ

Keywords: Phased Array RADAR, T/R module, Power Amplifier, SiGe BiCMOS, X-Band Integrated Circuits.

Abstract

Tremendous growth of RAdio Detecting And Ranging (RADAR) and communication electronics require low manufacturing cost, excellent performance, minimum area and highly integrated solutions for transmitter/receiver (T/R) modules, which are one of the most important blocks of RADAR systems. New circuit topologies and process technologies are investigated to fulfill these requirements of next generation RADAR systems. With the recent improvements, Silicon-Germanium Bipolar CMOS technology became a good candidate for recently used III-V technologies, such as GaAs, InP, and GaN, to meet high speed and performance requirements of present RADAR applications. As new process technologies are used, new solutions and circuit architectures have to be provided while taking into account the advantages and disadvantageous of used technologies.

In this thesis, a new T/R module system architecture is presented for single/on-chip X-Band phased array RADAR applications. On-chip T/R module consists of five blocks; T/R switch, single-pole double-throw (SPDT) switch, low noise amplifier (LNA), power amplifier (PA), and phase shifter. As the main focus of this thesis, a two-stage power amplifier is realized, discussed and measured. Designed in IHP's 0.25 μm SiGe BiCMOS process technology, the power amplifier operates in Class-A mode to achieve high linearity and presents a measured small-signal gain of 25 dB at 10 GHz. While achieving an output power of 22 dBm, the power amplifier has drain efficiency of 30 % in saturation. The total die area is 1 mm^2, including RF and DC pads. To our knowledge, these results are comparable to and/or better than those reported in the literature.

RADAR Uygulamaları için X-Bandında Güç Amfisi Tasarımı

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EE, Yüksek Lisans Tezi, 2011
Tez Danışmanı: Prof. Dr. Yaşar GÜRBÜZ

Anahtar Kelimeler: Faz Dizinli RADAR, T/R modülü, Güç Kuvvetlendiricisi, SiGe BiCMOS, X-Bandında entegre devre.

Özet

Radyo Algılama ve Menzil Tayini (RADAR) sistemleri ve iletişim elektroniğindeki gelişmeler düşük maliyetli, yüksek performansa sahip, küçük ve tek bir yonga üzerinde gerçeklenebilen Alıcı-Verici (T/R) modüllerinin tasarlanmasını gerektirmektedir. Gelecek nesil RADAR sistemlerinin bu gereksinimlerini karşılamak için yeni topolojiler ve teknolojiler aranmaktadır. Bu arayış içerisinde, son yıllarda büyük gelişme kaydeden SiGe BiCMOS teknolojisi günümüzde kullanılan III-V teknolojileri olan GaAs, InP ve GaN'ın yerine RADAR uygulamaları için gereken yüksek hız ve performans gereksinimlerini karşılayabilecek bir teknoloji adayıdır. SiGe BiCMOS gibi yeni bir teknolojinin RADAR uygulamalarında kullanımı, kullanılan teknolojinin avantaj ve dezavantajlarını göz önüne alarak yeni devre mimarisinin ve yeni sorunların ele alınmasını gerektirmektedir.

Bu tezde, X-Bandında çalışan faz dizinli RADAR sistemleri için yeni bir T/R modül mimarisi sunulmuştur. Bu T/R modülü; T/R anahtarı, tek-giriş çift-çıkış anahtarı, düşük gürültü kuvvetlendiricsi, güç kuvvetlendiricisi ve faz kaydırı blokları yer almaktadır. Bashi geçen ilk üç bloğun yanında, bu tezin odak noktası olan, iki-katlı güç kuvvetlendiricisi tasarlanmış, tartışılmış ve ölçülmüştür. IHP'nin 0.25 μm SiGe BiCMOS teknolojisinde tasarlanan bu güç kuvvetlendiricisi, yüksek doğrusallığa ulaşabilmesi için A sınıfı modunda çalıştırılmakta ve ölçüm sonuçlarına före 10 GHz'de 25 dB kazanca ulaşmaktadır. 22 dBm güç çıkışına sahip olan bu güç kuvvetlendiricisi % 30 drian verimi ile çalışmaktadır. RF ve DC çıkışlar ile beraber toplam kırmık alanı 1 mm^2'dir. Elde edilen bu sonuçlar literatürdeki diğer çalışmalarla karşılaştırılabilir veya daha iyi bir durumda olduğu görülmektedir.

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List of Abbreviations

AF	Array Factor
AM	Amplitude Modulation
BV_{CEO}	Collector-Emitter Breakdown Voltage
BV_{CBO}	Collector-Base Breakdown Voltage
CB	Common-Base
CCB	Constant Current Biasing
CE	Common-Emitter
CVB	Constant Voltage Biasing
DBF	Digital Beam Forming
DE	Drain Efficiency
DF	Direction Finding
EIRP	Equivalent Isotropically Radiated Power
FM	Frequency Modulation
FOM	Figure-of-Merit
GaAs	Gallium-Arsenide
HP	High Pass
IC	Integrated Circuit
IF	Intermediate Frequency
IL	Insertion Loss
InP	Indium phosphide
iNMOS	Isolated NMOS
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Pass
MEMS	Microelectromechanical System
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuits
mm-Wave	Millimeter-wave
MOS	Metal-Oxide-Semiconductor
MtM	More than Moore
OAE	Overall Efficiency
PA	Power Amplifier
PAE	Power-Added-Efficiency
PAWS	Phased Array Warning System
PS	Phase Shifter
QAM	Quadrature Amplitude Modulation
RADAR	Radio Detecting And Ranging
RF	Radio Frequency
RX	Receiver
SiGe	Silicon-Germanium
SPDT	Single-Pole Double-Throw
SSB	Single-Sideband
T/R	Transmit/Receive
TX	Transmitter
VGA	Variable Gain Amplifier

1 Introduction

1.1 A Brief History of Radar

RAdio Detecting And Ranging, more commonly known as RADAR, is an object-detection system which uses electromagnetic-waves to determine the distance, direction, speed, and more characteristics of both moving and stationary objects. RADAR has its early roots in World War II. The first military application of radar was employed by England as a defense against aircraft attacks by German bombers approaching England to drop their payloads [1].

With the progress in all fields in electronics, the value and complexity of radar systems progressed. Radar is now used for several commercial applications such as weather monitoring [2], auto collision [3], and as well as many military uses. Especially in military applications, radars using mechanically movable antennas have been, and still are, employed to increase the viewable area of the system, but the mass of the system limits the scanning rate which is limited to hundreds of scans per minute. Another method of steering is used in phased array radars where phase of the each individual aerial being controlled such that signal is reinforced in the desired direction. Electrically steerable systems are capable of hundreds of scans per second over wide viewing areas [4].

As time has progressed, so have the system architectures and the components. The magnetrons in the early times given way to systems utilizing vacuum tube based devices which have now been replaced by high performance solid state devices. Future trends in phased array radar are pushing for smaller, cheaper and multi-beam solid state systems with an ultimate goal of putting all radar blocks in a single module [5].

1.2 Modern Day Phased Array Radars

Phased array radar is the choice for modern applications, especially for military missile defense systems. Perhaps the most popular surface-to-air missile system utilizing phased array radar is the Patriot system that was widely used in The Gulf War in the early 1990s [6]. The system is modular and highly mobile in conjunction with a missile launching platform [7]. The rapid scanning of the phased array

Figure 1: Alaska District's 90-foot diameter phased array radar for missile warning and space surveillance.

radar improves the targeting capabilities of the system for single or multiple targets. Another example is a United States Air Force Space Command radar system called PAWS (Phased Array Warning System), as can be seen in Fig. 1 [8].

By the development of monolithic microwave integrated circuits (MMIC), the integration has reached the point where it can be possible to build a low cost phased array radar module operating at 35 GHz costing $30/element [9]. This makes possible to put all blocks on a single chip with low cost. Furthermore, the advances provided by Moore's Law has made it feasible to do the operations such as phase shifting and amplitude scaling for each antenna element digitally which is called digital beam forming (DBF) [10]. Besides it is now not futuristic to think about a new road-map, More than Moore (MtM) by creating and integrating various digital and non-digital functionalities such as Microelectromechanical systems (MEMS) and 3D integration to semiconductor products [9].

1.3 Phased Array Principles

Multiple antenna phased arrays can be used to change the direction of the overall antenna beam electronically [11]. By changing the phase of the exciting currents in each element, the radiation pattern and the gain of the array can be scanned through space.

A phased array receiver consists of several antennas and signal paths that com-

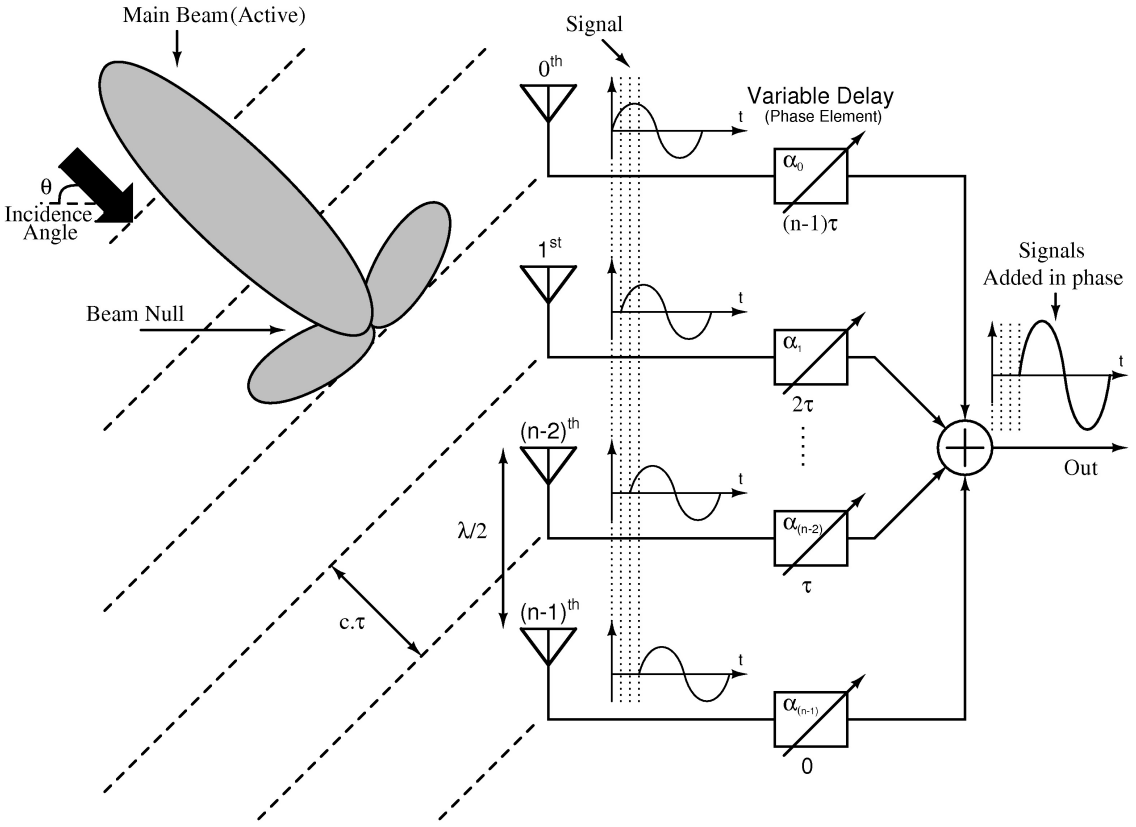


Figure 2: A simplified n-element phased array receiver.

bines signal received by each antenna element in a controllable way. In addition, a phased array transmitter works in the same manner where signal flow is in the opposite direction. The antenna elements of a phased array system can be arranged in different ways; one, two or even three dimensions depending on the application [12].

As mentioned before the principle of operation of a phased array is similar for both transmitter and receiver. Fig. 2 shows a simplified n-element phased-array receiver. If the incoming signal is assumed to be *s(t)* for each element, in the desired radiation angle, θ, and this signal is processed such that delay for each progressive element is a multiple of τ, the combined signal is given by [13],

$$S(t) = \sum_{k=0}^{n-1} s\left(t - k\tau - (n-1-k)\frac{d\sin\theta}{c}\right) \tag{1}$$

It means that the signals received by all elements and processed for the desired radiation angle formule add up coherently, where *(d)* is the spacing between elements and *(c)* is the velocity of the light. This coherent addition increases the gain of the

signal in the desired direction and decreases the reception of the array antenna in other directions called Beam Nulls, as shown in Fig. 2. It can be seen from (1) that in a N-element phased array transmitter, if the power radiated by each is element is assumed to be P watt, and array elements are assumed to be isotropic (A_0=1) and weighted by linear amplitudes, the antenna gain of the array will be N and the Equivalent isotropically radiated power (EIRP[1]) in the main beam direction will be $P \times N^2$ watts. For example, if each transmitter in a four-element phased array system radiates 20 dBm, the EIRP of the system is increased by 12 dB ($2 * 10log_{10}(4)$) to 32 dBm, 6 dB by the antenna gain and 6 dB by the overall transmitted power. This increase in the signal power will be even more if thousands of elements are combined in a phased array system. It is worthwhile to mention that the same improvements will be available for the receiver case.

In a phased array receiver, the radiated signals from the target arrive at different time to each array element. With suitable phase adjustment and the spacing between elements, the angle of incidence can be directed to the desired angle. This enhances the received signal power in the incidence angle and degrades the received signal from other directions. The advantage of using phased array receiver is not limited to nulling out these interferences. A phased array also provides better sensitivity at the receiver part of the system [15].

1.4 Phased Array Architectures

Advances in silicon technology for integrated systems have resulted in high speed transistors operating beyond 200 GHz [16]. However, transistor speed is only one of the parameters for high performance phased array systems for millimeter-wave (mm-Wave) applications. Additional constraints imposed by the breakdown voltage, losses of integrated circuit for passive components, low power budgets, as well as cost and area of the modules have important impact on the overall system performance. Therefore, there are different proposed architectures for silicon based phased array systems and designer has to choose the architecture satisfies the requirements best [17, 18, 19].

[1]EIPR is defined as the amount of power that would have been radiated by an isotropic antenna to produce the peak power density observed in the direction of maximum antenna gain [14].

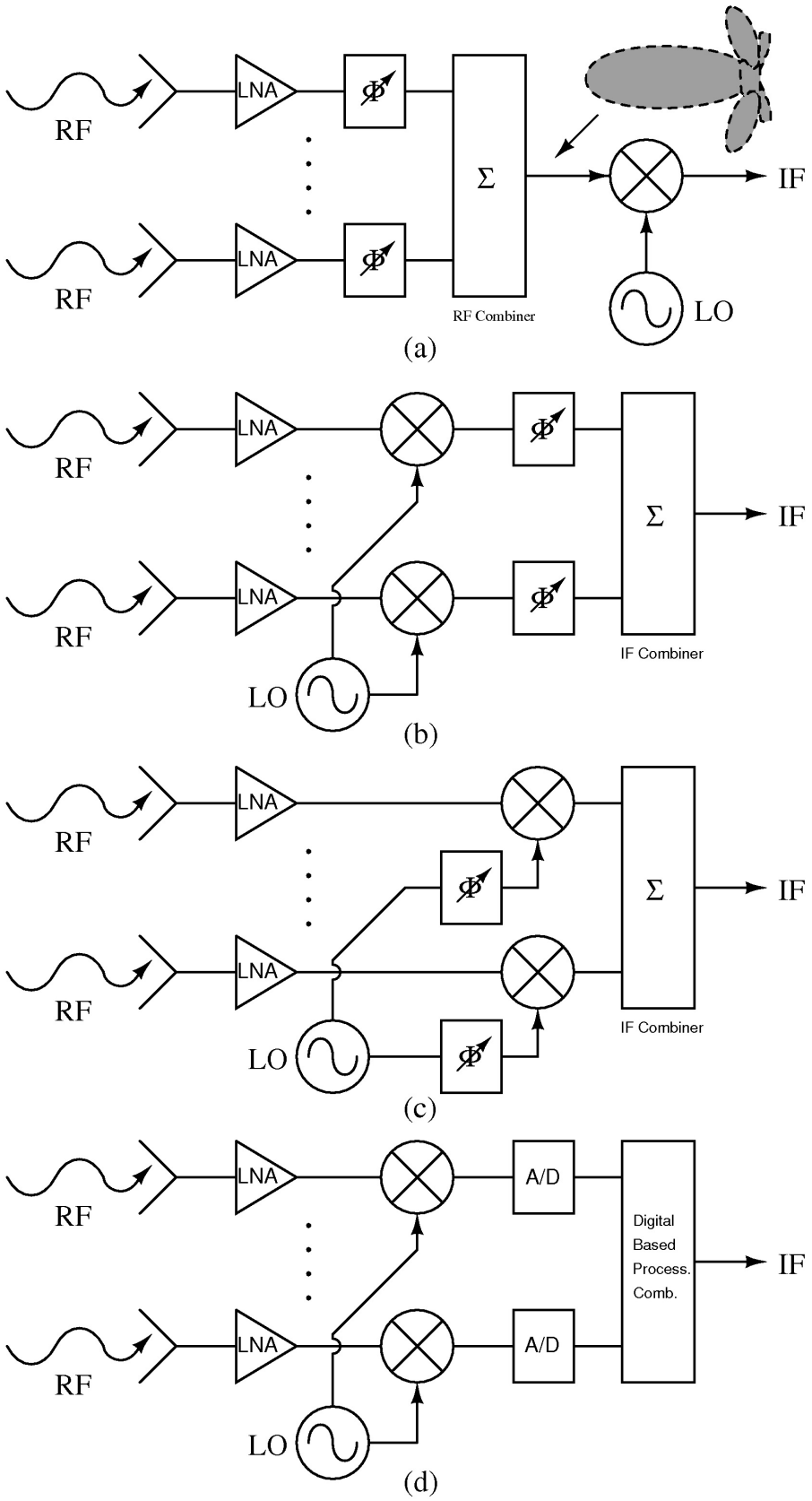


Figure 3: Phased array receiver architectures: (a) RF phase shifting, (b) IF phase shifting, (c) LO phase shifting, and (d) digitally phase shifting.

In ideal case, broadband variable delays are required to make all signal paths coherent for operating frequency range. Moreover, the gain of each delay stage should be independent of the delay. If the time delay and gain are not constant for different elements and also frequencies, this will result in inaccurate information about the target. For this reason, different architectures implementing phase shift at different stages of the phased array receiver is given in Fig. 3. The phase shift can be implemented at RF (Radio Frequency)-stage (All-RF architecture) (Fig. 3(a)), at IF (Intermediate Frequency)/Baseband-stage(Fig. 3(b)), at LO (Local Oscillator) stage (Fig. 3(c)), or digitally (Fig. 3(d)). The selection of the architecture depends, as always, on certain trade-offs in power consumption, cost and total area.

The All-RF architecture is the most compact and suitable architecture for silicon based integrated phased array systems because it requires only one mixer and LO signals at the IF-stage as shown in Fig. 3(a). On the other hand, IF and LO phase shifting architectures require large number of mixers which occupies more chip area and increases the power consumption. In addition, LO distribution is one of the important problems for these architectures where the required LO phase noise for phased array systems is very low (for example, -133 dBc/Hz at 1 MHz offset from a 10 GHz carrier [20]). The requirement of such high performance LOs can only be achieved by using external oscillators, and this usage increases the system area consumption and cost.

Furthermore, IF and LO phase shifting architectures require phase shifters in IF band. There have been some proposed on-chip phase shifters for low frequency operations but their size and performance do not make them suitable for on-chip phased array applications [21]. On the other hand, there is much more focus on the study of phase shifters for All-RF architecture [22, 23]. Even though losses are the biggest problem in RF phase shifters, variable gain amplifiers are utilized inside phase shifter blocks to compensate losses and phase variations to avoid array pattern degradation.

Another advantage of All-RF architecture over others is that the output signal is formed after the RF combiner and thus any interference can be substantially rejected before the following receiver units, as shown in Fig. 3(a). This will reduce the linearity requirements of rest of the receiver blocks. This requirement applies

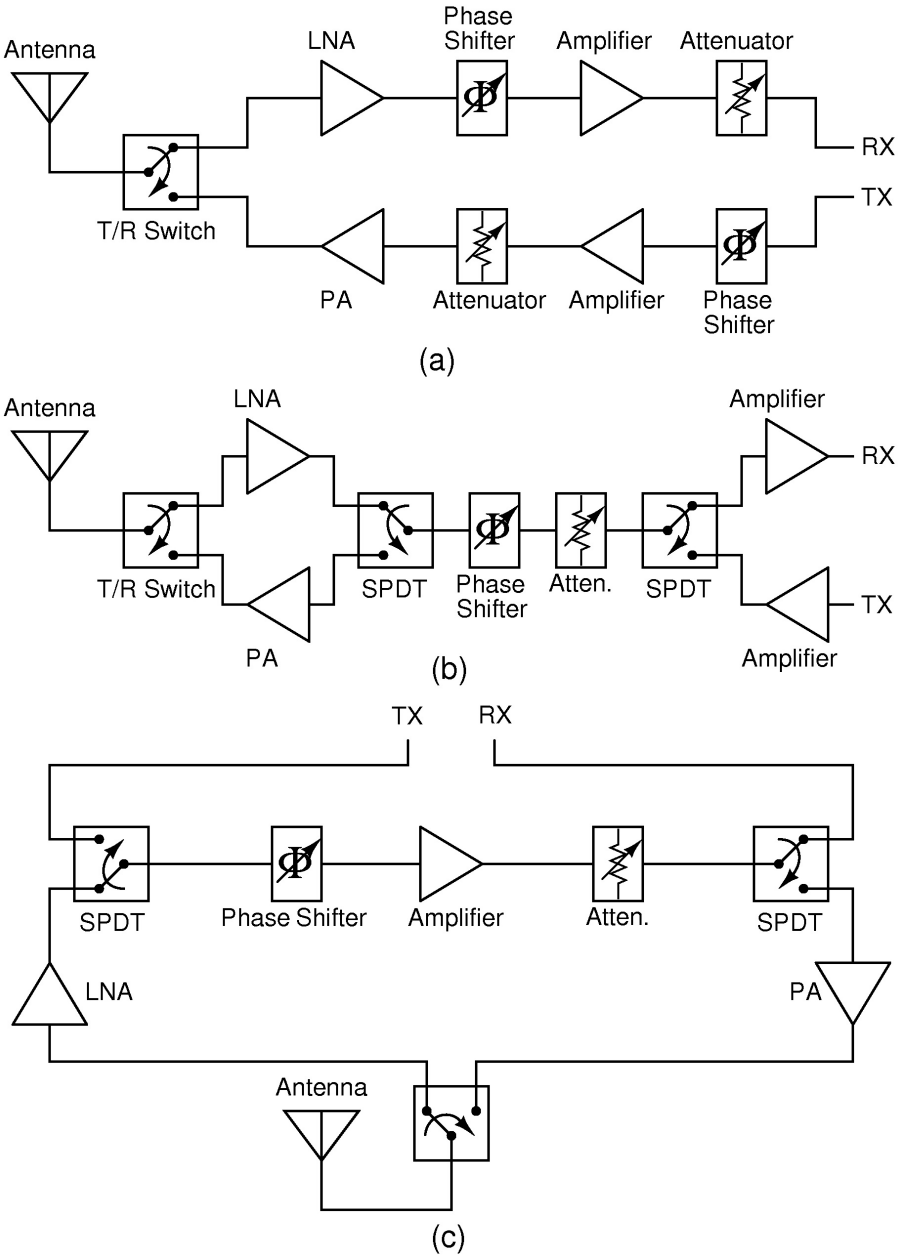


Figure 4: T/R module architectures for All-RF receiver.

even the digital beam forming (Fig. 3(d)) architecture where a high dynamic range analog-to-digital (A/D) is essential to accommodate all incoming signals without any distortion. Also, digital beam forming architecture requires both high-speed and large number of A/D converters which will increase the chip area and power consumption dramatically. However, digital signal processing is the only architecture where large number of beams can be processed simultaneously.

1.5 RF Phase Shifting T/R Module

The performance of a phased array system mainly depends on the performance of the transmit/receive (T/R) module utilized in this system. As discussed before, due to the superiorities to others in power consumption, linearity, area and most importantly cost, All-RF is selected as receiver architecture in this project. After now on, system architectures for All-RF receiver will be discussed. A T/R module includes a low noise amplifier (LNA), a power amplifier (PA), phase shifter, variable gain amplifiers (VGA), attenuators, single-pole-double-throw (SPDT) switches, and lastly T/R switch.

There are various system architectures that utilize phase shift in RF stage. In this part, three main architectures will be discussed. Fig. 4(a) is a T/R module block with two different transmitting and receiving paths. The usage of two phase shifters, attenuators and variable gain amplifiers increase the complexity and area of the system. These two paths can be combined in one using two SPDT switches as shown in Fig. 4(b). However, this module requires a bidirectional phase shifter and attenuator for signal flow in both directions which limits the number of sub-block topologies can be used. Moreover, high gain LNA is required to compensate the losses from phase shifter and SPDT switches and high isolation SPDT switches are required to prevent possible oscillations for LNA-PA-SPDT switch circular loop. To solve the bidirectional problem, Fig. 4(c) is introduced which solves the possible oscillation problem, allowing to use variable gain amplifiers which will relax linearity requirements for LNA.

The phase shifter is the most essential building blocks of a T/R module in All-RF architecture. Because the gain, directivity and side-lobe levels of the antenna array is determined by the spacing, amplitude weight and time delay of array elements, phase shifter and VGA are critical elements in a T/R module. The phase shifter can be either analog-type (continuous phase shift) or digital-type (step phase shift). Even though analog-type phase shifters offer higher resolution for phase shift, control circuitry of these type of phase shifter are more complex than digital ones and vulnerable to noise in the control line. Furthermore, digital-type phase shifters can be controlled without any power consumption with simple metal-oxide-semiconductor (MOS) switches in silicon technology.

The choice of a digital-type phase shifter starts with the selection of number of bits. For this analysis, antenna array theory will be discussed shortly. As mentioned before, in a receiver array with N elements spaced a distance d apart and a signal with the incidence angle θ, the delay for the n^{th} element will be

$$\tau_n = \frac{nd \sin(\theta)}{c} \tag{2}$$

therefore n^{th} element is required to add a phase shift of $\alpha_n = (N-n)\,\alpha$. As a result the output signal of the n^{th} element before combining all will be

$$I_n(t) = I(t-\tau_n)\cos(\omega_{RF}(t-\tau_n) - \alpha_n) \tag{3}$$

If the amplitude of the received signal is assumed to be same,

$$I(t) = I(t-\tau) = I(t-n\tau) = I_o(t) \tag{4}$$

and applying the approximation (3)

$$I_n(t) = I_o(t)\cos(\omega_{RF}(t-\tau_n) - \alpha_n) = \mathrm{Re}\left(I_o(t)e^{j\omega_{RF}t}e^{-j\psi n}\right) \tag{5}$$

where

$$\psi = \frac{\omega_{RF}\tau}{n} - \alpha \tag{6}$$

It is well known that for a special case of equally spaced linear arrays with equal amplitude, array factor (AF) is simply the summation of all received signals [24]

$$AF = I_o \sum_{n=0}^{N-1} e^{jn\psi} = I_o(1 + e^{j\psi} + ... + e^{j(N-1)\psi}) \tag{7}$$

with work on this equation, it simplifies to

$$AF = \frac{1-e^{jN\psi}}{1-e^{j\psi}} I_o = I_o e^{j(N-1)\frac{\psi}{2}} \frac{\sin(N\psi/2)}{\sin(\psi/2)} \tag{8}$$

and the $e^{j(N-1)\frac{\psi}{2}}$ term is not important unless this array antenna is combined with another array antenna. Neglecting the phase factor and normalizing the AF with

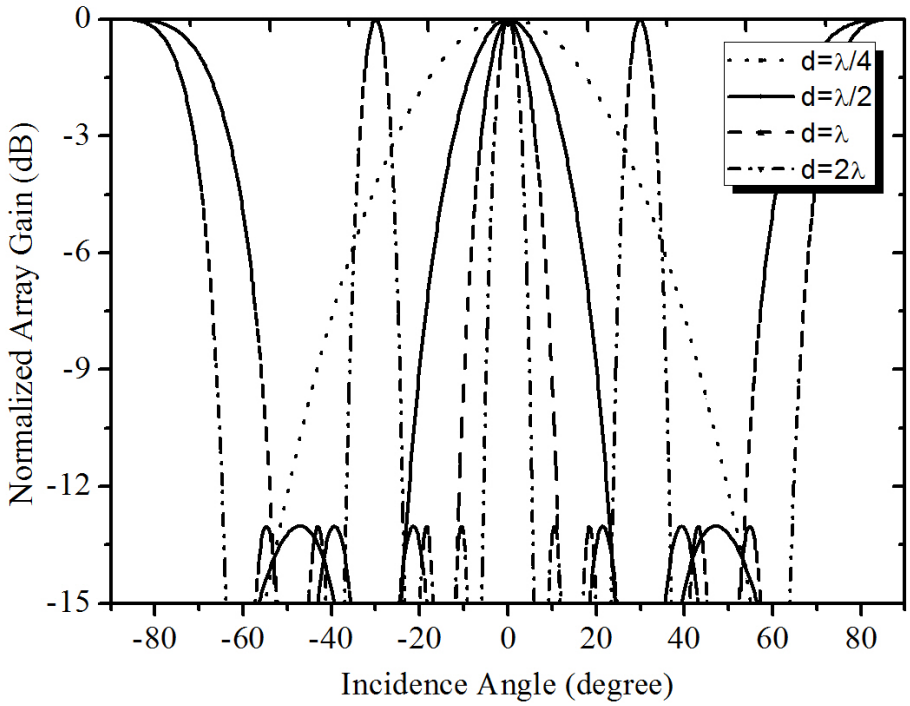


Figure 5: Four-element array pattern for different antenna spacing $\frac{\lambda}{4} < d < 2\lambda$

the maximum of this value which is $I_0 N$ gives the normalized array factor

$$f(\psi) = \frac{\sin(N\psi/2)}{N\sin(\psi/2)} \tag{9}$$

This is the normalized array factor for an N element, with uniformly excited, equally spaced linear array.

As a result, gain, directivity and side lobe levels depend on the number of elements, excitation and phase difference between each other. A larger distance between antenna elements results in less coupling and easier to fabricate but this degrades the directivity and resolution of the system. Fig. 5 shows the normalized array gain of a isotropic 4-element array for different antenna separation d. As shown in Fig. 5, higher than $\frac{\lambda}{2}$ separation between elements leads to grating lobes in the system. Also lower than $\frac{\lambda}{2}$ separation decreases the antenna directivity. Therefore, $\frac{\lambda}{2}$ is a good choice for the separation. Fig. 6 plots normalized antenna gain as a function of the angle of incidence for isotropic four-element (N=4) broadside phased array system with 22.5 degree (360 / 2^4) phase resolution where $d = \frac{\lambda}{2}$. As shown in Fig. 6, the incidence angle of a 4-element phased array antenna can have up to 60° incidence angle with isotropic antenna elements which limits the total scanning angle of the system. The code implemented in MATLAB for Fig. 5 and Fig. 6 is

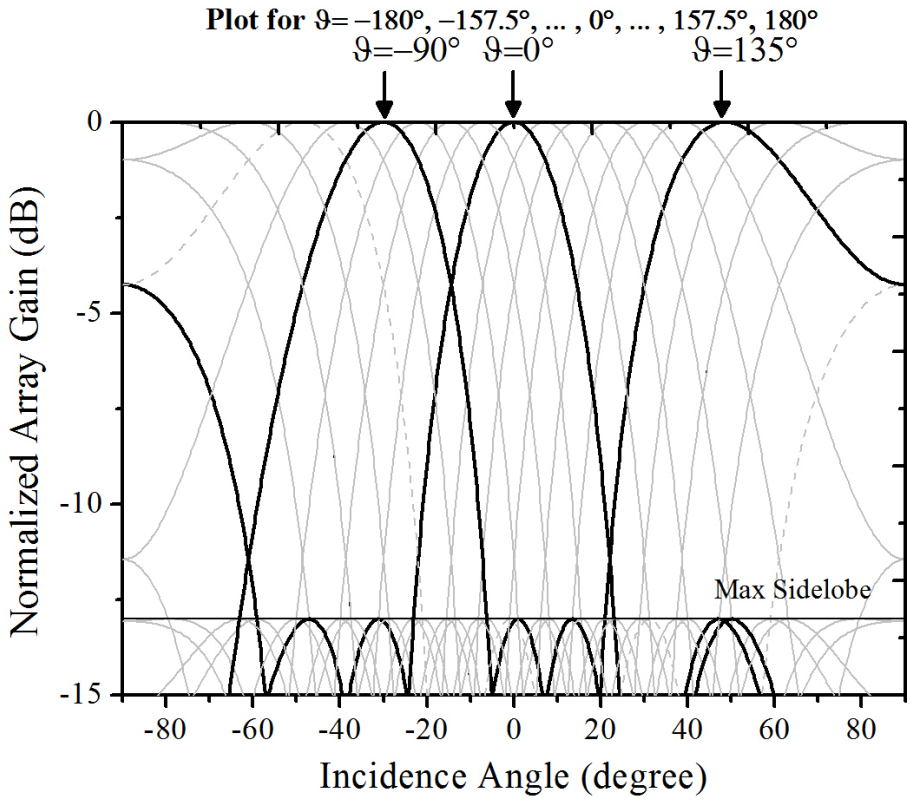


Figure 6: Four-element array pattern with uniformly spaced values of θ.

given in Appendix A and Appendix B, respectively.

1.6 Downsizing of T/R Modules

There are several proposed measure of performance for phased array radars [25, 26]. Three main figure-of-merits (FOM) are the power-aperture product for search (10), the power-aperture-gain product for track (11), and the power-aperture-gain-squared for track accuracy (12) given in [27], respectively as

$$FOM_s = PA \tag{10}$$

$$FOM_t = PAG \tag{11}$$

$$FOM_{t-a} = PAG^2 \tag{12}$$

where P_{avg} is the total transmit power, A is total effective aperture, and G is the gain of the phased array system. In an phased array system, these terms are not

necessarily independent and each of them can be defined as follows

$$P = P_e N \tag{13}$$

$$A = A_e N \tag{14}$$

$$G = G_e N \simeq \frac{4\pi A_e}{\lambda^2} N \tag{15}$$

where P_e,A_e and G_e are the transmit power, effective aperture and gain of a single element in a phased array system, respectively. Moreover, λ and N are already defined as the wavelength and the number of elements in this system. If (13), (14) and (15) are substituted in (10), (11) and (12), FOMs can be rearrange as

$$FOM_s = P_e A_e N^2 \tag{16}$$

$$FOM_t = P_e {A_e}^2 N^3 \frac{4\pi}{\lambda^2} \tag{17}$$

$$FOM_{t-a} = P_e {A_e}^3 N^4 \left(\frac{4\pi}{\lambda^2}\right)^2 \tag{18}$$

It is clear that figure-of-merit equations depend on P_e,A_e, N and λ. Increasing the transmit power of a single element, P_e, improves each FOM value in linear scale. However an increase in P_e means more power will be dissipated in each array element which will increase the heat and much more work will be required for cooling system. On the other hand, increasing the effective aperture of a single element provides a squared increase in the FOM_t and cubic increase in the FOM_{t-a}. But any increase in the effective aperture means the physical increase of the array antenna element and as shown in Fig. 5 increase of element spacing, d, more than $\frac{\lambda}{2}$ leads to grating lobes which will limit the performance of the system. As opposed to the prior changes, increasing the number of elements, N, in a phased array system gives the advantage of cubic improvement in the FOM_t. For the modern phased array systems, there has to be a limit for the increase of N because of the weight, power consumption and cost factors which are not included in any of *FOMs*.

Table 1: An example design demonstrating available improvement in required system power as a function of elemental power at a fixed value of $PAG = 100dB(Wm^2)$.

P_e (Watts)	Array Area (m^2)	System Power (kilo Watts)	Number of Elements
100	5.8	468	4,680
10	12.6	100	10,000
0.5	34	20	40,000
0.01	126	26	2,600,000

As shown in Table 1 [28], overall system power requirements decrease drastically with the increase of N while keeping PAG same for the system. However, the transmit power of a single element cannot be decreased small values such as 0.01 W because of the required number of element of the system shoots up over 2.6 Millions, which is not realistic. Therefore, choosing an array element with 0.5 W to 2W output power with around 25,000 to 40,000 elements will save more than 90 % of the system power with 5 times larger array area while increasing the total cost of the system. If it is assumed that for military applications power saving is more important than the cost, this trade-off seems to be feasible for phased arrays for military applications.

The current technologies based on Gallium-Arsenide (GaAs) and Indium phosphide (InP) are quite capable of satisfying the needs of T/R modules used in phased array systems especially for X-band applications. The integration of different chips in addition to the digital control circuitry on the same board both lower the system performance and increases the cost and area of a T/R module. However, a technology which easily integrates digital circuitry and RF blocks with high frequency transistors on the same die with lower cost and smaller area such as Silicon-Germanium (SiGe) based integrated circuits (ICs) can be a strong candidate to be considered to perform full T/R system for phased array systems.

1.7 Selected Technology: SiGe

The ready availability, ease of handling and high quality dielectric fabrication with vast investments in research and infrastructure lead Silicon to be the integrated circuit of substrate choice for the last decade. In addition, the Moore's type of

Table 2: Relative performance comparison of different IC technologies (Excellent: ++; Very Good: +; Good: 0; Fain: -; Poor: –).

Performance Matrix	SiGe HBT	Si BJT	Si CMOS	III-V MESFET	III-V HEMT
Frequency response	+	0	0	+	++
1/f and phase noise	++	+	-	- -	- -
Broadband noise	+	0	0	+	++
Output conductance	++	+	-	-	-
Transconductance/Area	++	++	- -	- -	-
CMOS integration	++	++	N/A	- -	- -
IC cost	0	0	++	-	–

scaling of transistors with supply voltage while maintaining high yield gave rise to mass-produced high transistor-count technology that is a cost-effective solution for integrated circuits with acceptable performance [29, 30]. Unfortunately, the small band-gap of Silicon limits the frequency performance of transistors in this technology that makes Silicon a poor competitor for mm-Wave solutions. On the other hand, compared to Silicon, III-V technologies like GaAs, InP and GaN can provide devices with higher performance, especially for mm-Wave circuits, but these technologies are not preferred for cost-sensitive consumer applications, instead used only where high performance is required like military applications.

There have been lots of research going on to improve the frequency performance of Silicon and this has driven band-gap engineering research for this substrate. The most effective solution introduced by Kroemer was the addition of Germanium to the base of a Silicon transistor [31]. Germanium addition allows inherent Silicon band-gap to be tuned which, in return, greatly increases the operating frequency of the transistor. Moreover, Ge composition is graded across the base region which generates and electric field and accelerates minority carriers and again improves the frequency performance. At the end, with an additional step to a typical Silicon fabrication process, the SiGe BiCMOS technology provides high frequency performance with minimal cost, as compared to other technologies in Table 2 [32].

Improvements on Silicon technology gave rise to a high performance SiGe technology that can compete with other III-V technologies. The main advantage of SiGe is the level of integration with conventional Silicon CMOS technology which supports the main building blocks of digital circuits. In conventional T/R modules

where digital control circuits are required, additional CMOS chips are utilized in addition to chips fabricated with III-V technologies. This increases the design complexity and degrades the performance of the module. Easy compatibility of CMOS blocks into SiGe BiCMOS overcomes this disadvantage of III-V technologies with comparable high frequency performance. Moreover, SiGe BiCMOS technologies take all the advantages of Silicon based IC manufacturing, such as yield, low cost and easy availability. All of these make SiGe BiCMOS technology a strong competitor to III-V technologies. There are several commercially available SiGe processes offered by the leading semiconductor companies like IBM, Hitachi, IHP Microelectronics, Infineon, Philips, TSMC etc.

From the perspective of RF systems, SiGe technology has advanced exponentially over the years, with the peak f_t and f_{max} in the excess of 250 GHz and 350 GHz, respectively [33]. For example, there is a project called DOTFIVE involving 15 partners from different European countries which has set its goal to fabricate SiGe HBT transistor with the f_{max} of 0.5 THz until 2013 at room temperature, a performance usually thought only possible with III-V technologies [34]. This means in following years, higher performances will be available using SiGe technology. Unfortunately, the same scaling that improve the operating frequency of transistors also leads to lower the operating voltage means lower breakdown voltages [30]. This phenomenon is very critical especially on the transmitter side of T/R modules where high output power as are required. Moreover, integration of passive components into Silicon substrate also presents problems due to interconnect losses and lossy substrate. While substrates like GaAs and InP are insulating (10^7–10^9 Ω-cm), the silicon bulk used in Silicon technologies and so SiGe technology has a conductivity from 5 $m\Omega$-cm to 10 Ω-cm. In the case of inductors, conducting substrate generates eddy currents in the substrate contributing losses which lower the quality factor of inductors. Even though there have been several solutions to prevent eddy currents in silicon substrate by patterned ground shields [35], the shielding under the inductor increases the parasitic capacitance of the inductor leasing to lower self-resonant frequency.

Table 3: IEEE frequency bands

Frequency Range	Wavelength	IEEE Band
300 kHz - 3 MHz	1 km to 100 meters	MF
3 - 30 MHz	100 meters to 10 meters	HF
30 - 300 MHz	10 meters to 1 meter	VHF
300 MHz - 3 GHz	1 meter to 10 cm	UHF
1 - 2 GHz	30 cm to 15 cm	L-Band
2 - 4 GHz	15 cm to 5 cm	S-Band
4 - 8 GHz	5 cm to 3.75 cm	C-Band
8 - 12 GHz	3.75 cm to 2.5 cm	X-Band
12 - 18 GHz	2.5 cm to 1.6 cm	K_u-Band
18 - 26 GHz	1.6 cm to 1.2 cm	K-Band
26 - 40 GHz	1.2 cm to 750 mm	K_a-Band
40 - 75 GHz	750 mm to 40 mm	V-Band
75 - 111 GHz	40 mm to 28 mm	W-Band
Above 111 GHz	millimeter wave (mm-Wave)	

1.8 Motivation

As a result, the objective of this thesis is to propose a solution for phased array T/R module that can replace III-V components with low cost, high yield SiGe BiCMOS technology while reducing the component count in the module. There are several applications for on-chip phased array T/R modules like mobile satellite systems for high data-rate communications at X-Band, weather radars at X-Band, automotive radars at K- and W-Bands, biological applications for on-skin scanning at W and 122-GHz ISM-Band and most importantly military defense systems such as radars at L, S, C, X, and K-Bands [36] where IEEE frequency bands are given in Table 3. Low frequency bands like L, S, and C-Bands make on-chip radar designs unpractical because of larger area requirements, especially because of passive components like inductors. However, there are several publications utilizing SiGe BiCMOS technology for T/R modules at X and K-Bands [37, 38].

As mentioned before, the low breakdown voltages and low-Q factor passive components are most significant obstacles toward achieving high power on SiGe technology. Utilizing such lossy components in the matching networks in transmitter-end will degrade maximum achievable output power and efficiency. In the receiver end, lossy components and transistors with low operating frequency will increase the total noise figure leading to lower receiver sensitivity. An attempt to integrate phased arrays into SiGe technology by replicating the topologies used in III-V technologies

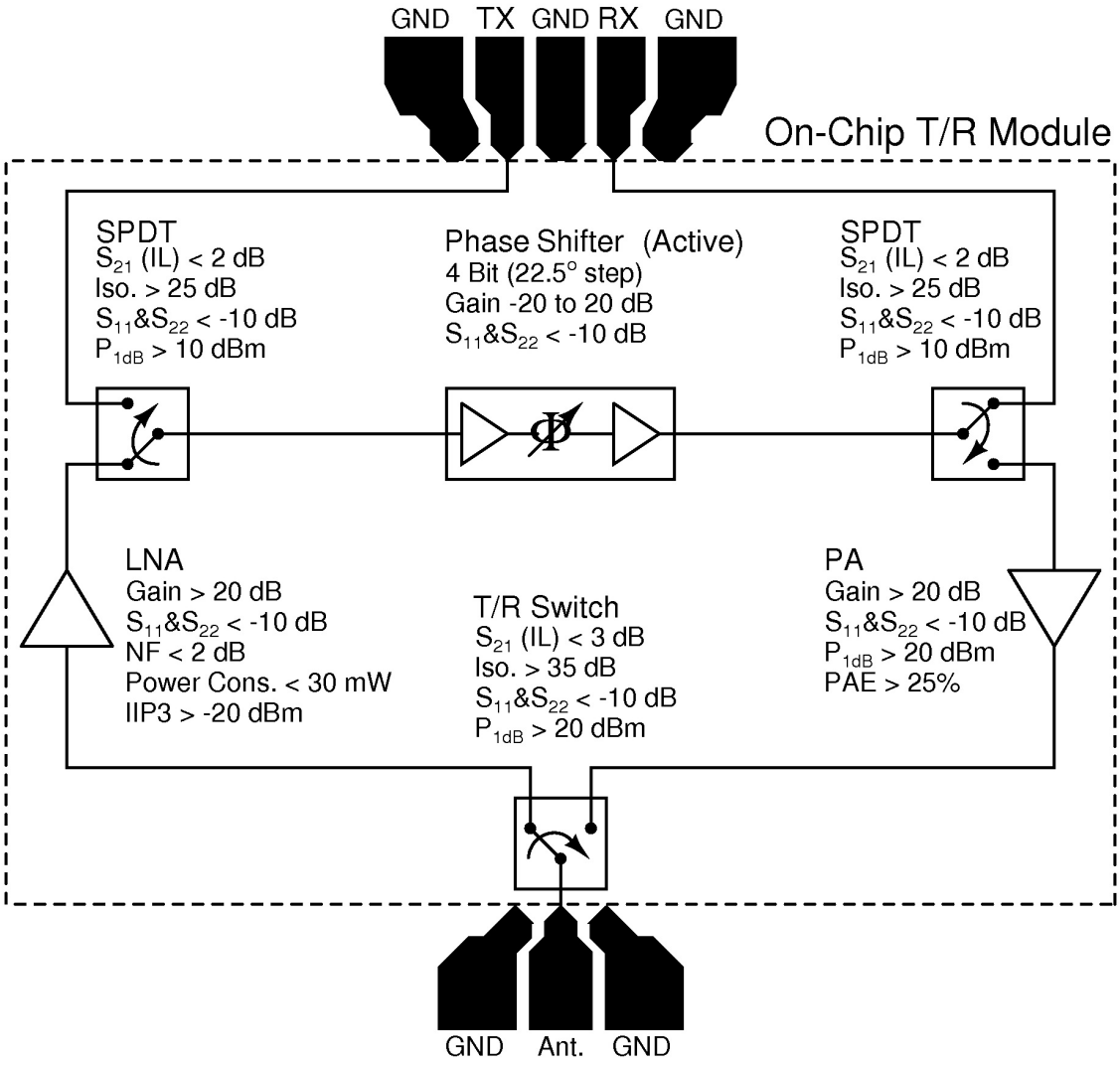


Figure 7: System block diagram of the proposed X-Band phased array T/R Module.

would be difficult due to unique challenges posed by this technology. Therefore, new solutions and new topologies have to be provided to overcome these problems specific to Silicon substrate and SiGe technology. Of all of the T/R module blocks, power amplifier present the greatest challenge due to high output power requirements of the system. As a result, this thesis aims to present techniques for improving breakdown voltages of SiGe power amplifiers and achieving more than 20 dBm output power with high gain for X-Band radar applications.

Fig. 7 shows the system block diagram of the proposed X-Band SiGe BiCMOS phased array T/R module with the performance specification of each block. In this T/R module all blocks, PA, LNA, T/R switch, SPDT and Phase Shifter are designed using IHP 0.25μm (SG25H3) SiGe BiCMOS technology.

1.9 Organization

Chapter 2 presents the proposed phased array T/R module with blocks designed in the project. The requirements and challenges of these designed blocks, T/R switch, SPDT switch and LNA will be briefly discussed. At the end of this chapter, simulation and measurement results of each block will be presented.

Chapter 3 introduces power amplifier fundamentals and specific approaches for achieving high output power such as cascode amplifier structure. It will be shown that employing different speed and different breakdown voltage transistors in cascode amplifier structure, the system requirement can be achieved.

Chapter 4 is an implementation of these techniques discussed in the previous chapter to achieve a two-stage cascode power amplifier. According to measurement results, the PA achieves more than 23 dB of gain with more than 25 % power-added-efficiency (PAE). Large signal measuremnt results show that the PA has a linear output power up to 22.2 dBm and a saturated output power of 23.2 dBm at 9 GHz. The resulting die size including RF and DC pads is 1 mm^2.

Chapter 5 includes an X-Band three-element phased array antenna with analog phase shifters designed as a course project in EE556 – Antennas & Propagation. As a proof of concept, implemented in Rogers substrate, Hittite Microwave HMC931LP4E phase shifters are arranged in circular array for direction finding at X-Band. Designed methodology, challenges and measurement results also will be presented in this chapter.

Chapter 6 concludes the thesis with a discussion on problems and possible future study.

2 The Proposed T/R Module

2.1 T/R Module

The initial development of the T/R module for phased array applications was introduced in Chapter 1. As mentioned in the previous chapter, blocks of the T/R module will be designed separately in order to understand the limitations of the design and technology. After testing each block separately, all blocks will be integrated on the same die, which we called as fully integrated T/R module. It is important to mention that dedicated effort will be required in the integration process due to several parameters like, die area, grounding, heat, noise and isolation. Therefore, we will focus on five of these blocks while attaching more importance to power amplifier.

In this chapter, four of T/R blocks are shortly introduced and measurement results of these blocks are provided. First of all, let's discuss the functionalities of these blocks while explaining the requirements of each block.

The connections and some important requirements of these blocks are given in Fig. 8. In the proposed architecture, there is one T/R switch which routes either receiver or transmitter stage to the antenna and two identical SPDT switches again for the same purpose as T/R switch. Moreover, low noise amplifier is the first block in the receiver path and power amplifier is the last block in the transmitter path. Finally, phase shifter, which is the main block for phased array systems, is used for both the receiver and transmitter path.

The specifications of the T/R switch are determined considering both in receiver and transmitter mode. In the receiver mode, losses of initial blocks, which are the T/R switch and low noise amplifier in the proposed architecture, degrade the noise performance of the T/R module. Therefore, insertion loss of the T/R switch is required to be as low as possible to minimize the noise performance. On the other hand, leakage signal from power amplifier to low noise amplifier in the transmit mode, also, has to be as small as possible to prevent oscillation and wrong information. To do so, the isolation performance of the T/R switch is needed to be as high as possible. For this reason, a few techniques are used to improve the isolation performance. Finally, high power performance is an essential criterion to handle high power signal from the power amplifier, which is higher than 20 dBm. For every

block, input and output ports are required to be matched to 50 Ω. This criterion is only required to able to measure every block individually and, in the integration step, blocks can be matched to each other directly.

Secondly, the specifications for the SPDT switch are also same as the T/R switch where insertion loss is the most important parameter. However, the isolation and power handling performance of this block is not very important because the SPDT switches are located in the input and output stages of the phase shifter. Therefore, techniques used in this switch are mostly focused on to minimize the die area.

Thirdly, low noise amplifier is one of the essential blocks in the system which determines the noise performance. Therefore, noise figure is the most important parameter and most of the effort spent to minimize it. In addition, gain of the low noise amplifier also improves the noise performance of the overall system while minimizing the contributions of following blocks such as SPDT switches and phase shifter. As a result, a two-stage, high-gain low noise amplifier is designed. Finally, linearity of this block is not very critical because it is assumed that very low signals

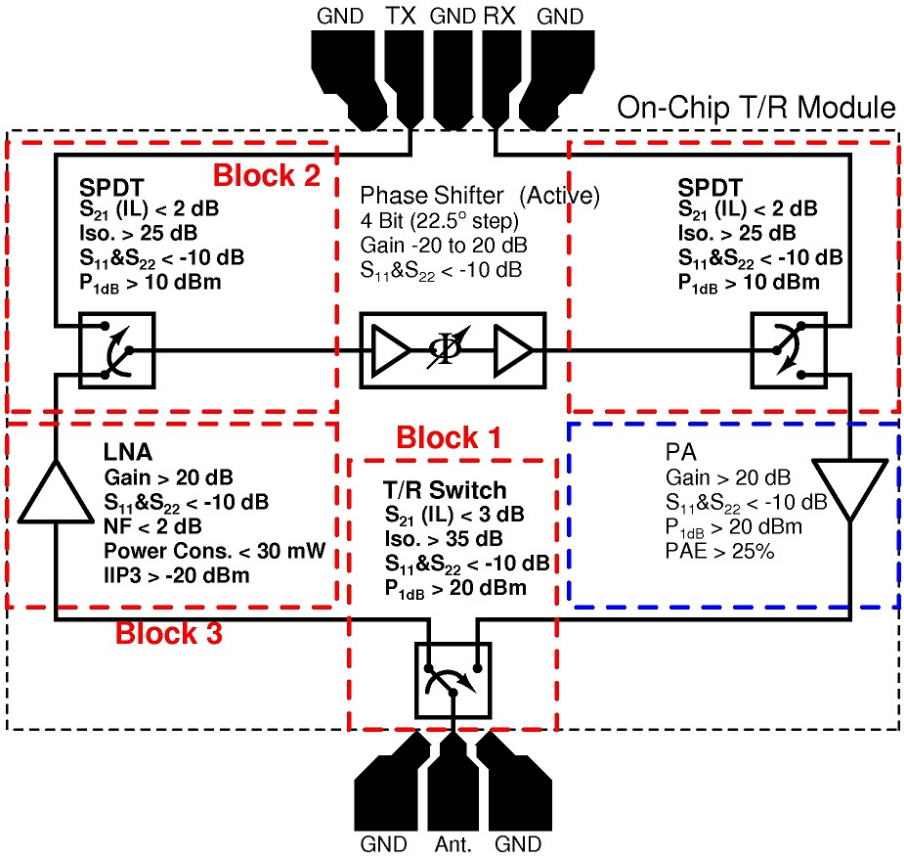


Figure 8: Blocks of the X-Band phased array T/R module.

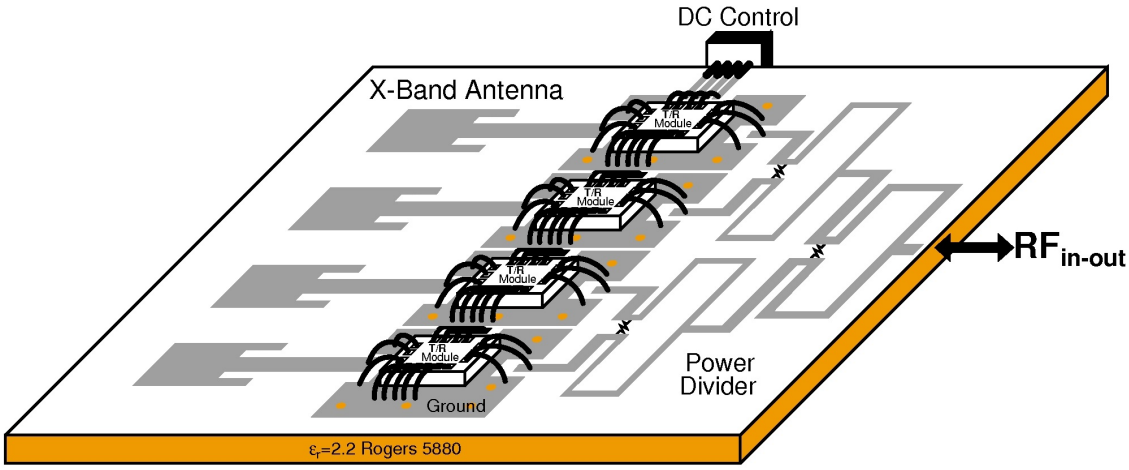


Figure 9: Four-element phased array T/R module with antenna elements.

will be received by the antenna array.

Another block in the T/R module is the phase shifter which is very important for the scanning phenomena of the phased array system. The sensitivity of this block also determines side-lobe, grating-lobe and main-lobe levels as well as scanning angle of the array. In other words, step-size of the phase shifter has to be minimized to get highest sensitivity and side-lobe levels. However, there is a practical limit for the step-size which is determined by number of bits in the digitally-controlled phase shifters and non-digitally in the analog phase shifters. In both of these phase shifters, noise-level and mismatches limit the step-size or sensitivity of this block. In the proposed architecture, a 4-bits digitally-controlled phase shifter is planned to be used, as shown in Chapter 1, and the array simulations are performed in this way. In addition to the phase, the amplitude of the processed signal is also determined by the phase shifter. As discussed in Chapter 1, the amplitude of each element can be changed to lower side-lobe levels, improve directivity and compensate the losses of blocks in the T/R module.

The final block in the T/R module is the power amplifier, which is the main focus of this thesis. The output power of this block is mainly determined by the used technology and cannot be increased to several Watts. Therefore, the main goal of this block is to get as much as output power as possible by a 50 Ω load. Therefore, a two-stage, high-gain power amplifier is designed and details of this block will be discussed deeply in the following chapters.

Although it is not in the scope of this thesis, a full demonstration of the T/R

module is required to understand the real-life performance. For this purpose, a X-Band antennas are required to measure the signal levels and scanning performance. As shown in Fig. 9, the T/R module will be mounted on a printed circuit board including power dividers and antennas for testing. The input power with the same input amplitude an phase is applied to each T/R module. The phase and amplitude of each T/R module is controlled by phase shifters in the module. To complete the system shown in Fig. 9, first a full T/R module has to be designed and measured. However, before this level, a simple 10 GHz microstrip patch antenna is designed and measured for direction fidning, as detailed in Chapter 5.

2.2 Designed Blocks

In this chapter, designed three blocks of the architecture are presented. First, the T/R switch design steps, simulation and measurements are provided. In Section 4.2, SPDT switch details and results are discussed. LNA design and simulation results are given in Section 4.3 and lastly, future work of the T/R module is presented.

2.2.1 Block 1 - Transmit/Receive (T/R) Switch

One of the circuit blocks essential to the envisioned X-Band T/R module is the transmit/receive or so called T/R switch. As shown in Fig. 10, T/R switch routes antenna either receiver (RX) or transmitter (TX) having a common port connected to antenna. The system specifications require T/R switch to operate from 8 GHz to 12 GHz, having a return loss better than 10 dB for each port, an insertion loss (IL) lower than 3 dB to minimize noise performance of the system, isolation higher than 35 dB to prevent signal leakage to the receiver route in the TX mode, 1 dB output compression point better than 20 dBm to handle signals with high power and minimum power dissipation.

2.2.1.1 Design

Fig. 10 shows the circuit schematic of the designed T/R switch. This switch mainly depends on series-shunt topology in [39]. M1 and M2 transistors perform the main switching function of directing the signal between TX/ANT and RX/ANT ports. M3 and M4 transistors are used to improve the isolation between TX and RX

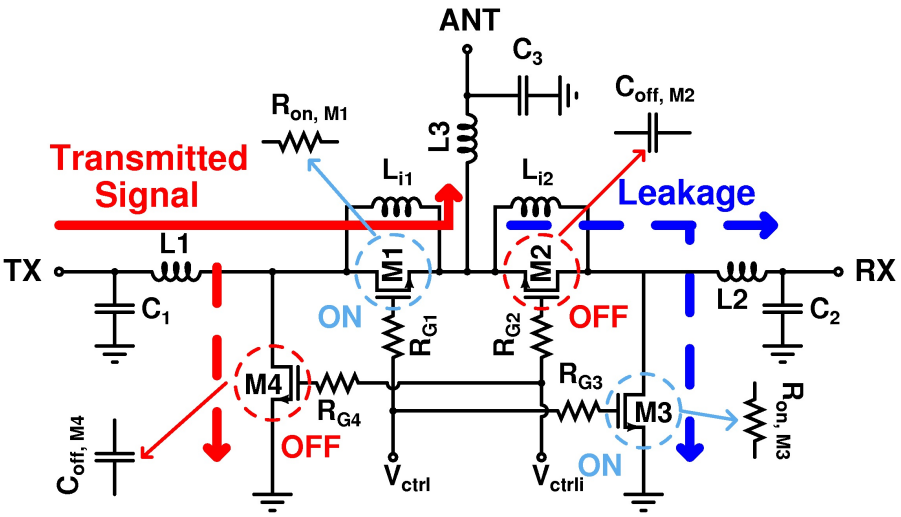


Figure 10: Circuit schematic of the T/R switch.

port while grounding the leakage signal. When V_{ctrl} is high, M1 and M3 transistors operate in deep triode region (ON state) meanwhile M2 and M4 transistors operate in the cuts off region (OFF state). Because channel resistance of M1 is very low, it creates a low impedance path between TX and ANT ports for incoming signal. Since M2 operates in the OFF state, the channel resistance is very high and RX port is isolated from TX and ANT ports. Moreover, M3 transistor has also a low resistance channel and grounds any leakage signal from M2 transistor which improves the isolation. Finally, M4 transistor operates in the cut off region and does not have any effect on the incoming signal from TX port but has the same functionality as M3 in the RX mode.

One of the figure-of-merits for T/R switch is the insertion loss which determines the noise performance of the system thus optimizations are performed to minimize

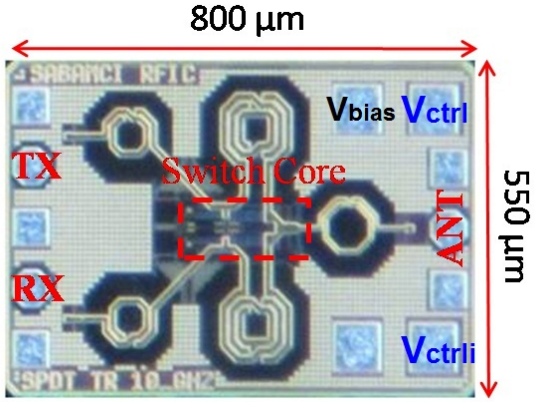


Figure 11: Die photo of the designed T/R switch.

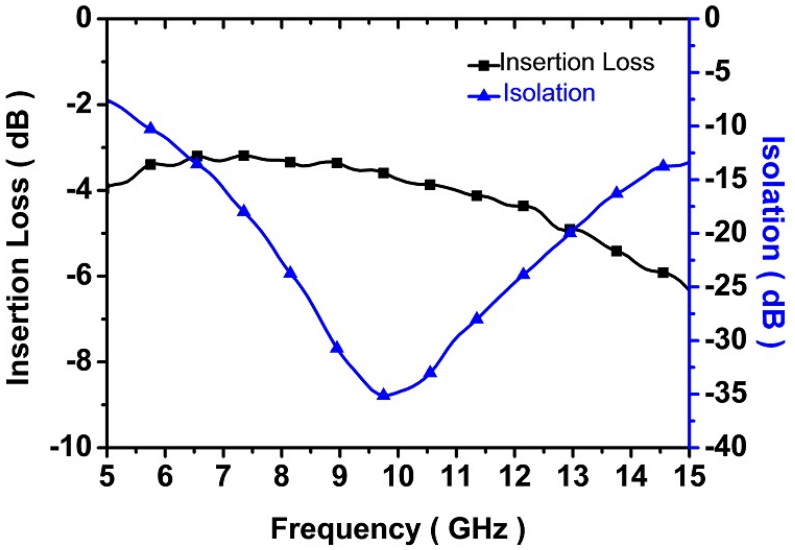


Figure 12: Measured insertion loss and isolation of the T/R switch.

IL. Because a MOS transistor can be modeled as a resistor, R_{on} in the ON state, the channel resistance has to be minimized to decrease the insertion loss of the switch. As known, the resistance of a MOS transistor operating in the triode region is inversely proportional to mobility (μ), aspect ratio (W/L) and gate to channel voltage (V_{GS}). Because μ, minimum length, L, and V_{GS} are limited by the used technology, maximum available width, W, has to be chosen to minimize the IL. However, there is a practical limit in increasing transistor width since as the width is increased, source/drain to body parasitic capacitances and in return coupling to substrate becomes significant and consequently insertion loss increases [40]. Increase in the parasitic capacitance also increases the OFF state capacitances of the transistor which leads to more coupling to undesired port. Therefore, there is a trade-off between R_{on} and parasitic capacitances which results in optimum value for width of the transistor that is 600 μm.

In addition to transistor widths, some other techniques such as body-floating, impedance transformation network, parallel resonance and source/drain biasing are used to improve the power handling, isolation and insertion loss of the T/R switch [41].

2.2.1.2 Measurement Results

As was the case for the PA, the T/R switch was also fabricated in IHP, 0.25 μm SiGe BiCMOS process technology. The die photo of the designed switch is given in

Fig. 11. The chip, including pads, occupies 0.44 mm^2 chip area. Inductors in the chip are custom designed using SONNET. Measurements are performed under 2 V V_{bias} voltage, 4.5 V and 0 V control voltages. Insertion loss and isolation between TX and RX ports are shown in Fig. 12. The insertion loss is between 3.2 dB and 4.1 dB at X-Band. In addition, isolation between TX and RX ports is also between 23.2 dB and 42.5 dB at X-Band. The return loss at TX port, S_{11} is 18 dB at 10 GHz and ranges from 16 dB to 19 dB at X-Band, as shown in Fig. 13. Due to the symmetry of the switch, RX performance is the same as the TX performance. As shown in Fig. 14, the switch results in an input 1 dB compression point (P_{1dB})e of 28.2 dBm at 10 GHz.

As a result, the designed switch meets all requirements of the system except the insertion loss which is higher than 3 dB. Although a new T/R switch is designed, the same insertion loss performance is measured. According to the analysis done after measurements, large width values of switching transistors M1 and M2, shown in Fig. 9, results in the degradation of the insertion loss. We deduced that after the measurements of the SPDT switch which is presented in the next section. In any way, the designed T/R switch is good enough and will be used in the full-system design.

Table 6, at the end of this chapter, compares the performance of the designed

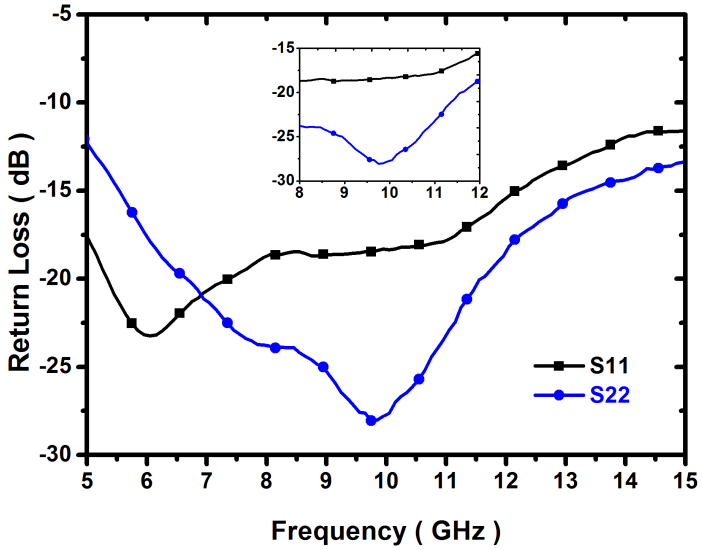


Figure 13: Measured input and output return losses of the T/R switch.

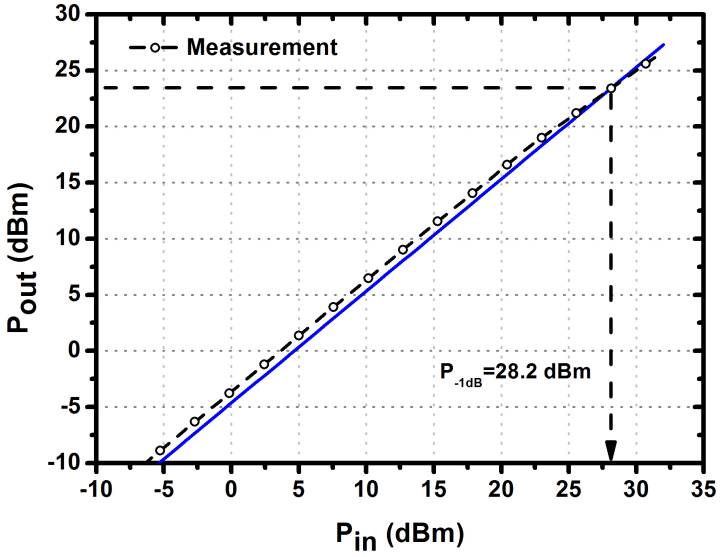


Figure 14: Measured 1 dB compression point (P_{1dB}) of the switch at 10 GHz.

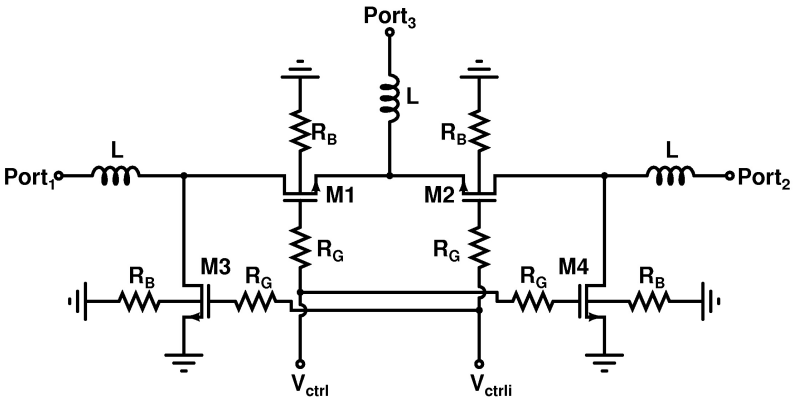


Figure 15: Circuit schematic of the SPDT switch.

switch with that of the single-ended CMOS T/R switches, operating at X-Band [42, 43, 38]. According to this comparison, this work achieves the highest power handling capability among the CMOS X-Band switches to up to the date, to the best of our knowledge.

2.2.2 Block 2 - Single-pole Double-throw (SPDT) Switch

The second block in the proposed X-Band phased array T/R module, as shown in Fig. 8, is the single-pole double-throw (SPDT) switch. There are two identical SPDT switches in the overall system with similar functionality. The main function of the first SPDT switch is to direct the incoming signal from LNA or transmitter port to Phase Shifter (PS). The functionality of the second SPDT switch is opposite

of the first one. Because of the simpler functionality and requirements than T/R switch which is required to have high isolation and power handling capability, the SPDT switch design is not complicated as T/R switch. Therefore, we will discuss the design details in short.

2.2.2.1 Design

Fig. 15 shows the circuit schematic of the designed SPDT switch. Similar to T/R switch, SPDT switch also depends on series-shunt topology consisting of four transistors. Again M1 and M2 perform the main switching activity while M3 and M4 improve the isolation performance. Similar to T/R switch on-chip input and output matching networks, mainly inductors L, are custom designed. In this design, iNMOS transistors are used for body-floating technique to improve the power handling performance. Moreover, gates of all transistors are biased though large gate resistors R_G to make the gates of transistors float at AC signals and prevent signal coupling. Without these resistors, variations would occur for gate to channel voltage V_{GS} and insertion loss would vary with different RF signal levels. On the other hand, these gate resistors with combination of gate capacitors affect the switching time that is defined as the time required for switch to change from receive mode to transmit mode or vice versa. However, insertion loss requirement outweigh switching time requirement since the switching time is not usually a limit.

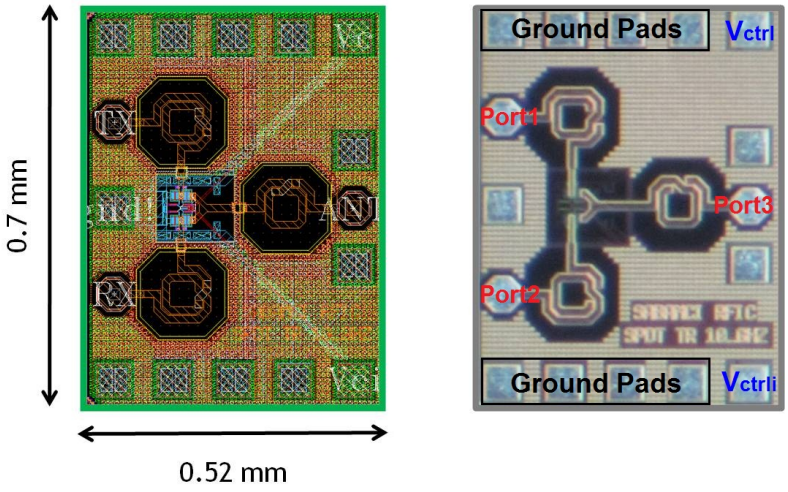


Figure 16: The layout and die photo of the SPDT switch.

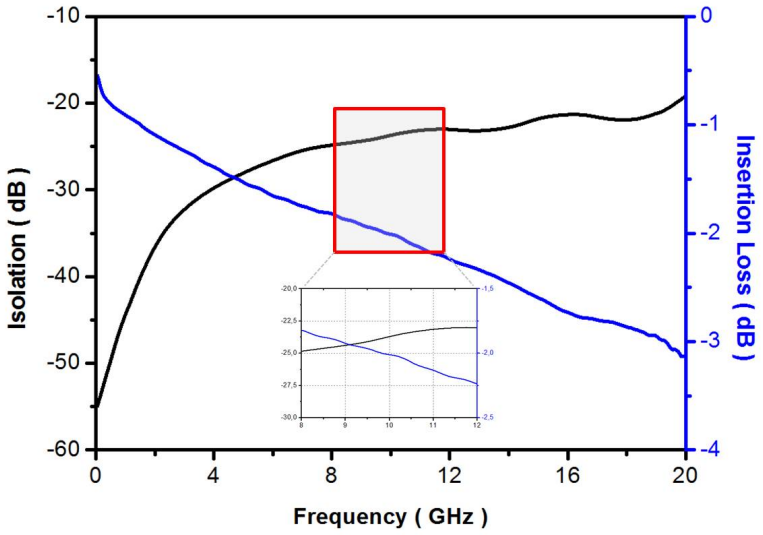


Figure 17: Measured insertion loss and isolation of the SPDT switch.

2.2.2.2 Measurement Results

As a result, a simple CMOS SPDT switch is designed for moderate performance requirements. The layout and die photo of the designed SPDT chip is shown in Fig. 16. Including DC and RF pads, the switch occupies 0.36 mm^2 (0.7 mm x 0.52 mm) chip area.

According to measurement results, the SPDT switch presents an insertion loss between 1.8 and 2.25 dB for the X-Band and lower than 3.2 dB for 0-20 GHz, as shown in Fig. 17. Moreover, the switch achieves isolation better than 23 dB for the X-Band and better than 20 dB up to 20 GHz. This means that the designed switch can be used for a wide range up to 20 GHz with an acceptable insertion loss and isolation performances. As it is mentioned before, lower insertion loss than T/R switch is achieved for the SPDT switch. This can be resulted from the smaller aspect ratio (W/L) transistors utilized in this design. Therefore, the requirements for the insertion loss can be achieved by utilizing smaller aspect ratio for T/R switch. Lastly, input and output return loss measurements which are better than 10 dB from DC to 20 GHz are shown in Fig. 18.

2.2.3 Block 3 - Low Noise Amplifier (LNA)

The third block designed for the proposed X-Band phased array T/R module, as shown in Fig. 8, is low noise amplifier (LNA). LNA is one of the most important

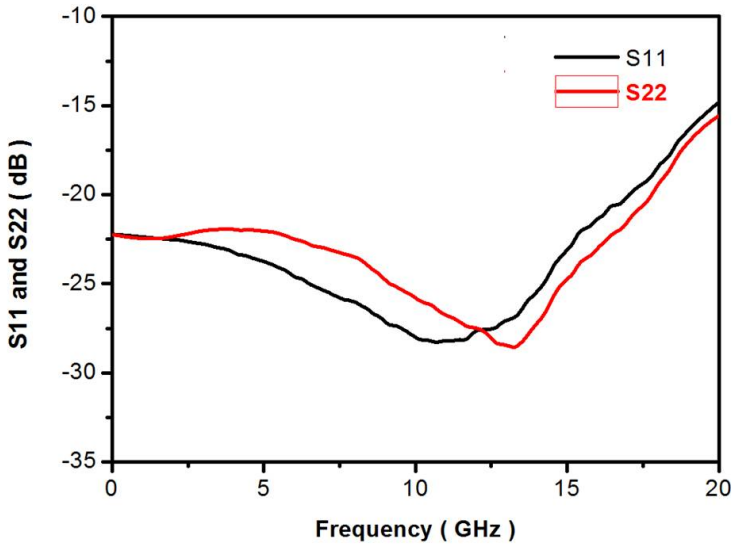


Figure 18: Measured input and output return losses (S11 and S22) of the SPDT switch.

blocks for a transceiver system because LNA mainly determines the performance parameters related to noise figure (NF) of the system. Therefore, the main aim of a LNA design is to minimize the noise figure of the block while having as much as gain possible. This statement is formulated as

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + ... + \frac{NF_m - 1}{A_{p1}...A_{p(m-1)}} \tag{19}$$

which is called the Friis equation [44]. Expressing the overall noise figure in terms of noise figure of each block, this relationship proves the importance of noise figure and gain of initial blocks in the system.

According to the system requirements, LNA is designed to have more than 20 dB gain, less than 2 dB noise figure, power consumption of lower than 30 mW and lastly IIP3 higher than -20 dBm for high dynamic range applications.

2.2.3.1 Design

To meet the gain requirement, a two-stage LNA is designed with cascode topology. Although cascode topology posses slightly increase NF compared to common emitter topology and results in reduced output voltage swing, frequency stability at higher gains and higher isolation by avoiding Miller capacitance of Q1 transistor are biggest advantages of this topology. Because of these reasons, cascode topology is

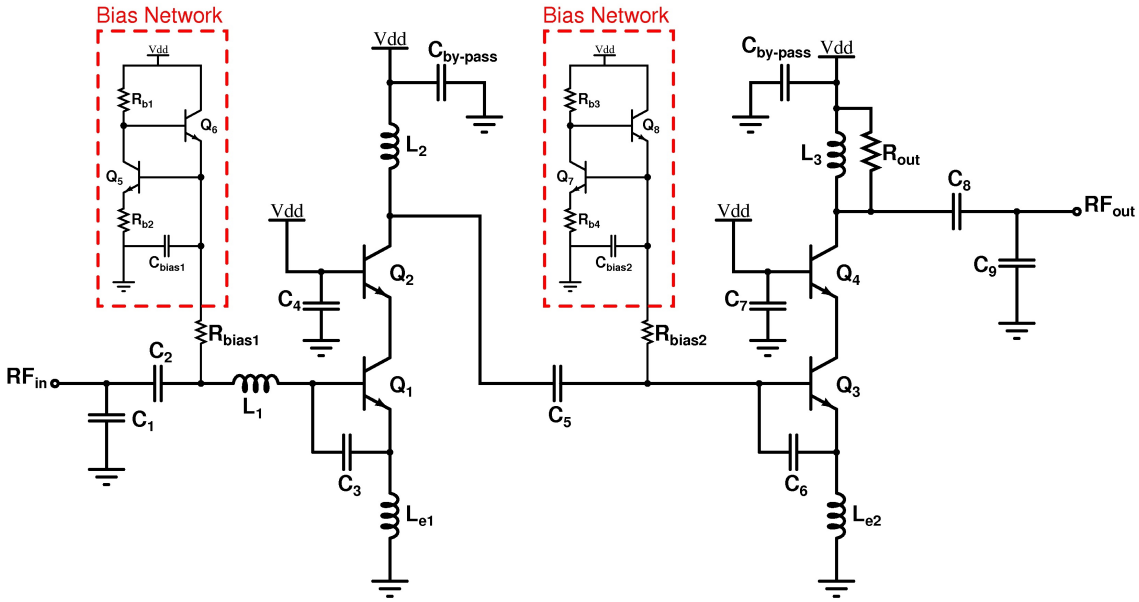


Figure 19: Circuit schematic of the designed LNA.

chosen. Moreover, two-stage amplifier is implemented to achieve gain more than 20 dB. The schematic of the designed LNA is given in Fig. 19.

First stage of the amplifier is biased for minimum noise figure whereas the second stage is biased for high dynamic range and IIP3. The inductors L_{e1} and L_1 performs both well-known simultaneous input noise-power match and power match to 50 Ω. As it has been in PA design, fastest (with maximum cut-off frequency) transistors of the used technology are selected to minimize NF of the amplifier. On the other hand, second state of the amplifier is biased for maximum output power and, hence,

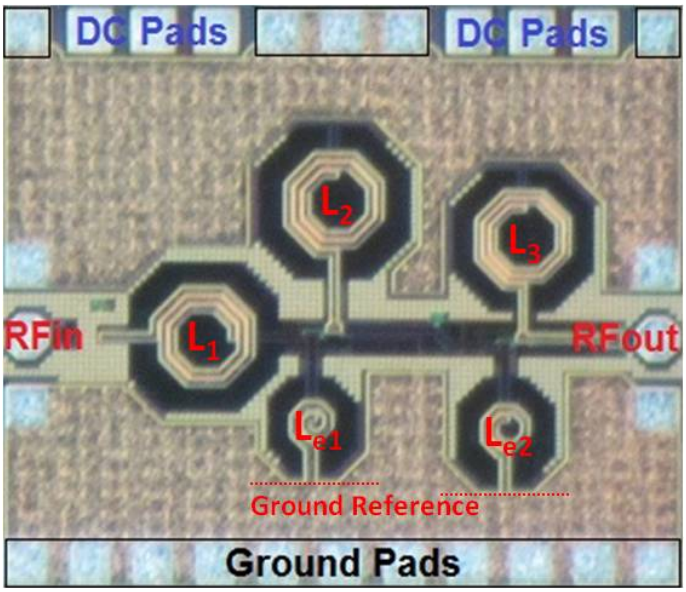


Figure 20: Die photo of the designed LNA.

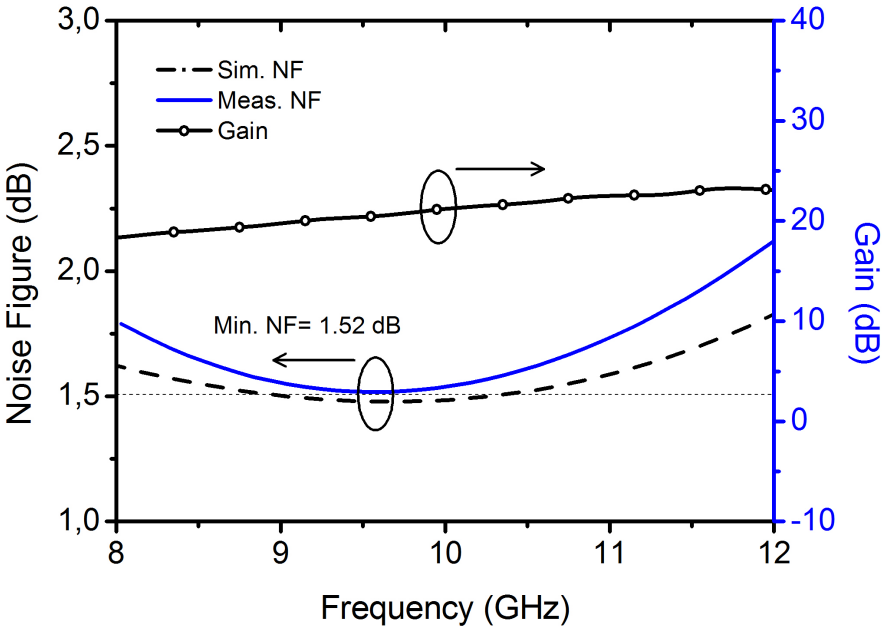


Figure 21: Measured NF and S21 performance of the designed LNA.

higher dynamic range.

In both stages, special biased circuit for temperature compensation and constant current generation is used in both of the stages, as shown in Fig. 19. Resistors, R_{bias1} and R_{bias2}, are used to determine the bias current and to make the output impedance of the bias circuitry in order to reduce the noise contribution. Moreover, capacitors, C_{bias1} and C_{bias2}, are used to filter out any noise generated by the bias network and prevent noise from affecting the noise performance of the amplifier. Transistors, Q_6 and Q_8, increase the accuracy of the current mirror.

Lastly, a special importance is paid to lower noise contribution from substrate in the layout step. Moreover, top metal of the chip is used as a ground layer to achieve perfect grounding for the single-ended LNA.

2.2.3.2 Measurement Results

The die photo of the designed LNA is given in Fig. 20. The ground reference technique is also used in this design. The measured noise figure performance of the LNA is shown in Fig. 21. It is clear that LNA has lower than 2.1 dB NF between 8 GHz and 12 GHz, while it reaches minimum noise figure value of 1.52 dB at the center of the band. As shown in Fig. 22, input and output of the LNA are matched to 50 Ω and lower than -10 dB in the overall band. The small-signal gain of the

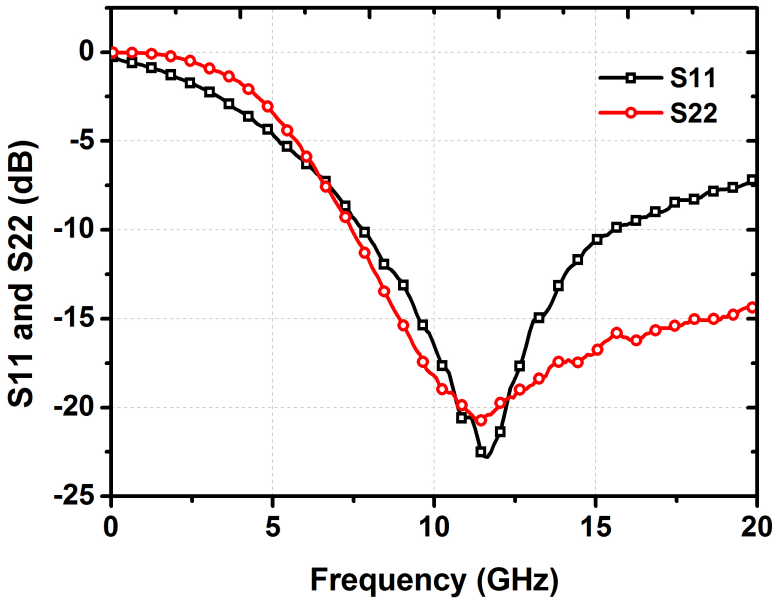


Figure 22: Measured S11 and S22 of the designed LNA.

amplifier is flat enough at X-Band and changes from 21 dB to 22 dB.

2.3 Future Work - Phase Shifter and Integration of Blocks

After presenting most of the blocks X-Band T/R module, we left with the last block; Phase Shifter (PS). During the process of writing this thesis, we were still continuing to search for optimum topology for this block. There are two main groups; passive and active. Because passive phase shifters have high insertion loss and consume large chip areas due to the usage of passive circuit components like capacitor and inductor, active phase shifter topologies are selected [45]. From two main topologies in the active phase shifter group, high-pass/ low-pass (HP/LP) with variable gain amplifiers (VGA) topology is chosen rather than vector modulators with VGAs to implement this block because of the simplicity.

After design and measurements of all blocks are completed, these blocks will be integrated in a single chip as a full T/R module shown in Fig. 8. This process is assumed to be more complicated and difficult because designer has to deal with problems like connections, noise and heat. Therefore plenty of time has to be dedicated to solve these problems.

Table 4: Comparison of the Switch with Reported Works

Frequency (GHz)	Figures of Merit			Chip Area mm^2	Technique	Technology	Ref.
	IL (dB)	Isolation (dB)	P_{1dB} dBm				
8−12	**3.2−4.1**	**23.2−42.5**	**28.2**	**0.44**	**Series-shunt, Body floating, Impedance Transformation Network, Parallel Resonance, S/D biasing**	**0.25μm SiGe BiCMOS**	**This Work**
3−10	3.1±1.3	25−32	18−20	0.62	Distributed Topology	0.18μm CMOS	Pao 2006
3−10.6	2.2−4.2	33−37	−	0.9	Synthetic Transmission Line	0.25μm CMOS	Jin 2005
10	1.81	21.9	10.1	0.67	Shunt	0.13μm SiGe BiCMOS	Kua 2007
	2.25	23.1	11.1	0.58	Series/Shunt		

3 Power Amplifier Fundamentals

3.1 Power Amplifier

The theory and operation principles of phased array radar modules are introduced in the previous chapter. As the main focus of this thesis, first of all, power amplifier fundementals will be presented and discussed in brief in this chapter.

The real world is "analog" in nature. Power amplifiers, also known as PAs, are used to amplify signals without degrading signal integrity, so that information can be received and recovered by the recipient. Power amplifiers typically trade off linearity and efficiency, and PAs can be categorized in to several classes from Class A to Class S according to this trade-off. Since most of these subjects in this chapter have been covered and analyzed comprehensively in many textbooks, what is presented in this chapter will be just a very brief overview. Readers interested in these subjects are encouraged to have a dip into other literature, such as [46, 47], to probe further.

A typical power amplifier design consists of several blocks; input matching network (IMN) and output matching network (OMN) to match 50 Ω for the system requirements imn most cases, biasing network (BN). There are other networks (ON) such as feedback network for bandwidth and stability requirements. The block diagram of a power amplifier is shown in Fig. 23.

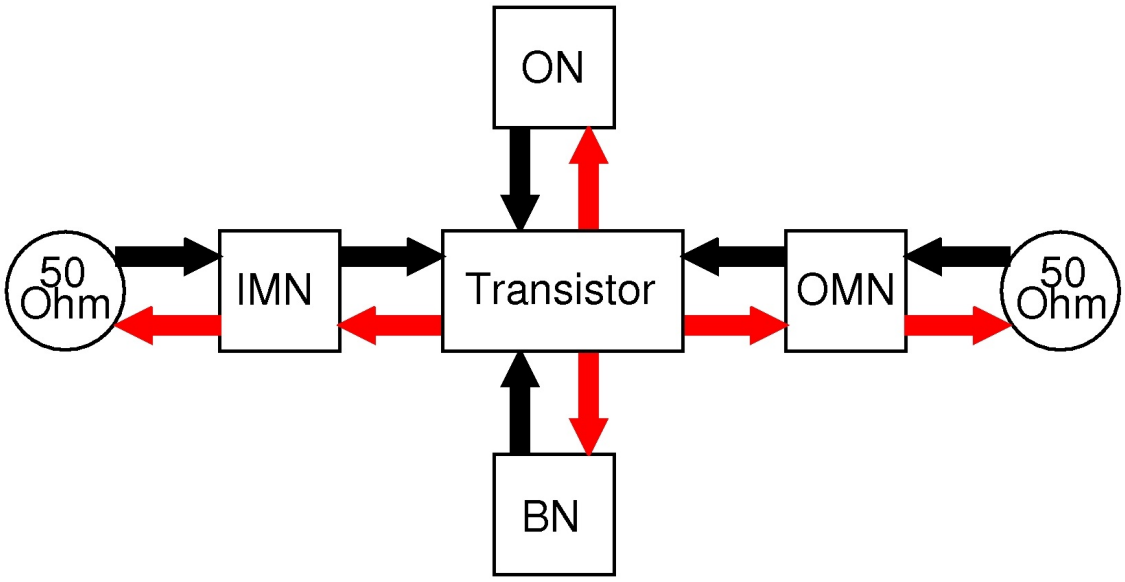


Figure 23: Block diagram of an amplifier.

3.2 Power Amplifier Classes

According to requirements, different types of classes have evolved over the years. Generally speaking, power amplifiers are divided into two types; transconductance and switching-mode amplifiers. Transconductance amplifiers include Class-A, Class-AB, Class-B and Class-C and switching-mode amplifiers include Class-D, Class-E and Class-F amplifiers. Amplifiers in each of these types focus on different subset of design criteria. Therefore each class has advantage of a certain criteria over others and vice versa. The classic trade-off between the transconductance and switching-mode amplifiers are linearity and efficiency. While Class-A amplifiers has the highest linear response, they can achieve at most 50 % efficiency. On the other hand, switching-mode amplifiers can have an ideal efficiency of 100 %, but they are strongly nonlinear amplifiers. Others classes like Class-AB, Class-B and Class C are compromises in between as shown in Fig. 24.

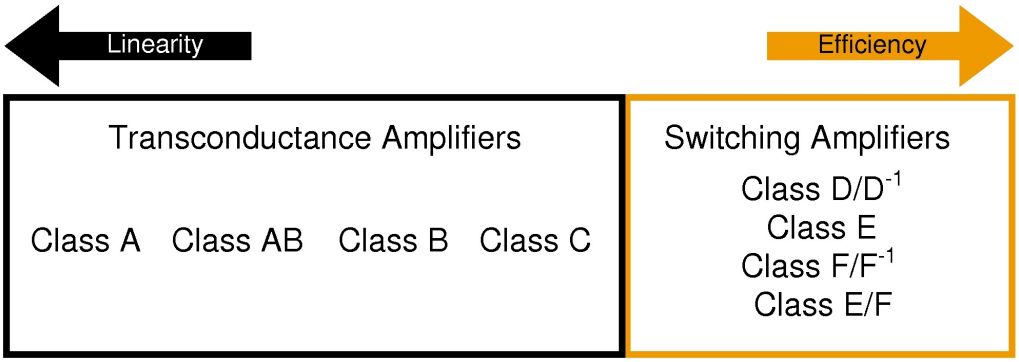


Figure 24: The linearity-efficiency trade-off between different classes of amplifiers.

First, transconductance amplifiers will be discussed and to do so, a single amplifier model shown in Fig. 25 may be enough to understand working principle of four classes, Class-A, AB, B and C. In this general model, the resistor R_L represents the load into which out power will be delivered. A "big, fat" inductor, *BFL*, feeds DC power to the transistor and is large enough so that the current through it is substantially constant. The drain of the transistor is connected to the load and tank circuit through capacitor *BFC* to prevent DC current flow to the load. Moreover, filtering is provided with the tank circuit, L and C, to cut down out-of-band signals due to the nonlinearities of the transistor. This is important because we are not dealing with only small-signal operation and distortion is expected by the amplifier.

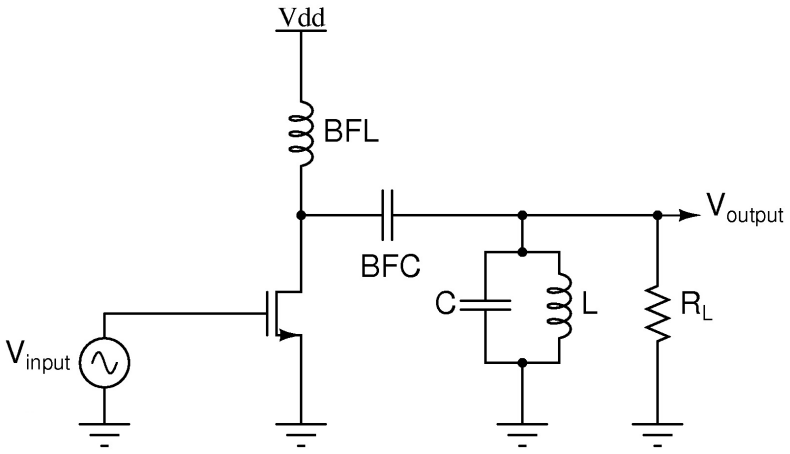


Figure 25: General power amplifier model.

To simplify the analysis, the quality factor of the tank is considered high enough that voltage across the tank can be approximated by a sinusoid. Although wideband power amplifiers are also of interest, the discussion will be limited to a narrowband operation case.

The typical classes of power amplifier according to the gate biasing are shown in Fig. 26. The most common amplifier classes are briefly discussed as follows.

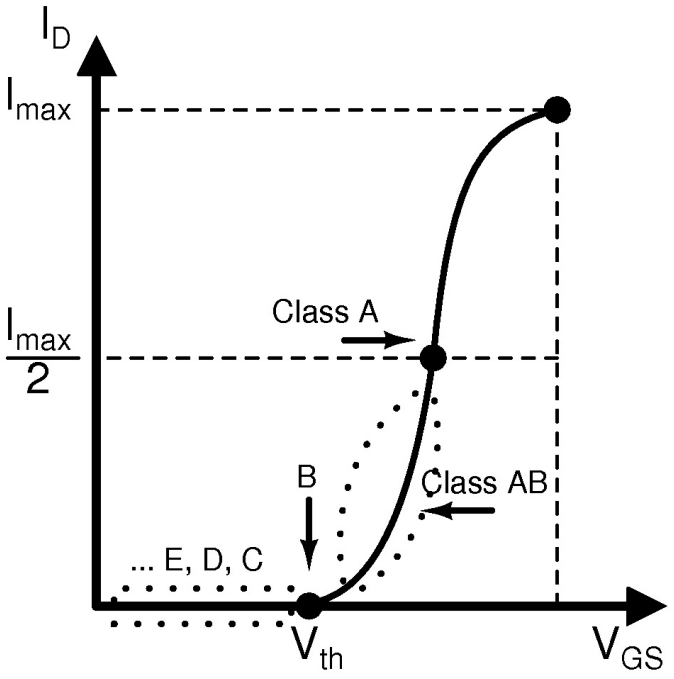


Figure 26: Amplifier classes according to the gate biasing.

3.2.1 Class-A

Class-A amplifier is a standard, textbook small-signal amplifier. These amplifiers have a conduction angle of $\theta_C = 2\pi$ whereas Class-AB amplifiers have a conduction angle of $\pi < \theta_C < 2\pi$, Class-B amplifiers have a conduction angle of π, and Class-C amplifiers have a conduction angle of $0 < \theta_C < \pi$. Because Class-A amplifiers conduct during a full period, the drain voltage and current are therefore offset sinusoids with a 180°. Fig. 27 shows the voltage and current waveforms of a Class-A amplifier.

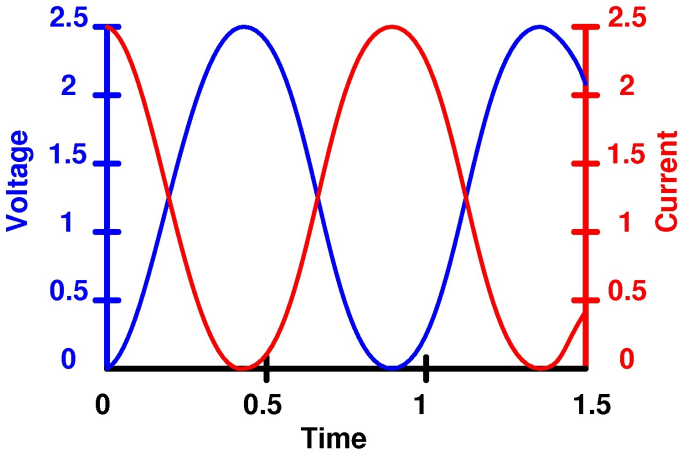


Figure 27: Voltage and current waveforms of Class-A amplifier.

As shown in Fig. 27, Class-A amplifiers are the most linear amplifiers at all. However their ideal maximum efficiency is 50 % and this is the biggest drawback of this class. Furthermore, efficiencies of 30-35 % are not at all unusual for practical applications for this class amplifiers. To understand the efficiency in brief, let us take 33 % drain efficiency as an example. If the output power of a Class-A amplifier is 100 W, and the total power consumption is 300 W, this means that 200 W power is dissipated by this amplifier. It is important that these numbers are unusual for the heating-handling capability of a common-source transistor package.

3.2.2 Class-B

One can improve the efficiency of an amplifier by reducing the power dissipation. A clue to how one can achieve this is actually implicit in the waveforms in Fig. 27. If voltage or current is set to zero for a fraction of a full period, amplifier will not dissipate any power. It should be clear that this can be achieved by changing the

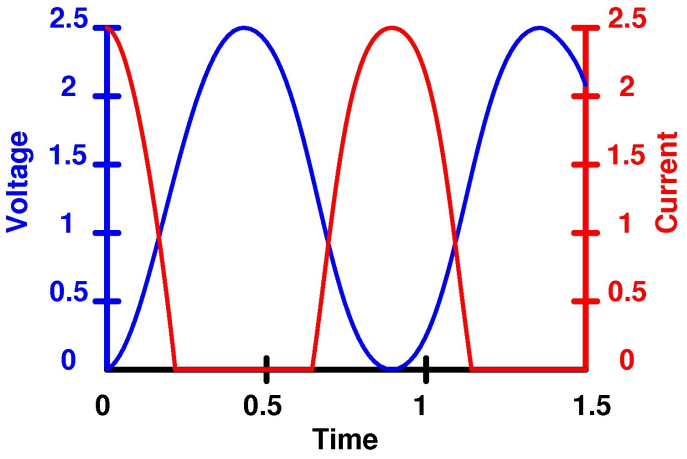


Figure 28: Voltage and current waveforms of Class-B amplifier.

bias of the amplifier as shown in Fig. 26.

The bias of Class-B amplifier is arranged to shut off the amplifier half of every cycle as shown in as shown in Fig. 28. Obviously, this will lead to nonlinearity in the output signal and a high Q resonator is absolutely will be mandatory in order to obtain an acceptable sinusoid output voltage. The ideal maximum efficiency of Class-B amplifiers is 78.5 %, which is significantly higher than Class-A amplifiers. If we take the previous example into account, to achieve a practical efficiency of 65 % while having the same output power of 100 W, Class-B amplifier only dissipates about 53.8 W of power. This is a great reduction from 200 W with a significant linearity cost.

3.2.3 Class-AB

It is shown that Class-A amplifiers conduct 100 % of every cycle and Class-B amplifiers 50 % of a time. As its name suggests, Class-AB is a transition between these two classes which mean the conduction angle is between 50 and 78.5 %. The voltage and current waveforms of this class amplifier for a full period is given in Fig. 29. The biasing scheme of this class amplifies is also shown in Fig. 26. This shows that Class-AB amplifiers offer a flexible solution for a trade-off between linear and efficiency of the previous cases. This compromise is frequently satisfactory for many PA designers as one can infer from the popularity of Class-AB amplifiers.

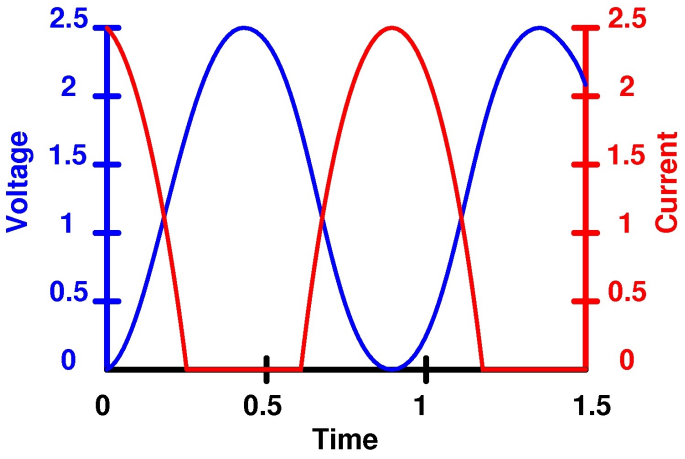


Figure 29: Voltage and current waveforms of Class-AB amplifier.

3.2.4 Class-C

In a Class-C amplifier, the gate voltage is biased such that amplifier conducts only a small fraction of a full period as shown in Fig. 30. Because Class-C amplifiers dissipate less power than previous classes, efficiency of this class amplifier can reach an efficiency of 90 %. However, there are some problems of this class amplifier especially for high frequency applications. One of the drawbacks of Class-C amplifiers is the power gain which comes at the expense of high efficiency. As the efficiency approaches to 100 %, the output power and so the power gain goes to zero. This is not an acceptable approach for high frequency applications where power gain is very critical. The second drawback is the high nonlinearity of Class-C amplifiers. It requires very high Q resonators at the output stage which is also not very practical for high frequency on-chip applications. However, Class-C amplifiers can be used in

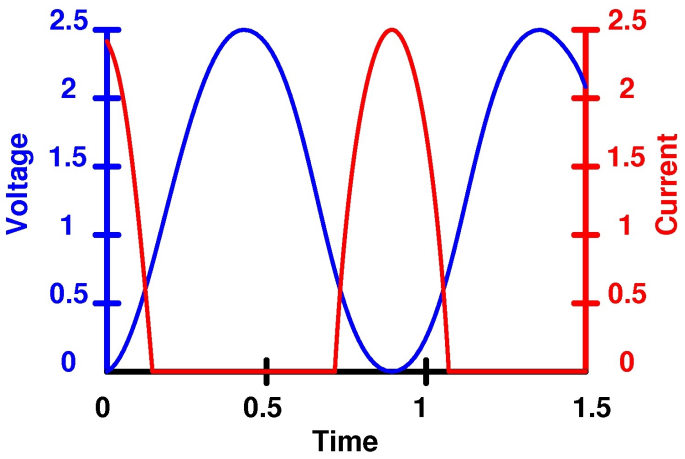


Figure 30: Voltage and current waveforms of Class-C amplifier.

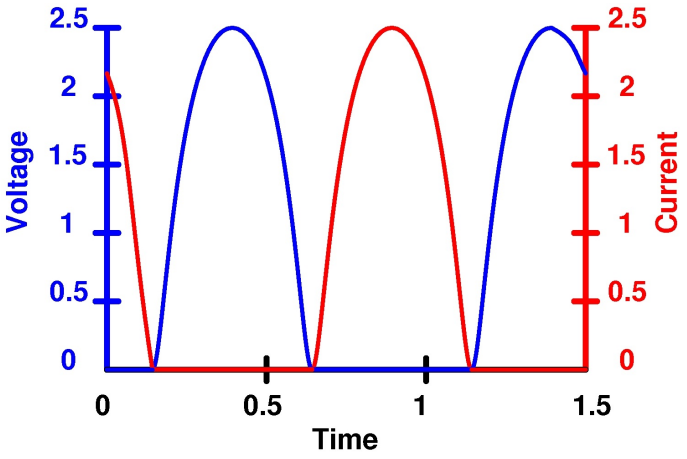


Figure 31: Voltage and current waveforms of a switching-mode amplifier.

such applications where a high degree of nonlinearity is tolerable.

3.2.5 Class-D

The classes presented so far uses active devices as transconductance amplifiers, therefore their efficiency was limited. Another approach is to use active devices as switches in several classes which are called switching-mode amplifiers. Switching-mode amplifiers utilize the active device either completely turned on or completely turned off as shown in Fig. 31. This means that there are two modes for this operation; amplifier is conducting (switched on) and there is no voltage across the transistor or amplifier is not conducting (switched off) and there is no current flowing through it. As a result, there is ideally no power consumption and all consumed power directly transferred to the output which results in 100 % of efficiency. Class-D amplifier is one example such operation. In a Class-D amplifier, voltage waveform is in a square shape whereas current is again sinusoid shape. Mostly Class-D amplifiers use two or more transistors as switches to generate square-shape drain current or voltage waveform.

3.2.6 Class-E

As we have seen before, switching-mode amplifiers like Class-D can provide very high efficiencies, but it is not always trivial to realize in practice due to imperfections in real switches. To achieve high efficiencies switching has to be quite fast relative to the speed of operation. This requirement may not be satisfies at high carrier

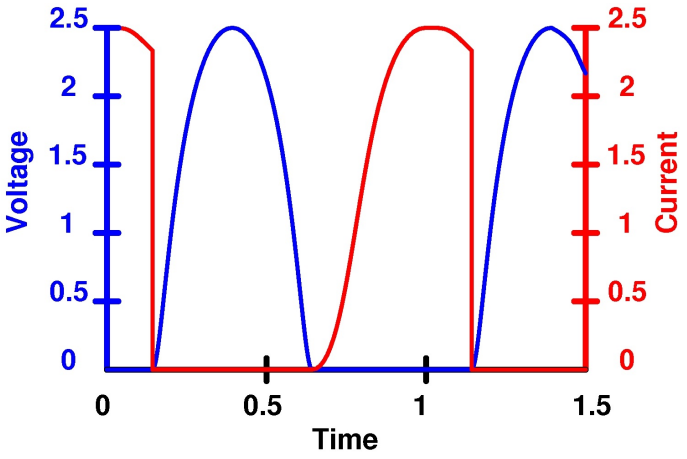


Figure 32: Voltage and current waveforms of Class-E amplifier.

frequencies and especially for on-chip applications.

If there is a way to realize zero switch voltage within a nonzero time interval of a full period, this will again decrease the power dissipation. The Class-E amplifier realizes this requirement with a high-order reactive network that provides enough freedom for zero voltage and zero current during a cycle. This method is called "soft-switching" where the voltage waveform is reduced before the switch turns on as shown in Fig. 32.

Another beauty of this class amplifiers is the relatively simple circuit topology to implement compared to Class-D amplifiers where zero output capacitance is assumed. However, high voltage peaks during a cycle can result in damages for the transistors.

3.2.7 Other High Efficiency PA Classes

There are other high-efficiency amplifiers such as F, F^{-1}, D^{-1}, G, H, S or hybrid class amplifiers which are combination of these presented. In the classes with an inverse sign implies simple the change in the waveform of voltage and current. Class-F amplifiers utilize a quarter-wave transmission line which results in a resistive load at the carrier frequency, short for all even harmonics means that the only current flow through the transmission line is the fundamental frequency and open for all odd harmonics means that a square wave with 50 % duty ratio will be seen at the drain of the transistor. All other classes somehow use a switching technique, a resonator or multiple power-supply voltage to reduce the current-voltage product.

3.3 Power Amplifier Design Considerations

Designers select the class type of an amplifier according to the requirements of the system. If a linear amplification is required for applications such as amplitude modulation (AM), single-sideband modulation (SSB), and quadrature amplitude modulation (QAM). On the other hand, high efficiency switching-mode amplifiers have satisfied the need for narrowband tuned amplifiers. These applications include amplification of frequency modulated (FM) signals.

In an ideal system, the output signal is directly related to the input signal. However, in real world this is a lot more complicated. This can be due to active devices, passive devices, supplies or environmental conditions. Unavoidably, even the gain of an amplifier is never perfect and can change with respect to input power level, frequency, temperature, and supply voltage. While many analog and RF amplifiers can be approximated with linear models to obtain their response to small signal, nonlinearities cal lead to interesting and important phenomena.

Nonlinearities can be divided into weak and strong (or small and large signal) nonlinearities. Small signal nonlinearities are due to the inherent I-V characteristics of devices, and give rise to intermediation whereas large signal nonlinearities occur when physical transistor limitations such as power supply and clipping at saturation are encountered. The following are the major properties and characteristics which have to be considered in designing power amplifiers.

3.3.1 Output Power

Output power is the amount of power (in Watts) of RF energy that is produced at the output of power amplifier. Transistors are the main active components that produce that much power. Generally, the output port of an amplifier is connected to an antenna or a T/R switch which directs the signal to the antenna.

3.3.2 Power Gain

The gain of a power amplifier is the ratio of the output power divided by its input power at the fundamental frequency.

$$G = \frac{P_{OUT}}{P_{IN}} \tag{20}$$

There are three different power gain definitions, operating power gain, transducer power gain and available power gain.

3.3.3 Efficiency

Efficiency, η, is the measure of how effectively power amplifier converts power from the supply into output power, in other words the DC power that is converted to RF power. There are three different efficiency definitions that are commonly used for power amplifiers.

3.3.3.1 Drain Efficiency (DE)

The Drain Efficiency (DE) is the ratio of the output power to the DC input power from supply

$$DE = \frac{P_{OUT}}{P_{DC}} \tag{21}$$

where P_{OUT} is the RF output power and is gigen by

$$P_{OUT} = \frac{i_1 v_1}{2} = \frac{{i_1}^2 R_L}{2} \tag{22}$$

where i_1 and v_1 are the peak fundamental components of the output current and voltage, respectively and R_L is the output load.

3.3.3.2 Power-Added Efficiency (PAE)

Power-added efficiency (PAE) includes also the effect of input power at the fundamental frequency. Different from the DE, PAE takes the gain of the amplifier into account.

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT} - P_{OUT}/G}{P_{DC}} = DE\left(1 - \frac{1}{G}\right) \tag{23}$$

It can be seen from (23) that for high gain amplifiers PAE is the same as DE.

3.3.3.3 Overall Efficiency (OAE)

The last efficiency definition is the overall efficiency (OAE) which is usable for all kinds of performance evaluations.

$$\eta_{overall} = \frac{P_{OUT}}{(P_{DC} + P_{IN})} \tag{24}$$

3.3.4 Linearity

In real world, power amplifiers (not ideal) are only linear within some practical limits. As one of these limits, when the input signal power is increased beyond a limit, the gain of the power amplifier will not be constant at all and will start to decrease until a point. This means the output power will not increase anymore and will saturate, this is called clipping and results in non-linearity for large signals. For example, Class-A is the most linear amplifier in all classes but the one has the lowest efficiency. The linearity decreases when we go to Class-AB,-B,-C and switching amplifiers.

These non-linearities of a power amplifier can be modeled by a power series representation which relates input signal to the output signal with

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^4(t) \tag{25}$$

If a sinusoidal input signal is applied to a non-linear system like modeled above, the output will exhibit the frequency components that are multiple of fundamental frequency. Moreover, because of this non-linearity, the amplitude of each component will not be a linear function of input component. If we assume an input signal $x(t) = A\cos\omega t$, then

$$\begin{aligned} y(t) &= \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \\ &= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \end{aligned} \tag{26}$$

in (26), the term with input signal $x(t)$ is the fundamental component and other high frequency terms are harmonics components. From now on, some of the widely used linearity parameters will be discussed.

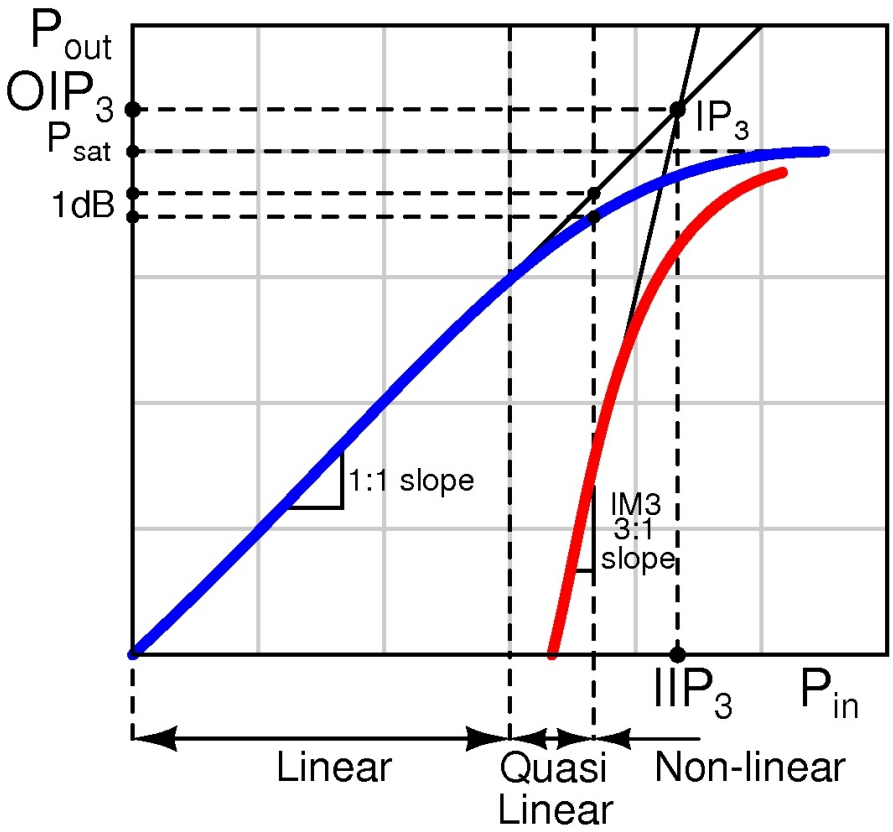


Figure 33: Output power vs input power for a power amplifier.

3.3.4.1 1 dB Gain Compression (P_{1DB})

The small-signal gain of an amplifier is assumed when it is assumed that high-order components are negligible small compared to fundamental term. In (26), small-signal gain can be equalized to α_1 if harmonics are neglected. However, if the signal level increases beyond a level, the gain begins to vary. This means output level increases by a smaller amount for a fixed increase in the input signal level. This is evident from the term $3\alpha_3 A^3/4$ added to $\alpha_1 A$ in (26). At low input signal levels, the output power is proportional to the input power. However, as the input level approaches saturation point, the term $3\alpha_3 A^3/4$ will be dominant because of the cubic dependence of α_3 (which is a negative number for most of the transistors), $\alpha_3 A^3$. The output level at which gain compresses by 1 dB is called "1 dB compression point" or P_{1dB}. This phenomenon is shown in Fig. 33 where both P_{IN} and P_{OUT} are plotted in logarithmic scale.

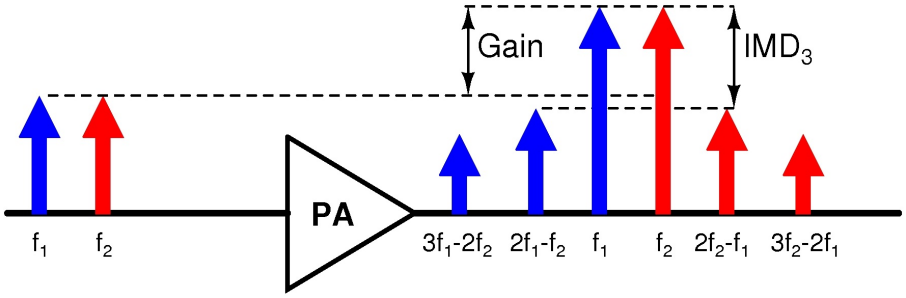


Figure 34: Corruption of a signal due to intermodulation between two signals, two-tone test.

3.3.4.2 Intermodulation Distortion

Another important amplitude distortion introduced by the amplifier is the intermodulation distortion (IMD). IMD is generated by undesired mixing products, which distort the fundamental tones and give rise to intermodulation products. A two-tone test can be used to understand the IMD level of a power amplifier. To understand how (25) gives rise to intermodulation, assume $x(t) = A_1 cos\omega_1 t + A_2 cos\omega_2 t$. When this input signal is inserted in (26) and expanded, we obtain the following intermodulation products:

$$\begin{aligned} \omega &= \omega_1, \omega_2 : \left(\alpha_1 A_{1,2} + \frac{3}{4}\alpha_3 {A_{1,2}}^3 + \frac{3}{2}\alpha_3 A_{1,2} {A_{2,1}}^2\right) \cos \omega_{1,2} t \\ &= 2\omega_{1,2} \pm \omega_{2,1} : \frac{3\alpha_3 {A_{1,2}}^2 A_{2,1}}{4} \cos\left(2\omega_{1,2} + \omega_{2,1}\right) t \\ &\quad + \frac{3\alpha_3 {A_{1,2}}^2 A_{2,1}}{4} \cos\left(2\omega_{1,2} - \omega_{2,1}\right) t \end{aligned} \tag{27}$$

In Fig. 34, the third-order intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are illustrated. It is important to note that if ω_1 and ω_2 are close to each other, as have been in two-tone test, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ products will appear in the vicinity of fundamentals tones ω_1 and ω_2.

3.3.4.3 Input and Output Intercept Point (IIP_3 & OIP_3)

Because third-order products are very important for RF systems, to characterize this behavior, a performance metrics called "third-order intercept point" (IP_3) has been defined. In this analysis, two-tone test is applied in which A is chosen to

be sufficiently small such that high-order terms will not dominate the gain of the fundamental products (ω_1 and ω_2) given in (27). From (27), it is clear that the increase of fundamental tones is proportional to A, whereas the increase in third-order products is proportional to A^3. This behavior is plotted in Fig. 33 on a logarithmic scale where third-order intermodulation (IM3) products increase in a rate three times of fundamental products. The third-order incept point is defined as the intersection of these two lines. The input power level at which *IP3* is occurred is called input *IP3* (IIP_3) and the output power level is called output *IP3* (OIP_3) points.

3.3.4.4 Phase Distortion

The origin of amplitude distortion is simple and intuitive: the device structure, signal power level, current and voltage waveforms, etc. On the other hand, the phase distortion is also simple but not that much intuitive. The phase distortion is simply originated by the voltage-dependent parasitic capacitances of the active components in an amplifier. With different power levels of the input signal, the parasitic capacitance of a transistor changes which leads to change in phase of an amplifier. Therefore, Class-A amplifiers have the best phase performance due to the same bias voltage. However, high-efficiency amplifiers results in high deviations of phase with respect to input power level due to biasing schemes.

3.3.5 Stability

Stable performance in the frequency of operation is one of the most critical requirements for an amplifier. This is a particular concern when dealing with RF circuits because these systems tend to oscillate depending on frequency and termination. Therefore stability analysis consume important portion of an amplifier design. Therefore there are some methods to define an unconditional stability for amplifiers such as μ-factor and k also known as Rollett factor [48].

In our analysis, we will apply k-factor method in our simulations to verify the unconditional stability of the amplifier. Here unconditional criteria are given in

$$
\begin{aligned}
k &= \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2\,|S_{12}|\,|S_{21}|} > 1 \\
|\Delta| &= |S_{11}S_{22}-S_{12}S_{21}| < 1
\end{aligned} \tag{28}
$$

Equations in (28) are both together stability conditions which are only valid at one frequency and bias conditions.

While k-factor method is helpful to analyze the stability analysis of linear amplifiers, this method has many limitations. First, it is a bias dependent method and any change in the bias can result instability due to the change of parasitic capacitances of the active device. Second, this method does not count the effect of input power level and frequency. Therefore designer has to check the k-factor for different frequency and input powers. Lastly, k-factor analysis does not provide any information about the amplitude and phase of oscillation. As a result, k-factor method has several disadvantages but an easy analysis to perform today's computers.

3.3.6 Biasing

One of the crucial steps designing PA is to provide reliable DC bias to transistor in the circuit. As discussed the section above and given in Fig. 26, DC bias of an amplifier directly determines the class of an amplifier. Consequently, any change in the bias point can lead to an undesirable region of operation from the point of linearity and efficiency. Therefore designer has to pay much attention to the bias circuit such that it guarantees a stable class operation. Moreover, bias circuit need to be designed to prevent any low frequency oscillation. Based on the technology and transistor type, bias circuits can also perform some additional tasks like stable voltage/current generation, temperature compensation or dynamic biasing [49].

3.3.6.1 Constant Current/Voltage

Constant current biasing (CCB) and constant voltage biasing (CVB) are two most used techniques in power amplifier biasing networks. As indicated by their names, CCB and CVB improves the performance of the amplifier by providing constant current and voltage with respect to input power. A typical CCB circuit is

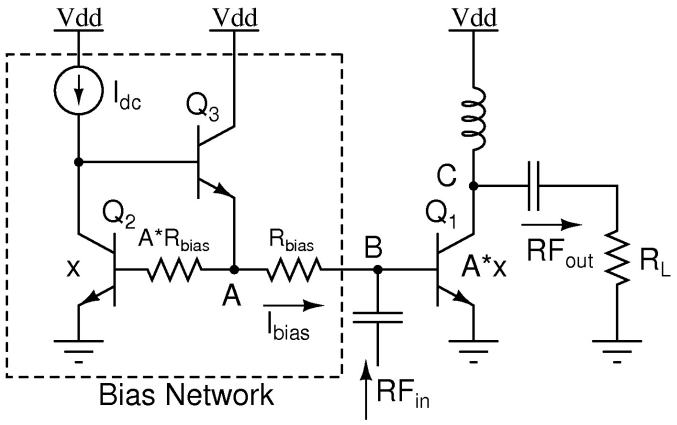


Figure 35: A simple constant current biasing network.

given in Fig. 35. At node A, a constant voltage is obtained as long as the current source I_{DC} is constant. With a proper resistor R_{bias}, amplifier transistor, Q_1 can be biased easily.

When the input RF power increase, the collector DC current does not change due to the constant bias circuit. This results in a drop of quiescent base-emitter voltage to drop as shown in Fig. 36. As a result, clipping is observed at the output node of the amplifier which generates unwanted harmonics. As a result, the linearity of the amplifier is degraded.

On the other hand, a simple CVB circuit consists of a single large inductor L_{large} is given in Fig. 37. A constant DC voltage is provided at the base of the amplifier through a large inductor. When the RF power increases, the base DC current of the amplifier increases and so does the collector DC current. As shown in Fig. 38,

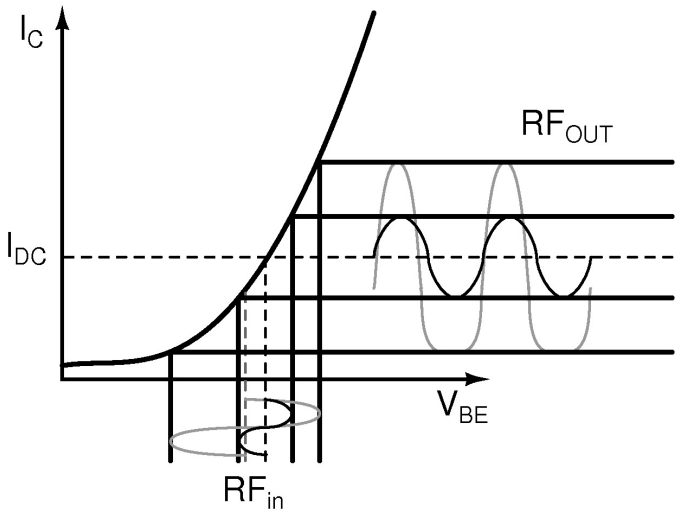


Figure 36: Large signal analysis of CCB network.

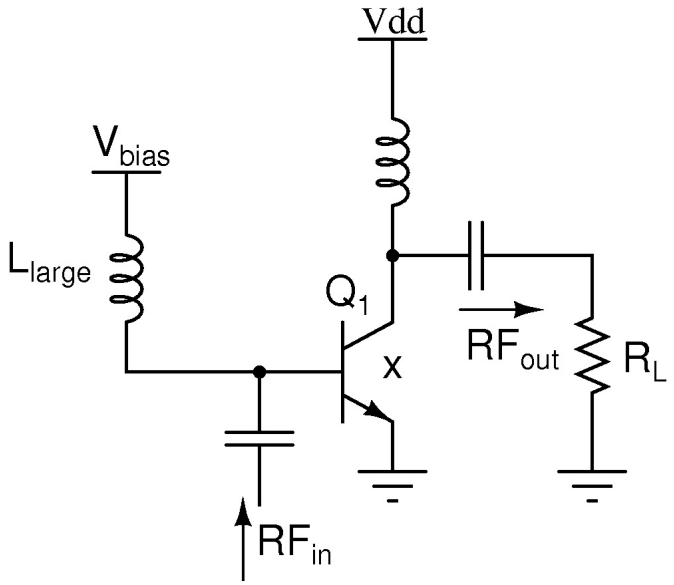


Figure 37: A simple constant voltage biasing network.

this method will improve the linearity because output current will clip less than CCB method. However, large inductors consume much area and increase the cost. Therefore, this method is often replaced with a biasing network including op-amps.

3.3.6.2 Other Biasing Methods

In addition to CCB and CVB methods, there are several biasing methods for power amplifiers such as temperature-compensation, linearization, and dynamic biasing. As mentioned above, undesirable shifts in bias of amplifiers can occur due to change in the input power level. In addition, increase in the junction temperature

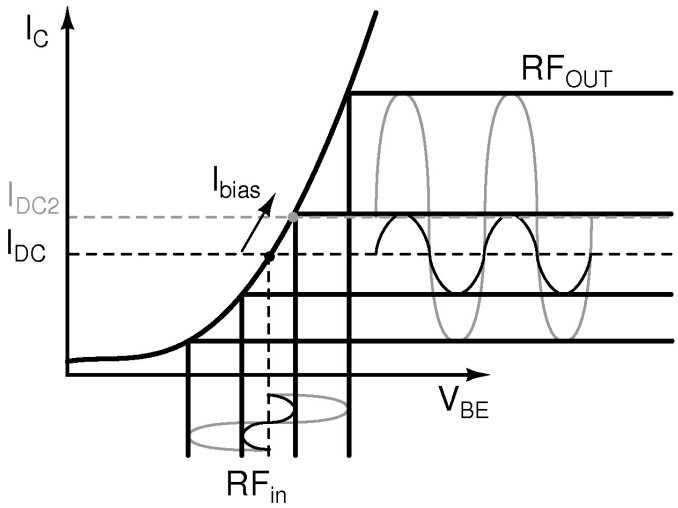


Figure 38: Large signal analysis of CVB network.

causes base-emitter voltage, V_{BE} to drop. The drop in V_{BE} significantly affects the operating region and class of a power amplifier. To prevent this bias networks consist of ballasting resistors and diode-connected transistors are used which compensates the drop [50]. Moreover, there are some special bias networks such that improve the linearity of a power amplifier during a large signal RF input [49]. In addition more complicated dynamic biasing networks exist in which switches and detectors are used to provide higher efficiency at the low power region [49]. Because the efficiency is directly proportional to the DC power consumption, this method changes the DC bias point of an amplifier at the low power inputs and thus increases the average power efficiency.

4 A Two-Stage X-Band Power Amplifier

The phased array X-Band T/R module is introduced and discussed with the system requirements in Chapter 1. In addition, power amplifier fundamentals and performance parameters are briefly discussed in Chapter 3. In this chapter, design steps of X-Band power amplifiers will be presented with simulation and measurement results.

4.1 Power Amplifier Requirements

As discussed in Chapter 1, one of the main aims for the usage of phased array systems is the increased radiated power in required direction, explained with equivalent isotropically radiated power (EIRP) which is PxN^2 where P is the power radiated by each PA and N is the number of elements in an array. The number of elements required for a radar system according to the radiated power of each element is already presented in Table 1. According to the perspective of an IC designer there is a practical limit for maximum achievable radiated power for fully-integrated power amplifiers, although this fact is not taken into account in Table 1. Although details will be discussed later in this chapter, now, let's assume that maximum output power is 23 dBm for a single PA operating at X-Band. In that case, with combination of four PAs, the phased array chip will have an EIRP of 38 dBm (23 dBm for output power of PA, 3 dB of a predicted antenna gain, and 12 dB for array gain), as shown in Fig. 39.

As a result, the output power of the PA that is chosen to be higher than 20 dBm is limited by the used technology. Furthermore, the gain of the amplifier is

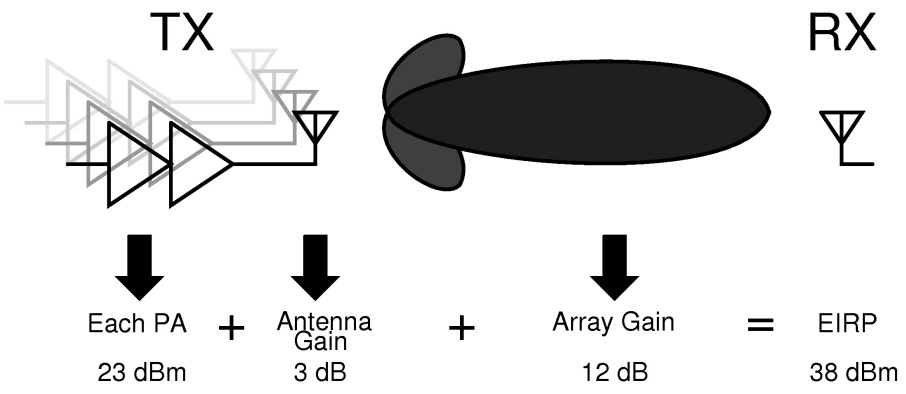


Figure 39: A 4-element phased array transmitter.

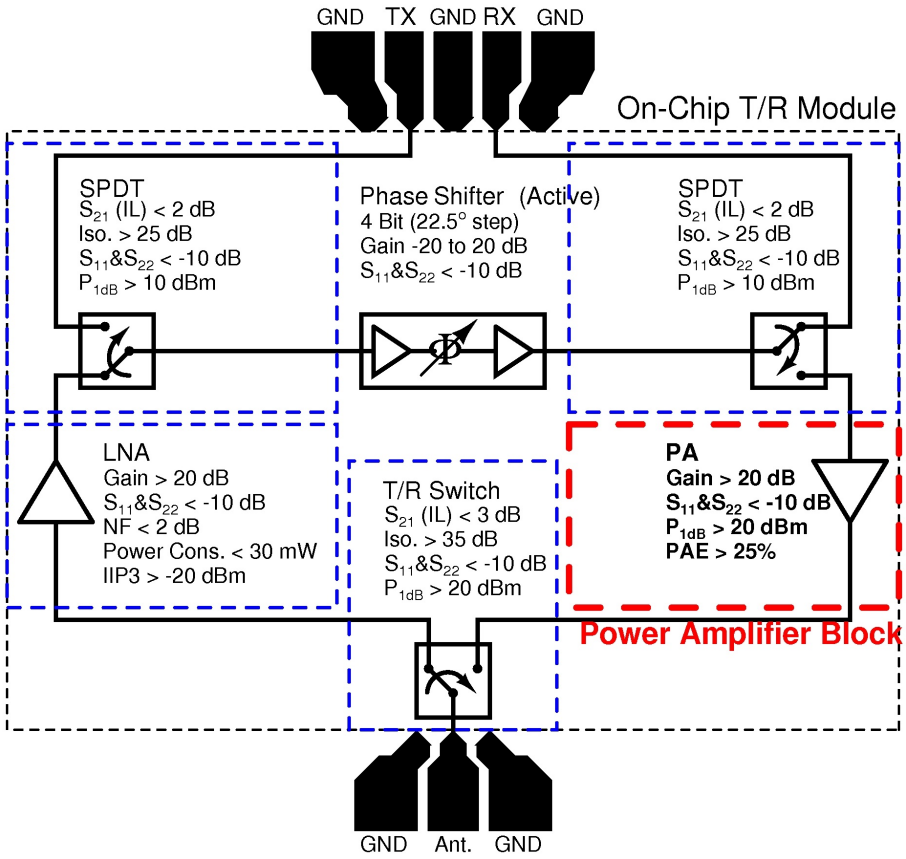


Figure 40: The connections and requirements of PA in the X-Band phased array T/R module.

required to be high enough to compensate losses introduces by passive components like SPDT, T/R switches and phase shifter. Therefore moderate gain of 20 dB that is achievable with two stage amplifier is selected as the block requirement. As was the case for all blocks, input and output of the PA have to be matched to 50 Ω. Because most of distance measuring radar systems is based on frequency modulation, pulse modulation or no-modulation in continuous wave systems, such as Doppler radar, the class of PA is chosen to be as linear as possible which means Class-A or Class-AB. The efficiency requirement of the PA is automatically determined by the selection of the class type, thus 25 %, which is typical Class-A amplifiers, will be the requirement for this design. The connections of the PA with the requirements discussed are given in Fig. 40.

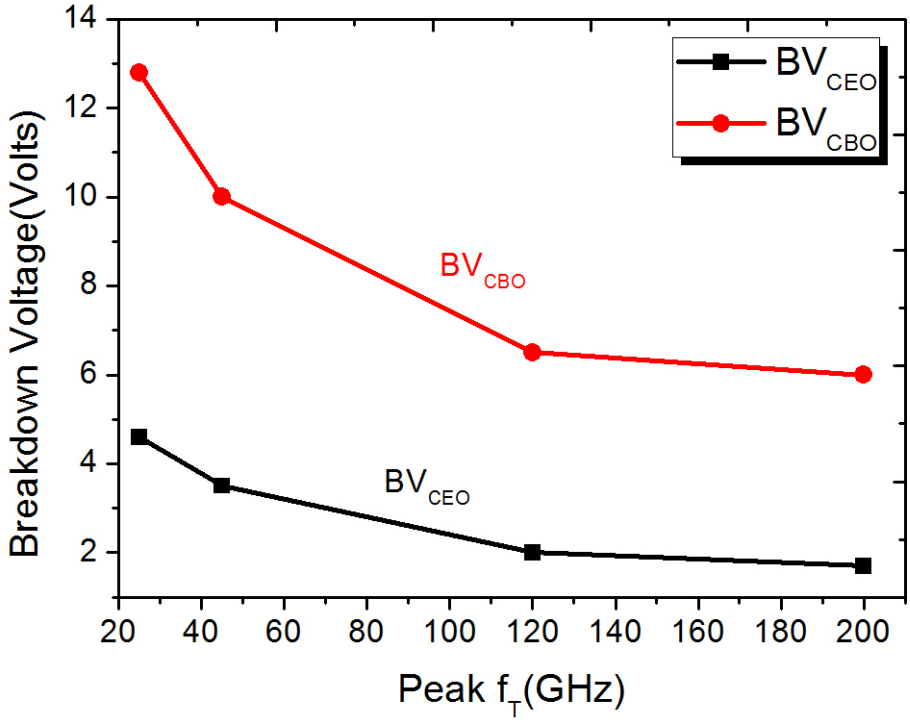


Figure 41: BV_{CEO} and BV_{CBO} vs. peak f_T in second and third generation SiGe technologies.

4.2 Breakdown Voltages

After discussing the requirements and selected class for the PA block, next step is the section of the topology. As it has been for all blocks, the topology of the PA has to be selected considering the used technology and advantages/disadvantages of it. To begin with, first problem comes up with the breakdown voltage of the transistors. It is known that the high-speed characteristics (e.g. f_T, f_{MAX}) of high-performance SiGe HBTs are generally obtained with the sacrifice of breakdown voltages [51]. Therefore, common knowledge topologies for PAs are not suitable for high-performance technologies having less than 2.5 V breakdown voltages; Collector-Emitter Breakdown Voltage (BV_{CEO}) and Collector-Base Breakdown Voltage (BV_{CBO}). Therefore, new topologies specific to technology and process are required to meet the requirements.

It was shown that driving SiGe HBT with a forced I_E, as opposed to I_B, can increase the breakdown characteristics of the device from the BV_{CEO} value up to that of BV_{CBO} voltage which is nearly twice that of the BV_{CEO} voltage, as shown in Fig. 41 [52]. This means that operating an amplifier in the Common-Base (CB) configuration as opposed to the more widely used Common-Emitter (CE) configuration can

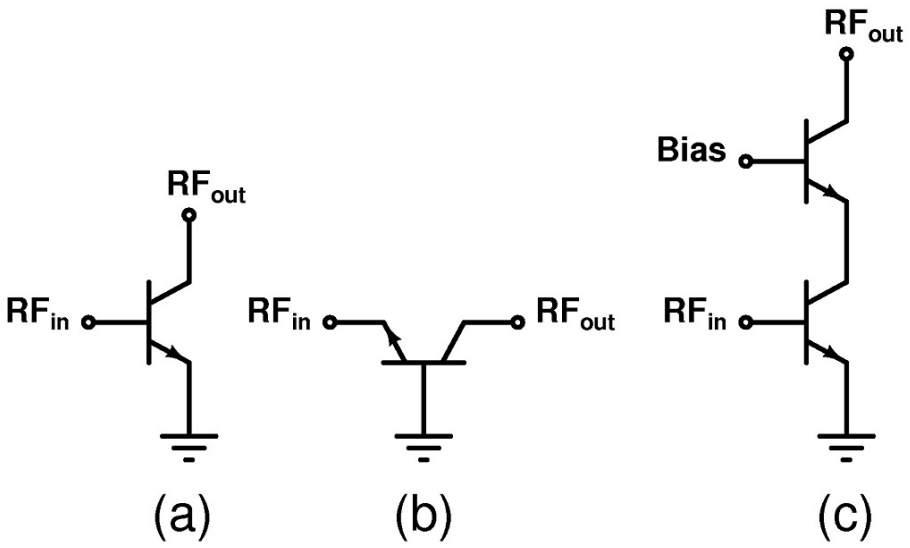


Figure 42: Configurations for (a) Common-Emitter, (b) Common-Base, and (c) Cascode amplifiers.

result in higher breakdown voltages, as shown in Fig. 42. Furthermore, combination of these two configuration results in a CE/CB hybrid which is commonly known as cascode configuration.

In the cascode configuration, the CE transistor not only acts as the gain provider, but also forces an I_E for the CB device, providing the aforementioned increased breakdown voltage. In addition, usage of moderate-speed but high-breakdown voltage device as the CB device also improves the total breakdown voltage of the cascode configuration. While the knee voltage of the cascode configuration is increased due to the addition in series of the voltage drop across the Collector-Emitter junction of the CE device and CB device, the impact of this on PAE is studied in [53]. Because the breakdown voltage is greatly increased compared to the CE configuration, it is possible to see increased PAE from the cascode configuration.

As a result, using a higher breakdown voltage device in the CB portion of the cascode configuration allows for increased operating voltage. On the other hand, using a lower breakdown and higher gain device for the CE portion results in greater gain. Because of all these analysis, a cascode configuration will be utilized in the further designs.

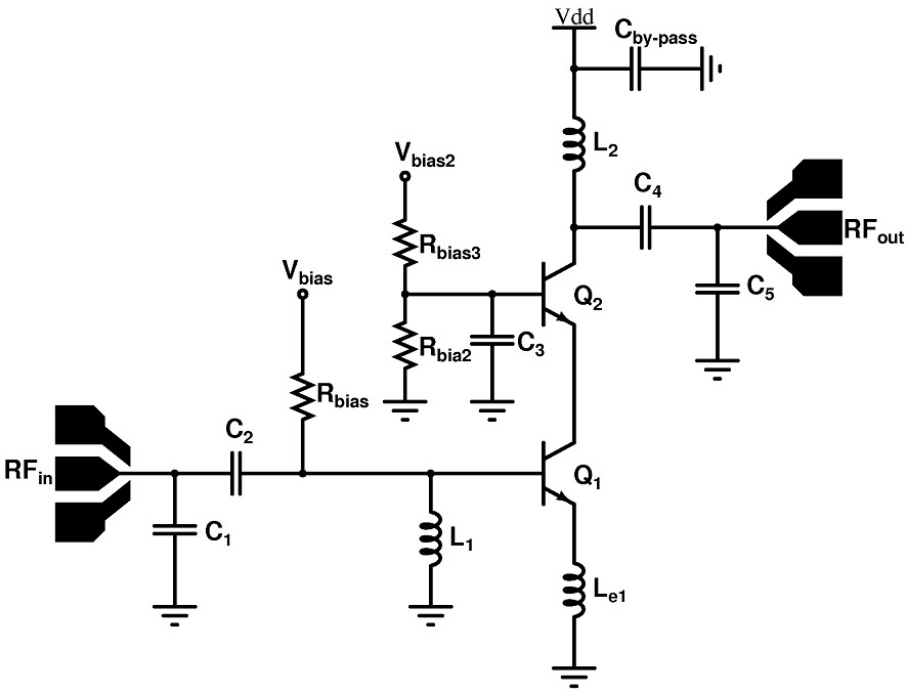


Figure 43: Schematic of the one-stage cascode power amplifier.

4.3 Single Stage Power Amplifier Design

Before the proposed system architecture and requirements of each block are decided, a one-stage X-Band amplifier is designed in IHP 0.25μm SiGe BiCMOS process technology. A schematic of the power amplifier is shown in Fig. 43. As discussed in the previous section, high-speed transistors are used as the CE stage and high-breakdown transistors are used as the CB stage. The device size and numbers are sized such that, at optimal bias, each device operates near its peak f_T current. Maximum emitter geometry available by this particular SiGe technology is used to decrease the parallel connection of transistors.

To match to the relatively small input impedance to 50 Ω, on-chip passive components are used. All inductors are custom designed using either ADS Momentum or SONNET. As a result, semi-port layout simulations are performed with both foundry provided models for transistors, capacitors, resistors and EM modeling of inductors.

Large banks of capacitance utilizing on-chip MIM (metal-insulator-metal) capacitors were used at the base and supply connection of the circuit. Trace lengths between transistors and capacitors are kept as short as possible to minimize series parasitic resistance and inductance.

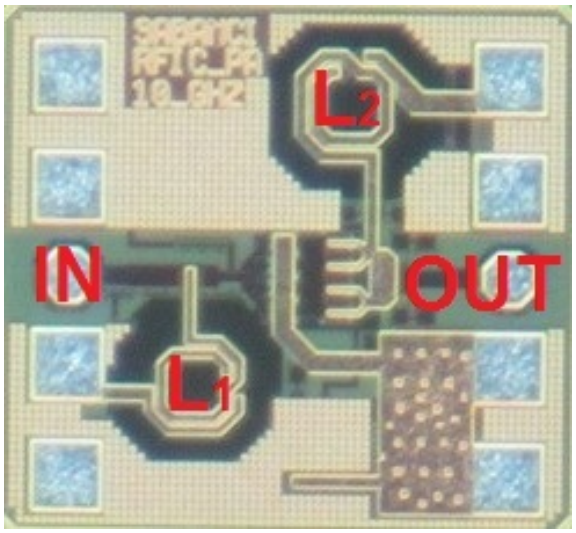


Figure 44: Die photo of the power amplifier.

4.3.1 Measurement Results

Shown in Fig. 44, the chip occupies an area of 0.6 mm x 0.65 mm, including pads. The chip is attached to the FR4 substrate using conductive epoxy to function both as ground, mechanical support and a heat sink.

Large-signal measurements are performed using the measurement setup shown in Fig. 45. The output of the power amplifier is first connected to a low-pass filter to attenuate all harmonic signal power and a power limiter is connected to prevent damage to the power sensor and power meter. At the end, the signal power is measured with a power meter. The power losses in the measurement setup are calibrated out with a thru measurement calibration, consisting of two cables and two probes connected in series.

As shown in Fig. 46, at 10 GHz the amplifier has a small-signal gain of 8 dB. However, there is a frequency shift for the input matching which is centered at 11

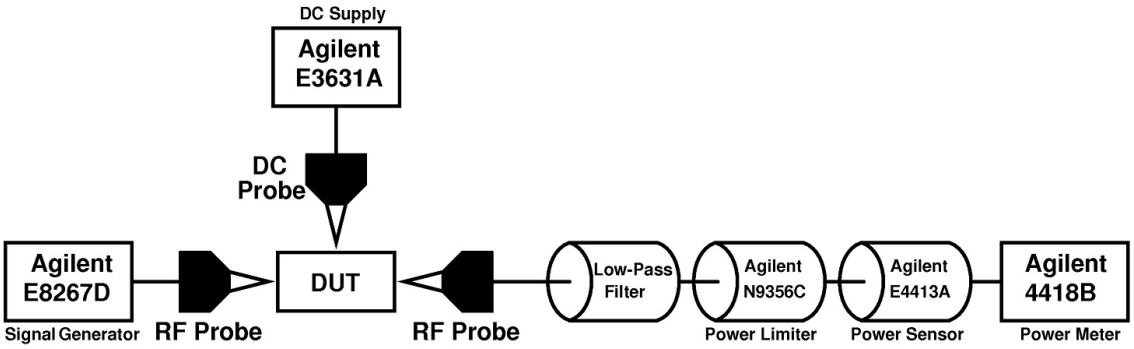


Figure 45: Large-signal measurement setup.

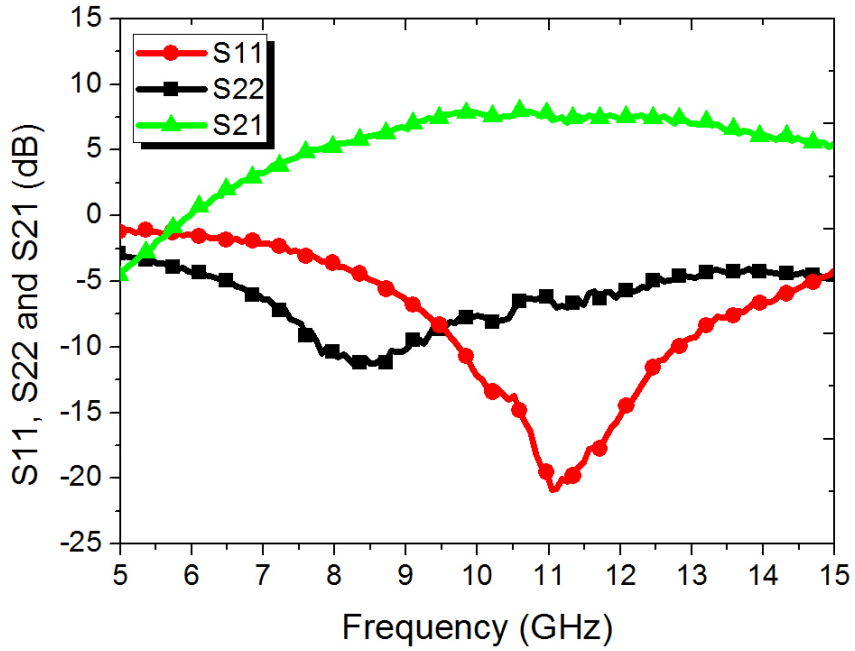


Figure 46: S-parameter measurement results.

GHz with a bandwidth of 2 GHz. In addition, the output matching is also shifted but to the lower frequencies.

The 1 dB output power compression point and gain measurements at 10 GHz are given in Fig. 47. It is measured that the power amplifier can produce 14.8 dBm output power with 8 dB gain while drawing 48 mA from a 3.5 V supply. The corresponding peak drain efficiency is 20 %.

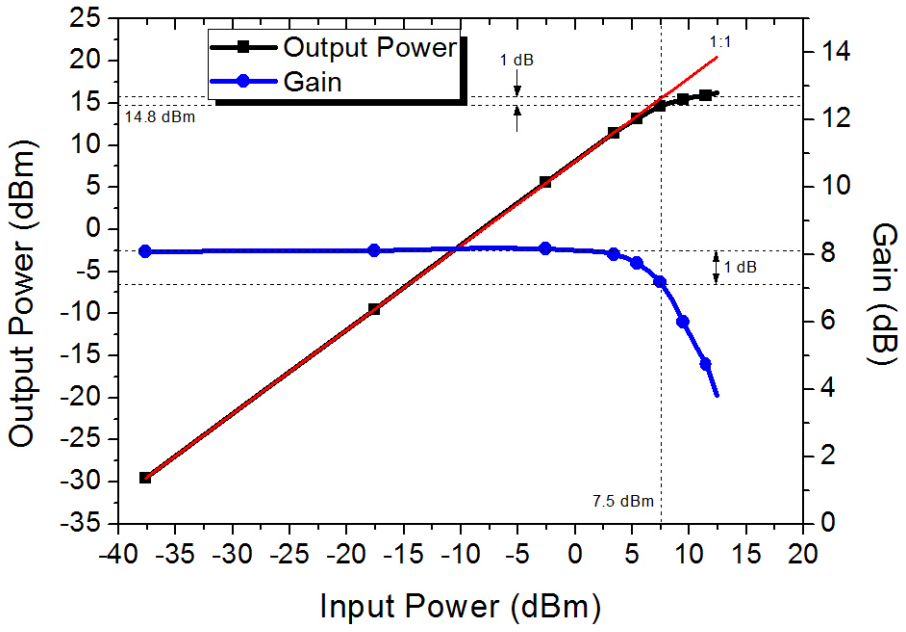


Figure 47: Output power and gain measurement results at 10 GHz.

4.3.2 Discussion

According to the measurements, there is frequency shift in S11, S22 and S21 values with respect to simulation where both S11 and S22 are matched to 50 Ω at 10 GHz with a small-signal gain of 13 dB. There are two reasons for this measured frequency shift; grounding and deficiency of by-pass capacitor shown in Fig. 48. L1 inductor used for the input matching network is not grounded well and connected directly one of the ground ports of the RF port. However, this is not enough because this type of connection is not well-grounded and the inductance value of the input matching network is increased due to the additional inductance contribution from the port. Moreover, the by-pass capacitance between the supply and ground is not enough to RF-short any parasitic contribution by bond-wire inductance. Therefore, the output matching is also shifted due to the additional inductance of bond-wire.

After the system specifications and requirements of blocks are determined, a new two-stage power amplifier is designed while these problems are taken into consideration.

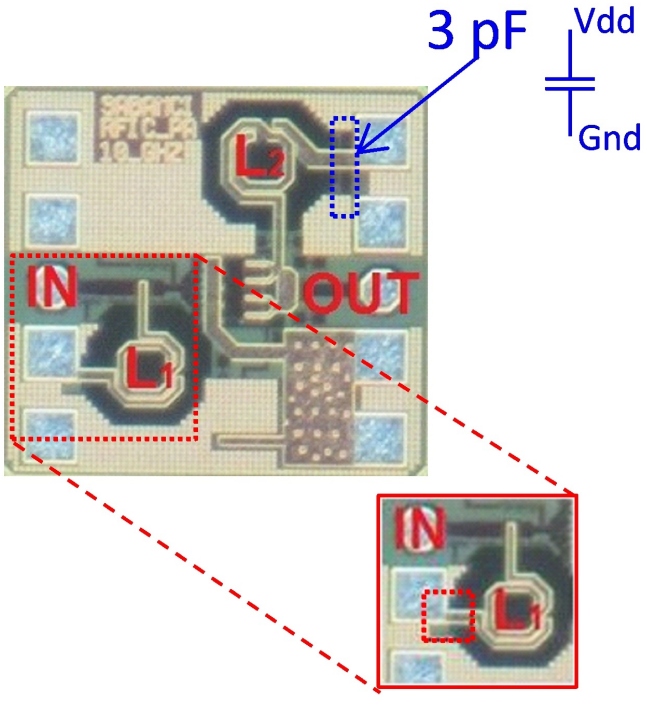


Figure 48: Grounding problem in the designed power amplifier.

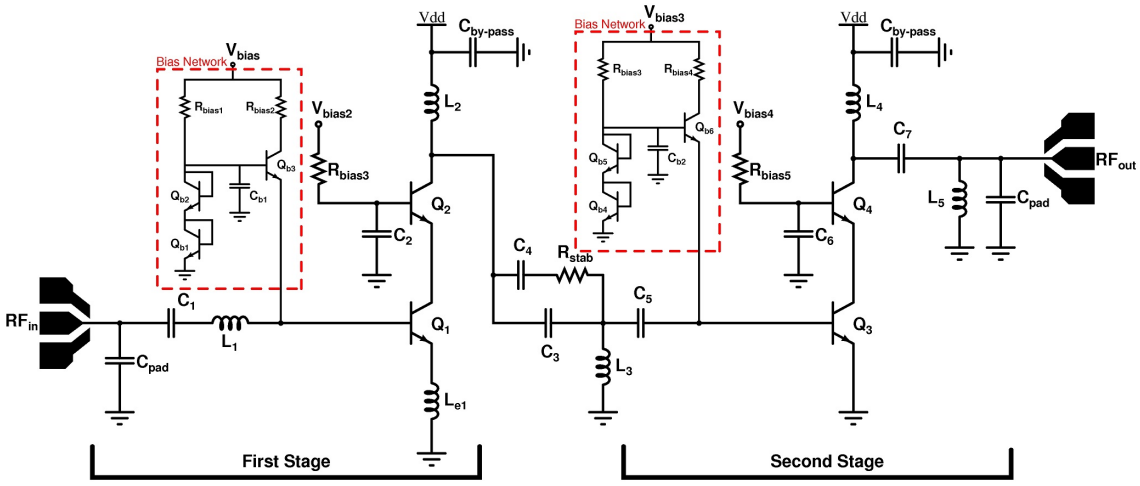


Figure 49: Schematic of the two-stage X-Band power amplifier.

4.4 Two Stage Power Amplifier Design

As it has been the case for the single-stage power amplifier, two-stage power amplifier is also designed in Class-A mode due to high output power and gain, but especially for the system requirements such as modulation. Since the RF bandwidth of pulse mode radar will be around 1 GHz, it is more suitable to make the group delay variation of the power amplifier as less as possible. Therefore, Class-A mode amplification is suited best as the class type. Also, as much output power as possible will be better for this design; therefore more than 22 dBm output power will be the aim.

In order to fulfill the design requirements of the T/R module, power amplifier specifications are given in Table 5.

The two-stage power amplifier design starts with the output stage. In the first place, the output stage needs to deliver the required output power. For this reason, I-V characteristics of transistors are analyzed and a bunch of transistors are used in parallel to draw enough current to catch specifications. In this stage, all bias

Table 5: Power amplifier specifications.

Bandwidth	8-12 GHz
Gain	$>$ 20dB
P_{1dB}	$>$ 22dBm
Input & Output Impedance	50 Ω
Supply Voltage	4 V
PAE	$>$ 25%

voltages and currents are determined. In the second place, output matching network is investigated for maximum power transfer but most importantly for maximum output power. Since the output stage is the most power-hungry module in the power amplifier, output matching network is selected carefully to minimize any parasitic resistances. The selected operating 4 V and the bias current is 120 mA. The output node can swing between 0.5 V to 8 V while all the transistors work in the active region. Therefore, the optimum load impedance is between 25 and 30 Ω due to voltage drops on parasitic resistances of inductors and metal connections. Therefore, 50 Ω load has to be converted to approximately 30 Ω with output matching network.

The next step is the design of first stage and inter-stage matching network. The first stage also biased at Class-A mode and draws much less current than the second stage. This stage helps to achieve required 25 dB small-signal gain. Input matching network is designed according to straight-forward conjugate matching for maximum power transfer. At the end, the inter-stage matching is designed to conjugate match input impedance of the second stage to the output impedance of the first stage. A T-type inter-stage matching is designed to increase the bandwidth of the amplifier. As a result, the schematic of the two-stage X-Band power amplifier is given in Fig. 49. Moreover, component values of the design are also given in Fig. 50. It is important that all components are custom designed including inductors. Finally, the design of the output matching network with the smith chart reference is given in Fig. 51. The

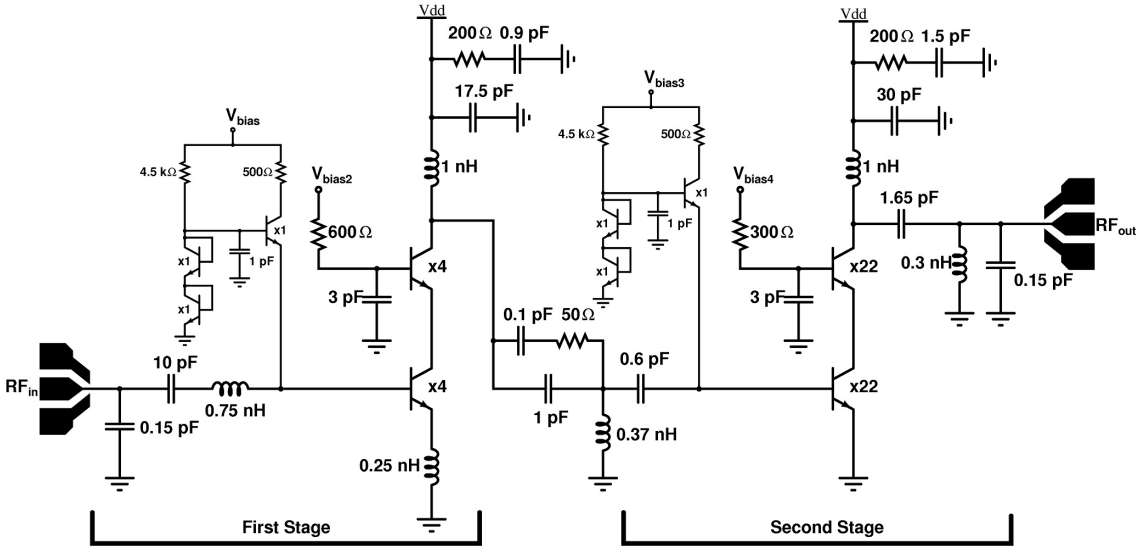


Figure 50: Schematic of the two-stage X-Band power amplifier, component values are indicated.

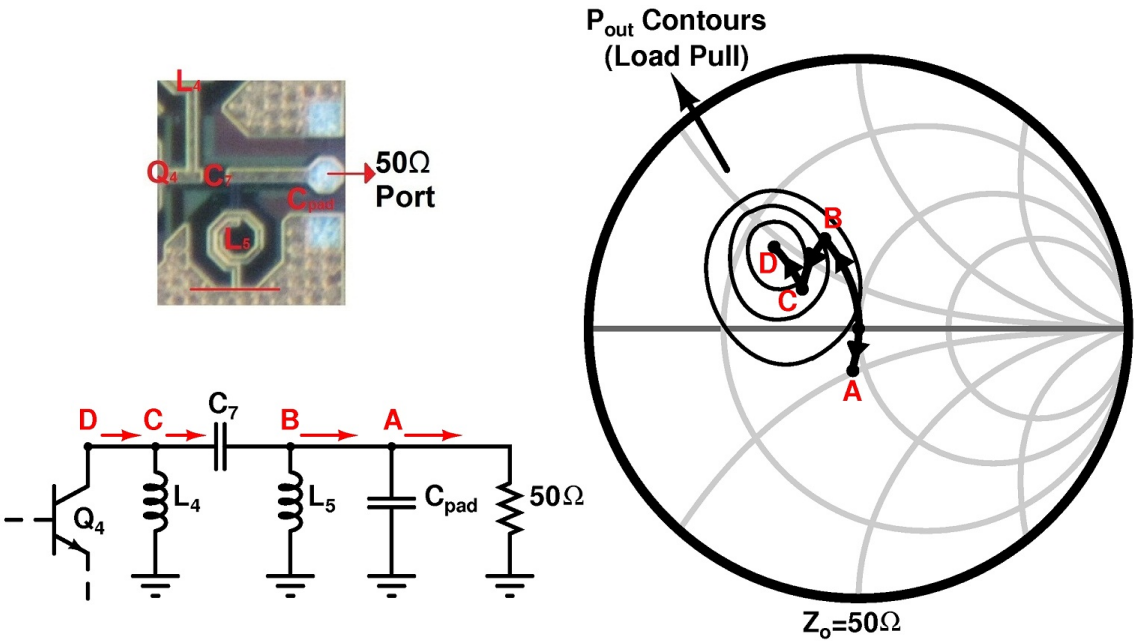


Figure 51: Design of the output matching network with the smith chart reference.

capacitance C_{pad} is the parasitic capacitance of the RF-pad between Top-Metal2 and substrate-ground. This parasitic capacitance of the RF-pad is around 60 to 80 fF and it is large enough to affect the output matching at 10 GHz.

4.4.1 Special Considerations

As it is the case for all circuits at any frequency, there are technology and frequency-dependent problems. The design of a power amplifier is straight-forward, and one can find tens of books about it. However, when it comes to design a high frequency, on-chip power amplifiers, it is maybe one of the most challenging building blocks of a T/R module due to parasitic, low-Q passives, chip area, heat and etc. Therefore, we faced with some problems while designing the power amplifier and special considerations are taken into account.

One of the problems is the grounding as mention in previous sections. Because passives and transistors are connected to a perfect-ground in the simulations and DC-probes and bond-wires are used in the measurement setup, measurement results deviate from the simulation results as it was the case for the single-stage power amplifier. For example, inductance value of a bond-wire changes from 1 nH to 10 nH depending on the length of the wire and frequency. This inductance is directly added

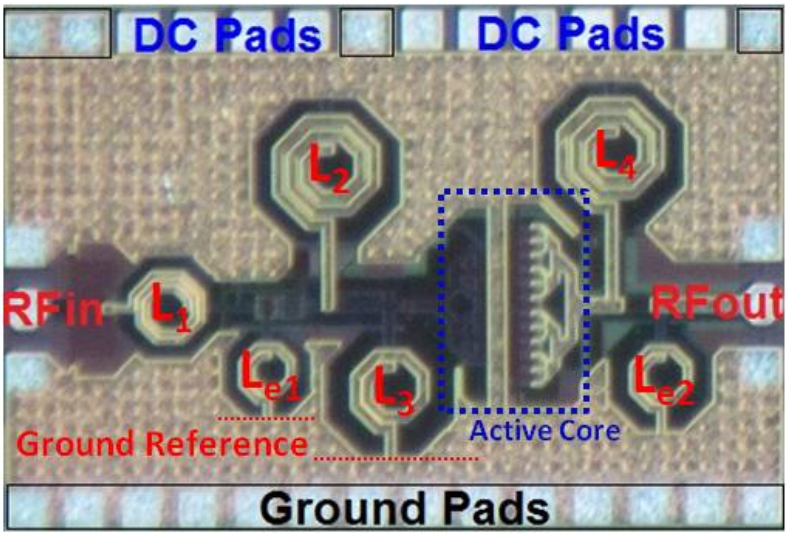
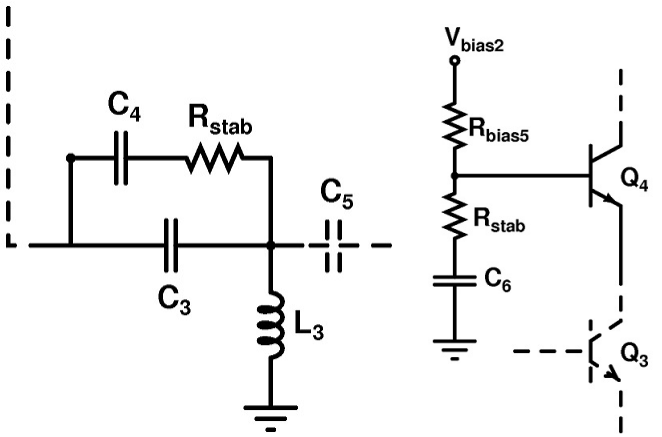


Figure 52: Die photo of the designed two-stage X-Band power amplifier.

to the circuit and changes the operating frequency and everything. To overcome this, Top-Metal2 is used as the ground and inductors are simulated until this big ground, Ground Reference, as shown in Fig. 52. With this method, inductors are located anywhere of the chip because we have the ground everywhere. It is important that Top-Metal2 is connected to the substrate of the chip with vias. Also, lots of ground pads are located to connect Top-Metal2 to the ground of the package.

The second problem is again about bond-wires but this time on the output part of the circuit. To prevent additional inductance of bond-wires at the supply node of the circuit, several capacitors are connected in parallel to make this node RF short. Therefore, empty parts of the layout are filled with capacitors. As known, this is not a special process to high frequency and on-chip circuits but used in every active circuit.

Lastly, stability is analyzed through the power amplifier design. The stability was not taken into account deeply in the beginning because of the cascode topology. As we mentioned earlier, the stability of the cascode topology is better than a CE amplifier because of the cascode transistor. However, the stability becomes critical during the inter-stage matching and the layout. The inter-stage matching network results in an extra pole in the circuit and, thus, a low frequency (1-4 GHz) stability problem is observed. It is clear that power amplifier has to be stabil not only in the operating band but also all over the spectrum. Therefore, a simple RC is connected in parallel to capacitor C_3, as shown in Fig. 53(a). Moreover, as shown in Fig. 53(b),



(a) The base of cascode pair (b) Inter-stage matching

Figure 53: Analysis of stability at (a) the base of the cascode pair, and (b)inter-stage matching network.

the capacitance C_6 is connected to the base of the cascode device. However, if this connection comes with a parasitic inductance in the layout, this results in a stability problem and with a small resistance R_{stab}, one can prevent this stability problem. However, any resistance, R_{stab}, will change the output impedance and performance of the circuit because an ideal RF short is needed at this node. Instead, we bring the capacitance C_6 near enough to the cascode device so that any parasitic inductance is prevented.

4.4.2 Measurement Results

The power amplifier is fabricated in IHP's 0.25 μm SiGe BiCMOS process technology and bonding of the chip is performed by ourselves as shown in Fig 54. The

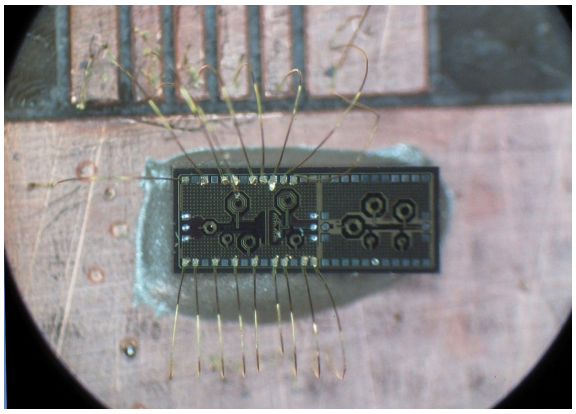


Figure 54: The chip with bond-wires.

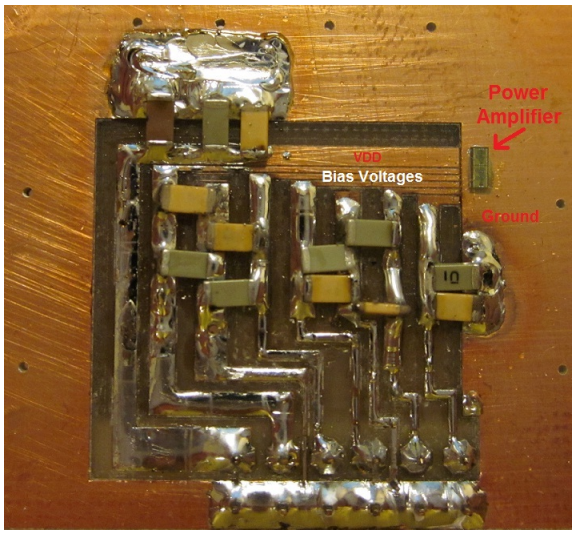


Figure 55: Designed test-board for the power amplifier.

pins on the bottom row of the chip are bounded directly to the ground, PCB. On the other hand, other pins are bonded to each of lines in Fig. 54. Different from other pins, two bonds are used to connect the supply pin to lower parasitic inductance and resistance of bond-wires. On the PCB, several value capacitors are used for each bias line to filter any noise received from cables and other instruments, as shown in Fig. 55. In the measurement setup, shown in Fig. 56, two 100-μm pitch GSG Z040 Z-probes are used in the input and output ports. All bias voltages are supplied by coaxial cables to decreases noise coupling. And finally, the drawing of the small-signal measurement setup is given in Fig. 57. On the other hand, large-signal characteristics are measured in the same setup shown in Fig. 45.

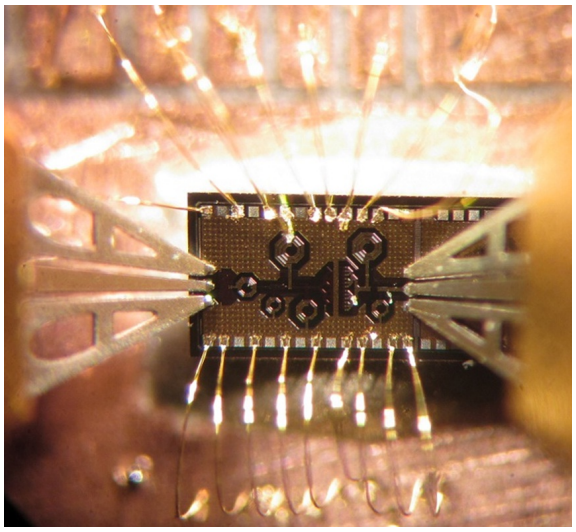


Figure 56: Chip photo of the measurement setup.

First s-parameter measurement results are shown in Fig. 58. Although there is nearly 1 GHz frequency shift, the small-signal gain of the power amplifier is more than 23 dB with a gain variation of 4 dB between 8.5 GHz and 11.5 GHz. Moreover, input matching is better than 9 dB more than 5 GHz bandwidth as shown in Fig. 58. Because maximum output power is the essential design criteria, output matching is not as good as input matching and lower than 10 dB for 2 GHz bandwidth and better than 5 dB in the overall X-Band. Although it is not shown in the simulation results, reverse gain (S12) is better than 45 dB from up to 20 GHz due to two-stage cascode topology. And finally, there is no indication of an oscillation in the overall spectrum.

In addition to small-signal results, the large-signal measurement results are shown in Fig. 59. The frequency shift approximately 1 GHz can also be seen in the large signal measurements. The designed power amplifier achieves output referred 1 dB compression point (P_{1dB}) of 22.2 dBm at 9 GHz. For a 3 GHz bandwidth, power amplifier produces more than 20 dBm output power on 50 Ω load. The frequency response of the output power and saturation power is given in Fig. 60. The maximum output power (saturation) that power amplifier achieves is 23.2 dBm, which is more than 200 mW. Although there are several techniques to improve P_{1dB}

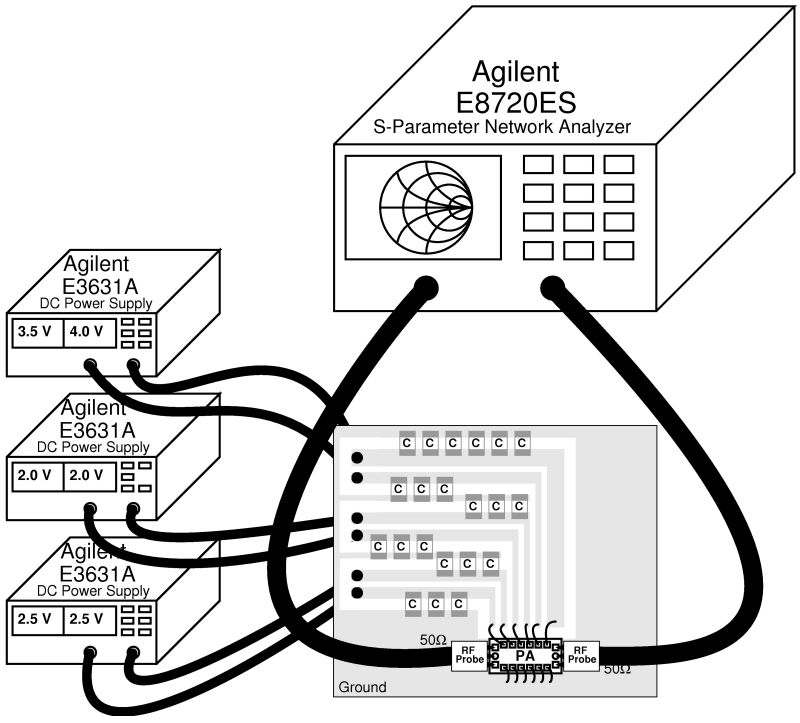


Figure 57: Measurement setup.

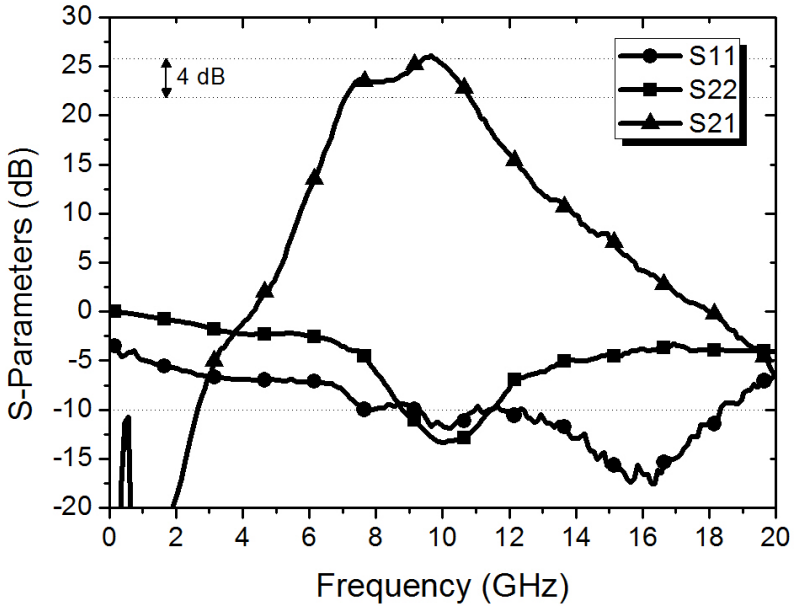


Figure 58: S-parameters measurement results of the designed X-Band PA.

of the power amplifier, these techniques are not utilized to keep the design simple. However, higher output powers can be achieved by increasing the bias voltages in the expense of reliability.

Lastly, power-added efficiency (PAE) of the power amplifier is given in Fig. 61. The first stage draws 4 mA from 3.2 V supply whereas the second stage draws 70 mA from 4 V supply in small-signals (smaller than -10 dBm). For high input powers,

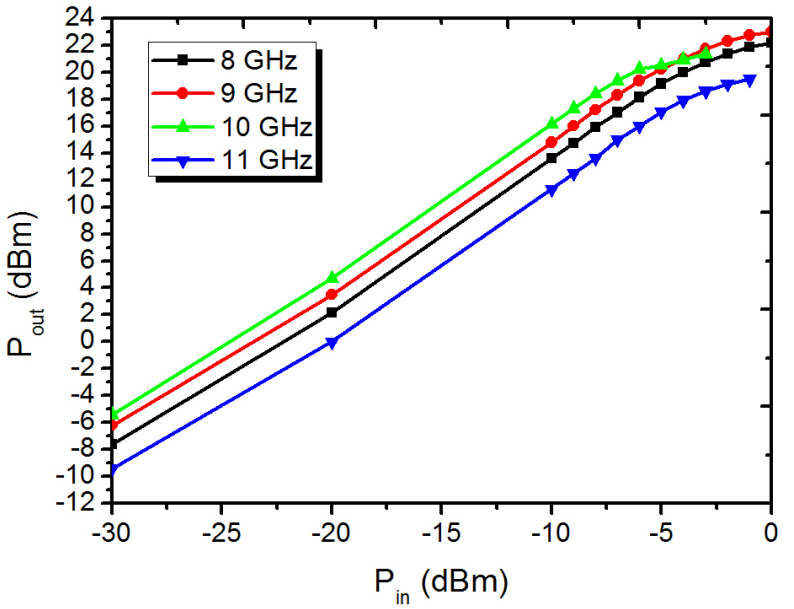


Figure 59: Measurement results of the output power vs. input power at several frequencies.

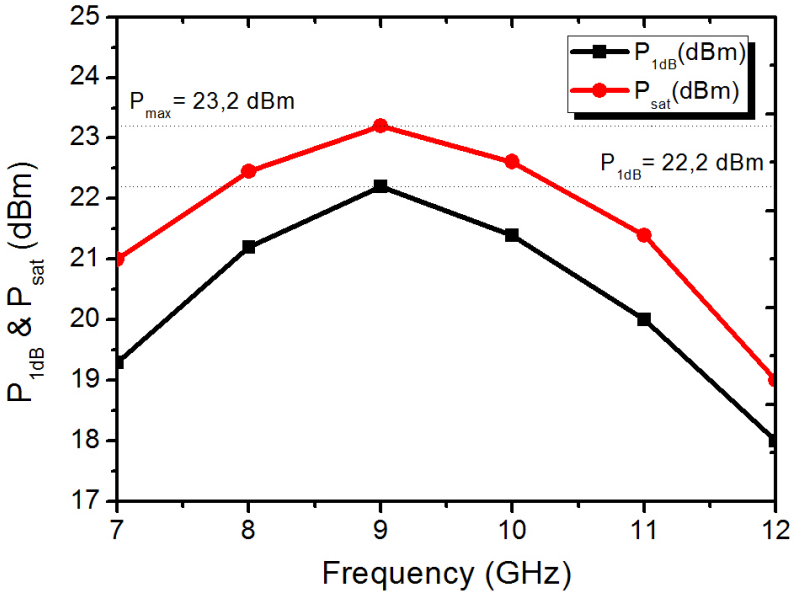


Figure 60: Measured saturated output power and power at the output-referred P_{1dB}.

the DC current consumption increases up to 120 mA for the second stage. As a result, shown in Fig. 61, the power amplifier achieves more than 25 % of PAE in a 3 GHz bandwidth from 8 GHz to 10 GHz at the 1 dB compression point. Lastly, the power amplifier has a 30 % PAE in the saturation at 9 GHz, as shown in Fig. 61.

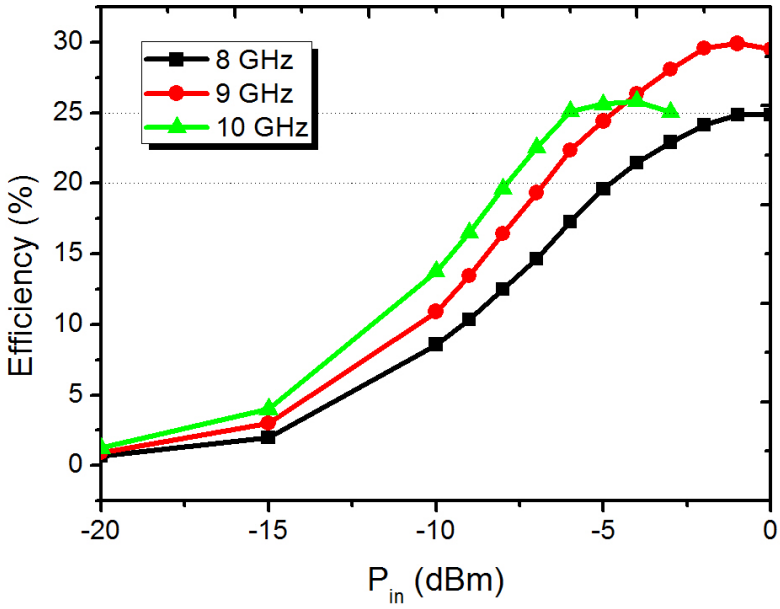


Figure 61: Measurement results of power-added efficiency.

4.4.3 Discussion

As a result, the designed two-stage PA fulfills all the requirements except approximately 1 GHz frequency shift. However, this is not a big issue because this problem will be solved in the full T/R module design. The comparison of the PA with other works in literature is given in Table 6 [54, 55, 56, 57]. According to the Table 6, the PA achieves comparable gain with comparable output power of 23.2 dBm with a compact area of 1 mm^2 and wide bandwidth of 3 GHz. Moreover, this design shows higher efficiency than other works in literature. There can be some improvements in the linearity of the amplifier with improved bias networks. This improvement may increase the output power of the PA even more. Moreover, the center of the operating band has to be at exactly 10 GHz to cover whole X-Band. Also, the output matching of the amplifier may be improved with better output matching networks of usage of on-chip transformers. However, the design of an on-chip transformer is more complicated than inductor design because of the area and efficiency issues.

Table 6: Comparison of the PA with Reported Works

Frequency (GHz)	Figures of Merit				Chip Area mm^2	Technique	Technology	Ref.
	Gain (dB)	P_{OUT} (dBm)	PAE (%)	VDD (V)				
7.3−10.5	**25.5**	**23.2**	**28**	**4**	**1.0**	**Two-stage, cascode**	**0.25μm SiGe BiCMOS**	**This Work**
8.6-10.3	25	24.5	18	3	1.2	Two-stage, differential, cascode	0.18μm CMOS	Jonathan 2011
8.5−10.0	29	23.5	19	3.3	1.3	Two-stage, differential, cascode	0.18μm CMOS	Ku 2008
8.5−10.5	41	21.4	26	NR	1.3	Two-stage, cascode	0.13μm SiGe BiCMOS	Andrews 2007
3.7−8.8	8.2	19	25	NR	2.8	Distributed, cascode	0.13μm SiGe BiCMOS	Lu 2007

5 X-Band Phased Array Antenna Design

In this chapter, a phased array antenna design will be discussed through simulations and measurement results. Until now, blocks of a T/R module introduced and simulation/measurement results are provided. To complete a fully functional phased array system, several of T/R modules are needed to be used with antennas included, as shown in Fig. 62. A fully-integrated T/R module is not ready, therefore there is no need an antenna right now. However, to warm up future work of this fully-integrated T/R module project, a X-Band antenna has to be designed and maybe analyzed in an array format. Therefore, in the scope of Antennas & Propagation course, a X-Band microstrip patch antenna array is designed and measured as a proof-of-concept for 10 GHz direction finding applications. To do so, a circular phased array is designed consist of three antenna elements utilizing two Hittite HMC931LP4E Analog Phase Shifters. Rogers RT/duroid 5880 high frequency laminates are used to achieve high-efficiency antennas at 10 GHz.

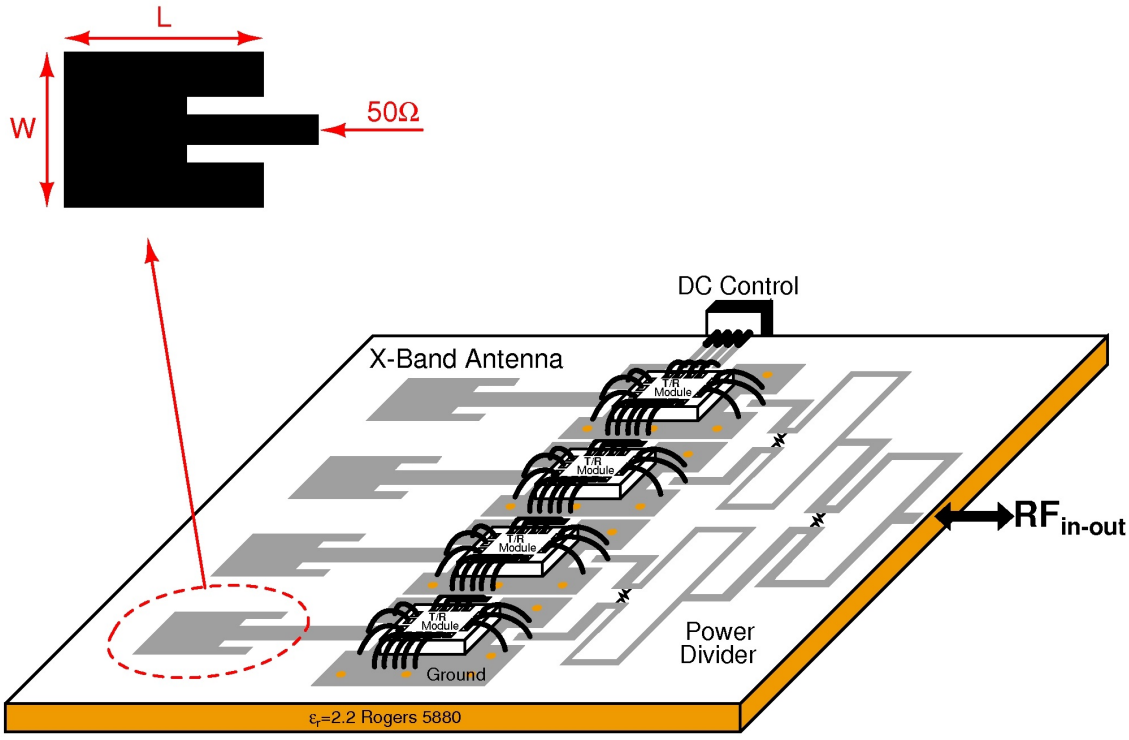


Figure 62: Antenna element in a full T/R module test setup.

5.1 Direction Finding

There are two primary methods that examine for single channel direction finding (DF); Watson-Watt Method using an Adcock antenna array known as amplitude based and Pseudo-Doppler Method using a circular array known as phased based method [58, 59].

Watson-Watt DF method is an amplitude-based method that uses relative amplitudes of antennas in an array arranged according to the Adcock design. The Adcock design consists of four antenna elements arranged in a perpendicular, crossed-baseline configuration. In this configuration, received signals are subtracted between pairs and the outputs give the direction of the target. Although this method is an effective way to find the direction, it requires high precision amplifiers to detect the amplitude difference between two antenna elements nearby. This can be possible for frequencies up to 1 GHz, but for an application at 10 GHz, this will be hard to handle at such high frequency. Moreover, this method requires circuits for phase and magnitude imbalance, sum and difference hybrids and etc.

Another direction finding method is the Pseudo-Doppler method based on Doppler shift on successive elements in a circular array. Measurements of incoming signal from each element enable the direction of the target. In principle, when we move an antenna in a circular path, the instantaneous frequency of received signal will be shifted. As the antenna moves, it imposes as Doppler shift on the received signal. The Doppler shift is at a maximum if the antenna moves toward and away from the direction of the incoming wavefront. On the other hand, there will be no Doppler shift if the antenna moves in the orthogonal direction. Alternative to a moving antenna, a circular antenna array can be designed and a rotating RF switch can be used. If the size of the circular array is increased, the resolution increases but this requires more switches and area.

In our design, a simple circular array will be designed like Pseudo-Doppler method but the direction of the main beam of the antenna array will be moved to find the direction of the target. Because maximum signal is received in the direction of the main beam, by changing the direction of the beam we can detect the target. This is a simple method and not as efficient as other two methods. But with a few antenna elements and phase shifter, one can easily design a DF circuit.

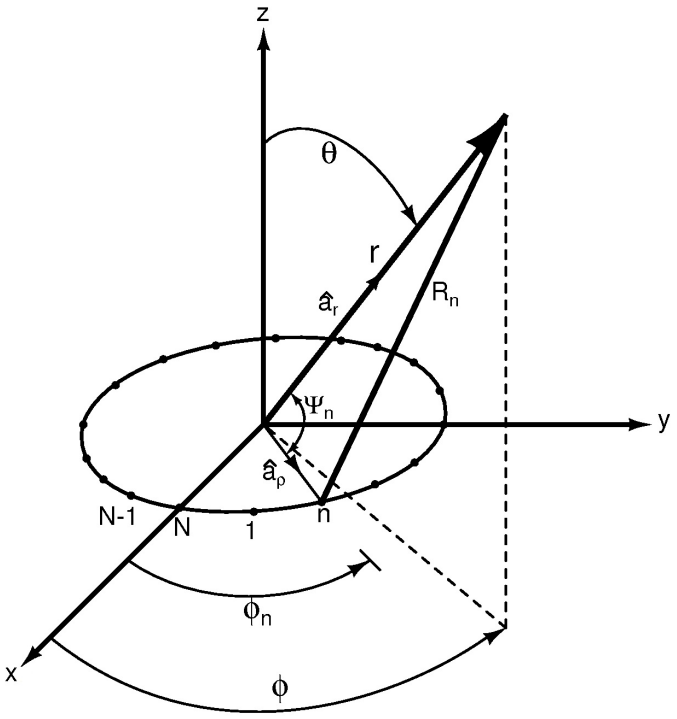


Figure 63: An N-element circular array.

5.2 Array and Feed Network Design

For this particular application, a three-element circular antenna array is designed. Because we have only two phase shifters, the number of elements in the array is limited to three; two of them will be connected to phase shifters and third element will have always 0° degree phase. To understand the theory of circular array antennas, let's first examine the phase shifting activity. Referring to Fig. 63, let us assume that there are N isotropic, equally spaced antenna elements on the x-y plane along a circular path of radius a. Using the same analysis that is used to derive the array factor of a linear array show in Fig. 2, one can easily derive the array factor for a circular array of N equally spaced elements such that [60]

$$AF(\theta,\phi) = \sum_{n=1}^{N} I_n e^{j[ka\sin\theta\cos(\phi-\phi_n)+\alpha_n]} \tag{29}$$

Here the peak of the main beam is in the $(\theta_0 - \phi_0)$ direction and the phase excitation of the nth element is required to be

$$\alpha_n = -ka\sin\theta_0\cos(\phi_0 - \phi_n) \tag{30}$$

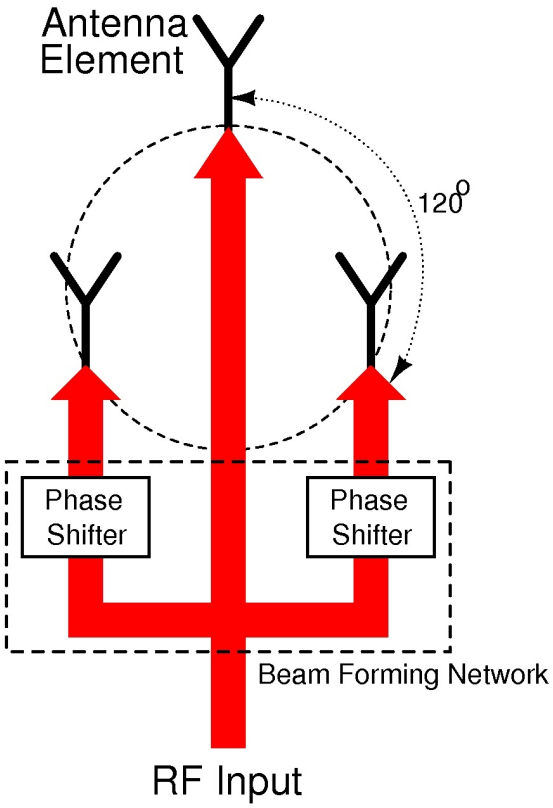


Figure 64: Three-element circular antenna array and feed network.

According to this formula, the phase configuration of the antenna array will be analyzed in the following sections of this chapter.

As a result, a three-element circular antenna array is designed in the configuration shown in Fig. 64. There are 120° angle and approximately 0.75λ distance between successive elements. One of the elements in the antenna array is directly drive and two of the elements are driven by phase shifters. Therefore, beam feed network consists of two phase shifters and transmission-lines as shown in Fig. 64.

5.3 Antenna Elements

Before analyzing the antenna array let's first look at a single antenna element as shown in Fig. 65. For this application a microstrip patch antenna is used in the antenna array. As it is known, microstrip antennas consist of a very thin metallic strip (patch) above a ground plane. The microstrip path is designed so that its radiation pattern is normal to the patch. There are several excitation methods for patch antennas; line feed, probe feed, aperture-coupled and proximity-coupled feed. Because phase shifters are used in this design, we will feed the antenna elements using

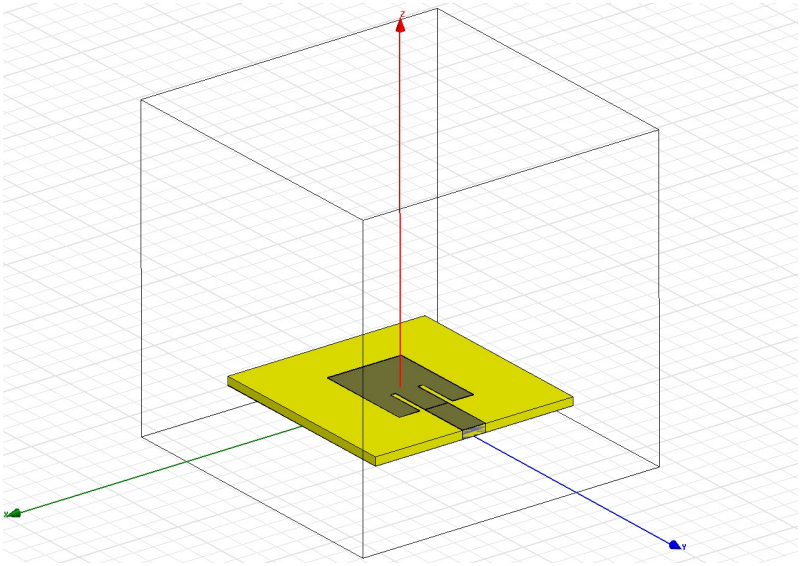


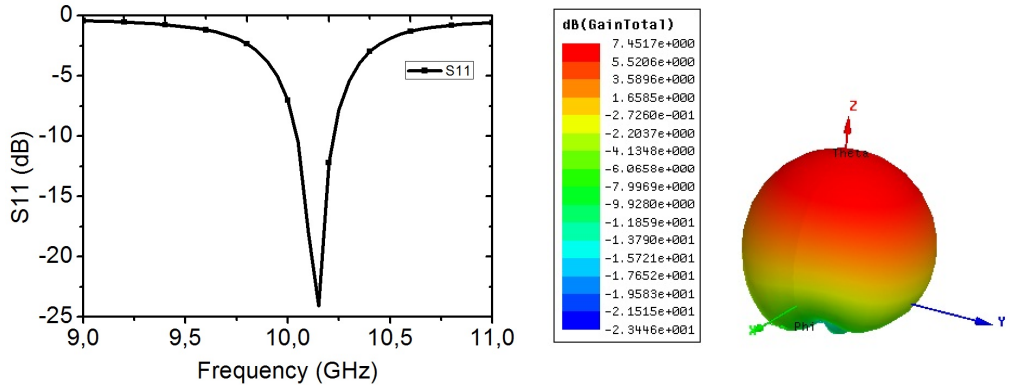
Figure 65: Single antenna element used in circular array.

line feed method. For a rectangle patch, the length of the patch antenna is usually $\lambda_0/3 < L < \lambda_0/2$. If we consider the dielectric constant of Rogers RT/duroid 58880 as 2.2 and the operating frequency as 10 GHz, the length of the antenna element can be calculated approximately 1 cm. With these dimensions, resonant input resistance of a rectangle patch antenna is higher than 50 Ω. However, it has been shown that the resonant input resistance can be changed with an inset feed as shown in Fig. 65. With this technique, the input resistance of the antenna element is matched to 50 Ω easily.

According to these techniques, a 10 GHz antenna element has already designed and simulated in a 3D full-wave electromagnetic field simulator, HFSS^{TM}. S11 and radiation pattern of the antenna element are given in Fig. 66(a). As shown in Fig. 66(a), it's input is matched to 50 Ω at 10.15 GHz and has a bandwidth of 180 MHz (10 dB bandwidth) which equals to 1.7 % bandwidth. This is a very narrow bandwidth but it is typical value for thin substrate microstrip patch antenna. In addition, the antenna element has a directivity of 7.4 dB with an efficiency of 96 %, which are again typical values, as shown in Fig. 66(b).

5.4 Antenna Array Design Without Phase Shifters

In order to realize the proposed DF method, a three-element circular array antenna is designed using two Hittite HMC931LP4E Analog Phase Shifters. The an-



(a) S11 for an antenna element (b) Directivity of an antenna element

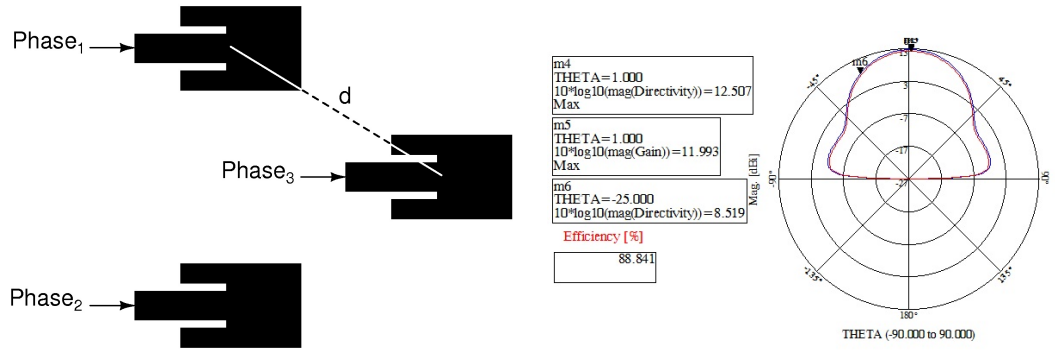
Figure 66: Simulation results for an antenna element shown in Fig. 41, (a) S11, and (b) Directivity

tenna elements are positioned in a circular path with a spacing $d = 0.75\lambda$ between successive elements as shown in Fig. 67(a).

In order to realize the proposed DF method, a three-element circular array antenna is designed using two Hittite HMC931LP4E Analog Phase Shifters. The antenna elements are positioned in a circular path with a spacing $d = 0.75\lambda$ between successive elements as shown in Fig. 67(a).

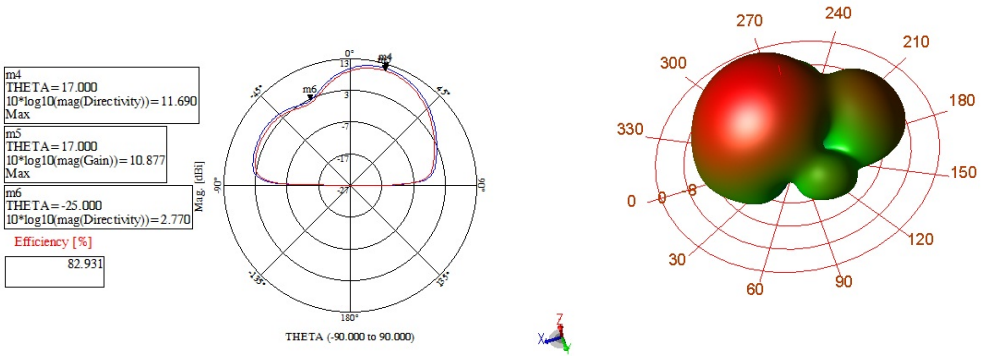
First, antenna array with only three elements are simulated in ADS Momentum due to simple construction and easy handling. As shown in Fig. 67(b), antenna has 12.5 dB directivity (7.5 dB from the antenna and 4 dB from the array gain 10log (3) = 4 dB) with an efficiency of 88 % due to substrate loss.

Next, different excitation phases are applied to the antennas according to (30). A simple MATLAB code, given in Appendix B, is generated to find relevant excitation



(a) Three-element circular antenna array (b) Directivity, gain and efficiency

Figure 67: Simulation results for three-element antenna array: (a) placement, and (b) antenna parameters.



(a) Polar plot of antenna parameters

(b) Radiation pattern

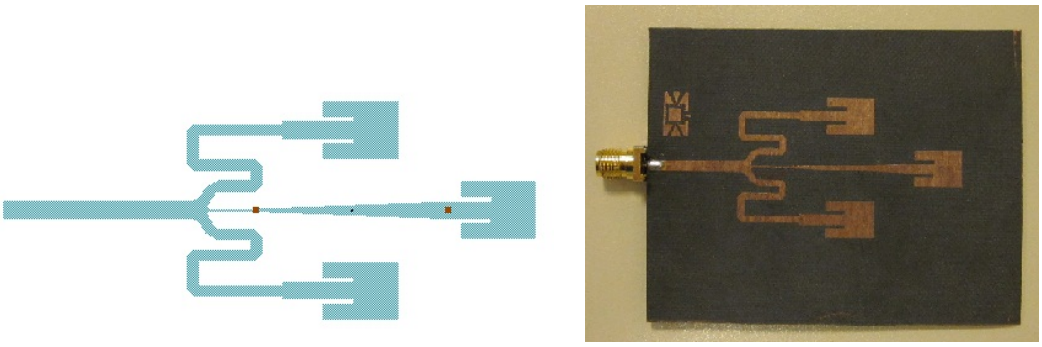
Figure 68: Simulation results for three-element antenna array with an angle of direction: (a) polar plot, and (b) radiation pattern.

phases of all elements for the required direction (θ, ϕ). For example, each element in the array is excited with uniform amplitude and different phases to achieve $\theta = 20°$ and $\phi = 0°$. To do so, 30°, 30°, and $-60°$ phases are applied to 3 isotropic elements according to the array theory and simulation results are given by both polar plot in Fig. 68(a) and 3D pattern in Fig. 68(b), respectively. It is important to note that only 17° theta angle could be achieved rather than 20° due to non-isotropic antennas and proximity of ground as shown in Fig. 68(a).

The final step is the design of beam forming network for antenna array. Because we have three elements in the array, a three-way power divider is required. However, due to the insertion loss of phase shifter used for only two of the antenna elements, an unequal three-way power divider is required for this design. In addition, electrical length of feeding network has to be equal for each element because we want radiation angle to be 0° for both theta and phi angles. Therefore meandered transmission lines will be used to achieve the same electrical length for all elements. The final layout and fabricated three-way unequal power divider with equal electrical length is shown in Fig. 69(a) and Fig. 69(b), respectively.

5.5 Antenna Measurements

After fabricating the antenna, input impedance is measured using Agilent E8720S Network Analyzer. Measured S11 results fit simulation results perfectly as shown in Fig. 70(a). From these results, at least we can understand that antenna has some



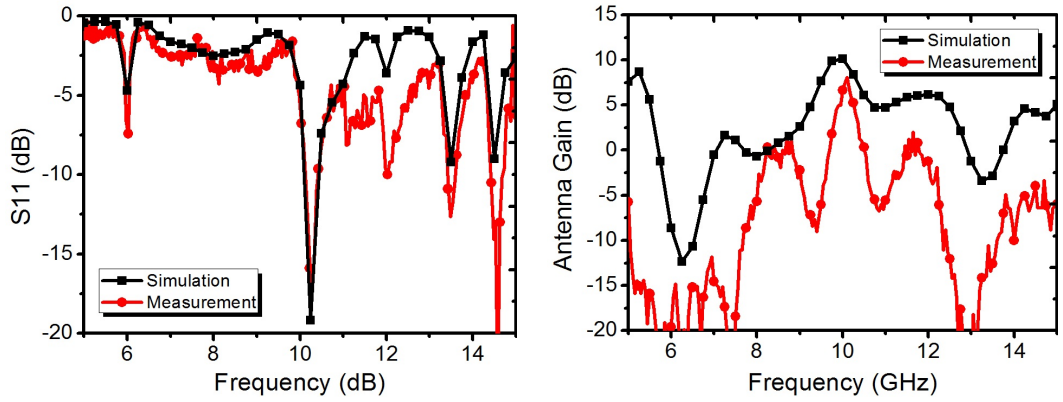
(a) Layout of antenna array (b) Fabricated antenna array

Figure 69: (a) Layout and (b) fabricated antenna array.

radiation at 10.1 GHz. However, extra measurements are required to determine the antenna gain. Therefore one of the gain measurement techniques is used as shown in Fig. 71. A horn antenna which has a known gain at 10 GHz is placed 2 meters away from the antenna. For the gain measurement, we have to consider the far-field condition. The far-field conditions are summarized as follows [60]

$$\begin{aligned} r &> \frac{2D^2}{\lambda} \\ r &>> D \\ r &>> \lambda \end{aligned} \tag{31}$$

where r is the distance between antennas, λ is the wavelength and D is the line source. However D is the diagonal length of the horn antenna which is equal to



(a) S11 (b) Gain

Figure 70: Measured and simulated (a) S11 and (b) gain of the antenna.

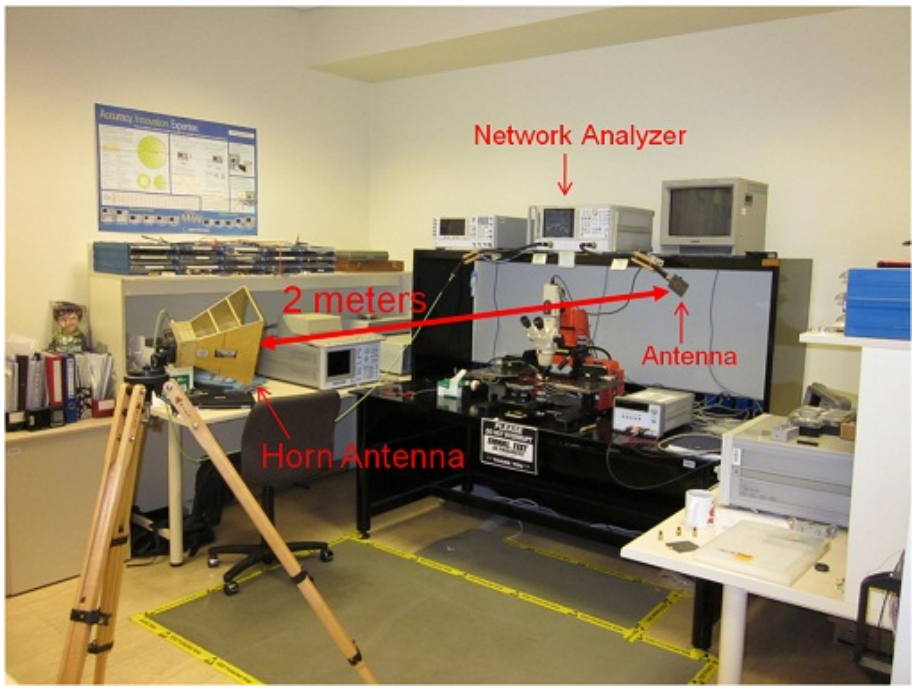
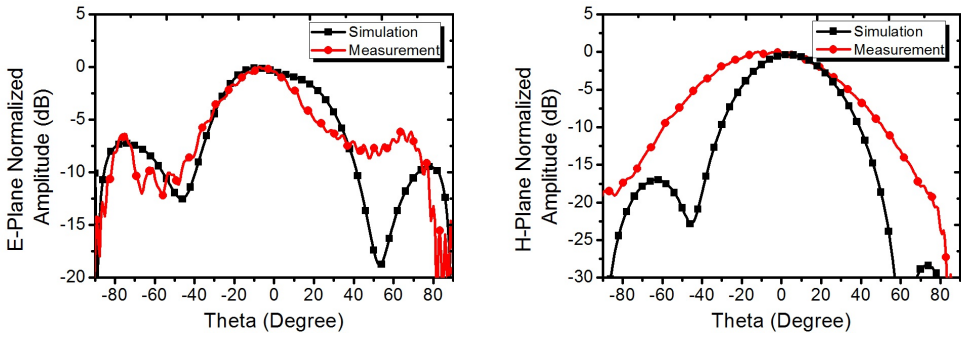


Figure 71: Antenna measurement setup.

20 cm in this measurement setup. According to (31) the minimum distance has to be 2.67 meters but there was not enough space in front of the network analyzer. However this is not very critical for our measurement because only gain of the antenna is measured.

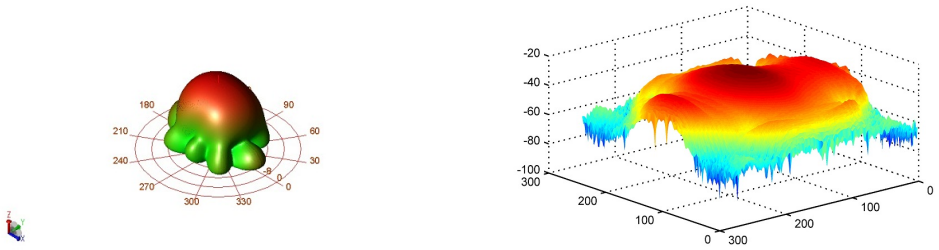
After all calibrations are performed, the insertion gain (S21) between two ports of the network analyzer is measured. According to Frii's transmission equation,

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 \tag{32}$$



(a) E-plane (b) H-plane

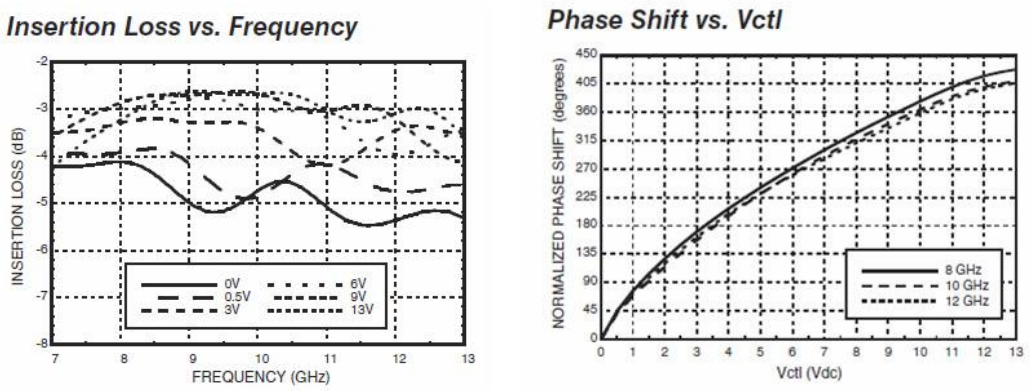
Figure 72: Simulated and measured (a) E-plane and (b) H-plane normalized amplitude of the antenna.



(a) Simulated (b) Measured

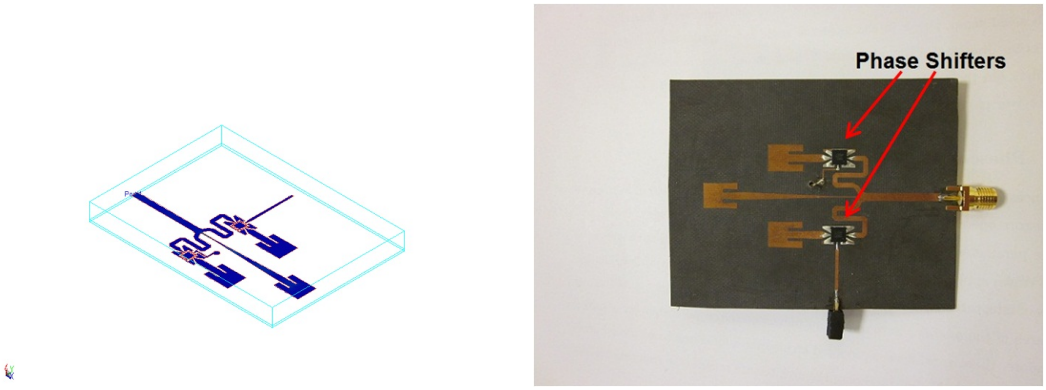
Figure 73: (a) Simulated and (b) measured radiation pattern of the antenna.

where P_t and P_r are the transmitted and received power, G_r and G_t are the gain of the receiver and transmitter antennas, and R is the distance between antennas. The inverse of the factor parentheses in (32) is the so-called free-space path loss. P_r/P_t is measured which is S21, G_t, gain of the transmitter horn antenna is known as 10 dB, and free-space path loss is calculated for 10 GHz and 2 meters of distance. As a result the simulated and measured gain of the antennas is given in Fig. 70(b). As shown in Fig. 70(b), the simulated gain of the antenna is 10 dB which is 2.5 dB lower than ideal case due to lossy substrate and power divider. According to measurements, the gain of the antenna is approximately 6 dB which is even lower than simulated results. We can attribute this difference to errors in the measurement setup and fabrication. Moreover, E-plane and H-plane measurements as well as 3D radiation pattern is performed in TUBITAK using near-filed measurement setup. E-plane and H-plane results are provided in Fig. 72(a) and 72(b). E-plane and H-



(a) Insertion loss (b) Phase shift

Figure 74: (a) Insertion loss and (b) phase shift of Hittite HMC931LP4E analog phase shifter with respect to frequency.



(a) Layout of antenna array (b) Fabricated antenna array

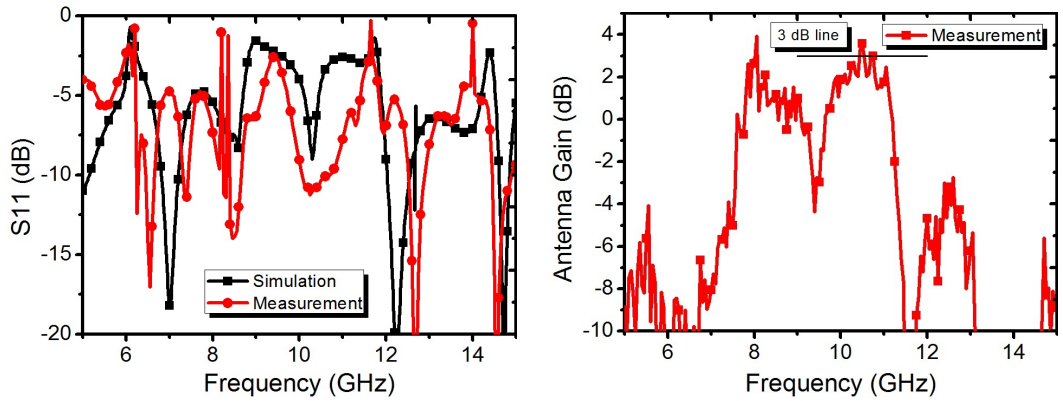
Figure 75: (a) Layout and (b) fabricated antenna array.

plane results are provided in Fig. 72(a) and 72(b). In addition to these, simulated and measured 3D radiation patterns are also given in Fig. 72(a) and Fig. 72(b), respectively.

5.6 Antenna Design With Phase Shifters

As mentioned before, insertion loss of the phase shifter is troublesome for the antenna design because all the analysis depends on the assumption of uniform amplitude excitation. Therefore an unequal three-way power divider is required to compensate losses of phase shifters. The insertion loss and phase shift of HMC931LP4E are given in Fig. 74(a) and Fig. 74(b), respectively [61].

After all compensations are performed, antenna array is designed and fabricated as shown in Fig. 75(a) and 75(b). Because simulation is not straight forward, only



(a) S11 (b) Antenna Gain

Figure 76: Measured and simulated (a) S11 and (b) gain of the antenna.

S11 is simulated considering 3 dB loss for each phase shifter using ADS Momentum. Again the same measurement setup is preferred and all results are given in Fig. 76(a) and Fig. 76(b). As shown in Fig. 76(a), input impedance of the antenna is not very well matched to 50 Ω due to losses and mismatches of phase shifters. Furthermore, the gain of the antenna is measured and it is approximately 4 dB lower than the antenna without phase shifters. Also the direction finding performance is not measured and rest of the measurements like E-plane, H-plane, gain and direction performance are planning to be measured in an anechoic chamber in TUBITAK.

6 Conclusion & Future Work

6.1 Summary of Work

Tremendous growth of RADAR and communication electronics requires low manufacturing cost, high performance, minimum area consumption, and highly integrated solutions for next generation Transmit/Receive (T/R) modules which are one of the most important blocks. Specifically, designing all sub-blocks in the same die in opposite to present T/R modules, where sub-blocks are designed separately and connected in a main-board, is the main aim of the next generation RADAR systems. To realize these ideas, new topologies are investigated to fulfill requirements of these RADAR systems where hundreds or thousands of T/R modules are utilized. In addition to the topological work, proper selection of the technology to realize these modules forms big portion of the overall work. With the recent improvement and developments, Silicon-Germanium (SiGe) Bipolar CMOS (BiCMOS) technology became a good candidate for these applications. Thus, III-V Technologies like GaN, InP and GaAs can be replaced with high speed Silicon based technologies to meet performance requirements of applications. Contrary to III-V T/R modules where all sub modules integrated discretely, SiGe BiCMOS technology will make it possible to integrate control circuits in the same chip which is a necessity of a fully-integrated T/R module.

In this thesis, system architectures for phased array T/R modules are investigated and design procedure and measurement results of several blocks are presented for the selected architecture. Especially, design steps with encountered problems are discussed for one and two-stage power amplifiers. Finally, a three-element phased array antenna is designed for a simple direction finding algorithm at 10 GHz.

Until now, three blocks are designed in addition to the power amplifier. These blocks are T/R switch, SPDT switch and low noise amplifier. T/R switch achieves 3-4 dB insertion loss at X-Band with a power handling performance of 28.2 dBm and isolation better than 23.2 dB. On the other hand, SPDT switch has lower insertion loss than T/R switch which is between 1.8 and 2.25 dB at X-Band. Finally, simulation results for two-stage low noise amplifier are given as; NF of 2.1 dB, more than 20 dB gain. Except the insertion loss of the T/R switch, the designed blocks

fulfill their requirements in the proposed T/R module.

Fundamentals of power amplifiers are discussed in Chapter 3. Power amplifier classes are introduced and some design considerations such as output power, power gain, efficiency, linearity and biasing are briefly covered. As the main focus of this thesis, X-Band SiGe BiCMOS power amplifiers are presented. Power amplifier requirement and challenges of achieving high output powers, specific to the selected technology, are discussed. As a first trial, a one-stage power amplifier is designed and measurement results are presented. The power amplifier achieves 8 dB gain with 14.8 dBm output power and 20 % drain efficiency. Problems of this power amplifier are clarified and this important data is utilized in the second power amplifier. A two-stage power amplifier is designed and measurement results are given. According to these results, amplifier achieves a small-signal gain of 25 dB at X-Band with a variation of 4 dB. Both input and output are matched to 50 Ω for system integration. The maximum linear output power is 22 dBm (higher than 20 dBm in a 3 GHz bandwidth) and maximum saturated output power is 23.2 dBm. The designed PA achieves more than 25 % of PAE for 3 GHz bandwidth.

Lastly, a phased array antenna operating at X-Band is designed as a future work for the proposed T/R module. Two phase shifters are used to form a three-element circular antenna array on Rogers RT/duroid 5880 high frequency laminate. First design without phase shifters achieves 6 dB gain due to losses of the unequal power divider and substrate. Moreover, the antenna array with phase shifters can achieve only 4 dB gain at 10.25 GHz due to losses of phase shifters.

6.2 Possible Future Work

The problems of the one-stage amplifier are already discussed in Chapter 4 and the two-stage amplifier is designed according to these results. However, there are still some problems of the two-stage amplifier like frequency shift and low frequency stability. As discussed before, the center frequency of operation for the PA is 9 GHz rather than 10 GHz. To cover 8-12 GHz bandwidth, the center frequency will be shifted to 10 GHz for the full T/R chip integration. Moreover, there are some problems at very low frequencies like 100 MHz. At large input signals, there are some signals observed at spectrum analyzer and the reasons of these are not truly

understood yet. However, SMD capacitors and measurement setup are suspected to be one of the reasons for this problem. The analysis and improvements will be performed for the future integration.

For the next step, the design of the amplifier will be performed again, giving special attention to the second stage and layout. Stability analysis will be one of the most important criteria for this design. Because the small-signal simulation and measurement results of the two-stage amplifier matches well, there will not be very much doubt about frequency shifts and modeling problems.

The integration of the power amplifier with other blocks will be the final step of the project. At the end, the fully-integrated T/R module will be measured and the project will be concluded with the final report.

A Appendix

In this section MATLAB code for generating Fig. 5 and Fig. 6 is given where d is the element spacing, N is the number of elements and *alpha* is the incidence of the angle desired. Also it is important to mention that this code is special to uniformly weighted, equally spaced antenna arrays.

```
function PhasedArray(d,N,alpha)
M=500
k=2*pi
deg=linspace(-90,90,M+1)
theta=(deg/180)*pi-pi/2
psi=k.*d.*cos(theta)+alpha*pi/180
AF=(sin(N*psi./2)./(N*sin(psi/2)))
plot(deg,10*log(abs(AF)),'-b')
```

Possible inputs are

PhasedArray(0.5,4,0) for 0.5λ spaced 4 element array with 0° incidence angle
PhasedArray(1,8,60) for 1λ spaced 8 element array with 60° incidence angle

B Appendix

```
function Phase(theta0,phi0,Nelem,rad)

thetalow=0;
thetaup=180;
philow=0;
phiup=360;
disc=181;
MM=disc;
NN=disc;
theta=linspace(thetalow*pi/180,thetaup*pi/180,MM+1);
phi=linspace(philow*pi/180,phiup*pi/180,NN+1);
k=2*pi;
dtor=pi/180;
AF=0;

arraya=zeros(1,Nelem);
for n=1:Nelem
phin(n)=2*pi*n/Nelem;
alpha(n)=-k.*rad.*sin(dtor.*theta0).*cos(dtor.*phi0-phin(n));
disp(alpha(n)/pi*180);
arraya(1,n)=alpha(n)/pi*180;
end

for n=2:1:Nelem
arraya(1,n)=(arraya(1,n)-arraya(1,1));
end
```

Possible inputs are

Phase(0,0,3,0.75) for 0.75λ spaced 3 element array, $\theta = 0°, \phi = 0°$

Phase(20,120,3,0.75) for 0.75λ spaced 3 element array, $\theta = 20°$, $\phi = 120°$

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2004 – 2009

Sabanci University Faculty of Engineering

Electronics Engineering (EE), B.Sc. GPA 3.75/4.00

Graduation Project: Fully Integrated, Multiband (WLAN and WiMAX) VCO-PA / Transmitter Design using AMS 0.35um SiGe HBT Technology

2000 – 2004

Edirne Anatolian High School

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Research Activities:

IHP–Innovations for High Performance Microelectronics

Position: Intern at Technology Department

Duration: 2009 Feb – May & Jun – Sep.

Responsibilities:

- Design and measurement of BiCMOS BEOL (Back-end-of-line) embedded capacitive RF-MEMS switches for mm-wave applications
- Design of multiband (2.4 – 4.8 GHz) VCO using capacitive RF-MEMS switch
- Design and simulation of substrate-etched inductors for mm-wave applications

ASELSAN Electronic Industry

Position: Intern in Microelectronics Group

Duration: 2008 Summer

Responsibilities:

- Design and analysis of infrared readout integrated circuits

PAVO Electronic Design House

Position: Intern in Analog Design Group

Duration: 2008 Summer

Responsibilities: - Design and measurement of Second-Order Butterworth Filter

Teaching Experience:

2011:

- Digital Integrated Circuits (EL302) by Assoc. Prof. Ayhan Bozkurt

2010:

- Radio Frequency Circuit Design (EL480) by Prof. Yaşar Gürbüz
- Electronic Circuits 1 (ENS203) by Assoc. Prof. Meriç Özcan
- Introduction to RF and Microwave Design (EL306) by Assoc. Prof. Meriç Özcan

2009 & 2008:

- Electronic Circuits 1 (ENS203) by Assoc. Prof. Meriç Özcan

Achievements and Awards:

2010:

- Co-authored the "Best Student Paper" at SIRF 2010, CA
- Graduate Scholarship from The Scientific and Technological Research Council of Turkey
- Full Graduate Scholarship of Sabancı University (Full tuition and dormitory fee exemption and monthly stipend)

2009:

- IEEE Microwave Theory and Techniques Society Undergraduate/Pre-Graduate Scholarship Award

2009 – 2005:

- Certificates of High Honor and Honor, Sabancı University

2009 – 2004:

- SU Honor Scholarship, ranking 541 among 1.8 Million Participants in the Nationwide University Entrance Exam (Full tuition exemption and monthly stipend

Skills:

Substantial IC design, tape-out and test experience :

-IHP 0.25um SiGe BiCMOS (tape-out and measurement)

-AMS 0.35um BiCMOS

CAD Tools:

-Cadence (SpectreRF, Assura, Diva, Virtuoso), ADS - Momentum, SONNET, HFSS, TCAD, Modelsim/Xilinx, Orcad Pspice, HP-Vee

Computer:

-C++, MatLab, Latex, Verilog, LabView, Linux, Unix, Solaris

Clean Room Experience :

-Photolithography, deposition, etching and alignment

Languages:

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Contributed Projects

a) X-band Phased-Array Transciever Module for RADAR Applications Using SiGe-BiCMOS and CMOS Integrated RFMEMS Switch Device Technologies", TUBITAK 110E107 project

b) RF Transmitter-Based Transducer for Biosensor Applications", TUBITAK 107E014 project

c) Development of Label-Free Aptamer Based Biosensors for the Early Diagnosis of Disease Using Capacitor Microelectrode Array Chip", TUBITAK project

Journal Publications

1) Zihir S., Tasdemir F., and Gurbuz Y., "A New LC Tank Circuit for 2.45 GHz Linearly Tunable VCO," Transactions on Microwave Theory and Technology, 2011 (submitted).

2) Dinc T., Zihir S., Tasdemir F., and Gurbuz Y., "A Fully Integrated, Highly Linear CMOS T/R Switch for X-Band Radar Systems," IEEE Journal of Solid-State Circuits, 2011 (submitted).

3) Dinc T., Zihir S., Tasdemir F., and Gurbuz Y., "A DC to 20 GHz 0.25-μm CMOS SPDT Switch," IEEE Microwave and Wireless Components Letters, 2011(submitted).

4) Dinc T., Zihir S., and Gurbuz Y., "A CMOS SPDT T/R Switch for X-Band on Chip Radar Applications," Electronics Letters, vol. 46 no. 20, 2010.

Conference Publications

1) Zihir S., Dinc T., and Gurbuz Y., "SiGe Building Blocks for On-Chip X-Band T/R Modules," Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF2012), 2012 (submitted).

2) Zihir S., Tasdemir F., Dinc T., and Gurbuz Y., "A New Resonant Circuit for 2.45 GHz LC VCO with Linear Frequency Tuning," European Microwave Week, Manchester, 2011 (accepted).

3) Dinc T., Zihir S., Tasdemir F., and Gurbuz Y., "A High Power Handling Capability CMOS T/R Switch for X-Band Phased Array Antenna Systems," European Microwave Week, Manchester, 2011 (accepted).

4) Quershi, A., Gurbuz, Y., Zihir S., and Niazi, J. H., "Label-free capacitive detection of bound C-reactive protein by complementary sequence using RNA aptamer functionalized capacitor," 2nd International Conference on Bio-Sensing Technology, Amsterdam, 2011.

5) Tasdemir F., Zihir S., and Ozeren E., "A New Lab-on-Chip Transmitter for the Detection of Proteins using RNA Aptamers," European Microwave Week, Paris, 2010, pp. 369-372.

6) Ozeren E., Zihir S., and Tasdemir F., "A Fully Integrated Multiband Frequency Synthesizer for WLAN and WiMAX Applications," European Microwave Week, Paris, 2010, pp. 489-492.

7) Kaynak M., Zihir S., Gurbuz Y., and Tillack B., "Characterization of an Embedded RF-MEMS Switch," In: SIRF2010, New Orleans, 2010, pp. 144-147. (Best Student Paper award)

8) Kaynak M., Zihir S., Gurbuz Y., and Tillack B., "Compact RF Model for S-Parameter Characteristics of RF-MEMS Capacitive Switches," in Mikrosystemtechnik Conference, Berlin, Sept. 2009.