Capacitance to Voltage Converter Design for Biosensor Applications

by

Ferhat Taşdemir

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Varactor Tunable Capacitance to Voltage Converter Design for Biosensor Applications

APPROVED BY

Prof. Yaşar GÜRBÜZ .....
(Thesis Supervisor)

Assist. Prof. Javed M. KOLKAR .....

Assoc. Prof. İbrahim TEKİN .....

Assoc. Prof. Meriç ÖZCAN .....

Assoc. Prof. Ayhan Bozkurt .....

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Capacitance to Voltage Converter Design for Biosensor Applications

Ferhat Taşdemir
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Abstract

Due to advances in MEMS fabrication, Lab-on-Chip (LoC) technology gained great progress. LoC refers to small chips that might do similar works to equipped laboratory. Miniaturization of laboratory platform results in low area, low sample-consumption and less measurement time. Hence, LoC with IC integration finds numerous implementations in biomedical applications. Electrochemical biosensors are preferred for LoC applications because electrochemical biosensors can be easily integrated into IC designs due to electrode-based transducing. Capacitive biosensors are distinctive in electrochemical biosensors because of their reliability and sensitivity advantages. Therefore Interdigitated electrode (IDE) capacitor based biosensor system is preferred for development of biosensor platform.

In this thesis, capacitive biosensor system with new Capacitance to Voltage Converter(CVC) designs for LoC applications is presented. Multiple IDE capacitor sensing and varactor-based compensation are new ideas that are presented in this thesis. Proposed system consists of five blocks; IDE Capacitor based tranducer, CVC, Low-Pass Filter, Linear LC-Tank Voltage Controlled Oscillator (VCO) and Class-E Power Amplifier (PA). System building blocks are designed and fabricated using IHP's 0.25 μm SiGe BiCMOS process because of its advantage at high frequency and post-process that IHP offers. Varactor tunable CVC design provides highly linear relationship between output voltage and capacitance change in sensing capacitor. Varactor is used in reference capacitor to compensate changes in sensing capacitor. Total chip area is 0.4 mm^2 including pads. 10 MHz operating frequency is achieved. Total power consumption changes between 441 μW and 1,037 mW depending on the sensor capacitance.

Biyosensör Uygulamaları İçin Kapasitans-Gerilim Dönüştürücü Tasarımı

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Özet

MEMS üretimindeki ilerlemelerle, Yonga-üzerine-Lab (LoC) teknolojisinde önemli gelişmeler yaşanmıştır. LoC; küçük bir yonga, bir laboratuar ile aynı işlevi yapabilecek olanağa sahip olması anlamına gelmektedir. Alan, numune ve zaman kazancı sağlamasından dolayı LoC teknolojisi biyolojik uygulamalarda önemli bir etkiye sahiptir. Bundan dolayı, tümleşik devreye entegre edilmiş LoC teknolojisi, biyomedikal uygulamalarda çok fazla kullanılmaktadır. Elektrokimyasal biyosensörler, elektrod bazlı dönüştürme yapmalarından dolayı IC entegrasyonu bakımından öne çıkmaktadır. Kapasitif biyosensörler de güvenilirlik ve hassaslık avantajlarından dolayı, elektrokimyasal biyosensörler içerisinde en göze çarpan tekniktir. Bundan dolayı içiçe geçmiş elektrod (IDE) kapasitör bazlı kapasitif biyonsensör sistemi tasarlanmıştır.

Bu tezde, LoC uygulamalarında kullanılmaya yönelik yeni kapasitans-gerilim dönüştürücü tasarımlarını içeren kapasitif biyosensor sistemi sunulmaktadır. Birden fazla IDE kapasitör ölçümü ve varaktör bazlı kompansasyon tekniği, bu tezde sunulan yeni düşüncelerdir. Önerilen sistem 5 bloktan oluşmaktadır: IDE kapasitör bazlı dönüştürücü, Kapasitans-Gerilim Dönüştürücü (CVC), Alçak Geçitli Süzgeç, Doğrusal LC-Tank Gerilim Kontrollü Salıngaç (VCO) ve Class-E Güç Yükselticisi (PA). Bu tezin ana konusu olmasından dolayı Varactor ile ayarlanabilen CVC tasarımı analiz edilecek ve tartışılacaktır. Sistem blokları IHP firmasının 0.25 μm SiGe BiCMOS prosesi kullanılarak tasarlanmış ve üretilmiştir. Bu teknolojinin kullanılmasındaki ana neden, yüksek çalışma frekansına olanak sağlaması ve üretim-sonrası prosesleri sağlayabiliyor olmalarıdır. Varaktör ile ayarlanabilen CVC tasarımı ile çıkış sinyali ve duyar kapasitöründeki değişim arasında yüksek doğrusallıkta bir ilişki elde edilmiştir. Bu blokta varaktör elemanı, referans kapasitörünün yerine, duyar kapasitöründeki değişimleri kalibre edebilmek için kullanılmıştır. Yonganın toplam alanı is 0.4 mm^2'dir. 10 MHz çalışma frekansına ulaşılmıştır. Duyar kapasitörüne bağlı olarak toplam güç tüketimi 441 μW ile 1,037 mW arasında değişmektedir.

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List of Abbreviations

BioVCO Lab-on-Chip Transmitter design project

BiCMOS Bipolar Complementary Metal-Oxide Semiconductor

CBCM Charge-based Capacitive Measurement Circuit

CMOS Complementary Metal-Oxide Semiconductor

CVC Capacitance to Voltage Converter

CPWC Capacitance to Pulse Width Converter

CRP Carbon-Reactive Protein

CVDs Cardiovascular Diseases

FEM Finite Element Modelling

FIB Forced Ion Beam Microscopy

IC Integrated Circuit

IDE Interdigitated Electrode

ISM-band Industrial, scientific anf medical radio frequency bands

LoC Lab-on-Chip

Op-Amp Operational Amplifier

PA Power Amplifier

PAE Power Added Efficiency

PM Phase Margin

SAM Self-Assembled Monolayer

SiGe Silicon Germanium

VCO Voltage Controlled Oscillator

VLSI Very Large Scale Integration

1 Introduction

This thesis presents Interdigitated Electrode (IDE) based integrated circuit (IC) in the form of capacitance to voltage converter (CVC) along with wireless signal transfer. Sensor platform will be initially measured for C-Reactive Protein (CRP) biomarker detection to diagnose cancer. Proposed biosensor system has flexibility to be extended to detection of various biomarkers that are specific to different diseases.

Biosensor is a device that is specific to biological particles and detects the existence of biological materials. Starting from 1900s, harmful conditions for human life has been detected by biosensor devices / tools. These developments started with using canaries in coal mines to detect the existance of carbon monoxide [1]. This basic solution has been extended to more technical solutions and different application areas in time. One of these extended application areas has been early diagnosis and detection of diseases to increase the health conditions of human. Most commonly researched diseases are diabetes that has been crucial disease for more than 2-3 decades and cardiovascular diseases(CVD) that is a threat for human health in recent years.

In biosensor world, most popular research area has been detecting the glucose concentration in human blood [2, 3]. There have been successful studies concerning blood-glucose measurement and development of commercially available devices named as glucose-meter [4]. These successful results triggered other studies and biosensor researches have been extended to much wider fields.

Biosensors are used for detection and diagnosis of diseases specifically CVD since early detection covers important part of human health care systems. With early diagnosis, many lives can be saved. Most commonly used technique to detect the disease is capturing the biomarker that is specific to particular disease. For instance CVDs that has been the most fatal diseases for humanity can be detected by a biomarker. As World Health Organization (WHO) 2011 statistics show, CVDs are the number one cause of death globally. In 2004 17.1 million people that corresponds to %29 of global deaths resulted from CVDs and it is expected to rise to 23.6 million by 2030 [5]. CVDs have different biomarkers for different stages but most commonly used one is CRP that has been used for detection of CVDs at acute stage [6]. In order to detect the level of CRP in patient's blood, bioreceptor that is specific to

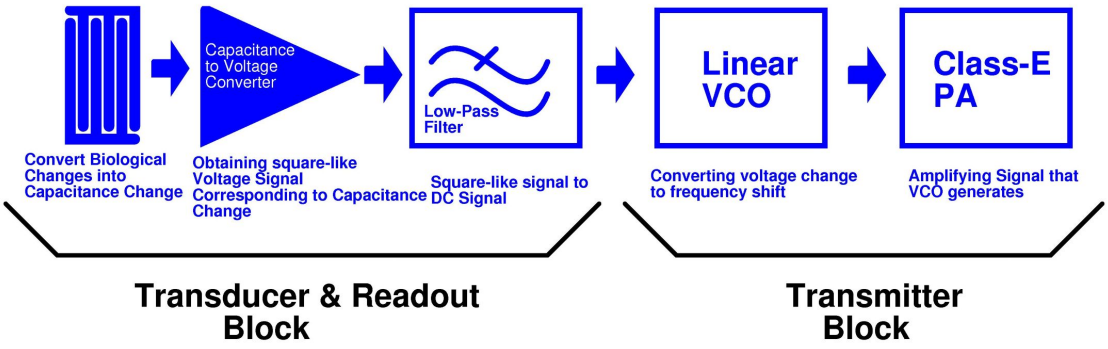


Figure 1: Proposed biosensor system diagram

CRP is used [7]. This bioreceptor can be aptamer, antibody or other protein-based detection materials depending on the sensor specifications.

As block diagram in Figure 1 indicates, biosensor system consists of IDE capacitor, CVC, Low-Pass Filter, VCO and PA blocks. CRP biomarker that is specific to cancer will be immobilized on IDE capacitors and biological change will be observed after addition of antigen. This change is converted to electrical signal via CVC block and signal will be transmitted to host device by transmitter block.

1.1 Biosensor Basics

Biosensors have significant effect on detection and diagnosis of diseases. Currently, clinical diagnosis is provided by centralized laboratories. These laboratories are costly and time-consuming since tests take long time and measurement tools are very expensive. Recently, emerging of Lab-on-Chip(LoC) technology will be possible solution for this problem [8]. With these new technologies better performance in terms of sample & time consumption and cost will be acquired. Performance of biosensor can be questioned considering numerous specifications. Some of these specifications can be listed as follows;

- **Sensitivity:** Sensitivity is defined as the change in output signal with respect to change in the amount of biological sample. Sensitivity is often expressed as output signal per physical or chemical change. Basically the sensor and bio-sample interface has great impact on the sensitivity of the system.

- **Selectivity:** Each biosensor has a specific target material. In addition to

these particles, there are some unwanted particle in bio-sample. Selectivity is a parameter that is the ability of biosensor to distinguish the difference between target and unwanted particles. Selectivity of biosensor is determined by surface activation or enzyme selection.

- **Resolution:** Resolution is minimum detectable change in sample (i.e. mass). System noise has a great impact on resolution of the biosensor system. Minimum detectable signal level is determined by noise level. (Signal-to-noise ratio should be greater than 1).

- **Response Time:** Time that is necessary to have 95% of result. This will determine which data is correct and which data is not. If response time is too high, initial response will not be considered. Also low response time is desired to observe the instantaneous changes.

- **Accuracy:** For testing the accuracy of system, produced platform will be compared to a reliable product.

- **Life-Time:** Biosensor systems will not give reliable results forever. After numbers of cycles, the reliability of the system will be suffered. Additionally, if biosensor is used for in-vivo applications, life-time specification will get more importance.

- **Dynamic Range:** Measurement range that biosensor system covers. This parameter will give the possible smallest and largest concentrations that can be measured with target biosensor system.

- **Ease of Usage:** User-friendly-interface is a desired property of biosensor systems. In commercial applications, ease of usage has a great impact on success of biosensor. Because the users will not have same background as the designer and user may not be even an engineer.

- **Ease of Calibration:** For the first measurement and further measurements, the system should be calibrated. For instance, there will be bio-sample deposition even if surface cleaning processes are applied, effects of these remaining particles has to be neglected. Therefore there should be a calibration mechanism if one biosensor will be used multiple-measurements [9, 10].

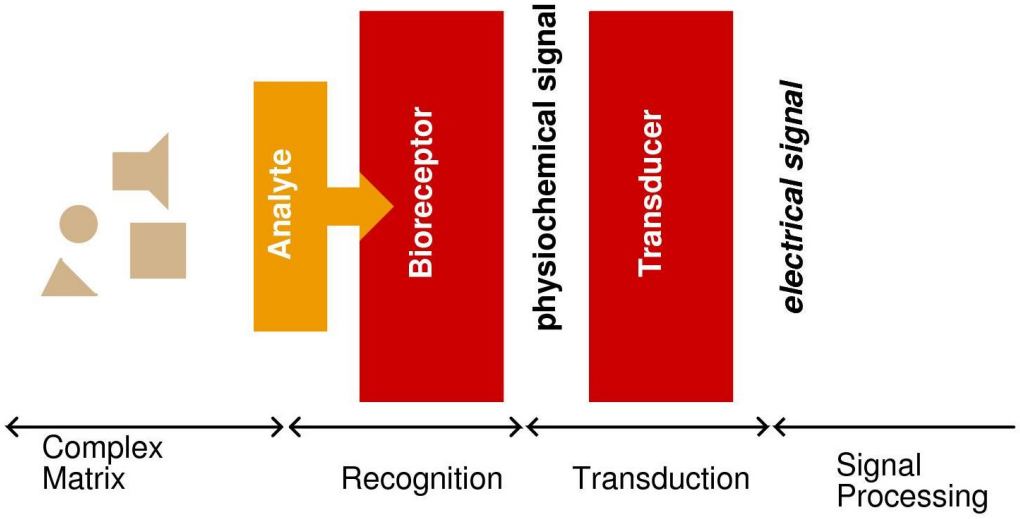


Figure 2: Working Flow of Biosensors

As shown in Figure 2, all biosensors have specific sensing mechanisms that are composed of multiple steps. Initially there will be complex matrix that is composed of different analytes. These analytes are not same, desired analytes should be selected from this complex matrix by bioreceptor. During this process, analyte will bind to probes that are specific to desired analyte and eliminate unwanted particles. As a result of this binding process, physiochemical signal is generated. With the help of transducer element, obtained physiochemical signal is transformed to electrical that can be further processed. Generated electrical signal may be processed to obtain quantitative data [11].

1.2 Types of Biosensors

Depending on the differences in working flow mechanism, which is explained in Chapter 1.1, biosensors are divided into several groups. Receptor and transducer based classifications can be counted as examples for different assortment techniques. In literature, transducer type is the most commonly used biosensor classification criteria. [12].

As explained in Section 1.1, biosensors have common process steps for sensing the analyte. Depending on the differences on these steps, biosensors are classified as in Figure 3. First of all classifications can be made depending on the receptor

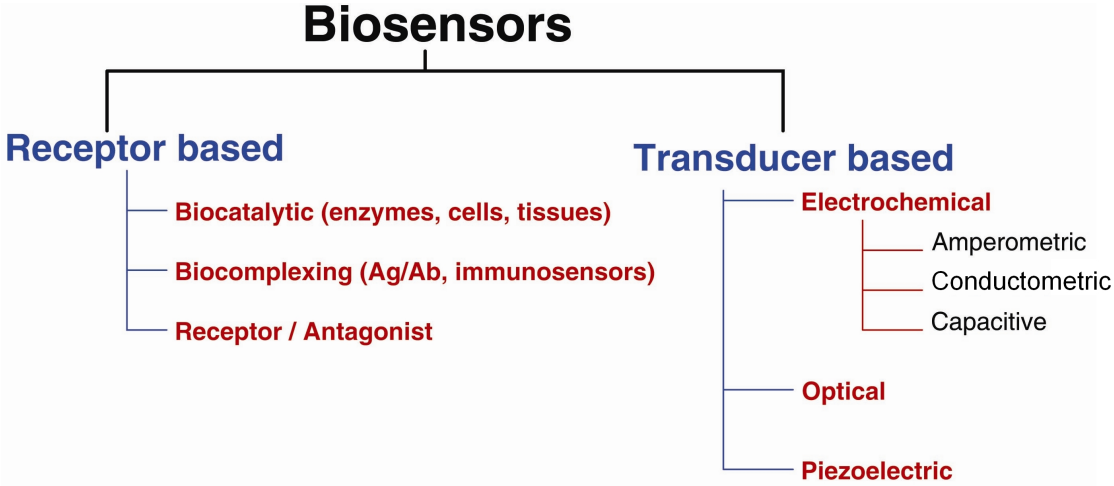


Figure 3: Classification of Biosensors

type. Depending on the receptor type, biosensors are classified as biocalatytic, biocomplexing and receptor based biosensors. Additionally, another classification is made depending on the transducing technique. Moreover, there are three commonly used options for transducer: electrochemical, optical and piezoelectrical transducer.

Different biosensor technologies have been researched ranging from piezoelectric material-based biosensors to micro-cantilever biosensors. Most commonly used ones are chemical and optical biosensors. Considerable advantage of optical biosensors or fluorescent labeled biosensor is their ability to label target molecules. With labeling, the target molecules can be easily detected by eye as well. For quantitative analysis, optical measurement set-up is used. The drawbacks of these optical sensing techniques are that they require bulky and expensive equipment for sample preparation and measurement [13]. These drawbacks make them non-compatible to LoC device for point-of-care applications. On the other hand electrochemical biosensors can be easily integrated to IC and they can be used in LoC applications because of electrode-based structures. Due to these reasons, electrochemical biosensors are best choice for LoC applications. Therefore electrochemical transducer based biosensors that can be listed as amperometric, conductometric and capacitive biosensors will be explained briefly.

1.2.1 Amperometric Biosensors

Amperometric biosensors have electrode-based transducer structures. Working principle of these designs is integrating the current that passes through one electrode. Frequently, three electrodes are used for measurements. One of the electrodes is working electrode (WE) that is used for measuring the current. The surface of the WE is chemically-activated, binding process occurs at WE surface. Second electrode is counter electrode (CE) which is used as a voltage source to the system. Third electrode is reference electrode (RE) that enables stabilizing voltage difference between CE and WE.

As shown in schematic of commonly used amperometric readout circuit in Figure 4, potential at RE is compared with V_{src} voltage then potential at CE is generated. With the V_{src} voltage and feedback between CE and RE, potential difference between

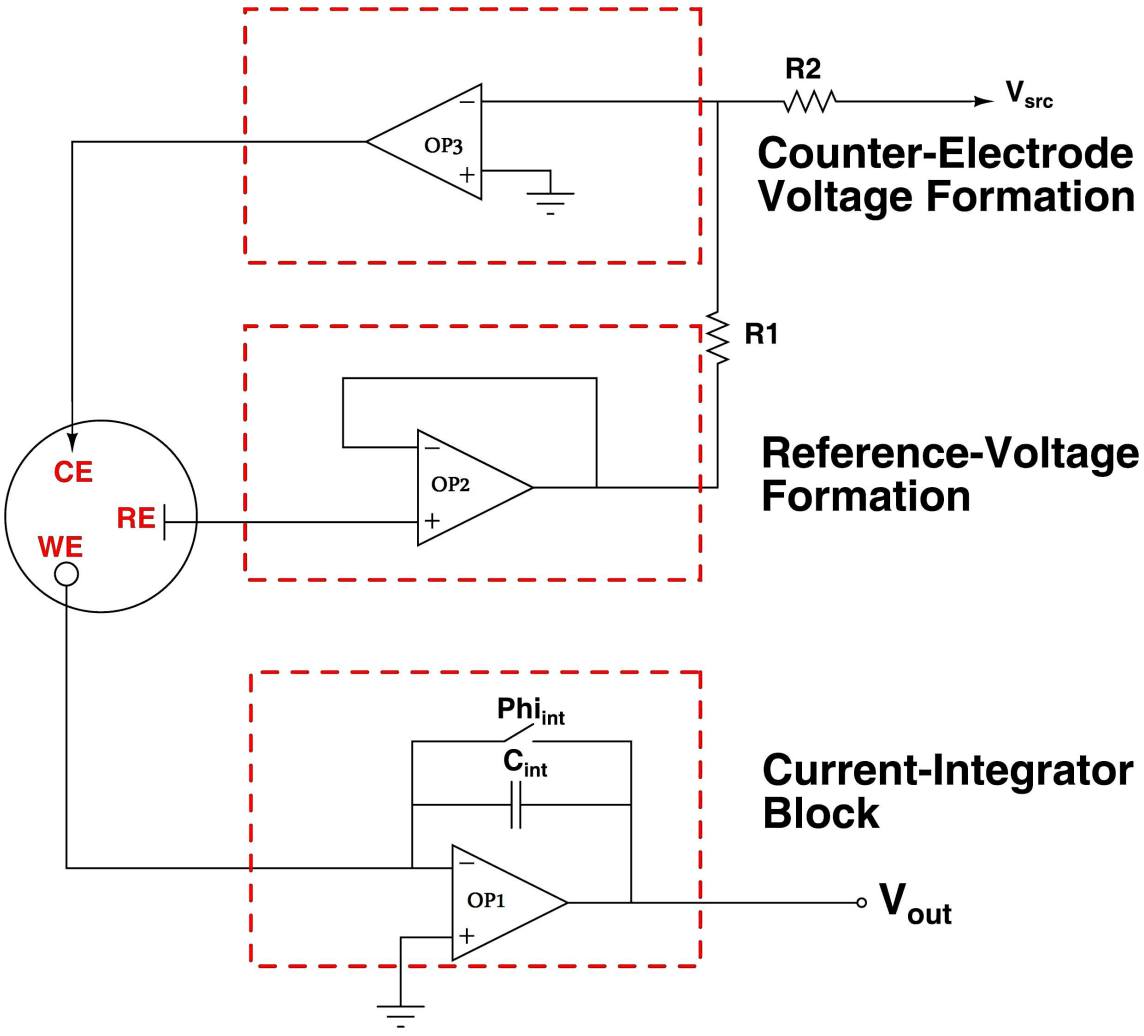


Figure 4: Schematic of Commonly used Amperometric Biosensor Readout Circuit

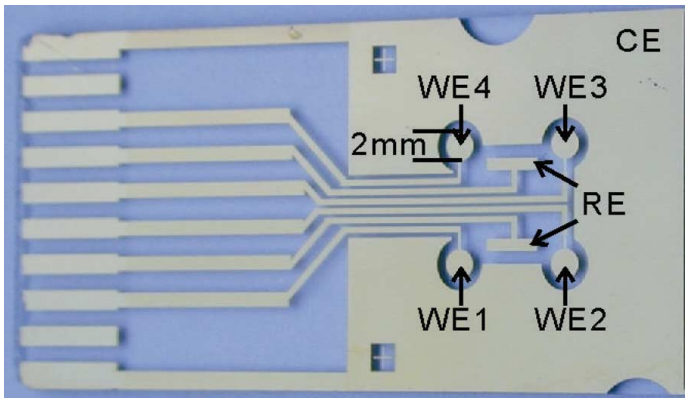


Figure 5: Amperometric Sensor Platform with 4 Working Electrodes

CE and WE can be kept constant. The voltage at WE will be ground because non-inverting input of OP1 is grounded. Generated current is integrated through C_{int} capacitor and integrating is controlled with Phi_{int}. Resulting from this integration, different voltage levels can be obtained at the output depending on the amount of binding on WE that is determined by the concentration of target solution [14].

Amperometric biosensors can be integrated into IC designs and used as a sensor array. One of the recent researches that was done by Michigan State University, [15] three electrode sensing system has been utilized and there are 4 working electrodes. Additionally, amperometric biosensor was integrated into standard IC process with additional post-process steps. Design of electrodes that forms transducer block is shown in Figure 5.

1.2.2 Conductometric Biosensors

Conductometric biosensors use electrode based measurement structures as amperometric biosensors. As a result of enzymatic reactions, changes occur in conductance of intermediate medium. This conductance change will be measured by conductometric biosensors [16, 17].

Compared to amperometric biosensors, conductometric biosensors do not require third electrode as in amperometric biosensors. As explained in chapter 1.2.1 ,for proper operation of amperometric biosensor WE, RE and CE are required whereas in conductometric biosensors two electrodes will be enough for measurement [18].

Since conductometric biosensors use enzymes for selecting target particles, consumption of target materials occurs [19].

1.2.3 Capacitive Biosensors

Capacitive sensors have high application areas ranging from cars' engine to smart-phones. In cars, engine oils become unusable after a while because of the mixture of acid and water therefore the oil should be changed periodically. Coil-type capacitive sensors used in cars to decide when oil should be changed [20]. On the other hand, capacitive sensors are used in today's smart phones to sense where user touches. Apart from these usage, capacitive sensors find numerous usage in biosensor technology as a result of existence and improvements in MEMS technology. Owing to micro and nano-size target bio-particles, miniaturization in sensor platforms has taken attention of researchers in capacitive biosensors. Capacitive biosensors are chosen in researches because of their advantages such as reliability and sensitivity over conventional techniques. As stated in [21], capacitive biosensors are ultrasensitive compared to other sensor technologies because of their ability to sense a few electrons.

Capacitive biosensors have advantages over other designs in different ways. For instance, there are products that enable continuous blood glucose monitoring use capacitive transducer based biosensor technique. These devices continuously measures the glucose concentration in blood. Even though they are very common, there are some problematic issues with these devices, such as damages on electrodes because of continuous usage. Also the technique used in these systems consumes glucose therefore after a while glucose concentration may change the equilibrium glucose concentration. Additionally, the glucose consumption is diffusion limited, any problem in diffusion may cause fluctuations in glucose concentration. Hence reliability of these devices may be questioned after using some time. Therefore they have to be recalibrated after some pre-determined period [9, 10]. To solve these problems, new techniques that do not consume glucose are utilized. Capacitive biosensors do not affect the glucose in human body, therefore they will not harm human body. With improvements in MEMS technology researches on capacitive biosensors increased rapidly for continuous glucose detection [22].

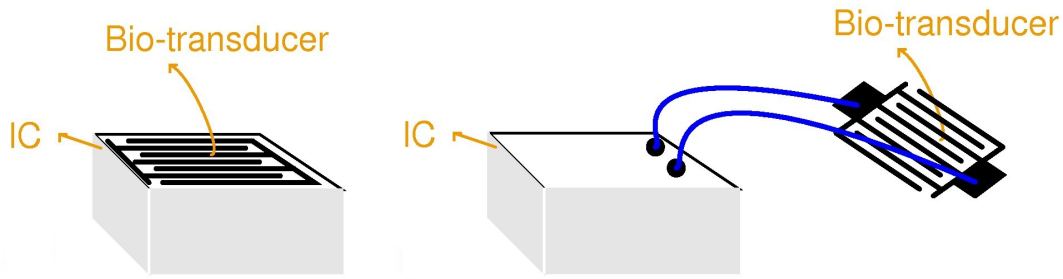
In addition to reliability advantage of capacitive biosensors, these biosensors provide high sensitivity. Even small change of biological change can be detected by biosensor. In one of the recent researches that was done by University of Bologna,

IC-integrated capacitive biosensor was developed. In that study, sub-fF capacitance change was successfully measured [23]. This work and similar works show that, high sensitivity can be obtained from capacitive biosensors.

Electrochemical biosensors can be integrated into IC technology easily compared to other biosensor technologies. Amperometric, conductometric and capacitive biosensors are leading electrochemical sensors. Capacitive biosensors are prominent technology compared to other electrochemical sensing techniques because of sensitivity and reliability advantages. Due to these advantages, capacitive biosensor technology has been chosen as a transducer technique for proposed system.

1.3 IC integrated Biosensor Designs

With the developments in fabrication technology, biosensor systems have been integrated into IC designs. Jang discussed the biosensor integration into CMOS process in his study. He states that advantages of CMOS over other processes such as MEMS are unmatched yield, cost-efficiency and integration capabilities of CMOS process. Also CMOS is commonly used and it is flexible in term of designing. Transduced biological signal can be easily processed by CMOS design [24]. CMOS design does not differ too much from other IC designs in terms of process flow. Therefore these advantages can be generalized for IC technologies such as SiGe BiCMOS process (except from cost-efficiency). Electrochemical biosensors require electrodes for transducing biological signal for electrochemical sensing. As explained in chapter 1.2, amperometric biosensors use three electrodes for measurement whereas capacitive and conductometric biosensors require two electrodes for sensing. As Figure 6 shows, sensing electrodes can be on-chip or bonded to readout chip.



(a) (b)

Figure 6: a) On-chip b) Bonded biosensor transducer and IC readout circuit connections

1.3.1 Bonded Biosensors

CMOS process has great advantage in integrating biosensor transducer with readout circuit but it has limitations in terms of available metal materials. Most commonly-used metals are Aluminum and Copper in standard IC process. Changing this materials or adding other materials are not desirable options for IC foundries. First of all changing metal layer will be costly, full process flow should be rebuilt and design parameters should be recalculated. Additionally, adding new metal material to standard process will result in contamination in devices. Hence each metal process should have dedicated devices for fabrication. Furthermore aluminum is cheap metal compared to Gold and other metals. Changing metal will cause high metal cost. Aluminum may not be best metal for biomedical applications because of its metallic nature. Therefore it is better to use gold, platinum, titanium or Ag/AgCl electrodes for biosensor applications because of their bio-compatibility [24]. Therefore it requires post-processing steps to form electrodes on top of IC chip.

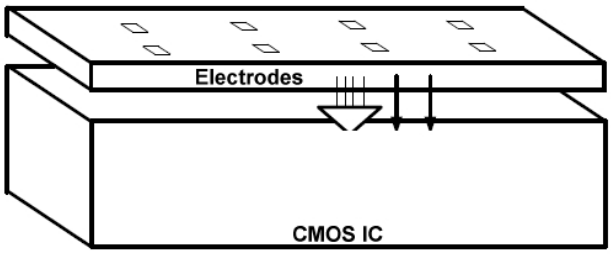


Figure 7: Schematic of developing electrodes on IC chip

These types of biosensors require post-processes or bonding for IC connection [25, 26, 27]. Chips are fabricated using standard CMOS process and electrodes are bonded through pads on chip. As Figure 7 shows, electrodes are formed on IC chip and there are openings for biosample. Also these kind of designs are advantageous for microfluidics formation since electrodes and microfluidics can be fabricated in parallel and using same fabrication process. There is no need to try to design microfluidics that is compatible to IC chip.

1.3.2 On-Chip Biosensors

The main difference between bonded biosensors and on-chip biosensors is options in metal materials that can be used [28]. As mentioned, bonded biosensors can use

additional metal apart from aluminum or copper that are used for forming top-metal of CMOS process. On the other hand, on-chip biosensors use top-metal of standard CMOS process. Integration of transducer and readout chip on same platform will reduce the noise which will increase the sensitivity of platform. If IC is used for a system, best way is to integrate whole system on same chip for noise reduction. This will increase the resolution of the system. Secondly, bonding transducer on IC chip requires extra processing steps. There should be expensive devices to pattern required metal layers.

Therefore there is a trade-off between bonding transducer on IC chip and on-chip system. Either much more importance will be given to bio-compatibility or higher resolution will be achieved with less expense. In Sabanci University's clean-room, minimum size that can be patterned is 20 μm which will not be good enough for bonding biosensor design. Additionally, cost will be high if foundry or other companies are paid to do post-process (gold-electrodes) for us. Therefore On-Chip biosensor development is best option for our biosensor system because of its low-noise and low-cost advantages.

1.4 Biosensor Readout Circuit

Capacitance of a design can be extracted with numerous techniques. Most basic techniques are based on utilizing measurement devices such as impedance analyzer, RLC-meter and network analyzer for capacitance analysis. Measurement principle of these devices are based on applying AC signal with pre-determined frequency and analyzing impedance data that results from applied AC signal. Additionally capacitance can be extracted using network-analyzer through s-parameter analysis. In previous researches and for current researches that are done by Sabanci University Biosensor Research Group, these device based capacitance extraction methodologies have been utilized. Apart from these, IC-based readout circuits are studied by researchers to ensure Lab-on-Chip principle. Capacitance-to-pulse converter and capacitance-to-voltage converter are known topologies for analyzing capacitances and further processing of capacitance data.

One of these techniques is capacitance to pulse width converter (CPWC). In some researches that apply CPWC for capacitance sensing, Schmitt Trigger is used. As

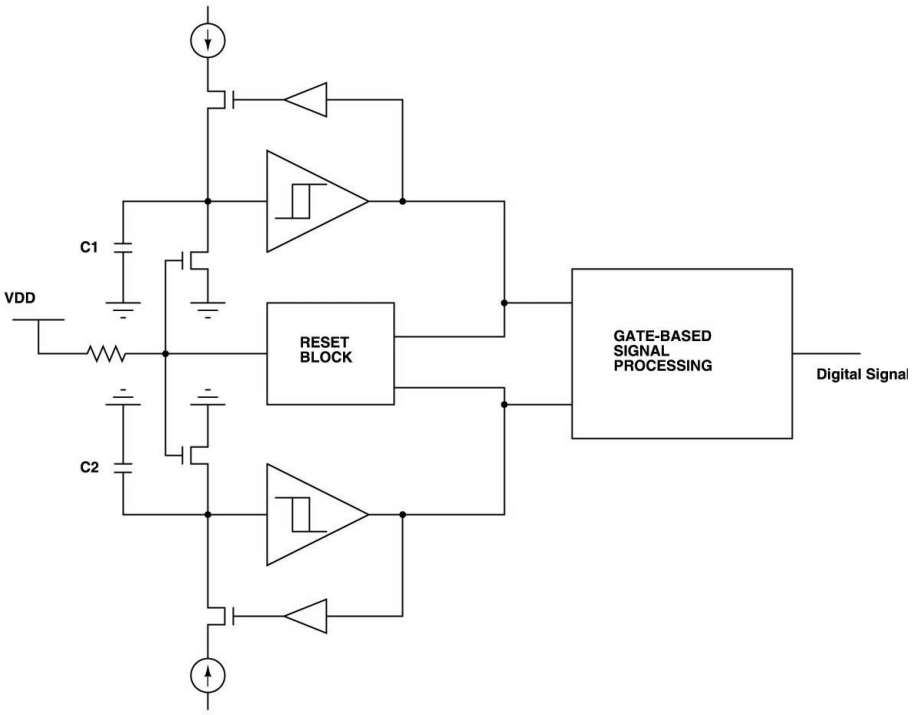
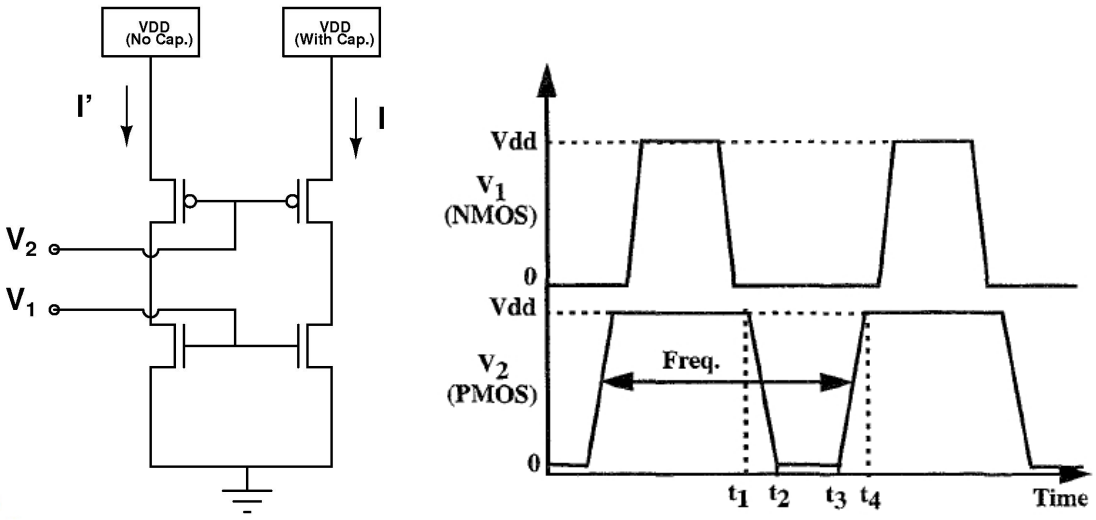


Figure 8: Schematic of Capacitance to Pulse Width converter design for capacitive sensing applications

block diagram in Figure 8 shows, this circuit also requires time-to-digital converter for further signal processing. Differential measurements are done in this technique. Capacitors are charged with current supplied from current source. This charge integration causes a linear increase of the potential on capacitor. This node is connected to input of the Schmitt Trigger. As voltage on capacitor increases up to upper-trigger-point, output of Schmitt Trigger will be high. With a feedback mechanism, when output is high, current source is blocked. Therefore capacitor will be discharged until voltage on capacitor decreases to lower-trigger-point. As a result of having differential measurement, there will be time difference between two output voltages. This difference is analyzed with gate-based circuit and digitized output signal is obtained [29]. Main problem of this design is mismatch problem. Mismatch between Schmitt Triggers may cause high variations at the output which decreases the sensitivity of sensor. If high sensitivity is desired, other options should be considered. As measurement results of this design show, 0.2 pF sensitivity was obtained from 3 pF capacitor. Sensitivity of these converter circuit is lower even though power consumption is apparently lower than other techniques [30] .

Second technique that is used for capacitance readout circuits is capacitance-to-

voltage converter. Different topologies have been implemented to read capacitance change as voltage change. There are some techniques that utilizes operational amplifiers as readout block [31, 32]. Apart from Op-Amp based CVC designs, there are some designs that utilize CMOS switches for capacitive reading. These designs are also known as Charge-based Capacitive Measurement Circuit (CBCM). This capacitance reading circuit can provide high resolution. Starting point for CBCM design is given in Figure 9 where current difference is measured using DC current meter. Main aim of that design was to extract the interconnect capacitance using CBCM design topology [33].



(a) (b)

Figure 9: a) Schematic of CBCM that was designed by Chen b) Applied signals to designed CBCM

This design has been improved to be used in capacitive sensor application rather than interconnect capacitances. As schematic draw in Figure 10 shows, single-end CBCM design [34] was developed for capacitive sensor applications. Current on sensing capacitor will be integrated via C_{int} and output voltage will be generated.

Table 1: Comparison of Capacitive Biosensor Readout Circuits

	Conv. Type	Capacitance Range	Sensitivity	Area mm^2	Power Cons. mW	Technology
[29]	CPWC	-	0.2pF/g	7.84	0.47	0.35μm
[30]	CPWC	16-256fF	16fF	0.53	0.084	0.32μm
[35]	CVC	0.1-1.64 pF 120-380 pF	20 fF 10 pF	-	0.939	0.13μm
[36]	CVC	-	10 pF	1	0.7	0.18μm

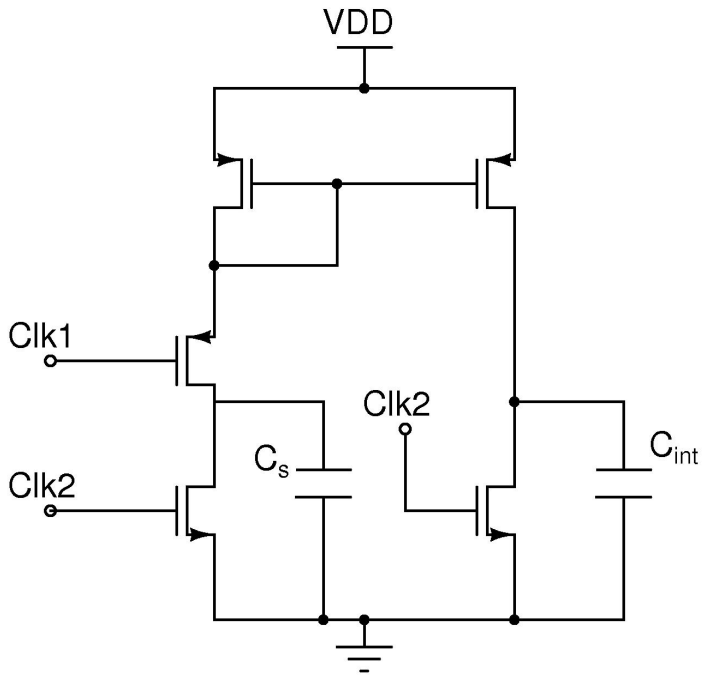


Figure 10: Modified CBCM Schematic Design

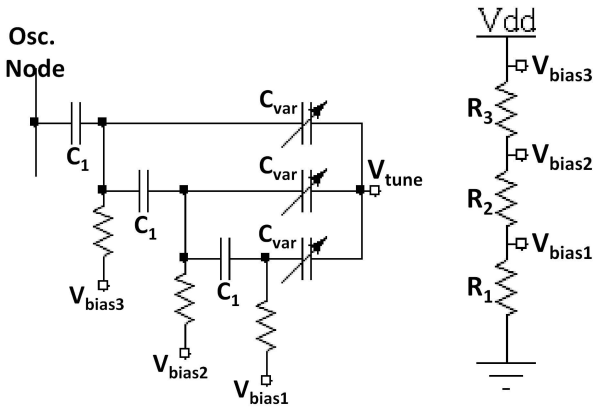
1.5 Transmitter Design

Transmitter block is used to send signal via wireless transmission to stable devices for further signal processing. To transmit signal, VCO and PA combinations can be used. In this project important concerns are linearity of response and low power consumption. For these purposes, VCO and PA literature review is given below.

1.5.1 Voltage Controlled Oscillator Design

Main concern of VCO design in proposed system is linearity. Linearity is defined as relationship between frequency of output signal and voltage that is applied to varactor. Linearity of this design will enable us to analyze frequency data that is obtained. For this aim LC-tank VCO is chosen as VCO topology and linearization techniques are applied.

VCO is a design that provides sinusoidal signal at a certain frequency. Active devices are used in oscillator designs because of lower cost and minimized noise. There are two types of VCO designs, waveform and resonant VCOs. Ring oscillator and relaxation oscillators are waveform VCOs [37, 38]. Since relaxation oscillators have bad phase noise behavior, they are not commonly used. On the other hand, crystal and LC tank oscillators are resonant VCOs. Even though Ring oscillators



(a) (b)

Figure 11: a) Varactor Tank for Linearization b) Bias Circuit for Varactor Tank

are easier to integrate into VLSI designs, LC tank VCO is chosen for our design. Because LC tank VCO has better noise performance compared to ring oscillator.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

In order to analyze the transmitted data easily, linearity of VCO is main concern for this project. Oscillation frequency of LC tank VCO is determined by varactor and inductors that are used in LC-tank. Frequency tuning is done by tuning varactor control voltage. In Equation 1, the oscillation frequency of LC-tank VCO is inversely related to square root of varactor capacitance. Therefore improvements should be applied to LC-tank for obtaning linear frequency response with respect to corresponding tuning voltage change. Commonly applied linearization techniques use varactor bank which includes varactors with different bias voltages as in Figure 11 for forming LC-tank [39].

1.5.2 Power Amplifier Design

Another block for transmitter stage is PA that is used to amplify the signal which VCO generates. According to specifications and priorities, different PA classes are used in designs. Conventional PAs have schematic design as in Figure 12 that includes matching circuits and transistor. There are different classes of PAs depending on gate biasing of transistors. Figure 13 indicates PA classes via I_D vs. V_{GS} graph. In this design, main concern is efficiency because battery will be used as voltage

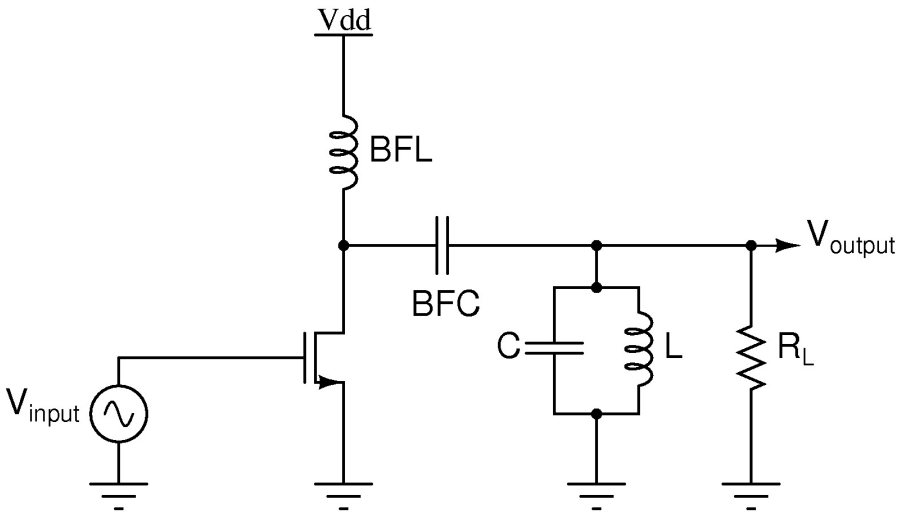


Figure 12: Schematic of Power Amplifier Designs

supply.

Power amplifier classes and their significant properties are listed below:

- **Class-A PA:** Phase difference between current and voltage is 180° therefore power consumption is higher compared to other classes. This results in lowest efficiency. Efficiency of Class-A PA is lower than 50%. This class amplifiers are chosen for high output power designs.

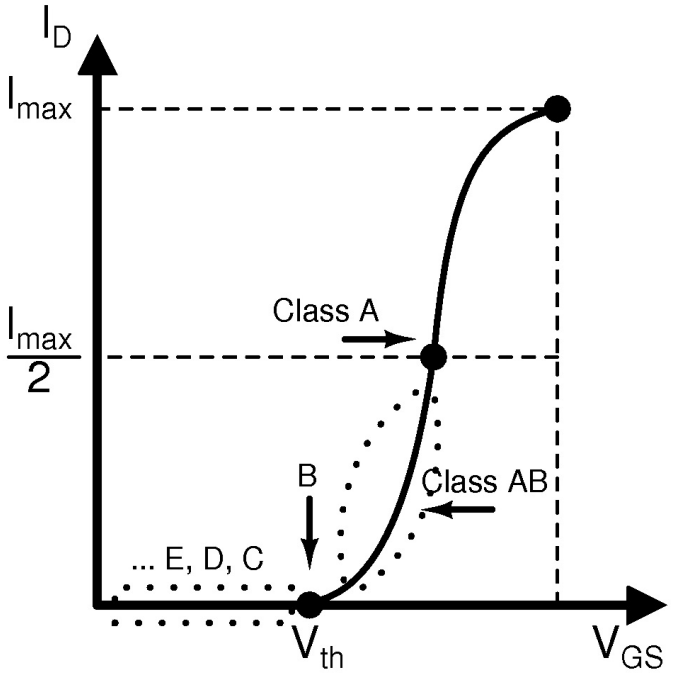


Figure 13: Power Amplifier Classes depending on gate biasing

- **Class-B PA:**Power Amplifier will not be always active in these PA classes. In half of the cycle, power amplifier will be active. This decreases the linearity of amplifier whereas efficiency will be increased compared to Class-A PA. Maximum achievable efficiency is 87.5% for these class of amplifiers.

- **Class-AB PA:** This amplifier class is combination of Class-A and Class-B. Power Amplifier is open between 50% and 100% of the cycle. Efficiency will be between Class-A and Class-B. This class is chosen when high output power and high efficiency is desired. Output power will not be as high as Class-A and efficiency will not be as good as Class-B.

- **Class-C PA:** Class-C PAs will be open for a small portion of period. Efficiency can approach 100% and output power is smaller compared to ClassA,B and AB.

- **Class-D PA:**Class-D and Class-E are switching PAs. They will have two operation modes either no voltage across the transistor or no current over transistor. In class D PA, current is sinusoidal and voltage is square shaped.

- **Class-E PA:** Difference of Clas-E PA from Class-D PA is signal shapes. In Class-E, voltage is in sinusoidal form whereas current is in square form. Advantage of Class-E PA is easiness in designing because while designing Class-D PA, it is assumed that output capacitance is 0.

As a result, Class-E PA was chosen for biosensor platform. Main specification of proposed biosensor platform is low power because we are aiming at development of hand-held device which will be supplied by batteries. Also most power-consuming block in this system is PA [40, 41]. Therefore power consumption is main concern and high output power is less significant specification.

1.6 Previous Completed Projects

As Sabanci University Biosensor Research Group, we have successfully completed projects on affinity-based electrochemical capacitive biosensor development. One of these works includes design and fabrication of stand-alone IDCs. These capacitors are measured through s-parameter analysis with probe station. Another work

is based on design of VCO that uses Interdigitated Electrode (IDE) capacitor as varactor.

1.6.1 Stand-Alone IDE Capacitor based Projects

The starting point of the project that is discussed in this thesis is Stand-Alone IDE capacitor based projects, because it forms a basis for further projects. Depending on the measurements obtained from these IDEs, new projects have been developed. Advantage of these IDEs is less fabrication time. Since the arrival time of IC chips is two/three months after the tape-out. Even though designed capacitors are not IC integrated capacitors, it will be advantageous to observe the results as soon as possible.

Designed and fabricated gold IDE capacitors that biomarkers are bound to are indicated in Figure 14. The binding process has multiple processes. Process starts with activation of gold IDE surface with antibody or aptamer that are specific to aimed biomarker. Then biomarker is bound to aptamer and electrical flow starts. In one of the recent researches, capacitive immunosensor is used for analyzing multiple biomarker. It is commonly known that C-Reactive Protein (CRP), TNFα and IL6

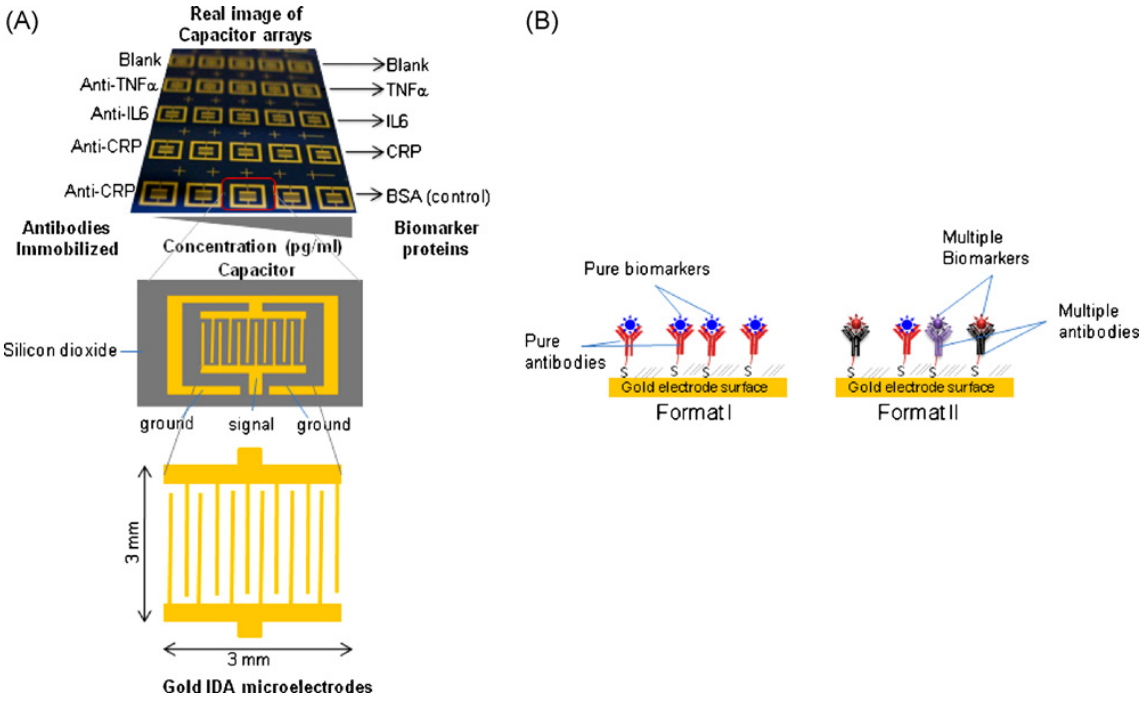


Figure 14: Gold IDE capacitors and visualization of antibodies and binding of biomarkers

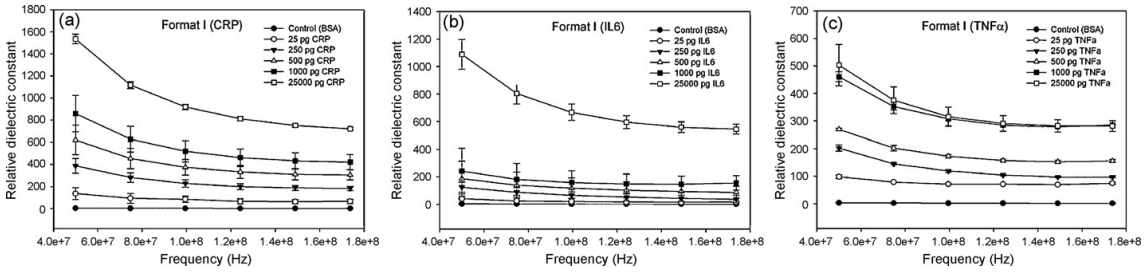


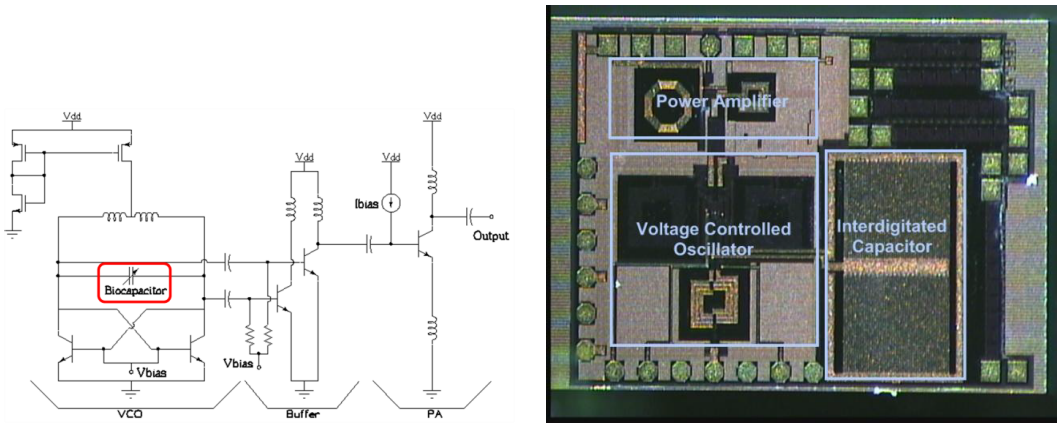
Figure 15: Measurement Results of IDE Capacitors with different biomarkers

are markers for indication of risks of CVDs [42].

The results of this project show the change of capacitance with respect to different biomarkers. Relative dielectric constant change results for different CVD biomarkers are given in Figure 15. Relative dielectric constant term does not correspond to electrical dielectric constant terms but biological term that has an effect on electrical dielectric constant. As it can be observed from the results, maximum relative dielectric constant change is obtained from CRP measurement. Standalone IDE capacitor platform enables multiple disease detection via IDE capacitor array. There are 8 IDE capacitors in an array that enable detection of different disease biomarkers concurrently.

1.6.2 A New Lab-on-Chip Transmitter for the Detection of Proteins Using RNA Aptamers

In this project, new RNA aptamer based affinity biosensor for sensing CRP was developed. System consists of IDE Capacitor, LC-tank Voltage Controlled Oscillator (VCO) and Power Amplifier (PA). Conventional LC-tank VCO designs use varactor that is controlled by external voltage. Changing the tuning voltage results in shift in output signal frequency through change in varactor capacitance. Compared to conventional LC-Tank VCO design, IDE capacitors are used as the varactor in this VCO. Capacitance of varactor changes with applied control voltage whereas the in this new design capacitance changes with CRP concentration of sample that is put on IDE capacitor. Power amplifier stage amplifies the signal that is generated by VCO. Capacitance change gave information about the CRP concentration of sample through frequency change. Aimed frequency band was ISM band, centered at 2.46 GHz. Schematic and layout of the design are given in Figure 16(a) and Figure



(a) (b)

Figure 16: a) Schematic b) Layout of the VCO design that uses IDCs as varactor

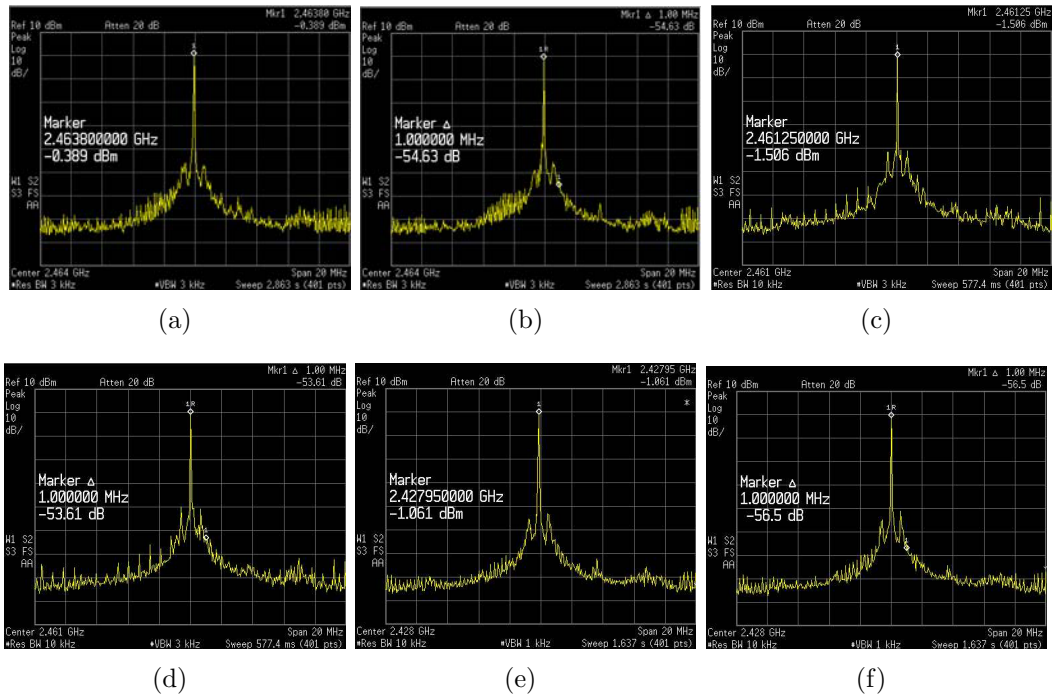
16(b). The chip was fabricated using 0.25μ SiGe BiCMOS technology of IHP from Germany.

There were some challenges in this project that resulted from integration of IDE capacitors into IC technology. For applying voltages to chip, wirebonds were used. Contacts of bonds on chip were broken because of the samples used in measurements. To prevent this problem, bonds were covered with non-conductive epoxy. This precaution improved the measurement conditions.

Binding of aptamer/antibody on metal surface requires less process and cleaning steps. As commonly known, in standard IC process, on top of chip there is a passivation layer that has few μm thickness. Hence, fabricated chip underwent postprocessing steps to remove or thin passivation layer.

Measurements are done using probe station and spectrum analyzer. Phase noise of the generated signal is between -114.3 dBc/Hz and -116.5 dBc/Hz for all measurements that are given in Figure 17(b), 17(d), 17(f). Oscillation frequency changed between 2.428 GHz and 2.469 GHz as Figure 17(a), 17(c), 17(e) shows. Capacitance change was extracted from the frequency of signal using the formula that is relating the capacitance change to frequency given in Equation 1 in chapter 1.5.1. It was designed that L (inductance) value is 1.6 nH that is the value of inductor used in design. Corresponding C (capacitance) value is sum of on-chip capacitor, parasitic capacitance and capacitance resulting from addition of bio-sample.

As the measurement results are given in Table 2, 500pg/ml CRP solution results in 77 fF capacitance change whereas after self-assembled monolayer (SAM) forma-



(a) (b) (c)

(d) (e) (f)

Figure 17: (a) Frequency Spectrum (b) Phase Noise of Blank Chip; (c) Frequency Spectrum (d) Phase Noise after immobilization of RNA aptamer on ICD; (e) Frequency Spectrum (f) Phase Noise after binding protein with using 500pg/ml CRP solution

tion almost no capacitance change is obtained. After SAM formation, capacitance change was not expected because this step was for surface activation without CRP binding, no electrical effect would be observed [43].

Standalone gold-electrode capacitors and IDE capacitor based VCO designs are motivations for this project. First step of our research was stand-alone capacitors that will help to prove that bio-samples can be sensed using this technique. Then IDE capacitors are integrated into VCO design to improve stand-alone capacitor by integrating into integrated circuit (IC) design while miniaturizing the capacitors. Next step is to improve the sensitivity of capacitors by designing new readout system that will have higher dynamic range. In addition to that, decreasing sens-

Table 2: Measurement Results of VCO that uses IDCs as Varactor

Measurement Condition	Osc. Freq. (GHz)	P_{out} (dBm)	Phase Noise (dBc / Hz)	Capacitance (pF)
Blank Chip	2.4648	-0.369	-114.3	2.603
After SAM	2.4613	-1.506	-113.6	2.608
After 500 pg/ml CRP Solution	2.4280	-1.061	-116.5	2.680

ing frequency will be another important aim because at high operating frequencies, protein-protein reaction will be more unpredictable.

1.7 Overview of this Thesis

The thesis has already introduced the biosensor basics, common parameters for biosensor design and IC intergrated biosensor works in literature. Additionally, biosensor types and readout circuits are discussed. Following chapters describe the development of biosensor plaftorm.

Chapter 2 will give information about the whole sensor system and IDE Capacitor & Readout Blocks. IDE Capacitors are used for capacitive transducing. IDE capacitor geometry optimization with simulations will be analyzed in this chapter. Also some measurement results of IDE capacitor will be given. Transduced signal will be analyzed by Capacitance to Voltage Converter block that helps to convert biological change that is obtained from IDE capacitor to voltage change. Three different CVC blocks are designed and these designs will be explained in detail. Voltage Buffer block will be used to obtain better response since higher capacitance can be driven. Buffer connected two-stage Op-Amp is used as buffer for driving high load capacitance. This buffer stage will be explained in this chapter as well.

Chapter 3 will describe the simulation and measurement results of the transmitter block. Main aim of this transmitter block is to send the signal generated by readout system to host device. For transmitter stage Linear LC-tank VCO that has linear output voltage with respect to varactor tuning voltage and Class-E Power Amplifier are used. Linearity of VCO is important concern because of easier data-analysis and high-efficiency is desired since proposed system will be in the form of hand-held device.

Chapter 4 will discuss the possible improvements that can be implemented to enhance the system. Integration of blocks and microfluidics for system are important issues that will be discussed.

2 Readout Circuit Blocks for IDE Capacitor

2.1 System Description

Proposed system is sub-block of a project that aims at development of a Lab-on-Chip (LoC) platform for point-of-care applications. This platform may enable laboratory measurements, that requires complex laboratory equipments, into non-laboratory settings. In addition to that, LoC platforms will decrease the sample consumption into micro-liter ranges. Signal transducing will be made through IDE capacitors. As diagram in Figure 18 shows, main project will have two signal processing options. Generated signal will be processed either on hand-held device or on PC for further analysis. Two parallel signal analysis might be available in this platform. First analysis will be based on on-board signal conditioning which will output preliminary data to LCD screen. In addition to that, the signal will be transmitted to distant device at a frequency band that cover ISM frequency band and received signal will be evaluated. System that is explained in this thesis is signal conditioning using wirelss data transmission. The system is composed of three blocks; IDE capacitor & Readout Block, Transmitter Block and Digital Signal Processing Unit. In proposed system, IDE capacitor & Readout Block and Transmitter Block are integrated, wireless signal processing is used. Digital Signal Processing unit will be developed and will be integrated into proposed system later. This work can be considered as an improved version of BioVCO design. Advantage of this design is operation at lower frequencies which will enable better opportunity for on-board

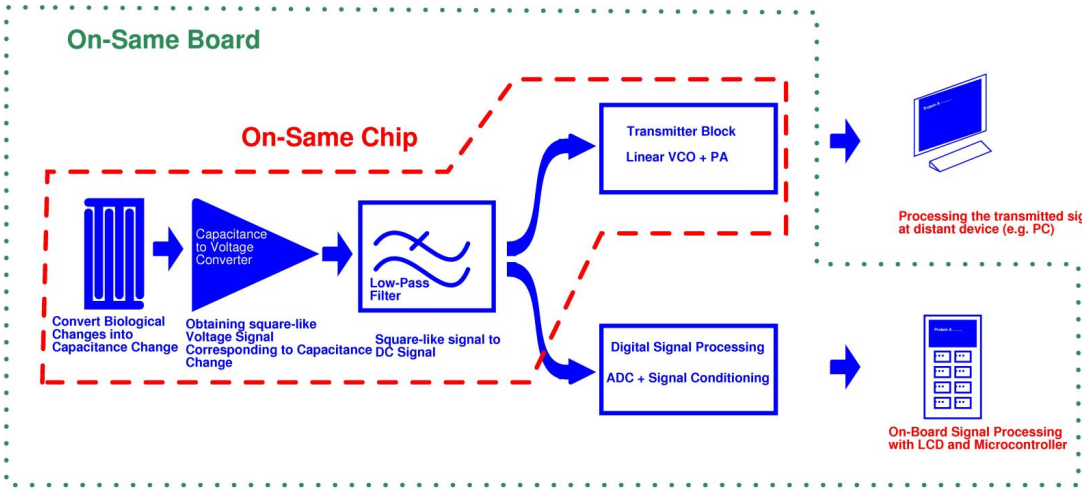


Figure 18: Project description that is aiming at two parallel signal processing

signal analysis and better analysis for protein-protein reactions. Additionally for capacitance analysis it would be better to choose lower frequencies in which imaginary part of impedance is dominated by capacitance.

The on-chip display may provide preliminary results because of source and area limitations of hand-held device. For deeper analysis, transmitting analog signal to PC can be used, real-time data might be obtained. Two working modes will help user to continuously analyze the data that is obtained from biological sample.

The working principle of the platform is as follows;

- Biological sample will be dropped on IDE-based capacitor that is activated. Target biomarkers in sample will be bound to IDE capacitor surface by bioreceptor that is specific to target disease. Then capacitor surface will be cleaned and unbound samples will be removed. Amount of binding will differ depending on the biomarker concentration of sample. This biochemical process will result in change in capacitance of IDE capacitor. Capacitance change will be different for different concentrations.

- Then this capacitance change will be converted into square-like signal whose upper voltage level depends on input capacitance. Duty cycle of signal is 80% for next step.

- Generated voltage signal will pass through low-pass filter to generate a DC signal with negligible fluctuations. High fluctuations will degrade the phase noise of transmitter block.

- Obtained DC voltage level is proportional to input capacitance. As explained at the beginning of this chapter, the signal will be processed with two parallel ways. Either signal can be analyzed on-board or can be transmitted to host device for detailed analysis. This detailed analysis may include obtaining graph that composed of real-time data or saving numerous data for comparison.

The platform will provide the detection and early diagnosis of disease. Primarily aimed diseases are CVDs and cancer. Futhermore, system might be extended to detection and early diagnosis of multiple diseases. Applicability for multiple diseases may result from the flexibility of the sensing platform. Changing the receptor to new

receptor that is specific to different biomarker will result in new biosensor platform that can sense other diseases apart from CVD and cancer.

For designing and fabricating the system blocks, IHP 0.25 μm SiGe BiCMOS technology is used. Main reason for utilizing SiGe BiCMOS process instead of CMOS process is ability to integrate all blocks into single chip. SiGe process advantages at higher frequency and system includes transmitter blocks that work between 2.29 and 2.72 GHz. In addition to that, there is a collaboration with IHP Microelectronics related to this project. As a result of high frequency and collaboration advantages, IHP SiGe BiCMOS process has been used. IDE capacitor & Readout Block and Transmitter Block are designed and fabricated using this technology. Results are given in following subtopics.

2.2 Interdigitated Electrode based Capacitors

2.2.1 Design of Interdigitated Electrode based Capacitors

For capacitive transducing, various techniques and geometries has been applied to sense the change in target sample. Interdigitated geometry has resolution and sensitivity advantage that results from increased surface area. As 3D visualization of IDE capacitors is shown in Figure 19, parameters of IDE capacitors can be listed as : Finger Thickness, Finger Length, Finger Width and Gap Between Fingers.

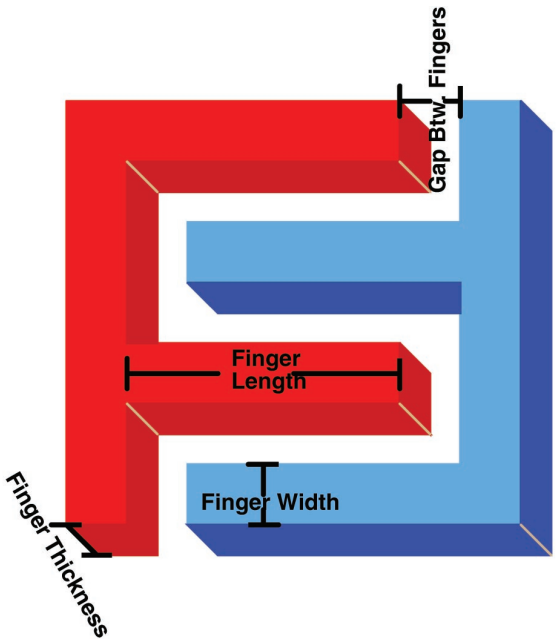


Figure 19: Visualization of IDE capacitors and its parameters

IDE-based capacitor structure has advantage over other geometries. Since the surface-to-biological material interface area is increased with this geometry assuming there is a constant capacitor area.

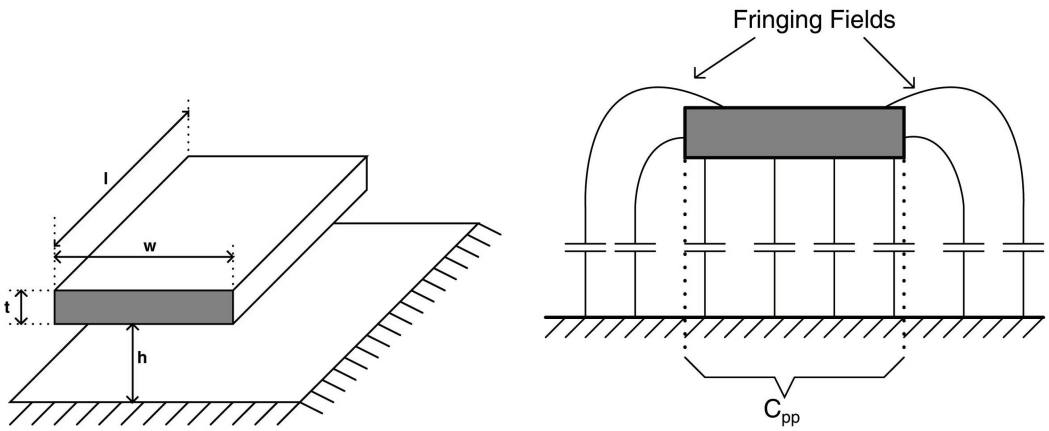
Commonly known capacitance type is parallel plate capacitance that is formulated as Equation 2 where ε is permittivity of dielectric between plates, A is area of plate, d is distance between plates.

$$C = \varepsilon \frac{A}{d} \tag{2}$$

In addition to parallel-plate capacitance, there is also a fringing capacitance that should be considered for capacitance analysis. Effect of fringing capacitor is analyzed by [44]. For the capacitor configuration in Figure 20, Equation 3 was given for fringing capacitance. As this equation imply, h which is Gap Between Fingers should be increased while keeping other parameters same.

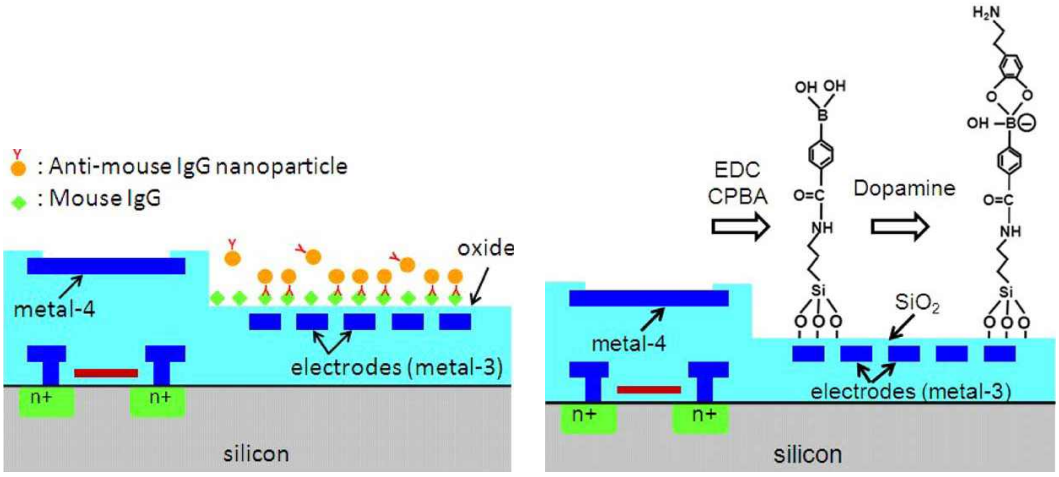
$$\begin{aligned} C &= \varepsilon \left[\frac{(w-\frac{t}{2})}{h} + \frac{2\pi}{\ln(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}(\frac{2h}{t}+2)})} \right] \qquad for\ w \geq \tfrac{t}{2} \\ C &= \varepsilon \left[\frac{w}{h} + \frac{\pi(1-0.0543*\frac{t}{2h})}{\ln(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}(\frac{2h}{t}+2)}} + 1.47 \right] \qquad for\ w \prec \tfrac{t}{2} \end{aligned} \tag{3}$$

There are some interesting studies that uses IDE capacitors as transducing element. In one of these researches the capacitors are designed in Metal3 of 2P4M 0.35 μm CMOS process. Advantage of Metal3 is its thickness since the thickness of



(a) (b)

Figure 20: a) Two parallel plates to form capacitor b) Parallel Plate and Fringing Capacitances between two plates



(a) (b)

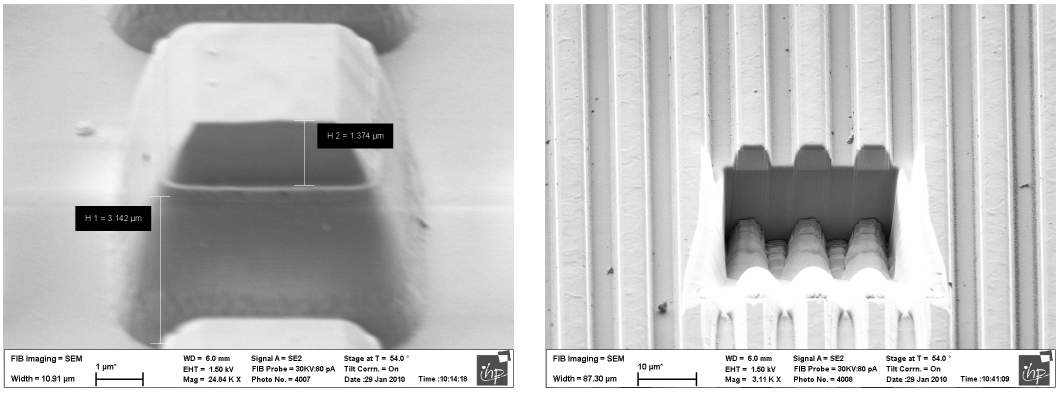
Figure 21: (a) Operation principle of Capacitive Immunosensor designed by Wang b) Operation of immunosensor with Neurotransmitter Dopamine

the metal is 0.65 μm. As equation implies, the thickness of metal layer is inversely proportional to the effect of fringing capacitor for constant width and length. IDE capacitors are implemented as in Figure 21 and resolution in aF range was achieved by [21]. This kind of capacitive biosensors are hard to implement unless there is an agreement between fabrication company and researchers. Since it is hard to thin the passivation layer up to Metal3 layer in 4M process. Similar collaboration is ongoing between Sabanci University and IHP Microelectronics. Stand-alone capacitors were designed using Metal3 of 1P5M BiCMOS process and will be produced using IHP's back-end process. It is expected to have much higher capacitance change from these capacitors. In another research that uses IDE capacitors 6M process has been used and passivation layer has been thinned to increase the sensitivity. Sub-fF resolution has been obtained according to their results [45]. These studies motivated us to start this project.

2.2.2 Simulation Results of Interdigitated Electrode based Capacitors

In addition to these simulations, IDE capacitors requires post-process steps to remove or thin the passivation layer. This thinning of passivation layer is done by IHP Microelectronics and FIB pictures of thinned structures are shown in Figure 22. Capacitors with Integrated Circuit were fabricated using standard BiCMOS process and post processing steps have been applied for higher sensitivity. As FIB images

taken by IHP Microelectronics visualizes, thinning process has been successfully done and will be improved for further fabrications.



(a) (b)

Figure 22: FIB images of IDE capacitors fabricated and thinned by IHP Microeelctronics

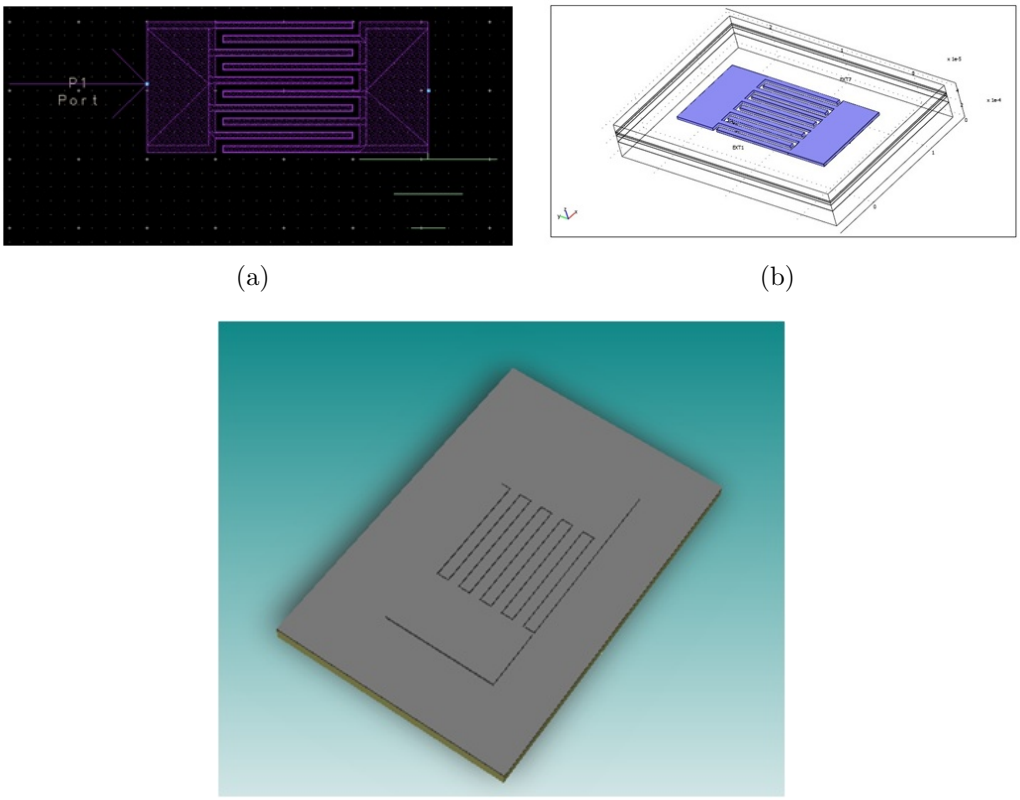
As explained in Chapter 2.1, IDE based capacitors are utilized as transducing element. For optimizing the geometry parameters of IDE capacitor, 3D electromagnetic simulations were done with 3 different tools; ADS, COMSOL and Coventorware with structures in Figure 23(a), 23(b) and 23(c) respectively.

2.2.3 Simulations with ADS

ADS Momentum tool was used for comparing the geometries and optimizing them. We had IHP's process files for ADS Momentum such as metal layers, dielectric layer parameters. Therefore it is advantageous to use IHP's parameters for simulation also ADS is preferred for electromagnetic analysis. For observing the effect of change in capacitance, simulation results with different dielectric constants has been made. Most important drawback of ADS Momentum for this analysis is that it is being considered as a 2.5D simulator [46]. Therefore other simulation tools were used for simulation as well.

2.2.4 Simulations with COMSOL

Another simulations were made using COMSOL Multiphysics FEM tool. Advantage of COMSOL is ability to run multiple analysis for the same structure at the same time. For instance, mechanical and electrical analysis can be run at the same time and interaction between these analysis can be controlled manually.



(a) (b)

(c)

Figure 23: Designed Geometries for Simulating IDE capacitors using a) ADS b) COMSOL c) Coventorware Finite Element Modelling Tool

Effect of fringing capacitance was simulated by COMSOL Finite Element Modelling (FEM) tool using IHP's metal thickness and IC structures. Figure 24 shows the utilized structure during simulations. In these simulations, medium between fingers was used as SiO_2 that has relative dielectric constant as 4.2. Free space relative dielectric constant was simulated from 1 to 5 and Table 3 is generated from these simulation data. Relative capacitance change with respect to $\varepsilon_{r,freespace}$=1 is

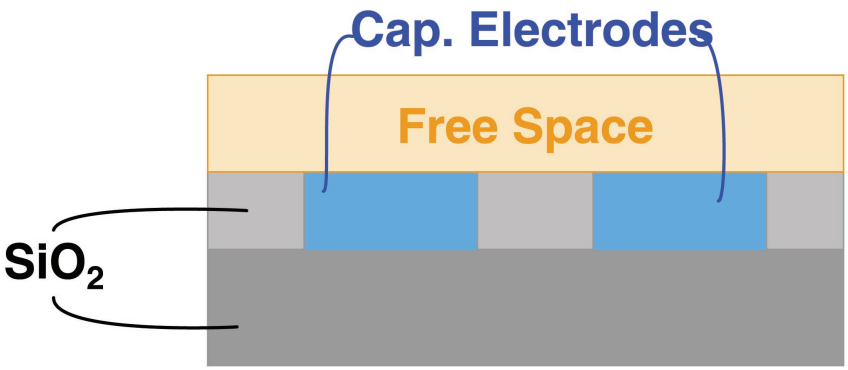


Figure 24: Capacitor structure that is used for simulating fringing capacitance using COMSOL FEM tool

also indicated in same table. In these simulations, area of IDE capacitors are kept same to provide equal conditions. Capacitance of IDE structures to substrate was not included. This will have an effect on sensitivity of capacitance.

Table 3: Fringing Capacitance Simulations Using COMSOL FEM Tool

	Cap. for $\varepsilon_{r,fs} = 1$	Cap. for $\varepsilon_{r,fs} = 2$	Cap. for $\varepsilon_{r,fs} = 5$	Relative Capacitance change per $\varepsilon_{freespace}$
W: 2.5μm G: 2.5μm	1.186 pF	1.237 pF	1.393 pF	4.36%
W: 2.5μm G: 5μm	461 fF	490 fF	573 fF	6.1%
W: 5μm G: 2.5μm	897 fF	950 fF	1.109 pF	5.9%
W: 5μm G: 5μm	353 fF	379 fF	456 fF	7.3%
W: 5μm G: 10μm	204 fF	229 fF	305 fF	12.4%
W: 10μm G: 5μm	294 fF	320 fF	400 fF	9%

These simulations shows the effect of fringing capacitance on IDE capacitor. In these simulations, effect of area capacitance was not included. Area of capacitor structures are 300 μm x 350 μm and area capacitance for Top Metal 2 is given as 13 aF/μm^2. Considering area capacitance of structures, 341 fF area capacitance will be obtained for W (finger width) = G (gap between fingers) structures, 227 fF for 2W=G structures and 455 fF for W=2G structures. Considering this effect, Table 3 can be improved to Table 4. From these results, two best geometry options that can be used in IDE design are W:2.5μm-G:5μm and W:5μm-G:10μm. It seems second option seems better to be used but disadvantage of this design is effect of parallel plate capacitance. Thickness of binded structures will be in the 100s nm range. Therefore lower gap is desired. It can be questioned if choosing W:5μm-G:2.5μm will not be better option for parallel plate measurements. Answer to this question will be negative because of fluidics effects. Fluid may not flow between fingers in that small gap and this may prevent binding of proteins to sidewalls. Additionally, W:5μm-G:10μm structure is more sensitive to environmental effects because of having lower capacitance value. Unwanted changes may occur because of small changes in environment. Due to these considerations, W:2.5μm-G:5μm geometry was chosen for IDE capacitor designs.

Table 4: Addition of Area Capacitance to Fringing Capacitance Simulations Using COMSOL FEM Tool

	Cap. for $\varepsilon_{r,fs} = 1$	Cap. for $\varepsilon_{r,fs} = 2$	Cap. for $\varepsilon_{r,fs} = 5$	Relative Capacitance change per $\varepsilon_{freespace}$
W: 2.5μm G: 2.5μm	1.527 pF	1.578 pF	1.734 pF	3.4%
W: 2.5μm G: 5μm	688 fF	717 fF	800 fF	4.1%
W: 5μm G: 2.5μm	1.352 pF	1.405 pF	1.564 pF	3.9%
W: 5μm G: 5μm	694 fF	720 fF	797 fF	3.7%
W: 5μm G: 10μm	431 fF	456 fF	532 fF	5.8%
W: 10μm G: 5μm	749 fF	775 fF	855 fF	3.5%

2.2.5 Simulations with Coventorware

Another simulation tool that is used for electromagnetic analysis is Coventorware. Advantage of Coventorware over others is process compatibility. Initially, design process is described and layers are formed. Then masks were designed to create IDE structures on top-metal layer. With Coventorware, IHP's standard back-end process can be implemented and thinning or removing passivation layer process can be implemented as well.

In addition to COMSOL simulations, simulations with Coventorware were done with real geometries. IHP's 0.25 μm process with 1P5M 2 Top Metal layers was generated. Main advantage of these simulations is simulation with thinning passi-

Figure 25: Capacitor structure that is used for simulating capacitance change of W:2.5μm-G:5μm structure using Coventorware FEM tool

vation layer that enhances the simulation results. For these simulations, structure in Figure 25 was designed. Thickness of passivation layer in IHP's 0.25 μm process is 1.9 μm, with post-process steps thickness was decreased to 1 μm.

For simulation using COMSOL, Air, BPSG, PDMS and SiO_2 were used as materials of sample. Graph in Figure 26 indicates the change of capacitance with changing the dielectric constant of sample.

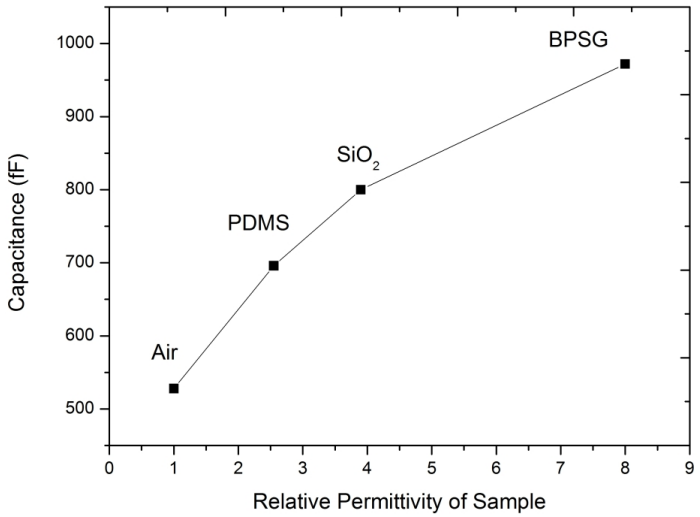


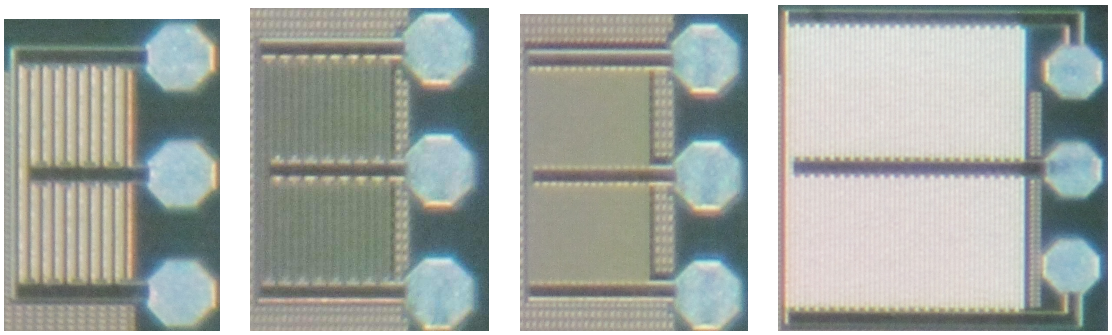
Figure 26: Change ocapacitance of IDE capacitor with changing relative dielectric constant of sample

2.2.6 Measurement Results of Interdigitated Electrode based Capacitors

In addition to these, stand-alone capacitors that were fabricated using IHP Microelectronic's standard CMOS process were measured. Fabricated capacitor structures are shown in Figure 27.

$$C = \frac{1}{Z_{im} 2\pi f} \tag{4}$$

Two different capacitor structures were used for measurements. Measurements were made using probe station, Impedance Analyzer and Network Analyzer shown in Figure 28. Measurement results for capacitor structure in Figure 27(c) is given in Figure 29. Response of capacitor changes with respect to concentration of sample that was used. Methodology that was applied for these measurements is extracting



(a) (b) (c) (d)

Figure 27: Fabricated IC integrated IDE Capacitors with different width and gap values

capacitance from the imaginary part of impedance using the formula in Equation 4. As equation implies, capacitance is inversely proportional to frequency. Capacitance is not the unique parameter that affects the change in impedance but at lower frequencies capacitance is the dominant parameter that affects the impedance. Dominance of capacitance at lower frequencies explains the peak that is observed in Figure 29.

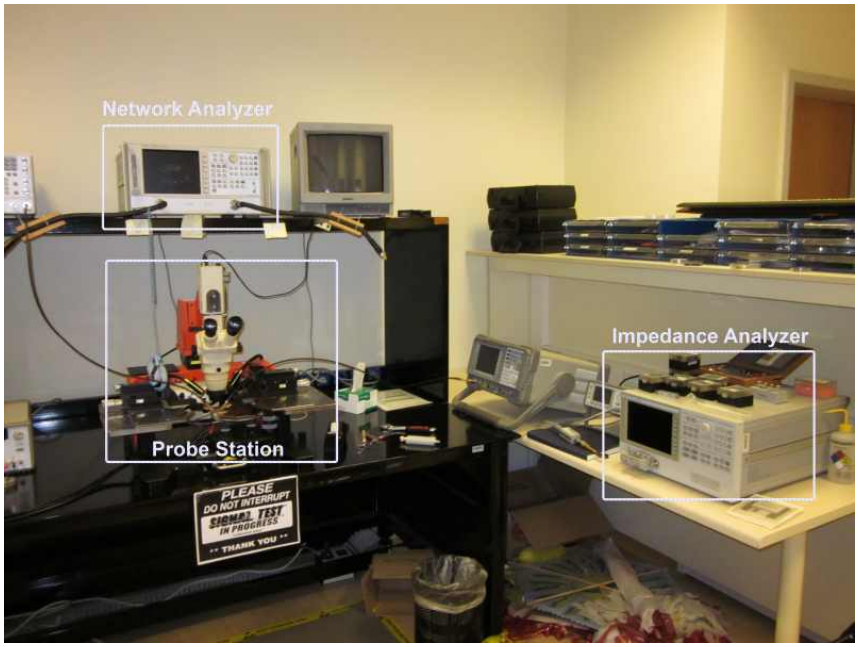


Figure 28: Setup for IDE Capacitor Measurements

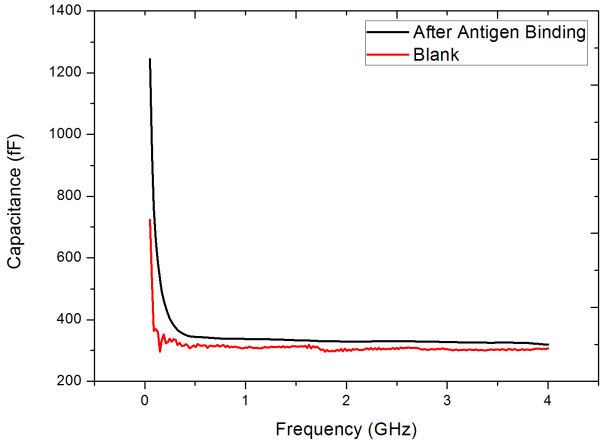


Figure 29: Capacitance of IDE capacitor for Blank Chip and after Antigen binding

2.3 Capacitance to Voltage Converter for Single IDE Capacitor

Second block of system is CVC design that is used for converting the capacitance change resulted from biosample on IDE capacitor. For designing CVC blocks IHP's 0.25 μm SiGe BiCMOS process was used. After biosample is dropped on capacitor, there will be capacitance change which should be quantified. There were three CVC designs that are developed for this system. First of them is based on measuring the capacitance change of single capacitor and commonly used CVC topology that is indicated in Figure 30. Second design aims at measuring capacitances of three IDE-capacitors because this system was decided to be improved for analyzing multiple IDE capacitors. Furthermore, there should be a mechanism that can compensate the shift in data that results from deposition of particles during measurement or cleaning processes. Therefore third CVC design was implemented as varactor tunable CVC to calibrate after deposition of particles.

CVC design in Figure 30 [45] has been chosen for this system. Advantage of this design is differential measurement that will decrease the effect of parasitics. With this development in topology, better sensitivity is aimed. Sub-fF capacitances can be measured with high precision [47]. Signals that will be applied to CVC are given in Figure 31. There are three operating states of this design. The states and the applied signal levels can be listed as following:

State 1 (V_{nmos}:0 V, V_{pmos}:0 V): At this state NMOS transistors whose gates are

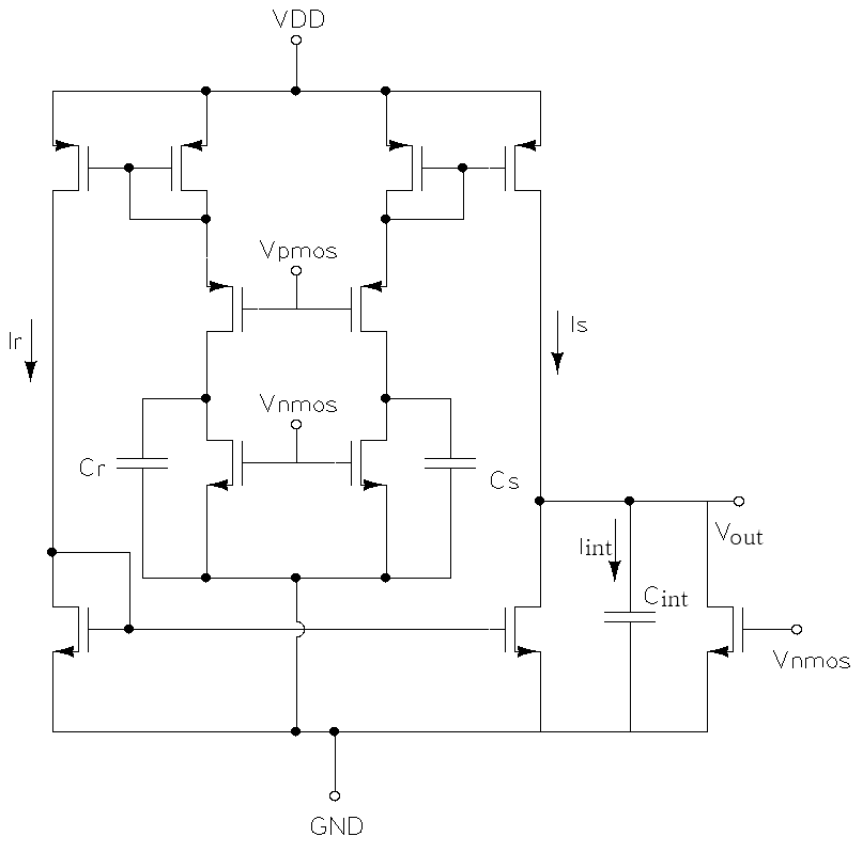


Figure 30: Readout Circuit Schematic for Capacitance to Voltage Converter

controlled by V_{nmos} signal will be OFF and PMOS transistors that are controlled by V_{pmos} are ON. C_v, C_s and C_{int} capacitors will be charged in this state.

State 2 (V_{nmos}:0 V, V_{pmos}:2.5 V): At this state NMOS transistors whose gates are controlled by V_{nmos} signal will be OFF and PMOS transistors that are controlled by V_{pmos} are OFF. The voltage levels on C_v, C_s and C_{int} will stay constant, the voltage level that is obtained in State 1 will be kept.

State 3 (V_{nmos}:1.5 V, V_{pmos}:2.5 V): At this state NMOS transistors whose gates are controlled by V_{nmos} signal will be ON and PMOS transistors that are controlled by V_{pmos} are OFF. The C_v, C_s and C_{int} capacitors are discharged over NMOS transistors.

Obtained output signal is indicated in Figure 31. At state 1, output signal increased to desired level instantaneously and during state 2 the signal level stays same. At state 3, the signal level at the output decreases to low level. The voltage that output level increases to is determine with the following equations:

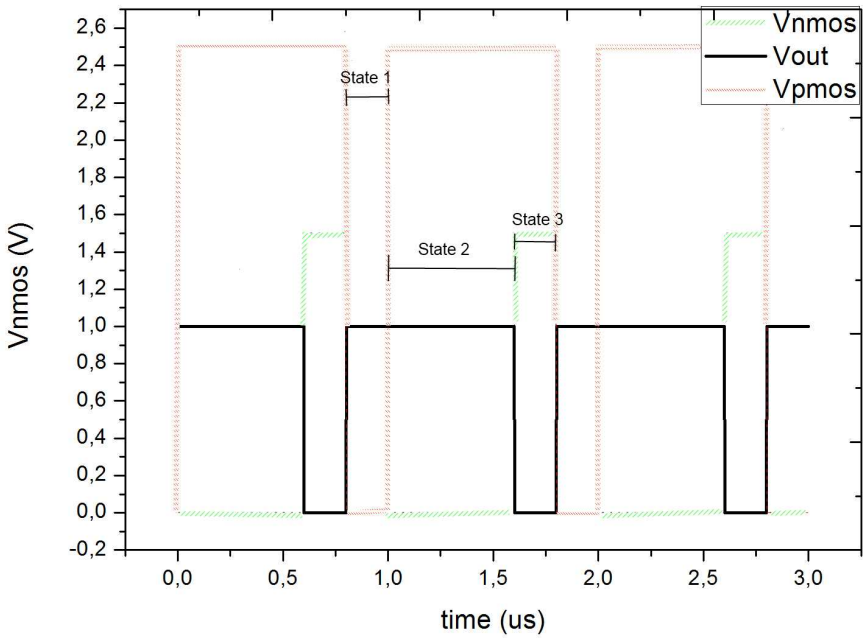


Figure 31: Applied pulses to transistors, operating states and corresponding ouput signal

$$I_{int} = I_s - I_r \tag{5}$$

$$V_{out} = freq * \frac{VDD - VGS}{C_{\text{int}}} * (C_s - C_r) \tag{6}$$

$$Sensitivity = \frac{V_{out}}{C_s - C_r} = freq * \frac{VDD - VGS}{C_{\text{int}}} \tag{7}$$

As shown in Equation 6 output voltage is a function of frequency and capacitors. Sensitivity which can be defined as the ratio of output voltage to difference between sensing and reference capacitors is proportional to operating frequency and inversely proportional to integration capacitor. Therefore it is desired to have higher operating frequency and lower integration capacitor [48].

2.3.1 Design of Capacitance to Voltage Converter for Single IDE Capacitor

Main concerns for this CVC block are to decide on the transistors' parameters and dimensions of integrations capacitances. since this design is first CVC design, high frequency is not an important parameter, most important criterion is linearity of output response.

First of all the transistors' width and length parameters will directly affect the sensitivity and parasitic capacitance of the transistor. At off-state, capacitance between source/drain and channel is proportional to width of transistor assuming there is an overlap. To decrease the capacitance W should be taken as low.

$$C_{Overlap} = W * L_{Overlap} * C_{ox} \tag{8}$$

On the other hand, to decrease the resistance of channel and decrease the RC time constant that will be important while capacitor is discharged, transistor width should be kept very large. Therefore there is trade-off between parasitic capacitance and parasitic resistance. Additionally, to decrease the effect of parasitics, length of switch-transistors are chosen as larger than smallest length process offers. Considering these advantages and disadvantages, transistor geometries were determined.

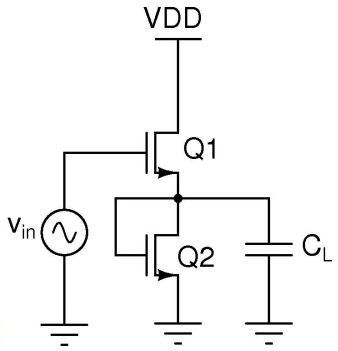


Figure 32: Schematic of common drain buffer amplifier with active load

One of the important parameters for biosensors is sensitivity. The sensitivity of biosensor block can be controlled via integration capacitance. If this capacitor is kept very high, sensitivity will be lower but dynamic range will be higher. Therefore there is a trade-off between sensitivity and dynamic range assuming single integration capacitor is utilized.

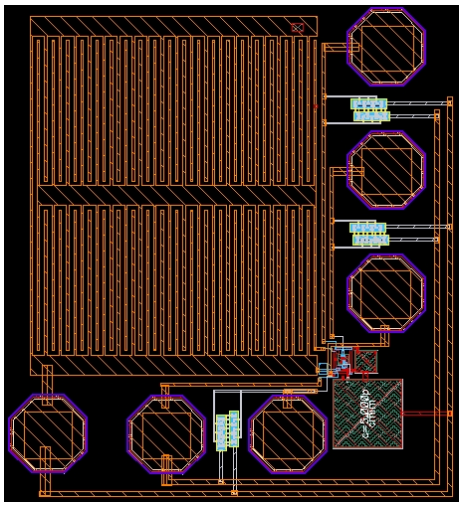


Figure 33: Layout of Conventional CVC Design

Additionally, in this preliminary design, Source Follower with Active Load whose schematic is given in Figure 32 was used as a buffer. Buffer was designed to drive high load capacitances. In this design, high frequency is not main aim, desired operation frequency is between 10 kHz and 100 kHz. This frequency range can be obtained using Source Follower with Active Load buffer stage.

2.3.2 Simulation Results of Capacitance to Voltage Converter for Single IDE Capacitor

Layout of the design including Source Follower Buffer stage is given in Figure 33 and total chip area is 0.22 mm^2. For post-layout simulations signals in Figure 34

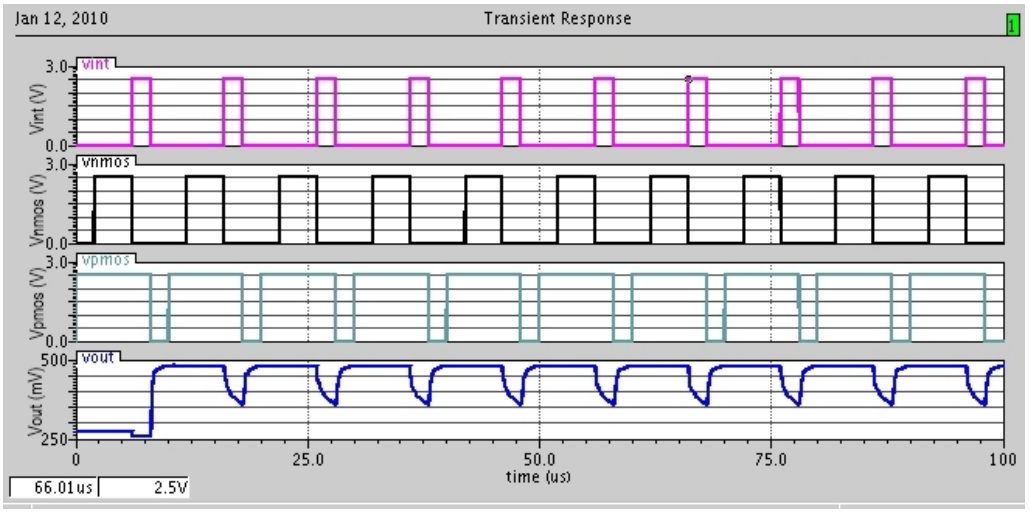


Figure 34: Applied Signals and Corresponding Post-Layout Output Signal for Designed CVC Block

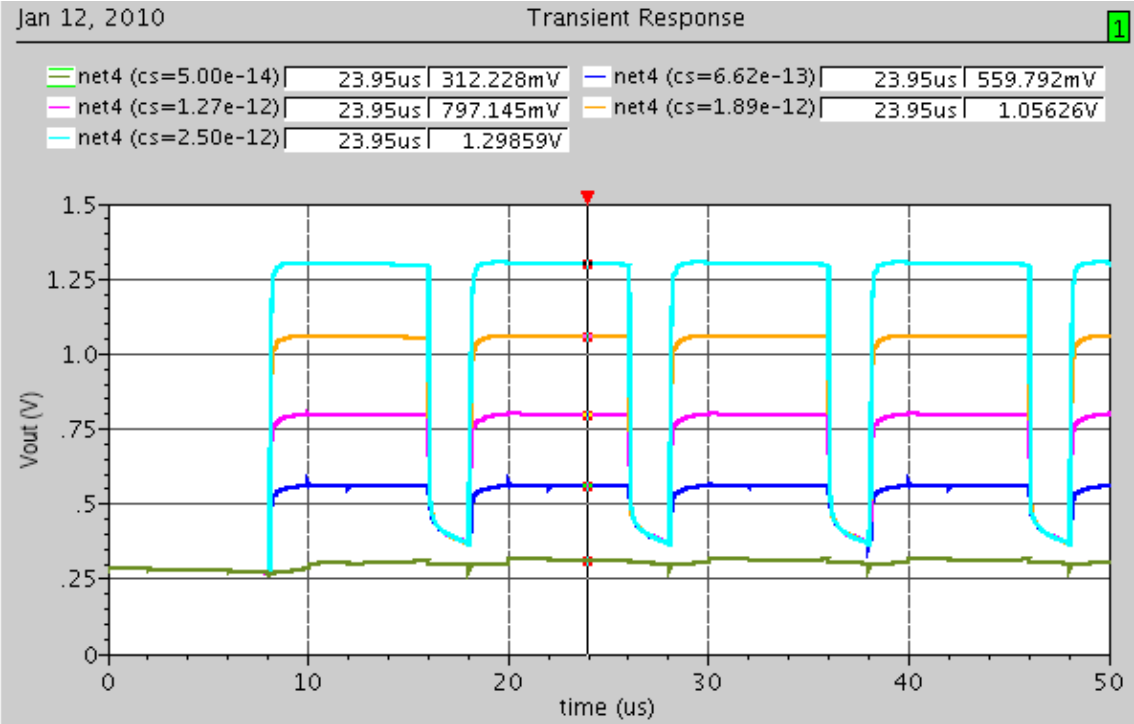


Figure 35: Post-Layout output signals of designed CVC for different sensign capacitor values

were applied and resulting output signal is also shown in the same figure.

For simulating capacitance change, built-in capacitor is connected parallel to sensing capacitor. Built-in capacitor is changed from 50 fF to 2.5 pF and output response given in Figure 35 is obtained. Main reason for this high range was to be able measure different biosamples and high dynamic range is aimed.

Highly linear response has been obtained. As Figure 36 shows, output voltage changes linearly with respect to capacitance change. This will be advantageous for measurements. Otherwise extracting capacitance from output voltage will be difficult.

Power Consumption of this preliminary CVC changes between 295 μW and 10.9 mW depending on the changes in sensing capacitance. This power consumption may seem high but 2.5 pF capacitance change will be ideal change. This design was developed for observing the capacitance change range.

There is an offset problem that is inevitable. Capacitor could not be fully discharged over the switch transistor. Therefore there is a remaining voltage offset at the output. This offset increases with decreasing the capacitance value of integration capacitor. Therefore it is beneficial to keep integration capacitor as high as possi-

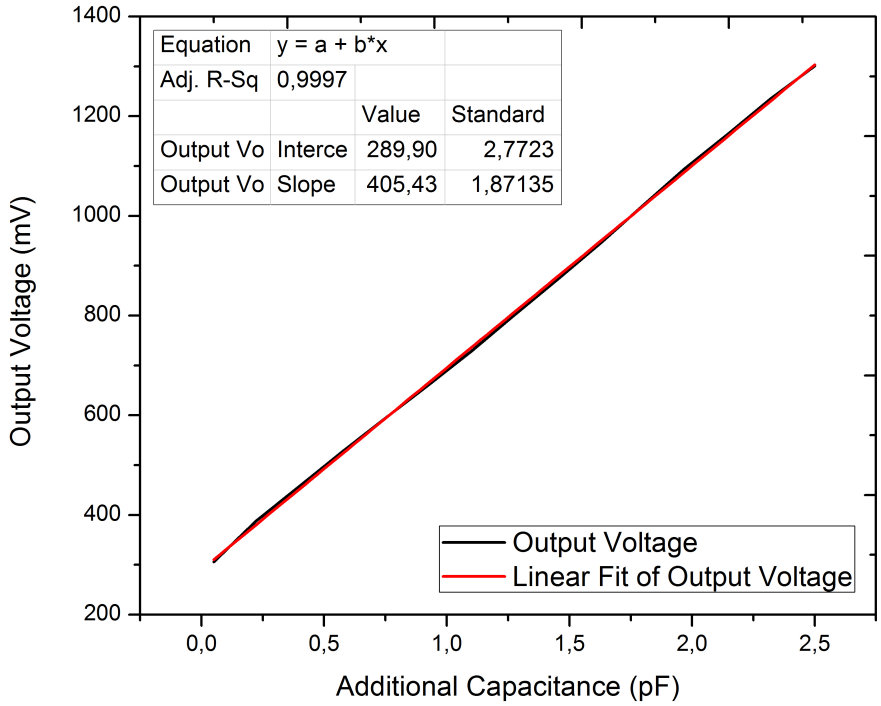


Figure 36: Output linearity of CVC design for single IDE capacitor

ble. In this design high dynamic range was aimed therefore integration capacitor was kept high therefore offset voltage was lower.

2.4 Capacitance to Voltage Converter for Three IDE Capacitors

2.4.1 Design of Capacitance to Voltage Converter for Three IDE Capacitors

In addition to commonly used CVC block, improved version was also designed. The improvement was to extend CVC for multiple capacitors. Since the aim of this project covers sensing multiple capacitors and controlling the active capacitor manually via gate voltages of switching transistors. Therefore there should be CVC design that is capable of reading capacitor array. For this aim conventional CVC design is modified to new CVC design whose schematic is given in Figure 37. According to our researches, conventional CVC design has not been modified for multiple IDE capacitors applications.

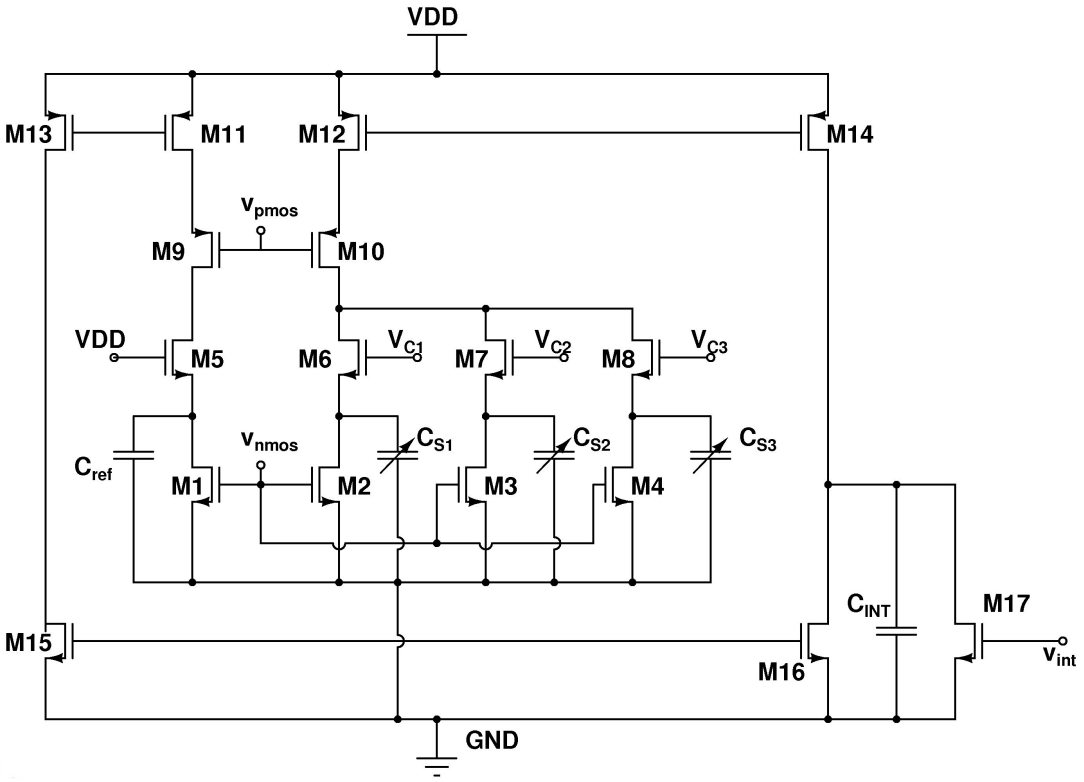
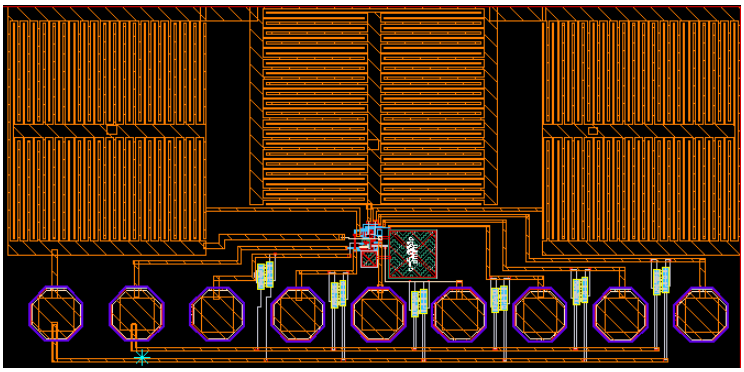


Figure 37: Schematic of CVC with Three Sensing Capacitors

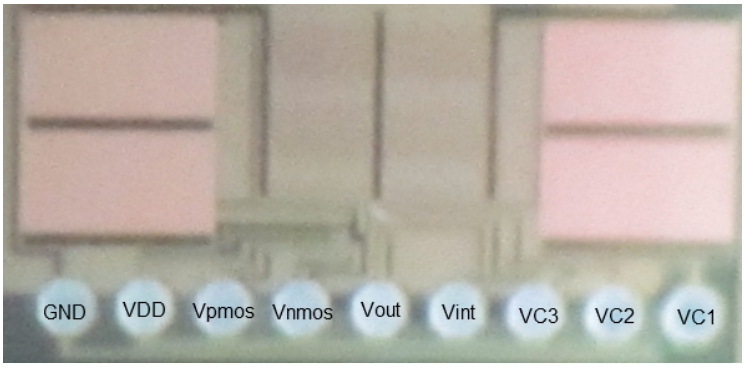
In this design, main differences from conventional design are three capacitors that are labeled as C_{S1}, C_{S2} and C_{S3}, instead of one sensing capacitor. For deciding which capacitor will be active, select signals will be applied to gates of M6, M7 and M8 transistors. Just one of these three capacitors should be active at a time. In this design, it is not guaranteed to have at most one active capacitor but this improvement can be applied with a simple demultiplexer circuit in further designs. Furthermore, M5 transistor was added to conventional design. Main reason for addition of this transistor is to maintain the match between reference and sensing branches. Otherwise there will be mismatch between two branches that will affect the output in a negative way. Additionally, M5's gate is connected to VDD since that line should be open always while just one of the sensing capacitors is active.

2.4.2 Simulation Results of Capacitance to Voltage Converter for Three IDE Capacitors

The layout and microphotography of CVC for Three IDE Capacitors are given in Figure 38. Chip area is 0.47 mm^2 excluding pads and total area is 0.58 mm^2. Switching between sensing capacitors will be important issue for both switching from high



(a)



(b)

Figure 38: a) Layout b) Microphotography of CVC Design with Three Sensing Capacitors

capacitance to low capacitance and low capacitance to high capacitance. Dimensions of M2, M3 and M4 play important role for switching. Capacitor discharging

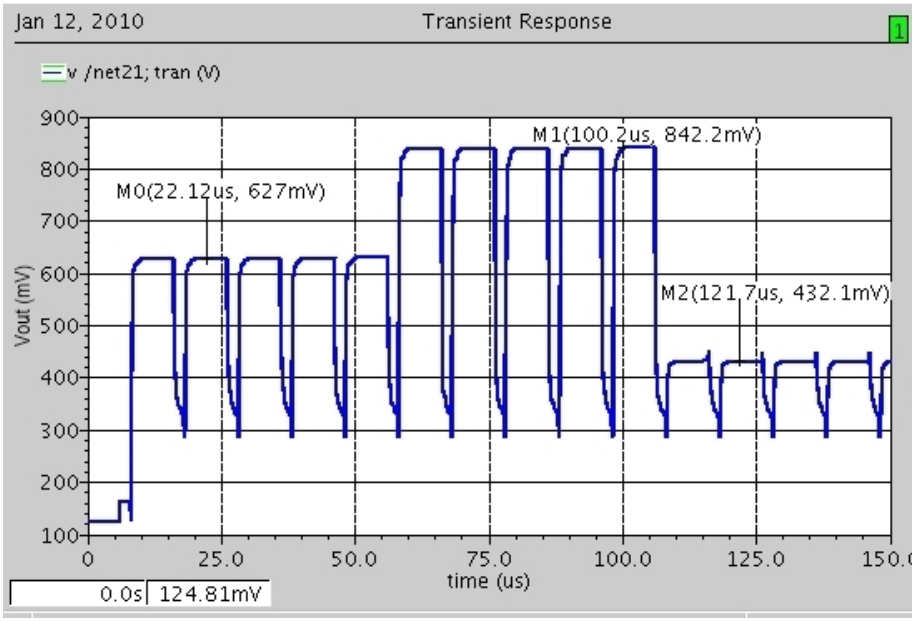


Figure 39: Post-Layout Simulation Result of Switching Capacitors that have different capacitance values

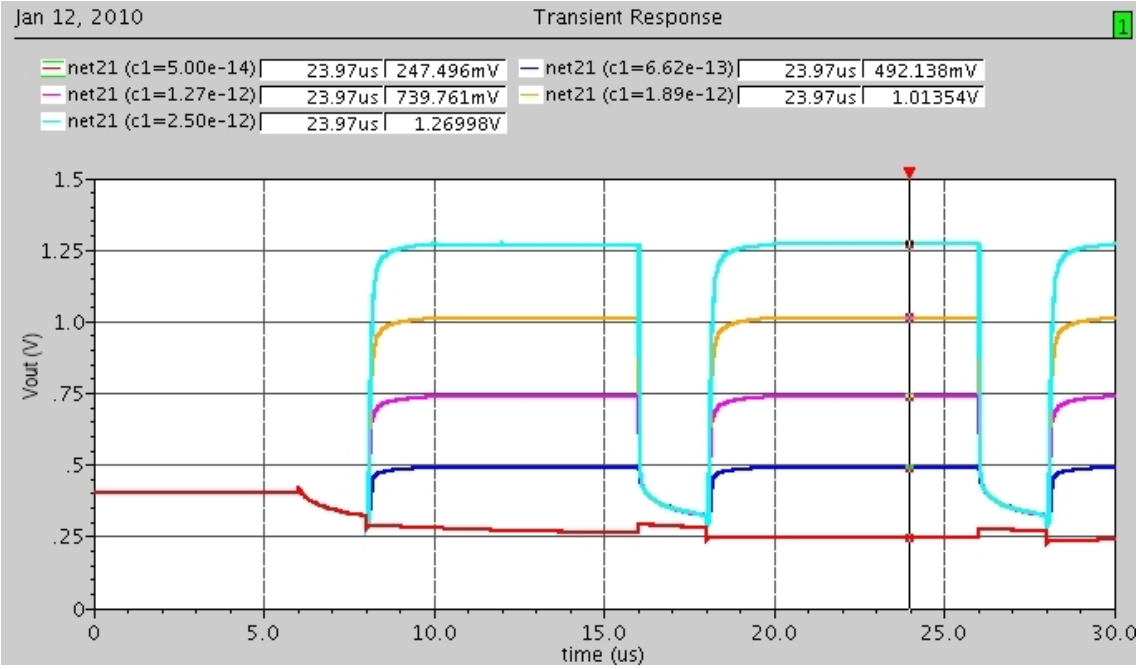


Figure 40: Simulation results of three capacitor design for different capacitor values to show the linear response of output voltage corresponding to sensing capacitor

should take quite short time for faster switching. In terms of working principle and advantage, most important aspect is ability to measure three capacitors at the same time. As post-layout simulation result in Figure 39 indicates, switching between capacitors was done without any delay or error as expected.

Output voltage of a three capacitor design is given Figure 40. As it can be clearly observed, output voltage values are almost same for both single and three capacitor designs. Another simulation result in Figure 40 shows the linearity of output signal with respect to change in sensing capacitor. More than 99% percent linearity is obtained from this design.

Power consumption of this design is lower than 845 μW for all sensing capacitance values. This power consumption value is good when compared to other researches. Post-layout simulation result given in Figure 41 shows the sensitivity of the device as 0.415 mV/ fF. Assuming minimum measurable signal level is 10 mV because of noise level of measurement setup, minimum detectable capacitance will be 24 fF.

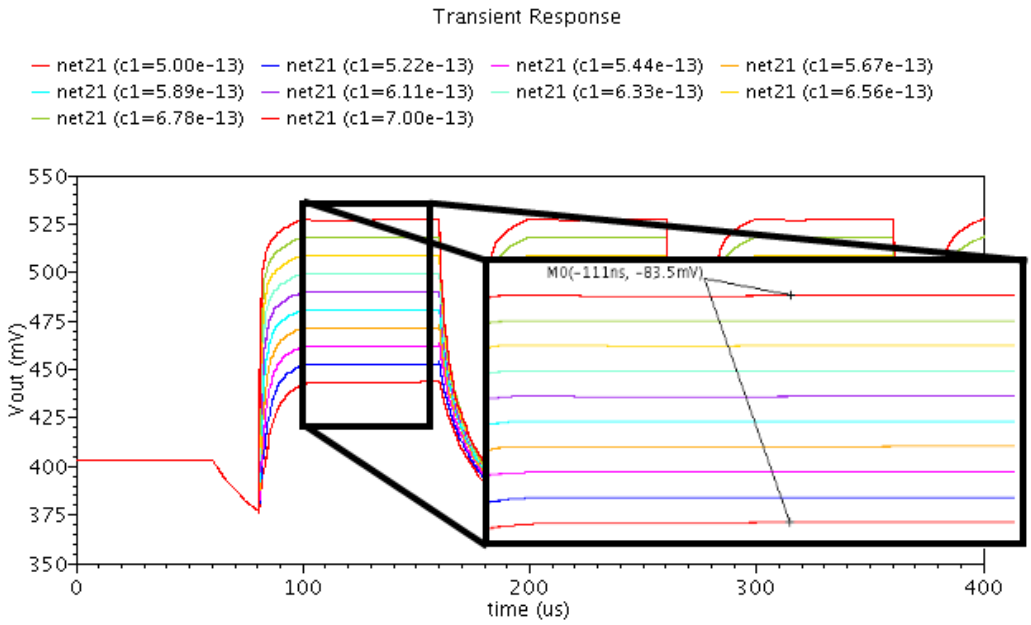


Figure 41: Post-Layout simulation results of sensitivity of CVC for three IDE capacitors

2.5 Varactor Tunable Capacitance to Voltage Converter

2.5.1 Design of Varactor Tunable Capacitance to Voltage Converter

In previous designs, single and three-capacitor CVC designs, there were some problems that have been encountered during measurements. To solve these problems, new design has been implemented. Moreover, compensating drift in sensing capacitor via varactor tuning is proposed as new idea to conventional CVC design.

First problem is related to paths that are drawn using Top Metal 2 metal layer of IHP SiGe BiCMOS process (TM2). Resistance and capacitance of TM2 metal layer is lower compared to other layers, therefore TM2 was used for long paths. It is obligatory to use long paths because IDE capacitor has large area whereas IC chip has smaller area. In terms of parasitic performance, these designs may work well but there was bonding problem that we have encountered. Since passivation layers on chip was removed for better sensitivity, TM2 layer is almost open. While bonding chip to PCB, short circuits occurred that affected measurements in a disastrous way. To solve this problem, in Varactor Tunable CVC design, long paths are drawn using Top Metal 1 (TM1) or Metal 3 (M3) layers to prevent possible short circuits during bonding. This may cause also problems during measurements as well, since metal

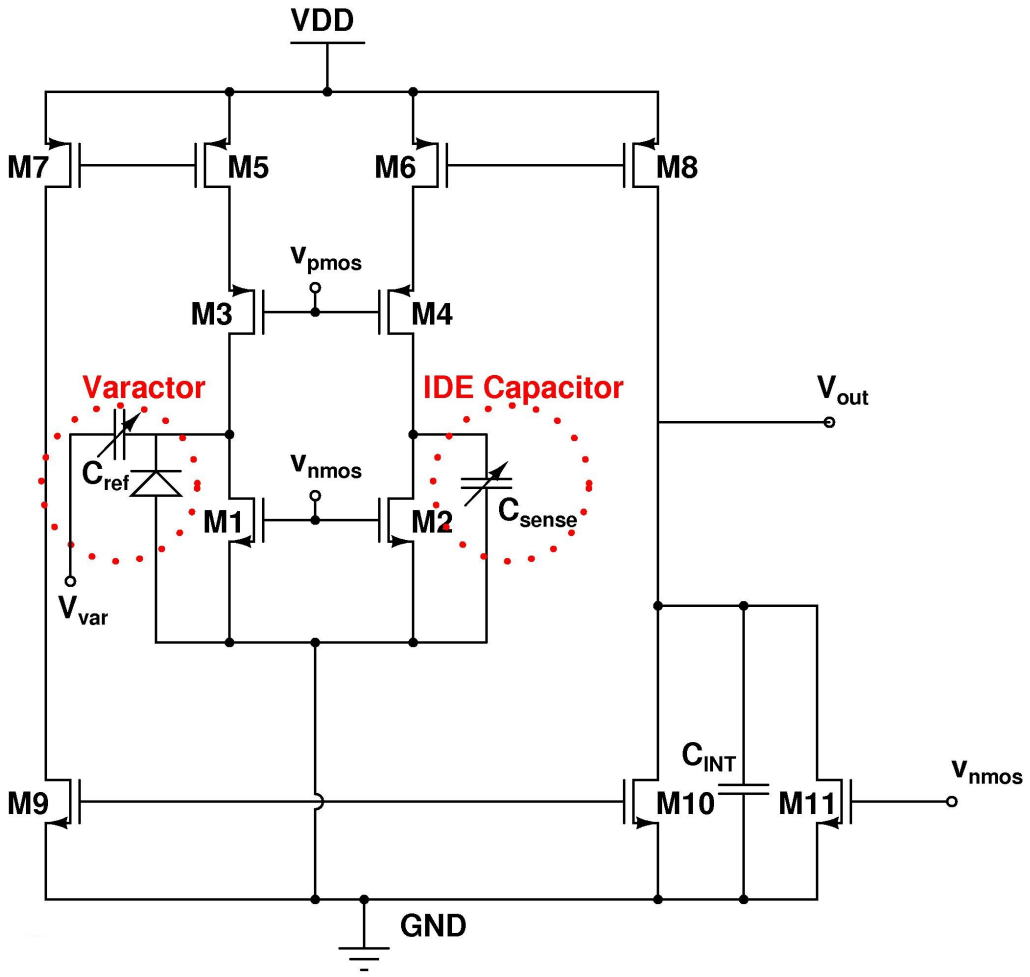
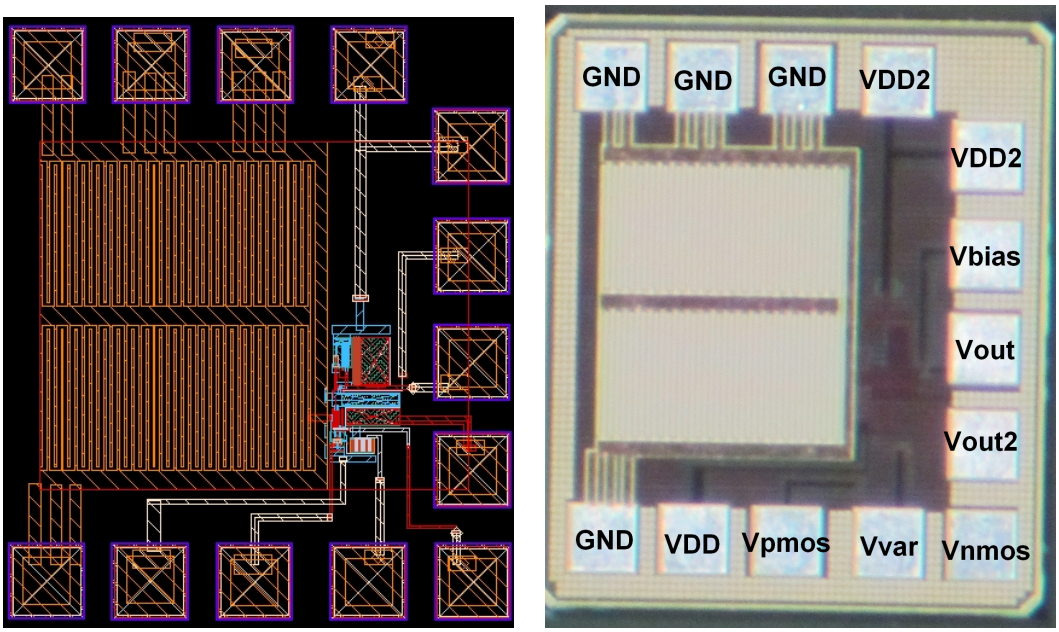


Figure 42: Schematic of Varactor Tunable CVC

layers are open, droplet of biosample may affect the behavior of chip.

Second problem is related to buffer stage. Source Follower stage could not drive high load capacitances at high frequencies. Therefore this buffer stage is replaced with Two-Stage Buffer OpAmp. Buffer Amplifier consists of two stages; first stage is differential amplifier stage and second stage is common source amplifier stage. Additionally series RC has been added between outputs of two stages to improve the frequency behavior of the design. With this improvement, high capacitive loads can be driven.

Third problem is related to life-time of biosensor. After biochemical processes, there may be deposited particles that cause shift in capacitance values. This problem will result in uncertainty in data extraction from capacitance change. In this design, reference capacitor is formed by varactor instead of built-in capacitor. Varactor's capacitance will be tunable by external voltage. Resulting schematic is indicated in Figure 42. Total area of CVC including buffer stage and excluding pads is 0.18



(a) (b)

Figure 43: a) Layout b) Microphotography of Varactor Tuning CVC Design

mm^2, total chip are is 0.4 mm^2. Layout and microphotography of the Varactor Tunable design are given in Figure 43.

One of the important concern for this design is change of voltage level at drain of M1 transistor. Simulation results show that, potential at this node does not change too much. There will be square-like signal at that node; at low level capacitors will be discharged whereas at high level, capacitors will be charged and stay at constant value. Therefore change of voltage at drain of M1 will not have effect on capacitance of varactor.

2.5.2 Simulation Results of Varactor Tunable Capacitance to Voltage Converter

Two stage OpAmp is used in this design for Buffer stage. Main aim of using buffer stage is to load high capacitances for measurements. Because oscilloscope probe will have its own capacitance that is 15 pF unless active probe is used. Desired operation frequency is 10 MHz therefore OpAmp should operate at 10 MHz with high Phase Margin. Designed Buffer OpAmp has 80° which will prevent oscillation of amplifier. Even though gain seems low, this will not create big problems. Therefore this design will be enough to drive 15 pF oscilloscope probe.

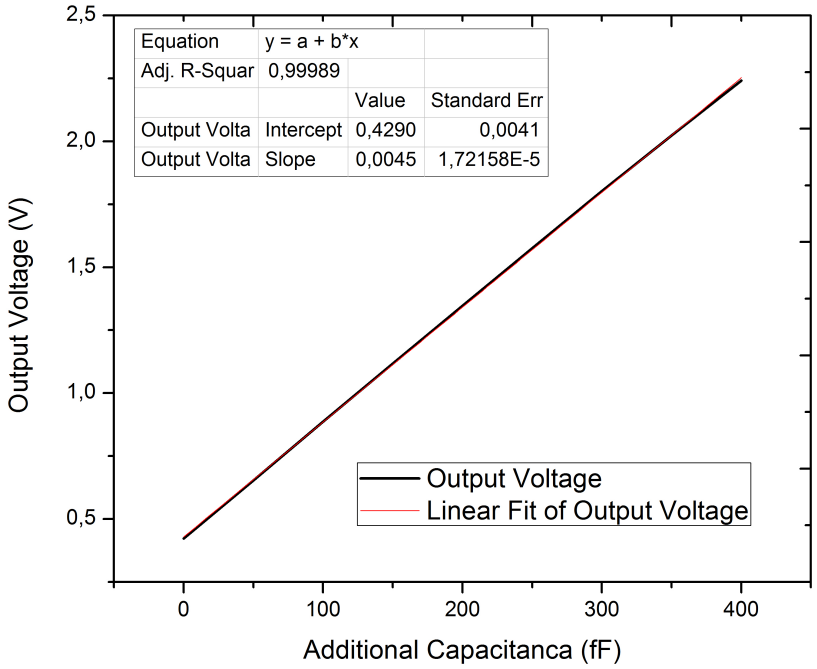


Figure 44: Linearity of Response Varactor Tunable CVC Design to Capacitance Change

As mentioned in Chapter 2.3.2, there is an offset voltage at the output. In this design high sensitivity is aimed. Instead 2.5 pF capacitance change range, 450 fF dynamic range is aimed. Hence, integration capacitor is kept low. This results in higher offset voltage. Figure 44 shows the post-layout simulation results of linear response of this varactor tunable CVC design. In addition to these results, total power consumption of Varactor Tunable CVC block including buffer changes between 441 μW and 1.037 mW depending on the capacitance of sensing capacitor.

Even though change in output signal seems linear with respect to sensing capacitance change, effect of varactor should be simulated. For this aim, calibration mechanism should be simulated. Assuming that, initially output voltage level is at V_X, sensing capacitance is C_X and varactor capacitance is C_{VX}. After some continuous measurements, drift in sensing capacitance may occur and capacitance changes to C_Y. This drift results in shift in output voltage level to V_Y. Using the tuning voltage of varactor, output voltage level can be tuned from V_Y to V_X again by changing varactor capacitance to C_{VY}. During this tuning process, important question that should be asked is that if change in sensing capacitance (C_Y-C_X) is

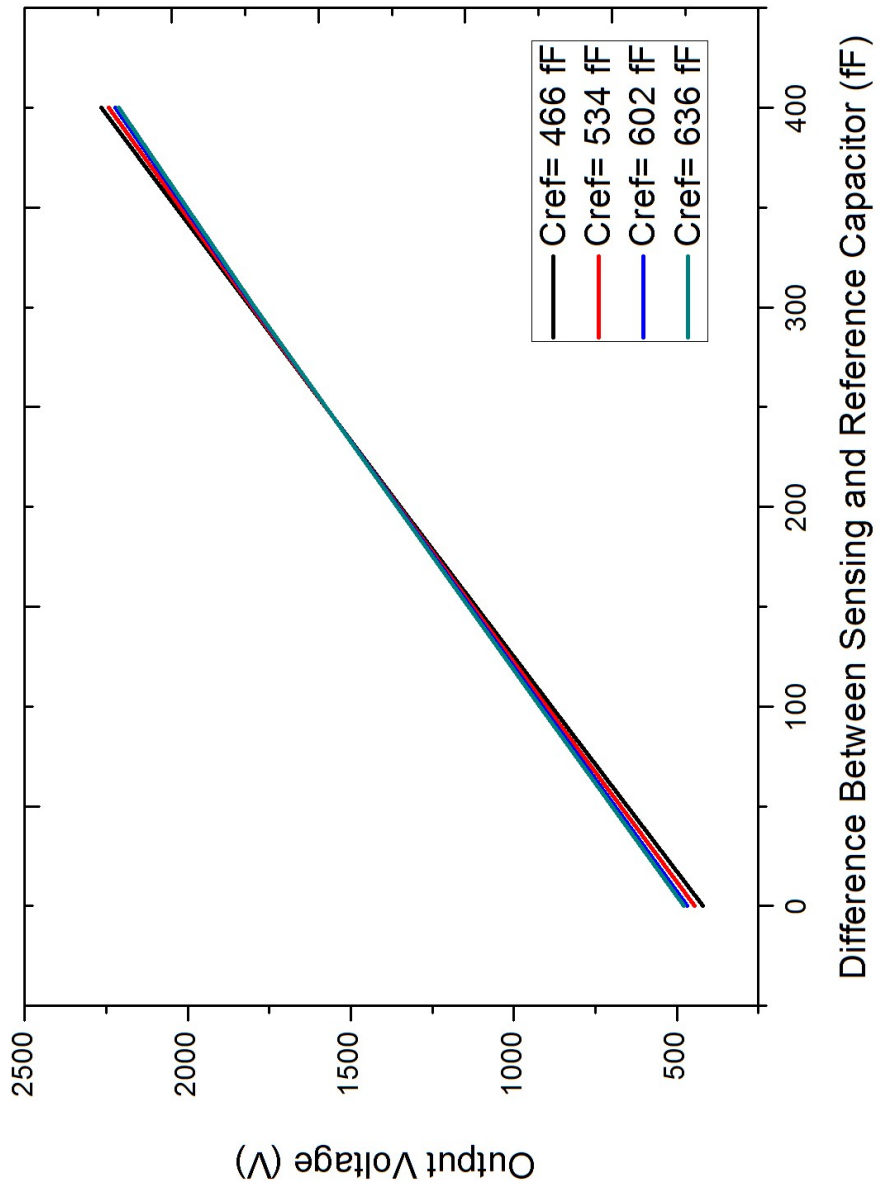


Figure 45: Change of output voltage for differenent reference capacitance values

equal to tuning in varactor capacitance (C_{VY}-C_{VX}). This question can be asked in another way, if output voltage level is same for a constant C_S-C_{REF} and different C_{REF} values. For verifying the compensation of drift in capacitance, post-layout simulation result in Figure 45 is obtained. As this graph shows, for different reference capacitances almost same linear lines are observed. This proves that varactor tunable CVC design can be used for compensation of drift in IDE capacitor.

2.5.3 Simulation Results of Two-Stage Operational Amplifier for Buffer Stage

Following the Capacitance to Voltage Converter stage, Two-Stage Operational Amplifier with zero compensation was used for driving 15 pF load that is the oscillope's probe capacitance. Without this buffer stage, the output signal of Capacitance-to-Voltage Converter wouldl be distorted because of high load capacitance. Advantage of Buffer stage results from its low output impedance. Buffer can be implemented with Common Drain topology or more complex topologies can be implemented.

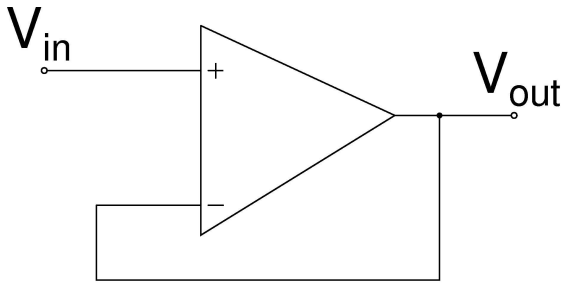


Figure 46: Schematic of buffer-connected Op-Amp with Ideal Op-Amp

Common Drain amplifier, that are also known as Source Follower, can be used as voltage buffer because the source voltage follows the voltage applied to gate of transistor. Source Follower amplifier has advantages such as simplicity and high operating bandwidth. Additionally output impedance is low that enables driving high load capacitances [49]. Despite of these advantages, complex configurations are preferred for buffer design. Main reason for this choice is linearity concern. Because of the non-ideal behaviors such as channel-length modulation, body effects, frequency dependent distortions etc. source follower stages are not used for high precision and high frequency applications [50]. In Source Follower design with active

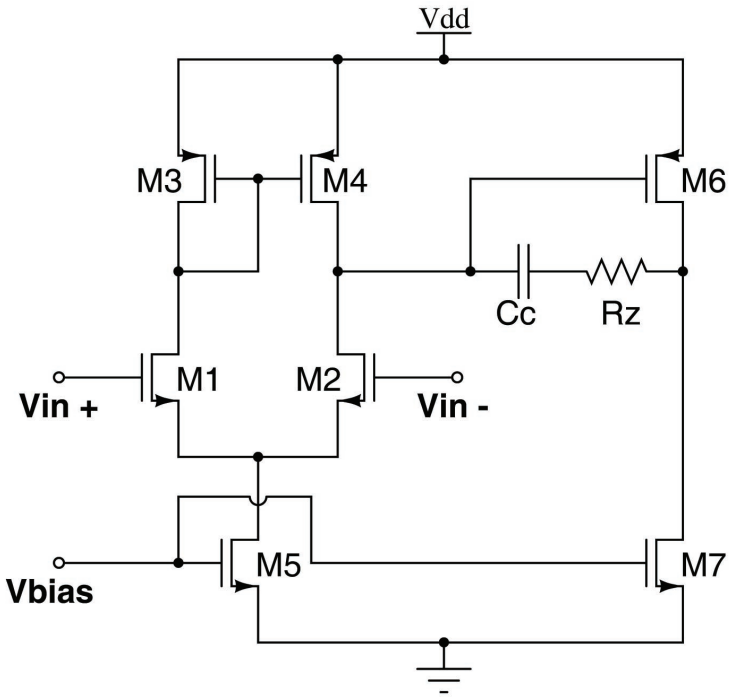


Figure 47: Schematic of Two Stage Operational Amplifier Design

load, source and bulk of M1 transistor will not be connected to same node. This results in body-effect which causes change of threshold voltage of the transistor.

As an alternative to Source Follower, two stage operational amplifier buffer circuit is commonly utilized. Schematic of buffer-connected Op-Amp with ideal amplifier is indicated in Figure 46, inverting input of Op-Amp is connected to output and signal is applied from non-inverting input. Ideal Op-Amp is replaced with Op-Amp in Figure 47. First stage is differential stage that decrease the effect of parasitics whereas second stage is common source stage to obtain high gain at the output. To decrease the oscillations of Op-Amp, series RC feedback is applied between output of first stage and second stage.

The Operational Amplifier that is implemented in buffer design is indicated in Figure 47. Voltage gain of Standard Two Stage Operational Amplifier is given in the following equation.

$$A_v = (-g_{m1} * (r_{04}//r_{02}) * (-g_{m7} * (r_{06}//r_{07})) \tag{9}$$

In addition to standard two stage Op-Amp, improvements are applied for obtaining better phase margin performance. Phase Margin (PM) of Op-Amp can be

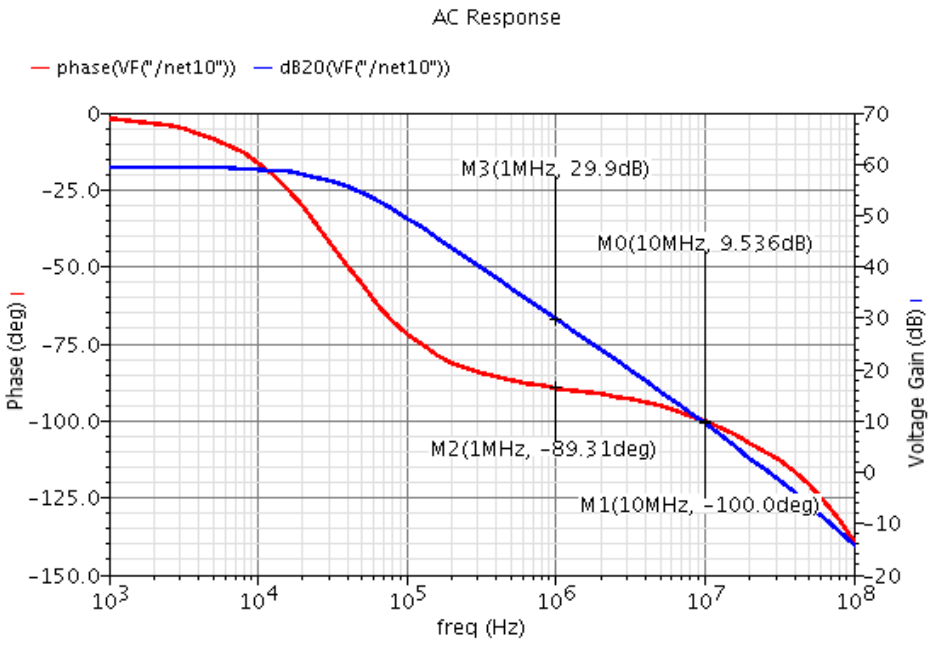


Figure 48: Simulation results of proposed Two-Stage Op-Amp for Buffer Stage

calculated using the formula in Equation 10.

$$\begin{aligned} PhaseMargin &= 180 - \phi_{P1} - \phi_{P2} - \phi_Z \\ &= 90 - tan^{-1}(\tfrac{f_t}{f_{P2}}) - tan^{-1}(\tfrac{f_t}{f_Z}) \end{aligned} \tag{10}$$

To increase the PM of Op-Amp, output of 2^{nd} stage and 1^{st} stage are connected via series resistor and capacitor. This feedback mechanism helps to move f_{P2} and f_Z to higher frequencies. It is expected to have f_{P2} 10 times greater than f_t whereas f_Z will be moved to infinity with a choice of R_Z impedance. After these improvements, it is expected to have PM around 60 which will be enough to prevent oscillation.

Simulation result of designed Op-Amp is given in Figure 48. Phase Margin of proposed Operational Amplifier is in safe margin and gain is higher than 1 at aimed frequency range.

Post-layout simulation result given in Figure 49 shows the sensitivity of the Varactor Tunable CVC with Buffer Amplifier as 4.5 mV/ fF. Assuming minimum measurable signal level is 10 mV because of noise level of measurement setup, minimum detectable capacitance will be 2.22 fF. As comparison of these works with works from literature shows, our works have smaller area compared to other pro-

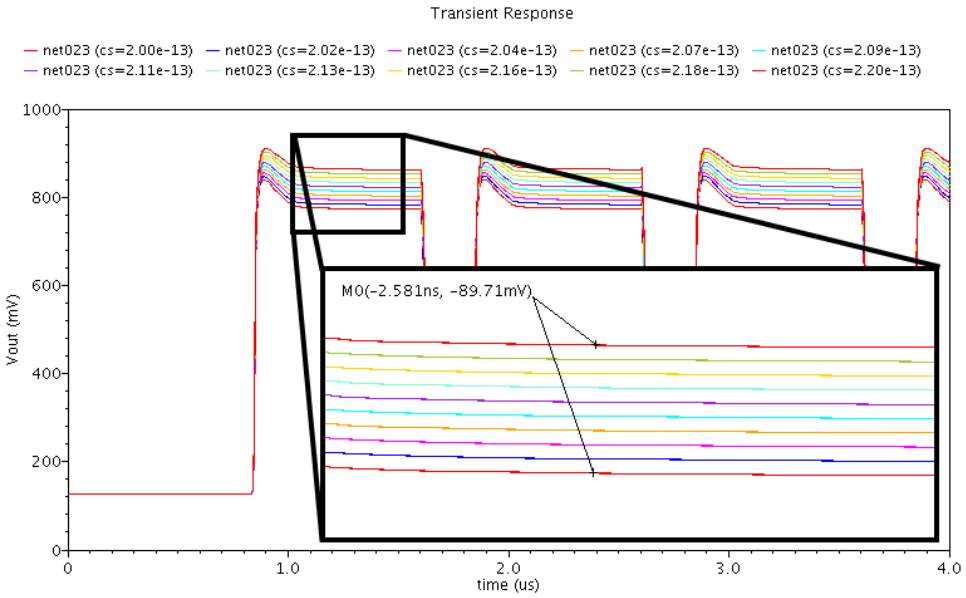


Figure 49: Post-Layout simulation results of sensitivity of Varactor Tunable CVC

cesses. Additionally, our works have higher output voltage swing range even though break down voltage of our process is lower than other processes.

Table 5: Comparison of Biosensor Works

	Process	Area (mm^2)	Sensitivity	Dynamic Range
[31]	0.35 μm	4	80 mV / pF	10 pF
[32]	0.5 μm	8.75	325 mV / fF	4.8 fF
[51]	0.35 μm	-	1 mV / fF	800 fF
[52]	0.35 μm	2	0.2 mV / fF	4 pF
CVC for 3 IDE	0.25 μm	0.58	0.415 mV / fF	2.5 pF
Var. Tunable CVC	0.25 μm	0.4	4.5 mV / fF	450 fF

2.6 Low-Pass Filter

CVC block will generate square like signal and it should be converted to DC signal. This conversion can be done via RC Low-Pass Filter in Figure 50 that has very high RC time constant. Since time constant should be very large, this block requires large area if it is intended to be designed on-chip. Therefore this block will be designed off-chip.

Generated square-like signal oscillates between two signal levels. Square signal will have AC and DC components. Since purpose of using Low Pass Filter (LPF) in this system is obtaning DC signal, AC signals will be subtracted from square-

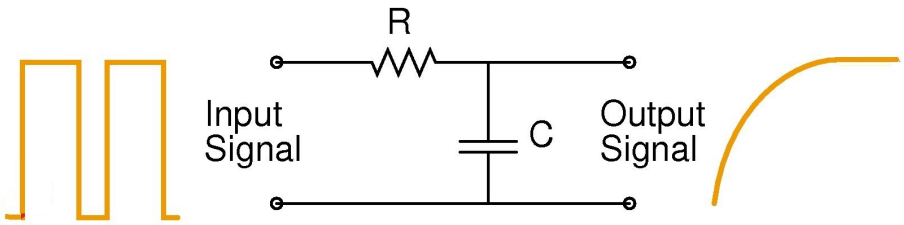


Figure 50: Schematic of RC Low-Pass Filter

like signal. Furthermore, pulse width should be kept as high as possible to obtain higher DC level. To verify this, two LPF structures are simulated with same LPF structures (same resistor and same capacitor). Input signals oscillate between 0V and 2V. Except from pulse width of input signals, parameters are kept same for two designs. As graph in Figure 51 shows, signal with higher width has higher voltage value. This result can be predicted by taking pulse width 0% and 100% of period. Output signal will be 0V if pulse width of input signal is 0%. On the other hand, output signal level will be 2V if pulse width of input signal is 100%. Hence, pulse width is chosen 80% for this design.

Another concern for LPF is RC time constant decision. Decreasing time constant too much will improve the flatness of output signal. Drawback of low RC time constant is increase in transition time that will result in loss of data. Therefore there is a trade-off between flatness of output signal and transition time. For simulations, resistor and capacitor are chosen as 5 MΩ and 20 pF respectively. Post-layout

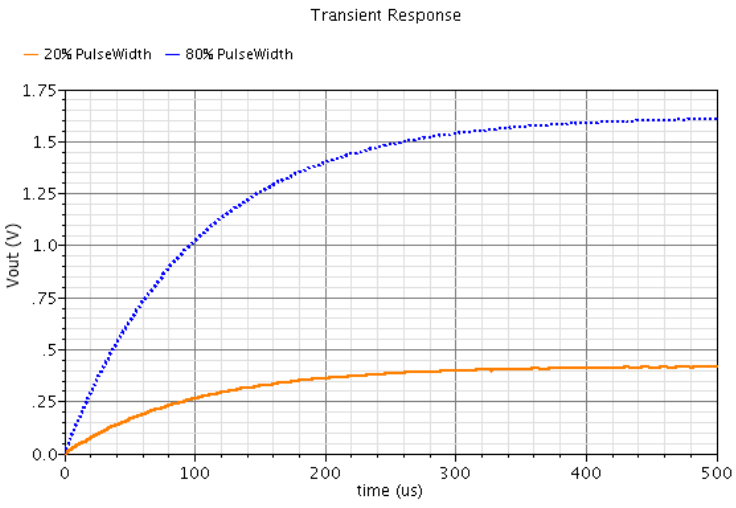


Figure 51: Effect of pulse-width of input signal on DC level of output signal

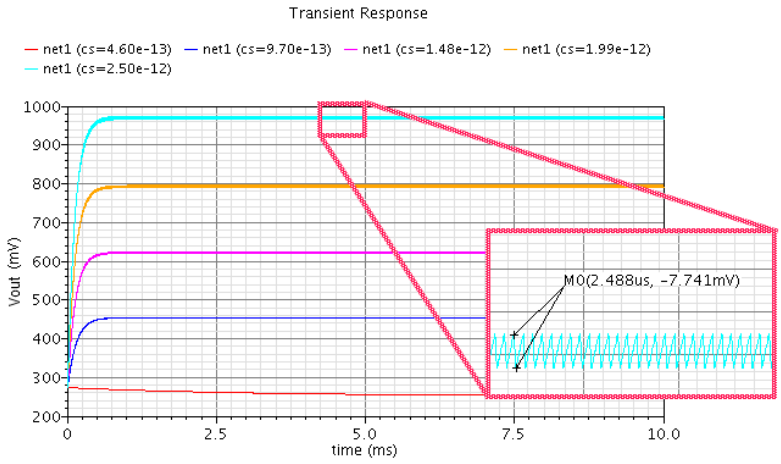
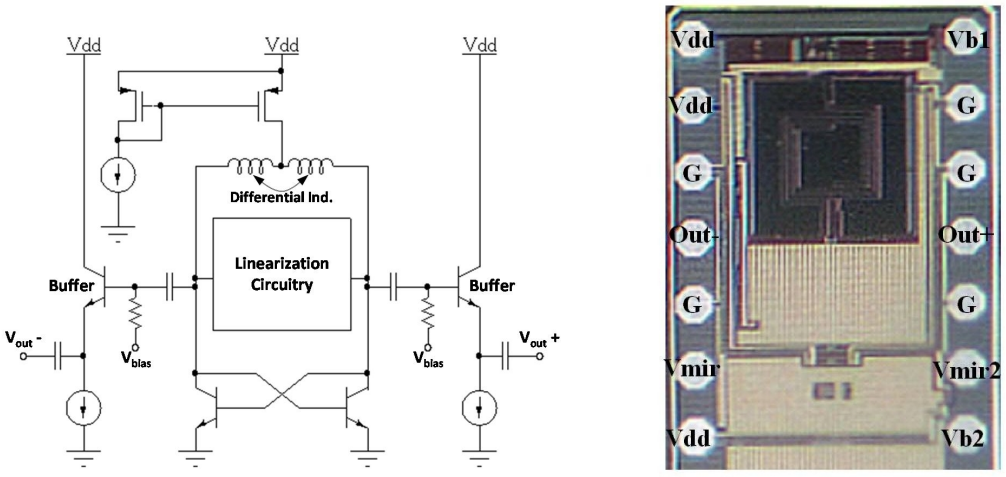


Figure 52: Post-Layout simulation result obtained from CVC and LPF blocks with R=10 MΩ and C=20 pF

simulation result of connecting LPF and CVC design is given in Figure 52.This graph shows that less than 1% fluctuation occurs at the output signal.

3 Transmitter Design Blocks and Measurement Results

In this project transmitter block is used for converting the obtained voltage to corresponding frequency by LC-tank VCO block. Second block will be utilized for amplifying the generated signal to higher power levels. In this work, transmitter wass designed to operate at frequency band (2.29-2.72 GHz) that covers ISM frequency band [53]. ISM frequency band is a free-band that is dedicated to industrial, scientific and medical applications. As system working principle indicated, main purpose of transmitter block is transmitting signal that is obtained via IDE capacitors and readout circuit. These data will be received by host device and further analysis might be done on host device such as PC. Due to operation wide frequency band and possible interference from environment, it is assumed that operation will be carried in a room that environmental interference at operating frequency is negligible. Therefore transmitting signal by proposed system and recognizing signal by stationary device will be manageable. Aiming at hand-held device with high linearity directed us to choose Linear LC-tank VCO design and Class-E PA for transmitter topology. Although transmitter blocks are designed by my colleagues, I have involved in design process, analysis and measurements of these blocks.



(a) (b)

Figure 53: a) Schematic b) Microphotography of Linear VCO design

3.1 Voltage Controlled Oscillator Design and Measurement Results

A wide-frequency band including ISM band LC-tank VCO with linear frequency tuning chracteristic is implemented in 0.25 μm IHP SiGe BiCMOS process technology. Figure 53 shows the layout and microphotograhy of the designed VCO with labeled pins. Area of VCO chip is 0.5 mm^2 excluding pads and total area is 0.7 mm^2.

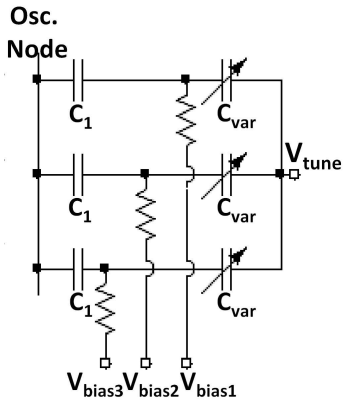
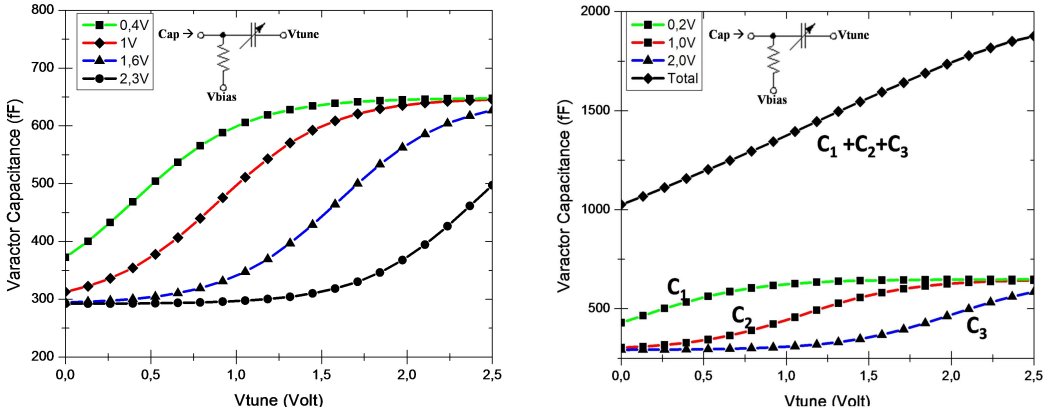


Figure 54: Proposed varactor topology for Linear VCO design

For obtaining linear response, new varactor tank topology is proposed. The schematic of proposed varactor tank is given in Figure 54. Basically, as Figure 55 indicates, varactors has different capacitances depending on bias voltages. Combination of multiple varactors may result in varactor bank that can enable linear frequency shift with respect to tuning voltage of varactor bank.



(a) (b)

Figure 55: a) Capacitance change of single varactor with tunning voltage for different bias voltages b) Capacitance change of proposed varactor tank with tunning voltage

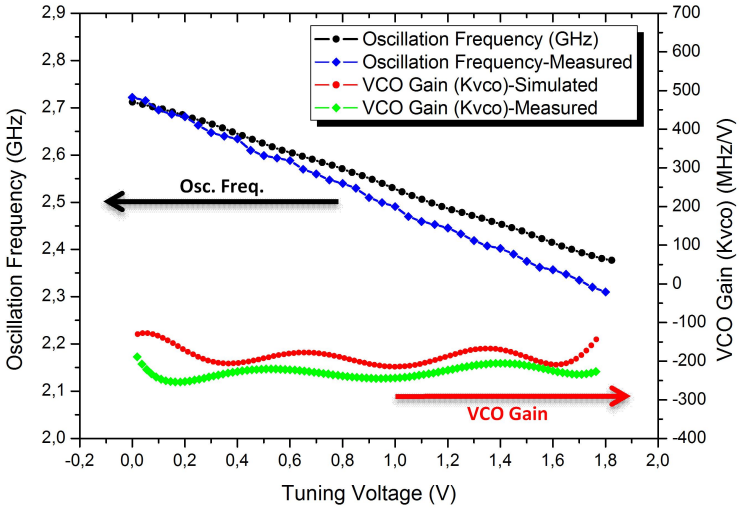
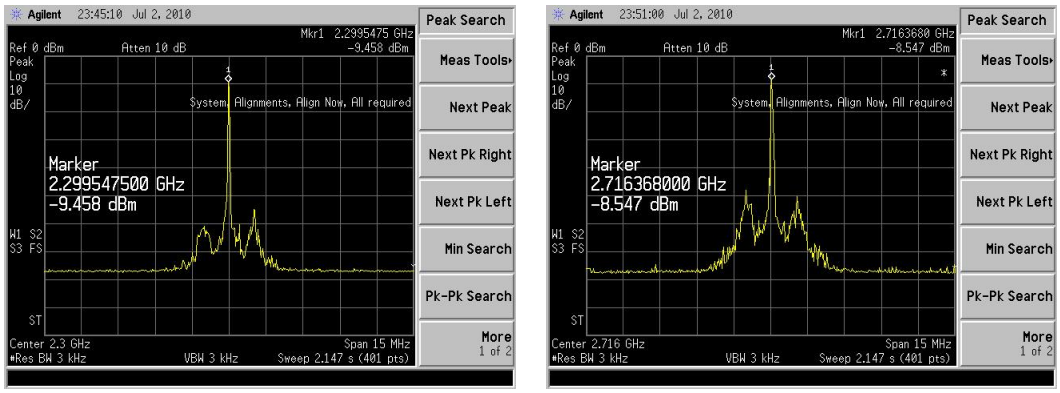
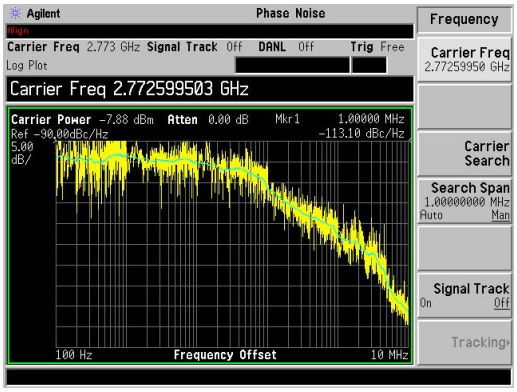


Figure 56: Oscillation frequency and gain of designed VCO

Single-ended measurements were performed for one of the differential outputs with the 50 Ω probes. Agilent's E4407B Spectrum Analyzer was used to measure both output frequency-power and phase noise performance of the VCO. Oscillation



(a) (b)



(c)

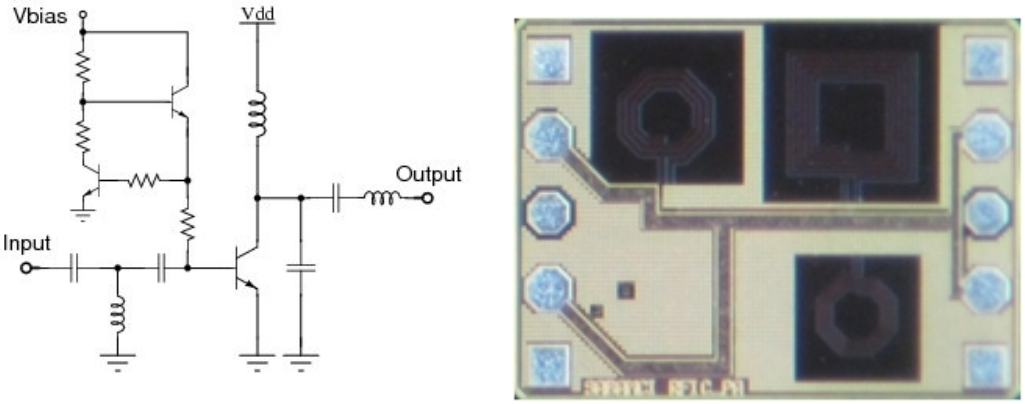
Figure 57: Measured (a) minimum oscillation frequency, (b) maximum oscillation frequency, and (c) phase noise of the proposed VCO

frequency and VCO gain of designed Linear VCO are shown in Figure 56. As results show, frequency change is almost linear with tuning voltage. VCO can be tuned between 2.29 GHz and 2.72 GHz. This frequency range corresponds to 16.7% of center frequency. Core of the VCO consumes 1.7 mA and buffers consume 4.8 mA from 1.8V supply. Power Consumption of VCO is 3.06 mW without buffer stage and 11.7 mW including buffer stage. As results indicate, most of the power is consumed by buffer stage that is implemented for measurements. In integrated platform, buffer stage will not be used, therefore lower power consumption will be aciheved. Additionally, output power varies between -9.4 dBm and -8.5 dBm. Measured Phase Noise changes from -112 dBc/Hz to -114.3 dBc/Hz.

High and low frequency spectrum are given in Figure 57(a) and 57(b). Also phase noise graphic from spectrum analyzer is also provided in Figure 57(c)

3.2 Power Amplifier Design and Measurement Results

Compared to other PA classes, Class-E PA has higher efficiency. Hence Class-E Power Amplifier was designed and fabricated using IHP 0.25 μm SiGe BiCMOS technology. Total chip area including pads in 0.75 mm^2. Aimed frequency band is ISM band with a center frequency at 2.45 GHz. Main concern of this power amplifier is high efficiency and low power consumption therefore linearity and 1-dB compression points are not primary concerns. According to post-layout simulation results, 1-dB compression point is 7.5 mW. Layout and microphotography of design



(a) (b)

Figure 58: a) Schematic b) Microphotography of Class-E Power Amplifier design

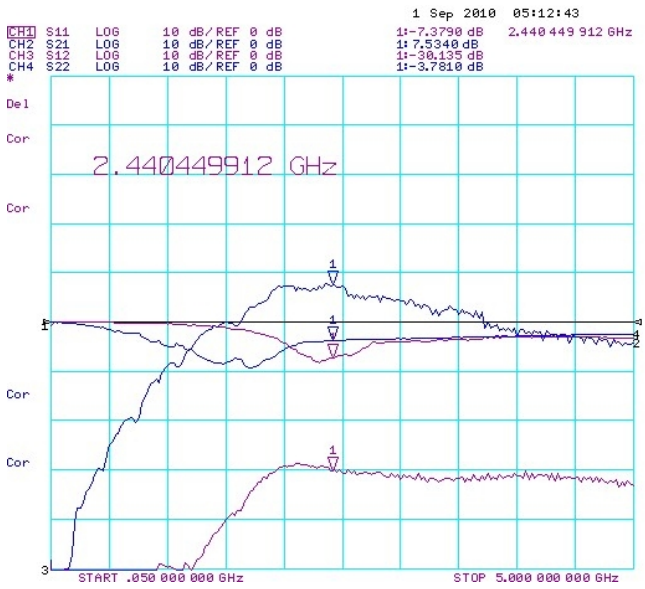


Figure 59: S-Parameter Measurement Results of Input and Output Matching of Class-E Power Amplifier

Class-E Power Amplifier is shown in Figure 58.

During measurements, both input and output terminals are connected to 50 Ω probes and network analyzer is used for analyzing Class-E PA. According to S-parameter analysis data given in Figure 59, at aimed frequency range S11 is below 10dB. That indicates that input matched well. Also S22 is around -4dB which will be enough for satisfying operation. Therefore it can be concluded that matching of the PA was done successfully.

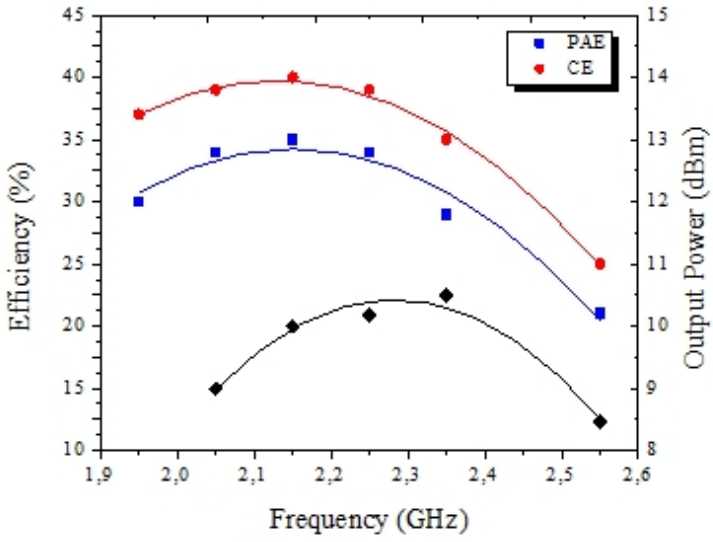


Figure 60: Post-Layout simulation results of Efficiency and Output Power graph of Class-E Power Amplifier

Even though it is stated that Class-E PA can have 100% PAE, efficiency of Class-E PA will be lower than 70% for operating frequencies larger than 2 GHz [54]. Main reason for decrease in this efficiency value is switching time. If there was an instantaneous switching, current and voltage graphs would not overlap. Therefore, efficiency would be 100% instead of lower vallues. However, switching will take time for higher frequencies and this results in overlap in current and voltage. As a result of this overlap, power loss will occur during switching and decreased PAE will be observed. As Figure 60 shows, max. achieved efficiency is 41%. Also maximum gain is 12 dB as results are shown in Figure 60.

4 Conclusion & Future Work

4.1 Summary of Work

Improvements in microtechnology and nano technology resulted in increased attention of researchers on biosensor designs. Since biosamples are mostly in micro or nano scales, miniaturized sensor development may increase the sensitivity of sensor platform.

Proposed biosensor platform aims at transmitting biological data to host device at ISM-band. System consists of transducer & Readout Blocks and Transmitter Block. IDE capacitor surface will be activated using bio-receptors and biomarkers will bind to activated surface. Due to this binding process, sensible capacitance change will occur. Capacitance change will be converted to voltage signal with Capacitance to Voltage Converter (CVC) and obtained signal will be converted to DC voltage signal via RC Low-Pass Filter. DC voltage that differs depending on the sample concentration will be applied to varactor of Voltage Controlled Oscillator (VCO) that operates at ISM band. Signal that is generated by VCO will be amplified by Class-E Power Amplifier (PA) to increase the power level of transmitted signal. I have taken main responsibility in IDE Capacitor optimization and simulations and CVC block design and simulations. Additionally I partially involved in Linear LC-Tank VCO and Class-E PA designs. In all integrated designs, IHP's 0.25μm Silicon Germanium (SiGe) BiCMOS technology was utilized because of frequency advantage of SiGe technology and IHP's opportunity for post-process. Design of transducing, readout and transmitting blocks are done. Also measurements of IDE-capacitors, VCO and PA are completed.

IDE capacitors are simulated using three different FEM tools, COMSOl, ADS Momentum and Coventorware. Each tool has different advantage therefore three of these tools are used and geometry of IDE capacitor is optimized. In the light of simulation results, gap between fingers is chosen as 2.5 μm and finger thickness is 5μm. Dimensions of optimized capacitor for IC integrated transducing is 300 μm x 370 μm.

Second block is CVC design that will convert capacitance change into voltage change. Three CVC circuits are designed for different purposes and highly linear

response to capacitance change is obtained in three designs. Initially conventional CVC circuit is designed for measuring single IDE on-chip capacitor. Working frequency of this design is between 10 kHz and 100 kHz. Also CVC design for measuring three IDE capacitors is designed and fabricated in the same tape-out. One capacitance is active for each measurement and switching between capacitors is successful as post-layout simulations indicate. Operating frequency of this design is same as first design. In these designs output signal is buffered with Source Follower stage.Dynamiz range of this design is 2.5 pF. Obtained sensitivity is 0.415 mV / fF and resolution is 24 fF assuming minimum detectable voltage signal is 10mV. Third design is varactor tunable CVC design in which reference capacitor is replaced with varactor for compensating capacitance offset after biochemical processes. For buffer block, buffer connected two stage OpAmp is used and operating frequency is improved to 10 MHz for varactor tuning CVC design. Total power consumption of Varactor Tunable CVC design including buffer stage changes between 441 μW and 1.037 mW depending on the capacitance of sensing capacitor. Varactor tunable CVC design has dynamic range, sensitivity and resolution as 450 fF, 4.5 mV / fF and 2.22 fF respectively.

Lastly, for transmitter block, linear VCO and Class-E PA are designed by my colleagues. For this application Linear VCO is designed and linear correlation between varactor tuning voltage and output frequency is obtained. For increasing the linearity of conventional LC-tank VCO, varactor bank is used in LC tank. According to measurement results output power is higher than -9.5 dBm for all frequency range, phase noise is lower than -112 dBc/Hz and frequency can be tuned between 2.29 GHz and 2.72 GHz. Class-E PA is chosen because of hig-efficiency specification. Measured output power of PA is larger that 9 dBm for operating frequency band. Measured Power Added Efficiency (PAE) is between 25% and 20%.

4.2 Future Works

Blocks have been built separately, they should be integrated to form a single platform with completing digital signal processing block. Initially VCO and PA blocks will be integrated to observe response of this transmitter block. In addition to that ADC specifications will be determined and ADC will be designed. Then

on-board signal processing unit will be completed. Later readout block, on-board signal processing unit and transmitter unit will be put on same board to form a hand-held device for Lab-on-Chip applications.

Microfluidics on IC chip are required for user-friendly interface and easier measurement. Also microfluidics will improve the life-time of biosensor since wirebonds will not be harmed by biochemical steps. In BioVCO design, bonds were prevented with non-conductive epoxy but this was not a permanent solution. Microfluidics designs are performed by our research group for stand-alone capacitors but these are not miniaturized for IC applications yet. For IC integrated microfluidics we researched and some of them are applicable to our system. First applicable microfluidics example is direct-write microfludics for LoC applications. Ink that is used as sacrifical layer is deposited on chip via micro-nozzle. Then non-conductive epoxy will be deposited on chip. After completing these fabrication steps, ink will be removed and channel will be formed on IC chip [55]. Second instance is based on depositing negative photoresist on IC chip that is glued to wider material such as wafer. This photoresist will be masked and channel will be formed using lithography steps. After forming channel, PDMS layer will be used to close the channel [56]. One of these microfluidics examples can be applied proposed LoC platform.

After integration and microfluidics are done, system will be packed as an hand-held device with buttons that enable users' control over system.

References

[1] C. R. Keese and l. Giaeve, "A biosensor that monitors cell morphology with electrical fields," *Engineering in Medicine and Biology Magazine, IEEE*, vol. 13, pp. 402–408, 1994.

[2] R. Shah, M. Gold, and R. Schaffer, "Development of a fiber optic oxygen and glucose sensor," *Engineering in Medicine and Biology Society, 1988. Proceedings of the Annual International Conference of the IEEE*, pp. 742–744, 1998.

[3] G. Rong *et al.*, "Porous Silicon Microcavity Biosensor for Rapid and Real-Time Glucose Detection," *Photonics and Optoelectronics (SOPO), 2011 Symposium*, pp. 1–4, 2011.

[4] A. LABS, "ACON Labs - Medical Diagnostic Manufacturer of Rapid Tests, Glucose Monitors, Urinalysis, and ELISA." http://www.aconlabs.com, 2010.

[5] W. H. Organization, "Cardiovascular Diseases (CVDs)." http://www.who.int/mediacentre/factsheets/fs317/en/, January 2011.

[6] T. A. Pearson *et al.*, "AHA/CDC Scientific Statement: Markers of Inflammation and Cardiovascular Disease: application to clinical and public health practice. A statement for healthcare professionals from the Centers for Disease Control and Prevention and the American Heart Association," *Circulation*, vol. 107, pp. 499–511, 2003.

[7] T. B. Ledue and N. Rifai, "Preanalytic and Analytic Sources of Variations in C-reactive Protein Measurement: Implications for Cardiovascular Disease Risk Assessment," *Clinical Chemistry*, vol. 49, pp. 1258–1271, 2003.

[8] IMEC, "BIOSENSORS AND LAB-ON-CHIP TECHNOLOGIES." http://www2.imec.be/, 2010.

[9] I. Medtronic MiniMed, "MiniMed Paradigm Revel Insulin Pump." http://www.minimed.com/products/insulinpumps/, 2011.

[10] I. Dexcom, "A Dexcom Continuous Glucose Monitoring System Is Your Guide To Diabetes Control." http://www.dexcom.com/products, 2011.

[11] A. Hassibi and T. H. Lee, "A Programmable 0.18-μm CMOS Electrochemical Sensor Microarray for Biomolecular Detection, journal = Sensors Journal, IEEE, volume= 6, issue= 6, pages = 1380–1388, year = 2006,"

[12] J. N. Kolkar, "Overview-history-types of biosensors." University Lecture, 2010.

[13] G. Medoro *et al.*, "A Lab-on-a-Chip for Cell Detection and Manipulation," *Sensors Journal, IEEE*, vol. 3, pp. 317–325, 2003.

[14] W.-Y. Chung, A. C. Paglinawan, Y.-H. Wang, and T.-T. Kuo, "A 600 μw Readout Circuit with Potentiostat for Amperometric Chemical Sensors and Glucose Meter Applications," *Electron Devices and Solid-State Circuits*, pp. 1087–1090, 2007.

[15] C. Yang *et al.*, "Amperometric Electrochemical Microsystem for a Miniaturized Protein Biosensor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, pp. 160–168, 2009.

[16] R. Sethi and C. Lowe, "Electrochemical microbiosensors," *Sensors Journal, IEEE*, pp. 9/1–9/5, 1990.

[17] M. Hnaien *et al.*, "A conductometric biosensor for the estimation of the number of cleaving sites in peptides and proteins," *Electrochemistry Communications*, vol. 11, pp. 165–168, 2009.

[18] N. Jaffrezic-Renault and S. V. Dzyadevych, "Conductometric Microbiosensors for Environmental Monitoring," *Sensors 2008*, vol. 8, pp. 2569–2588, 2008.

[19] S. Dzyadevych *et al.*, "Conductometric formaldehyde sensitive biosensor with specifically adapted analytical characteristics," *Analytica Chimica Acta*, vol. 445, pp. 47–55, 2001.

[20] A. Hassibi and T. H. Lee, "A coil-type capacitive sensor for measurement of the deterioration of engine oil," *Precision Electromagnetic Measurements, 2002. Conference Digest 2002 Conference*, pp. 184–185, 2002.

[21] S.-W. Wang and M. S.-C. Lu, "CMOS Capacitive Sensors With Sub- μm Microelectrodes for Biosensing Applications," *Sensors Journal, IEEE*, vol. 10, pp. 991–996, 2010.

[22] X. Huang *et al.*, "A Capacitive MEMS Viscometric Sensor for Affinity Detection of Glucose," *Journal of Microelectromechanical Systems*, vol. 18, pp. 1246–1254, 2009.

[23] S. B. Prakash and P. Abshire, "On-Chip Capacitance Sensing for Cell Monitoring Applications," *Sensors Journal, IEEE*, vol. 7, pp. 440–447, 2007.

[24] B. Jang and A. Hassibi, "Biosensor systems in standard CMOS processes: Fact or fiction?," *Industrial Electronics, 2008. ISIE 2008. IEEE International Symposium*, pp. 2045–2050, 2008.

[25] Y. Huang *et al.*, "Post-CMOS Compatible Microfabrication of a Multi-Analyte Bioelectrochemical Sensor Array Microsystem," *Sensors, 2006. 5th IEEE Conference*, pp. 612–615, 2006.

[26] J. Zhang *et al.*, "Electrochemical array microsystem with integrated potentiostat," *Sensors, 2005 IEEE*, pp. 385–388, 2005.

[27] L. Li *et al.*, "1.5 V Sub-mW CMOS Interface Circuit for Capacitive Sensor Applications in Ubiquitous Sensor Networks," *ETRI Journal*, vol. 30, pp. 644–652, 2008.

[28] M. S.-C. Lu, Y.-C. Chen, and P.-C. Huang, "5x5 CMOS capacitive sensor array for detection of the neurotransmitter dopamine," *Biosensors and Bioelectronics*, vol. 26, pp. 1093–1097, 2010.

[29] S. Lee, W. Qureshi, X. Liu, and A. Mason, "Amperometric instrumentation system with on-chip electrode array for biosensor application," *Biomedical Circuits and Systems Conference (BioCAS)*, pp. 294–297, 2010.

[30] P. Bruschi, N. Nizza, and M. Dei, "A low-power capacitance to pulse width converter for MEMS interfacing," *Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European*, pp. 446–449, 2008.

[31] Y. Bin Abd Manaf, A.and Matsumoto, "Low voltage charge-balanced capacitance–voltage conversion circuit for one-side-electrode-type fluid-based inclination sensor," *Solid-State Electronics*, vol. 53, pp. 63–69, 2008.

[32] J. Wu, G. Fedder, and L. Carley, "A low-noise low-offset capacitive sensing amplifier for a 50-$\mu g/\sqrt{Hz}$ monolithic CMOS MEMS accelerometer," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 722–730, 2004.

[33] J. Chen *et al.*, "An on-chip, interconnect capacitance characterization method with sub-femto-farad resolution," *Microelectronic Test Structures, 1997. ICMTS 1997*, pp. 77–80, 1997.

[34] T. Evans, I.and York, "Microelectronic capacitance transducer for particle detection," *Sensors Journal, IEEE*, vol. 4, pp. 364–372, 2004.

[35] C.-T. Chiang and Y.-C. Huang, "A Low-Cost CMOS Integrated Sensor Transducer Implemented as a Capacitance-to-Frequency Converter for Capacitive Measuring," *Instrumentation and Measurement Technology Conference Proceedings*, pp. 1–4, 2007.

[36] E. Ghafar-Zadeh and M. Sawan, "A CMOS-Based Capacitive Sensor for Laboratory-On-Chips: Design and Experimental Results," *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium*, pp. 85–88, 2007.

[37] L. Oliveira *et al.*, "Experimental Evaluation of Phase-Noise and Quadrature Error in a CMOS 2.4 GHz Relaxation Oscillator," *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium*, pp. 1461–1464, 2007.

[38] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 331–343, 1997.

[39] S. Kurachi, T. Yoshimasu, and K. Itoh, N.and Yonemura, "5-GHz Band Highly Linear VCO IC with a Novel Resonant Circuit," *Silicon Monolithic Integrated Circuits in RF Systems, 2007 Topical Meeting*, pp. 285–288, 2007.

[40] S. Muthukrishnan, J. Zhao, G. Studtmann, and S. Raman, "An ESD protected RFIC power amplifier design," *Radio Frequency integrated Circuits RFIC Symposium, 2005*, pp. 605–607, 2005.

[41] M. Kaynak, M. Uzunkol, b. Tekin, and Y. Gürbüz, "Performance comparison of a single and multiband power amplifiers using IHP 0.25 μm SiGe HBT technology," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 19, pp. 434–442, 2009.

[42] A. Qureshi, J. H. Niazi, S. Kallempudi, and Y. Gurbuz, "Label-Free Capacitive Biosensor for Sensitive Detection of Multiple Biomarkers Using Gold Interdigitated Capacitor Arrays," *Biosensors and Bioelectronics*, vol. 25, pp. 2318–2323, 2010.

[43] F. Taşdemir *et al.*, "A new Lab-on-Chip transmitter for the detection of proteins using RNA aptamers," *Microwave Conference (EuMC), 2010 European*, pp. 489–493, 2010.

[44] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits-Analysis and Design*, pp. 245–249. McGraw-Hill higher Education, third ed., 2003.

[45] E. Ghafar-Zadeh and M. Sawan, "High accuracy differential capacitive circuit for bioparticles sensing applications," *Circuits and Systems, 2007. MWSCAS 2007. 50th Midwest Symposium*, pp. 193–196, 2007.

[46] P. D.-I. F. Gustrau, "EMDS for ADS Momentum." `http://www.home.agilent.com/`, 2009.

[47] E. Ghafar-Zadeh, M. Sawan, and D. Therriault, "Novel direct-write CMOS-based laboratory-on-chip: Design, assembly and experimental results," *Sensors and Actuators*, vol. 134, pp. 27–35, 2007.

[48] E. Ghafar-Zadeh, M. Sawan, M. Hajj-Hassan, and M. Miled, "A CMOS based microfluidic detector: Design, calibration and experimental results," *Circuits and Systems. 48th Midwest Symposium*, pp. 1362–1365, 2007.

[49] S. A. Smith and K. C. Smith, *Microelectronic Circuits*, pp. 315–318. Oxford, New York: Oxford University Press, 2004.

[50] X. Fan and P. Chan, "Analysis and Design of Low-Distortion CMOS Source Followers," *Circuits and Systems I: Regular Papers, IEEE Transactions*, vol. 52, pp. 1489–1501, 2005.

[51] S. Lichun, M. Palaniapan, and T. W. Wan, "A continuous-time capacitance to voltage converter for microcapacitive pressure sensors," *Journal of Physics: Conference Series 34*, vol. 34, pp. 1014–1019, 2006.

[52] Z. Chong, W. Qisong, Y. Tao, and Y. Haigang, "Noise and mismatch optimization for capacitive MEMS readout," *Journal of Semiconductors*, vol. 30, pp. 115003–1–115003–6, 2009.

[53] "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: Higher-speed Physical Layer Extension in the 2.4-GHz Band, IEEE std. 802.11b, Part 11, ," 1999.

[54] D. Lie *et al.*, "Highly Efficient Monolithic Class E SiGe Power Amplifier Design at 900 and 2400 MHz," *Circuits and Systems I: Regular Papers*, vol. 56, pp. 1455–1466, 2009.

[55] E. Ghafar-Zadeh *et al.*, "A direct-write microfluidic fabrication process for CMOS-basedLab-on-Chip applications," *Microelectronic Engineering*, vol. 86, pp. 2104–2109, 2009.

[56] Y. Liu, H. Lee, R. Westervelt, and D. Ham, "IC/Microfluidic Hybrid System for Biology: Review," *Bipolar/BiCMOS Circuits and Technology Meeting, 2005*, pp. 174–179, 2005.