SiGe BiCMOS Front-end Integrated Circuits for X-Band Phased Arrays

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SiGe BiCMOS Front-end Integrated Circuits for X-Band Phased Arrays

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Keywords: Phased Arrays, T/R module, SiGe BiCMOS, X-Band Integrated Circuits, Low Noise Amplifier, T/R Switch and SPDT Switch.

Abstract

The current Transmit/Receive (T/R) modules have typically been implemented using GaAs- and InP-based discrete monolithic microwave integrated circuits (MMIC) to meet the high performance requirement of the present X-Band phased arrays. However their cost, size, weight, power consumption and complexity restrict phased array technology only to certain military and satellite applications which can tolerate these limitations. Therefore, next generation X-Band phased array radar systems aim to use low cost, silicon-based fully integrated T/R modules. For this purpose, this thesis explores the design of T/R module front-end building blocks based on new approaches and techniques which can pave the way for implementation of fully integrated X-Band phased arrays in low-cost SiGe BiCMOS process.

The design of a series-shunt CMOS T/R switch with the highest IP_{1dB}, compared to other reported works in the literature is presented. The design focuses on the techniques, primarily, to achieve higher power handling capability (IP_{1dB}), along with higher isolation and better insertion loss of the T/R switch. Also, a new T/R switch was implemented using shunt NMOS transistors and slow-wave quarter wavelength transmission lines. It presents the utilization of slow-wave transmissions lines in T/R switches for the first time in any BiCMOS technology to the date. A fully integrated DC to 20 GHz SPDT switch based on series-shunt topology was demonstrated. The resistive body floating and on-chip impedance transformation networks (ITN) were used to improve power handling of the switch.

An X-Band high performance low noise amplifier (LNA) was implemented in 0.25 μm SiGe BiCMOS process. The LNA consists of inductively degenerated two cascode stages with high speed SiGe HBT devices to achieve low noise figure (NF), high gain and good matching at the input and output, simultaneously. The performance parameters of the LNA collectively constitute the best Figure-of-Merit value reported in similar technologies, to the best of author's knowledge. Furthermore, a switched LNA was implemented SiGe BiCMOS process for the first time at X-Band. The resistive body floating technique was incorporated in switched LNA design, for the first time, to improve the linearity of the circuit further in bypass mode.

Finally, a complete T/R module with a state-of-the-art performance was implemented using the individually designed blocks. The simulations results of the T/R module is presented in the dissertation. The state-of-the-art performances of the presented building blocks and the complete module are attributed to the unique design methodologies and techniques.

X-Band Faz Dizinleri için SiGe BiCMOS Ön Uç Devreleri

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Özet

Günümüzde X-Band faz dizinlerinin yüksek performans gereksinimi karşılamak için alıcı-verici (T/R) modülleri genellikle GaAS, InP temelli tektaş mikrodalga tümdevreler kullanılarak gerçeklenmektedir. Ancak III-V yarı iletken teknolojisine dayanan bu modüllerin maliyeti, boyutu, ağırlığı, güç tüketimi ve karmaşıklığı faz dizini teknolojisinin kullanımını sadece bunlara musamaha gösterebilen askeri ve uzay uygulamalarıyla sınırlamaktadır. Bu kısıtlamayı, gelecek nesil X-Band faz dizinli radar sistemleri düşük maliyetli, silikon tabanlı entegre T/R mödülleri kullanarak aşmayı amaçlamaktadır. Bu amaçla, bu tez düşük maliyetli SiGe BiCMOS prosesinde tamamen entegre X-Band faz dizinlerinin gerçeklenmesine katkıda bulunacak yeni yaklaşım ve tekniklere dayalı T/R modül ön uç bloklarının tasarımını inceleyecektir.

Literatürdeki diğer çalışmalar ile karşılaştırıldığında en yüksek IP1dB değerine sahip seri-paralel CMOS T/R anahtarının tasarımı sunulmaktadır. Tasarım daha yüksek izolasyon ve daha iyi ekleme kaybı elde etme tekniklerinin yanında özellikle daha yüksek güce dayanıklılık elde etme teknikleri üzerinde odaklanmaktadır. Ayrıca, paralel NMOS tranzistörler ve dalga yavaşlatan çeyrek dalga boyundaki iletim hatları kullanılarak yeni bir T/R anahtarı tasarlanmıştır. Şu ana kadarki tüm BiCMOS teknolojileri göz önüne alındığında, dalga yavaşlatan iletim hatlarının T/R anahtarında kullanımı ilk defa sunulmaktadır. Ek olarak, seri-paralel topolojisine dayalı DC-20 GHz tek giriş çift çıkış (SPDT) anahtarı gösterilmiştir.

X-Band yüksek performans bir düşük güç kuvvetlendiricisi (LNA) 0.25 μm SiGe BiCMOS prosesinde gerçeklenmiştir. LNA aynı anda düşük gürültü figürü, yüksek kazanç ve giriş ve çıkışlarda güzel uydurma elde etmek için endüktif olarak dejenere edilmiş ve yüksek hızlı SiGe HBT kullanan iki kaskot katından oluşmaktadır. Yazarın bilgisine göre, LNA'in toplu olarak performans parametreleri benzer teknolojilerde yayınlanan başarım ölçütleri arasında en iyisidir. Buna ek olarak, yazarın bilgisi dahilinde X-Band'ta çalışan anahtarlamalı bir LNA SiGe BiCMOS teknolojisinde ilk defa uygulanmıştır. Dirençsel gövde dalgalandırma tekniği baypas modunda devrenin doğrusallığını arttırmak için ilk defa anahtarlamalı LNA tasarımına dahil edilmiştir.

Son olarak, teker teker tasarlanan bloklar kullanılarak teknolojinin geldiği son nokta bir performansa sahip T/R modül bütün olarak entegre edilmiştir. T/R modülün benzetim sonuçları tezde sunulmaktadır. Teker teker sunulan yapı bloklarının ve bütün T/R modülünün en son teknoloji performansı özgün tasarım metodlarına ve tekniklerine atfedilmektedir.

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List of Abbreviations

AF	Array Factor
AM	Amplitude Modulation
ANT	Antenna
BV_{CEO}	Collector-Emitter Breakdown Voltage
BV_{CBO}	Collector-Base Breakdown Voltage
CMOS	Complementary Metal Oxide Semiconductor
EIRP	Equivalent Isotropically Radiated Power
FOM	Figure-of-Merit
GaAs	Gallium-Arsenide
HBT	Heterojunction Bipolar Transistors
IC	Integrated Circuit
IL	Insertion Loss
IIP3	Input Third-order Intercept Point
InP	Indium phosphide
ITN	Impedance Transformation Network
iNMOS	Isolated NMOS
LNA	Low Noise Amplifier
MEMS	Microelectromechanical System
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuits
mm-Wave	Millimeter-wave
MOS	Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
PA	Power Amplifier
PAE	Power-Added-Efficiency
PS	Phase Shifter
Q	Quality Factor
RADAR	Radio Detecting And Ranging
RF	Radio Frequency
RX	Receiver
SiGe	Silicon-Germanium
SiO_2	Silicon Dioxide
S-MSL	Slow-wave Microstrip Transmission Line
SPDT	Single-Pole Double-Throw
T/R	Transmit/Receive
TX	Transmitter
TWT	Traveling Wave Tubes
UWB	Ultra Wide Band
VGA	Variable Gain Amplifier
V_{GS}	Gate-to-Channel Voltage
WWII	World War II

1 Introduction

1.1 An Overview of Radar History

The history of the radar, RAdio Detecting and Ranging, systems which can both detect and provide the range information of the potential objectives by using radio waves starts with World War II (WWII). The early radar systems during WWII consisted of fixed antennas driven with high power electro-magnetic devices called magnetrons which were capable of producing high power microwave pulses and determined the echoes reflected from targets [1].

The importance of detection and ranging became indispensable during and after WWII so that radars have gradually evolved into more complex and multi-functional systems since then. During this evolution, first the conventional mechanically steerable antennas with hundreds of scans per minute have been developed to increase the visible area of the radar systems. Eventually the electrically steerable radar systems which were capable of hundreds of scans per second over wide monitoring angles were introduced. These systems are more commonly known as phased arrays or beem-forming arrays [2].

As the radar systems have advanced with the development in phased array technology, so have the application areas. Although radar systems continued to be predominantly used for military and satellite applications, they have also spread into commercial applications such as vehicular collision avoidance [3], weather monitoring [4], and presence detection for smart houses [5]. The spread of the phased arrays has come true with everlasting trend of pushing for smaller, more solid state solutions with an ultimate goal of integrating all the front-end circuits on a single chip [6].

1.2 Phased Array Principle

Phased arrays have been proposed in 1950's and widely used to achieve electronic beam forming and scanning much faster than mechanically steerable systems [7–9]. Phased arrays can be used either on the transmitter or receiver side, or in transceivers.

The phased arrays consist of thousands of antenna elements spaced at the frac-

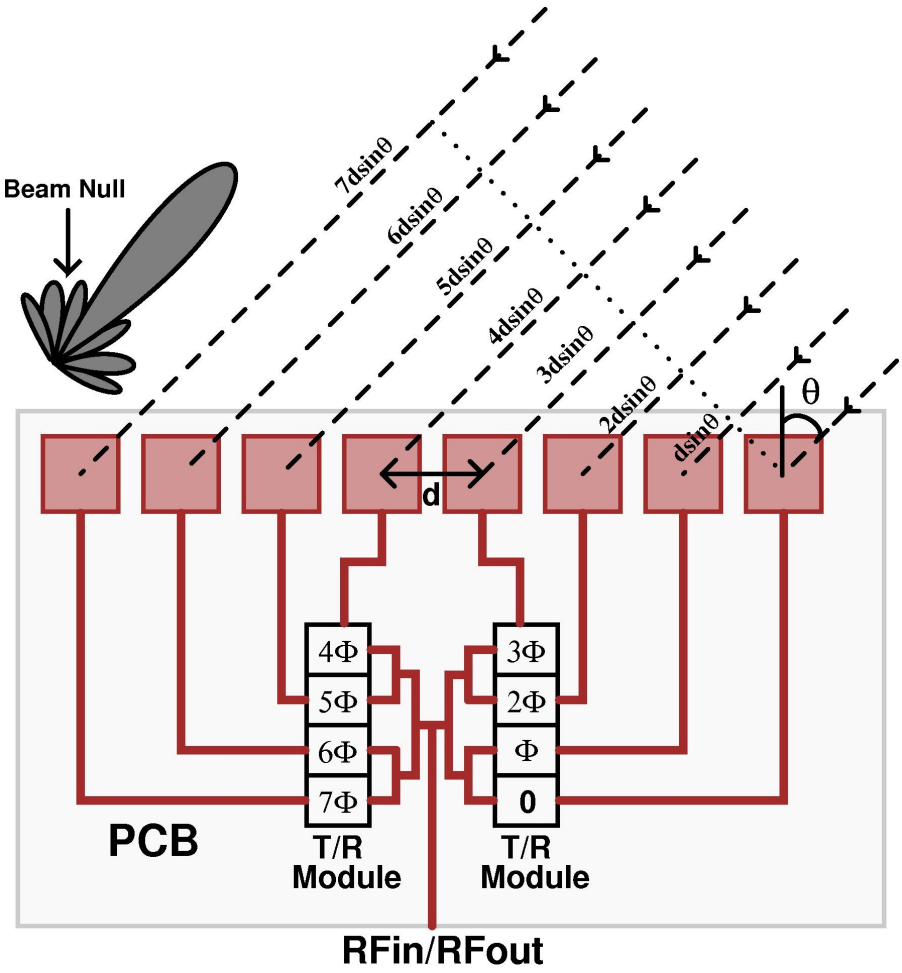

Figure 1: Phased array system with 8 antenna elements

tional wavelength of the operation in typically two dimensions to steer overall antenna beam electronically. The amplitude and phase of the signals feeding each element are varied so that the effective radiation pattern and gain of the array is reinforced in a desired direction and suppressed in other directions [10]. This property of phased arrays is widely used for addressing the emerging requirements of military radar systems for detecting incoming airplanes or missiles and satellite communications. On the transmitter side, phased array focuses the beam at a desired direction while on the receiver side focuses on the desired signal while alleviating interferences from other directions.

Fig. 1 shows a basic concept of phased arrays with linearly arranged 8 antenna elements. In this system, the length of the transmission lines can be arranged so that the phase introduced by them is equal to multiple of 2π to provide a progressive phase difference of Φ between antennas. Another way of doing this is compensating

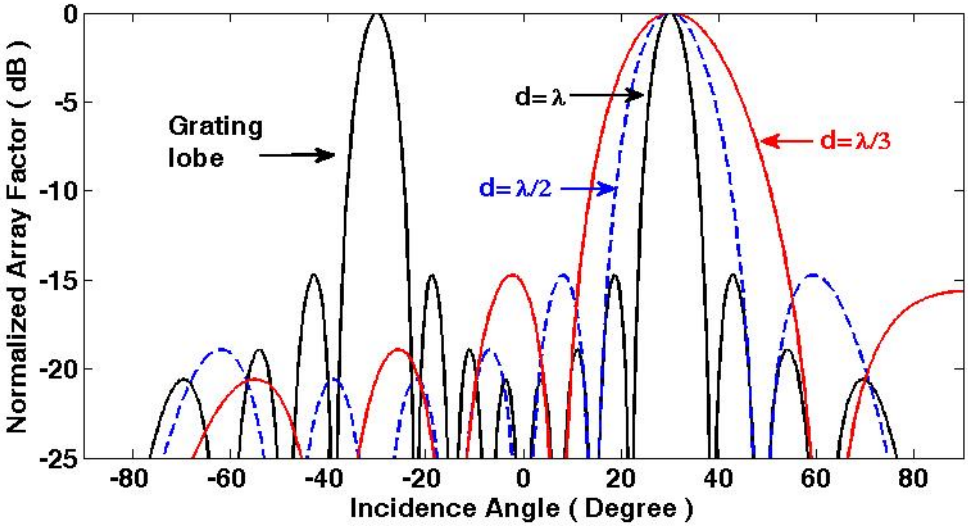

Figure 2: Normalized array factor of a 8-element phased array with three different antenna spacing

for phase differences introduced by the antenna feeds in T/R module. In a linear array similar to shown in Fig. 1, in receive mode, the phase difference between signals that arrive in adjacent antenna elements is given by

$$\phi_\Delta = \frac{2\pi}{\lambda} d \sin\theta \tag{1}$$

where λ is the wavelength, d is the spacing between antennas, and θ is the incidence angle. When a progressive phase difference of Φ is introduced at antenna elements by phase shifters in T/R modules, the direction of antenna beam can be changed to

$$\theta = \sin^{-1} \frac{\lambda}{2\pi d} \Phi \tag{2}$$

The radiation pattern of an antenna array, as can be seen on the left side in Fig. 1, is given by the multiplication of a single antenna element pattern with a factor which is known as array factor (AF) [11]. The normalized array factor of a progressively excited, equally spaced linear array is calculated as

$$f(\psi) = \frac{\sin(N\psi/2)}{N \sin(\psi/2)} \tag{3}$$

where ψ is $\beta \mathrm{d} \sin\theta + \Phi$. Fig. 2 shows the normalized array factor of a 8-element

phased array with different antenna spacing. As can be seen, increasing the spacing between antenna elements decreases the main beam width and thus improves the performance of the array. However, increasing spacing more than $\lambda/2$ may introduce grating lobes which makes system more vulnerable to interference from other directions. Therefore, it is common practice to set the spacing between antenna elements to $\lambda/2$ to achieve a high directivity without creating any grating lobes.

Phased arrays do not only steer the radiation pattern electronically and suppress the interferences from other directions, they also improve the overall signal-to-noise (SNR) at the output of the receiver and hence provides better sensitivity at the receiver [12]. This merit of the phased arrays arises from the fact that signals from the antenna add coherently while the noise generated in each receive path adds incoherently, given that the distance between successive antennas is large enough [13], [14]. On the transmitter side, the coherent addition of the signals increases the radiated power in the main beam direction while creating less interference to nearby communication channels. Hence, assuming an n-element phased array transmitter where each element is radiating P_e watts omni directionally, in the main beam direction the Effective Isotropic Radiated Power (EIRP) will be n^2P_e watts or P_e(dBm)+20log(n) dBm. Considering the 8-element phased array in Fig. 1, if each antenna is radiating 20 dBm, the EIRP is 20+18 dBm. This merit of the phased arrays is really beneficial at microwave/mm-wave frequencies, especially in silicon-based technologies since the output power of power amplifiers is limited due to the low breakdown voltages of the devices and lossy substrates. On the receiver side, the combined signal output is given by

$$S_{out} = n^2 G S_{in} \tag{4}$$

where n is the number of antenna elements, G is the total gain in a single receive path and S_{in} is the input signal. Assuming that antenna noise in different receive paths are uncorrelated, total noise power at the output is given by

$$N_{out-array} = n(N_i + N_{added})G \tag{5}$$

where N_i is the input noise from feeding antenna and N_{added} is the noise power added

by the receiver network. SNR at the output is given by

$$SNR_{out-array} = \frac{S_{out-array}}{N_{out-array}} = \frac{nS_{in}}{N_i + N_{added}} \tag{6}$$

For a single receiver channel the signal and the noise power at the output would be

$$S_{out} = GS_{in} \tag{7}$$

$$N_{out} = (N_i + N_{added})G \tag{8}$$

Thus signal-to-noise ratio at the output of a single receiver would be

$$SNR_{out} = \frac{S_{out}}{N_{out}} = \frac{S_{in}}{N_i + N_{added}} \tag{9}$$

Eventually dividing (6) by (9) it is found that an n-element phased array can improve the SNR at the output of the receiver by 10log(n) dB. For instance, in an 8-element phased array SNR can be improved by 10log(8)=9 dB. A better SNR results in several improvements in radar such as rapid beam forming, accurate target location and ability to perform multiple functions at the same frequency [15].

1.3 Phased Array Systems

Phased array systems can be divided into two main types according to how the antenna elements are driven; passive phased arrays and active phase arrays. The block diagram of a passive phased array radar is shown in Fig. 3. As can be seen, passive phased array radars drive multiple antennas, a sub array of phase shifters and antennas, on transmit mode using high-power tubes such as magnetrons, Traveling Wave Tubes (TWT), Klystrons and Gyrotrons. Similarly, in the receive mode, multiple phase shifters drive a single high performance LNA. The passive phased arrays were early detection system of choice for military applications such as scanning rapidly for single or multiple enemy targets, assisting with missile defense and guidance systems [16]. The most eminent ground based passive phased array radar is Patriot that is widely used during the Gulf War in 1990s [17]. Unlike passive systems, in active phased array radars each antenna element has its own dedicated solid state transmit/receive module as shown in Fig. 4. Photos of a passive and

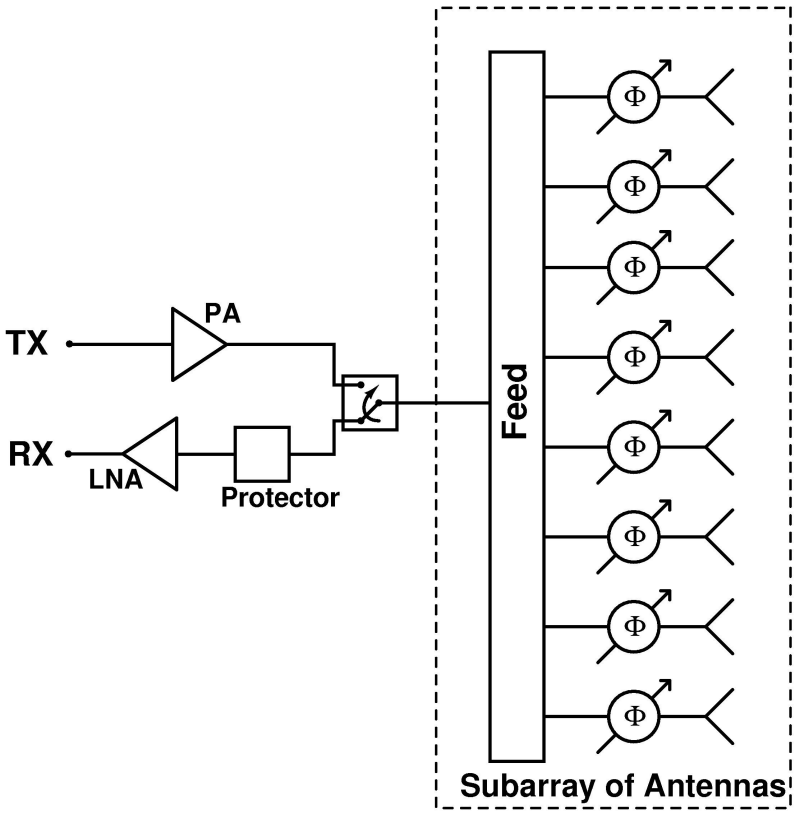

Figure 3: Simple block diagram of a passive phased array radar.

active phased array radars is shown in Fig. 5. Both passive and active phased array radars has several advantages like offering excellent beam agility, mechanical reliability due to lacking moving parts and smaller radar cross section over the conventional mechanically steerable radars [18].

An active phased arrays offers several advantages over passive arrays so that they are usually more favorable. As can be seen in Fig. 3, in passive phased array phase shifter, which is typically lossy due to implementation by passive components, comes right after antenna and degrades the overall noise figure of the system in receive mode [19]. Similarly, phase shifter comes after power amplifier and right before the radiating element in transmit mode and this increases the transmit loss and in return degrades the transmit efficiency of the overall system. Conversely, active phased arrays, offer inherently lower overall system noise figures since a low noise amplifier comes right after antenna along with a low loss T/R switch. Furthermore, in passive phase arrays, performance requirements for phase shifters are more stringent compared to active phased arrays since they should be able to handle relatively high transmit signals coming from power amplifier. In addition, passive systems are

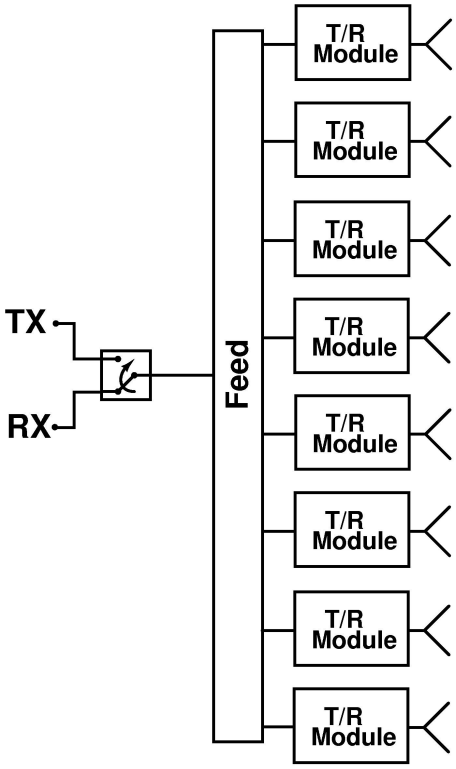

Figure 4: Simple block diagram of an active phased array radar.

more vulnerable from the reliability standpoint since a sub array of antenna element would be directly affected by a failure in PA or LNA. For instance, in Patriot a sub array of 16 antenna elements are driven by a single PA and LNA and a failure in either amplifier would take out the contributions from 16 antenna elements [20]. Contrary to Patriot, Terminal High Altitude Area Defense (THAAD) system is comprised of five times more radiating elements [21], but each antenna element has its own dedicated solid state T/R module. Therefore, a failure in either PA or LNA would has an effect on only a single antenna in contrary to sixteen antennas of Patriot and in return reliability of the overall system is improved. The active phased array architecture, also relaxes the required output power per amplifier as well as power handling requirement of the phase shifters by driving only a single antenna rather than being distributed over multiple radiating elements. Thus, high power tube devices with hundreds of kilowatts output power in passive arrays are no longer required and actually are replaced by relatively lower power monolithic microwave integrated circuits (MMIC) in the T/R modules of active arrays. Table 1 summarizes the pros and cons of the radar architectures.

Fig. 6 shows a simple block diagram of a typical T/R module in active phased

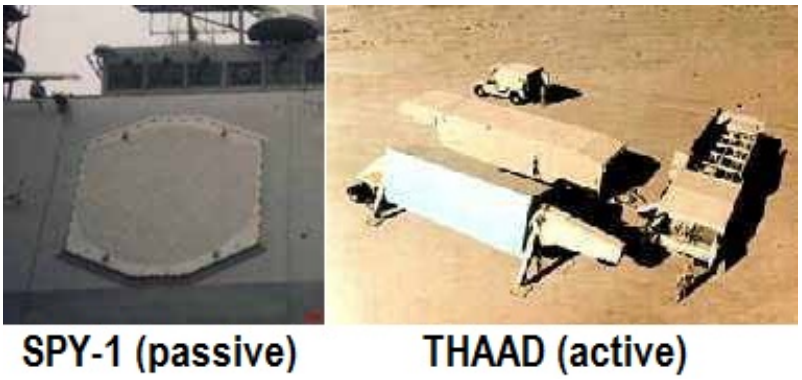

Figure 5: Photograph of a passive and active phased array radar

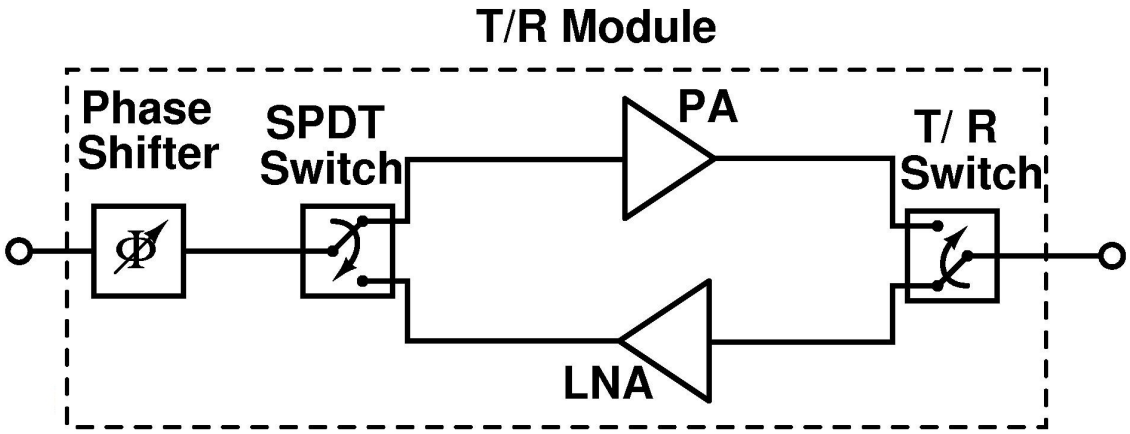

Figure 6: Simple block diagram of a solid state T/R Module

Table 1: Comparison of the Radar Architectures.

	Dish Antenna (mechanical steering)	Passive Phased Array	Active Phased Array
Pros	Very low cost Frequency diversity	Beam agility Effective resource management	Highest performance Effective resource management Low distribution loss
Cons	Slow scan rate High distribution loss Single point of failure	High distribution loss Higher cost Moderate reliability	Highest cost

array radars which consist of a T/R switch or a circulator, an LNA, a PA, an SPDT switch and a phased shifter. The performances of the current, active, phased array radar systems are mainly determined by the performance of transmit/receive (T/R) modules. The current T/R modules have typically been implemented using GaAs- and InP-based discrete monolithic microwave integrated circuits (MMIC), especially at X-Band and higher frequencies. Fig. 7 shows an example of such a module based

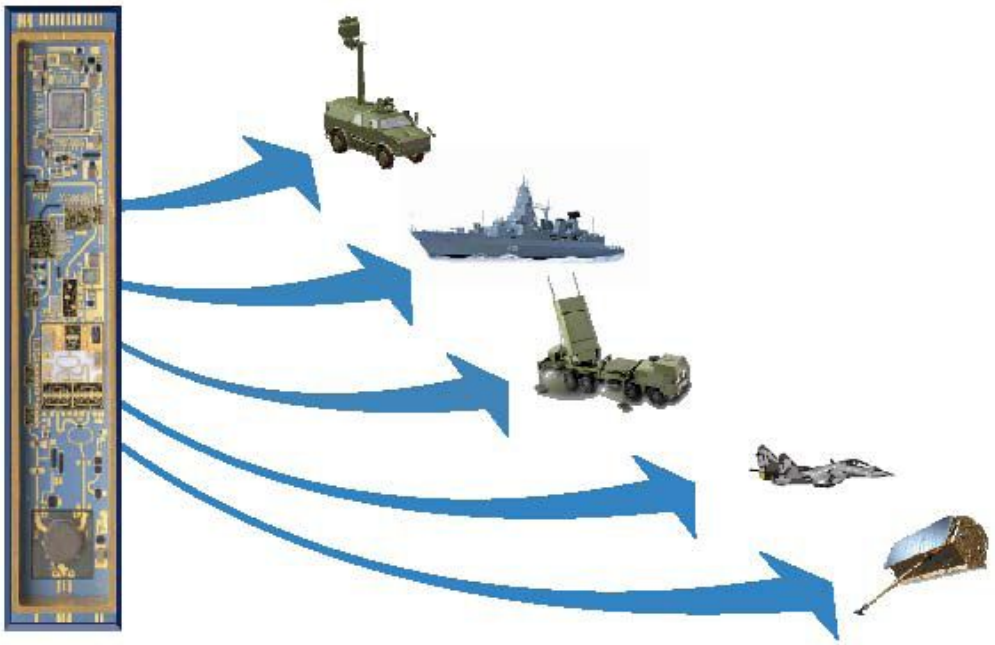

Figure 7: A III-V based T/R Module in different platforms [23].

on assembling III-V MMICs in different platforms. These III-V technologies completely meet high speed performance, especially lower noise, requirements of the present phased array radars. However, the extremely good performance of III-V compound semiconductors comes at the expense of relatively higher manufacturing cost, higher power consumption and lower integration density, resulting in higher deployment and operational expenses for X-Band phased array radars [22]. Therefore, low-cost, weight, size and highly integrated T/R modules for future phased array radar systems are required to decrease all these expenses.

1.4 Downsizing of T/R Modules

The performance of phased array radar systems are determined by using several figure-of-merits for search, track and track accuracy. Among these, the maximum range R_{MAX} in which a radar system can successfully detect and track a target is the fundamental FOM for radar systems. R_{MAX} can be calculated as

$$R_{MAX} = \left(\frac{P_t G A_e \sigma}{(4\pi)^2 S_{min}} \right)^{1/4} \tag{10}$$

where P_t is the transmitted power, G is the transmitting gain, A_e is the aperture, effective area, of the antenna, S_{min} is the minimum detectable signal, and σ is the radar cross section of the target [15]. The power-aperture-gain product for track, is another figure-of-merit which is widely used to evaluate the performance of the radar systems and can be expressed as

$$FOM_{track} = P_t A_e G \tag{11}$$

As can be seen from (10) and (11), once the operation frequency of the phased array is specified, a given system performance can only be achieved by changing the radiated power, sensitivity of the system and effective aperture area. In active phased array radars, the power, effective aperture area and the transmitting gain of the entire array can be redefined in terms of individual antenna element parameters as [24]

$$P = P_e N \tag{12}$$

$$Ae = A_{es} N \tag{13}$$

$$G = G_e N \approx \frac{4\pi A_e}{\lambda^2} N \tag{14}$$

where P_e is the radiated power per element, A_{es} is the equivalent area of a single antenna element, G_e is the gain of a single antenna element, λ is the wavelength of the frequency of operation and N is the number of antenna elements in the phased array. The track FOM for an active phased array can then be expressed as

$$FOM_{track} = \frac{4\pi P_t {A_e}^2}{\lambda^2} \approx N^3 \frac{4\pi P_e A_{es}^2}{\lambda^2} \tag{15}$$

Hence, improvements in the active phased arrays can be achieved by either increasing the radiated power per element P_e, aperture of a single element A_{es}, or the number of antenna elements N. Increasing P_e and A_e provides a linear and squared increase in the track figure of merit, respectively. However, increasing radiated power per element will increase the heat generation and require better cooling systems which in return increase the deployment and operational expenses of the radar. Similarly, increasing the elemental aperture is not an attractive approach since it may degrade the steering ability of the phased array by introducing grating

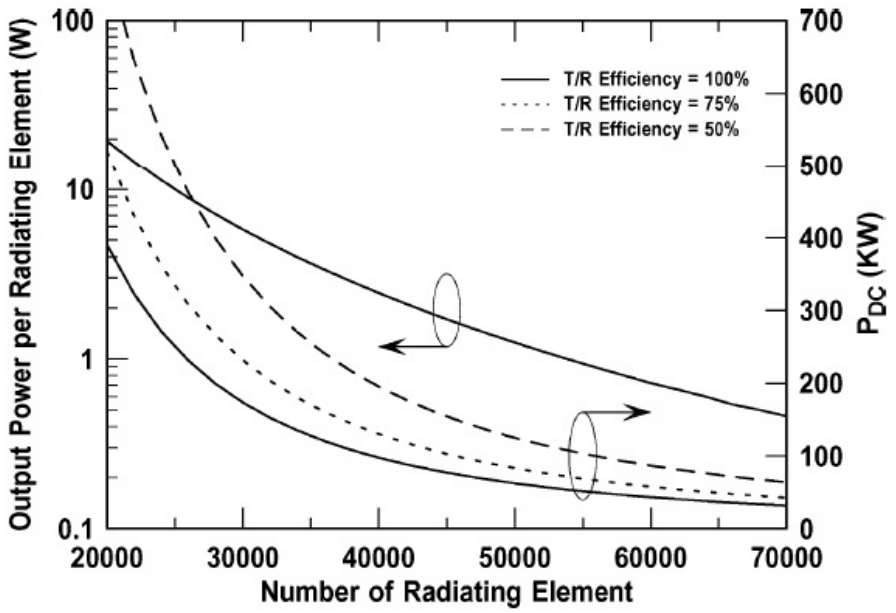

Figure 8: Output power per radiating element and total DC power required for all of the T/R modules versus number of elements for a fixed power-aperture-gain product [24].

lobes.

On the other hand, increasing number of antenna elements, T/R modules, provides a cubic improvement in the track figure of merit. Additionally, for a given power-aperture-gain product the radiated power per element P_e can be reduced drastically, at the expense of a modest increase in the number of radiating elements N [24]. However, P_e can not be decreased to an arbitrarily small value as can be seen in Fig. 8 and a radiated power of 0.4-0.5 Watts per element is optimal. This reduction in elemental power will also allow a lower DC power for the complete system, as seen in Fig. 8. Another benefit is decreasing deployment and operational expenses by the reduction in raw materials and equipments needed to transport, power and cool the system. Based on this concept, moving toward a low-power density radar system which includes tens of thousands of single-chip T/R modules (costing $<$ \$ 10 each) can significantly reduce the cost of the next generation phased array radars [25].

To implement this new low-power density radar systems, a lower-cost technology with higher integration potential capabilities are needed to be used for the T/R module design. The current T/R modules need relatively high output powers (>5W) so that they require a III-V solution. However, a SiGe BiCMOS is a more viable

and cost-effective solution for next generation low-power density T/R modules than III-V Technologies for increasing cost savings and integration capabilities.

1.5 SiGe HBT Technology

With the recent advancements in SiGe heterojunction bipolar transistor (HBT) technology, it is possible to implement low-cost microwave and mm-wave systems on a single chip. Although the idea of using SiGe alloys to practice bandgap engineering in silicon dates back to the 1960's, the first functional SiGe HBT was demonstrated only twenty five years ago [26]. Since the first SiGe HBT demonstration, SiGe HBT technology has shown an incredible improvement in terms of performance.

In SiGe HBT technology, Ge which has a smaller bandgap of 0.66 eV compared to that of Si, 1.12 eV, is introduced into the base of transistor to tailor the device performance. The introduction of Ge results in improvements in main performance parameters of the transistor such as current gain (β), base transit time (τ_b), cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) which foster high frequency operation. The improvements are better illustrated on an energy band diagram of a typical SiGe HBT. As seen in Fig. 9, in a typical SiGe HBT, the Ge content is not constant but linearly graded from emitter-base (EB) junction to collector-base junction and thus induces a decreasing bandgap in the direction of electron flow. The content of Ge at EB junction lowers the potential barrier and in return increases the electron injection into the base exponentially for a given applied base-emitter voltage (V_{BE}). Hence a higher current gain, β is achieved.

The unity gain frequency (f_T), which is defined as the maximum frequency at which the transistor demonstrates unity current gain, is the most common figure of merit for comparing the transistors and given by [27]

$$\frac{1}{2\pi f_T} \approxeq \frac{kT}{qI_E}(C_{EB} + C_{CB}) + R_C C_{CB} + \tau_B + \tau_C \tag{16}$$

where C_{EB} is the emitter-base capacitance, C_{CB} is the collector-base capacitance, R_C is the collector resistance, τ_B and τ_C are the base transit time and collector transit time, respectively. The grading of Ge across the base of SiGe HBTs, bends the energy diagram as shown in Fig. 9 and this generates a field in the opposite

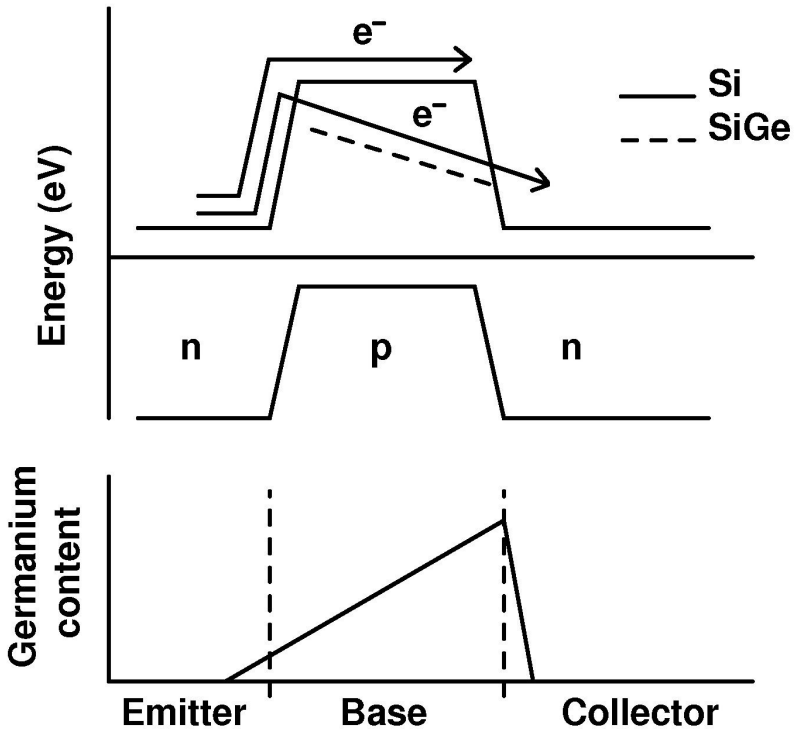

Figure 9: Ge concentration (bottom) and band structure (top) of a SiGe HBT. The Ge provides a lower barrier to injection from emitter to base as well as an accelerating field through the base.

direction of electron flow. Thus, the electrons are accelerated across the device, thereby the base transit time τ_B is reduced and in return f_T and f_{max} are improved. In addition, HBTs have been scaled vertically and laterally to lower dimensions to improve f_T and f_{max} further by reducing the parasitics, especially base, emitter and collector resistances and total collector-base capacitance. Recently the record setting transistors in SiGe with f_T/f_{max} of 300/500 GHz at room temperature has been reported [28].

The most remarkable advantage of the SiGe HBT BiCMOS technology is that it provides a performance competitive with III-V devices for microwave and mm-wave applications, while preserving the yield, cost and manufacturing advantages associated with conventional Si CMOS fabrication. Therefore, in SiGe technology digital circuits with CMOS transistors can be easily integrated with RF building blocks. This advantage over III-V technologies makes SiGe HBT technology a more viable and cost effective solution for system-on-chip integration of T/R modules than the III-V technologies used today. In brief, SiGe BiCMOS is a low-cost technology with high integration capabilities and with the recent advances, it has shown the

potential to be utilized for the next generation low-cost, small size, light weight, low-power density X-Band phased array radars.

1.6 Previously Proposed T/R Module

1.6.1 Building Blocks and Specifications

Fig. 10 presents the system block diagram of the X-Band SiGe BiCMOS T/R module proposed last year in the context of a master dissertation [29]. The T/R module is based on the all-RF system architecture in where phase shifting is performed at RF frequencies. It consists of a T/R switch, two single-pole double-throw (SPDT) switches, a power amplifier (PA), a low noise amplifier (LNA), a phase shifter and a variable gain amplifier (VGA). The signal amplification blocks such as LNA, VGA, PA are designed using HBTs while T/R and SPDT switches are designed using CMOS transistors in IHP 0.25 μm SiGe BiCMOS technology. In this module, the phase shifter is shared for both the receiving and transmitting paths through SPDT switches. Thus, in this architecture, there is no need to use a bidirectional phase and magnitude control circuit and thus a VGA can be employed right after a passive phase shifter as shown in Fig. 10 to compensate the signal losses for different phase states of the T/R module.

In this section the function of each building block will be summarized while explaining how the specifications shown in Fig. 10 are determined. Firstly, the power amplifier is the main block which directly affects the performance of the complete T/R module in transmit mode. As discussed before, 0.4-0.5 W output power per element is optimum to build next generation active phased arrays with an increase in the number of elements. This correlates to a minimum radiated power of 26 dBm from each antenna. In practice, most antennas used in phased arrays provide about 6 dB gain. Thereby, assuming 6 dB antenna gain and a 2 dB insertion loss for the T/R switch in transmit mode, a output power higher than 22 dBm is required for the power amplifier. A two-stage, high gain power amplifier which can fulfill this requirement was reported last year and its performance will be briefly summarized in the next subsection.

In receive mode, low-noise amplifier is one of the most important building blocks of the T/R module. It has a direct impact on the noise performance and in return

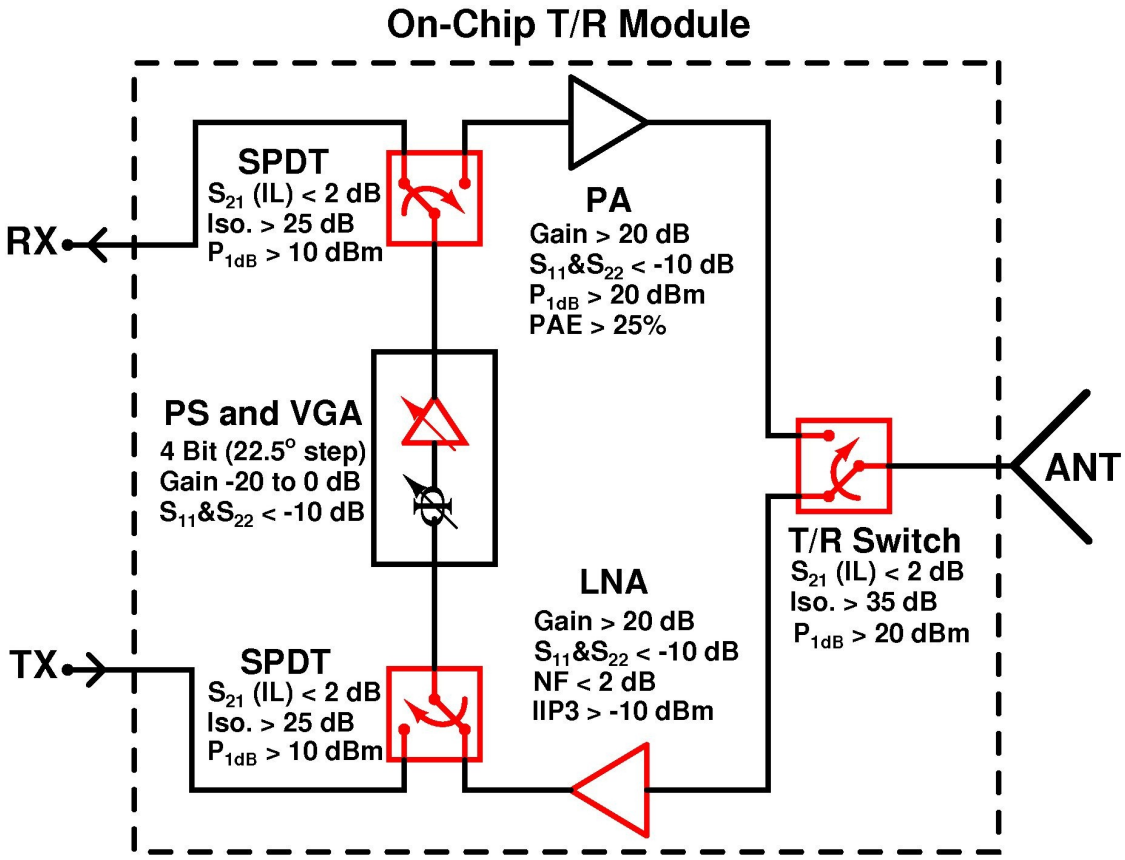

Figure 10: SiGe X-Band T/R module system block diagram. The highlighted blocks are the main focus of this thesis.

on the sensitivity of the T/R module. Considering the state of the art performances reported in the literature an overall noise figure around 5 dB is aimed for the module. Assuming a 2 dB insertion loss for the T/R switches, a noise figure lower than 2 dB is required to be able to achieve a state-of-the-art performance for the T/R module. Additionally, low noise amplifier require a high gain to suppress the noise contributions of the consecutive stages, especially from the lossy phase shifter. However, linearity, input referred third order intercept point (IIP_3) of the T/R module deteriorates with increasing gain in first stages. Therefore a minimum 20 dB gain and -10 dBm IIP_3 are aimed to reduce to noise added by later stages significantly without degrading the linearity of the module. These are clearly challenging performance specifications to achieve simultaneously in SiGe BiCMOS technology.

In a typical T/R module, primary aims are to direct high power RF signal from transmitter to antenna while preventing leakage of that large signal into more sensitive front-end of receiver and to provide a low loss path between TX/ANT, in

particular between ANT/RX ports. Therefore, the T/R switch should provide a low loss and a high isolation between TX and RX paths, as well as handling high power output signals of power amplifier during transmit mode of operation. The power handling capability of a T/R switch is defined as the input referred 1dB compression point of the switch. It should be at least equal to output referred 1dB compression point of the PA, minimal 22 dBm. Additionally, an insertion loss lower than 2 dB is required to be able to satisfy the overall noise figure specification of the T/R module in receive mode. Considering the IIP_3 specification of the LNA, the isolation of the T/R switch should be higher than 35 dB, higher than 40 dB is favorable, to be able to reduce the leakage signal level from PA to LNA which can saturate the LNA.

The function of the SPDT switches is similar to T/R switch; routing signal to two different terminals depending on the control voltage. The figures of merit of the SPDT switch are similar to the T/R switch. However, the isolation and power handling capability requirements of the SPDT switches are less stringent since they are located before the power amplifier and do not experience high power signals. Therefore, in the SPDT switch design the main aim will be to minimize the insertion loss while occupying a small die area.

The phase shifter is the most essential building block of a T/R module for the scanning functionality of the phased array systems. The resolution of phase shifter determines side-lobe, grating-lobe and main-lobe levels as well as scanning array of the array. The phase shifter is located after the LNA in the receive path and should have a high IIP_3 not to degrade the overall linearity of the T/R module. Therefore, a passive 4-bit phase shifter with 22.5° phase resolution is chosen. The phase shifter can be easily controlled with MOS switches without any DC power consumption, theoretically. Using 4-bit phase shifters, phased arrays can steer main beam almost continuously with a negligible variation in array gain or sidelobe levels [30].

Up to now, a two stage PA, a SPDT switch, a high performance LNA, a switched LNA and two different types of T/R switches have been designed and their performances have been verified with measurements. The two-stage PA was reported in detail last year in the context of a master dissertation [29]. In the next section, its performance will be briefly given. The other blocks except phase shifter are the main focus of this dissertation and will be covered in detail in the following chapters.

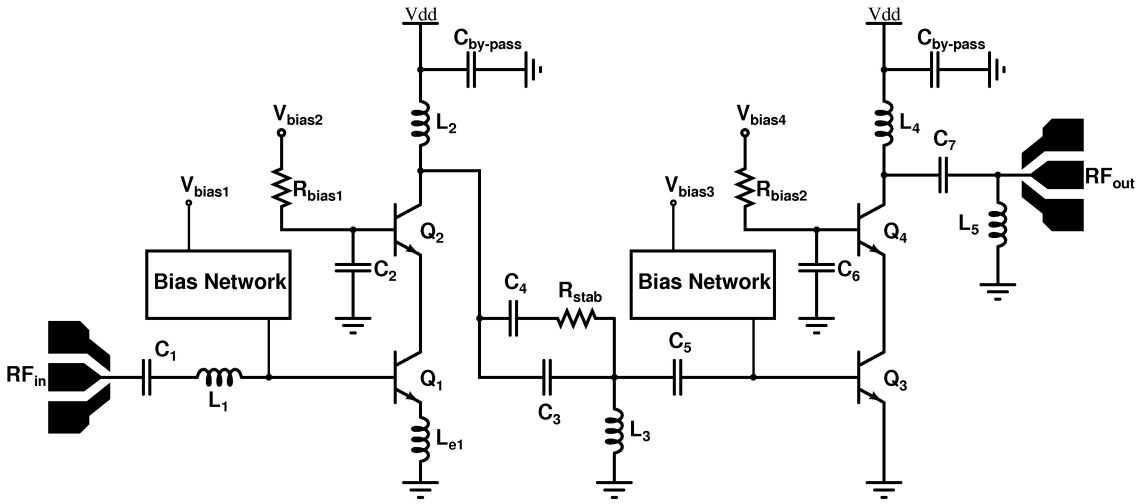

Figure 11: Schematic of the designed two-stage power amplifier.

1.6.2 Power Amplifier

A linear two-stage single-ended PA is designed using SiGe HBTs as shown in Fig. 11 [31]. Both stages are based on cascode topology to overcome the technology's 2.5 V BV_{CEO} breakdown voltage by presenting low impedance at the base terminal of the cascode transistors. In each stage, fastest HBTs in the process are used for the common emitter part and medium voltage and speed transistors are used for the common base part. Moreover, active bias networks are used to enhance the linearity of the PA effectively [32]. To improve the stability of the PA, C_3 and C_4 coupling capacitors are shunted with a series RC network to introduce resistive loss at low frequencies.

The PA occupies 0.6 mm^2 chip area without pads. Biased at Class-A mode, the PA resulted in peak small-signal gain of 25.5 dB as shown in Fig. 12. S_{11} is better than 10 dB at X-Band while S_{22} is better than 10 dB in a 2 GHz bandwidth. The measured saturated output power is more than 23 dBm, and more than 20 dBm linear output power is achieved in a 4 GHz bandwidth (Fig. 13). While operating at P_{1dB} output power the PA draws 100 mA from 4 V supply, and achieves a peak PAE of 28 %, and more than 25 % PAE in a 3 GHz bandwidth centered at 9 GHz.

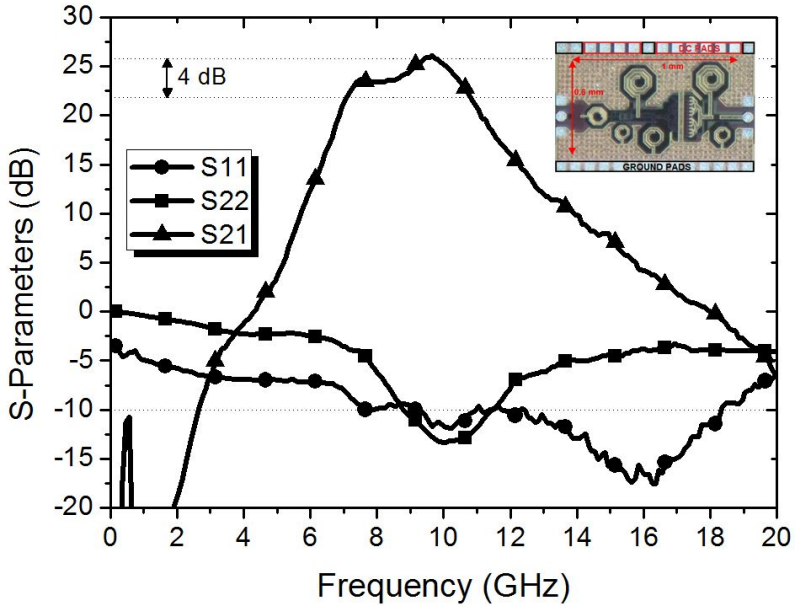

Figure 12: Measured small-signal gain and return loss of the two-stage power amplifier.

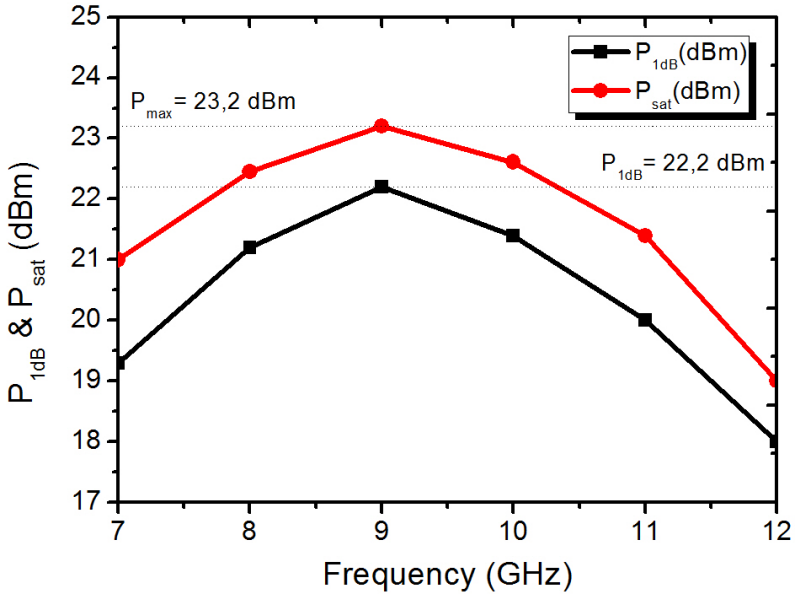

Figure 13: Measured saturated output power and the output referred P_{1dB}.

1.7 Motivation

As discussed in the previous sections, the cost, size, weight, power consumption and complexity of the current phased array T/R modules restrict this technology only to certain military and satellite applications which can tolerate these limitations. The significant spread of phased arrays in next generation military and satellite applications as well as commercial markets is only possible by overcoming these technical limitations and reducing the unit cost. Therefore, next generation X-

Band phased array radar systems aim to use low cost, fully integrated T/R modules to overcome these hurdles. Considering the high frequency and digital capabilities, SiGe HBT BiCMOS technology can be an excellent candidate for this purpose.

Therefore, the objective of this thesis is to replace III-V T/R module components with high performance SiGe BiCMOS front-end circuits for building next generation X-Band phased array radar systems. For this purpose, high speed circuits which can satisfy the demanding requirements of the next generation T/R modules are implemented in IHP 0.25 μm SiGe BiCMOS technology. This dissertation aims to present unique T/R module front-end circuits based on new approaches and techniques.

1.8 Organization

Chapter II presents the design of a highly linear CMOS series-shunt T/R switch, a slow-wave transmission line based T/R switch and a DC-20 GHz SPDT switch, primarily optimized at X-Band, in 0.25-μm SiGe BiCMOS process for a fully integrated active phased array T/R module. The series-shunt T/R switch resulted in a measured IL of 3.6 dB, isolation of 34.8 dB and IP_{1dB} of 28.2 dBm at 10 GHz. This switch achieves the highest power handling capability among the single-ended CMOS X-Band switches, to the best of our knowledge, attributed to the unique design methodologies and techniques. The slow-wave T/R switch was implemented using shunt NMOS transistors and slow-wave quarter wavelength transmission lines. It presents the utilization of slow-wave transmissions lines in T/R switches for the first time in any BiCMOS technology to the date. The SPDT switch resulted in a measured insertion loss of 0.5-3.1 dB, isolation of 55-21 dB and IP_{1dB} of 16-17.3 dBm from DC to 20 GHz. It is a successful demonstration of the full integration of ultra-wideband SPDT switches in CMOS process.

Chapter III presents the design of a high performance two-stage and a switched LNA at X-Band in 0.25-μm SiGe BiCMOS process. The high performance LNA is composed of two cascode stages using SiGe HBTs to achieve low noise figure, high gain and a better matching to 50 Ω at the input and output, simultaneously. First stage is designed for low noise performance while the second stage is optimized to improve the IIP_3. The LNA resulted in a measured gain of 21 dB, a noise figure

of 1.52 dB and an input third-order intercept point of -8 dBm at 10 GHz. These performance parameters collectively constitute the best Figure-of-Merit reported in similar technologies. The switched LNA is based on single stage bipolar cascode topology and the switching circuitry is designed by a series isolated NMOS switch. In gain mode, the switched LNA achieves a NF of 1.6-1.9 dB, a gain of 9.5-11.5 dB and an input-referred P_{1dB} of -6 dBm with 18.6 mW power consumption. In bypass mode, the switched LNA resulted in a measured insertion loss of 6 dB and an input-referred P_{1dB} of 17.4 dBm at 10 GHz. To the best of author's knowledge, this is the first SiGe switched LNA reported at X-band. Furthermore, the resistive body floating technique is incorporated in switched LNA design, for the first time, to improve the linearity of the circuit in bypass mode.

Chapter IV shows the integration of a complete X-Band SiGe BiCMOS T/R module using separately designed 50 Ω building blocks presented. 50 Ω microstrip lines are implemented in the BEOL of the process to connect the building blocks together. The module does not employ a T/R switch and it is assumed an off-chip circulator, with a lower insertion loss, would be used to improve sensitivity of the system in receive mode.

Chapter V summarizes the contributions of this thesis and concludes the dissertation with a discussion on possible future work.

2 RF CMOS Switches for the X-Band SiGe T/R Module

2.1 An X-Band Highly Linear CMOS T/R Switch

2.1.1 Introduction

A major challenge for next generation fully integrated SiGe BiCMOS T/R modules is to implement a high performance CMOS T/R switch which can handle high transmit powers and provide high isolation as well as a low insertion loss. In the literature, several single ended T/R switches implemented in CMOS processes are reported [33–45]. However, none of them is capable of handling relatively high output powers required for viability of SiGe T/R modules, typically higher than 0.4 W at X-Band.

This section presents the design and implementation of a CMOS SPDT T/R switch in 0.25-μm GHz SiGe BiCMOS technology for an X-Band, fully integrated T/R module presented in Chapter I. As mentioned before, SPDT T/R switch comes right after the antenna and is a crucial component in a T/R module that routes antenna to either transmitter (TX) or receiver (RX) (Fig. 14). Thereby, it directly affects the transmission efficiency and the receiver noise figure of the system. The T/R switch in this work was designed using techniques to achieve, primarily, the highest P_{1dB}, without sacrificing IL and isolation. These techniques include resistive-body floating, using on-chip impedance transformation networks (ITN) and DC biasing of all terminals of the T/R switch. In addition, optimization of transistor widths and parallel resonance technique are used to improve insertion loss (IL) and

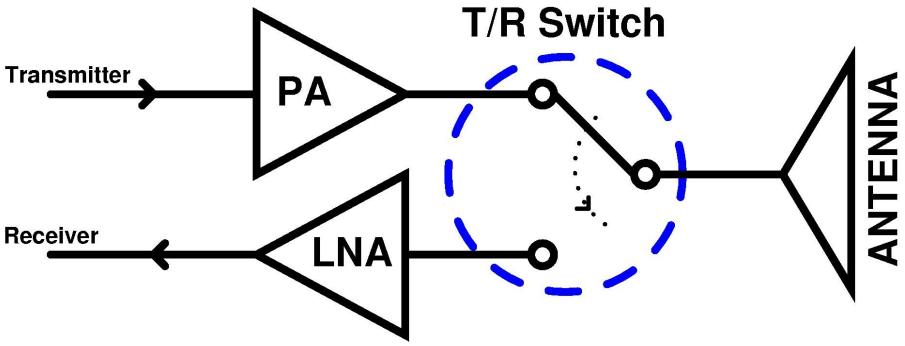

Figure 14: A simple block diagram of T/R module

isolation, respectively. Section 2.1.2 presents the design of the T/R switch and these tecniques. In Section 2.1.3, layout considerations and the measurement results are presented.

2.1.2 Circuit Design and Analysis

Fig. 15 shows the circuit schematic of the designed X-Band SPDT T/R switch, based on series-shunt topology. M1 and M2 transistors perform the main switching function of directing signal between TX/ANT or ANT/RX ports. M3 and M4 transistors are used to improve isolation between TX and RX ports by grounding the leakage signal. Operation of the switch is as follow: when V_{ctrl} is high and V_{ctrli} is low, the switch operates in the transmit mode. In this mode, M1 and M3 operate in deep triode region (ON state) while M2 and M4 operate in cut off region (OFF state). Hence, the channel resistance of M1 is very low, forming a low loss connection between TX and ANT so that incoming signal from transmitter is routed to antenna. Since M2 is operating in cut off region, the channel resistance is very high, isolating RX port from TX and ANT. Also, leakage signal due to parasitic coupling in M2 is directed to ground through low resistance path formed by M3 transistor before reaching receiver end. In receive mode, basic operation of the switch is similar to

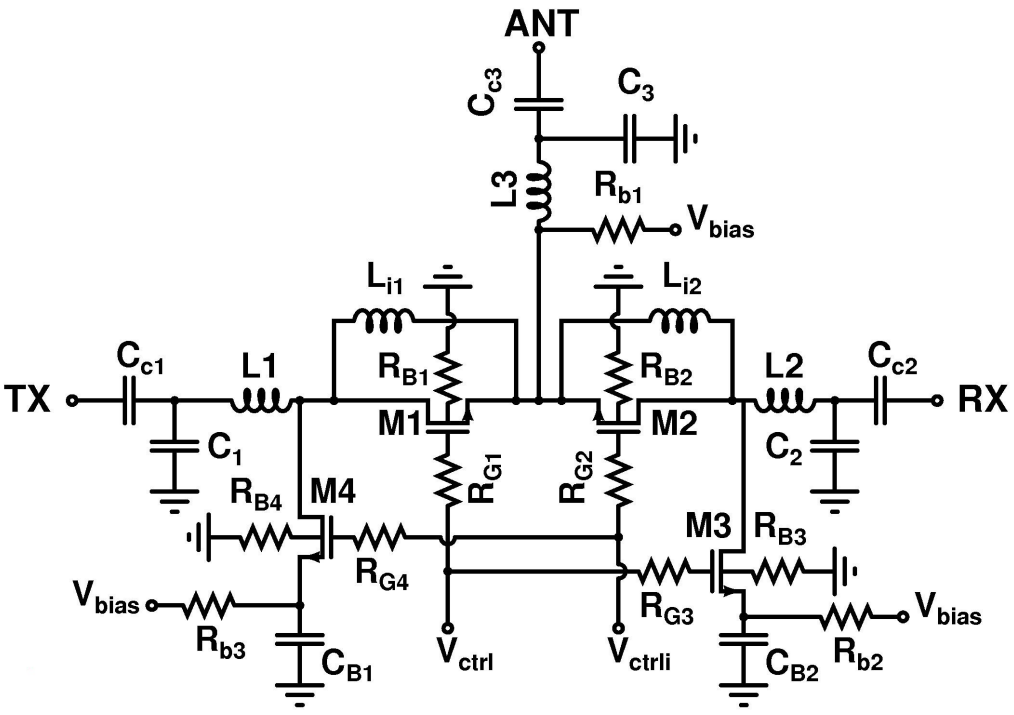

Figure 15: Circuit schematic of the designed SPDT T/R switch.

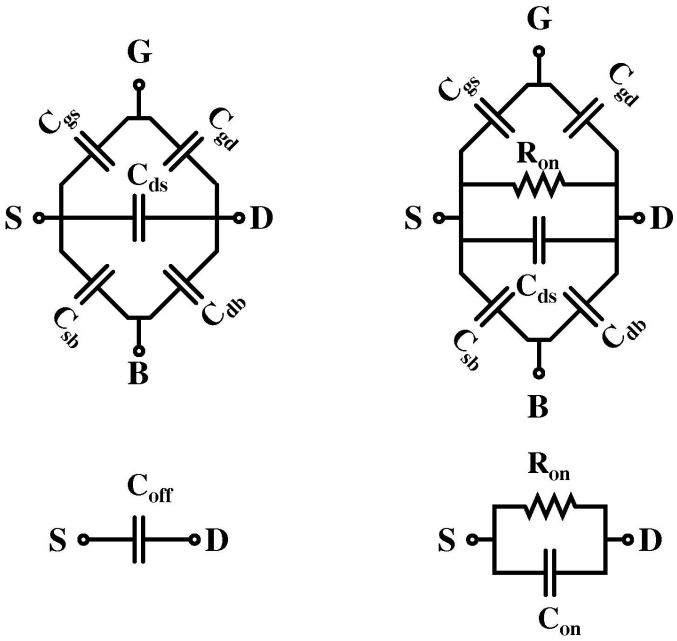

Figure 16: (a) OFF-state Model and (b) ON-state Model of NMOS.

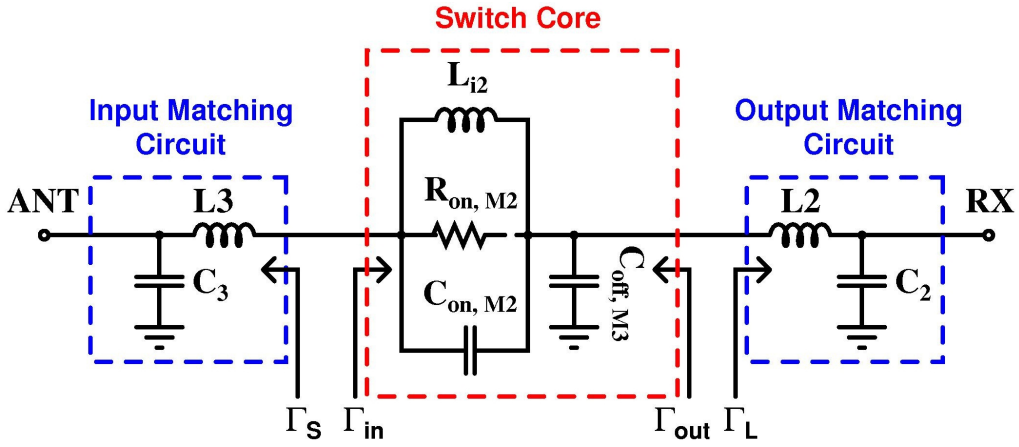

Figure 17: Transmit mode small-signal simplified model.

transmit mode, with an only difference of roles of M1 and M3 are replaced by M2 and M4 transistors, respectively.

In either mode, insertion loss is mainly dominated by the channel resistances of M1 or M2 in the ON state, R_{on}. Also port matching has a significant effect on insertion loss since IL can be defined as reciprocal of transducer gain. Simplified triode and cut-off models of a MOS transistor with both gate and body floated are shown in Fig. 16. In the receive mode, the circuit in Fig. 15 is reduced to the equivalent circuit in Fig. 17 by using triode and cut-off models of the MOS transistors and by neglecting coupling to transmitter. Based on this approach, the transducer gain of the equivalent circuit can be defined by [42],

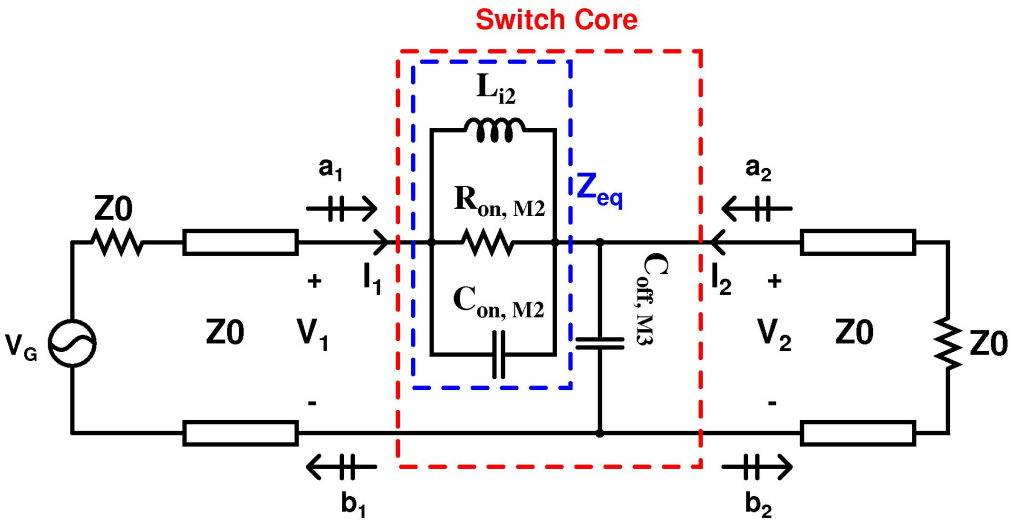

Figure 18: Circuit configuration to derive S21 of the ON transistor.

$$G_T = \frac{1-|\Gamma_s|^2}{|1-\Gamma_s\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{17}$$

$$IL = \frac{1}{G_T} \propto \frac{1}{|S_{21}|^2} \tag{18}$$

According to (18), insertion loss of the switch is inversely proportional with the S_{21} parameter of the switching core. S_{21} of a MOS transistor in the ON state can be calculated by using the configuration in Fig. 18

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{V_2 - I_2Z_0}{V_1 + I_1Z_0} = \frac{2V_2}{I_1(Z_1+Z_0)} \tag{19}$$

where a_1 is the incident power wave in port 1, b_2 is the reflected power wave in port 2, Z_1 is the total impedance seen looking into port 1, V_n and I_n is the total voltages and currents where the index n refers to port number.

$$S_{21} = \frac{2\left(Z_0 \parallel \frac{1}{j\omega C_{off,M3}}\right)}{Z_0 + Z_{eq} + \left(Z_0 \parallel \frac{1}{j\omega C_{off,M3}}\right)} \tag{20}$$

$$Z_{eq} = \frac{1}{j\omega C_{on,M2} + \frac{1}{R_{on,M2}} + \frac{1}{j\omega L_{i2}}} \tag{21}$$

By substituting (20) into (18)

$$IL \propto \left(\frac{Z_0 + Z_{eq} + \left(Z_0 \parallel \frac{1}{j\omega C_{off,M3}} \right)}{2\left(Z_0 \parallel \frac{1}{j\omega C_{off,M3}} \right)} \right)^2 \tag{22}$$

where Z_0 denotes the characteristic impedance of the system and $R_{on,M2}$ is on resistance of the M2 transistor. Furthermore, by neglecting the $C_{on,M2}$, $C_{off,M3}$ and L_{i2} equation (22) simplifies to

$$IL \propto \left(\frac{2Z_0 + R_{on,M2}}{2Z_0} \right)^2 \tag{23}$$

According to equation (23), resistance of the MOS transistor in the ON-state should be lower to decrease insertion loss of the switch. The resistance of a MOS transistor operating in the deep triode region is defined by

$$R_{on} = \frac{1}{\mu_n C_{ox} (\frac{W}{L})(V_{GS} - V_{th})} \tag{24}$$

Equation (24) shows that lower R_{on} can be achieved by using high mobility (μ) transistors, large aspect ratio (W/L) and high gate-to-source/channel voltage (V_{GS}). Based on the first criterion, NMOS transistors are chosen to implement T/R switch since mobility of the NMOS transistors is approximately three times higher than the mobility of PMOS transistors in the used technology. Transistors in the ON-state are biased by using 2.5 V gate-to-channel voltage, also the maximum allowed voltage of the used technology to prevent avalanche and gate-oxide breakdown. Additionally, aspect ratio (W/L) is the dominant factor determining the ON-resistance of M1 or M2 and insertion loss in return. As seen in (23) and (24), as the aspect ratio increases, ON-resistance decreases, in return, decreasing insertion loss. In order to achieve a larger aspect ratio, length of the M1 or M2 should be minimized, provided that minimum length limited to 240 nm, while larger widths are used for transistors.

2.1.2.1 Optimization of Transistor Widths

There is a practical limit in increasing transistor width. That is as the width is increased, source/drain to body parasitic capacitances and in return coupling to

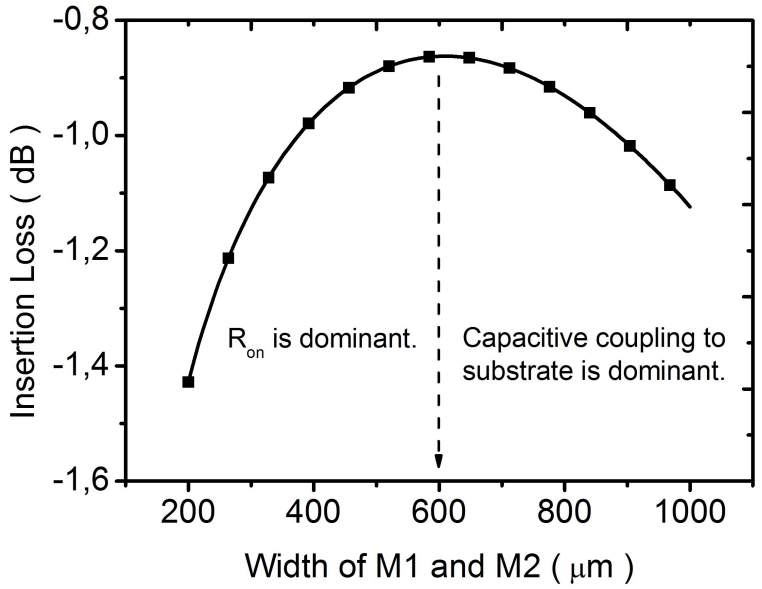

Figure 19: Transistor width versus insertion loss of the SPDT T/R switch.

substrate increases. If the width of transistor is extremely increased, signal loss through capacitive coupling to substrate becomes significant and, consequently, insertion loss increases [38]. Increase in the parasitic capacitances also increases the OFF-capacitance of the transistors, leading to more coupling to undesired port and resulting in degradation of isolation. In brief, there is a trade-off between R_{on} and parasitic capacitance, resulting in an optimum value for the width of the transistor at a given operating frequency. The optimum width for the minimum insertion loss has been found by simulations using Cadence Spectre-RF tool at 10 GHz. Fig. 19 shows the simulation results of insertion loss versus the width of the switching transistors. As can be seen, M1 and M2 should be around 600 μm to achieve a minimum insertion loss for 2 V of V_{bias} and 4.5 V control voltage.

As the frequency increases, the effect of the parasitic capacitances on the isolation becomes significant. Therefore, the use of different techniques to achieve a better isolation, without significantly degrading insertion loss, becomes essential at higher frequencies. One approach to improve isolation is to increase width of shunt transistors to direct leakage signals to ground better in the undesired ports. However, as the width of the transistors increases, parasitic capacitances increase, accordingly. In particular C_{db} of M3/M4 becomes more important since they are between signal path and substrate. Therefore, coupling of RF signal to substrate

and in return insertion loss increase as C_{db} of M3/M4 increases. Taken into account the trade-off between insertion loss and isolation introduced by shunt transistors, widths of M3/M4 are chosen as 240 μm to improve isolation without considerable degradation on insertion loss.

2.1.2.2 DC Biasing

In addition to transistor widths, parasitic capacitances of the transistors and in return insertion loss of the switch are affected by the DC bias of the circuit. Source/drain to body junction capacitances in the MOS model are voltage dependent. As the reverse bias voltage is increased between source/drain-to-body, depletion width in corresponding junctions increases. Since these junction capacitances are inversely proportional with depletion width, C_{sb} and C_{db} decrease with increasing reverse bias. Bias dependence of C_{sb} and C_{db} can be formulated as [44]

$$C_{sb/db} = \frac{Area.C_{j0}}{\left(1 + \frac{V_{SB/DB}}{V_{0j}}\right)^{m_j}} + \frac{Perimeter.C_{jsw0}}{\left(1 + \frac{V_{SB/DB}}{V_{0jw}}\right)^{m_{jw}}} \tag{25}$$

where $V_{SB/DB}$ is the reverse bias voltage across the junction, V_{0j} and V_{0jw} are the junction and sidewall built-in potentials, C_{j0} and C_{jsw0} are the capacitance value of unit area of bottom junction and unit length of sidewall at zero bias voltage. This equation clearly shows that smaller junction capacitances, thus, reduced coupling of RF signal to substrate for improvement in insertion loss can be obtained by higher $V_{SB/DB}$. Additionally, biasing source/drain of the series and shunt transistors improve the power handling capability of the switch. Power handling capability of the SPDT T/R switch, input referred P_{1dB}, is mostly limited by turn on voltages of the drain/source-to-body junctions of M1/M2 due to large RF signals. DC biasing the sources and drains of M1/M2 increases the turn on voltage of the drain/source-to-body junctions. When $V_{SB/DB}$ potential goes below the turn on voltage of the junction during the negative cycle of large input signal, a conduction path between substrate and source/drain would occur. Thus significant portion of the RF signal would be routed to substrate and in return output power would compress. Amplitude of RF input signal, forward biasing source/drain-to-body junctions of M1 and

M2 for different DC biases, can be formulated as

$$V_{RF} = V_{bias} + V_{turnon} \approx V_{bias} + 0.5V \tag{26}$$

and corresponding power level for the input

$$P = \frac{V_{RF}^2}{2Z_0} \tag{27}$$

where V_{bias} is the DC bias applied to source and drain terminals of M1/M2 and V_{turnon} is the minimum voltage required to turn on source/drain-to-body diodes. These expressions signify that as the DC bias voltage is increased, allowed maximum voltage swing and power handling capability (IP_{1dB}) of the switch increases.

Taking into account of the effects of DC biasing on the insertion loss, power handling capability and power consumption of the switch, all the sources and drain of NMOS transistors are biased by 2 V. The complete biasing method is shown in Fig. 15. The antenna node and sources of the shunt transistors are biased by 2 V through R_{b1} - R_{b3} to prevent forward biasing of source/drain-to-body junctions and to decrease voltage dependent parasitic capacitance. The values of R_{b1} - R_{b3} should be high enough to prevent leakage into bias port. Otherwise, considerable amount of the RF input signal would be lost due to leakage and thus insertion loss would increase. Additionally, C_{B1} and C_{B2} by-pass capacitors are used to bias the source of M3/M4 while introducing RF ground to the sources of M3 and M4. Considering the maximum allowed voltage across four terminal of transistors in this technology, 2.5 V, V_{ctrl} and V_{ctrli} has been set to 4.5 V and 0 V for transmit mode and vice versa for receive mode.

The gates of all transistors are biased through large gate resistors R_{G1}-R_{G4} to make the gates of transistors float at AC signals and prevent signal coupling. The bias resistors allow gate capacitance to keep gate-to-channel voltage constant when different cycles of RF signal arrived. Without these resistors, variation in gate-to-channel voltage (V_{GS}) would occur and insertion loss would vary with RF signal at a given frequency [46]. The resistors at the gate of transistors also affect the switching time, defined as the time required for switch to change from transmit mode to receive mode or vice versa. Fast switching time entails low gate resistors to

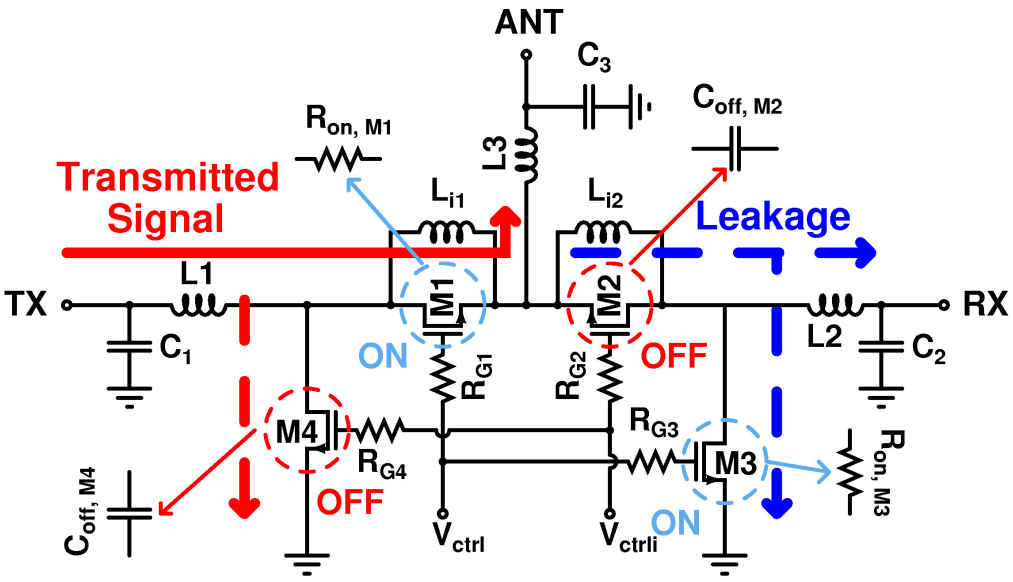

Figure 20: T/R switch in the transmit mode.

charge or discharge gate capacitances quickly. In brief, there is a trade-off between AC floating gate and switching time. However, keeping gate to floating for AC signals outweigh switching time consideration since switching time is not usually a limiting factor. Therefore, 10-kΩ gate bias resistors are used in the design.

2.1.2.3 Parallel Resonance

In this work, another technique used for improving the isolation of the X-Band SPDT T/R switch is the shunt inductor resonance. In Fig. 16, small signal model of a MOS transistor with both gate and body floated in OFF state is given. According to this model, by neglecting the large channel resistance, typically more than 100 kΩ, OFF capacitance can be derived as

$$C_{off} = C_{ds} + \frac{C_{gs}C_{gd}}{C_{gs} + C_{gd}} + \frac{C_{sb}C_{db}}{C_{sb} + C_{db}} \tag{28}$$

This total equivalent capacitance between drain and source of a transistor in OFF mode causes signal coupling from TX to RX port. Shunt inductors between source and drain terminals of the switching transistors M1 and M2 improve isolation by reducing leakage and thus coupling through OFF switching transistor. Fig. 20 shows the equivalent circuit of the switch core in the transmit mode. The inductor L_{i2} resonates with equivalent parasitic capacitances to form a high impedance path

to RX port. Resonance frequency can be calculated as

$$f_R = \frac{1}{2\pi\sqrt{L_{i2}C_{off,M2}}} \tag{29}$$

In this work, considering possible deviation from design specifications after fabrication because of the model-mismatch, resonance frequency is arranged at 10 GHz, the center frequency of X-Band. To achieve a 10 GHz resonance frequency in post layout simulations, 680 pH octagonal inductors with the quality factors of ~ 20 at 10 GHz are used for L_{i1} and L_{i2}. These inductors are modeled using ADS Momentum and S-parameters of the inductors are extracted to incorporate them to Cadence for post layout simulations.

2.1.2.4 Resistive Body Floating

DC biasing the sources and drains of all transistors to improve power handling capability is already discussed. In addition, body floating technique is used to improve P_{1dB} of the switch by reducing the signal loss through source/drain-to-body junctions. The transistor bodies are connected to ground through 10-kΩ resistors. To implement this technique, iNMOS (isolated NMOS) transistors, available in the process, are used to separate the body of each transistor from the common p-substrate (Fig. 21). In Fig. 22, junction diodes between the substrate and source/drain are explicitly shown on the T/R switch core schematic. During the negative cycle of RF signal in transmit mode, D_1-D_3 and D_7 diodes would be turned on. As a result, in a conventional switch without body floating resistors, small on resistance of diodes result in leakage paths to the ground, limiting the power handling capability. However, when the bodies of the transistors are connected to ground via large resistances, the equivalent resistance to the ground is larger so those bodies of the transistors float at AC signals. Hence, the leakage to ground occurring at large RF voltage swings is prevented.

2.1.2.5 Impedance Transformation Networks

Apart from DC biasing sources and drains of all transistors and body floating, impedance transformation networks (ITNs) are employed to improve power handling

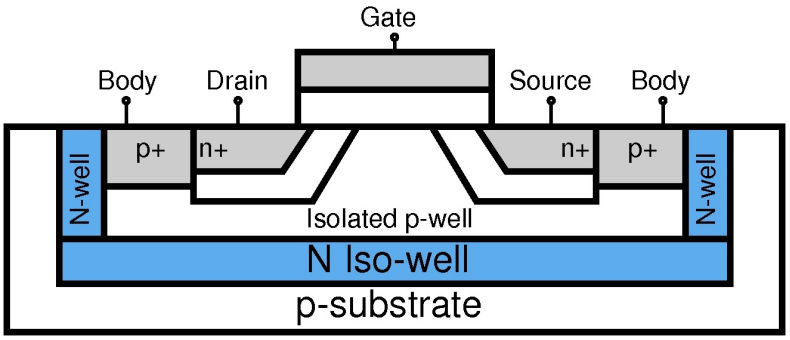

Figure 21: Cross-sectional view of a typical isolated NMOS transistor.

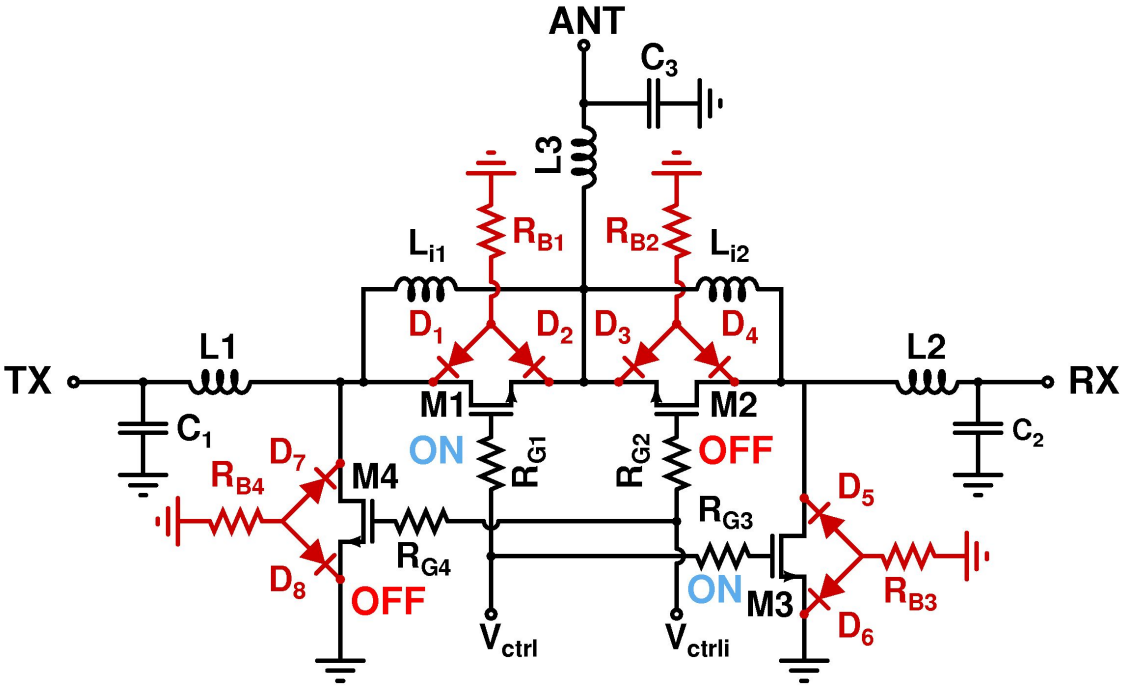

Figure 22: The switch core with body floating technique in TX mode.

capability of the switch. In Figure 22, 50 Ω source and load impedances are transformed into lower impedances through parallel C-series L matching networks. Power handling capability of the switch is limited by the forward biasing of source/drain-to-body junctions. Thus, largest amplitude of the RF signal that could appear is V_{max}=V_{bias}+V_{turnon} as discussed. Corresponding power can be calculated as

$$P = \frac{V_{max}^2}{2Z} \tag{30}$$

where V_{max} is the largest amplitude that could appear at signal path and Z is the transformed source and load impedances. As the transformed impedance decreases, power handling capability of the switch increases, according (30). However, while

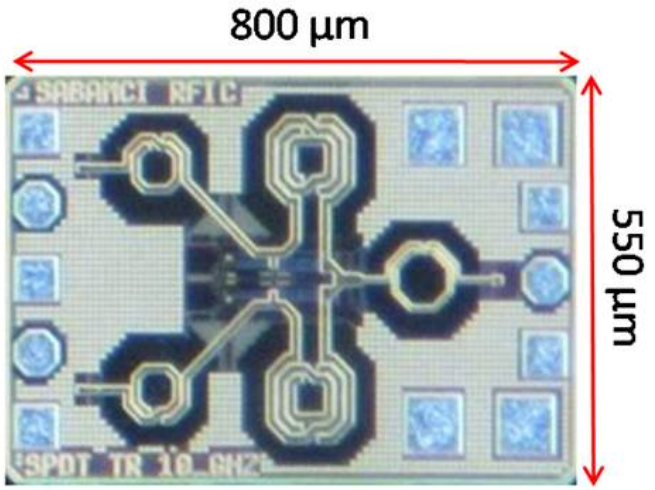

Figure 23: Die photo of the T/R switch. The chip area including pads is 0.44 mm_2.

reducing transformed impedance, IL's dependence on the port matching should be considered. As discussed, IL is defined as reciprocal of transducer gain which is significantly affected by port matching. Taking into account the trade-off introduced by ITN's between the insertion loss and power handling capability, shunt C-series L network is used for impedance transformation. Both of series C- shunt L and shunt C- series L matching networks were implemented in our simulations. According to the results, matching achieved by shunt C- series L was in a broader frequency band, leading to be preferred. Besides, by using shunt C-series L matching network, parasitic capacitance of the pads, the inductors L1/L2/L3 and DC blocking capacitors C_{c1}, C_{c2}, C_{c3} can be merged into the shunt C. 200 fF metal-insulator-metal (MiM) capacitors and 540 pH integrated octagonal inductors with quality factors of ~ 22 are used to implement these networks.

2.1.3 Measurement Results

The T/R switch was fabricated in IHP, 0.25-μm SiGe BiCMOS process. The die photo of the switch is shown in Fig. 23. The chip area, including pads, is 0.44 mm^2. Inductors in the chip are custom designed with the thickest top metal layer in the process to utilize its lower resistivity and capacitance to ground. Hence, loss due to series resistance of inductors and coupling to substrate can be reduced, leading to high quality factor inductors. Additionally, design of the matching inductors, L1,

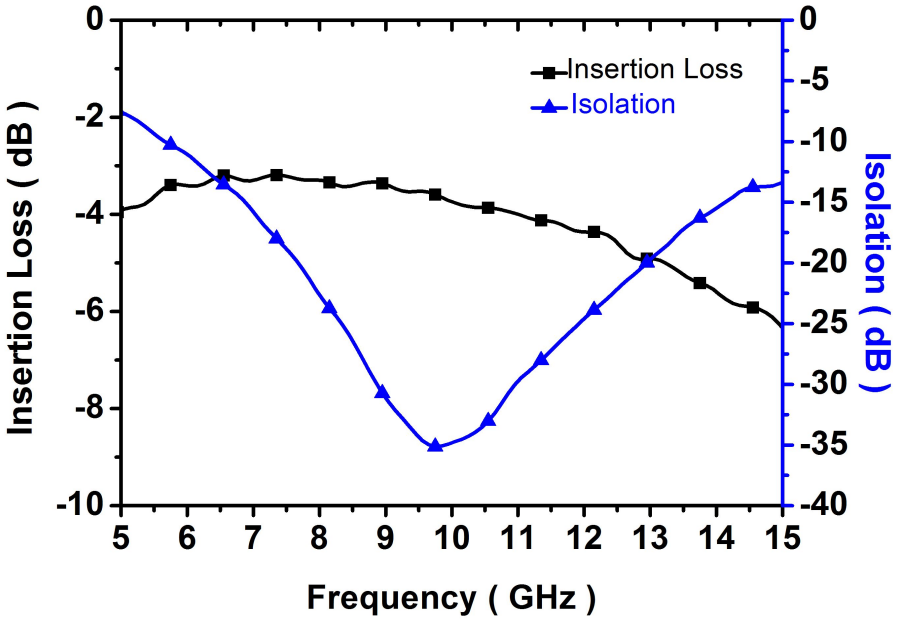

Figure 24: Measured insertion loss and isolation of the T/R switch.

L2, and L3 requires special attention. Quality factor of these inductors affects the insertion loss of the switch since they are laid out on the signal path. Octagonal inductors tend to have better Q (Quality Factor) than square inductors. Therefore, inductors in the design are implemented as octagonal, as seen in Fig. 23. Full custom design of the inductors during layout allowed us to minimize interconnection paths between the inductors and other components in the design.

Optimization of the layout is crucial for the RF performance of the T/R switch. Therefore, layout of the switch, including all interconnections and inductors, are simulated by Momentum in ADS. Particularly, placement of the inductors needs extra care since coupling between inductors deteriorates Q's of adjacent inductors. There are two types of coupling mechanism: substrate coupling and electromagnetic coupling [47], [48]. In order to alleviate substrate coupling between inductors, perimeter of each inductor is covered by p+ substrate contacts which are 50 μm away from the inductors. Also, inductors are separated by 110 μm to alleviate electromagnetic coupling.

Measurements of the T/R switch were performed under 2 V V_{bias} voltage, 4.5 V and 0 V control voltages. As shown in Fig. 24, the measured insertion loss and isolation between TX and RX ports is 3.6 dB and 34.8 dB, respectively, at 10 GHz. Insertion loss of the switch is between 3.2 dB and 4.1 dB at X-Band. Measured

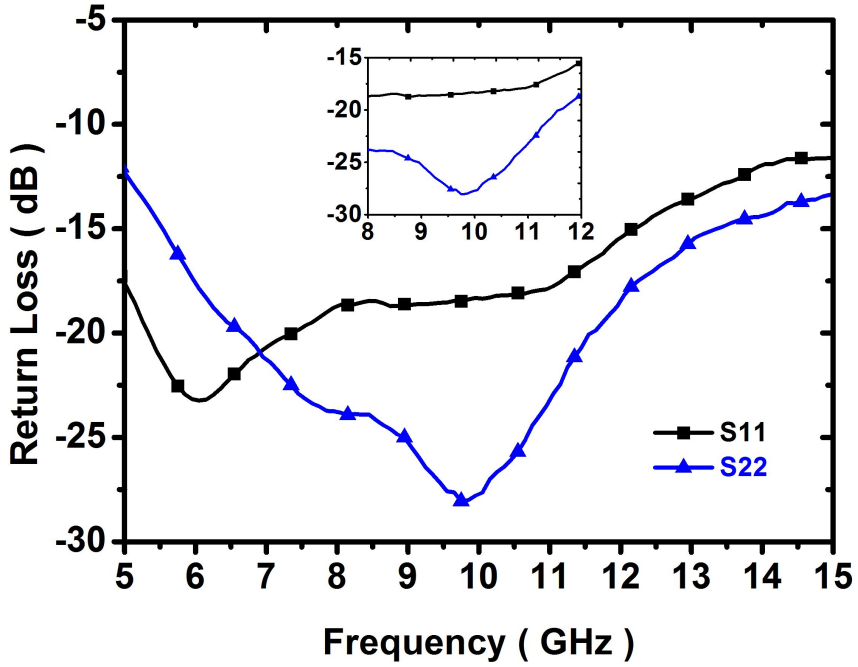

Figure 25: Measured input return loss, S_{11}, and output return loss, S_{22} of the T/R switch.

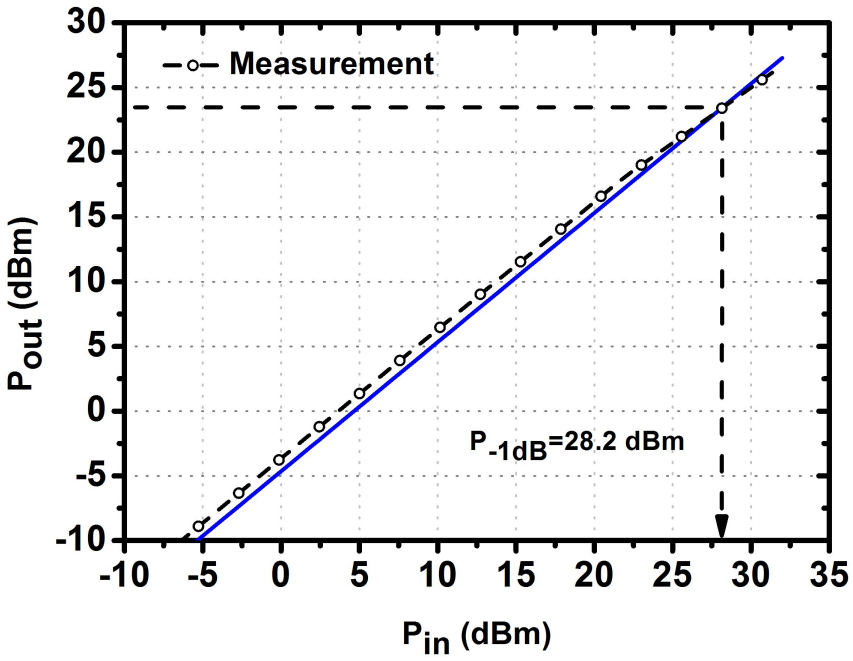

Figure 26: Measured 1 dB compression point (IP_{1dB}) of the switch at 10 GHz.

return losses are shown in Fig. 25. The return loss at TX port, S11, is 18 dB at 10 GHz and changes from 16 dB to 19 dB at X-Band. The return loss at ANT port, S22, is 28 dB at 10 GHz and ranges between 18 dB and 28 dB at X-Band. Due

to the symmetry of the switch, IL and RL in the receive mode are almost equal to transmit mode values. As shown in Fig. 26, the switch results in an input 1 dB compression point (IP_{1dB}) of 28.2 dBm at 10 GHz. At the expense of reliability of the switch, higher power handling can be achieved by biasing source and drain of the transistors to a higher potential.

2.1.4 Performance Comparison

Table 2 compares performance of the presented switch with that of other single-ended CMOS T/R switches reported in the literature, operating at X-Band. This work achieves the highest power handling capability with competitive isolation and comparable IL, among the single-ended CMOS X-Band switches. It is attributed to the unique design methodology which is based on combining various techniques reported seperately in an effective way.

2.2 A DC-20 GHz CMOS SPDT Switch

2.2.1 Introduction

Single-pole-double-throw (SPDT) switches are one of the key building blocks in the next generation radar and communication systems. CMOS switches can be used in applications such as transmit/receive modules, phase shifters and multi-standard communication systems [53]. Up until now, high performance SPDT switches are widely implemented as off-chip components using III-V based transistors and PIN diodes. However, replacement of III-V SPDT switches with CMOS switches with comparable performance is indispensable for future system-on-chip phased array applications.

Other than low-cost and high integration, there is also an increasing demand for wideband systems to achieve higher data rates on a single chip with less complexity. Wireless transceivers which can simultaneously cover multiple frequency bands are also extremely attractive to enable more efficient spectrum utilization. As the bandwidths of radar and communication systems are pushed wider or required to cover multibands to address newly emerging applications, the need of designing ultra-wideband (UWB) CMOS SPDT switches become more critical [51].

Table 2: Comparison of the T/R switch with the state-of-the-art reported works

Frequency (GHz)	Figures of Merit			Chip Area mm^2	Technique	Technology	Ref.
	IL (dB)	Isolation (dB)	P_{1dB} dBm				
8−12	**3.2−4.1**	**23.2−34.8**	**28.2**	**0.44**	**Series-shunt, Body floating, Impedance Transformation Network, Parallel Resonance, S/D biasing**	**0.25μm SiGe BiCMOS**	**This Work**
10	1.81	21.9	10.1	0.67	Shunt	0.13μm SiGe BiCMOS	[46]
	2.25	23.1	11.1	0.58	Series/Shunt		
3−10	3.1±1.3	25−32	18−20	0.62	Distributed Topology	0.18μm CMOS	[49]
3−10.6	2.2−4.2	33−37	−	0.9	Synthetic Transmission Line	0.25μm CMOS	[50]
DC-20	0.7 at 10 GHz	32 at 10 GHz	25.4 at 10 GHz	0.06	Synthetic transmission line, body floating and biasing	0.18μm CMOS	[51]
15	1.8	23	15.1	0.2	ITNs	0.13μm CMOS	[52]
	1.8	17.8.1	21.5	0.25	No ITNs		

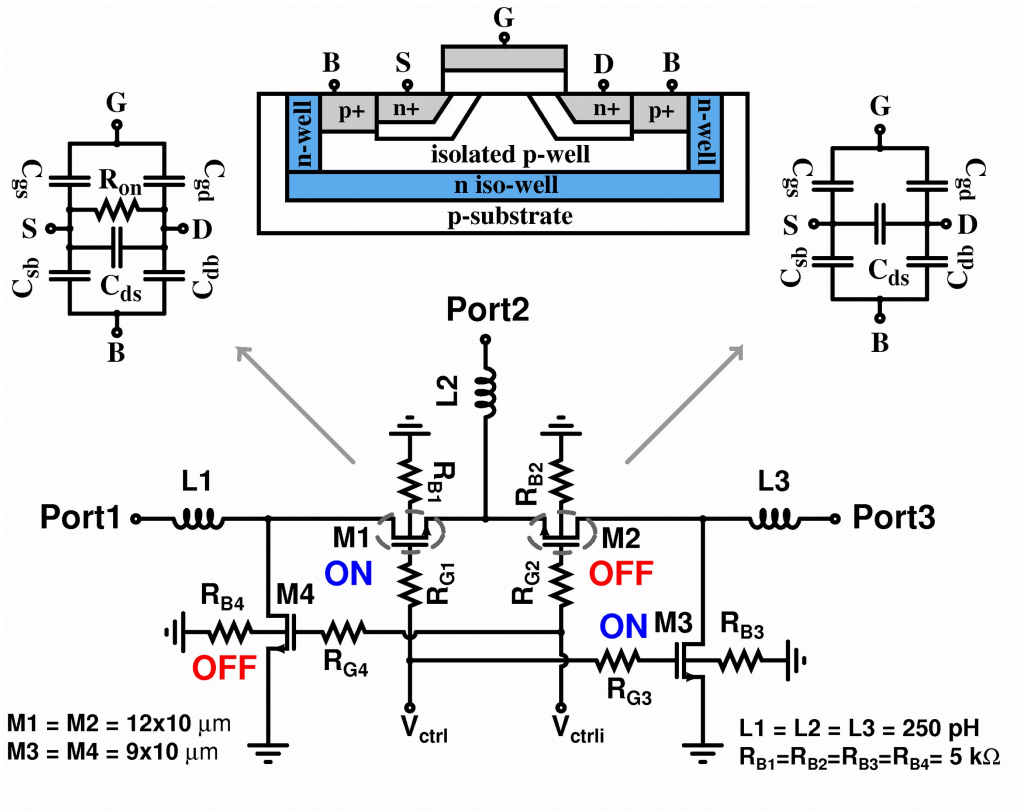

Figure 27: Circuit schematic of the designed SPDT switch and cross-sectional view of a typical isolated NMOS transistor.

In this section, the design and implementation of a fully integrated DC-20 GHz SPDT switch, optimized at X-Band for using in the T/R module, is presented. The switch is based on series-shunt topology. Resistive body floating and on-chip impedance transformation networks (ITN) are used to improve power handling capability (P_{1dB}) of the switch. Additionally, transistor widths are optimized to improve insertion loss (IL) and isolation. These techniques have already been explained in detail in Section 2.1 and will not be further discussed in this section. Here, we will mainly discuss the circuit design shortly.

2.2.2 Circuit Design and Analysis

Fig. 27 presents the schematic of the SPDT switch based on series-shunt configuration with resistive body floating and on-chip matching networks. The basic circuit models of the ON and OFF transistors are also shown in Fig. 27. Similar to the T/R switch, the main switching function is performed by M1 and M2 transistors while M3 and M4 transistors are employed to improve isolation. When V_{ctrl} is high and V_{ctrli} is low, M1 forms a low loss path between Port1 and Port2 while M2 is

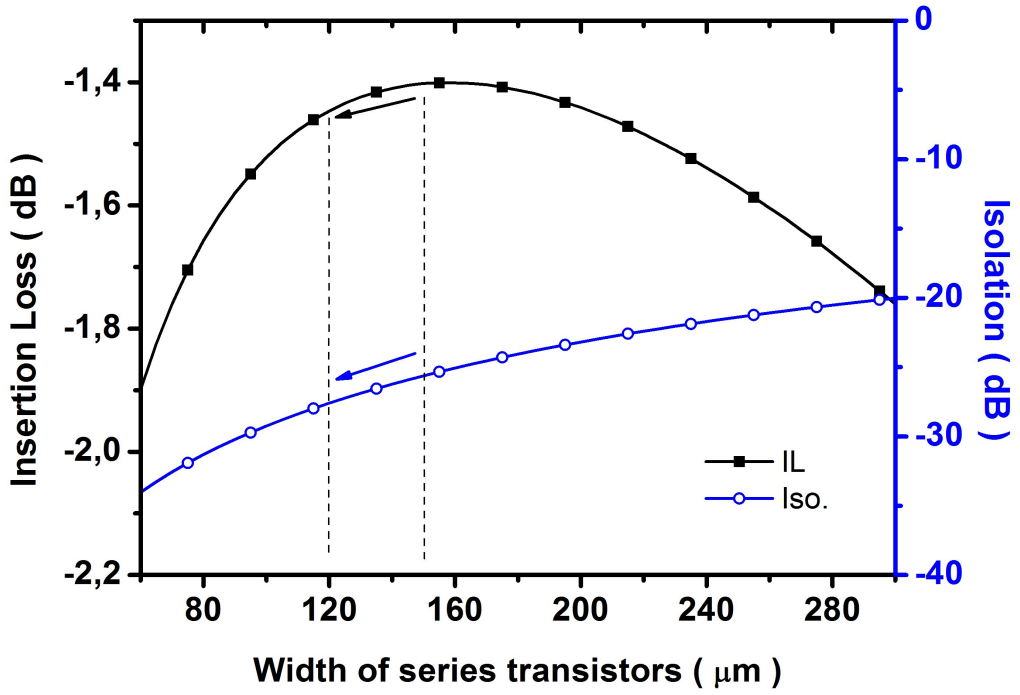

Figure 28: Simulated series transistor width versus insertion loss and isolation.

off and isolates Port3 from other ports. In this mode, M3 directs leakage signal to ground before reaching Port3. Due to symmetry, operation of the SPDT switch is similar when the control signals are inverted.

The SPDT switch is realized using the IHP SGB25V process. The transistors are based on isolated NMOS technology (iNMOS) which enables the use of transistors as four terminal devices to separate body of transistors from the common p-substrate and applying body floating technique. The transistor bodies are tied to ground using 5-kΩ resistors to improve power handling capability. Gate of series-shunt transistors are biased through 10-kΩ resistors, R_{G1}-R_{G4}, to make the gates of transistors float at AC signals. An optimization was done at 10 GHz using Cadence SpectreRF tool to determine transistor widths for minimum insertion while preserving sufficient isolation. Insertion loss is mainly dependent on the channel resistance of the switching transistor, M1 or M2, in the ON state. A transistor width of 150-μm for series transistors results in a minimum insertion loss at 10 GHz (Fig. 28). However, a transistor width of 120-μm (12 fingers) was chosen to improve isolation without significantly degrading insertion loss. Hence insertion loss was effectively traded for isolation. Then, a width of 90-μm (9 fingers) was chosen for shunt transistors, M3 and M4, to obtain desired isolation of 25 dB at 10 GHz. Although increasing width

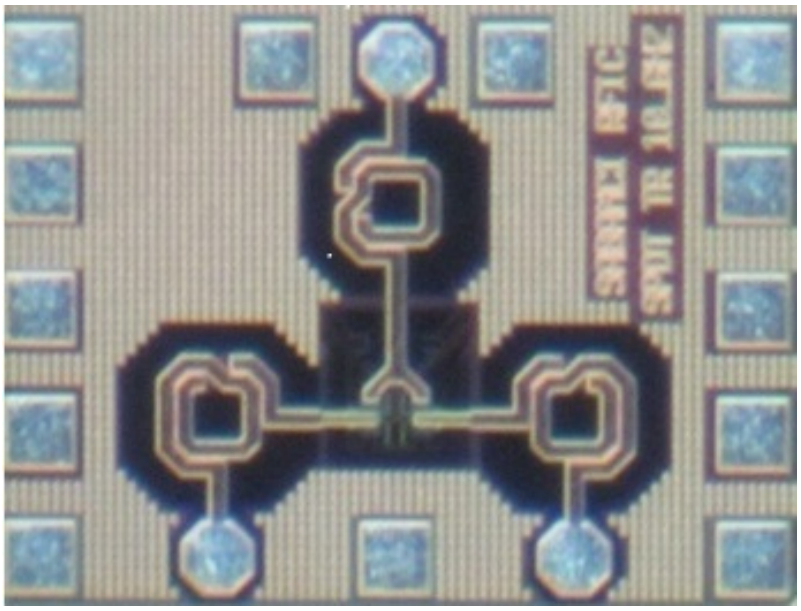

Figure 29: Die photo of the DC-20 GHz SPDT switch. The active chip area is 0.48x0.36 mm^2.

of shunt transistors improves isolation, parasitic capacitances introduced by wider transistors would degrade the insertion loss. Impedance transformation networks (ITNs) are implemented using 250 pH series inductors to improve power handling capability of the switch. These inductors are designed using Sonnet with the quality factors of ∼21 at 10 GHz and occupy an area of 160x160 μm^2.

2.2.3 Measurement Results

The SPDT switch was fabricated in IHP, 0.25-μm SiGe BiCMOS process. The die photo of the switch is shown in Fig. 29. The active chip area, without pads, is 0.48 μm x 0.36 μm = 0.18 mm^2. Inductors in the switch are custom designed using the thickest top metal layer in the process. Pad-to-pad S-parameter measurements were performed using the 20 GHz Agilent 8720ES network analyzer. Pads were simulated in the Sonnet EM solver and resulted in a loss of ∼0.1 dB at 10-20 GHz.

The SPDT switch resulted in a measured insertion loss of 0.5-3.1 dB at DC-20 GHz (Fig. 30). The measured isolation between Port3 and Port1 is better than 21 dB up to 20 GHz (Fig. 30). The measured return losses are shown in Fig. 31. The return losses at both input and output ports are better than 15 dB from DC to 20 GHz. S-parameter measurements agree well with the simulation results. The switch resulted in a P_{1dB} of 16-17.3 dBm from DC to 20 GHz (Fig. 32). The

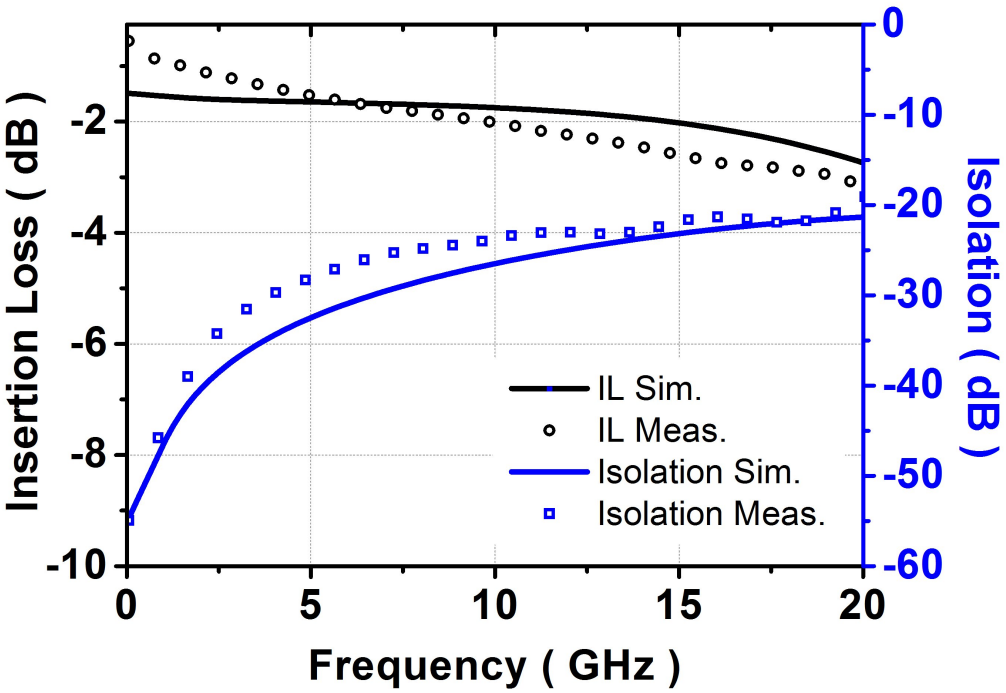

Figure 30: Measured insertion loss and isolation of the SPDT switch.

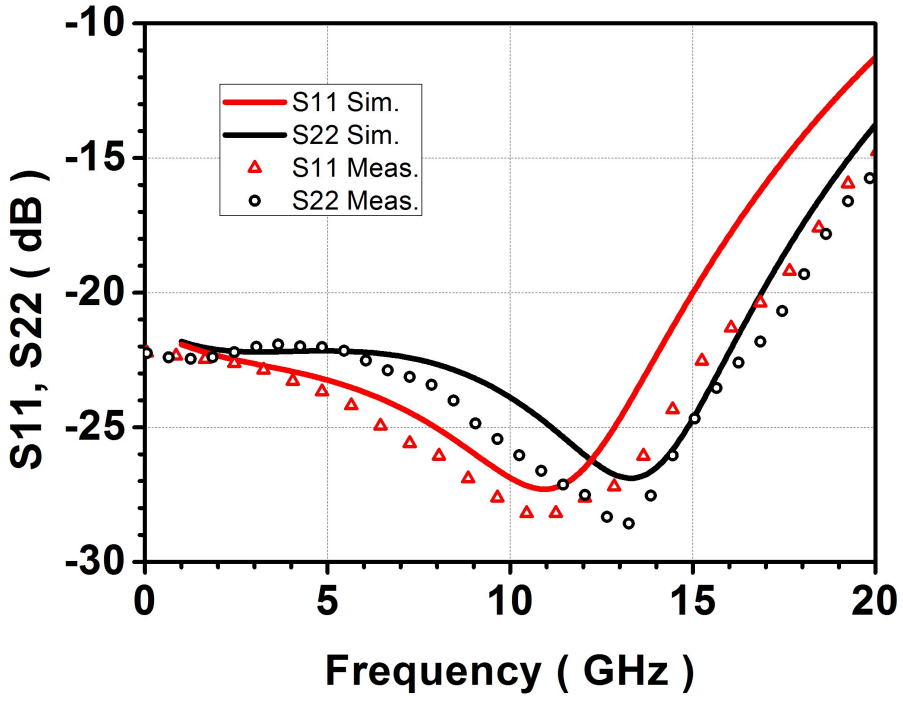

Figure 31: Measured and simulated return loss of the SPDT switch.

switch noise figure is measured to up 18 GHz (Fig. 33) by using E4407B spectrum analyzer with noise figure personality and Agilent 346A noise source. Agilent 87405C preamplifier was placed between the output of the SPDT switch and input of the spectrum analyzer to have sufficient sensitivity for the noise figure measurement.

The measured noise figure of the SPDT is between 1 dB and 3.58 dB at 1-18 GHz frequency range. The simulated rise and fall time of the switch are 1.9 ns and 1.6 ns, respectively.

2.2.4 Performance Comparison

Table 3 compares the performance of the presented switch with that of other wideband CMOS switches reported in the literature. Although the SDPT switch is primarily optimized for X-Band phased array applications, as seen in Table 3 it competes well with the reported switches for ultra-wide band applications. Therefore, apart from its utilization as one of the T/R module blocks, this switch is also a successful demonstration of the full integration of ultra-wideband SPDT switch in SiGe BiCMOS process.

Table 3: Comparison of the wideband CMOS SPDT switches

Frequency (GHz)	IL (dB)	Isolation (dB)	P_{1dB} dBm	Technology	Ref.
DC-20	<3.1	>21	16−17.3	0.25μm	This
DC-20	<2.0	>21	24.6−30	0.18μm	[40]
3−10	<4.4±1.3	>27	18−20	0.18μm	[49]
3−10.6	<4.2	>33	−	0.25μm	[50]
DC-20	<2.5	>25	19.8−26.2	0.18μm	[51]

2.3 An X-Band T/R Switch based upon Slow-wave Transmission Lines

2.3.1 Introduction

Although the T/R switch presented in section 2.1 has a remarkable power handling capability and isolation, it suffers from the relatively high insertion loss. The high insertion loss in this switch is mainly attributed to the NMOS transistor models (according to discussions with IHP, this issue is prevalent only for triode mode of operation) supplied in design kit. As discussed in section 2.1, the main switching function in this switch is performed by the series transistors which are placed in the signal flow route. The insertion loss is mainly dominated by these series transistors and modeling discrepancies in these have a direct impact on the measured

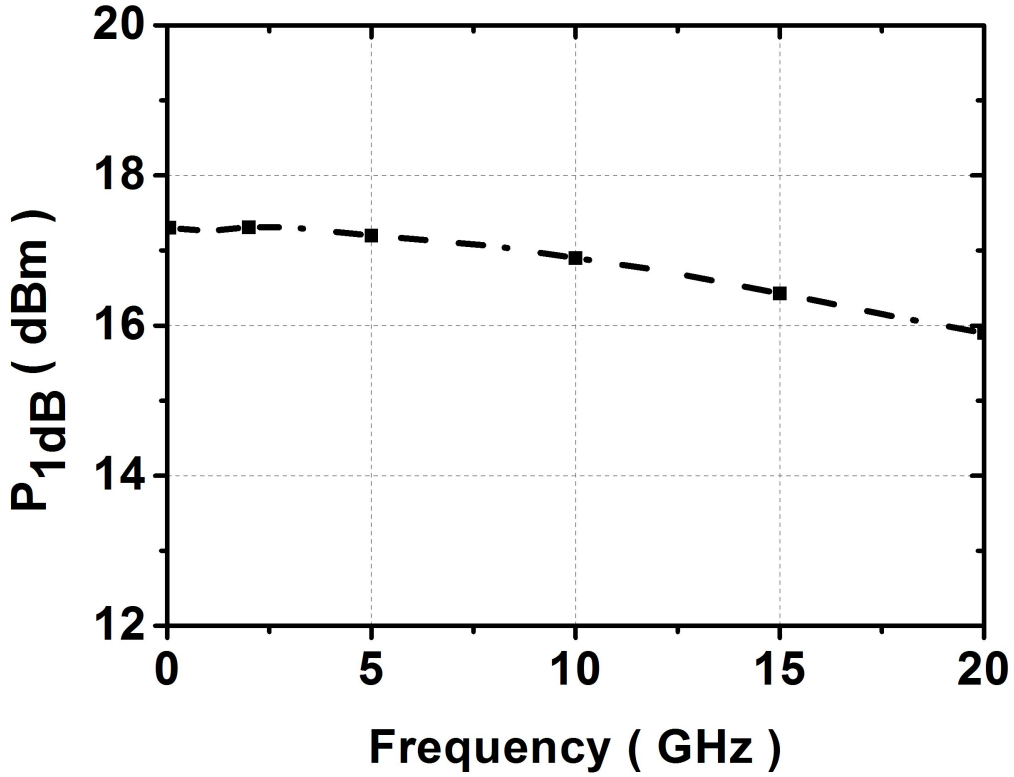

Figure 32: P1dB versus frequency of the SPDT switch.

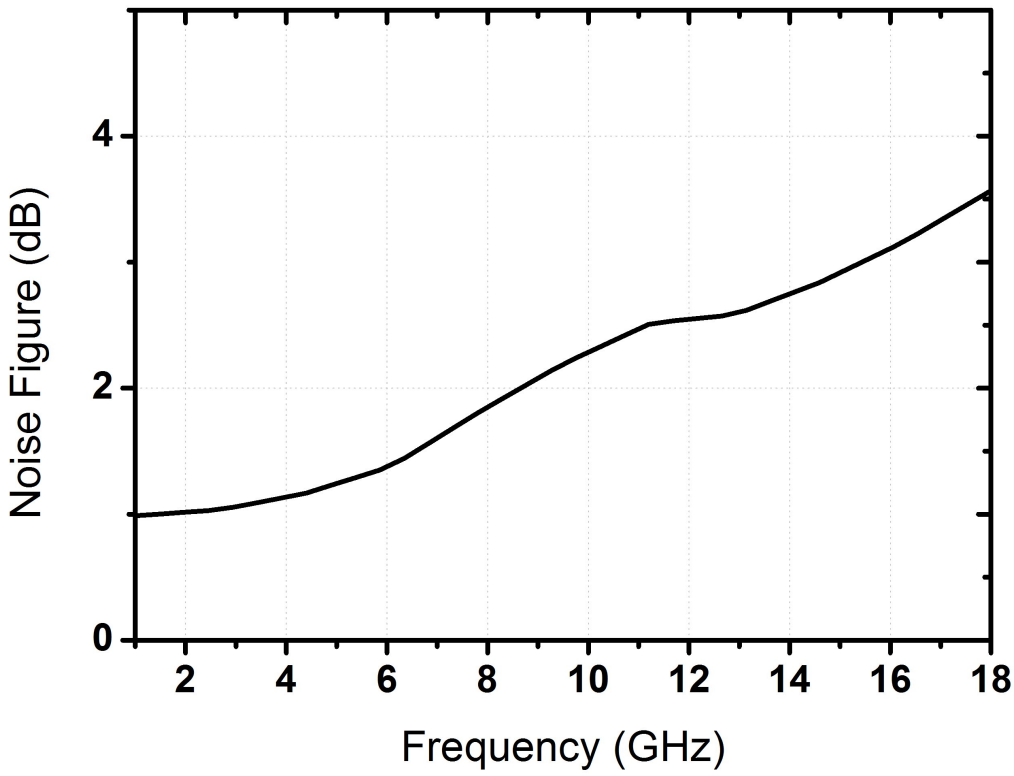

Figure 33: Measured noise figure of the SPDT switch.

insertion loss of the T/R switch. The use of the previous switch in the T/R module would significantly limit the overall system performance, especially noise figure and in return sensitivity of the system. To resolve this issue, we have focused on the topologies and techniques which would enable us to design a T/R switch which is less vulnerable to the modeling issues.

In this section, the design and implementation of an X-Band T/R switch based upon slow-wave microstrip transmission lines is presented. The switch employ only shunt NMOS transistors and the series transistors in the signal path are replaced by the quarter wavelength microstrip transmission lines to alleviate the discrepancies between simulations and measurements. Thus the designed switch is more robust and less dependent on the transistor models compared to the previous one. The main challenge in the design of this switch is to implement high quality quarter length transmission lines on chip by consuming a relatively small area at X-Band. To this end, the slow-wave concept has been employed for reducing the wavelength of the signal and in return minimizing the required chip area. Additionally, resistive body floating and DC biasing are used to improve the power handling capability of the switch. These techniques have already been explained in great detail in section 2.1. Therefore, here we will mainly focus on introducing slow-wave concept and the circuit design.

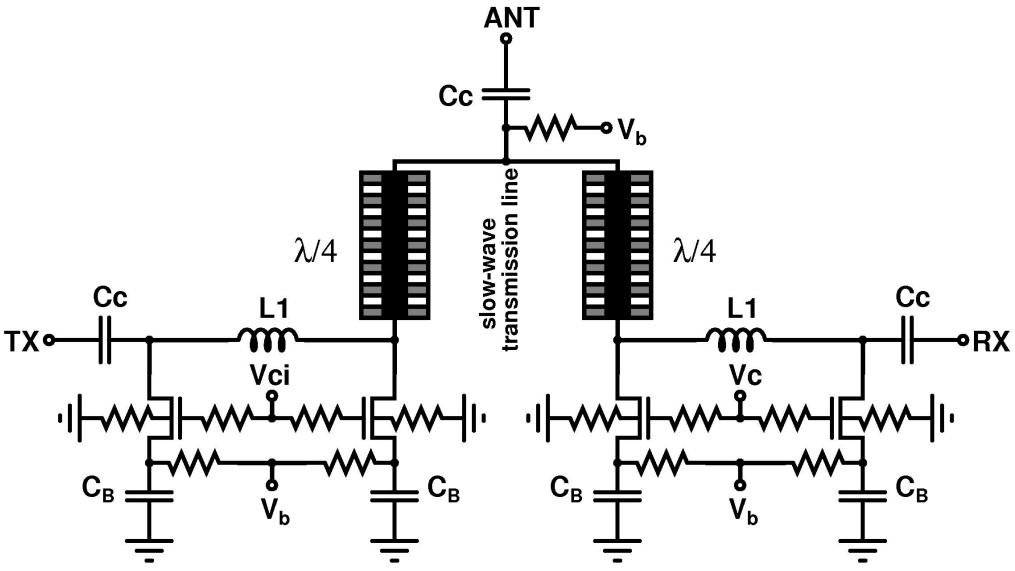

Figure 34: Schematic of the designed T/R switch using slow-wave transmission lines.

2.3.2 Circuit Design and Analysis

Fig. 34 shows the schematic of the T/R switch using slow-wave quarter wavelength ($\lambda/4$) transmission lines. The T/R switch is based on shunt-shunt configuration in order to improve the isolation further by grounding the leakage signal to the undesired port better [54], [55]. The operation of the switch is as follow: when V_c is high and V_{ci} is low the switch operates in the transmit mode. In this mode, $\lambda/4$ transmission line between ANT and RX ports transforms the low ON resistance of shunt switches into high impedance and thus isolates the RX port from the TX port while RF signal is routed from TX to ANT through the transmission line. Due to symmetry, operation of the SPDT switch is similar when the control signals are

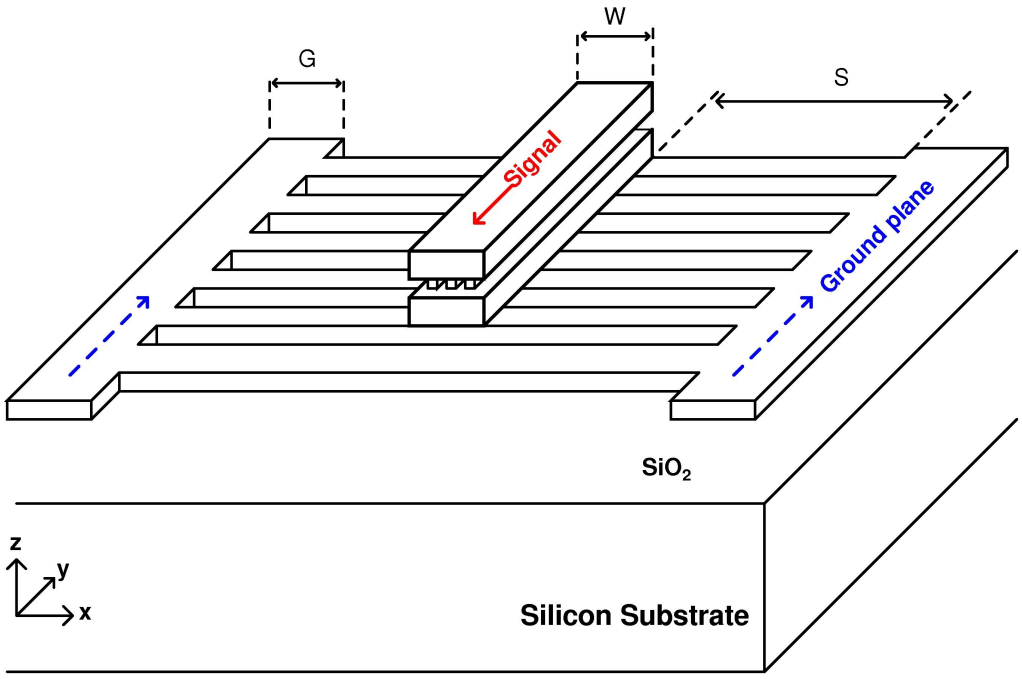

Figure 35: Structure of the slow-wave microstrip transmission line (S-MSL).

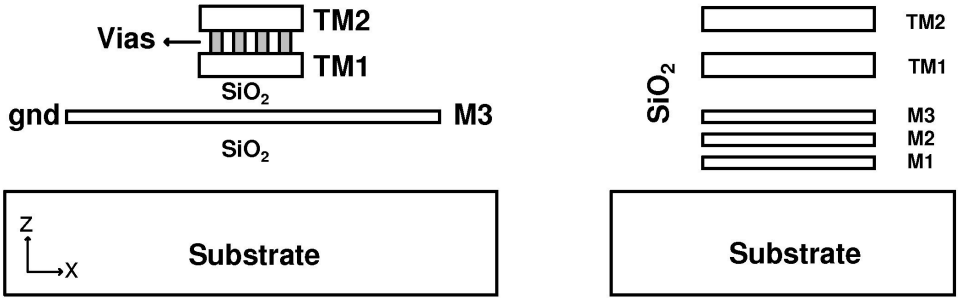

Figure 36: Simplified cross-section of the slow-wave transmission line and metal layers in the technology.

inverted. In this configuration, the insertion loss can be improved over the conventional series-shunt topology since the quarter transmission lines are used rather than series transistors which usually brings relatively high parasitic resistances in the signal path.

In order to integrate on-chip $\lambda/4$ transmission lines by consuming relatively small chip area and to improve the insertion loss, slow-wave microstrip lines are used [56–59]. This work presents the utilization of slow-wave transmission lines for the first time in T/R switches reported in any CMOS and BiCMOS technology to the date. Fig. 35 and Fig. 36 show the structure of the slow-wave microstrip transmission lines (S-MSL) and simplified cross-section of them along with the metal layers offered in BEOL of the technology. The 50 Ω transmission lines are built stacking 3-μm thick TM1 with 2-μm thick TM2 top metal layers with 6-μm width to reduce the attenuation while ground plane with metal slots orthogonal to the signal propagation direction are placed on the M3 layer. The distance between the signal line and ground plane is 0.9 μm. All metal layers are aluminum and insulator material between the metals is SiO_2.

Thereby the signal line is periodically loaded with capacitances. The wavelength of the propagating signal is calculated by

$$\lambda = \frac{\nu_p}{f} \tag{31}$$

where

$$\nu_p = \frac{1}{\sqrt{LC}} \tag{32}$$

and L is the inductance per unit length and C is the capacitance per unit length. From (31) and (32) both phase velocity and the wavelength can be reduced while keeping the characteristic impedance of the line constant by increasing L and C with the same ratio. As shown in Fig. 35, the signal line is periodically loaded with capacitances by grounded metal stripes orthogonal to the signal propagation direction. These stripes are implemented on M3 layer to increase the capacitance per length. Additionally, since the metal stripes are orthogonal to the propagation direction, the return current which is in the signal direction can only flow far away from the signal line and thus high inductance per unit length is provided [60]. By

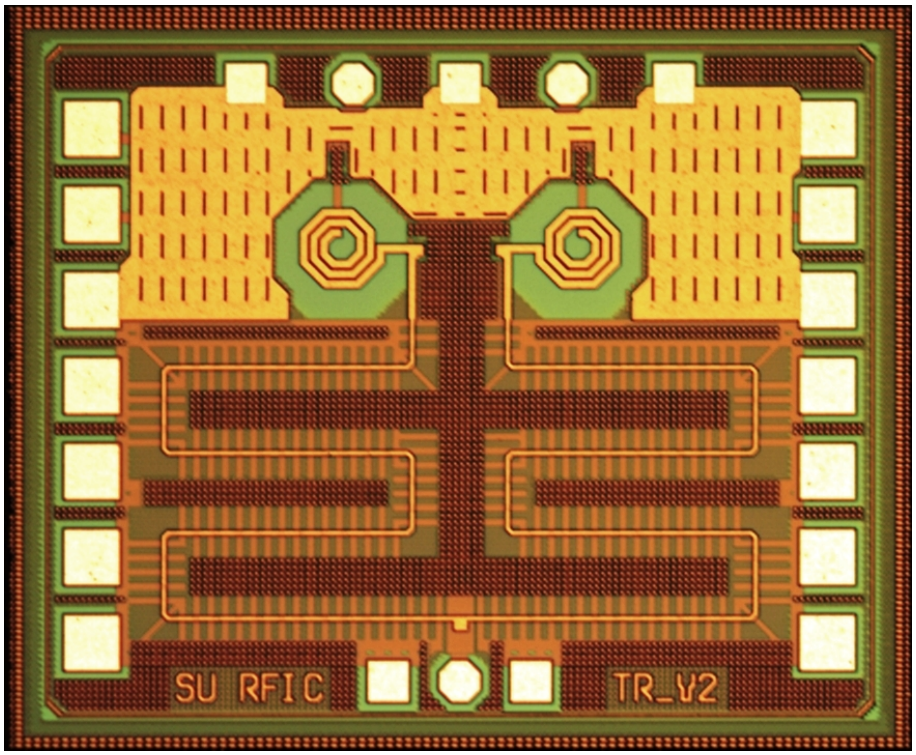

Figure 37: Die photo of the DC-20 GHz SPDT switch. The active chip area is 0.48x0.36 mm^2.

arranging the metal stripe and slot widths, L and C can be increased by the same ratio while keeping the 50 Ω characteristic resistance. For this purpose, the width of the grounded metal stripes under the signal line is set as 10-μm and they are separated by 10-μm slot widths. The ground plane with the metal slots under the signal line also prevents E-field to penetrate into the lossy substrate and thus reduces the loss of the S-MSL. The EM simulations of the slow-wave microstrip lines were performed in Sonnet. The electrical length of $\lambda/4$ is achieved with 1700-μm long S-MSL with a simulated loss of 0.25 dB/mm at 10 GHz. This means a reduction of 50% wavelength at 10 GHz.

In addition to the slow-wave concept, a variety of techniques were incorporated into the design to improve power handling capability (IP_{1dB}). Firstly, drains and sources of the all transistors were biased with 2 V to improve IP_{1dB}. In addition, resistive body floating technique is used to improve IP_{1dB} further. The isolated NMOS transistors are used to separate the body of each transistor from the common p-substrate. The transistor bodies are connected to the ground through 5-kΩ resistors to reduce coupling to the substrate via junctions and in return improve the insertion loss and power handling capability. The transistor widths are equal and

an optimized considering the trade-off between the insertion loss and isolation. A transistor width of 300 μm (15 fingers) was chosen for shunt transistors. The matching at TX or RX port are achived with pi-type networks formed by the equivalent off-state capacitances of two shunt transistors and 600 pH on-chip inductors.

2.3.3 Measurement Results

The T/R switch was fabricated in IHP 0.25-μm SiGe BiCMOS process. The die photo of the T/R switch is shown in Fig. 37. The active chip area, excluding pads, is 770 μm x 950 μm = 0.73 mm^2. L1 Inductors laid out on the signal path and they are custom designed using the thickest top metal layer in the process to achieve higher quality factors.

Pad-to-pad S-Parameter measurements were performed using the 20 GHz Agilent 8720ES network analyzer under 2 V bias with 4.5 V and 0 V control voltages. Fig. 38 shows the measured insertion loss and isolation of the T/R switch. The T/R switch resulted in a measured insertion loss of 2.3 dB and 39 dB isolation at 10 GHz. The isolation of the T/R switch across the X-Band is between 39-42 dB. The insertion loss of the switch is between 2.1 dB and 2.9 dB across the X-band

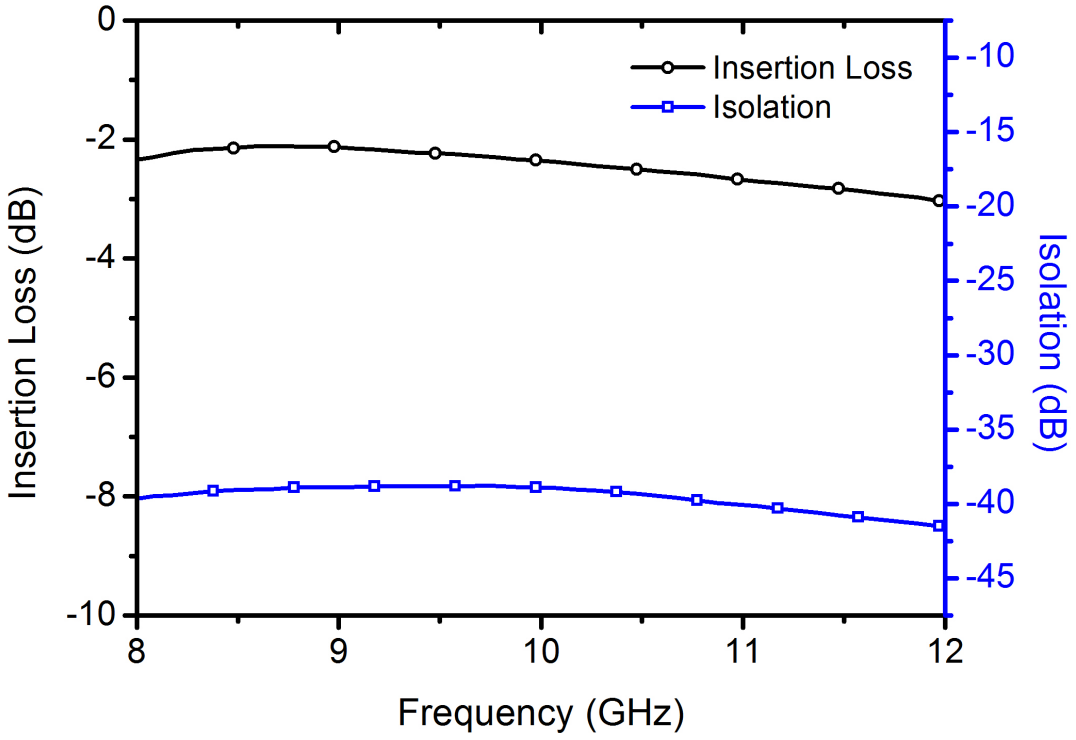

Figure 38: Measured insertion loss and isolation of the S-MSL based T/R switch.

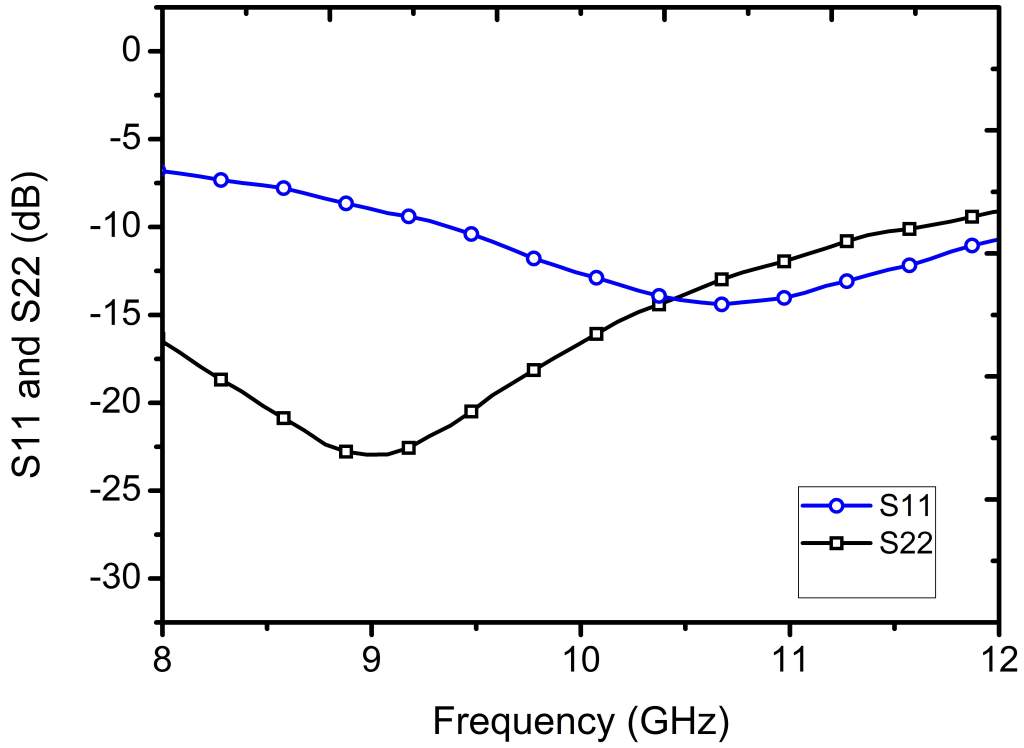

Figure 39: Measured return losses of the S-MSL based T/R switch.

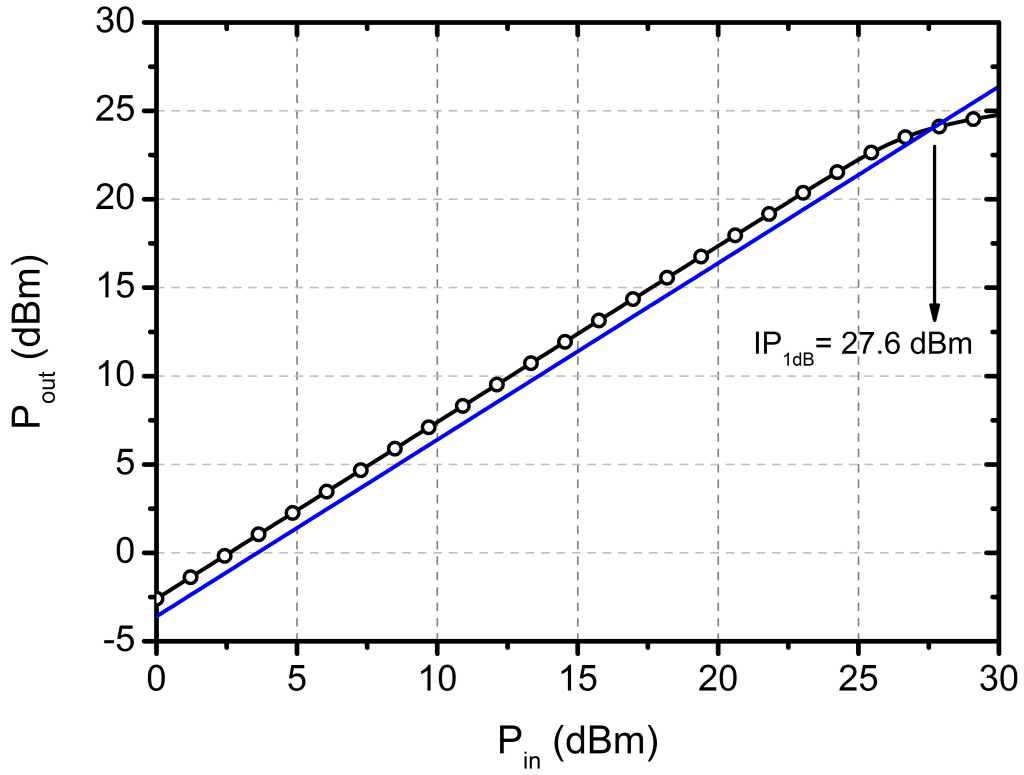

Figure 40: Measured 1 dB compression point (IP_{1dB}) of the T/R switch at 10 GHz.

frequencies. The RF Pads were simulated in the Sonnet EM solver and resulted in a loss of ∼0.1 dB at 10 GHz. Therefore, an insertion loss of 1.9 - 2.7 dB at X-Band is expected for the switch when it is integrated into the complete module. The return losses at both input and output ports are shown in Fig 39. The return loss at TX port, S11, is 13 dB at 10 GHz and varies from 7 dB to 14 dB at X-Band. The S22 is 16 dB at 10 GHz and changes from 9 dB to 22 dB across the X-Band frequencies. Insertion loss and return losses are almost same in both transmit and receive mode due to the symmetry of the switch.

Power handling capability of the switch was evaluated by one-tone simulations and measurements. Fig. 40 shows the simulated input referred 1-dB compression point (IP_{1dB}) of the T/R switch for a single-tone input signal at 10 GHz. As shown in Fig. 40 the switch results in a simulated IP_{1dB} of 27.6 dBm at 10 GHz. The IP_{1dB} is measured using Agilent E4417A power meter. Due to the physical limitations, the power handling capability of the switch was measured up to 23.5 dBm input signal at 10 GHz (maximum signal level supplied by signal generator was 25 dBm and cable loss before the input port of the switch is ∼1.5 dB). During these measurements, even 0.1 dB compression was not observed up to 23.5 dBm input signal applied. Therefore, it is expected that the measured 1 dB compression point would be rather compatible with the simulated value.

2.3.4 Performance Comparison

Table 4 compares performance of the presented switch with that of other single-ended CMOS T/R switches reported in the literature, operating at X-Band. As can be seen, it can provide a low insertion loss and an excellent isolation and a high power handling capability simultaneously at X-Band. It is attributed to the utilization of slow-wave transmissions lines in T/R switch design for the first time in any BiCMOS technology to the date as well as combining various techniques in an effective way.

Table 4: Comparison of the T/R switch based upon slow-wave transmission lines with the state-of-the-art reported works

Frequency (GHz)	Figures of Merit			Chip Area mm^2	Technique	Technology	Ref.
	IL (dB)	Isolation (dB)	P_{1dB} dBm				
8−12	**2.1−2.9**	**39−42**	**27.6**	**0.73**	**Shunt, Body floating, Slow-wave Microstrip Lines, S/D biasing**	**0.25μm SiGe BiCMOS**	This work
8−12	3.2−4.1	23.2−34.8	28.2	0.44	Series-shunt, Body floating, Impedance Transformation Network, Parallel Resonance, S/D biasing	0.25μm SiGe BiCMOS	[61]
10	1.81	21.9	10.1	0.67	Shunt	0.13μm SiGe BiCMOS	[46]
	2.25	23.1	11.1	0.58	Series/Shunt		
3−10	3.1±1.3	25−32	18−20	0.62	Distributed Topology	0.18μm CMOS	[49]
3−10.6	2.2−4.2	33−37	−	0.9	Synthetic Transmission Line	0.25μm CMOS	[50]
DC-20	0.7 at 10 GHz	32 at 10 GHz	25.4 at 10 GHz	0.06	Synthetic transmission line, body floating and biasing	0.18μm CMOS	[51]
15	1.8	23	15.1	0.2	ITNs	0.13μm CMOS	[52]
	1.8	17.8.1	21.5	0.25	No ITNs		

3 SiGe HBT Low Noise Amplifiers for the X-Band T/R Module

3.1 An X-Band, High Performance, SiGe-HBT LNA for Phased Array Radar Applications

3.1.1 Introduction

In the recent years, design of the building blocks of X-Band T/R modules, based on SiGe BiCMOS technology, has become an active area of research. In this section we present the design and implementation of a LNA using 110 GHz SiGe BiCMOS technology for X-Band, on-chip phased T/R module. The LNA is composed of two cascode stages using SiGe HBTs to achieve low noise figure, high gain and a better matching to 50 Ω at the input and output, simultaneously. First stage is designed for low noise performance while the second stage is optimized to improve the IIP_3.

As discussed in Section 1.6, LNA comes right after the T/R switch. Therefore, along with the T/R switch, it has a stronger effect on the overall noise figure and, in return, sensitivity of the radar system. The designed LNA for the T/R module should have low noise figure (less than 2 dB), high gain (better than 15 dB) and high IIP3 (better than -10 dBm) to achieve a high dynamic range of operation. These are clearly challenging performance specifications to achieve simultaneously in a SiGe BiCMOS technology.

This section is organized as follows. Section 3.1.2 presents the SiGe technology, used to fabricate LNA. In Section 3.1.3, circuit design procedure of the LNA is discussed. Measurement results and comparison of the LNA with the reported works in literature are presented in Section 3.1.4. Finally, Section 3.1.5 compares the presented LNA with the state-of-the-art X-Band LNAs reported in the literature.

3.1.2 SiGe HBT Technology

In this work, a high performance 0.25-μm SiGe BiCMOS technology, SG25H3, offered by IHP-Microelectronics, was used to design the LNA. This technology mainly offers three types of HBTs; high-speed, high and low voltage. In this work, only high-speed HBTs with peak f_T/f_{max} of 110/180 GHz and 2.3V breakdown voltage

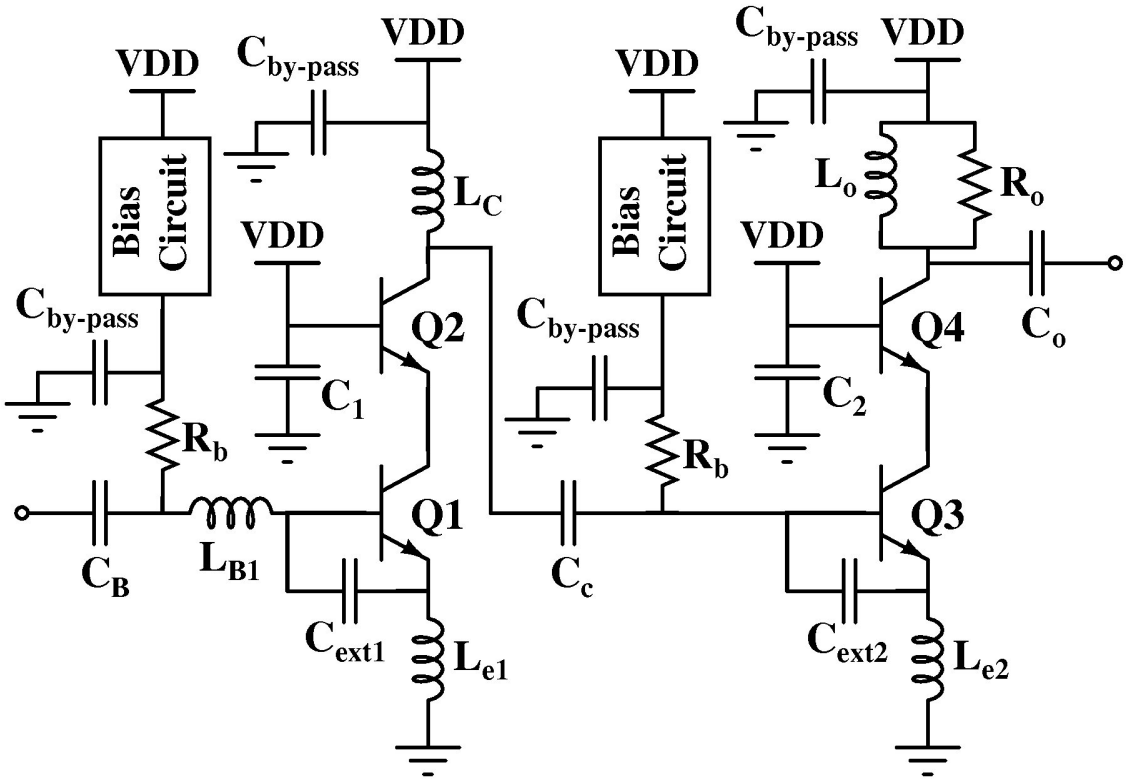

Figure 41: Schematic of the designed two-stage low noise amplifier.

were used to meet the low noise figure requirement of the T/R module. This technology also provides 2.5 V MOS transistors, isolated NMOS transistors and a full set of passive devices, including three types of polysilicon resistors with different precisions and metal-insulator-metal capacitors. The back-end of the technology offers three thin aluminum metal layers along with two thick metal layers for high quality on chip inductor and transmission line design.

3.1.3 Circuit Design Procedure

The circuit schematic of the designed LNA is shown in Fig. 41, excluding the bias circuitry. The LNA is implemented in two stages in order to obtain a gain in the excess of 15 dB and a better output matching to 50-Ω across the X-Band frequency range, simultaneously. The both stages are based on inductively-degenerated cascode topology due to its advantages of high frequency operation and stability at higher frequencies [24].

A well known design methodology for simultaneous noise and power matching is used with minor modifications in the design of the each cascode stage [62].

3.1.3.1 First Stage Design for Minimum Noise Figure

In order to obtain a good noise performance in the two-stage LNA, the first cascode stage is the most important stage, as presented by Friis's equation [63]

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_2 G_1} + ... \tag{33}$$

where F_1 is the noise figure of the first stage and G_1 is the gain. Noise figure of the second stage does not have a significant effect on the overall noise figure as long as the gain of the first stage is sufficiently high. Therefore, optimization of the first stage for minimum noise figure with sufficient gain is required.

The design methodology of the first cascode stage includes four steps:

1. NF_{min} of the common-emitter HBT device which dominates the noise figure in cascode configuration is given by [64]

$$NF_{min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_C}{V_T}(r_e + r_b)_u \left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}} \tag{34}$$

   where r_b and r_e are the base and emitter ohmic resistance, f is the operating frequency, f_T is the unity current gain frequency, J_C is the collector current density, β_{DC} is the current gain. As can be seen in (34), NF_{min} is a function of J_C, equivalently base-emitter voltage (V_{BE}), and independent of the transistor dimensions. Therefore, as the first design step, an optimum base-emitter voltage, $V_{BE,opt}$, which leads to optimal collector current density, $J_{C,opt}$, for NF_{min} was determined with transistors Q1 and Q2 sized as unit devices with emitter area of 0.22-μm x 0.84-μm. However, a V_{BE} of 0.83 V, higher than $V_{BE,opt}$, was selected to improve the gain and input third-order intercept point, IIP_3, of the first stage, without degrading NF_{min} significantly.

2. In order to achieve the minimum noise figure (NF_{min}) with a simultaneous power match in the first stage, an optimum source resistance ($R_{s,opt}$) should be set equal to system impedance, typically 50 Ω. A simplified equation of $R_{s,opt}$ to achieve NF_{min} is given by [65]

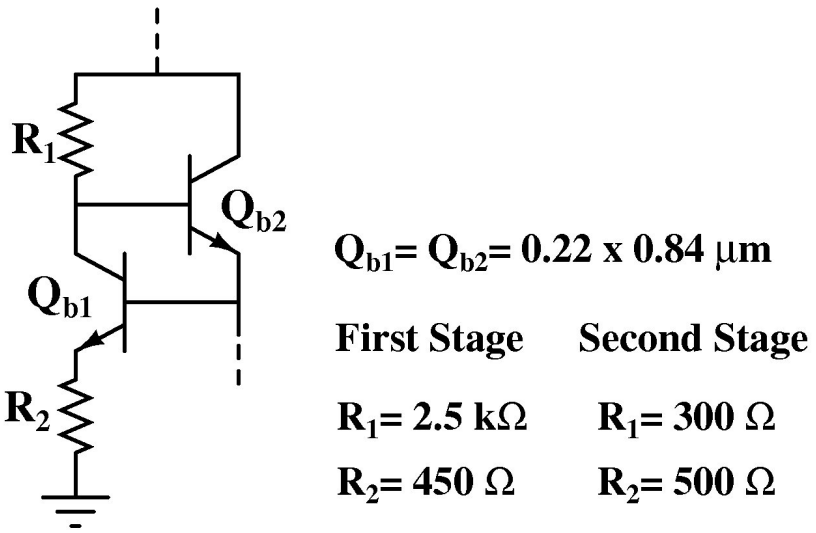

Figure 42: Schematic of the active bias circuit.

$$R_{s,opt} = \frac{f_T}{f}\frac{1}{L_E}\sqrt{\frac{2}{J_C}\frac{r_b L_E}{W_E}\frac{kT}{q}} \tag{35}$$

where L_E is the emitter length and W_E is the emitter width of the HBT. Equation explicitly shows that optimum source resistance $R_{s,opt}$ can be arranged by scaling L_E while maintaining $J_{c,opt}$ in order not to disturb NF_{min}. However, scaling L_E increases the current drawn and power consumption. In addition to scaling L_E, different from the conventional methodology, an external capacitance, C_{ext1}, was added between base-emitter terminals of Q1 to set $R_{s,opt}$ to 50 Ω. The effect of the C_{ext1} on $R_{s,opt}$ comes through f_T. f_T is a function of the base-emitter capacitance and with the addition of C_{ext1}, the overall base-emitter capacitance changes. Hence noise figure is effectively traded for power dissipation in this method. Here, $R_{s,opt}$ is set to 50 Ω by scaling unit device size 10 times and using a C_{ext1} of 115 fF.

3. Next step is to match input impedance to source resistance of 50 Ω by using an emitter degeneration inductor (L_{e1}) and a base-emitter inductor (L_{B1}). The input impedance looking into first stage is given by

$$Z_{in} = j\omega(L_{e1} + L_{B1}) + \frac{1}{j\omega(C_\pi + C_{ext1})} + \frac{g_m L_{e1}}{C_\pi + C_{ext1}} \tag{36}$$

where ω is the operating frequency. As can be seen in (36), L_{e1} sets the real

part of input impedance to 50 Ω, improving the linearity, IIP_3, of the first stage at the expense of the gain. L_{B1} tunes out the imaginary part of the input impedance and brings optimum noise reactance to 0 Ω. Here, a L_{e1} of 160 pH and L_{B1} of 1.15 nH are custom designed with peak Q of higher than 20 at 10 GHz. The input network can simply be considered as a series RLC network with a quality factor given by [10]

$$Q_{in} = \frac{1}{\omega_0 \left[g_m L_{e1} + R_s(C_{ext1} + C_\pi)\right]} \tag{37}$$

where ω_0 is the center frequency and R_s is the source resistance. As seen in (37), C_{ext1} also serves as to decrease the quality factor, Q_{in}, of the input network and thus increase the input bandwidth.

4. Finally, to conclude the first stage design, this stage is reactively loaded with an inductor L_C of 1.1 nH to achieve higher gain at operating frequency range of interest.

3.1.3.2 Second Stage Design and Optimization

The second stage is featured to increase the overall gain of the LNA further and to provide a good output matching to 50 Ω over all X-Band frequencies. The matching of the LNA output is crucial since the SPDT switch requires a well matched input [66]. The second stage is also a cascode configuration with an emitter degeneration inductor, L_{e2}, serving mainly as to improve the IIP_3 of the second stage by creating a negative feedback. The value of the L_{e2} is selected without degrading the gain significantly.

Design procedure of the second stage is basically similar to the method described for the first stage. In this stage, Q3 and Q4 transistors were biased with V_{BE} of 0.89 V which leads to a higher current density than the first stage in order to improve the gain and linearity. The total area of Q3 and Q4 transistors is 0.22-μm x 6.72-μm (8 times of unit device size), resulting in 7.5 mA current draw from 2.2 V supply. A wider output matching was achieved by using a shunt inductor (L_o of 1.15 nH) and series capacitor (C_o of 440 fF). C_o also serves as DC blocking capacitor. Contrary to the first stage output, a parallel resistance, R_o of 100 Ω, was also added to ease

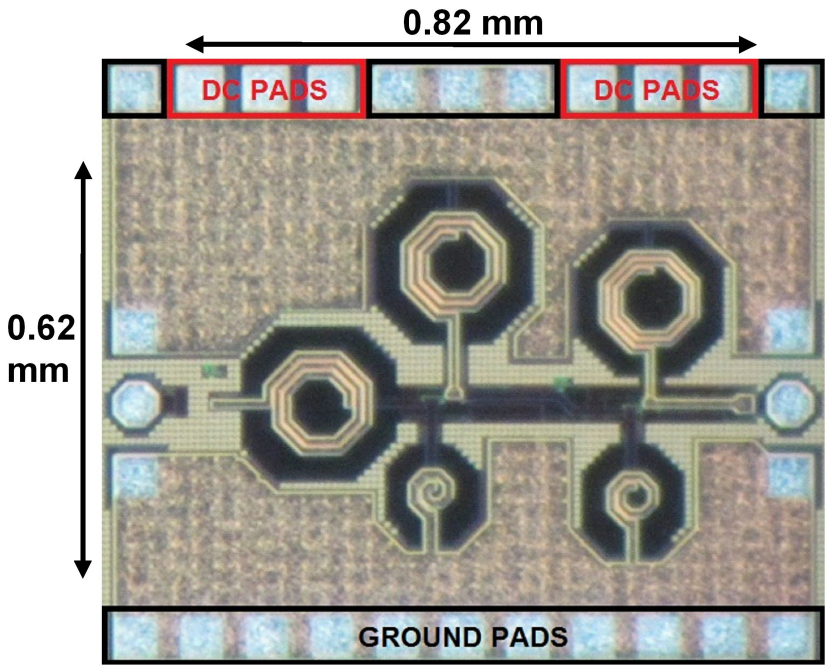

Figure 43: Micrograph of the X-Band two-stage low noise amplifier.

the output matching. The interstage matching between first and second stages was provided by C_c of 180 fF, C_{ext1} of 95 fF and L_{e2} of 250 pH.

Both cascode stages were biased using the active bias circuit, shown in Fig. 42. The bias circuits were connected to the base of Q1 and Q3 transistors through R_b resistors, having a value of 5 $k\Omega$ in order to keep their contribution to overall noise figure negligibly small and to prevent the additional noise coming from bias circuitry. In addition, by-pass capacitors, $C_{by-pass}$ are added to filter out the noise, generated by bias circuits, as well as to define RF ground at the operating frequency.

3.1.4 Measurement Results

The die photo of the LNA is shown in Fig. 43. The chip area, excluding the pads, is only 620 μm x 820 μm = 0.51 mm^2. Inductors in the LNA are custom designed using the thickest top metal layer to achieve higher quality factors, required for the inductors, especially for those used in input matching, in order to improve noise figure of the LNA.

A printed circuit board (PCB) was fabricated for testing the LNA. The LNA was glued on the PCB ground using an electrically conductive adhesive. The ground and DC pads of the LNA chip were wire-bounded to the corresponding ground

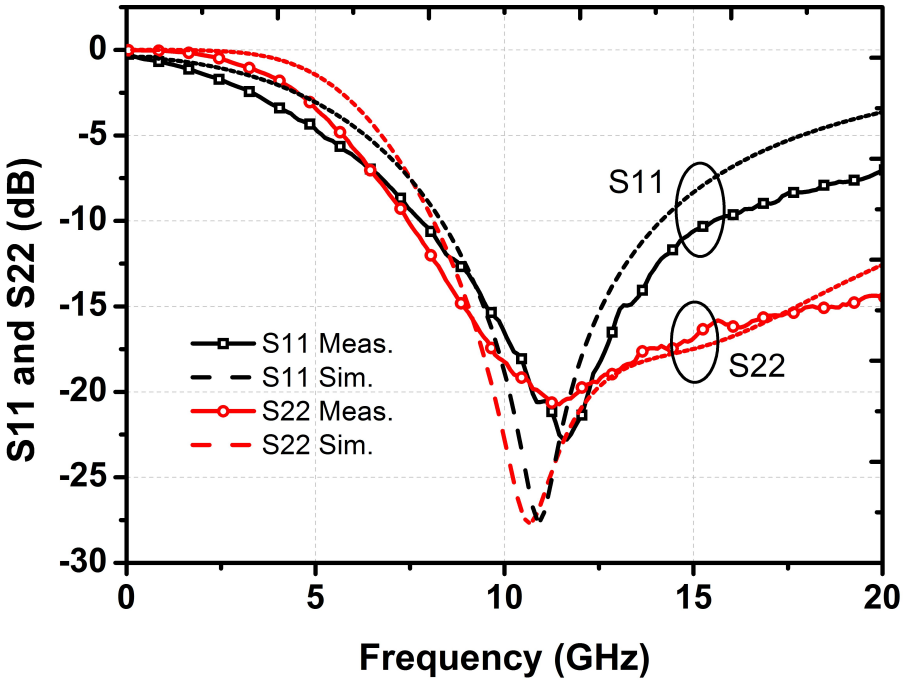

Figure 44: Measured S_{11} and S_{22} of the LNA (input and output matching).

and biasing paths on the PCB. Off-chip DC supply bypass capacitors were used to alleviate low frequency oscillation. The measurements of the LNA were directly performed on the LNA die using Cascade Microtech 40 GHz GSG probes. The bias current is 2.5 mA and 7.5 mA from 2.2 V supply voltage for the first and second stages (10 mA total current from 2.2 V), respectively. Thus, power consumption of the LNA is 22 mW.

S-parameters of the LNA were measured using Agilent 8720ES network analyzer at room temperature. Fig. 44 shows the input and output return losses, S_{11} and S_{22}, of the LNA from DC to 20 GHz. The measured S_{11} and S_{22} values are lower than -10 dB from 7.5 GHz to 15.5 GHz. The S_{11} varies between -11 dB and -22 dB across the X-Band frequency range. The S_{11} starts with -11 dB at 8 GHz and decreases to its minimum of -22 dB at 11.5 GHz. The measured S_{22} varies between -12 dB and -20.5 dB across X-Band. The S_{22} starts with -12 dB at 8 GHz and decreases to its minimum of -20.5 dB at 11.5 GHz. The gain (S_{21}) and reverse isolation (S_{12}) of the LNA are shown in Fig. 45. The S_{21} is higher than 19 dB from 8 to 14.5 GHz and reaches its maximum at 11.5 GHz. The measured 3-dB bandwidth of the LNA is from 8 to 14.5 GHz, which covers entire X-Band and some portion of the Ku-Band. The reverse isolation, S_{12}, is less than -47 dB at X-Band. This higher BW can be attributed to the effectiveness of the output matching network, formed by L_o, C_o

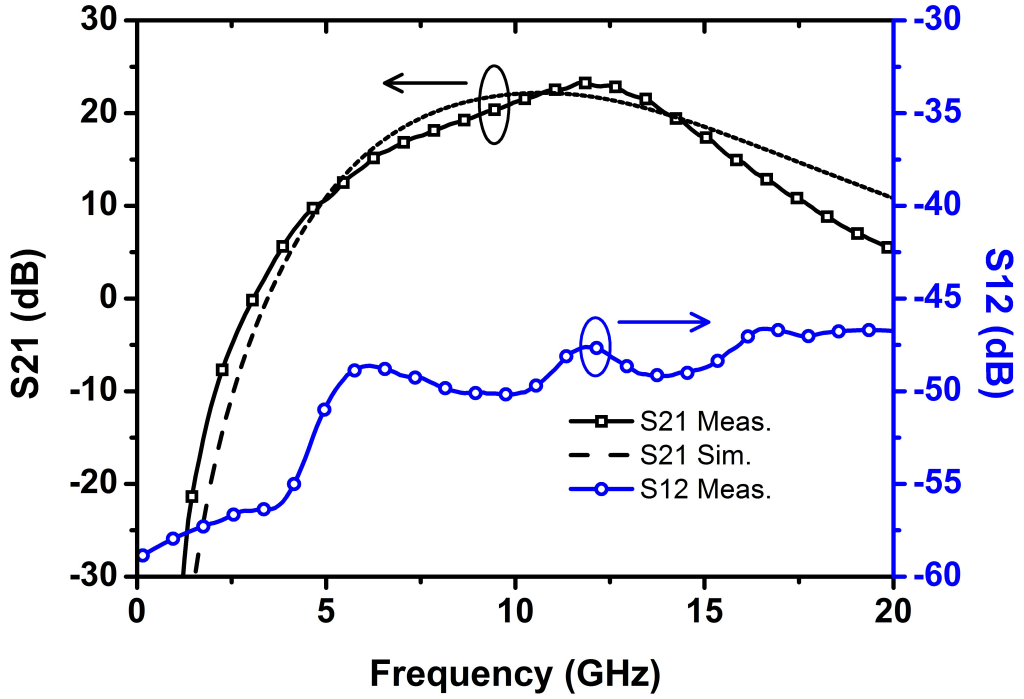

Figure 45: Measured S_{21} and S_{12} of the LNA (gain and isolation).

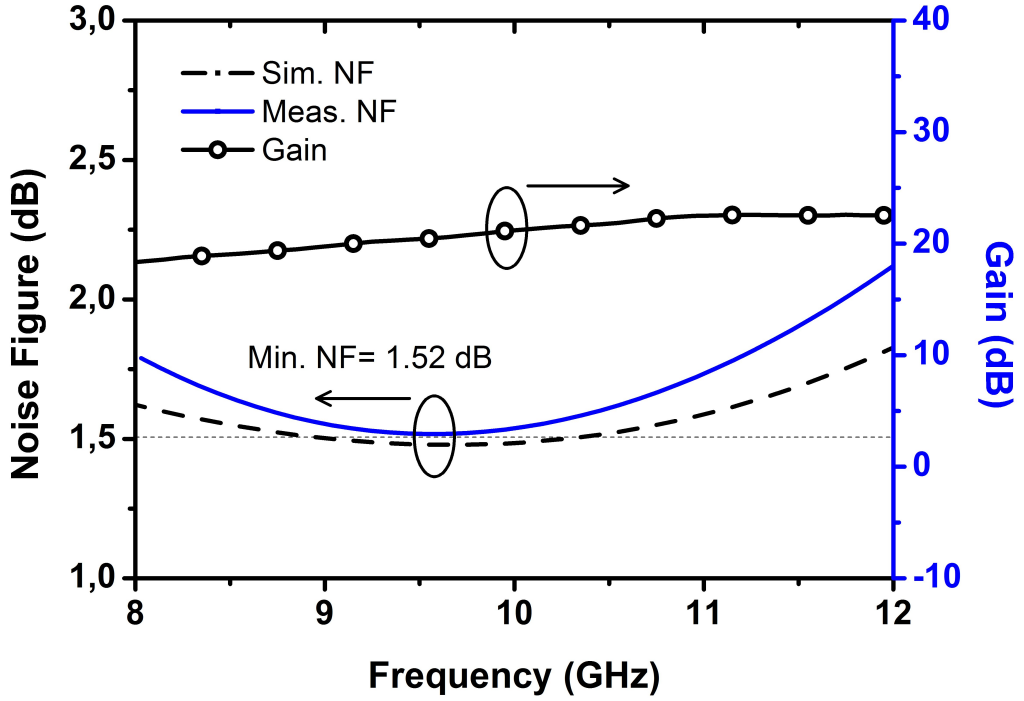

Figure 46: Measured noise figure and gain of the LNA across X-Band.

and R_o in the second stage.

Fig. 46 shows the measured and simulated noise figure of the LNA across the X-Band frequency range and Fig. 47 shows the measurement setup. The measured noise figure agrees well with the simulation results. The LNA noise figure is measured

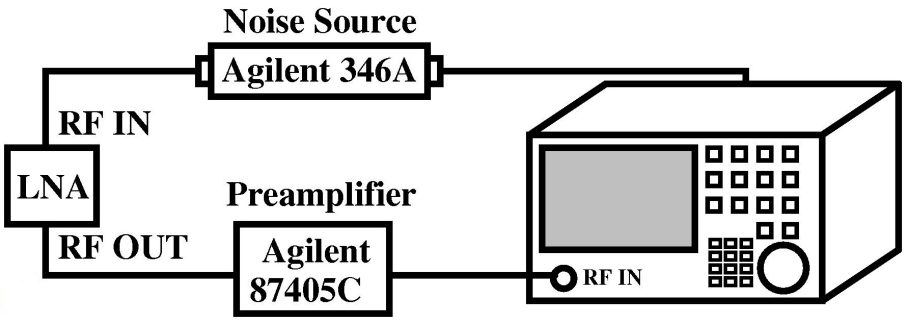

Figure 47: Measurement setup for noise figure.

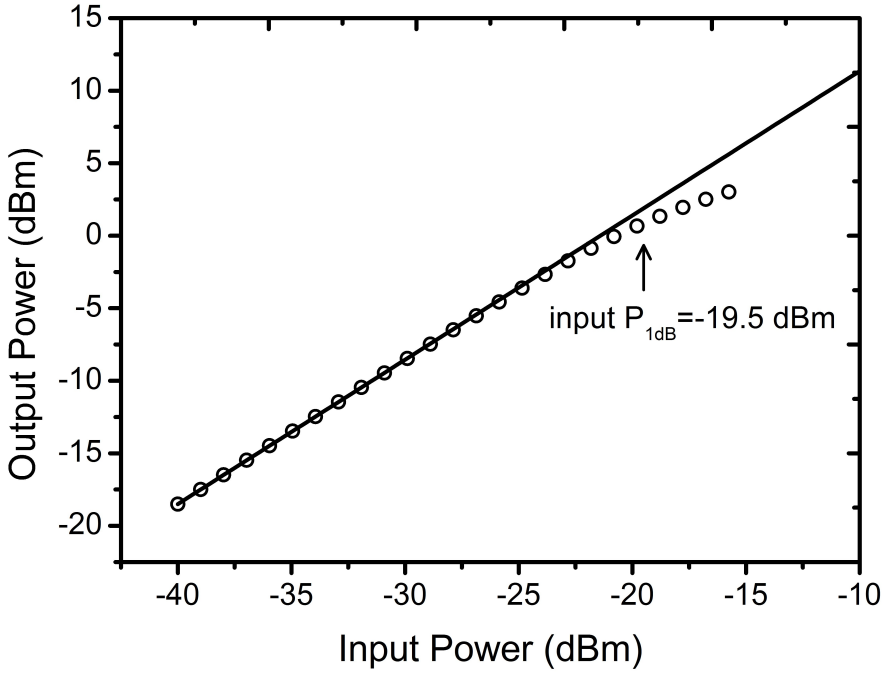

Figure 48: Measured 1-dB compression point of the LNA.

using E4407B spectrum analyzer with noise figure personality and Agilent 346A noise source. The cable and probe losses between output of the noise source and the LNA input were taken into account during the measurement. Agilent 87405C preamplifier was placed between the output of the LNA and input of the spectrum analyzer to have sufficient sensitivity for measuring low noise signals. The measured noise figure is 1.52-2.1 dB across the X-Band with a mean of 1.65 dB, competitive or better than other X-Band LNAs realized using SiGe technology reported to date. It is attributed to the effective biasing and the methodology to set $R_{s,opt}$ to 50 Ω in the first stage as well as high quality factor of custom designed inductors.

The linearity of the LNA was evaluated by one-tone and two-tone measurements. Fig. 48 shows the 1-dB compression point (P_{1dB}) of the LNA for a single-tone input

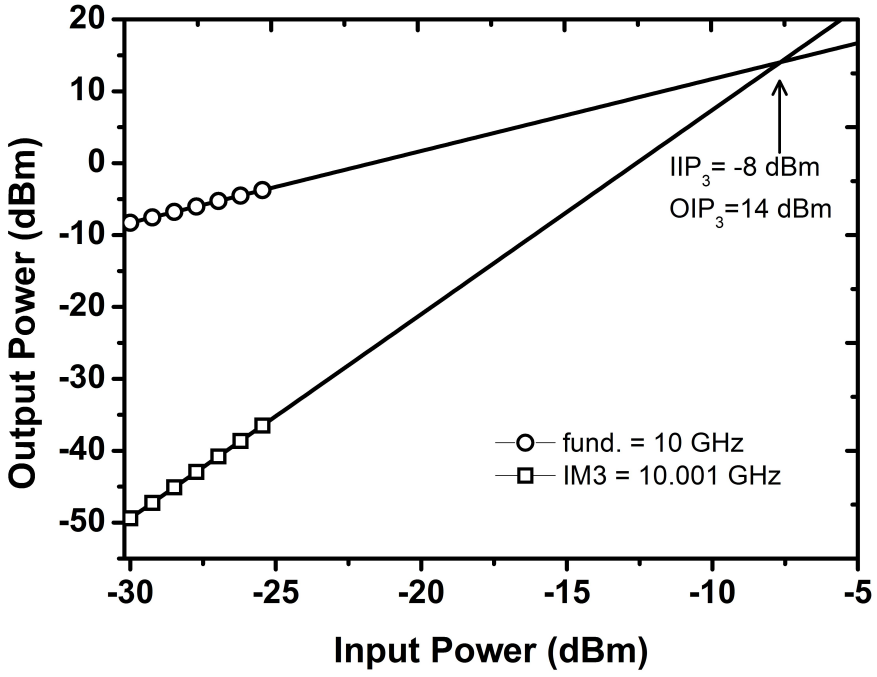

Figure 49: Measured input third-order intercept point.

at 10 GHz. The P_{1dB} is measured using Agilent E4418B power meter. The measured input and output P_{1dB} are -19.5 dBm and 1.5 dBm, respectively. Fig. 49 shows the measured third order intercept point (IIP_3). Input third-order intercept point, IIP_3, is -8 dBm and output third-order intercept point, OIP_3, is 14 dBm for a two-tone input at 10 and 10.001 GHz.

3.1.5 Performance Comparison

Table 5 shows the comparison of the presented LNA with other state-of-the-art X-Band LNAs, based on SiGe HBTs. In this table, a higher figure of merit (FOM) is better. In order to perform comparison between reported works, FOM reported in [10] augmented with bandwidth, an additional factor to be considered for defining the overall performance of LNAs.

$$FOM = \frac{(S_{21}[abs])^2.BW[GHz]}{(NF[abs]-1).P_{diss}[mW]} \tag{38}$$

The presented LNA achieves the highest FOM, despite of using HBTs with lower f_T (110 GHz) compared to other works. It also achieves the highest 3-dB bandwidth and its noise figure is competitive with the other state-of-the-art works.

Table 5: Comparison of state-of-the-art X-Band SiGe Low Noise Amplifiers

Reference	Frequency (GHz)	Gain (dB)	NF (dB)	$Bandwidth^*$ GHz	IIP_3 dBm	P_{diss} mW	FOM	SiGe HBT peak f_T GHz
This Work	10	22	1.65	6.5	-8	22	101	110
[10]	10	19.5	1.36	~ 5	0.8	15	80.8	200
[67]	10	25	1.7	4	-6.7	33.6	78.6	120
[68]	10	11	2.78	~ 3	-9.1	2.5	16.8	180
[69]	10	10	1.98	4.75	0	2	41	200

* 3 dB Bandwidth

3.2 An X-Band Switched LNA in 0.25-μm SiGe BiCMOS for Phased-Arrays

3.2.1 Introduction

As discussed in Section 1.6, in receive mode LNA is one of the main function blocks of the T/R module since it has a direct effect on the overall noise performance. It should provide a high gain and low noise figure to amplify weak signals, close to noise floor, captured by antenna while adding only a minimum amount of noise. On the other hand, at high level signals received by antenna, a high input referred third order intercept point (IIP_3) is required to achieve a high linearity. A high gain and a low noise figure is not the primary concern at high signal levels.

In recent years, the design of switched gain LNAs [70–74] and switched LNA [75–78] has become an active area of research. However, they are mainly reported for CDMA systems and do not address the requirement of X-Band phased arrays. The received signal level in a radar system may even increase up to 0 dBm if the target to be detected is close. Therefore, LNAs with wide dynamic range are indispensable to phased array radar systems for high capacity and high communication quality. For this purpose, the motivation in this work was to develop a wide dynamic range and high current efficient switched-LNA with two different modes for X-Band radar systems by using the high performance SiGe BiCMOS process.

In this section, the design, implementation and measurement results of a switched LNA is presented. The LNA is based on a single stage cascode topology and incorporates a series isolated NMOS transistor for switched function. Since RF CMOS switches and LNA design methodology is covered in detail in the previous sections, this section will briefly introduce the circuit without delving into the details. This X-band switched LNA aims at dynamic range improvement in phased array T/R modules in receive mode, in order to ease the system level specifications.

3.2.2 Circuit Design and Analysis

Fig. 50 presents the schematic of the proposed switched LNA. It is based on single stage, cascode topology (Q1 and Q2 HBTs) and series NMOS switch, M1. The operation of the circuit as follow: when V_C is low, bias circuit is ON and the

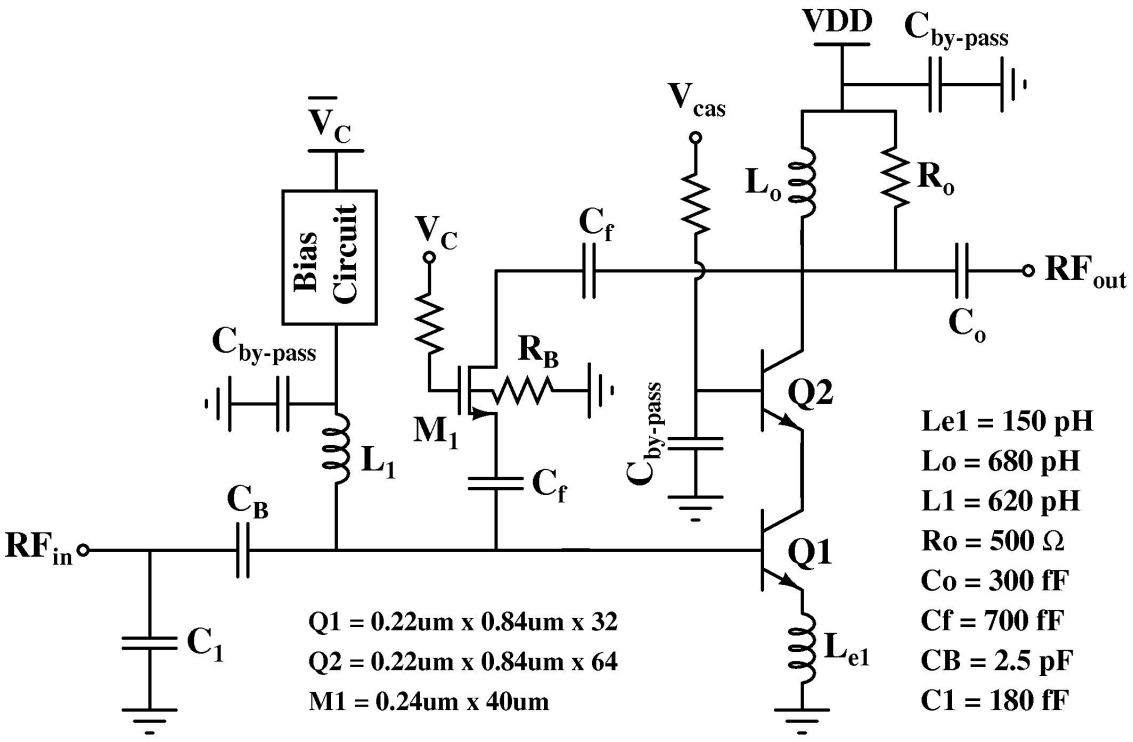

Figure 50: Circuit schematic of the switched gain LNA.

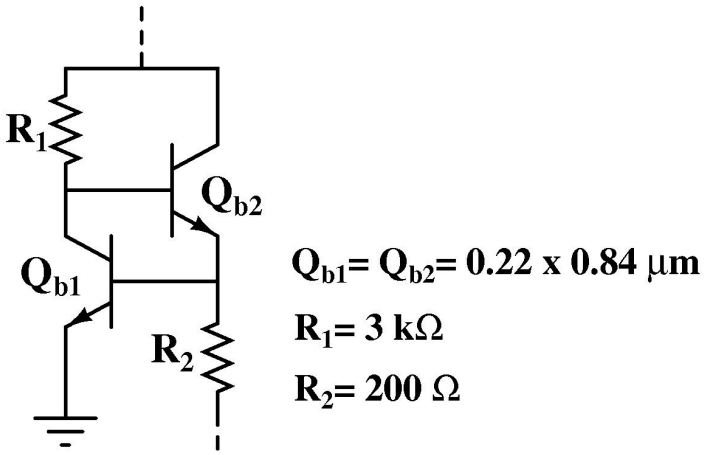

Figure 51: Bias circuit of the switched gain LNA.

circuit operates in the gain mode for amplifying weak signals whereas M1 transistor is OFF, operating in the cut-off region. On the other hand, when V_C is high M1 transistor is operating in the deep triode region, ON, while bias circuit is OFF and thus the circuit operates in the bypass mode or switch mode.

The circuit is designed by following the simultaneous noise and power matching procedure presented in the previous section. As the first step, an optimum base-emitter voltage which leads to an optimal current density is determined with the Q1

and Q2 transistors sized as unit devices. Then, the optimum source resistance is set to 50 Ω by scaling the length of Q1 and Q2 transistors. Finally, input impedance is matched to the source resistance of 50 Ω using L_{e1}, L_1 and C_1. Besides, in this configuration, the pad capacitance, which is around 30 fF, can be merged into the C_1 capacitance and reduce the potential of deviation in the measurements. C_B is the DC blocking capacitance and $C_{by-pass}$ capacitances are used to introduce ground close to the active core and filter out the additional noise coming from the supply and bias circuitry. Linearity of LNAs are strongly dependent on the biasing scheme and usually lower the impedance seen looking into the output of the bias circuitry, higher the linearity. Therefore, the bias current which has been supplied by an active circuit shown in Fig. 51 is fed to the base of Q1 transistor through an inductor L_1, in order to increase linearity of the LNA. The values of all the components are given in Fig. 50.

To implement switching functionality, a series NMOS switch is used between input and output terminals of the LNA. Similar to the RF CMOS switches presented in Chapter 2, the isolated NMOS transistor is used to implement resistive body floating technique to improve the power handling capability, IP_{1dB}, and the linearity, IIP_3, of the switched LNA in the by-pass or switch mode. The gate and body terminals of the M1 transistor are tied to control voltage and ground through 10 kΩ resistors, respectively. The challenge in the switched LNA design is to achieve good matching at the input and output ports for both mode of operations; LNA mode and switch or bypass mode. The C_f capacitors help to match the input/output terminals to 50 Ω for both gain and bypass modes. They also function as a DC blocking capacitances.

3.2.3 Measurement Results

The switched LNA was fabricated in IHP 0.25-μm SiGe BiCMOS process, using HBTs with an f_T/f_{max} of 110/180 GHz. The die photo of the switch is shown in Fig. 52. The chip area, excluding pads, is 0.52 μm x0.58 μm = 0.3 mm^2. Inductors in the switched LNA are custom designed in Sonnet using the thickest top metal layer in the process.

S-parameters of the switched LNA were measured using the 20 GHz Agilent

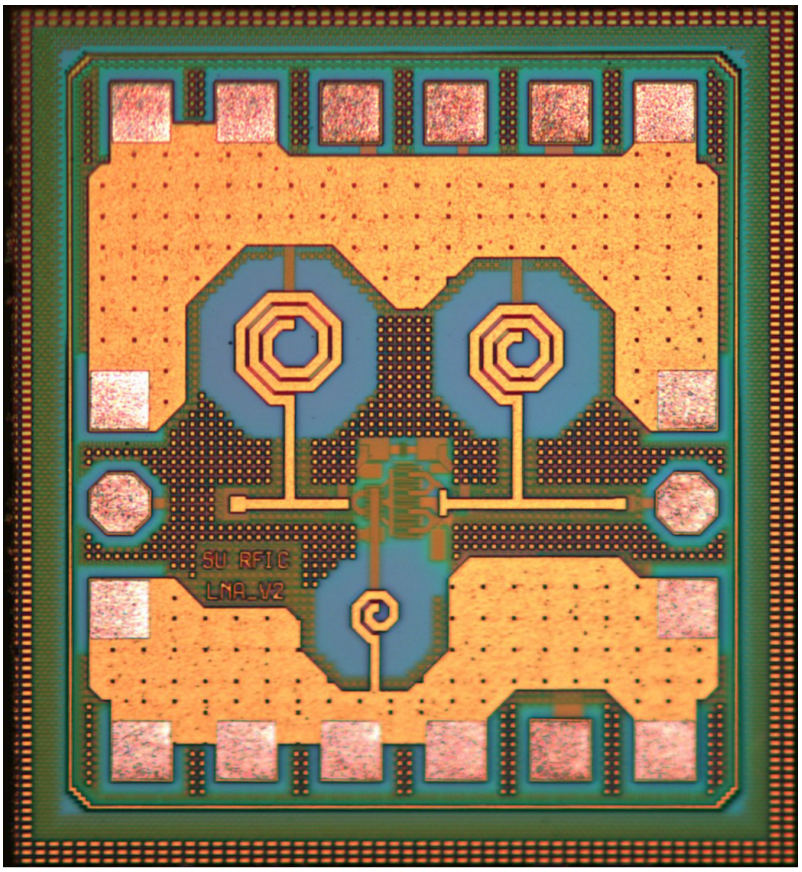

Figure 52: Die photo of the switched gain LNA. The active chip area, without pads, is 0.52x0.58 = 0.3 mm^2.

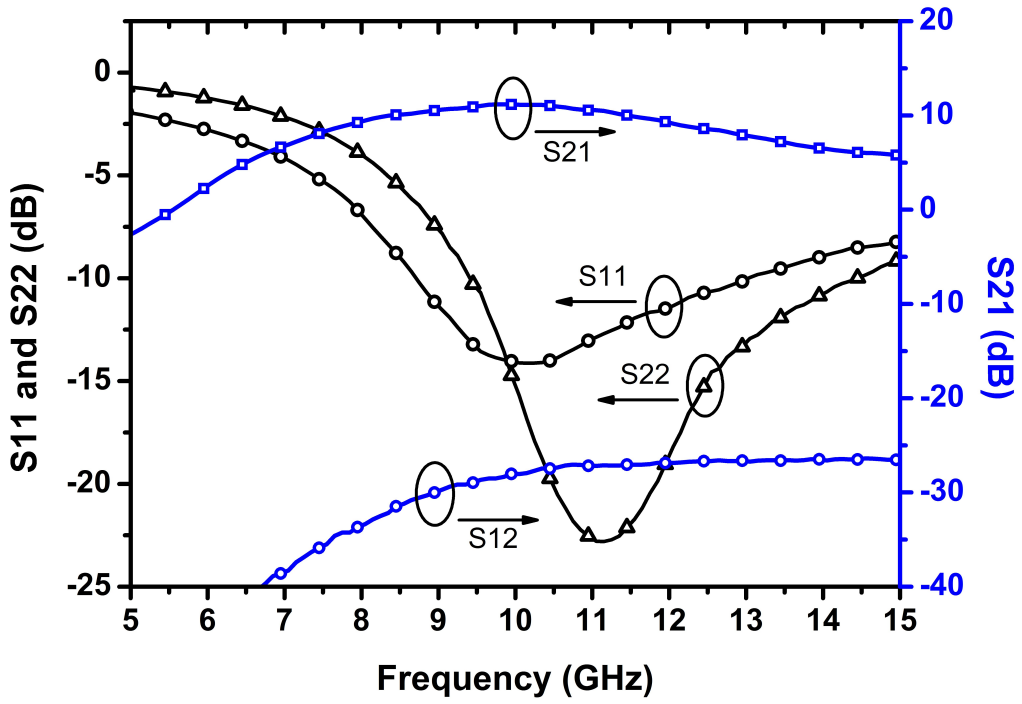

Figure 53: Measured S-parameters of the switched LNA in gain mode.

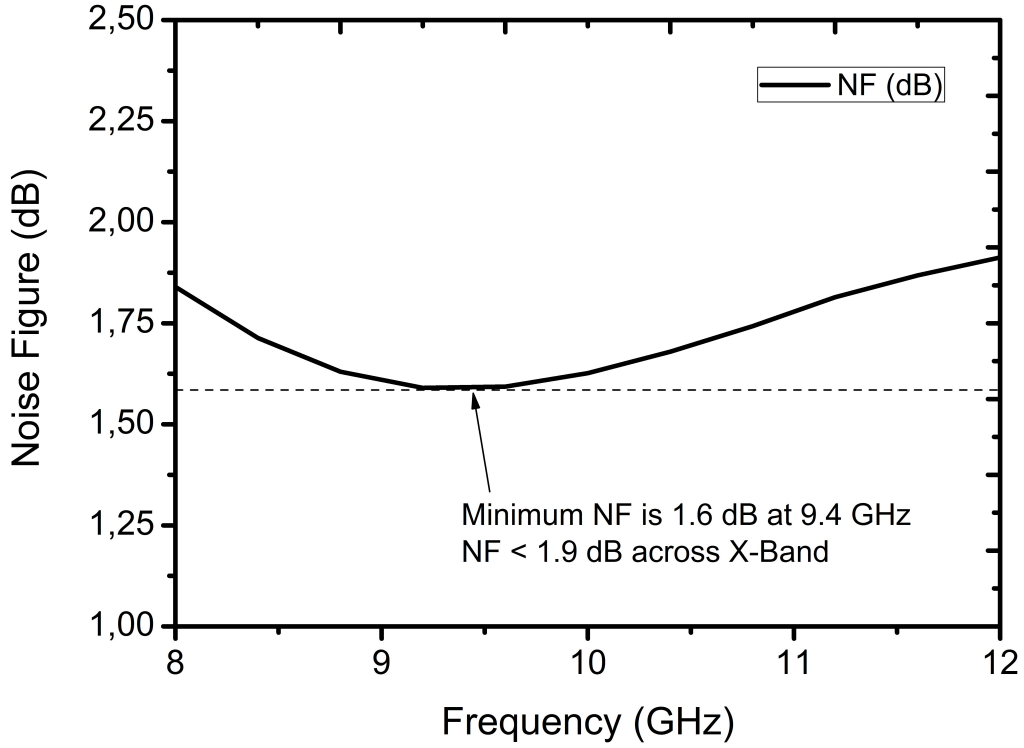

Figure 54: Measured noise figure of the switched LNA in gain mode.

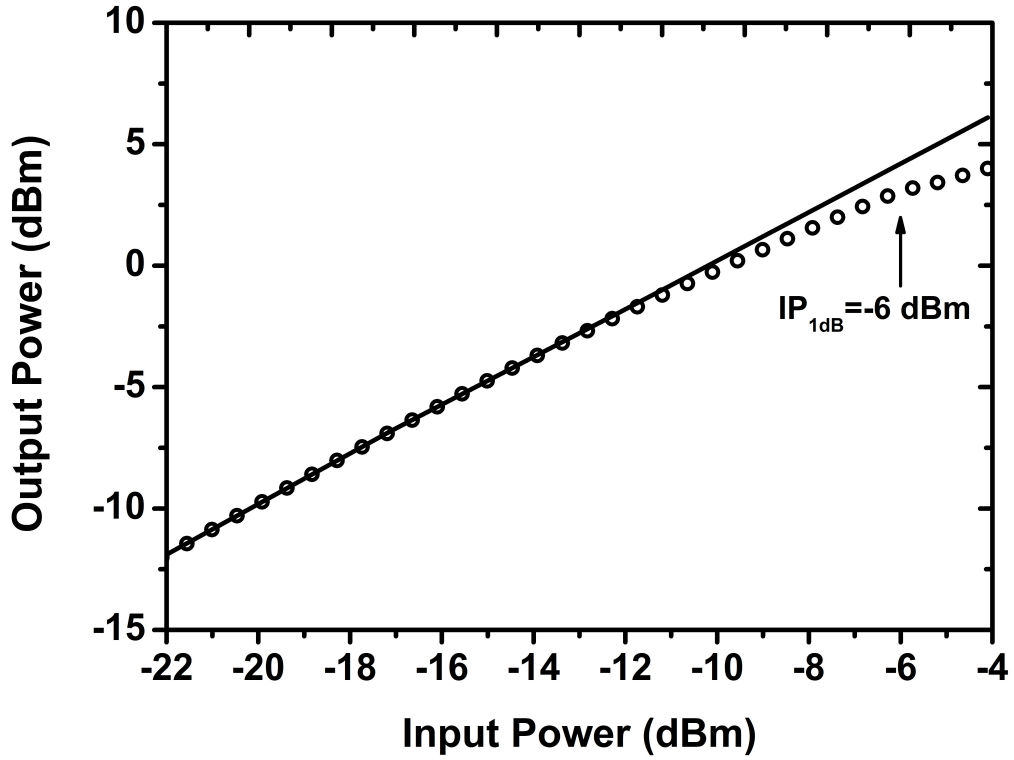

Figure 55: Measured P1dB of the switched LNA in gain mode.

8720ES network analyzer and probe station at room temperature. Fig. 53 shows the input and output return losses, gain and the reverse isolation of the switched

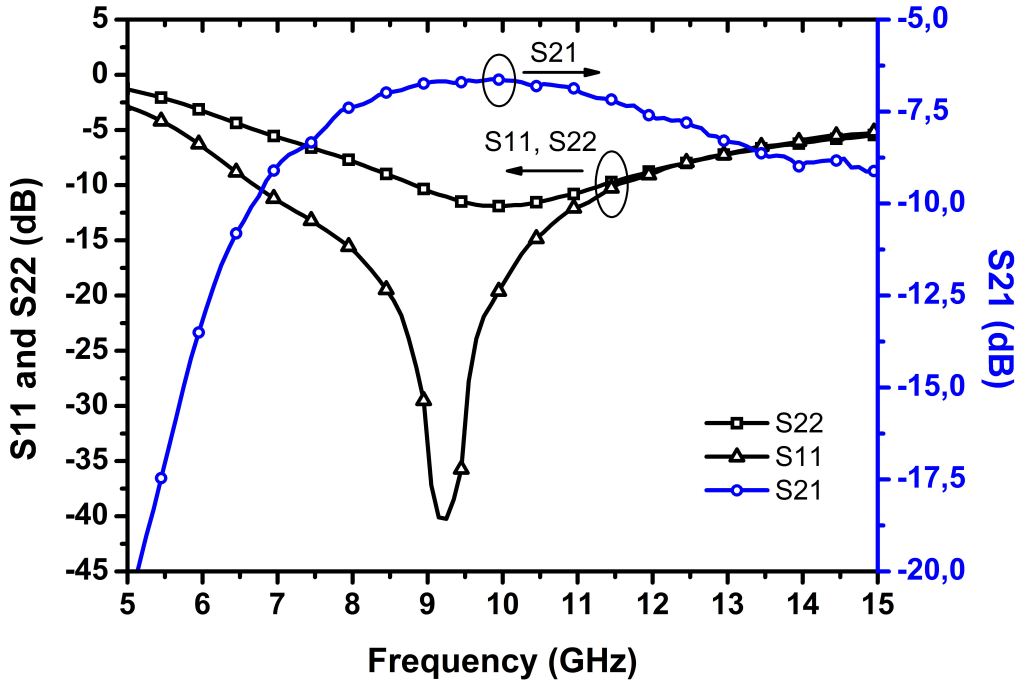

Figure 56: Measured S-parameters of the LNA in bypass mode.

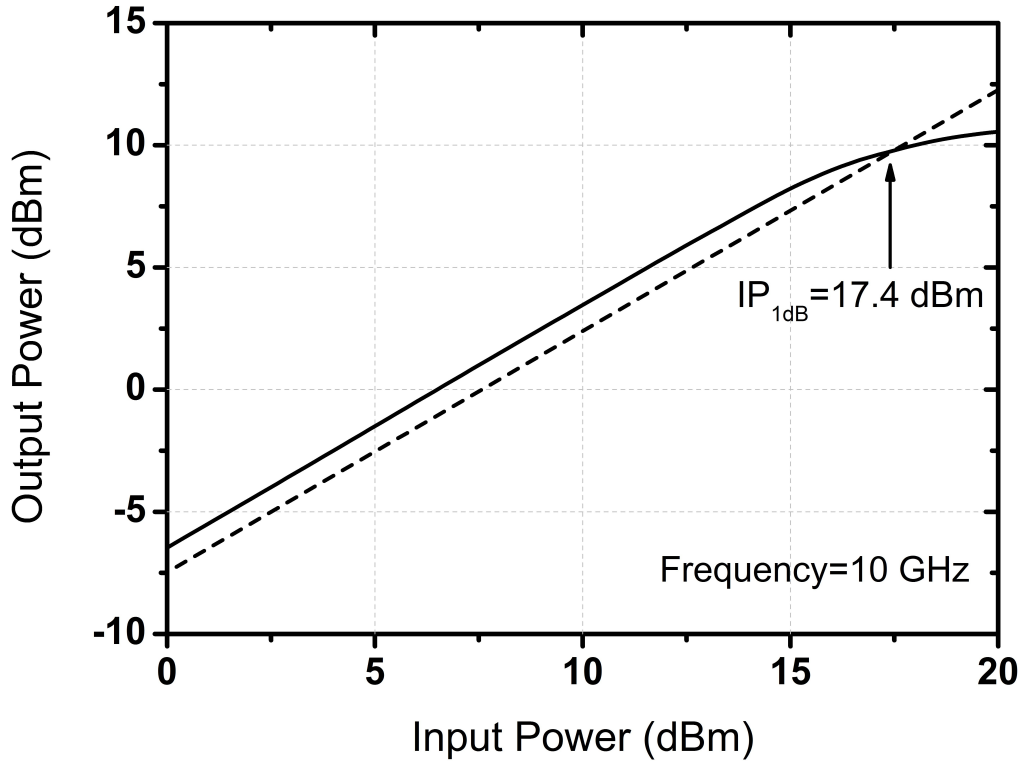

Figure 57: Measured P1dB of the LNA in bypass mode.

LNA in gain mode. In gain mode, switched LNA resulted in a gain of 9.5-11.5 dB accross X-band frequencies and a reverse isolation better than 26 dB. Input return loss is better than 10 dB in 8.5-13 GHz and output return loss is better than 10 dB in

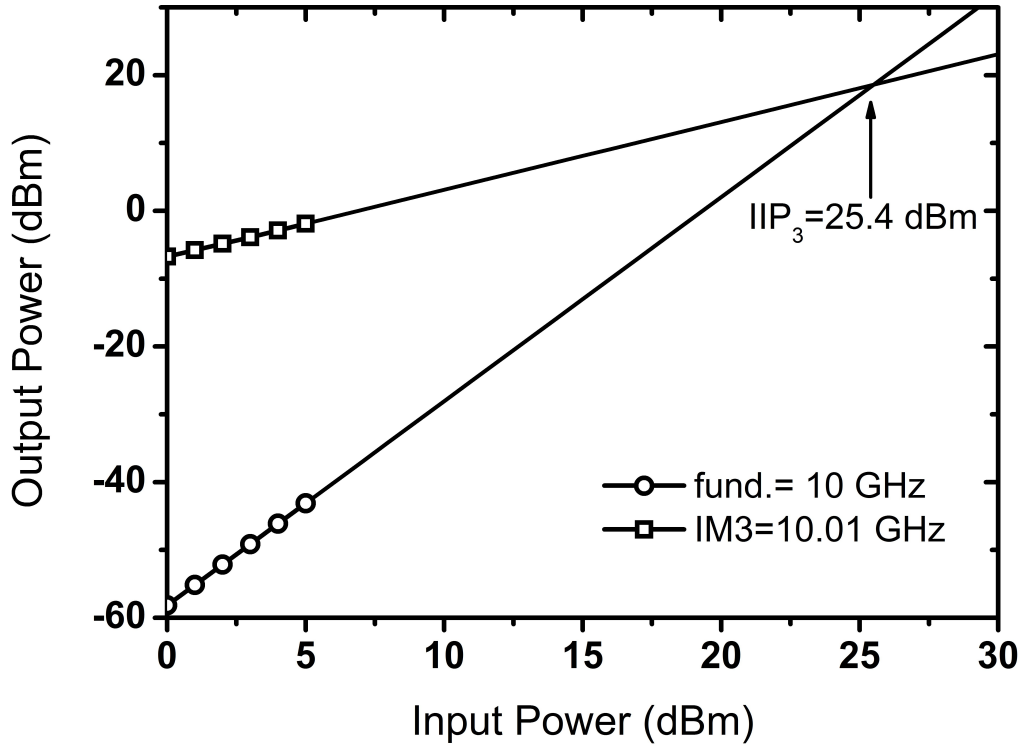

Figure 58: Input-referred third-order intercept point (IIP3) in bypass mode.

9-14 GHz. Fig. 54 shows the measured noise figure of the LNA across the X-Band frequency range. The LNA noise figure in gain mode is measured using E4407B spectrum analyzer with noise figure personality and Agilent 346A noise source. The cable and probe losses between output of the noise source and the LNA input were taken into account. Additionally, Agilent 87405C preamplifier was connected to the output of the LNA for measuring low noise signals. The measured noise figure in gain mode is better than 1.9 dB with minimum noise figure of 1.6 dB at 9.4 GHz.

The linearity of the switched LNA was evaluated by one-tone measurements. Fig. 55 shows the 1-dB compression point of the LNA for a single tone input at 10 GHz. The measured input P_{1dB} in gain mode is -6 dBm. The switched LNA draws 6.2 mA current from 3 V supply in gain mode and the total power consumption is 18.6 mW.

All measurements are also performed for the bypass mode. The measured S-parameters are shown in (Fig. 56). The switched LNA in bypass mode resulted in an insertion loss of 6-7.2 dB at X-band. The input return loss, S_{11} is better than 10 dB in 6.5-11.5 GHz and the output return loss is better than 8 dB in 8-12 GHz.

The linearity of the switched LNA in bypass mode was evaluated by one-tone and

two-tone measurements. Fig. 57 shows the 1-dB compression point of the switched LNA in bypass mode for a single tone input at 10 GHz. The measured input P_{1dB} in bypass mode is 17.4 dBm. Compared to the gain mode, there is a 21.4 dB increase in P_{1dB} in gain mode, correlating to a dynamic range improvement with the same amount. This improvement is mainly attributed the incorporation of resistive body floating technique into the switched LNA design, first time in the literature.

Fig. 58 shows the measured input third order intercept point in bypass mode. The IIP_3 measurement was performed using 9.99 and 10 GHz input signals, creating IMD component at 10.01 GHz. The switched LNA resulted in an IIP_3 point of 25.4 dBm in bypass mode. In bypass mode, the power consumption of the switched LNA is negligible (lower than 1 μW) and theoretically zero.

3.2.4 Performance Summary

These results display a clear improvement of dynamic range without extra power consumption, which can relieve system level specifications for X-Band phased-array radar systems. Therefore, this work is a successful demonstration of the integration and performance potential of SiGe BiCMOS process by combining high performance, low noise HBTs with isolated NMOS switches. To the best of author's knowledge, this is the first SiGe switched LNA reported at X-band. Furthermore, the resistive body floating technique is incorporated in switched LNA design, for the first time, to improve the linearity of the circuit in bypass mode.

4 An X-Band SiGe BiCMOS T/R Module for Phased Array Applications

4.1 Introduction

This chapter presents a full chip X-Band SiGe BiCMOS T/R module for phased array applications. The system block diagram of the SiGe T/R module is shown in Fig. 59. The module employs a single phase shifter for transmit and receive paths as discussed in the Chapter I. Thus, transmit and receive beams can be focused in the same direction with minimal calibration. The T/R module is implemented using the front-end circuits presented separately in the previous chapters. Different from the topology presented in Chapter I, which is the ultimate configuration aimed in the project, this module does not involve an on-chip T/R switch. At the time of integration, the T/R module based on slow-wave concept was not fabricated and using the T/R switch presented in Section 2.1 would degrade the noise figure performance of the T/R module in receive mode significantly due to its relatively high insertion loss. Therefore, it is assumed that the receiver input and transmitter

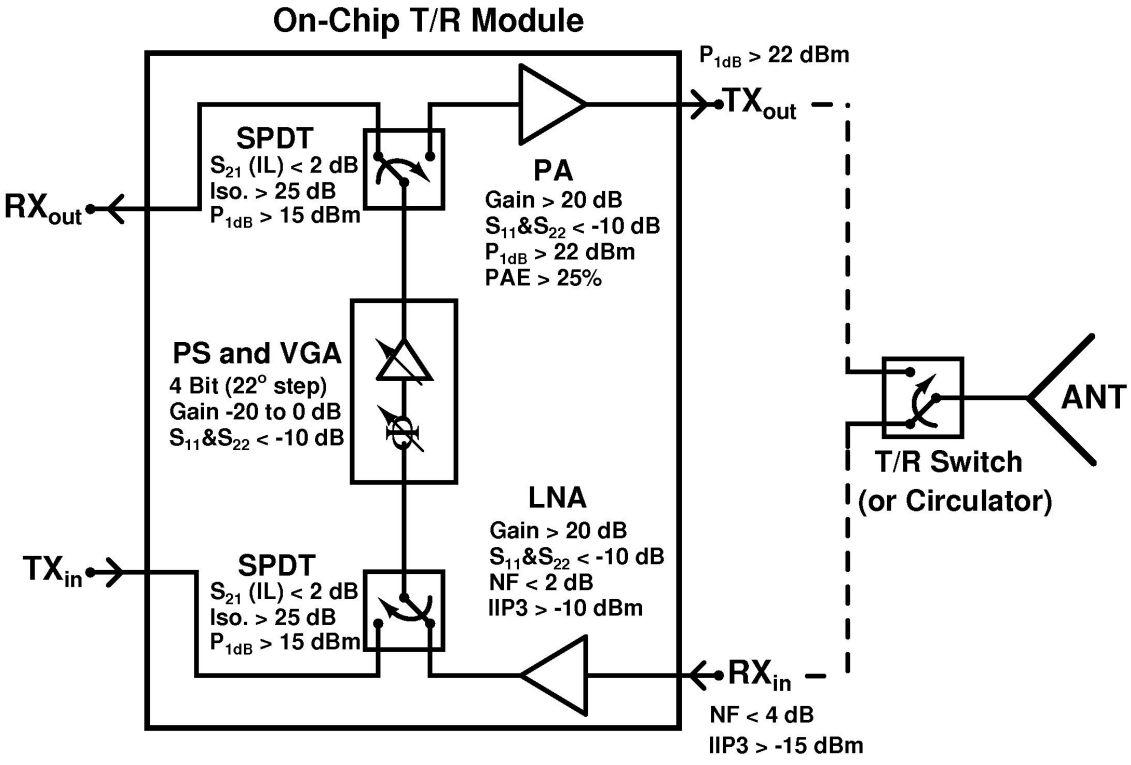

Figure 59: Block diagram of the X-Band SiGe BiCMOS T/R Module.

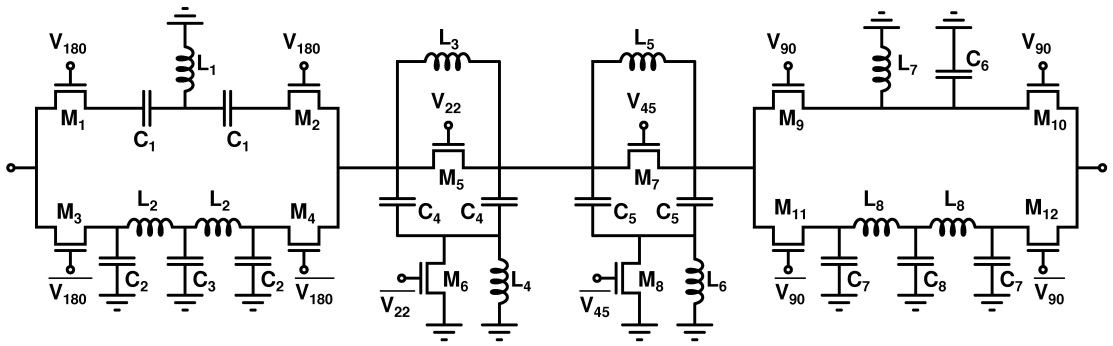

Figure 60: Layout of the X-Band T/R Module in IHP 0.25-μm SiGe BiCMOS process.

output of the T/R module would be connected to an off-chip MMIC T/R switch or circulator as envisioned in Fig. 59. Furthermore, this module allows for a dual chip T/R module by assembling III-V based high-power and ultra low noise amplifiers and T/R switch to address the stringent requirements in various applications such as air and missile defense systems.

In the receive mode, the T/R module achieves a simulated variable gain of 8-20 dB at X-Band with an avarage NF of 2-3.5 dB and a calculated IIP3 of -15 dBm. In the transmit mode, the simulated maximum gain and output P_{1dB} are 20 dB and 22.2 dBm respectively. Similar to the receive mode, the transmit gain can be controlled by the variable gain amplifier. The simulated RMS phase error are lower than 9°. The T/R module occupies 1.75 x 2.8 mm^2 and consumes 34 mW and 485 mW in the receive and transmit modes, respectively.

4.2 Design and Implementation

The individual building blocks are connected together using 50-Ω microstrip transmission lines to impelement the T/R module. The LNA, PA and VGA are designed using 0.25 μm SiGe HBTs available in IHP 25SGH3 process, while phase shifter and SPDT switches are implemented using the 0.24-μm isolated NMOS transistors offered in the technology. The PA (presented in Section 1.6.2) is a linear two-stage cascode topology with active bias networks to improve the linearity and results in 25.5 dB peak small signal gain, an output P_{1dB} of 22.2 dBm and a peak PAE of 28 % at X-Band and occupies 0.6 mm^2 chip area. The SPDT switches are presented in Section 2.2 and achieve a measured IL of 1.8-2.2 dB, isolation higher

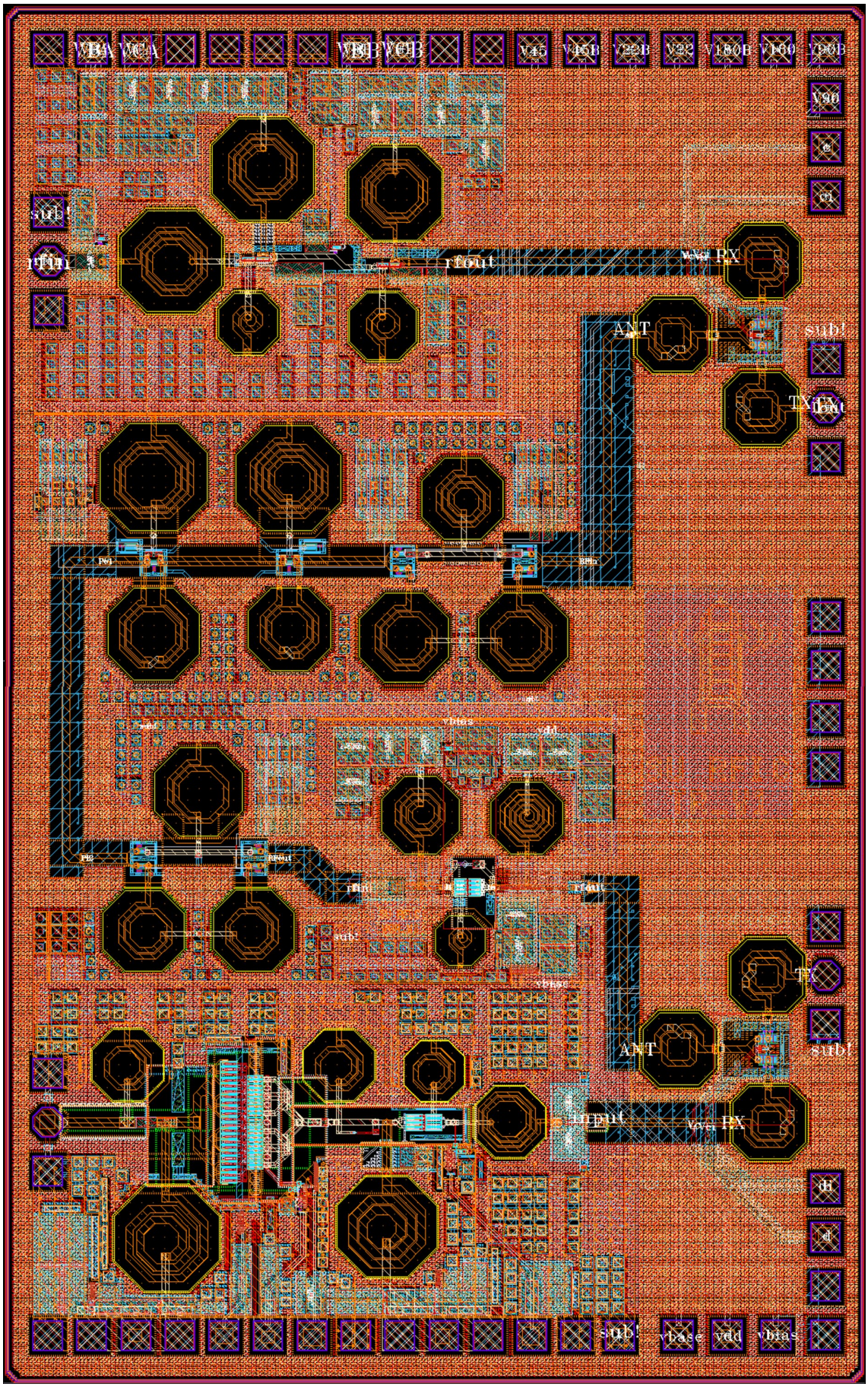

Figure 61: Layout of the X-Band T/R Module in IHP 0.25-μm SiGe BiCMOS process.

than 23 dB at X-band with an input P_{1dB} of 17 dBm at 10 GHz. The two-stage high performance cascode LNA is presented in Section 3.1 and results in a measured gain of 19-22 dB, measured average noise figure of 1.65 dB at X-Band with 22 mW power consumption and a IIP_3 of -8 dBm.

A four bits phase shifter with 22.5° phase resolution was designed using NMOS transistors and released for fabrication. The circuit diagram of the each bit is shown in Fig. 60. The input and output of each bit is matched to 50 Ω and then the bits are placed in series so as to minimize insertion loss. The 90° and 180° bits of the phase shifter switch between high pass and low pass delay states. The 22.5° and 45° bits switch between a low-pass phase delay state and bypass state. The phase shifter results in a simulated RMS phase error of 1°-3.5° and RMS gain error of 0.8-1.8 dB at X-Band. The simulated average insertion loss of the phase shifter (not shown) is 12±2 dB at 10 GHz and it occupies 0.9 mm^2 chip area.

The VGA is based on variable transconductance topology and it is simply implemented by replacing the NMOS transistor of the switched LNA presented in Section 3.2 by a feedback resistor and by using bias for gain control. It results in a simulated peak gain of 12 dB with 10 mW power consumption from 2.5 V supply with a IIP_3 of 6 dBm.

4.3 Simulation Results

The layout of the T/R module is shown in Fig. 61. The chip area, including pads, is only 4.9 mm^2. The components are connected to each other by microstrip transmission lines to reduce the coupling to the substrate. The connecting microstrip transmission lines are implemented using top metal layer (3 μm thick and 15 μm wide) for signal flow and first metal layer, M1, as ground. The simulated transmission lines in Sonnet shows a 0.25 dB/mm loss and a characteristic impedance of 51-Ω.

The T/R module is simulated in Cadence SpectreRF. Fig. 62 shows the simulated gain of the T/R module in the receive mode. The module results in a small-signal gain of 18±2 at 8.5-12 GHz without VGA compensation. Fig. 63 and Fig. 64 shows the simulated input and output return losses of the T/R module in the receive mode, respectively. It is seen that input and output are perfectly matched

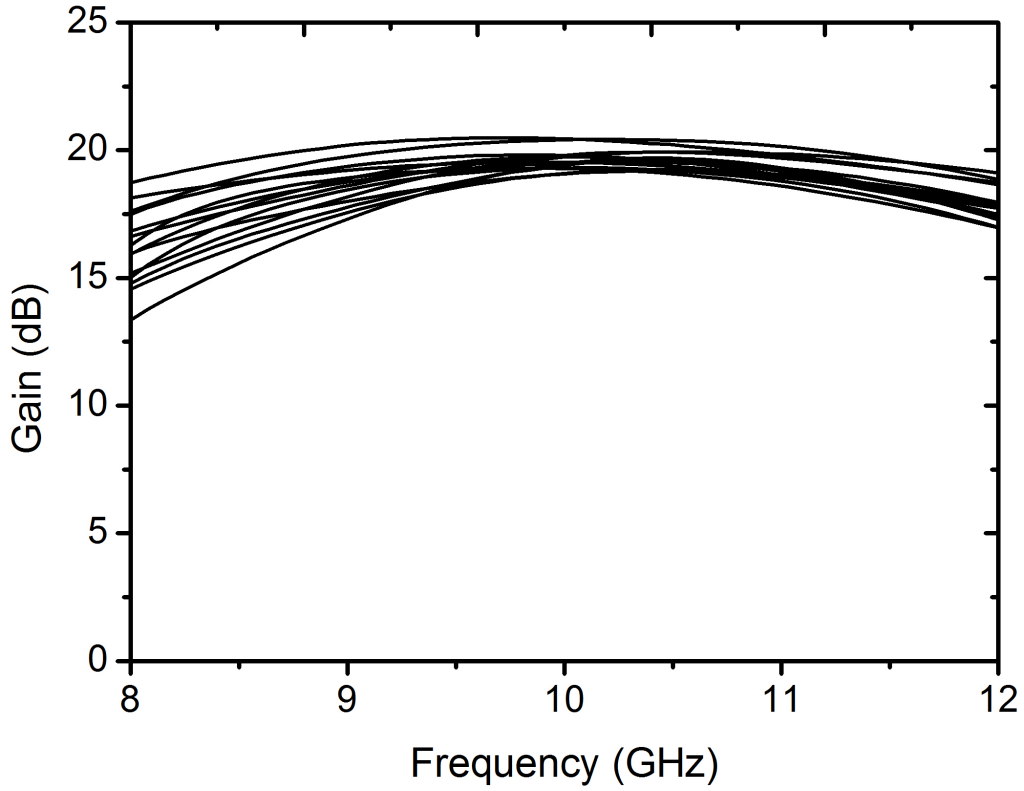

Figure 62: Measured gain of the T/R module in the receive mode for all phase states.

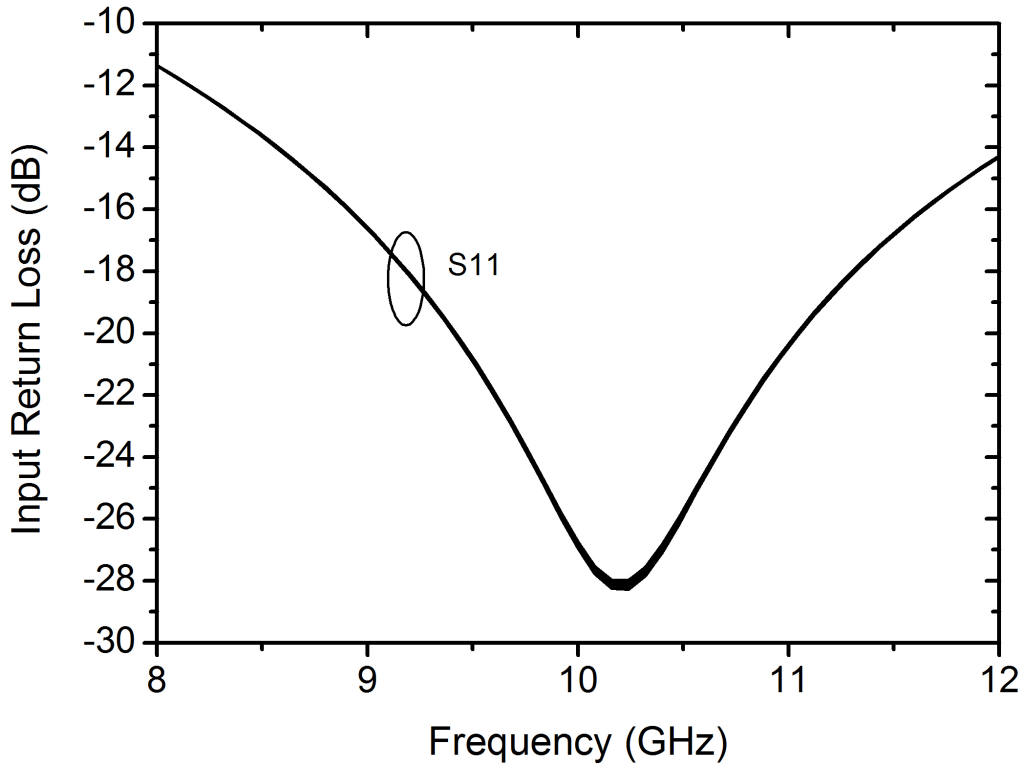

Figure 63: Simulated input return losses of the T/R module in the receive mode for all phase states.

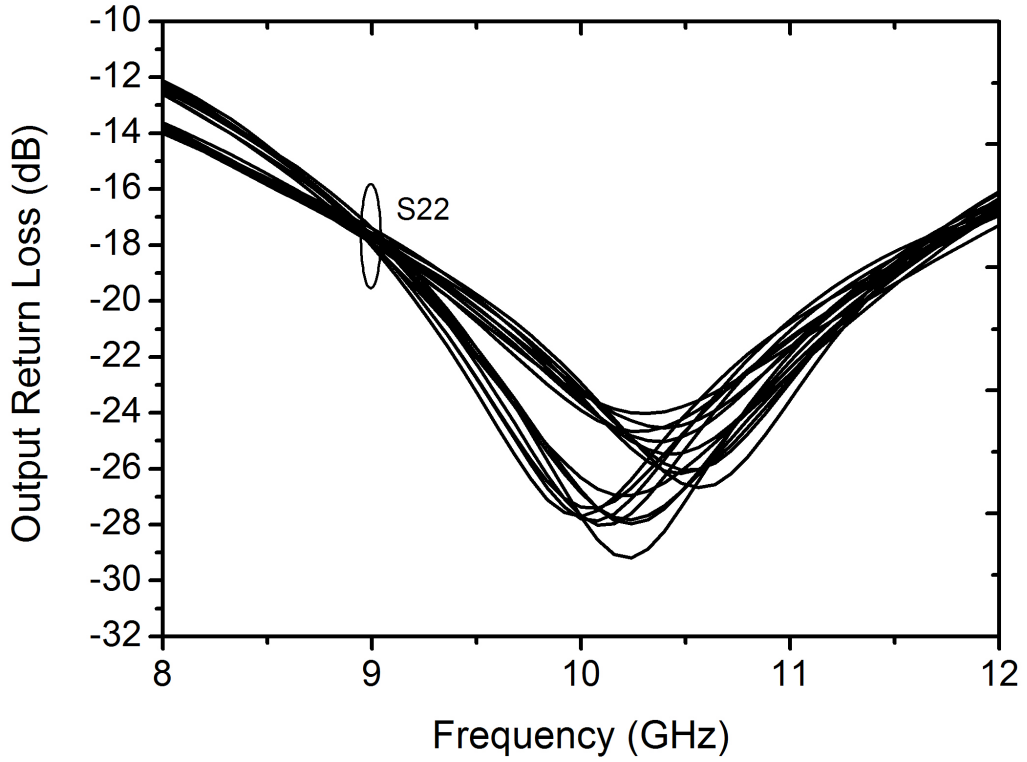

Figure 64: Simulated output return loss of the T/R module in the receive mode for all phase states.

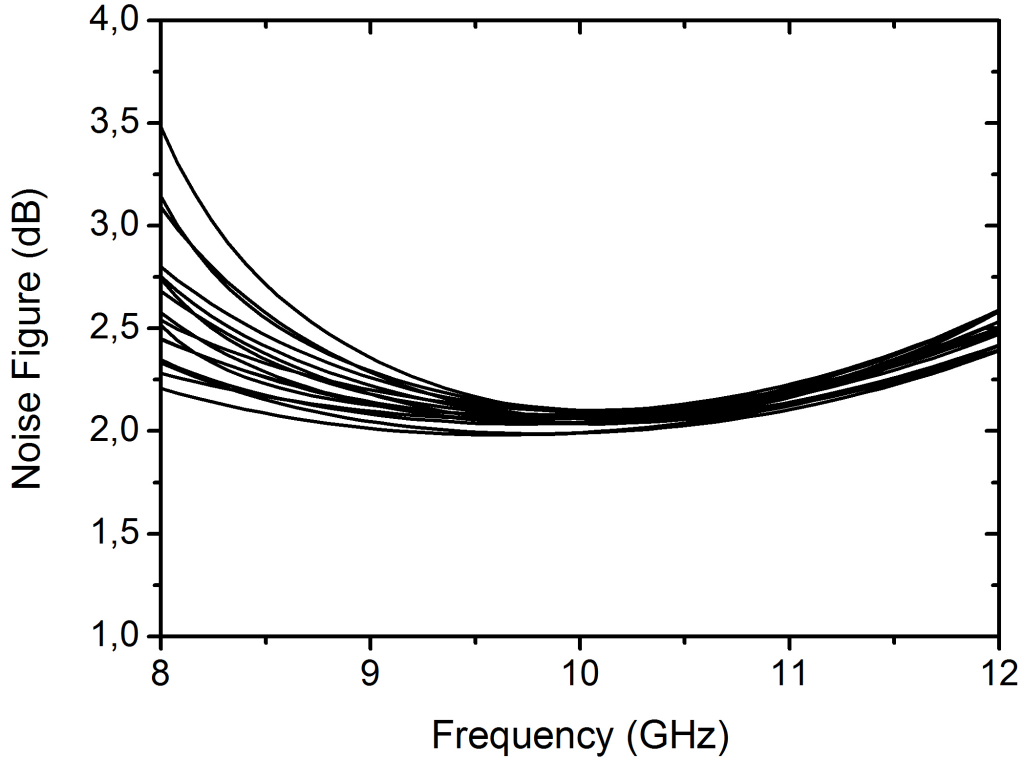

Figure 65: Simulated noise figure of the T/R module in the receive mode for all phase states.

and return loss at both ports are better than 11 dB for all phase states. The input return loss of the T/R module is dominated by the LNA and output return loss is dominated by SPDT switch.

The noise figure of the complete T/R module is 2-3.5 dB at 8-12 GHz for all phase states (Fig. 65) and it shows an average NF of 2.5 dB at X-Band. The phase response of the T/R module in the receive mode is also simulated. Fig. 66 and Fig. 67 shows the simulated 4-bit phase response and RMS phase error of the T/R module, respectively, in the receive mode. The T/R module provides a desired phase shift between 0° and 360° with 16 states. The insertion phase for 16 states relatively parallel to each other. The simulated RMS phase error is 3°-8.6° over all of X-Band and it is lower than 5.5° from 8.5 GHz to 12 GHz. It is clear from Fig. 66 that the high phase error at 8-8.5 GHz arises mainly from the 90° phase shifting block. Additionally, the received gain can also be controlled by 10 dB at the expense of 1 dB increase in the NF (Fig. 68). The power consumption in the receive mode is only 13.6 mA from 2.5 V supply (34 mW).

Fig. 69 presents the simulated gain of the T/R module in the transmit mode. The gain changes between 16 dB and 20 dB over all of X-Band and it demonstrates a

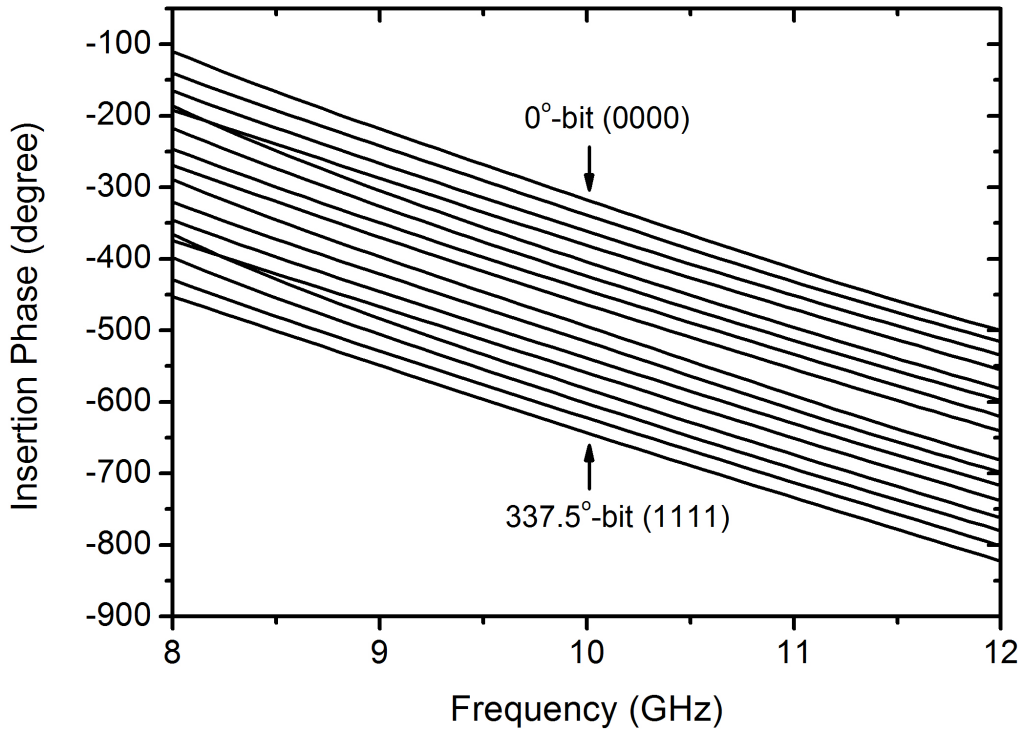

Figure 66: Simulated 4-bit phase response of the T/R module in the receive mode.

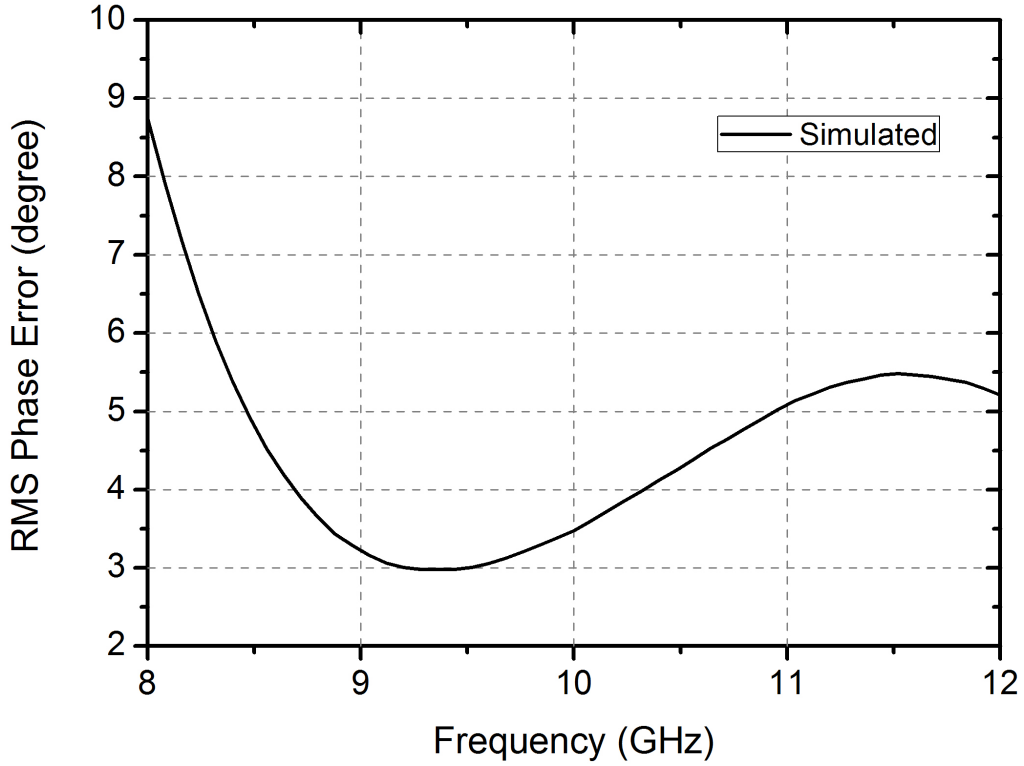

Figure 67: Simulated RMS phase error of the T/R module in the receive mode.

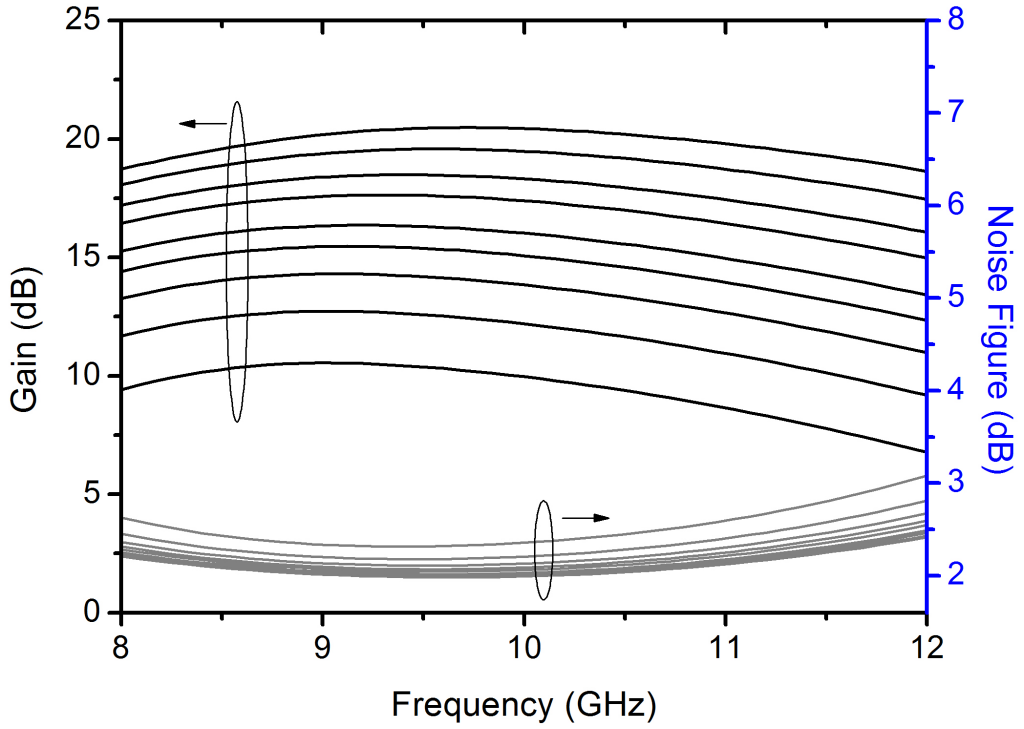

Figure 68: Simulated variation of the gain and noise figure of the T/R module in receive mode.

peak gain of between 18 dB to 20 dB at 11 GHz for 16 different phase states without VGA equalization. The gain of the module in transmit mode is dominated by PA

which produces two peaks at X-Band to achieve a flat gain. The T/R module also results in good input return loss performance for all phase states (Fig. 70). Similar to the receive mode, transmit gain can be controlled over a 10 dB range using the VGA. The output return loss of the T/R module is dominated by the PA and it is better than 10 dB only between 9.8 GHz and 11.2 GHz since the output of PA is primarily matched for delivering maximum power rather than maximum power transfer.

The expected output P_{1dB} is 22.2 dBm (measured on a stand-alone PA) unless a premature saturation of the VGA output occurs. This could not be demonstrated by the simulations due to inexplicable crushing of the PSS simulations probably due to the complexity of the system. Fig. 71 presents the 4-bit phase response and RMS phase error of the T/R module in the transmit mode. They are almost identical with those in the receive mode as expected from the utilization of a single phase shifter for the receive and transmit paths. The isolation between RXin and RXout in the receive mode is higher than 88 dB while the isolation between TXin and TXout is better than 79 dB (Fig. 72).

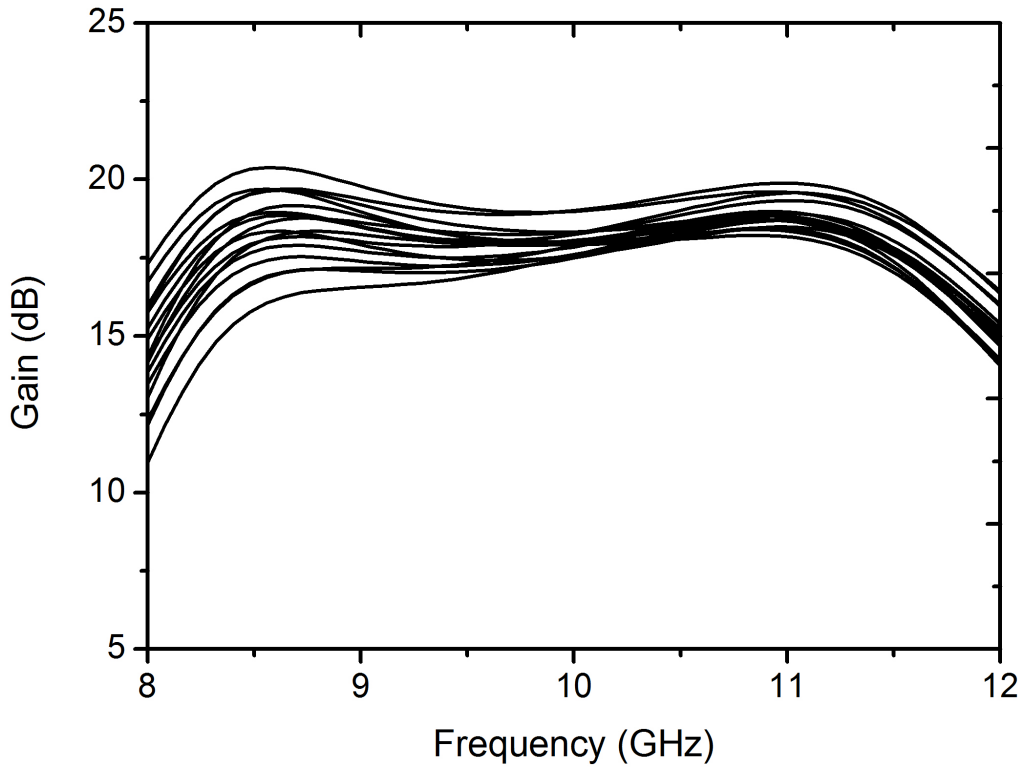

Figure 69: Simulated gain of the T/R module in the transmit mode for all phase states.

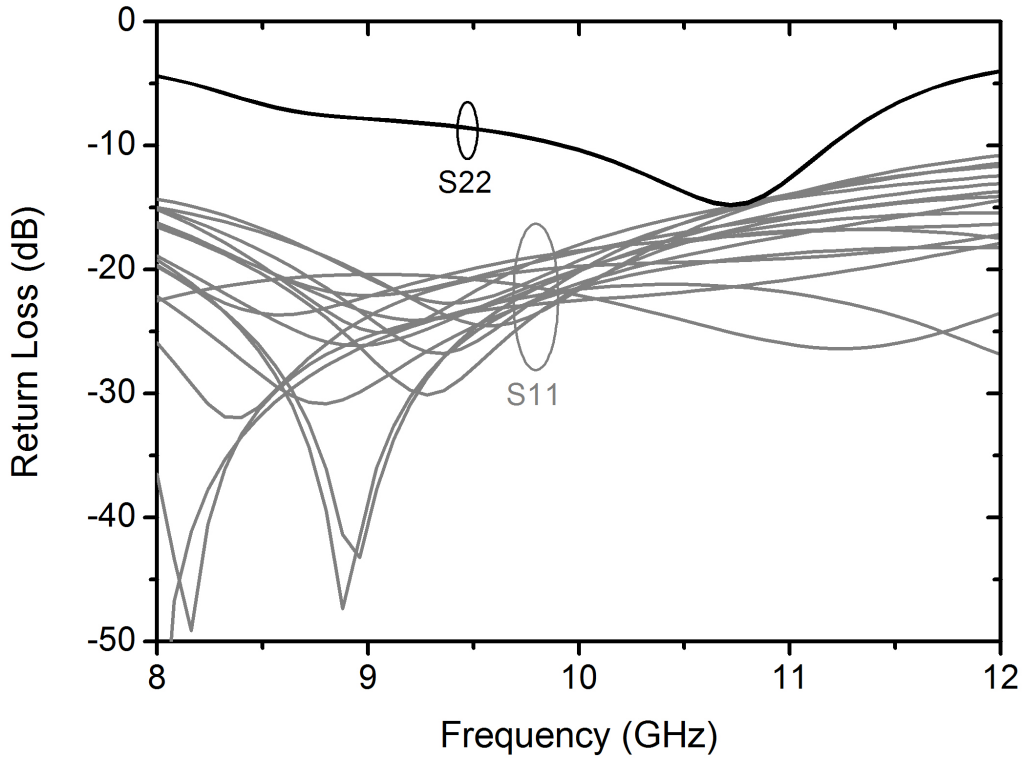

Figure 70: Simulated input and output return losses of the T/R module in the transmit mode for all phase states.

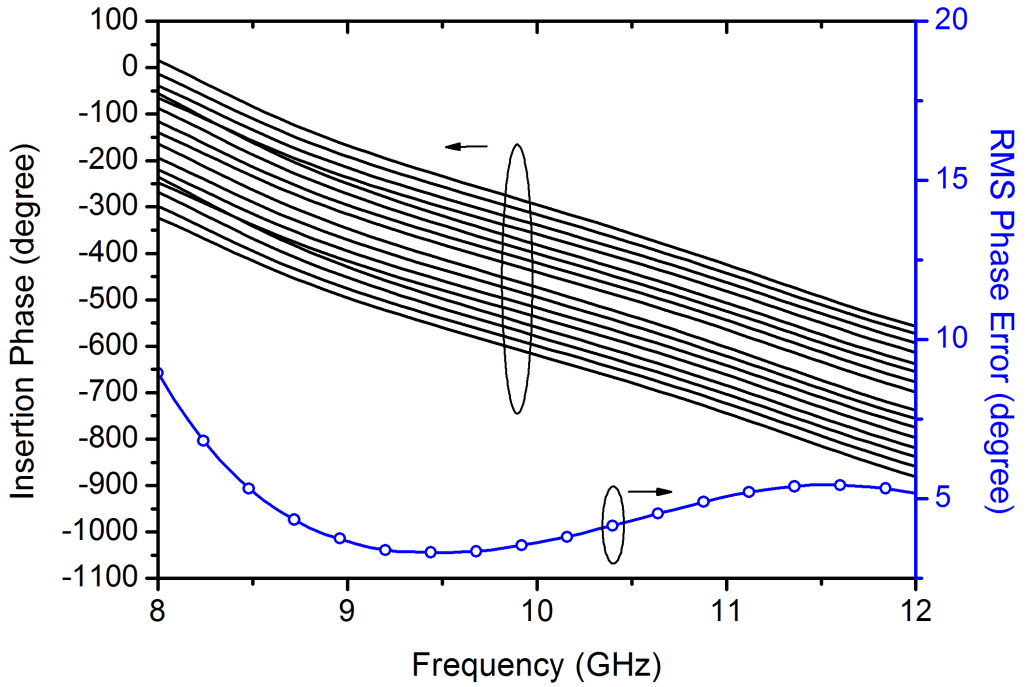

Figure 71: Simulated 4-bit phase response and RMS phase error of the T/R module in the transmit mode.

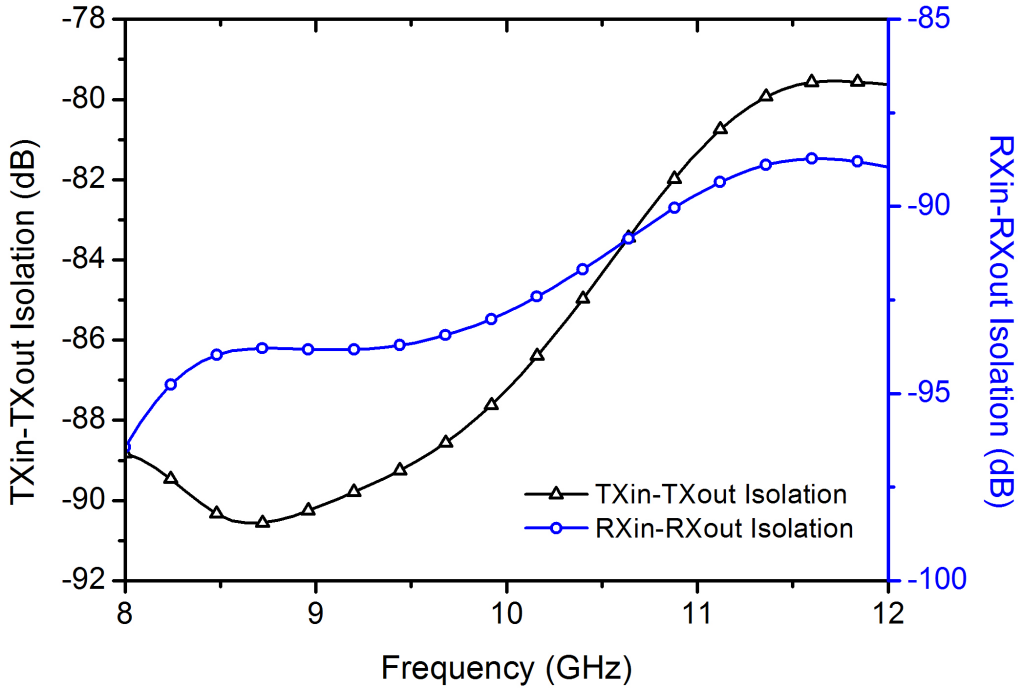

Figure 72: Simulated isolation of the transmit and receive modes.

4.4 Performance Comparison

This chapter presented a state-of-the-art X-Band SiGe BiCMOS T/R Module capable of excellent gain, phase control and NF. The performance of the T/R module was compared to the previously published state-of-the-art works, as shown in Table 6. To the best of our knowledge it achieves the highes P_{1dB}, lowest NF and competitive gain performance and power dissipation in smallest chip area. The RF performance of the module is even better/comparable to the GaAs chips.

Table 6: Comparison of the state-of-the-art X-Band T/R Modules

Frequency (GHz)	TX/RX Gain (dB)	NF (dB)	P_{1dB} (dBm)	PS Bit	$P_{diss}(mW)$	Chip Size (mm^2)	Process	Reference
8-12	20/20	2.5	22.2	4	519	4.9	BiCMOS	This Work*
8-10.7	11/11	4.1	NR	5	30	13.3	BiCMOS	[24]
8-11	30/20	9	18	5	1500	8.4	BiCMOS	[79]
8-11	15/15	10	12	5	800	16	BiCMOS	[80]
8-11	27/27	2.5	19	6	1200	20	GaAs	[81]

* Simulated Results

5 Conclusion & Future Work

5.1 Summary of Work

Modern phased array radars contain thousands of antenna elements, T/R modules, to change the direction of the overall antenna to achieve fast beam scanning. The performance of the T/R modules mainly drives the performance of the phased arrays. As a result of recent advances in Si-based IC technologies, next generation X-band Phased Array Radar systems aim to use low-cost, fully integrated transmit/receive (T/R) modules in order to decrease deployment and operational expenses. This thesis presented front-end integrated circuits for a state-of-the-art X-Band T/R module in a commercial 0.25 μm SiGe BiCMOS process. These circuit blocks include a highly linear CMOS T/R switch, a DC-20 GHz SPDT switch (primarily optimized for operation at X-band), a T/R switch based on slow-wave transmission lines, a high performance SiGe HBT LNA and a switched LNA.

The highly linear T/R switch was based on series-shunt topology with combination of the different design techniques such as parallel resonance technique to improve isolation, DC biasing the input and output ports, using on-chip impedance transformation networks (ITN) and resistive body-floating to improve P_{1dB} and finally scaling of transistor sizes for lower insertion loss of the switch. It exhibited an IL of 3.6 dB, isolation of 34.8 dB and input P_{1dB} of 28.2 dBm at 10 GHz. To the authors' best knowledge, this single-ended CMOS T/R switch shows the highest P_{1dB} with competitive isolation and comparable IL at X-Band.

The SPDT switch was basically based on series-shunt topology. On-chip impedance transformation networks (ITN) and resistive body-floating were used to improve P_{1dB} and transistor sizes were scaled for lower insertion loss and higher isolation of the switch. It resulted in a measured insertion loss less than 3.1 dB, isolation higher than 21 dB and P_{1dB} better than 16 dBm from DC to 20 GHz. This is a successful demonstration of the fully integration of ultra-broadband SPDT switches in SiGe BiCMOS process.

The slow-wave T/R switch was based on shunt-shunt configuration to improve isolation. The slow-wave concept was employed for reducing the chip area and making the T/R switch less vulnerable to modeling issues in the design kit. The

switch resulted in a measured insertion loss of 2.3 dB, isolation of 39 dB and a simulated input P_{1dB} of 27.6 dBm at 10 GHz. This is the first T/R switch employing slow-wave concept in any BiCMOS technology to the date.

The LNA was composed of two stages and each stage is cascode topology using 0.25-μm SiGe HBTs with peak f_T of 110 GHz. The first stage was designed for low noise performance while the second stage was optimized to improve the IIP_3. The LNA achieved a gain higher than 19 dB and a mean noise figure of 1.65 dB at X-Band with an IIP_3 of -8 dBm at 10 GHz. The LNA resulted in the highest FOM, despite of using HBTs with lower f_T (110 GHz) compared to other works.

The switched LNA was based on a single stage cascode topology and incorporated an isolated NMOS transistor for performing switching function. The switched LNA was biased through a shunt inductor to improve linearity in the gain mode. Also, resistive body floating technique was implemented, for the first time in a switched LNA, to further improve linearity in bypass mode. In gain mode, LNA achieved 9.5-11.5 dB gain, 1.6-1.9 dB noise figure, -6 dBm input P_{1dB}, with 16 mW power consumption. In bypass mode, insertion loss is 6-7.5 dB and P_{1dB} is 17.4 dBm.

Finally an X-Band T/R module was implemented in SiGe BiCMOS process by using the individually designed front-end circuits. The T/R modules resulted in an excellent performance and it is attributed to the unique design methodologies and techniques followed during the design of individual building blocks.

5.2 Future Work

There are currently some problems regarding the design of the phase shifter arising from the modeling issues of the NMOS transistors in the design kit. The phase shifter integrated in the T/R module was fabricated and measured as stand-alone but there were significant discrepancy between the simulation and measurement results. Therefore, the releasing of the T/R module for fabrication is postponed until the phase shifter's performance is verified. Presently, two alternatives are explored to resolve this issue. First approach is to fabricate each bit of the phase shifter separately and then updating the schematic design according to the measurements. The other alternative is to design an active phase shifter by using HBTs whose models are more reliable than those of NMOS. However, the second option is not favorable

since the IIP_3 of the active phase shifters is relatively lower than the passive ones and thus the utilization of the would degrade the overall linearity of the T/R module in the receive mode. Once the phase shifter is optimized, its final layout will be replaced with the current one and then the T/R module presented in Chapter 4 will be released for the fabrication. Optionally, the T/R switch based upon slow-wave transmission lines may be integrated into the full chip before releasing fabrication.

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PUBLICATIONS

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Dinc T., Zihir S., Tasdemir F., and Gurbuz Y., A Fully Integrated, Highly Linear CMOS T/R Switch for X-Band Radar Systems, Wiley International Journal of Circuit Theory and Applications, 2012 (accepted).

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Dinc T., and Gurbuz Y., An X-Band T/R Switch based upon Slow-wave Transmission Lines in 0.25-μm SiGe BiCMOS, IEEE Microwave and Wireless Components Letters, 2012 (in progress).

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Conferences:

Dinc T., Zihir S., and Gurbuz Y., SiGe Building Blocks for On-Chip X-Band T/R Modules, IEEE Radio Wireless Week (SiRF), Santa Clara, U.S., 2012.

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Awards And Scholarships

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Full Graduate Scholarship of Sabanci University Sep. 2010 - Present
- Covering full tuition and dormitory fee exemption.

SU Haci Sabanci Scholarship 2007 – 2010
- Covering tuition, dormitory fee, book support and stipend payment. (based on GPA at the end of freshman)

SU Honor Scholarship 2005 – 2007
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Work Experience

Sabanci University, RFIC Research Team **Sep. 2010 - Present**
Graduate Research Assistant
- Design of high power, high isolation and wideband RF switches in CMOS
- Design of high performance LNAs and Switched LNA in SiGe BiCMOS
- Measurement of RF front-end ICs (LNAs, PAs, Switches)

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- RF Modelling of BiCMOS BEOL (Back-end-of-line) Embedded Capacitive RF-MEMS Switches for mm-wave Applications(60-140 GHz) by using Sonnet EM Simulator.

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Teaching Experience

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Selected Course Projects

Selected Topics in Microelectronics:RFIC
- Design of an X-Band cascode LNA using 0.25-um SiGe BiCMOS HBT Technology, supervised by Prof. Yasar Gurbuz

Introduction to RF and Microwave Circuit Design
- RF Amplifier Implementation at 1GHz, supervised by Assoc Prof. Meric Ozcan

Microwaves
- Design and PCB Implementation of a Wireless Repeater at 2.4 GHz, supervised by Assoc. Prof. Ibrahim Tekin

Introduction to MEMS
- Design of a RF MEMS Capacitive Switch at X-Band by using Coventorware and Fabrication in Sabanci Class 1000 Clean Room, supervised by Prof. Yasar Gurbuz

Digital Integrated Circuits
- Full Custom Design of a Standard Cell Library using AMS 0.35um CMOS Technology in Cadence Environment, supervised by Assoc. Prof. Ayhan Bozkurt

Technical Skills	**CAD Tools:** High frequency circuit/system level and EM simulations in Cadence, ADS - Momentum, Sonnet, HFSS, CoventorWare.
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Transcript, References	Available upon request.