HIGH DYNAMIC RANGE PIXEL ARCHITECTURE WITH SMART LIGHT INTENSITY DECISION UNIT

by

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High Dynamic Range Pixel Architecture with Smart Light Intensity Decision Unit

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Keywords: ROIC, SWIR, Smart, Unit Cell, SNR, HDR, Infrared, FPA.

Abstract

In this thesis, a novel pixel architecture for third generation infrared detectors is proposed. This smart design introduces flux detection mechanism for the broad spectrum short wave infrared detector and dual/multicolor detectors. This architecture achieves very high dynamic range for analog ROICs.

HDR for ROIC means very dark and very bright signal levels is processed at the same time. In practical terms, HDR enables high contrast and accuracy which finds itself many applications from security to industry. The typical unit cell of a ROIC consists of the pre-amplifier, gain switches, multiplexer, output amplifier and some control switches. For a standard single band detector array, a ROIC uses only a single pre-amplifier which optimized for average performance.

In the proposed architecture, instead of using a single preamplifier, two pre-amplifiers, which are optimized for different light levels, are placed inside each pixel. A smart circuit mechanism, which decides the best input circuit according to the incoming light level, is also designed for the pixel.

In short, the smart pixel selects the best input amplifier circuit that performs the best SNR for the incoming signal level. A 32x32 prototype chip is designed in 0.18 μm CMOS technology. Chip achieves minimum 8.6 e^- input referred noise and 98.9 dB dynamic range. Operating temperature is 300 K and power consumption is 2.8 μW per pixel.

Geniş Dinamik Aralıklı Akıllı Işık Yoğunluğu Algılayıcılı Piksel Mimarisi

ROIC, SWIR, Akıllı, Birim Hücre, SNR, HDR, Kızılötesi, FPA.

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Özet

Bu tezde üçüncü nesil kızılötesi dedektörler için özgün piksel mimarisi önerilmiştir. Çift/çok bantlı dedektörler ve geniş spektrumlu dedektörler için gelen ışık akısını algılayan akıllı bir tasarım sunulmuştur. Bu mimari analog entegre okuma devreleri arasında çok geniş bir dinamik aralığa erişmektedir.

Okuma devreleri için yüksek dinamik aralık çok karanlık ve parlak sinyallerin aynı anda görüntülenip işlenmesi demektir. Özetle, yüksek dinamik aralık yüksek karşıtlık ve hassaslık sağlamaktadır. Bu özellik güvenlikten endüstriye bir çok alandaki uygulamalarda kendine yer bulmaktadır. Tipik bir entegre okuma devresindeki piksel hücresinde giriş güçlendiricisi, kazanç anahtarları, çoklayıcı, çıkış güçlendricisi ve çeşitli kontrol anahtarları bulunmaktadır. Tek bantlı bir dedektörde kullanılan entegre okuma devresi ortalama bir performans için optimize edilmiş bir tane giriş güçlendiricisi kullanmaktadır.

Önerilen özgün mimaride tek bir giriş güçlendiricisi kullanmak yerine farklı ışık seviyeleri için optimize edilmiş iki giriş güçlendiricisi kullanılmıştır. Gelen ışık seviyesine göre en iyi giriş güçlendiricisini seçen akıllı devre mekanizması da gene özgün pixel mimarisi için tasarlanmıştır.

Kısaca, akıllı pixel gelen sinyal seviyesine göre en iyi SNR seviyesini veren en uygun güçlendiriciyi seçmektedir. 0.18 μm CMOS teknolojisi kullanılarak 32x32 boyutunda prototip çip tasarlanmıştır. Çip en düşük 8.6 e^- gürültü seviyesine erişmiştir ve 98.9 dB lik dinamik aralığa sahiptir. 300 K ortam sıcaklığında çalışmaktadır ve piksel başına 2.8 μW'lık güç tüketimi vardır.

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List of Abbreviations

ADC ..... Analog to Digital Converter

ASIC ..... Application-Specific Integrated Circuit

BDI ..... Buffered Direct Injection

CCD ..... Charge Coupled Device

CDS ..... Correlated Double Sampling

CMRR ..... Common-Mode Rejection Ratio

CTIA ..... Capacitive transimpedance Amplifier

DAC ..... Digital to Analog Converter

DI ..... Direct Injection

DROIC ..... Digital Readout Integrated Circuit

DSLR ..... Digital Single Lens Reflex

DSNU ..... Dark Signal Nonuniformity

ESD ..... Electrostatic Discharge

FoM ..... Figure of Merit

FPA ..... Focal Plane Array

FPGA ..... Field Programmable Gate Array

FPN ..... Fixed Pattern Noise

FPS ..... Frame Per Second

GBW ..... Gain Bandwidth

GigE ..... Gigabit Ethernet

HDR ..... High Dynamic Range

LVDS ..... Low-Voltage Differential Signaling

LWIR ..... Long-wave Infrared

MCT ..... Mercury Cadmium Telluride

MOS ..... Metal-Oxide Semiconductor

MPW ..... Multi Project Wafer

MWIR ..... Mid-wave Infrared

NEP ..... Noise Equivalent Power

NIR ..... Near Infrared

NUC ..... Non-uniformity Correction

PCB ..... Printed Circuit Board

PRNU ..... Pixel Response Nonuniformity

RGB ..... Red Green Blue

RGBA ..... Red Green Blue Alpha

ROIC ..... Readout Integration Circuit

SFD ..... Source Follower per Detector

SNR ..... Signal to Noise Ratio

SWaP ..... Size Weight and Power

SWIR ..... Short-Wave Infrared

TEC ..... Thermoelectric Cooling

TEC ..... Termoelectric Cooler

VHDL ..... VHSIC Hardware Description Language

VLWIR ..... Very Long-wave Infrared

1 Introduction

1.1 A Brief History of Sensing the Invisible

The history of the infrared detector is backed in the year of 1800s with Hershel's the discovery of infrared radiation. In that experiment, Hershel was studying the spectrum of sunlight with a prism. He observed an increase of temperature when he was moving a thermometer from blue to red light. Just after red light when there was no visible light, he found a significant amount of rising in the thermometer. That was considered as the beginning of infrared detectors and systems.

After Hershel, there were not much effort to develop infrared detectors. Seeback's discovery of the thermoelectric effect in 1821 was the first development. Then, Nobili invented the first thermocouple in 1829. In 1880, the first bolometer was made by Langle utilizing a Wheatstone bridge. Before the end of 19th century, the first photoconductive effect was discovered by Smith. He was performing experiments using selenium.

There was a tremendous effort on photon detectors during World War I and II. Because of the ability to see the dark can bring an enormous advantage over enemies. The first infrared photoconductor, using thallium and sulfur (TI_2S), was developed by Case in 1917. The concept of the electro-optical converter was designed by Holst in 1928. The first image converter based on photocathode was made in 1934 by Philips [1].

Today's modern focal plane arrays (FPA) are recent technologies. The first generation FPA's are only single-dimensional linear structures developed in the 1960s. Those FPA's are used with scanners to generate two-dimensional images. AIM-9 Sidewinder missile used these first generation systems in their guidance system. The second generation ROIC's are hybridized with two-dimensional staring detectors. First examples of the second generation FPA's can be seen at the end of the 1970s. Third generation term is a little bit blurry; there are no clear-cut definitions as the first and second generation. However, the third generation promises more functionality and intelligence for pixels such as analog to digital conversion inside a pixel instead of column level, a large number of pixels (2048x2048), dual-band or multicolor detectors inside the same pixel and some pre-processing functionalities

Figure 1: Herschel and his famous experiment [2].

within a pixel [3]. Fig. 2 shows the evolution of detector types along with ROICs.

Digital ROIC (DROIC)'s is also part of the third revolution. They provide high dynamic range solutions [4] and charge handling capacities such as 2.3 Ge^- [5]. High photocurrents, which are available in LWIR detectors, are required to benefit from high charge handling capability. For analog pixels, there are a lot of papers and patents exist that proposes solution for high dynamic range, dual band, and dual-color third generation detectors. Some of them use more than one input amplifier instead of gain stage inside a pixel [6–9]. Their pixel provides two outputs at the

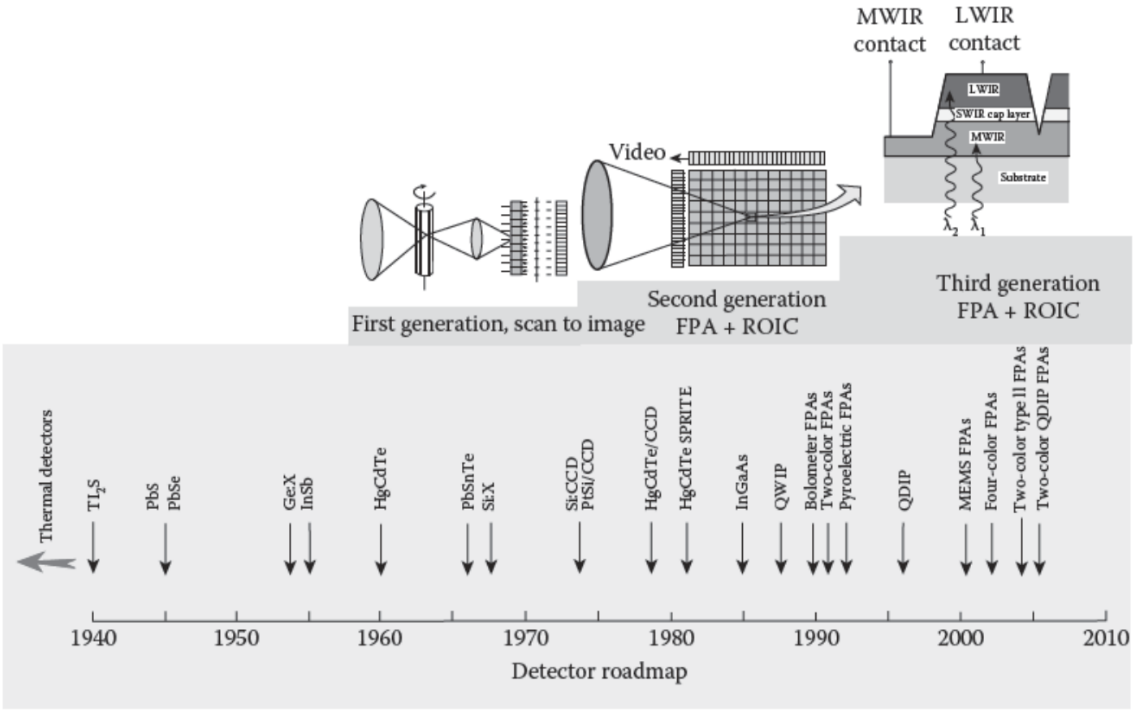


Figure 2: History of FPA [3].

same time. In [10] user may have the option to select one of the input amplifiers. Also, one of them only uses a single amplifier which produces two different outputs from two different gain settings [7].

Another approach is developing smart ROICs that includes on-chip processing capabilities and functionalities to reduce processing overhead or improve performance [11–14]. Due to features added into pixel structure, pitch sizes of these ROICs are bigger than trending small pitch sizes. Thus, they are aiming for specific low-resolution applications. Finally, the most popular third generation trend is dual or multi-color imaging systems or detectors.

1.2 Infrared Imaging Systems

Infrared imaging systems can be used in a variety of applications from civil to military; building or electrical/mechanical inspection, firefighting, machine vision, astronomy, security, surveillance, tactical systems are some of the application areas of infrared imaging systems [15]. All those systems utilize a different type of infrared sensors which work a particular part of the spectrum.

The infrared spectrum is sub-divided many sections according to its properties.

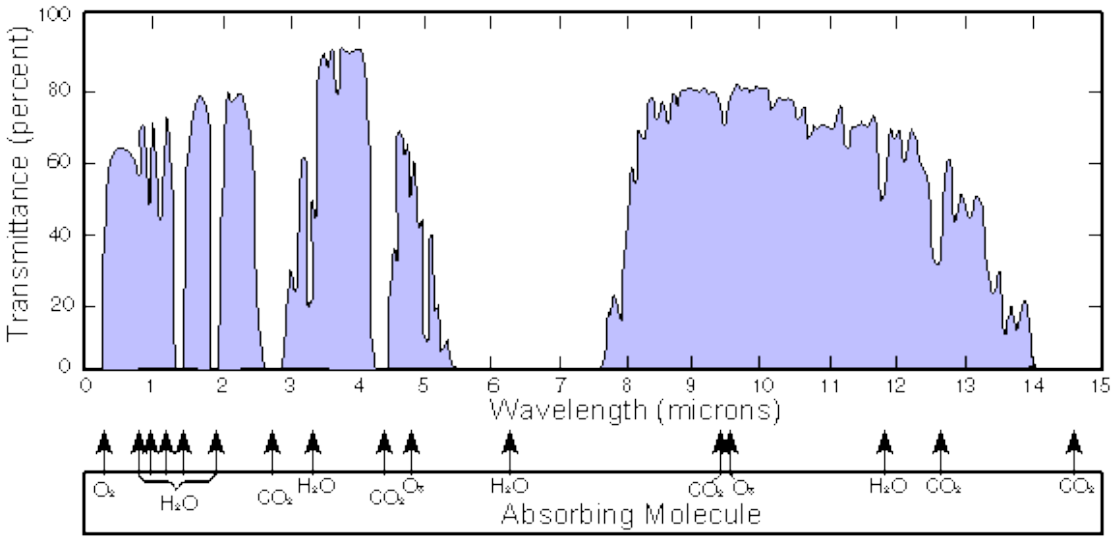


Figure 3: Atmospheric transmittance of infrared region [16].

Fig. 3 shows atmospheric absorption throughout infrared region. First sub-division starts right after at the end of visible spectrum 0.75 μm which is near-infrared (NIR). Short wavelength (SWIR) (1.4-3 μm), mid-wavelength (3-8 μm), long wavelength infrared (8-15 μm) and far-infrared (15-1000 μm) are rest of the divisions in the spectrum. To explain briefly, NIR and SWIR can be used night vision devices such as security cameras and goggles and industrial inspections for product quality. Devices that uses MWIR sensor is used mostly for missile guidance or detection together with LWIR. LWIR region known as "thermal imaging" region which can passively detect heat waves. Thermal imaging systems are mostly used for surveillance purposes in the defense industry. Finally, far-infrared region finds itself useful for astronomy such as observations of faraway galaxies.

Advanced, military and scientific infrared solutions that mentioned above are very expensive. Besides high-end products, companies are extending the product range of low-cost infrared solutions to end users. For instance, FLIR Systems Inc. released infrared camera module named FLIR ONE^{TM}for mobile phones which include a small bolometer based LWIR sensor in 2014 [17]. Moreover, SWIR sensors and systems gain popularity and can be seen for daily life more and more. For instance, SWIR camera is used in collision detection systems for cars to identify objects or human in the night or foggy weather. Another example is the detection of fake human hair, mustache, and beard due to SWIR reflection differences, in

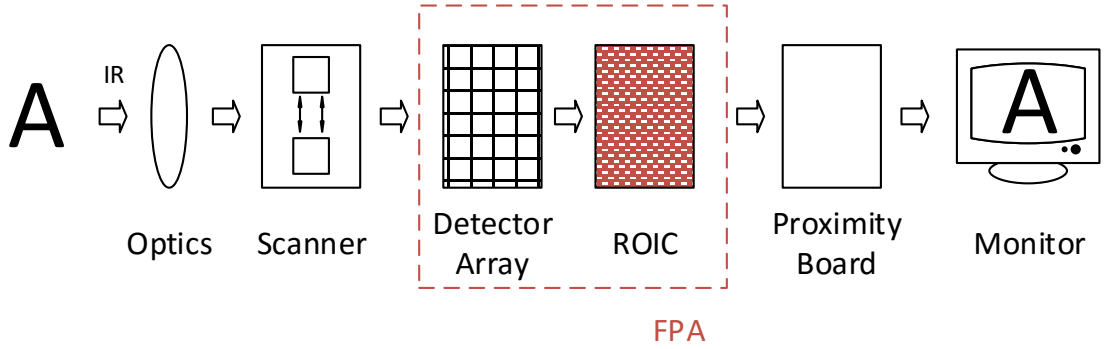


Figure 4: Block diagram of an IR imaging system.

airports and board control points.

NIR and SWIR bands are distinguished from thermal imaging bands (LWIR, MWIR). NIR and SWIR can be referred as reflected infrared and they do not sense thermal radiation. Since NIR and SWIR are reflective, they interact with objects such as bounces off of objects and create shadows and contrast like visible light. Unlike visible light, an output of reflective infrared is grayscale. For grayscale images, high dynamic range is desired for many applications such as machine vision, road traffic monitoring, security and military. Light sources or bright spots can saturate a large number of pixels and area of interest which is nearby the most lighted area can not be visible. HDR techniques are always desired to prevent saturations and improve SNR of an image, in SWIR.

Infrared imaging systems consist of many components such as detector, ROIC, signal processing and video processing modules. In Fig. 4 a typical block diagram of IR imaging system is shown. A scanner is an optional module that can be used with linear type detectors (single dimensional) to be able to create two-dimensional images. Fig. 5 shows both scanning and staring FPA's. Typically ROIC's and detectors are built on different substrates, then using flip chip bonding method, which is also called hybridization, they are connected to each other with indium bumps. This structure is called focal plane array (FPA) [18]. An output of FPA can be analog or digital.

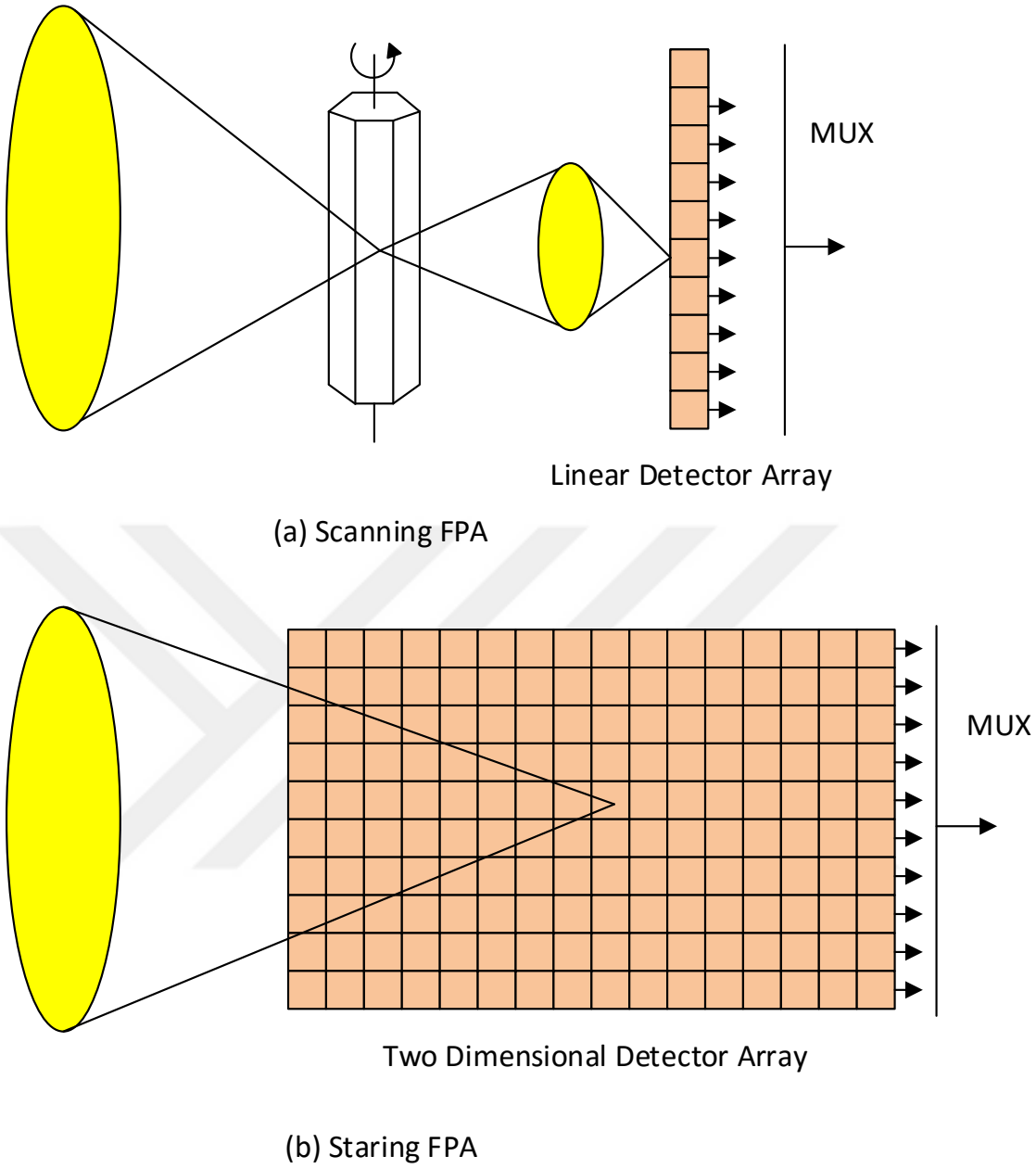


Figure 5: There are two type of FPA's a) single dimensional scanning and b) two-dimensional starring.

1.2.1 Optics

Optics is responsible for refracting infrared light to produce an image on the detector. All principles and design methodologies of visible optical elements apply to IR imaging systems. However, material choices are different. Germanium (Ge), Silicon (Si) and Gallium Arsenide (GaAs) are accessible infrared materials. Germanium is the most popular material among other options. It provides acceptable

transmittance between 2 to 15 μm wavelength. It requires extra attention for handling and cutting because it is very brittle. Ordinary glass cannot be used beyond 2.5 μm as an optical material [19].

Mirrors are frequently employed in IR systems. They were used in scanners and manifold systems. Optical crown glass, synthetic fused silica, low-expansion borosilicate glass, and Zerodur are most commonly used materials for mirror production. Also, Metallic coating is applied to these mirrors for maximizing reflectivity. Protected aluminum, gold and silver are popular material choices. Due to oxidization, bare aluminum is not among the first choices.

1.2.2 Detectors

Infrared detectors are responsible for the conversion of IR photons to electrical signals in IR imaging systems. Responsivity, noise equivalent power (NEP) and detectivity are main three figures of merit parameters for detectors. Responsivity is defined as a ratio of electrical output (rms) to input radiation (rms). Depending on the type of a detector unit of responsivity is volts per watt or amperes per watt.

$$R_v(\lambda, f) = \frac{V_s}{\Phi_e(\lambda)\Delta\lambda} \tag{1}$$

NEP is the signal power that gives SNR ratio of 1 in 1 Hz output bandwidth. It is defined regarding responsivity.

$$NEP = \frac{V_n}{R_v} \tag{2}$$

Detectivity (D) is simply given by:

$$D = \frac{1}{NEP} \tag{3}$$

Detectivity-star is found by Jones [20] to define FoM for detectors. D-star includes NEP and detector area. It simply provides normalized detectivity value to compare detectors.

$$D^* = D(A_d\Delta f)^{1/2} = \frac{(A_d\Delta f)^{1/2}}{NEP} \tag{4}$$

in which A_d is detector active area, Δf is noise equivalent bandwidth. Unit of D^* is Jones.

$$\left[\frac{cm - Hz^{1/2}}{Watt}\right] \equiv Jones \tag{5}$$

1.2.3 Cooling of IR Detectors

Depending on detector material some detectors require cooling for optimum performance. Dark current levels are reduced at some absolute low temperatures. For instance, cryogenic (77 K) coolers are used for the MWIR and LWIR detectors. Specifically, mercury cadmium telluride (HgCdTe) which is the most popular 8-14 μm detector operates the best at cryogenic temperatures. Cryogenic coolers are not efficient devices. The efficiency of cooling mechanism is around 4 %. Thus, system design of cooled IR detectors requires extra attention if the system is portable. The power consumption of the ROIC becomes significant due to low cooling efficiency. Even, system designers should consider number and shape wire bonds inside cooler from FPA to daughter board. Gold wire bonds radiate heat that is coming from FPA. Joule-Thomson and Stirling cycle refrigerator are the most popular closed cycle cooling systems. Fig. 7 shows dewar with Stirling cooler. The top part is plated with gold for shielding, and it contains FPA.

Depending on detector or performance thermoelectric cooling (TEC) is a choice for infrared imaging systems. Since cryogenic cooling requires dewar filled with LN_2, TEC becomes a cheap and compact solution. TEC's can achieve around 200 K with hermetic encapsulation. SWIR detectors do not require cryogenic cooling. Room temperature or TEC is sufficient for a typical SWIR detector.

Thermoelectric coolers work in the principle of Peltier effect. Choice of thermoelectric material is necessary and following formula can be used to determine figure of merit;

$$ZT = \frac{S^2\sigma}{k}, \tag{6}$$

in which S is the Seebeck coefficient, T is average temperature, and sigma is electrical, and k is thermal conductivity.

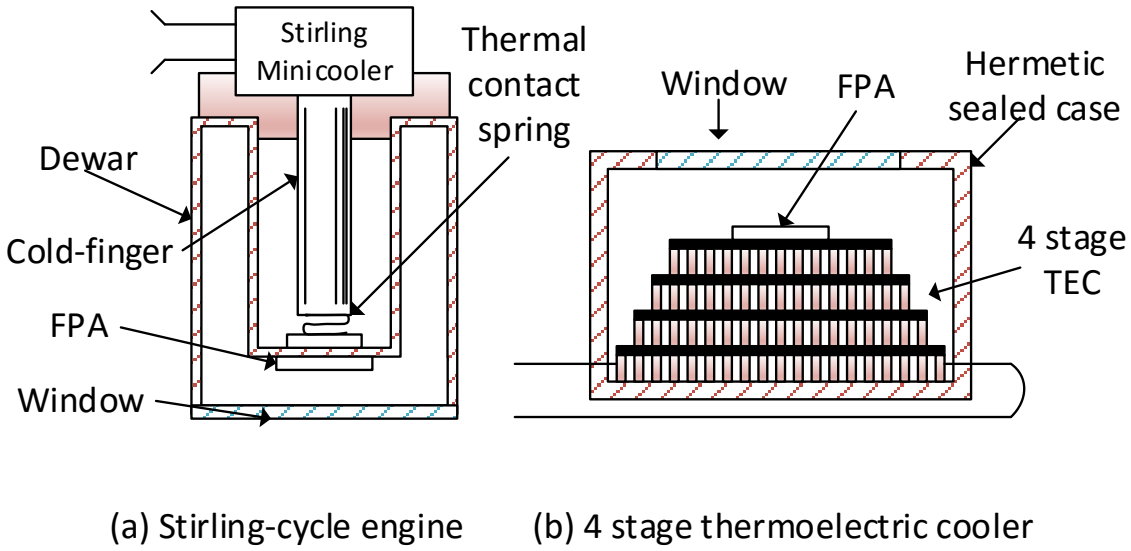


Figure 6: Cooling IR detectors (a) Stirling cycle engine (b) four stage thermoelectric cooler.

1.2.4 Proximity Board

Proximity board consists of different layers depending on the output of FPA. If FPA has an analog output, proximity board should have ADC's. All digital corrections and post-processing require being done in a digital domain. If FPA has a digital output, serial drivers such as LVDS are necessary for carrying signals to processor or FPGA. Inside the processing unit, further signal processing is applied to eliminate fixed pattern noise, non-uniformity correction, dead pixel correction. Non-uniformity correction and dead-pixel replacement are the most fundamental image processing algorithms for infrared imagers. Due to, all the detectors suffer from spatial non-uniformity and manufacturing defects.

Depending on application some sophisticated post-processing algorithms may be performed such as locking to moving objects, image fusion and, human detection on hardware or software level. Detecting human and moving objects are must have features for surveillance systems. On the other hand, image fusion element gains ground for advanced infrared imaging systems [22–26]. Image fusion is processing more than one image that comes from different sensors, into a single image. That image is a combination of essential features from various sensors. Image fusion is used in remote sensing, medical and infrared imaging systems. As mentioned

Figure 7: Crayogenic Dewar with Stirling cooler [21].

before LWIR and MWIR systems contains only heat information. Defining objects with only LWIR and MWIR information is hard. SWIR provides details such as shape and pattern of the object. Image fusion of SWIR and thermal imaging bands improves the quality of output for better detectivity. Fig. 8 shows SWIR, LWIR and hinted SWIR version of a scene. In SWIR, it is hard to identify a human being. In contrary, LWIR clearly highlights the human, but it lacks information from the

Figure 8: SWIR and LWIR Image fusion [27].

surroundings.

Furthermore, proximity board provides biases and supplies to ROIC and detector. Bias points can be adjustable via some digital interface on the board. Adjustable biases are essential to calibrate FPA. All supplies and biases coming from the board should have low noise levels to improve the performance of the system.

Digital programming of FPA also has been done on proximity board. Depending on communication protocol proximity board provides relevant digital signals. In general, FPA's comes with certain functionalities. To activate those functionalities, ROIC contains serial or parallel digital interface. Gain settings, integration time, windowing, frame speed adjustment, and dead pixel elimination are typical ROIC functions.

Finally, proximity board outputs processed image into industrial standard interfaces such as Camera Link and GigE.

1.3 Readout Integrated Circuits

ROIC is one of the key components of imaging systems. It is responsible for acquiring detector signal by integration and transfer it to the signal processing components. In other words, ROIC provides charge to voltage conversion. Signal chain block diagram of FPA is shown in Fig. 9. In short, an analog ROIC consists of a

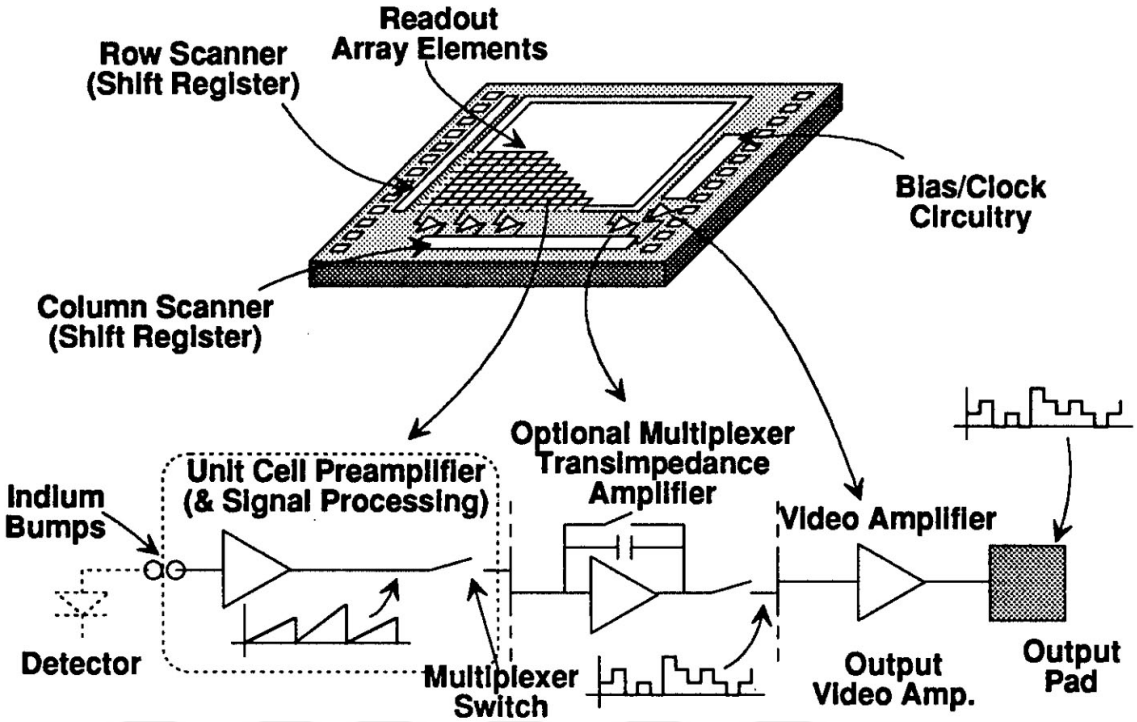


Figure 9: Block diagram of an analog readout [18].

unit cell, multiplexer, and output amplifier. In digital ROIC, the multiplexer is connected to column ADC. Instead of the output amplifier, the serial interface is used to output digital data. In ROIC designer wants to achieve the best performance for transferring photocurrent which can be defined as low noise, high SNR, and high injection efficiency.

Readout noise is undesirable, but it is unavoidable and fundamental part of the system. All ROICs suffer from readout noise which can be defined as a random variation of the output voltage level which is independent of the input current of the amplifier. Photons are emitted by light sources and emission process is defined by Poisson distribution which is a discrete probability of a given number of events occurring in a determined period. Commonly represented formula of Poisson distribution is equal to

$$P(\chi;\lambda) = \frac{\lambda^{\chi} \cdot e^{-\lambda}}{\chi!} \tag{7}$$

λ represents an average number of electrons which also equal to the variance. This phenomenon is known as Poisson noise or shot noise.

Ideal SNR can be defined the only square root of the electrons collected ignoring

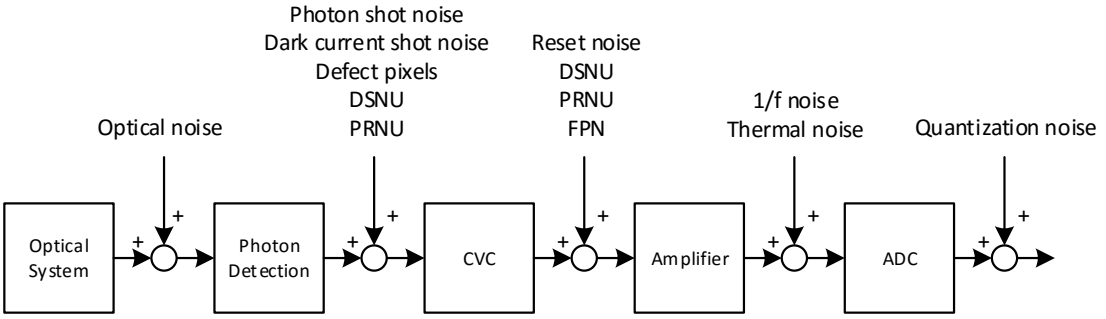


Figure 10: Noise sources in the imaging system [28].

readout noise contributions. Unfortunately, there are many noise contributions in the system, Fig. 10 shows all the noise sources that are coming from each stage. Optical noise occurs due to imperfections on the surface of a lens, coating, and material. DSNU and PRNU are dark signal non-uniformity and pixel response non-uniformity, respectively. These noise sources can be corrected with post-processing (using processor or FPGA) because they are spatial noises which do not depend on time. Fixed pattern noise (FPN) is also a spatial noise which comes from different responsivity of the pixels for the same illumination. Temporal noise sources are shot noise, reset noise (kTC noise), thermal noise (Johnson-Nyquist noise), 1/f noise and quantization noise [28].

Reset noise in order words kTC noise requires more attention to designers for low noise applications. Integration capacitance resets to fixed voltage value (reset voltage) at the beginning of a frame. Due to Maxwell-Boltzmann distribution of the number of the electrons on the capacitor, the voltage on the capacitor fluctuates and exact value is not defined. Reset voltage varies between reset cycles within some electron range depending on various effects such as design and temperature. This variation is called kTC noise or reset noise.

There is a fundamental method to remove reset noise which is called correlated double sampling (CDS). The CDS should take two samples for each frame; the first one is just after reset, and the second one is at the end of the integration. The difference between two sample will remove the reset noise because both samples introduced to the same level of reset voltage bias. This method is widely used not only FPAs but also CMOS and CCD sensors [29]. There are analog and digital implementations of this method. New generation readouts utilize a digital implementation of CDS because of it does not consume pixel space, and it provides calculation

Table 1: ROIC performance requirements and its relation with system parameters [18]

ROIC Performance Parameters	Related System Parameters	Comments
Input referred noise	Sensitivity	Reduce to enhance SNR
Charge handling capacity	Integration time and photo-current	Current handling range
Power dissipation	Cooldown time, life time ,and weight	SWaP
Crosstalk	Blooming of saturated elements	Element to element
Dynamic Range	Maximum saturation signal	Loss of signal
Linearity reliability	Calibration	Proper identification
Gain	Sensitivity	Signal amlifier above noise floor
Uniformity	Fixed pattern noise	Eliminated with post processing

flexibility and less complexity.

1.4 ROIC Performance Parameters

ROIC performance parameters strongly depend on detector and application. For instance, the detector type and its performance affect charge handling capacity. If a detector is a dark current level high small integration capacitance may saturate easily. Thus, high charge handling capacity can be the desired parameter for that kind of detector.

Designers do not have much choice regarding technology. Excluding DROIC's all other ROIC's uses 180 nm and bigger CMOS nodes mature technologies. Those technology nodes offer an excellent price-performance ratio. All these parameters should be considered regarding these technologies.

Table 1 summarizes critical ROIC performance parameters and their effects on system requirements. Some of the important concepts will be explained following subsections.

1.4.1 Charge Handling Capacity

Most of the detectors that used in FPA's are photoconductors. Thus, an output of the detector is photo-current. ROIC integrates these currents into capacitance in each pixel. The capacitor is a dominant device inside the pixel. Photon emission process is defined by Poisson distribution, and it shows shot noise behavior. So, capacitances store not only signal charge but also store noise which is proportional to square root of the stored signal. Hence, charge handling capacity is essential for improving SNR. Depending on interested wavelength charge handling requirements change. Photocurrents in SWIR typically between 10pA-3nA. On the contrary, typical LWIR photocurrent level is 10nA. It may go up to hundreds of nanoamperes. At the same time, an application is also the important parameter to determine charge handling capacity. For instance, space observation systems do not require significant charge handling capacity because photocurrent levels coming from stars are very low.

There is a tradeoff between charge handling capacity and pixel size due to capacitance size. Since charge handling capacity is necessary for noise and applications, detector trend pushes designers to smaller pixel pitch sizes and bigger arrays. In recent systems, spatial resolution is needed for detection than charge handling capacity. In very near future, smaller than 10 μm pitch sized detectors and systems will attract considerable attention.

Charge handling capacity (e^-) of analog preamplifier can be calculated simply by capacitance formula:

$$ChargeHandlingCapacity(e^-) = \frac{C\Delta V}{q} \tag{8}$$

1.4.2 Frame Rate

The frame rate is the frequency of sequenced frame data out of the ROIC. The frame rate is counted per second. The human eye and brain interpret more than 25 frames per second (fps) data as video. Most of the imaging systems work at 50 Hz. However, some scientific or military systems require higher frame rate such as 400 Hz. From IC designers perspective high frame rate requires high throughput. High throughput results into high power consumption and design challenges. Specifically,

the magnitude of those challenges gets bigger for large array sizes.

1.4.3 Input Referred Noise

Input referred noise electrons defines minimum detection floor of the ROIC. There are many contributions to input referred noise from unit cell. KTC noise of the integration capacitor, preamplifier, multiplexer, and buffer noises are square summed at the output and divided into transfer function of the ROIC. The final value is input referred noise. Depending on operating wavelength typical noise values vary. Due to high shot noise in LWIR and MWIR bands, 1000-100 e^- noise range is typical. A SWIR can have lower than 10 e^-.

1.4.4 Dynamic Range

Definition of dynamic range is universal. In ROIC, dynamic range is the ratio of the maximum detectable signal level without saturation over minimum detectable input signal. Maximum range is limited with charge handling capacity, and minimum range is input referred noise floor. Dynamic range is a number, and it is defined in dB.

ROIC with ultra high dynamic range provides high contrast and accuracy for target scenes. Bright areas will not saturate easily, and dark zones will include more information. Fig. 11 compares regular and high dynamic range images. In a normal image, bright and dark zones lost all the information. Saturated traffic signs are readable, and branch of trees are visible, in HDR image. Also, the road is not bright anymore, and the pattern is apparent.

Dynamic range is defined by;

$$DR = \frac{DR_{Hi}}{DR_{Lo}} = \frac{ChargeHandlingCapacity}{InputReferredNoise} \tag{9}$$

or

$$DR[dB] = 20log\frac{DR_{Hi}}{DR_{Lo}} \tag{10}$$

Figure 11: High dynamic image vs regular image [30].

1.4.5 Linearity

The relationship between photocurrent and the integrated charge should be linear. 95 % linearity is acceptable for most of the ROIC's. If ROIC has high nonlinearity output data either maps to dark or bright pixels. Linearity is also performance parameter for detectors. In modern technologies using well-known detector materials, 99 % linearity is achievable.

1.4.6 Uniformity

In FPA's, non-uniformity is inevitable. Due to mismatches and process variations, both pixels of ROIC suffers from non-uniformity. In other words, for a same photocurrent level pixel to pixel response is different.

Uniformity is also valid for detectors. In there, a cause of non-uniformity is fixed pattern noise. Dark signal non-uniformity (DSNU)and pixel response non-uniformity (PRNU) reasons of fixed pattern noise. DSNU is observed as a difference offset amount dark pixels. PRNU is pixel-wise variation under fixed illumination.

Non-uniformity is well known and studied subject; it is corrected in post-processing.

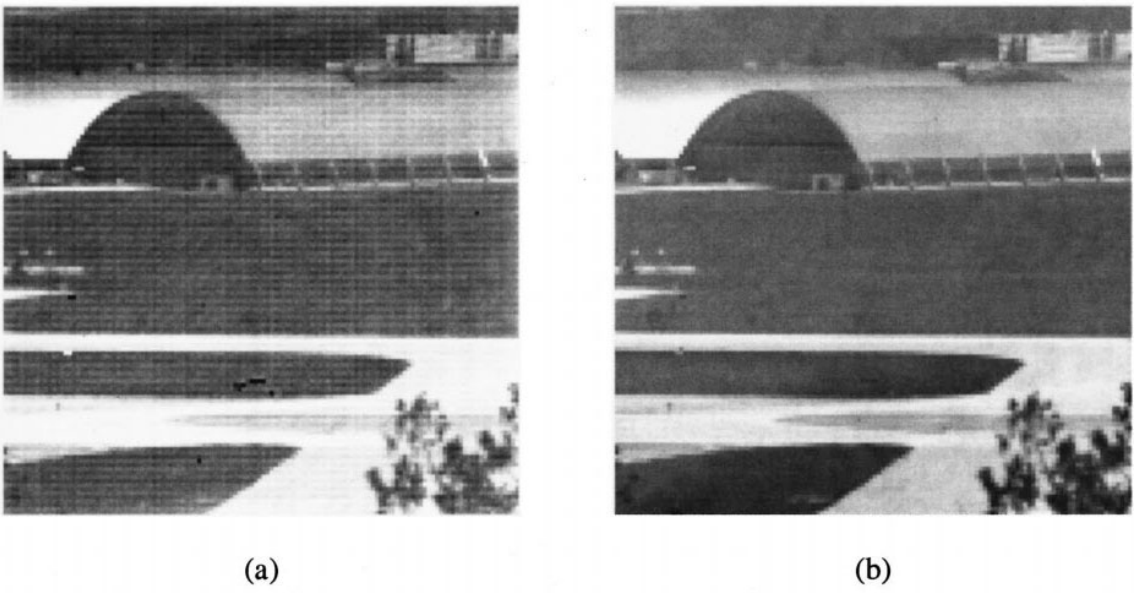


Figure 12: Non-uniformity correction, a) raw image b) corrected image [31].

Fig. 12 shows the comparison of the raw and corrected image. There is a visible pattern in Fig. 12 a) that pattern is corrected well in b). Non-uniformity correction (NUC) algorithm creates a map for both PRNU and DSNU which contains offset correction values for each pixel. That map is added on top of the output image. To generate correction map, FPA is calibrated with uniform dark and average hot (illuminated) scenes. Algorithm corrects for different illumination levels. In literature, there are many studies regarding efficiency and low power NUC algorithms.

1.4.7 Power Dissipation

Power dissipation is crucial for portable and cooled systems. For system perspective, low heat translates into a compact cooler, long operation time and increased lifetime. Moreover, reducing power dissipation shortens cooling time. Thus, infrared imaging system will be operational in very short period. Size, weight, and power reduction (SWaP) trend forces to swap large systems. The ongoing developments are trying to reduce system sizes (cooler size) without sacrificing performance (resolution and speed). Tactical and high-performance systems do not have strict power consumption parameters.

1.4.8 Gain

Integration capacitance inside the unit cell is not one-piece for almost all ROIC's. A user has the flexibility to increase or decrease total integration capacitance size at some point. This option gives a user to adapt low or high flux environments. Low capacitance provides better kTC noise performance, and high capacitance does not saturate easily. The user has 2 or 3 gain options. That option is manually selected for all array.

1.5 Motivation

This thesis is in the design of readout integrated circuits (ROIC) for infrared focal plane arrays (FPAs) with high dynamic range (HDR), utilizing a smart input circuit selection mechanism. HDR for ROIC means very dark and bright signal levels is processed at the same time, which in return results in a low noise level and high SNR. In practical terms, HDR enables high contrast and accuracy which finds itself many applications from security to industry. The purpose of the proposed thesis will be to show a new approach to achieving high SNR levels and create novel and smart circuit approaches that are applicable for next generation analog ROICs.

The typical unit cell of an ROIC consists of the input amplifier, gain switches, multiplexer, output amplifier and some control switches. For a standard single band detector array, an ROIC uses only single input amplifier which optimized for average performance. Moreover, gain switches inside unit cell used to adjust capacitance value at the integration node which allows changing charge handling capacity. In order words, increasing integration capacitance allows handling larger signals while compromising noise performance.

This thesis focuses on achieving high dynamic range for an ROIC. A novel method is applied to a unit cell. Instead of using single input circuits, two input circuits which are optimized for different signal levels placed inside each pixel. A smart circuit mechanism, which decides best input circuit according to incoming light level, is also designed for each pixel. In short, an individual pixel can select best input amplifier circuit that is performing best SNR for the incoming signal level.

1.6 Thesis Objectives

Up to now, ROIC's that have HDR capabilities designed and implemented on top the known architectures. Ideas and improvements are limited to minor changes inside unit cell. Meanwhile, HDR is a hot topic in image and signal processing world. People are trying to enhance capabilities of existing hardware with novel and efficient algorithms. They are always limited with boundaries of the hardware.

DROICs are recent technologies that achieve high dynamic ranges which exceed analog ROICs. Until today, there is no commercially available DROIC inside an IR system. Main reason is expensive for two-dimensional FPAs DROIC requires at least 90nm technology. As oppose to the recent trend, pixel sizes are big. Their advantage is with high charge handling capacities which enable them to achieve HDR. That limits their operation between MWIR and LWIR bands which have high photocurrents. Moreover, the noise floor is high compared to analog ROICs.

In the light of these points that mentioned above, the first objective of the thesis is to achieve HDR with low input referred noise (noise floor). Novel methods are employed to realize this architecture. That will be accomplished with analog ROIC concepts to avoid disadvantages of DROICs.

Another objective is compatibility with 3^{rd} generation detectors. 3^{rd} detectors promises more than detection of more than one band within the single pixel. Proposed ROIC architecture promises not only HDR but also a wide operating range (wide band operation).

1.7 Organization

This thesis is organized as follows:

The first chapter starts with the brief history of IR detectors. Then, it gives the overview regarding infrared imaging systems. In the following section, ROIC and its performance parameters are discussed. Finally, motivation and objectives of the thesis presented.

Chapter two provides detailed information regarding ROIC architectures. Then, proposed smart pixel structure and alternative architectures will be discussed in detail.

The third chapter is devoted to the implementation of proposed architecture.

32x32 ROIC is implemented to prove proposed idea. Design and implementation of the sub-blocks of the prototype will be provided.

Measurement results of the prototype are presented and discussed in the fourth chapter. Measurement equipment and methods also explained in there.

Last chapter summarizes proposed points of novel architecture along with pluses and minuses. Future design perspective is given utilizing proposed architecture.

2 ROIC Architectures

ROIC made it possible two-dimensional FPAs in the 1970s. Early ROIC's was based on custom charge-coupled device (CCD) technology. Today, CMOS technology offers cheap, low power, and highly integrated solutions to ROIC requirements.

ROIC provides integration of photocurrent and multiplexing from a large number of pixels. In other words, it provides charge to voltage conversion and multiplexing. Integration is the keyword. Not only ROIC is integrated by itself but also ROIC + Detector integration key technology. That integration is called hybridization. Fig. 13 represents hybridization techniques. The most popular technique is indium bumps. Indium bumps provide low resistance and soft contact between detector and ROIC pixels. Due to properties of indium, this technique is compatible with cryogenic temperatures. Indium stays soft even at that temperature levels.

Modern ROIC's that are used in FPA's can be categorized into two; analog and digital. Analog ROIC or ROIC integrates photocurrent and stores it into a capacitance. Analog pixel output is multiplexed to an output buffer. Some ROICs employ column ADC's; pixel output is digitalized, and output of ROIC becomes digital. The signal flow of DROIC is a little bit different than analog ROIC. ADC

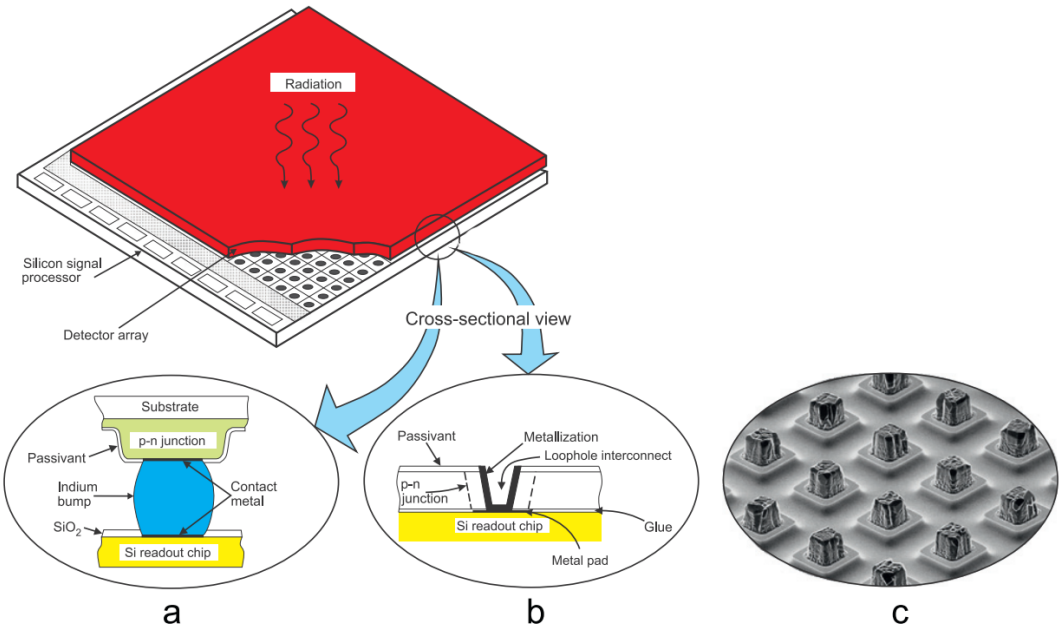
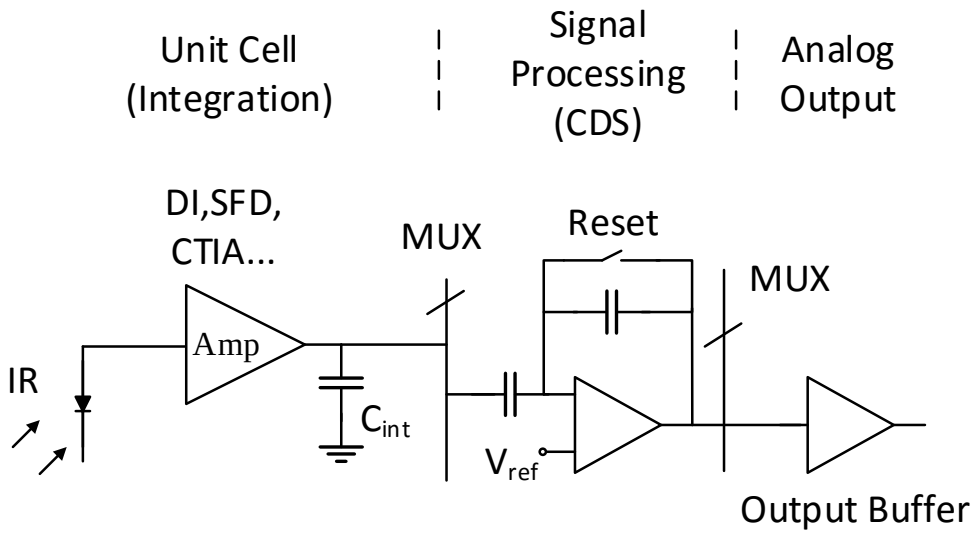
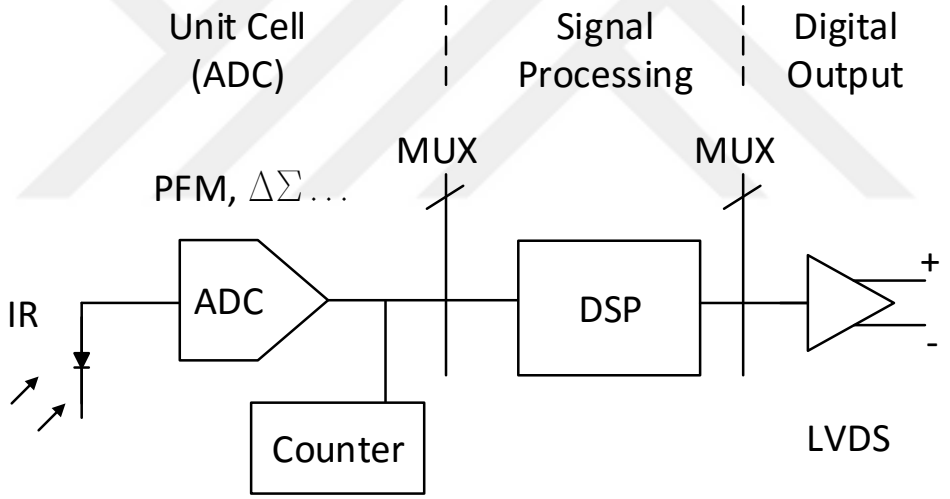


Figure 13: Hybridizated FPA (a) an indium bump (b) loophole technique (c) SEM photo of indium bumps [32].



(a) Analog ROIC Signal Chain



(b) Digital ROIC Signal Chain

Figure 14: Comparison of (a) analog and (b) digital (c) ROIC signal block diagrams.

conversion is done inside a unit pixel. Data is stored in digital domain inside the pixel. Instead of video buffer, a serial digital interface will output signal information.

Fig. 14 shows analog and digital ROIC signal chains. Analog ROIC consists of a unit cell, multiplexer and optional signal processing module (in this case CDS) and

output amplifier. Digital ROIC consists of in-pixel ADC, some signal processing module, and a digital serial output amplifier (LVDS). The main difference between two architectures lays inside a unit cell. One of them stores integrated charge into capacitance, other stores it inside a counter.

Analog ROIC may also have digital output amplifier (LVDS). Analog ROICs with column ADCs are quite popular. So these architectures also utilize benefits of digital output.

Each architecture has some advantages and drawbacks one to another. In the market, analog ROICs are dominated by a huge margin. 99 % of the market uses analog ROICs inside their FPAs. In literature, various DROIC architectures are available. There are many universities and companies available studying on DROIC. Table 2 compares both architectures with their advantages and drawbacks.

After charge-to-voltage conversion inside the pixel, there are two possible processing methods. The first method is multiplexing analog voltage to an outside of the FPA where it can be read by proximity card which consists off-chip electronics. The second method is using column ADC and converting analog data into digital and output digitally. Both approaches require different attention for designing proximity card. A user may need 14-16 bit ADC chip to sample an analog output. Depending on the speed of digital output some unique interfaces may need to acquire data such as LVDS. LVDS can typically provide around 650 Mbit/s speed, and it may go up to a rate of 3 Gbit/s. In both ways, analog to digital conversion is required at the same level to further process data. Final post-processing can be done with FPGA, ASIC or high-speed processor.

2.1 Analog ROIC Sub-blocks

2.1.1 Preamplifiers

The most critical part of the analog readout is preamplifier. Choice of preamplifier depends on many parameters such as frame rate, injection efficiency, and noise. As mentioned previously preamplifier contains a significant part of noise contributions of the system. Thus, if a designer wants to improve SNR of the system, preamplifier selection is crucial.

Basic unit cell operation is shown in Fig 16. Initially, reset switch is active

Table 2: Advantages and drawback of Analog and Digital ROICs.

	Analog ROIC	Digital ROIC
Advantages	+ Reliable architecture + Small pitch sizes + Works all bands + Cheap + Low noise + Big array size	+ High charge handling capacity + High dynamic range + Low power architectures available + Simple architecture
Drawbacks	- Limited charge handling capacity - Charge handling limited with capacitance size - Relavityle complex - Analog signal routing	- Commercially not available - Expensive tech. cost - High noise floor - Susceptible to switching noise

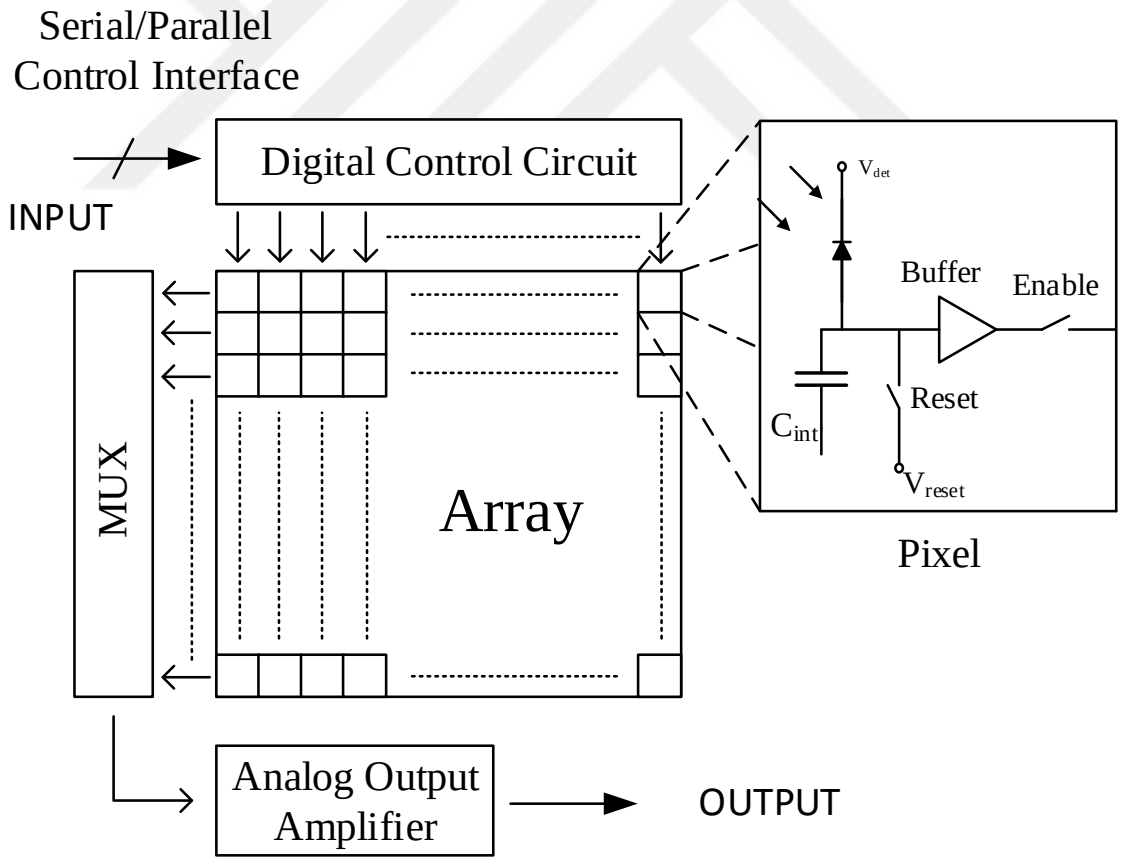


Figure 15: Architecture of analog readout integrated circuit.

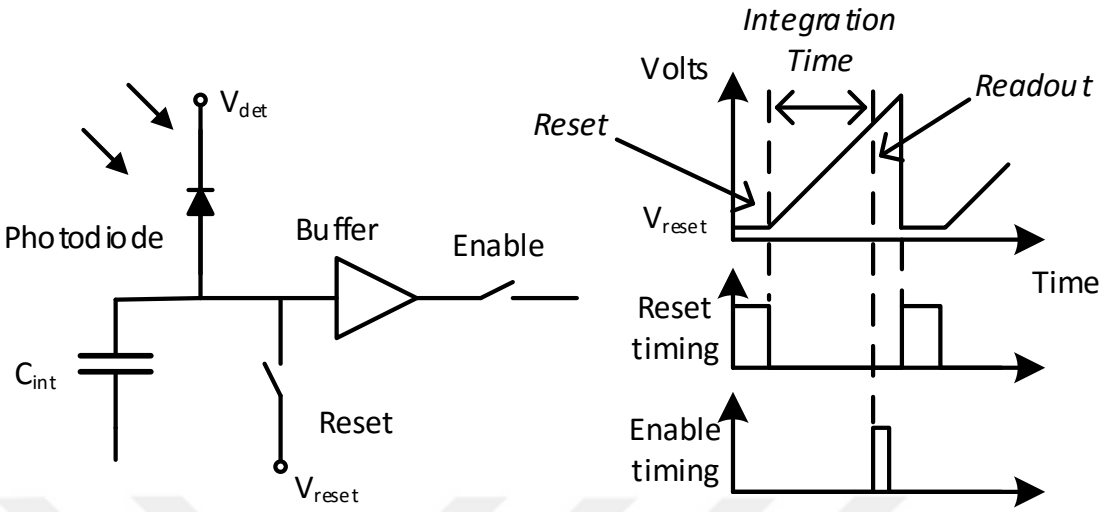


Figure 16: Schematic of unit cell operation.

and the detector is biased between V_{det} and V_{reset} voltages. Integration operation immediately starts after reset switch becomes open. During integration, according to light level and detector bias, DC current is integrated on C_{int} capacitor. C_{int} consists of all parasitic capacitances in that node, the input capacitance of buffer, integration capacitance, and interconnection capacitances.

Preamplifier which is located inside a unit cell is the first electrical interface between ROIC and detector, which is also responsible for the integration of current and charge to voltage conversion. Detector characteristics such as input impedance, detector bias and input current determine preamplifier topology. There are various types of preamplifiers, but most common ones are a direct injection (DI), source follower per detector (SFD) and capacitive transimpedance amplifier (CTIA). Two critical parameters can be used to determine amplifier type for a pixel. These are illumination level and readout frame rate. These parameters will be used to determine well capacity and noise performance of the pixel.

DI consists of an only single transistor, and it has very small circuit area. It is commonly used for high flux applications due to high well capacity. It shows poor injection efficiency under low flux applications. Since it consists of single transistor

Table 3: Comparison of popular preamplifier topologies.

Topology	Advantages	Disadvantages	Comments
Direct Injection (DI)	Low power Large well capacity Constant detector bias LWIR, MWIR	Poor performance with low flux	Popular for high flux applications
Capacitance Transimpedance Amplifier (CTIA)	Low noise Highly linear Stable detector bias Wide dynamic range High Gain	High power Complex Large footprint	Best choice for SWIR
Source Follower per Detector (SFD)	Simple Small Low Noise Low Power	Gain <1	Commonly used in IR astronomy
Buffered Direct Injection (BDI)	Detector bias is set independently High injection efficiency Improved frequency response	More complex Mid noise compared to DI Needs compensation	Rarely used

power dissipation of pixel is very low. Because of these properties, DI is widely used for LWIR and MWIR imaging applications.

SFD architecture is also very compact and low power. It consists of only three transistors. Unlike DI, SFD is more suitable for low flux applications such as CMOS image sensors and SWIR due to small well capacity (100,000 electrons). It poorly performs under high flux applications.

CTIA is very flexible and can be used for all type of detectors. It has very high linearity for low flux application and high noise compared to SFD. It performs poorly under high flux applications compared to DI. Well capacity is around 1 million electrons. Due to the complexity of structure and number of transistors it requires high power. High linearity for low flux and medium size full well capacity make this favorable architecture choice for SWIR applications. Fig 17. shows all three the most basic amplifiers that are used in ROICs.

2.1.2 Signal Processing

One of the most popular and fundamental signal processing for ROIC is correlated double sampling (CDS). CDS eliminates correlated noise, kTC switching noise.

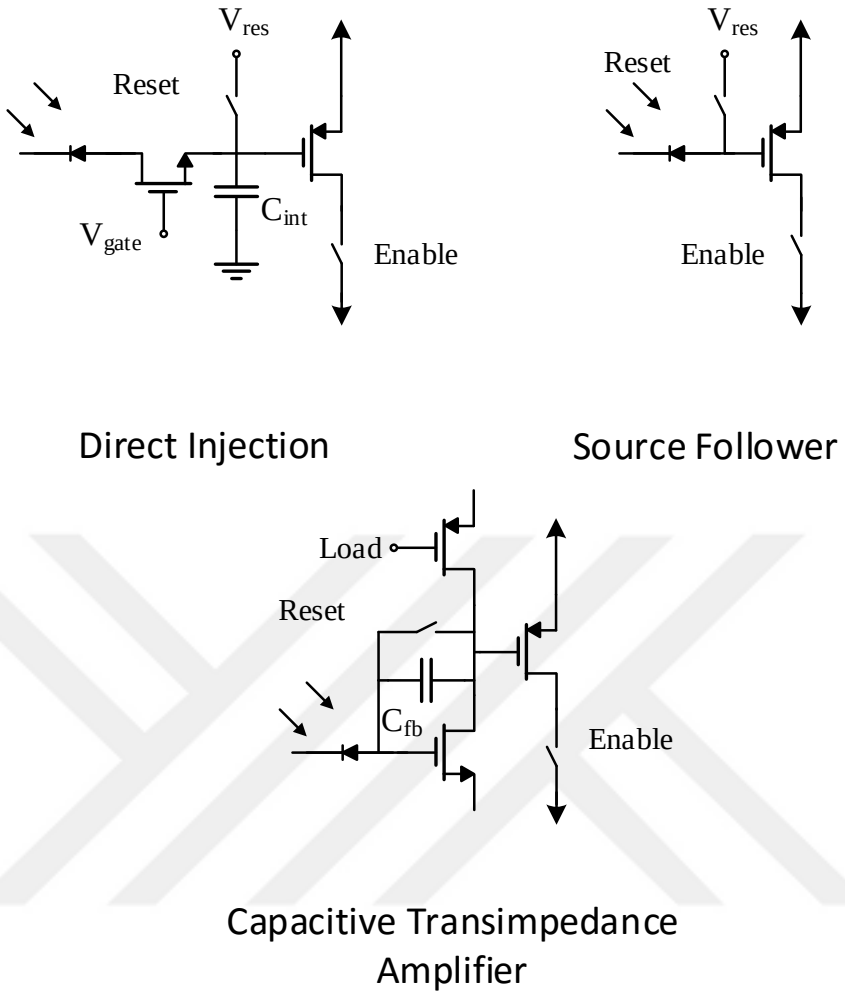


Figure 17: The most popular types of amplifiers used in readout circuits.

KTC noise also known as thermal noise is generated at the end of reset cycle. Noise ($v_n = \sqrt{\frac{kT}{C}}$) is stored on capacitor (C_inT) until beginning of next cycle [33,34]. Integration capacitance is measured twice to eliminate noise. First, voltage value after the reset cycle is stored. At the end of integration voltage value on the integration capacitance saved the second time. The difference value is free from offset and kTC noise.

KTC noise is caused by thermodynamic fluctuation of the charge on the capacitor. Once the capacitor is isolated from a source, the variation is frozen at same random value. Fig. 18 represents reset uncertainty for different integrations. Electrical charge of the reset noise on the integration capacitor can be represented as standard deviation [35],

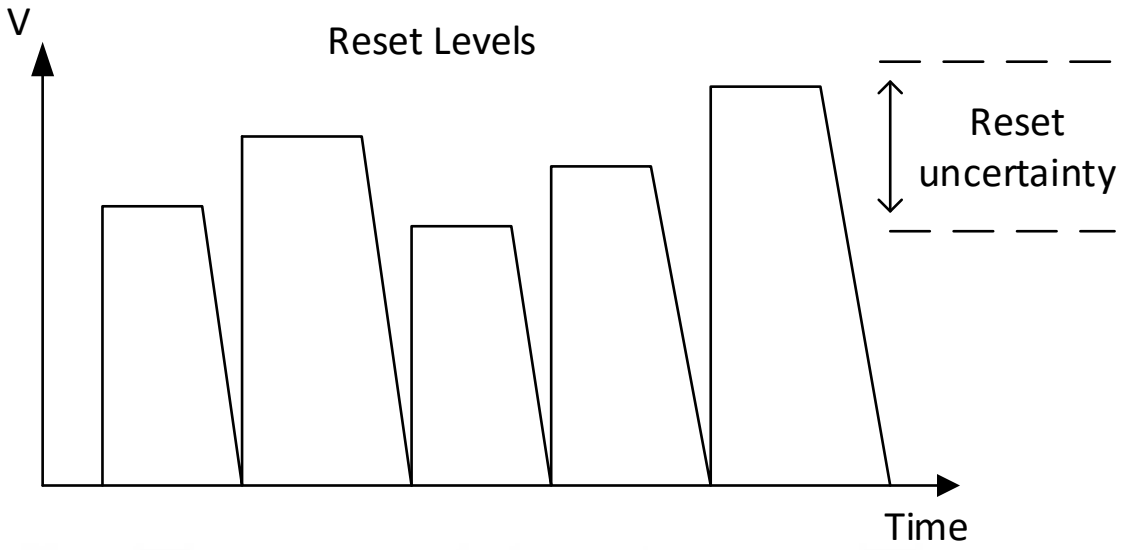


Figure 18: Reset uncertainty due to thermodynamic fluctuations.

$$Q_n = \sqrt{k_B T C} \tag{11}$$

where k_B is the Boltzmann's constant, T is the temperature in Kelvin, and C is integration capacitance.

2.1.3 Output Buffer

The output buffer is responsible for transferring different pixel voltage values to outside world. If FPA is working in cryogenic temperatures, output buffer should be able to drive long cryogenic interface cables. Designer pays attention to following points for output buffer; power dissipation, frequency response, and slew rate.

Output load (C_L) is the limiting factor designing output buffer. The output of the buffer is series of pulses with different voltage levels. Since the output is a pulse, GBW product of the buffer should be large enough. Slew rate is another critical parameter. Since buffer deals with series of pulses with different amplitudes, the buffer should be able to charge and discharge load fast to generate non-distorted pulses. Otherwise, amplitudes of pulses may not be accurate.

There are two traditional topologies of video output buffer which shown in Fig. 20. The most common method is source follower. It is relatively low power, and the

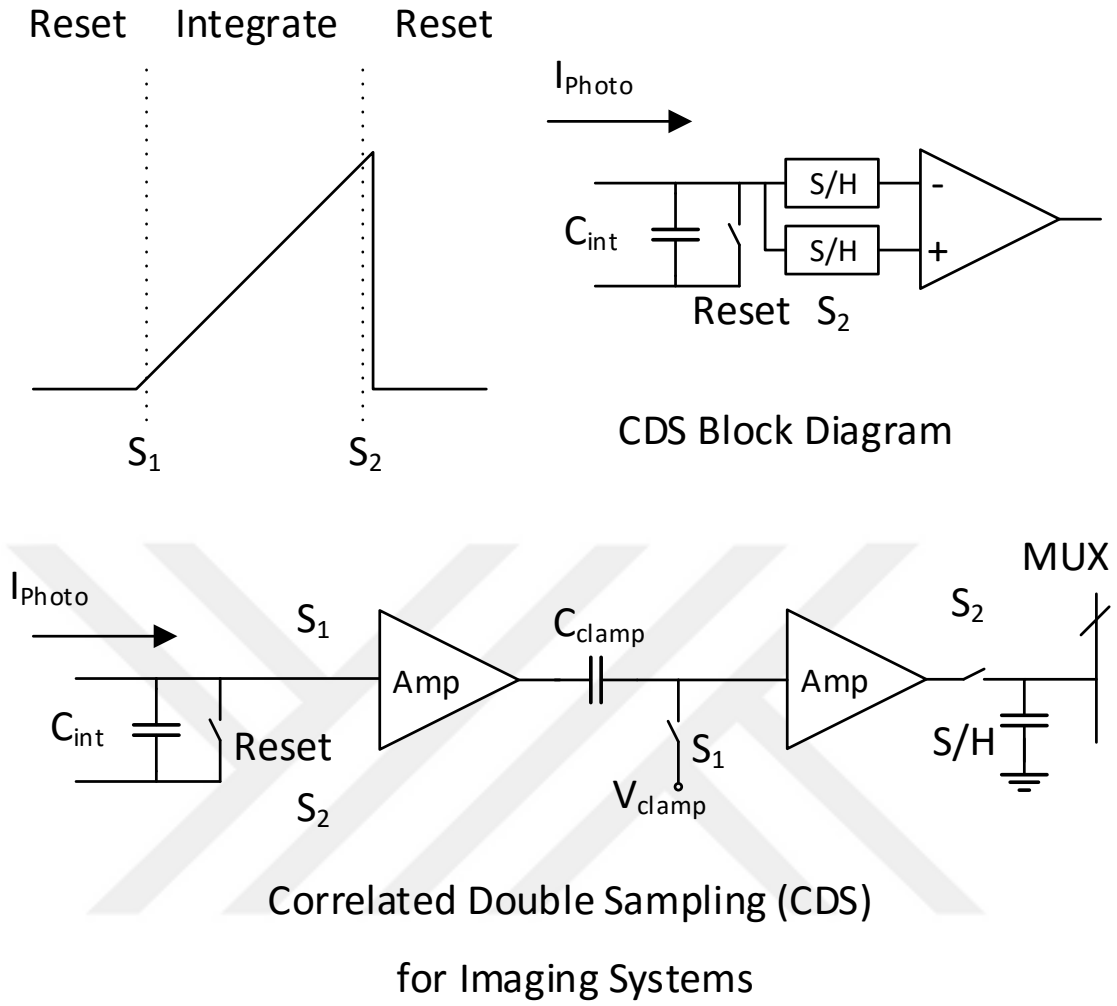


Figure 19: Correlated double sampling timings, block diagram, and implementation.

circuit is less complex. Another method is push-pull topology. Push-pull design is complicated than source follower. Push-pull needs to appropriately biased; quiescent current should be provided to transistors active. Push pull has advantages over source follower regarding power consumption.

$$E(C_L) = \frac{1}{2} C_L \Delta V_{max}^2 [J] \tag{12}$$

In the push-pull topology, the total power is calculated multiplying the energy and the repetition rate, and adding the energy required to provide the idle current [18].

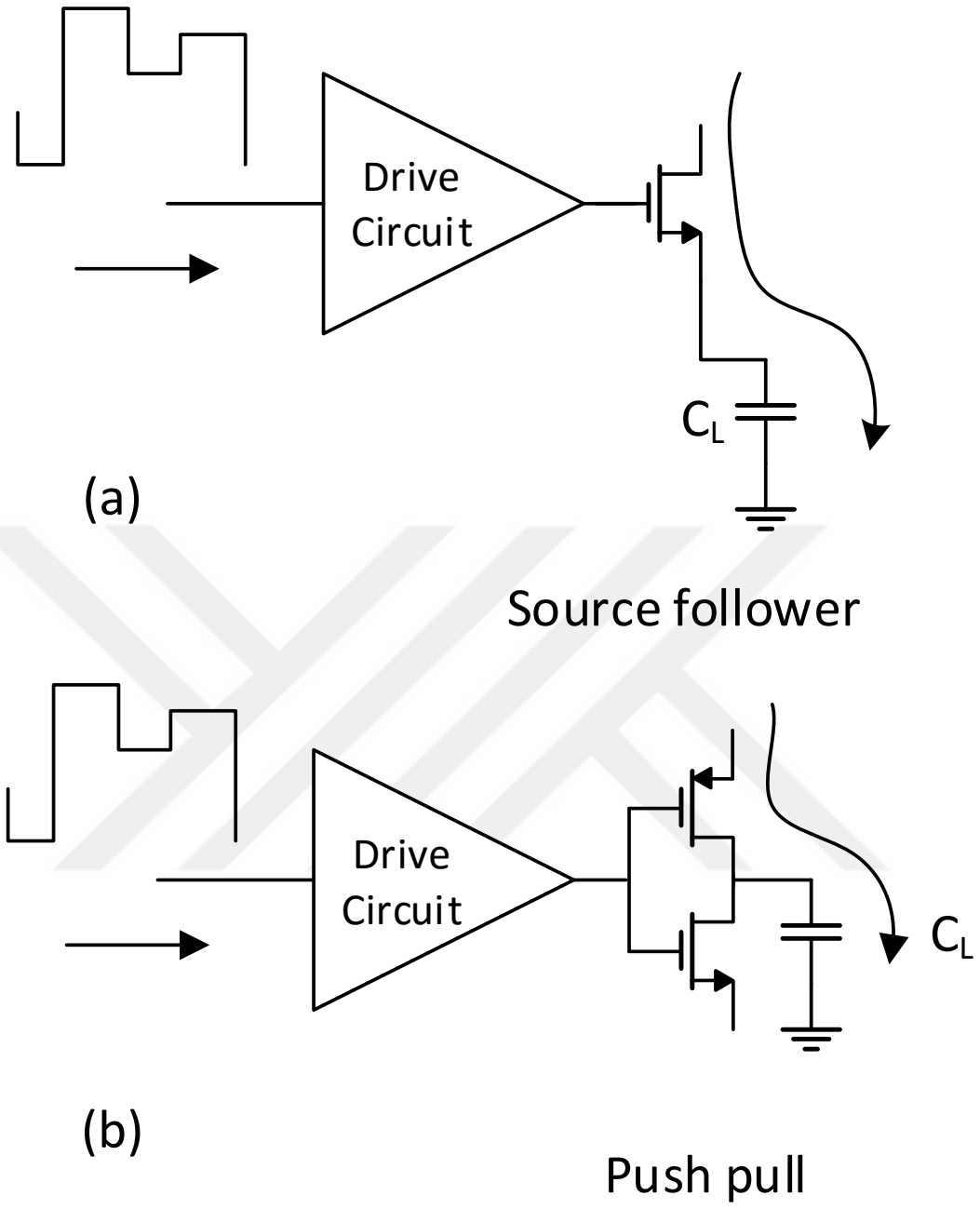


Figure 20: Video output buffer with a) source follower and b) push pull output stage.

$$P_{out}(min) > \frac{0.5 C_L \Delta V_{max}^2}{T_{frame}} + (\Delta V_{max} + 1.5) I_{idle}[W] \tag{13}$$

in which C_L is the total output load, ΔV_{max} is the maximum output swing, T_{frame} is the time between two frames.

2.1.4 Digital Control

Digital control blocks exist in all ROICs. It is responsible for generating all control signals. Integration time, controlling readout, adjusting gains, and this block provides all timing. Physically it is located on top of the unit cell array. Its height flexible but its weight is as wide as the array.

Digital control accepts inputs from outside. Clock and reset signals are essential for operation. Also, the integration time is provided to control circuit. Moreover, there are some basic functionalities such as gain adjustment, integrate while read, integrate then read, frame rate and the number of outputs. All these features can be adjusted via serial or parallel interfaces. Most of the ROICs prefer the serial interface over a parallel interface to reduce the number of pads. P

It is designed using one of the hardware description languages (Verilog or VHDL). It was very complicated to make fully custom. Then RTL code pass through digital synthesis procedure. The synthesized code was placed and routed by EDA software.

2.2 Proposed Architecture of the Smart Pixel

A generic pixel structure for hybrid readouts consists of the input amplifier, gain switches, control switches such as reset and enable, and a multiplexer. We have already examined this structure before along with commonly used input amplifiers. This proposed architecture uses two input amplifiers one is optimized for low illumination levels, and the other works well with relatively high illumination levels compared to first one. Fig 21 shows both regular and smart pixel architectures. Smart pixel not only distinguishes with some amplifiers but it also has an intelligent control unit.

The smart control unit, which is unique and works independently for each pixel, decides which input amplifier should be active. For both low and high illuminations always best input amplifier will be selected. Hence, input dynamic range will be extended. Additionally, the smart control unit provides 1-bit information which shows selected input amplifier. This information is useful for post-processing such as nonuniformity correction.

There are two possible mechanisms for smart control pixel which is the heart of the smart pixel. The first method is depending on previously integrated illumination

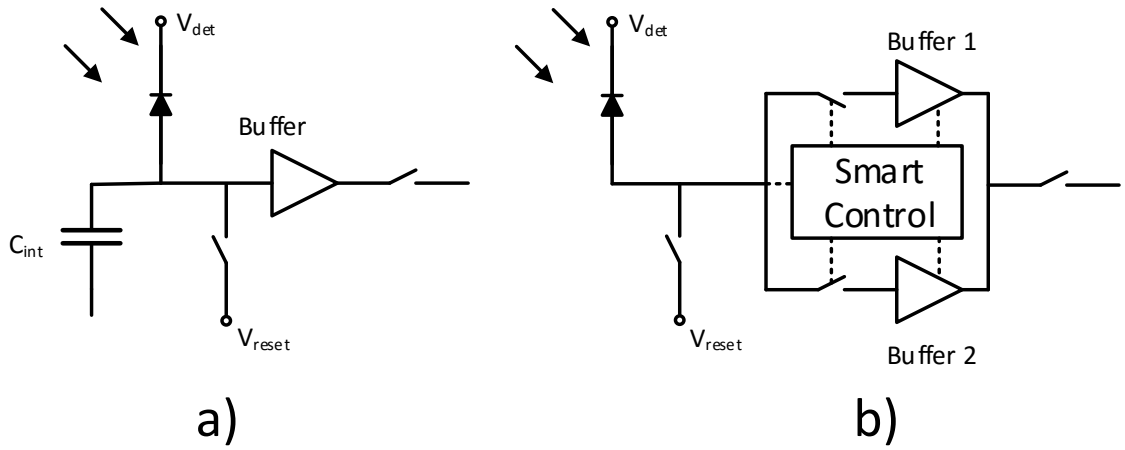


Figure 21: a) Standard pixel structure b) smart pixel architecture.

level. In this approach, if flux information from previous integration was low, in the present integration low flux optimized input stage is selected. When low illumination optimized input stage is selected, but incoming flux level is high, in the following integration high illumination optimized input stage will be chosen. This method has some drawbacks using best input amplifier may not be possible for fast changing scenes.

In the ideal world, each pixel should detect incoming light level and select best input amplifier. The second scheme tries to achieve an ideal scenario. In this scheme, there are two integrations. First integration is very short compared to the second (actual) integration. The charge which obtained from said first integration would be used to determine light level by the smart control unit. The intelligent control unit determines and activates best input amplifier for actual integration. Fig 21 shows the representation of timing diagram of the two-level integration.

For detecting light level, one of the amplifiers must be used. To obtain more gain and sensitivity low illumination level optimized amplifier is used as a default. Control mechanism compares acquired charge from first integration and certain threshold voltage. If the integrated charge is less than that certain threshold level, then the first input stage is chosen. Otherwise, the other input stage is activated by the smart control circuit. DAC can monitor this threshold voltage, and same value will be used for all pixels. Changing and modifying threshold voltage value gives

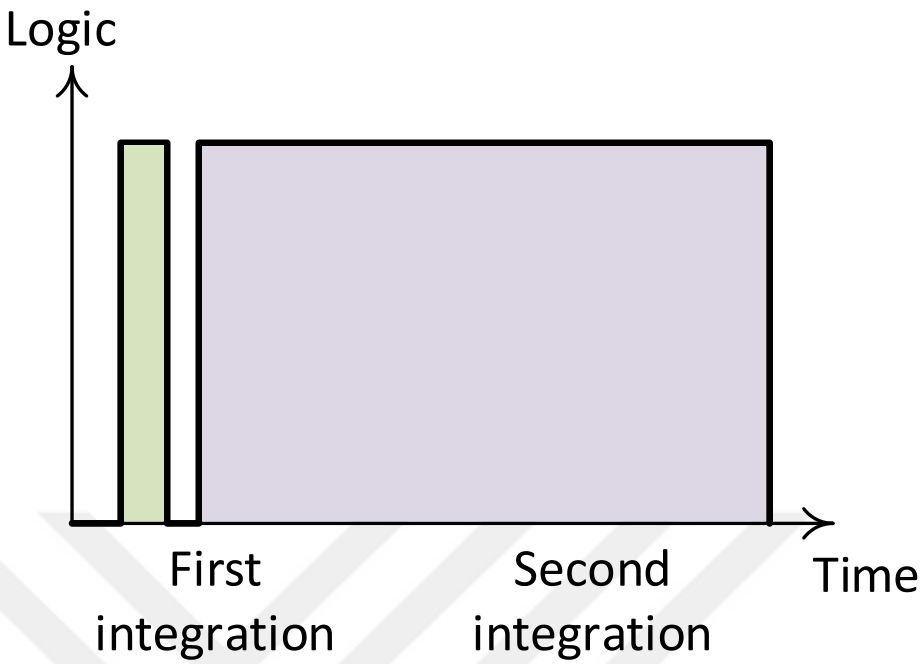


Figure 22: Two step integration. First integration is for detecting light level second one is actual integration of light.

flexibility to user favoring which amplifier to use mostly. For further improvement and flexibility hysteresis may be added to decision mechanism but this makes pixel structure complicated.

There are a couple of intuitive features and practicalities that come with smart pixel architecture. One of them is the flexibility of using dual-band detectors because two different input stages are already presented. Most of the dual-band detectors have single bonding area which makes it compatible with this architecture. Another extra feature is to be able to select one of the input amplifiers for whole FPA instead of automatic selection. That manual selection provides some power consumption if a user continuously observes very dark or bright objects. Block level architecture of smart pixel is presented in Fig 23.

Highlights from smart pixel architecture:

- There are two input amplifiers inside the pixel. One is optimized for low illumination levels; another one is optimized for high light levels.

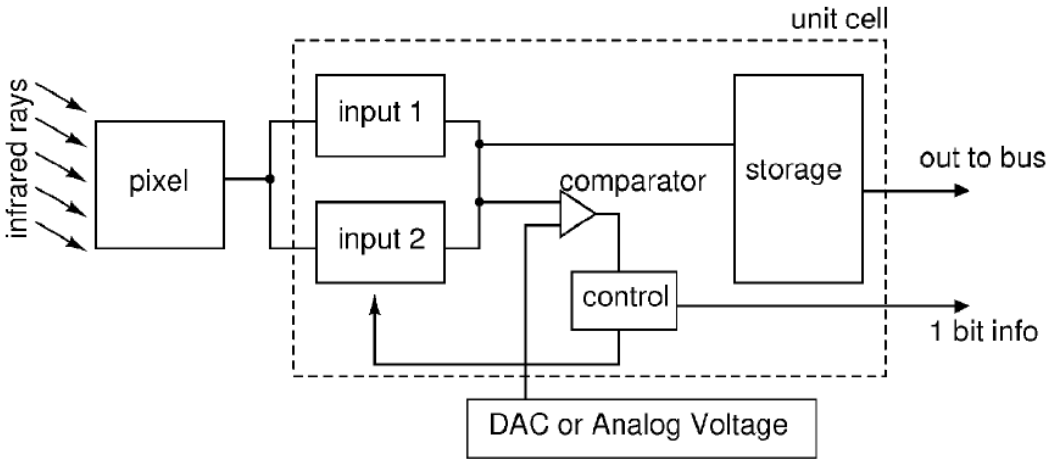


Figure 23: Detailed block diagram of the smart pixel.

- Smart control unit selects best input amplifier according to light level. This mechanism is located inside each pixel.
- Decision mechanism of the smart control unit is based on two-level integration. First integration is very short, and voltage accumulated during this integration will be used to determine best input amplifier.
- Threshold level of decision mechanism is controlled outside with some voltage level.
- Since optimum input amplifier is selected for each frame; best SNR value is achieved for FPA.
- 1-bit digital information also provided by pixel for post processing such as non-uniformity correction.
- User has flexibility between the automatic or manual selection of input amplifiers for pixels. Manuel mode selects amplifier for whole ROIC.
- Since it has two input amplifiers pixel is compatible with dual-band detectors by design.

This whole smart pixel architecture applies to wide range NIR-SWIR detectors. It helps to extend the dynamic range of near visible (NIR) and shortwave infrared (SWIR) image sensors by improving SNR value. This band has a broad range of

photocurrent output. This topology is also compatible with other combinations from all infrared spectrum from NIR to LWIR.

2.3 High Dynamic Range Imaging

Human eye discriminates around 10 million colors. Today's modern monitors are features 24 bit RGB color (True Color). 24-bit means that each color (Red, Green, and Blue) is represented with 2^8 different tones(shades). Total of 2^{24} or 16,777,216 color variations are possible [36]. There is also 32-bit color standard which uses different color space RGBA. "A" in the RGBA stands for alpha which contains transparency information. Thus, each color of 32-bit color space has again represented with 8-bit shades.

The deep color format supports 30/36/48 bits, and per channel represented more than 8 bits, as 10/12/16 respectively. Video cards support deep color formats. Also, imaging software's can handle deep color images. Hardware support is very limited. Only some professional monitors support 30-bit color (1.07 billion). Thus, it is fair to ask why we need more bits or high dynamic range when the hardware is limited to display images and videos. Even human eye cannot distinguish that much wide color space.

For infrared imaging systems, color space is limited to a single color. In term of SWIR, all images and videos are grayscale. Human eye barely differentiates between 8-bit and 10-bit grayscale images. It may not matter for the human eye and vision; it matters from image processing perspective.

Professional DSLR cameras, mobile phone cameras and infrared imaging systems processes and works more than 8-bit information for each channel. Processing with only 8 bit of data causes loss of information and artifacts on an image. This is the reason why we need more than 8-bit color. For instance, mobile phone's camera outputs at least 10-12 bit image. Many color enhancement algorithms applied on a picture by processor chip. After all, processing is done, the image is converted into 8-bit. First of all, 8-bit image or video save a lot of disk space. All popular compressed image and video formats support 8-bit per channel [37]. Moreover, 8-bit hardware display support is cheap and everywhere. Finally, human eye OK with 8-bit images.

Figure 24: NUC corrected and HDR image examples [38].

Regarding HDR infrared imaging, the question is the same; why we need 90

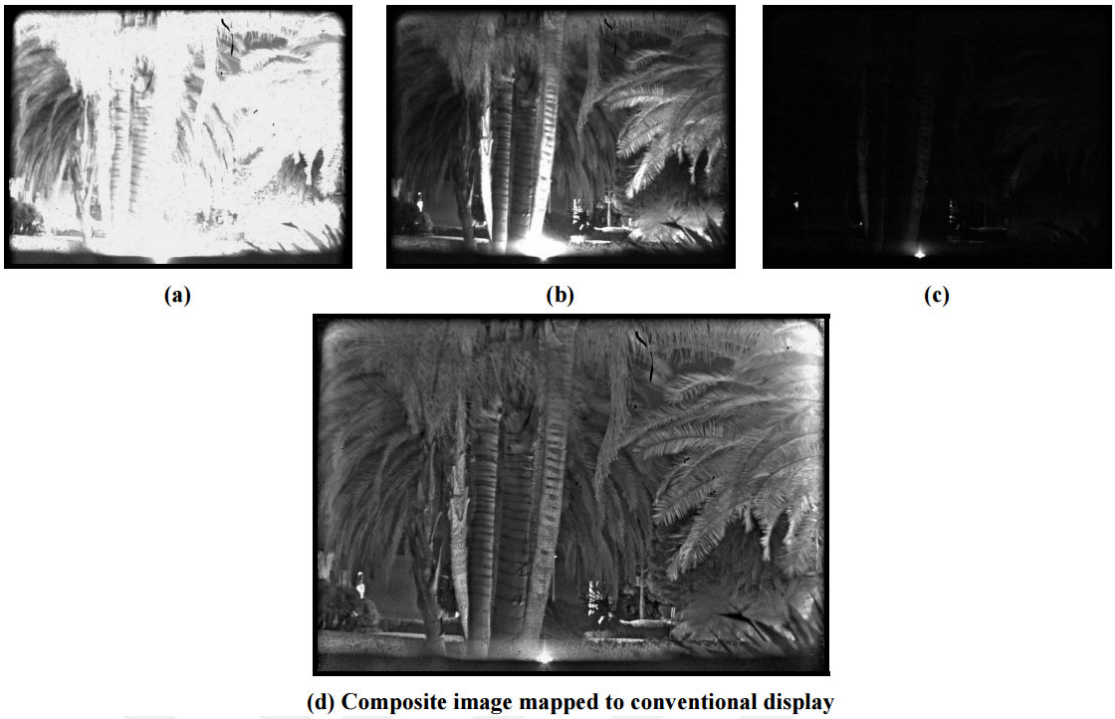


Figure 25: HDR imaging with different gain settings and final image [30].

dB or more dynamic range when we are not able to see it. We can only see 8 bit. Also, the answer is same; we need it for post processing. A human cannot see, but bits and voltage levels are there. It is the matter of post processing. 24 compares non-uniformity corrected normalized image and HDR image. Only NUC corrected image looks so flat details are not visible. Without post processing raw output of image sensors are not usable.

HDR post-processing enables to create 8 bit or max 10-bit images/videos that contain more visible areas. For instance, let's assume that we have a 14-bit grayscale image. There are some dark and almost saturated areas in the picture. The image looks normal to human eye. When we look at the pixels, we have information regarding dark and bright zones. High dynamic range image processing collects these information and highlights them by combining into a single 8-bit image.

The following example explains high dynamic range image processing in simple manner. Fig. 25 presents same scene with different gain settings in a), b), and c). a) contains information regarding dark zones. b) is medium gain image and c) has details about bright zones. Finally d) is the combination of all three different gain mode. Fig. 25 d) includes details and information from all three modes. Branches are more visible and light does not saturate the palm tree. Finally, there are not

much dark zones in the photo.

3 Smart Pixel Implementation

Up to now, history of infrared detectors and infrared imaging systems are touched on. Also readout integrated systems for infrared detectors are discussed with popular preamplifier structures. In this section, implementation of the prototype ROIC which includes smart pixel architecture will be discussed along with other peripheral circuits. Detailed analysis of smart pixel architecture will be provided.

3.1 32x32 Prototype

A 32x32 ROIC prototype with smart pixels is designed and fabricated using 0.18μm XFAB technology. Architecture of ROIC is represented in Fig. 26. The ROIC includes array, current sources, digital control circuit, multiplexer and output

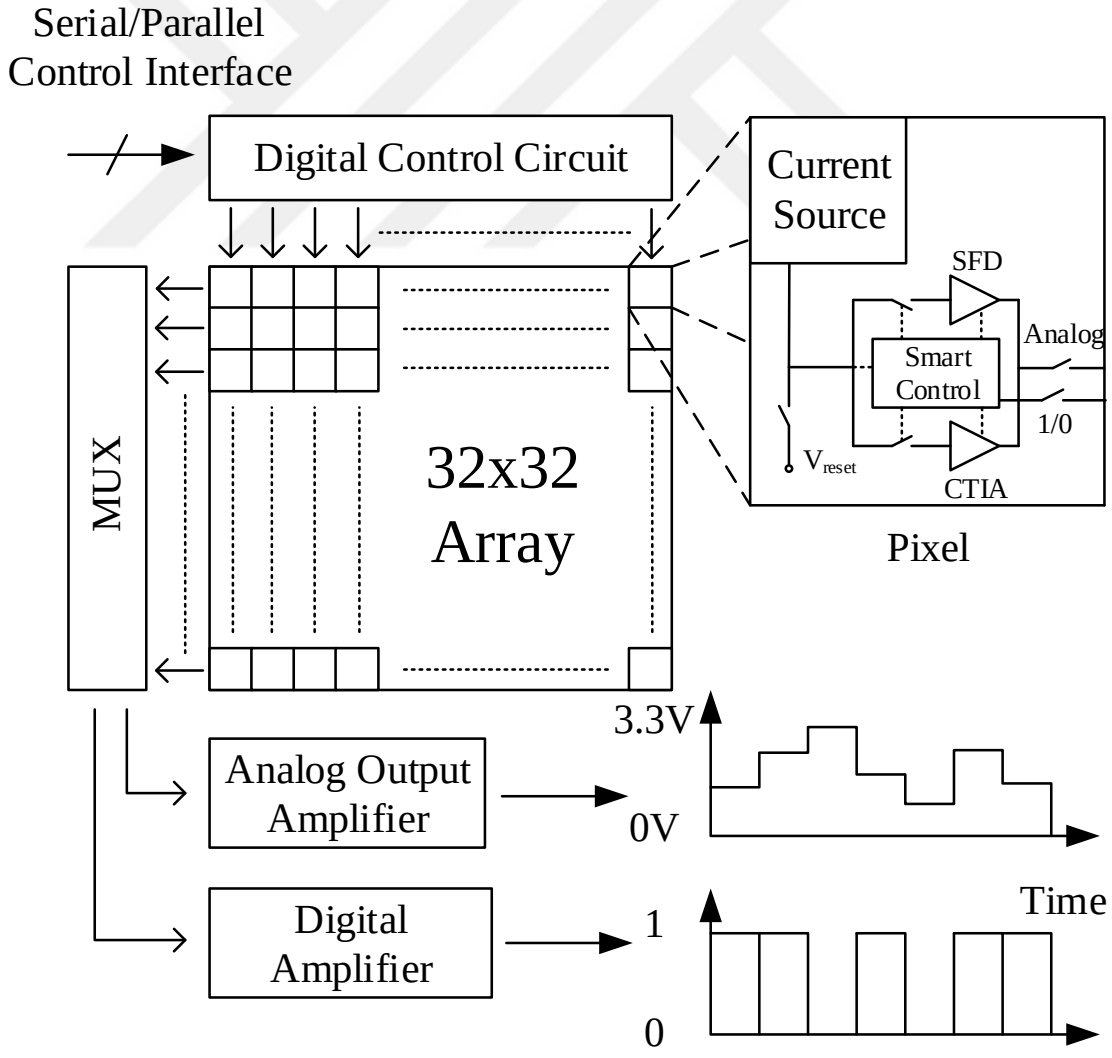


Figure 26: Block diagram of 32x32 Smart ROIC.

amplifier. Except smart pixel overall architecture is similar to other analog ROICs.

In this chip, current sources are used instead of infrared detector. Designed current source is compensated to process and mismatch variations and capable of providing current from 10pA to 3nA. Its architecture is based on [39], in order to reduce footprint of current source some optimizations are performed such as getting rid of temperature optimization part. Unlike a detector, the current sources are not hybridized to the ROIC chip, thus the detector bonding area inside the pixel is utilized for the current sources.

Along with regular analog output there is also a 1 bit digital output per pixel which comes from pixels. That 1 bit digital information indicates active amplifier. That is particularly useful.

Digital control circuit provides reset, two level integration and output signals for pixels. It is serial and parallel programmable. Parallel programming allows to set pre-defined timings for integration times. Two level integration time is fully controllable via parallel and serial interface. Control circuit is designed at RTL level. Layout of the prototype is shown in Fig. 27. Array, control circuit and output buffer are tagged on Figure. Core area is 800 x 880 μm^2 which excludes output buffer. Area is pad dominated because final tapeout includes one more chip. Total multi project wafer (MPW) area is utilized.

3.1.1 Circuit Design Analysis

In proposed circuit design of the SWIR smart pixel, CTIA and SFD input amplifiers are selected. In general, ROIC with CTIA amplifier is used for SWIR detectors [18]. Considering very good handling of ultra low currents, high injection efficiency and linear conversion characteristics make the choice of CTIA inevitable [40]. As mentined in previous chapter CTIA consists of an inverting amplifier, integration capacitance and reset transistor which is in parallel with integration capacitance.

Integration capacitance of CTIA can be made very small unlike other topologies, because output of the unitcell is connected to amplifier output which is a low impedance node. This yields to perfect low noise performance [41].

Input referred noise of CTIA is given by:

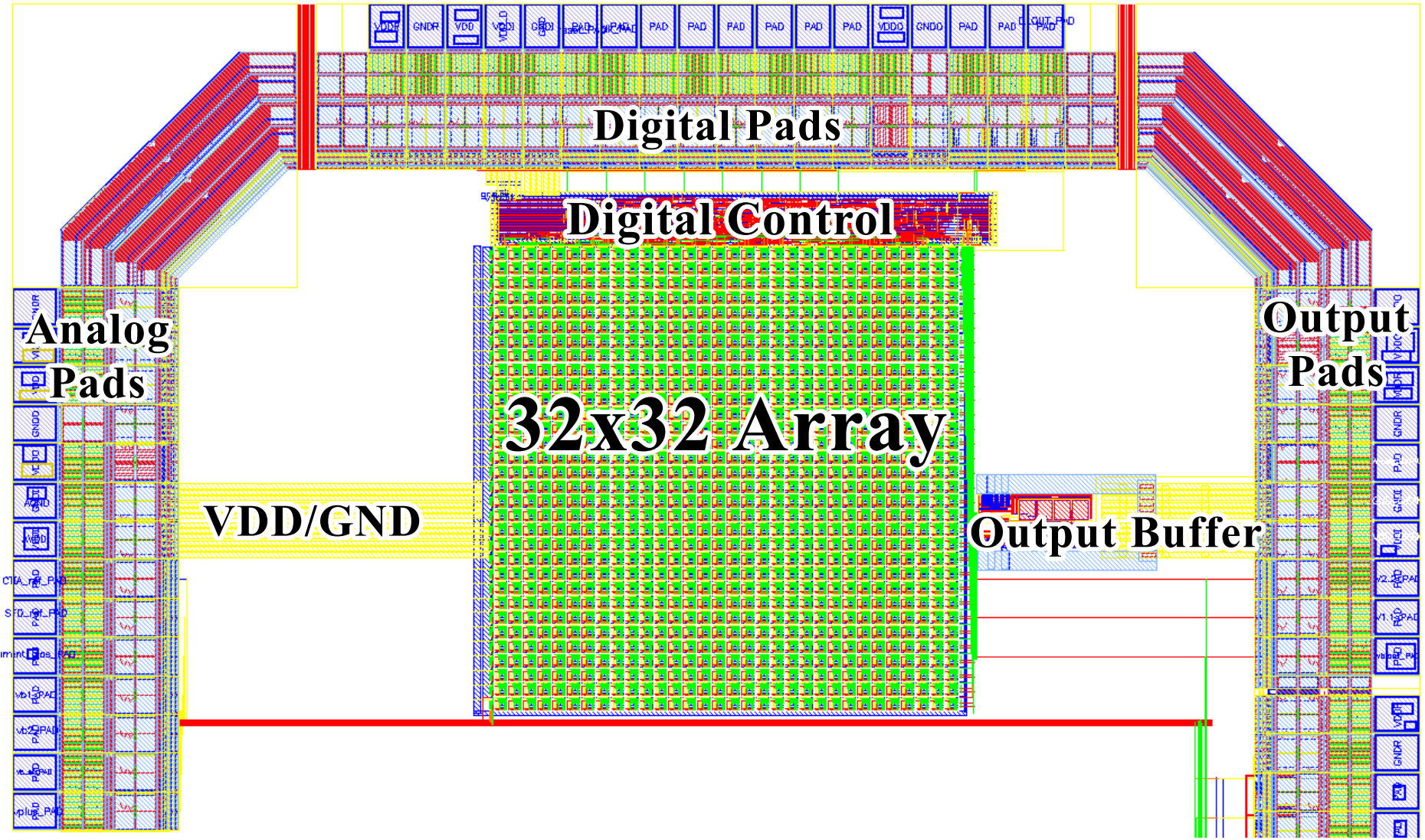


Figure 27: Layout of 32x32 Smart ROIC.

$$N_{white}^2 = \frac{kT}{q^2}\left[\left(\frac{2T_{int}}{R_o}\right) + \left(\frac{C_{int}+C_d}{C_L + \frac{C_{int}C_d}{C_{int}+C_d}}\right)\left(C_{int} + \frac{C_{int}+C_d}{A_{vo}}\right)\right] \tag{14}$$

$$N_{1/f}^2 = \frac{2T_{int}^2}{q^2}\left[S_{fd} ln\left(\frac{1}{\pi f_{sat} T_{int}}\right) + \left(\frac{f_s}{f_a}\right)^2 S_{fa}\left(\frac{C_{int} + \frac{C_{int}+C_d}{A_{vo}}}{C_L + \frac{C_{int}C_d}{C_{int}+C_d}}\right)^2 ln\left(\frac{11.8 f_a}{f_s}\right)\right] \tag{15}$$

kTC noise contributions in the formula can be eliminated with CDS. The input-referred noise can be made small by choosing the integration capacitance small. Also, increasing the load capacitance reduces the noise bandwidth.

For a typical detector which has 2 pF detector capacitance and around 50 MΩ resistance, white noise is calculated as 85 e^-. 6 fF C_{int} and 70 dB amplifier gain is used to achieve this calculation. CDS is required suppress kTC contribution. Depending on detector type effectiveness of CDS, less than 10 e^- is a typical target value.

Source follower per detector consists of integration capacitance, reset transistor and source follower transistor. Integration capacitance can be calculated by adding integration capacitance and source follower input capacitance. While signal is integrated on to the capacitance, the detector bias changes since the signal is integrated directly on the same node as the detector unlike CTIA which keeps detector voltage constant [41].

The main source of white noise in the SFD is the source-follower transistor itself. Additionally, SFD is very susceptible to flicker noise [40].

Input-referred white noise electrons is given by:

$$N_{white}^2 = \frac{kT}{q^2}\left[\frac{C_{int}}{C_L}C_{int} + \frac{2T_{int}}{R_O}\right] \tag{16}$$

in which for a detector with 2 pF capacitance and 50 MΩ impedance 250 e^- noise is calculated for a 10 μs integration time. less than 500 e^- noise is reasonable value for a big integration capacitance in literature.

CTIA and SFD are used in the SWIR smart pixel design which they respectively cover low and high illumination levels. Choice of CTIA for low illumination level is based on its handling of very low currents and its noise performance with

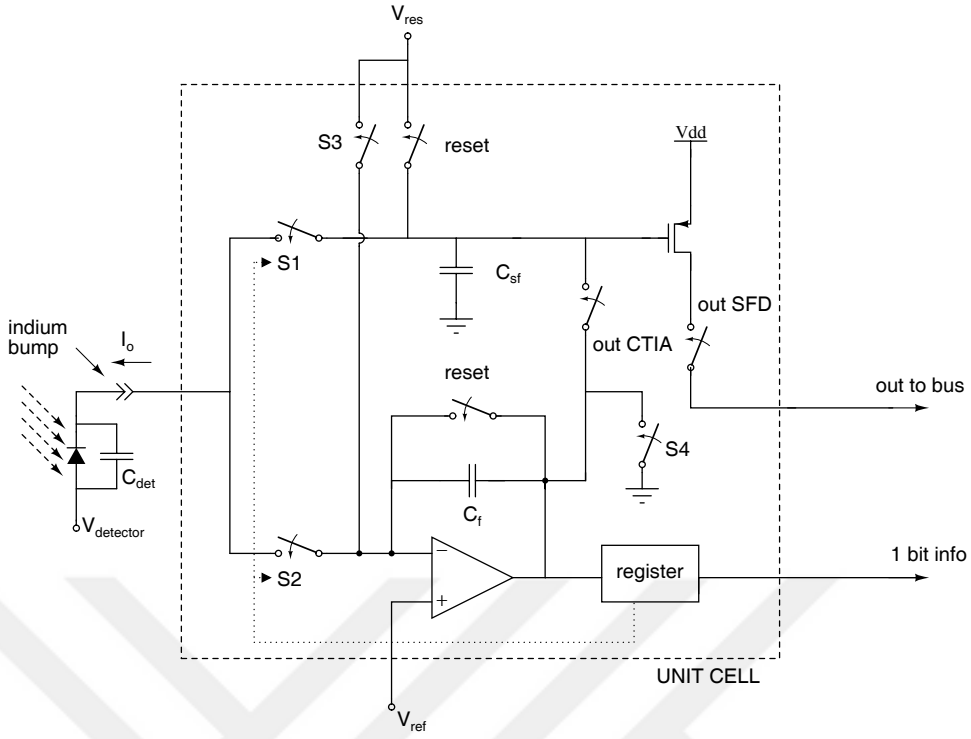


Figure 28: Schematic of the SWIR smart pixel.

very small integration capacitance. Small integration capacitance is not allow much charge handling capacity. Thus, for high illumination levels SFD with relatively big integration capacitance is used. SFD also promises low noise and good performance for SWIR.

Fig. 28 presents schematic of the smart pixel. It consists of CTIA, SFD and smart control register. In this structure, CTIA amplifier is designed as differential instead of common source structure which is commonly used as CTIA. This differential structure provides extra feature that CTIA can be used as a comparator.

Working principle of light detection mechanism is based on two level integration which is mentioned previously. Smart register activates CTIA in the first integration. Then, CTIA starts to work as a comparator and compare integrated charge with V_{ref} which is user defined voltage level for determining light level. If integrated charge exceeds threshold level comparator activates SFD for actual integration, otherwise CTIA will continue for integration. S1 and S2 switches determine SFD or CTIA being used. At the end of integration register provides a 1 bit information regarding selected amplifier; logic 0 for CTIA and logic 1 for SFD. All digital timings are

controlled by digital control circuit. Register only switches appropriate amplifier according to comparator data.

Remarks from smart pixel circuit:

- There are two input amplifiers inside pixel; CTIA and SFD.
- CTIA covers low illumination levels and SFD is optimized high illumination levels.
- CTIA is used as a comparator in the manner that a space saving implementation amplifier is adopted.
- V_{ref} threshold level for light detection is controlled by user.
- Smart register selects best amplifier according to illumination level.
- 1 bit digital information also provided by register for post processing such as non-uniformity correction.
- User has flexibility between automatic or manual selection of input amplifiers for pixels. Manuel mode selects amplifier for whole ROIC.
- Since it has two input amplifiers pixel is compatible with dual band detectors by design.

3.2 Pixel

CTIA is low illumination optimized amplifier of the smart pixel. It is shown in Fig 29 and designed as cascode differential amplifier in order to be used as comparator. Double usage of CTIA saves inside pixel.

Cascode structure also provides more gain which helps to reduce input referred noise 14. More than 70 dB gain is achieved by the amplifier. High gain is also useful for improving comparator accuracy.

C_{int} chosen as minimum in order to obtain minimum input referred noise and maximum SNR. Minimum drawable capacitance is 6 fF in this technology. Detailed noise calculations are made in previous section. Layout of the CTIA is can be seen in Fig. 30. Area of CTIA is 19x11 μm^2. Fig. 30 also represents full pixel layout which

is 22.5 x 22.5 μm^2. SFD is composed of a single transistors. Integration capacitance is chosen as 40 fF to cover high illumination levels. Detailed noise calculations made in previous section. W/L=2/0.5 μm ratio of SFD is optimized for maximum linerity.

As observed from pixel layout in Fig. 30 smart control takes a lot of space. Hearth of the smart control is high active transparant D-latch with reset. Area of D-latch is 37.66 μm^2. Truth table of D-latch is represented in Table 4. D is connected to output of G is used to keep data during integration and read cycles. Output of D-latch control S1 and S2 switches. Only one of them is active in any cycle.

3.3 Current Source

The purpose using current source is to replace detector. Current source is placed inside detector bonding area of a smart pixel. Most general practice to design a cur-

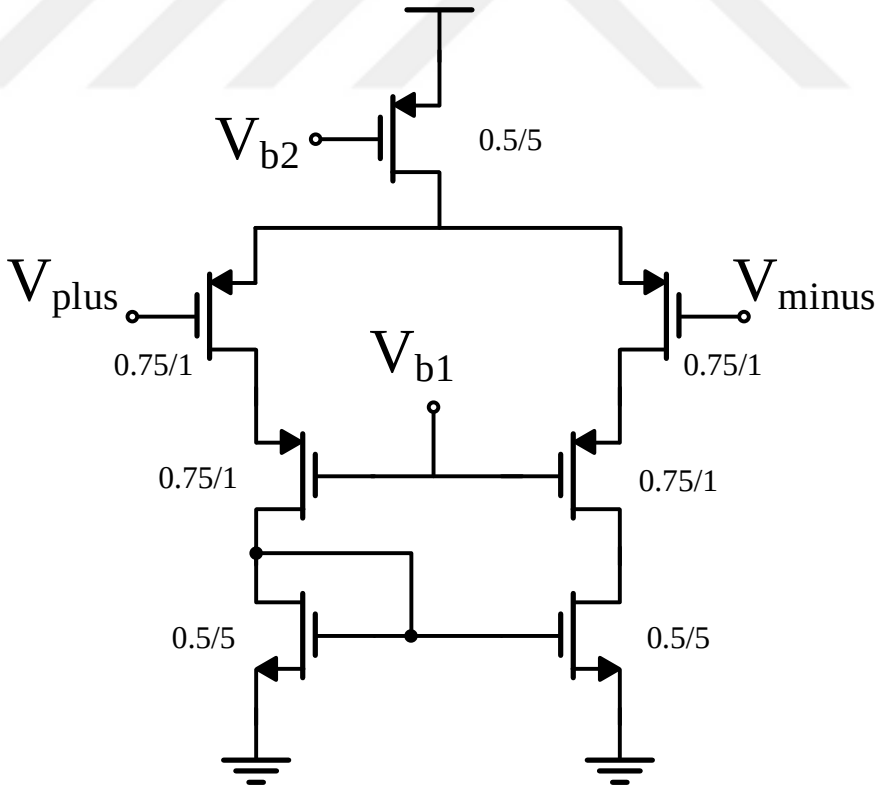


Figure 29: Schematic of the CTIA.

Table 4: Truth table of the D-latch.

RN	D	G	Q	QN
L	X	X	L	H
H	L	H	L	H
H	H	H	H	L
H	X	L	Q	QN

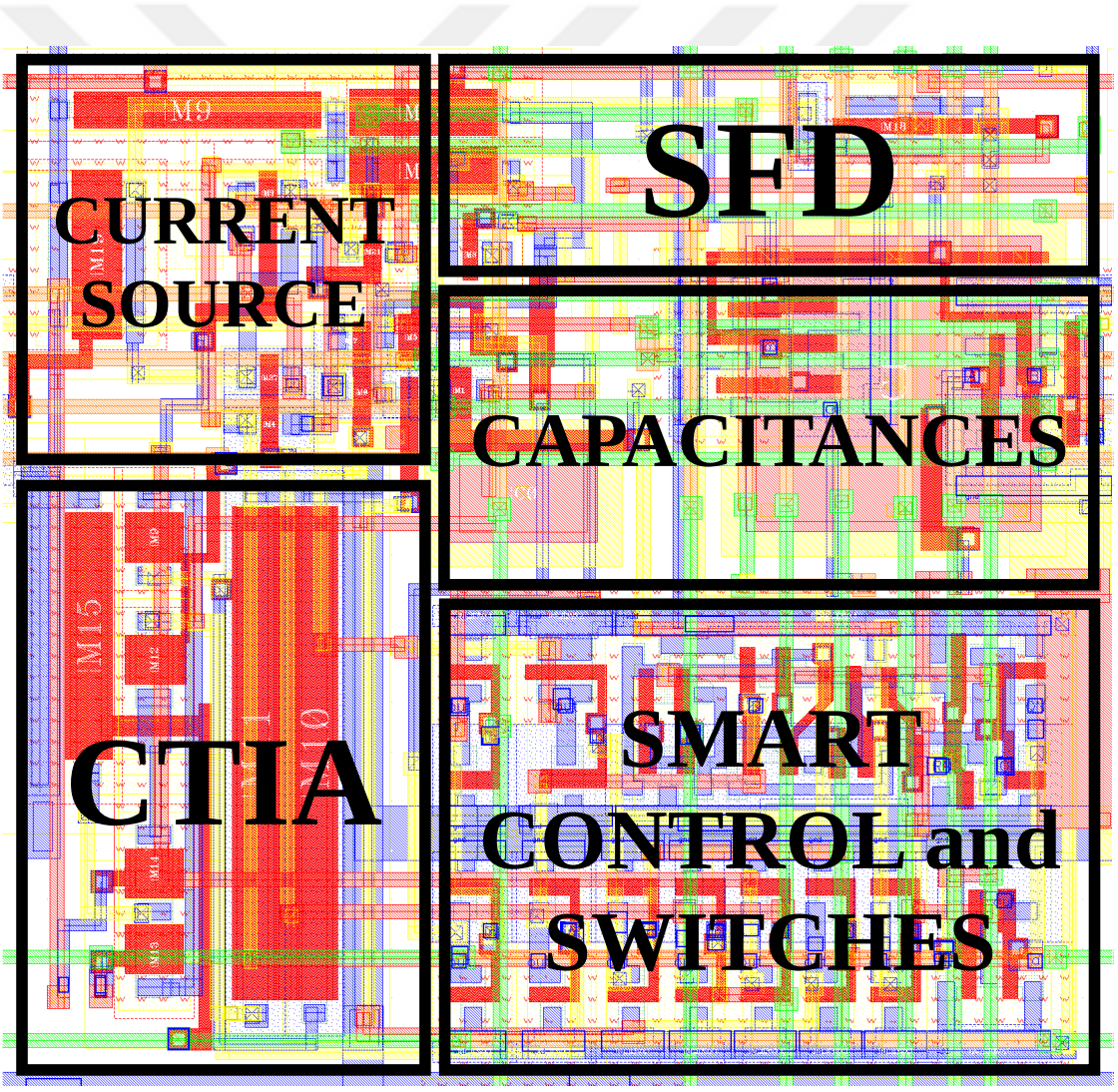


Figure 30: Layout of the pixel.

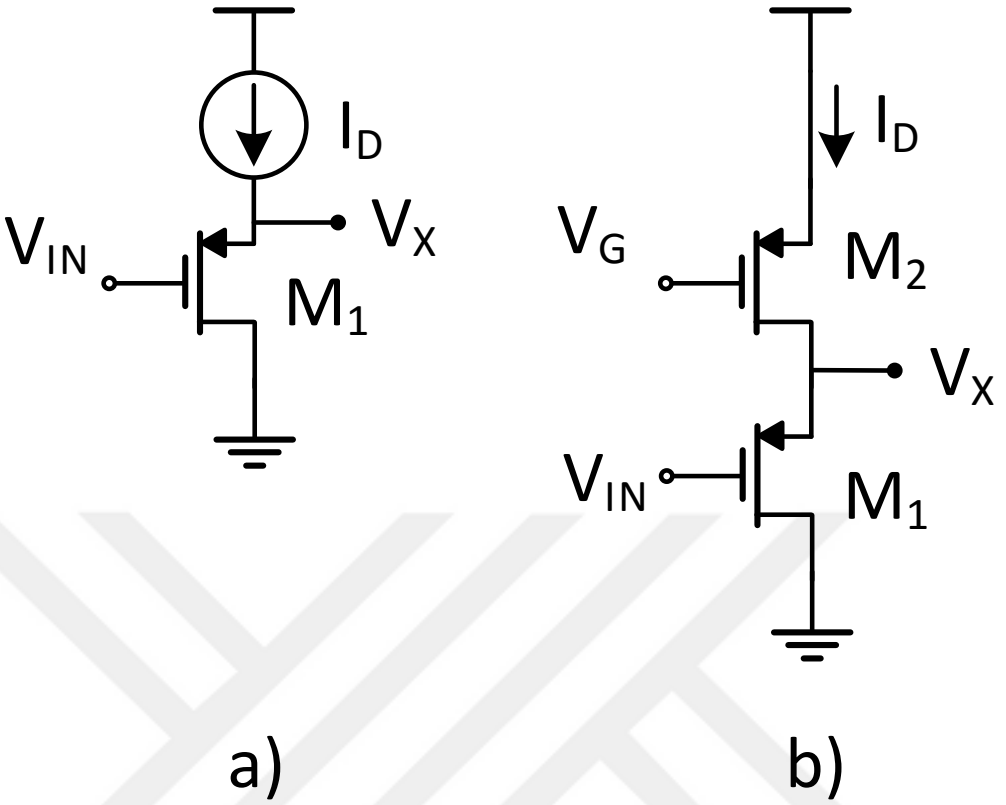


Figure 31: Constant current source circuit.

rent source is using single MOS transistor with a bias voltage. Considering current equation of MOS devices; oxide capacitance, mobility and threshold significantly affect current value. Due to variation of these parameters mismatch and process variations may occur. That simple constant current source structure can be seen in Fig. 31a.

In Fig. 31b modified version of constant current source is shown. In this circuit, M_2 helps to reduce temperature variations compared to first version. But, M_1 is still vulnerable to threshold changes. V_X node can vary according to mismatches. If we make V_X node constant we can achieve process and mismatch tolerant current sources.

Circuit in Fig. 32 V_X is used to bias M_3's gate, then M_3 will have a drain current independent of the threshold changes. Uncompensated current references

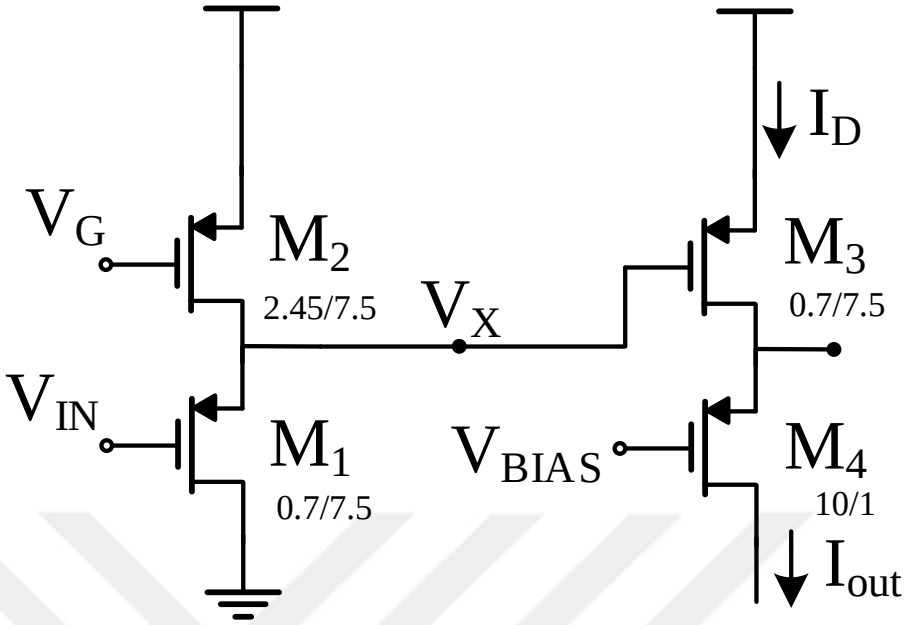


Figure 32: Process and mismatch compensated current source circuit.

may deviate more than 100 %; however designed current source can provide 12 % mismatch and process variation. Monte Carlo analysis of the circuit for 1 nA current is shown in Fig. 33.

3.4 Output Amplifier

Output amplifier is very crucial for analog readouts. It should provide wide output dynamic range, slew rate and enough bandwidth for analog output. In order to achieve those specifications, folded cascode opamp with rail to rail input and output stage is implemented. Schematic of the opamp is provided in Fig. 34

GBW calculations includes gm of the differential pairs and compensation capacitance which is also related with load capacitance (generally one third or half of the output capacitance).

$$GBW = \frac{gm_1 + gm_3}{2\pi C_c} \tag{17}$$

In order to have a stable amplifier current through output stage is important.

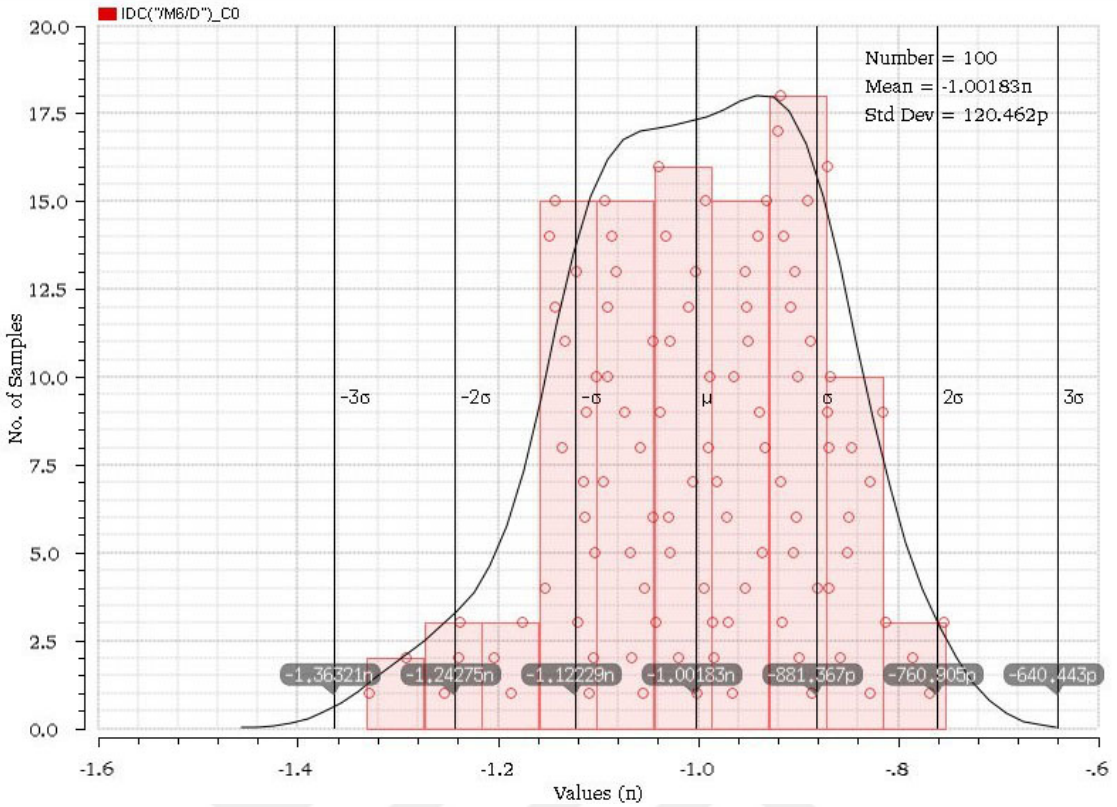


Figure 33: Monte Carlo simulation result for 1 nA current.

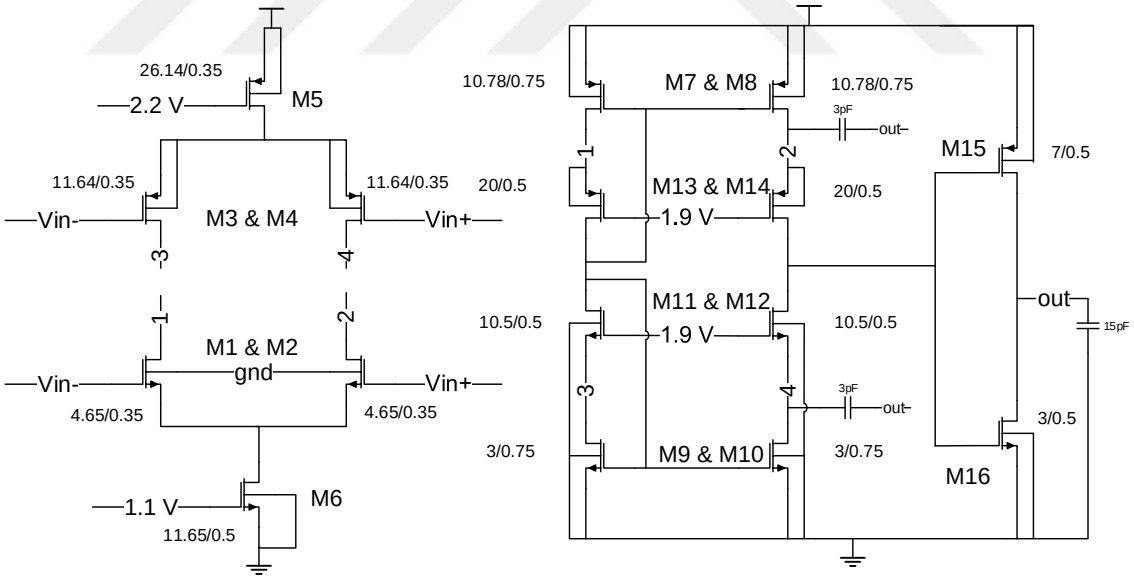


Figure 34: Process and mismatch compensated current source circuit.

For a phase margin around 60-70 degrees is desirable due to optimum between low ringing versus low settling time. To achieve this, nondominant pole at the output of the first stage should be around 3 GBW and this leads to the following equation;

$$gm_{16} \approx 2\pi C_L 4GBW \tag{18}$$

Since gm_{16} is determined, it is also possible to determine the current at the output for a given (V_{GS}–V_T).

$$gm = \frac{2I_{DS}}{(V_{GS} - V_T)} \tag{19}$$

For input and output transistors M_{1-4}, 0.2 V $V_{GS} - V_t$ is chosen because there is enough headroom and it is a good balance between large transistors and high gm/I ratio. In order to decrease output parasitic capacitance at the output of the first stage, high overdrive voltage is used. Length of the output transistors are also enlarged to increase the gain of the amplifier. Output stage is biased in Class AB mode to decrease the output current and increase the linearity at the output stage for large signals. Length of the current sources for the input pair is also implemented big to increase output impedance thus common mode rejection ratio (CMRR). Differential input transistors are implemented as large to decrease noise of the input pair which is the most crucial noise sources and to avoid mismatch between two input transistors which is the dominant reason for the offset.

Miller capacitance is divided into two and implemented both from NMOS cascode and PMOS cascode to introduce symmetry and also to get rid of one very big capacitor. Current at the cascode transistors is half of the current at the input pairs to decrease further the output impedance without sacrificing from gm of the input pair. The ratio is not increased further since the difference in size between the cascode transistors and input pair would result an unsymmetrical layout.

Once gm_{16} and gm_1 is determined, it is possible to determine the length of the transistors at the output of the first stage and at the second stage from gain formula. If they are assumed to be equal length for a better layout beside $r_{out12} = r_{out14}$ and $r_{out15} = r_{out16}$ are assumed then;

$$A_v = 2gm_1 gm_{16}(r_{out12}//r_{out14})(r_{out16}//r_{out15}) \tag{20}$$

$$r_{out} = \frac{LV_E}{I_{DS}} \tag{21}$$

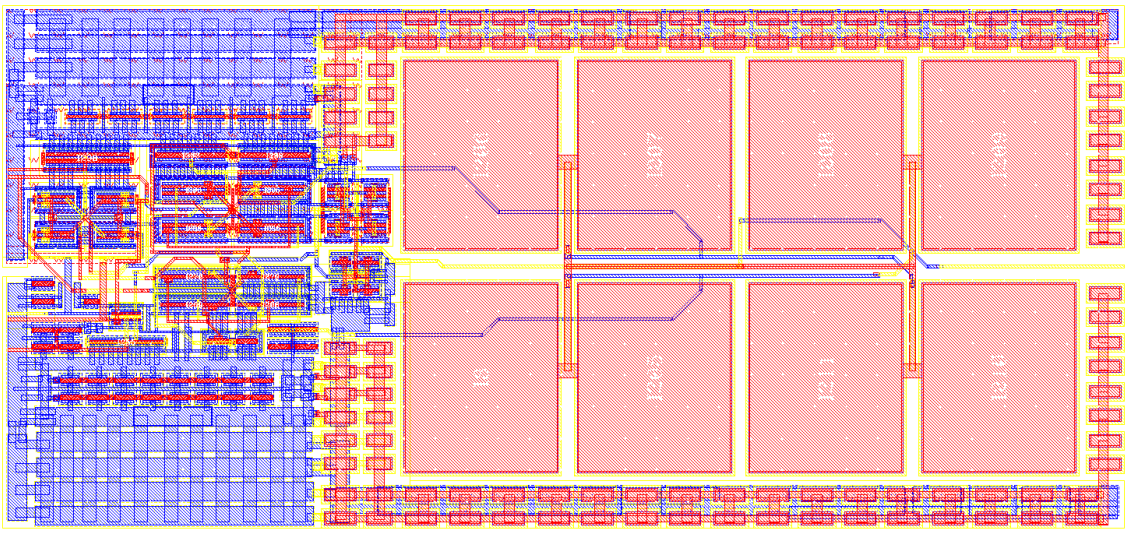


Figure 35: Layout of the opamp.

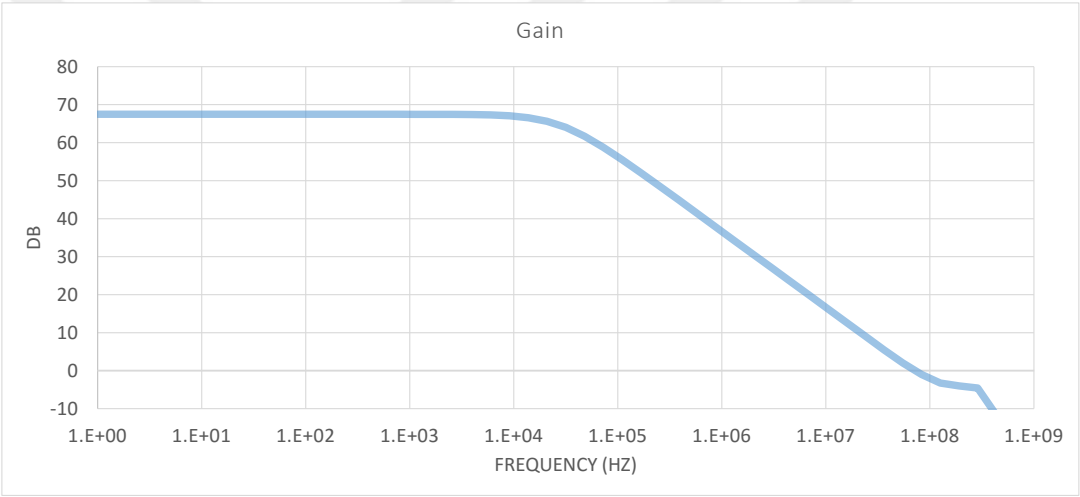


Figure 36: Gain of the opamp (67.6 dB).

Using equation in 20 72 dB gain is calculated for the rail-to-rail folded cascode opamp with class AB output stage. Total power consumption for the amplifier is below 2.5 mW which is acceptable for this amplifier with very high GBW specifications. After post layout optimizations gain and phase of the opamp are simulated as 67.6 dB and 68 degrees respectively. Fig. 36 shows post-layout simulation results of the gain. Layout of the opamp is shown in Fig 35. Core of the layout is designed as common centroid to improve matching and avoid process variations. Dummy transistors are used to improve matching and symmetry of differential pairs. Compensation capacitances located right side of the Fig. 35 as in eight pieces. Compensation capacitances surrounded by dummy capacitances. Dummy capacitances

improves matching of compensation capacitors.

4 Measurement Results

4.1 Measurement Setup

Measurements were performed using Keysight 16702B Logic Analyzer and MSO 9254A Digital Storage Oscilloscope. Logic Analyzer provides digital control and clock signals for the chip. The oscilloscope is used for sampling analog and digital data. PCB test card which includes low noise voltage references, coupling capacitances and switches are designed for ROIC. SMA connectors with shielded cables which protect from noise used for supply voltages. Fig. 37 shows two-layer PCB with the chip that is under the test. All measurements are done at room temperature (298 K).

Some of the tests performed using Pulse Instruments 7700 (PI 7700). PI 7700 has the capability of generating DC biases and clock signals. Also, it has data acquisition capabilities. It employs four 40 MHz 14 bit ADC for acquisition, up to 100 MHz clock drivers and 12 DC bias modules.

Table 5 represents all supply voltages that are required for the chip. These voltages are not directly connected to the chip. These are supply values of ultra low noise voltage references. The voltage references provide required supply values to chip. VDDO and VDDR are supplying for chip pads. VDDO provides power

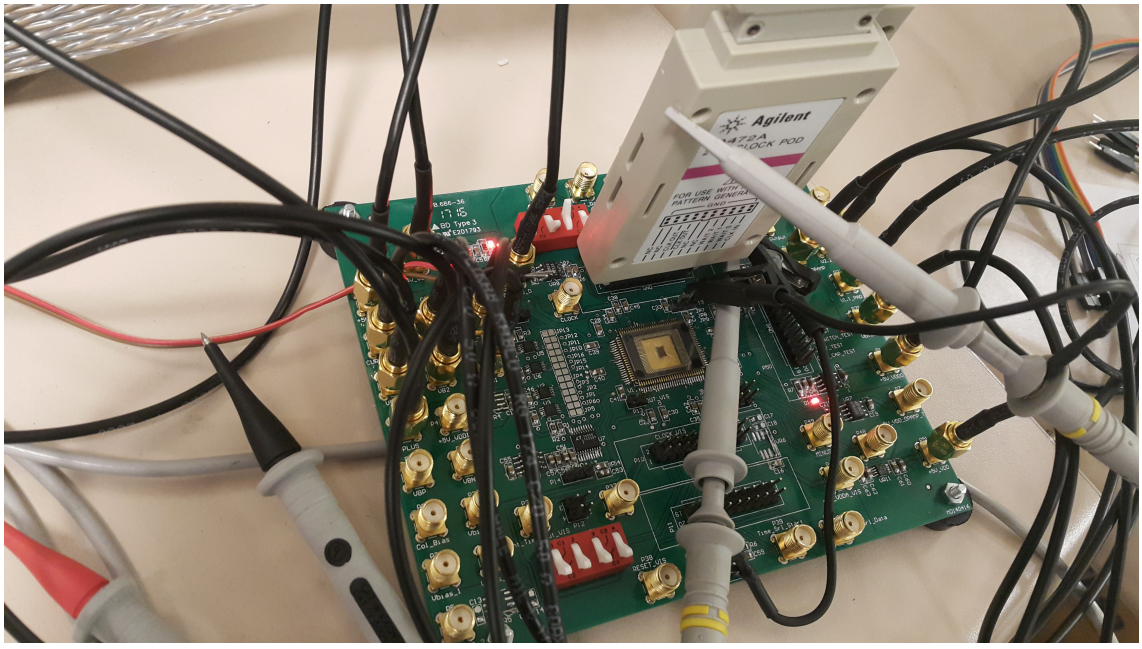


Figure 37: Test PCB of the final prototype

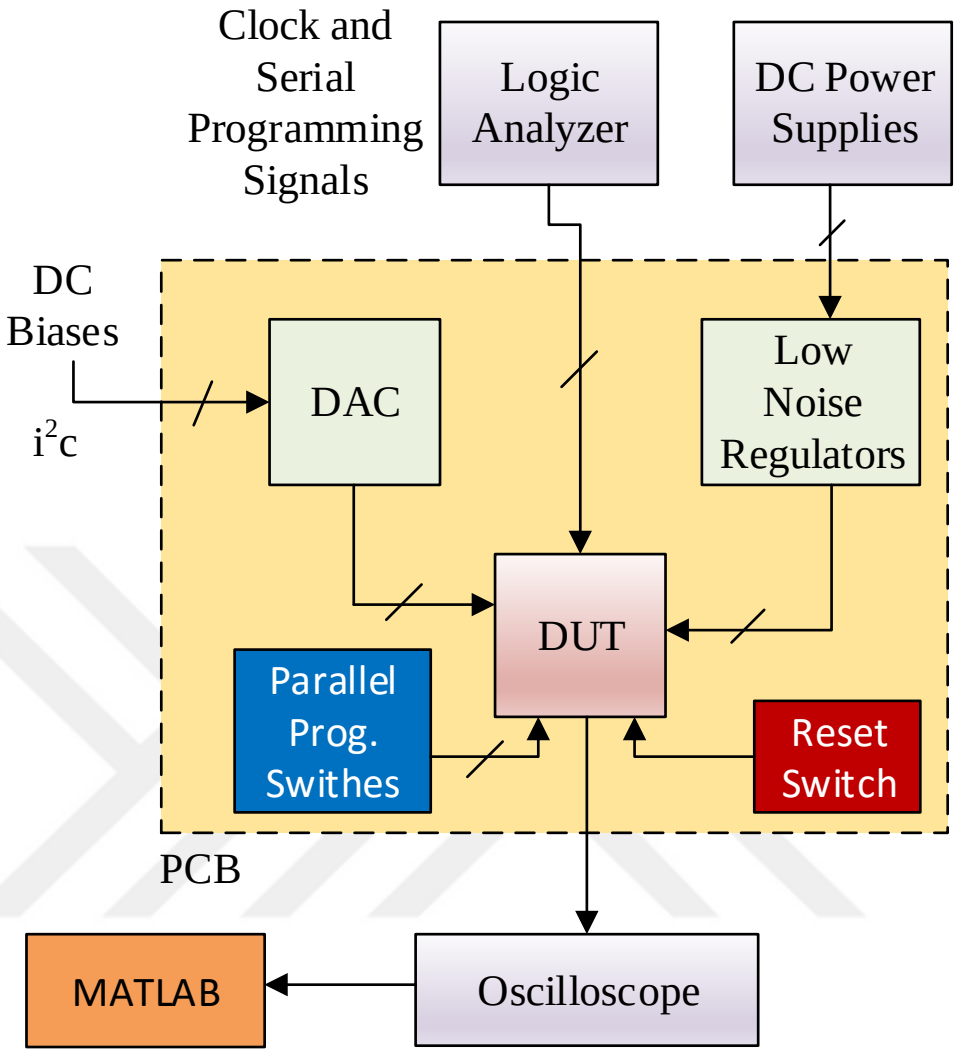


Figure 38: Block diagram of the DUT.

to output ESDs and digital output buffers. VDDR provides power to digital input buffers.

Table 6 lists bias voltages of the ROIC. Finally, Table 7 shows digital signals. Paralel programming bits show logic *1000* value that means serial programing is activated.

Fig. 38 is the block diagram of the measurement system. Low noise regulators provide supply voltages to DUT. DAC which outputs bias voltages is controlled by i2c interface. Digital signals are given by logic analyzer and on PCB switches. Analog and digital data acquisition performed using the oscilloscope. All oscilloscope data is processed using MATLAB.

Table 5: Supply voltages of PCB board and ROIC.

Component	Name	Value (V)
P1	5V_VDDO	5
P2	5V_VDDR	5
P3	5V_AVDD	5
P9	5V_VDD_D	5
P8	5V_VDD_OPAMP	5

Table 6: Bias values of the ROIC.

Component	Name	Value
P34	VPLUS	1
P35	VB_SF	2.6
P33	VB2	1.9
P32	VB1	1.25
P31	CURRENT_BIAS	2.86
P30	SFD_REF	0.5
P29	CTIA_REF	0.5
P26	V2.2_PAD	2.2
P27	V1.1_PAD	1.1
P28	VBIAS1	1.2

Table 7: Digital signals of the ROIC.

Component	Pin Number	Name	Logic
P17	20	Serial Start	1/0
	18	Serial Data	1/0
	16	RESET	1/0
P16	6	CLK	1/0
S2	5	Parallel_prog 0	1
	2	Parallel_prog 1	0
	8	Parallel_prog 2	0
	11	Parallel_prog 3	0

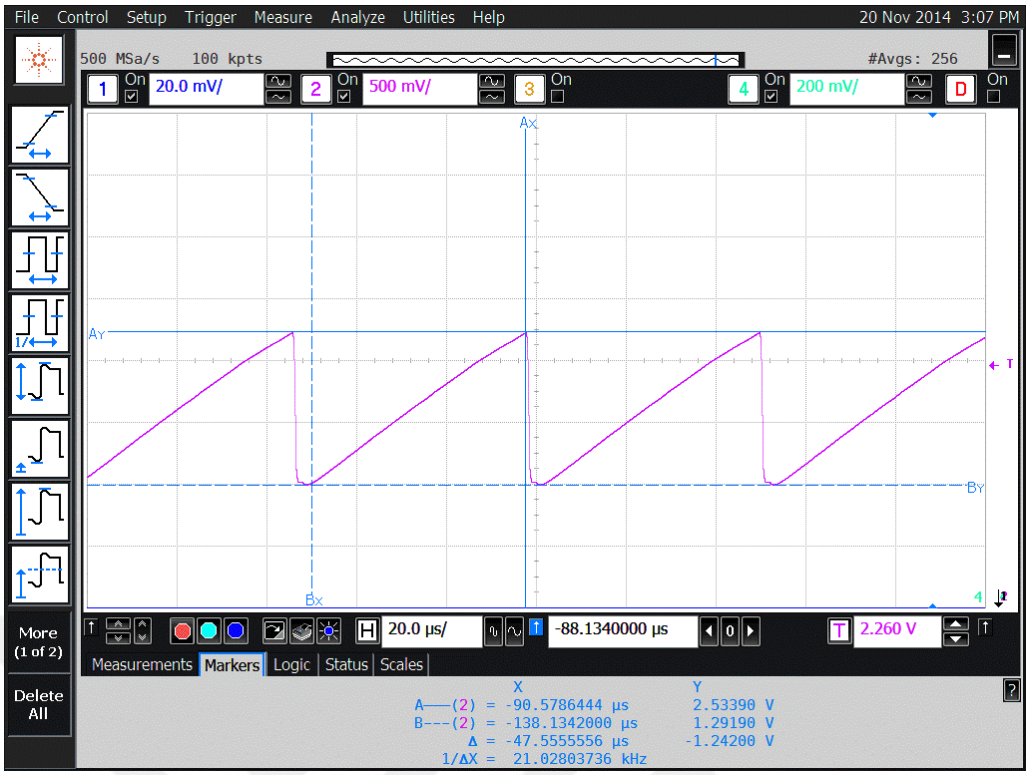


Figure 39: 50 μs integration time, 2.714V bias voltage, and 1.24V integrated charge.

4.2 Pixel Response

Since we do not have any detectors, all structures tested with current references. While changing the bias of the current source we can adjust integrated current.

Fig 39, 40 and 41 present measurement results from SFD input amplifier. 2.714 V bias voltage corresponds to approximately 1 nA current which is high current value for SWIR. 50 μs, 100 μs and 150 μs integration times applied to SFD amplifier which has 40 fF integration capacitance. In Fig 39 capacitance is not saturated after reset signal drops immediately. In Fig 40 and 41 ramp signal is saturated since integration time is long ramp.

The product of integration time and photocurrent equals capacitance times integrated voltage.

$$i_{photo}t_{int} = C_{int}\Delta V \tag{22}$$

in which we can calculate by using numbers in 39. It is found that $C_{int} = 40.3$ fF. The number is very close to what we found by simulations.

Fig 42 and 43 demonstrate response of CTIA amplifier. Unlike SFD, CTIA works

Figure 40: 100 μs integration time, 2.714V bias voltage, and 2.05V integrated charge.

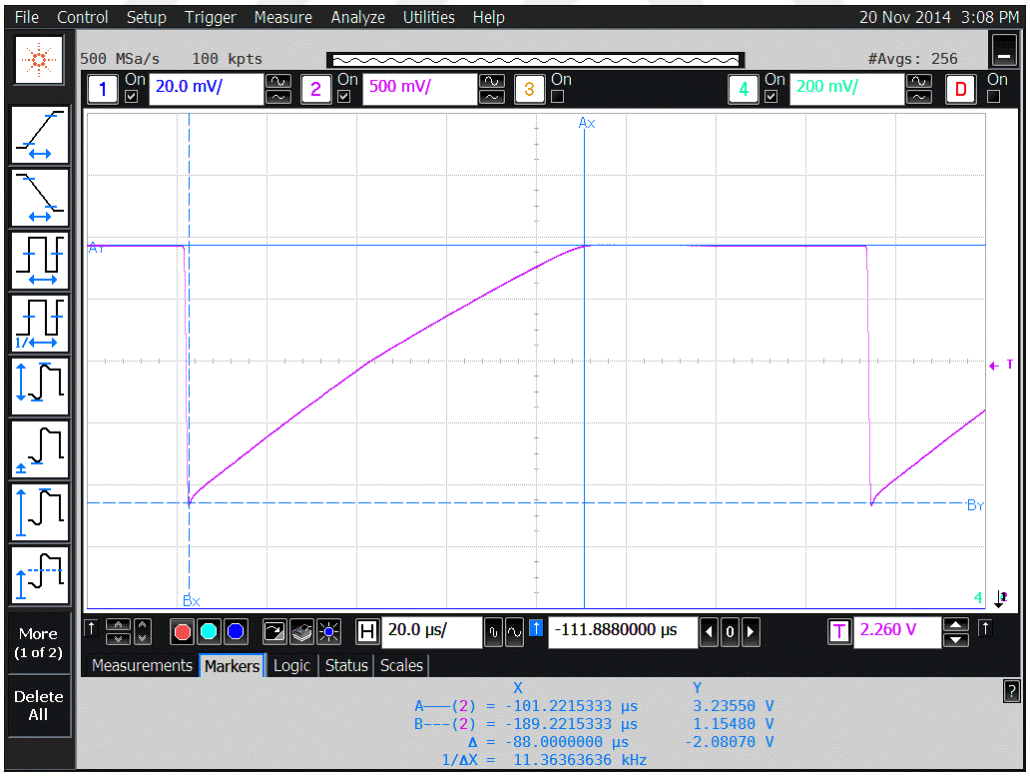


Figure 41: 50 μs integration time, 2.714 V bias voltage, and 2.05 V integrated charge.

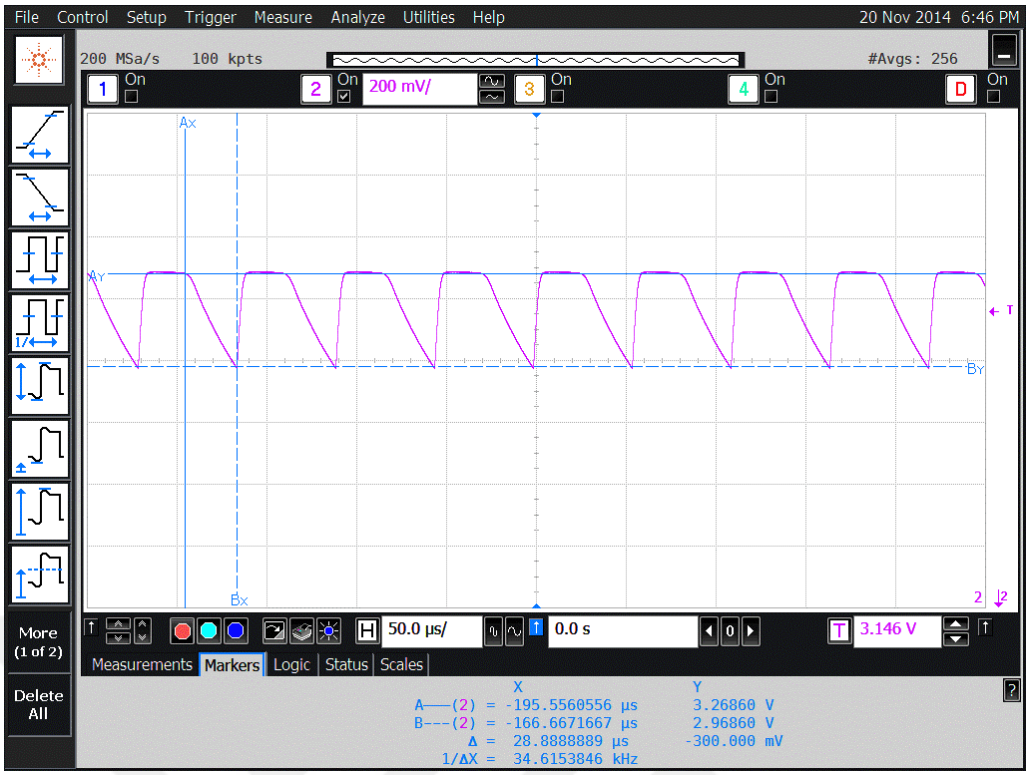


Figure 42: 30 μs integration time, 2.83 V bias voltage, and 300 mV integrated charge.

as sinking amplifier, thus ramp signals are downwards. Since CTIA is activated in low currents. In Fig. 42 2.83 V bias voltage corresponds to 70 pA current and 300 mV voltage is integrated. Using equation 22 integration capacitance of CTIA is calculated as 7 fF. That includes all parasitic capacitances at that node and integration capacitance. In Fig 42 and 43, same current level is integrated for different integration times. In Fig 42 ramp signal reaches to 2.53 V but with longer integration time ramp signal ramp signal in Fig 43 approaches to 2.96 V.

Fig. 44 and 45 shows linearity performances of SFD and CTIA amplifiers, respectively. SFD is perfectly linear with a regression rate of a 0.9999. CTIA has a linearity of 0.9844. A data point very close to saturation which causes a nonlinearity. Still, it has a reasonable and usable linearity value within the specifications.

4.3 Noise Measurement

In the beginning, reset noise is measured and subtracted to measure input referred noise for SFD and CTIA amplifiers. Since the architecture does not include CDS, subtraction is done manually with two measurements. MSO 9254A oscillo-

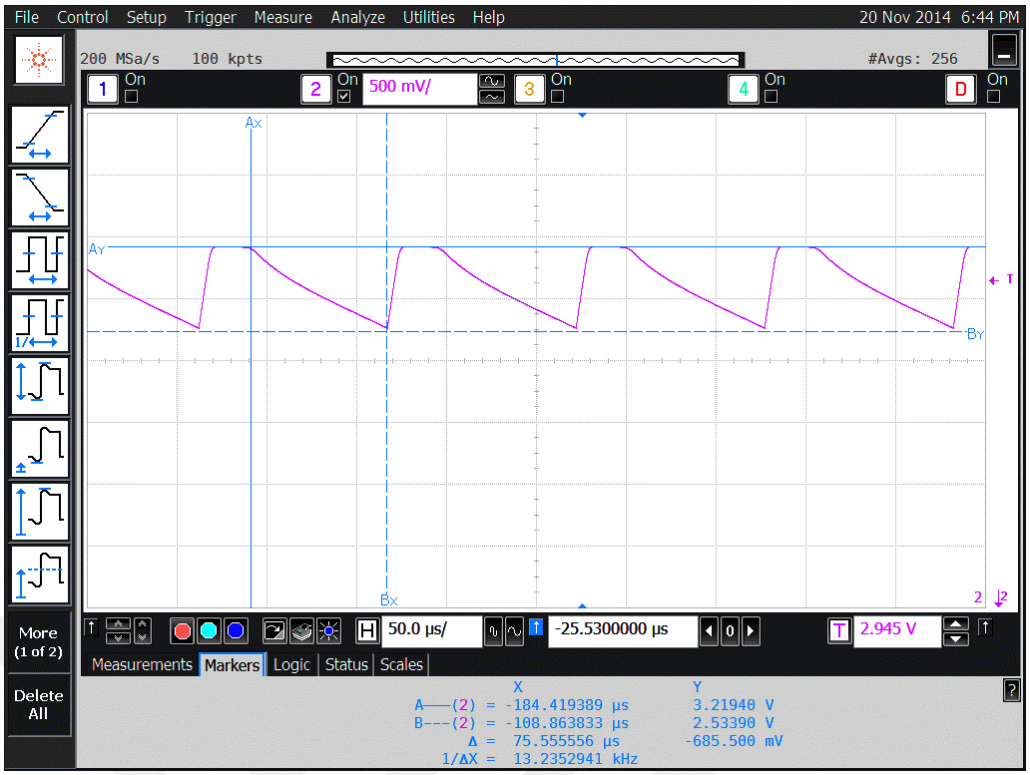


Figure 43: 75 μs integration time, 2.83 V bias voltage, and 685.5 mV integrated charge.

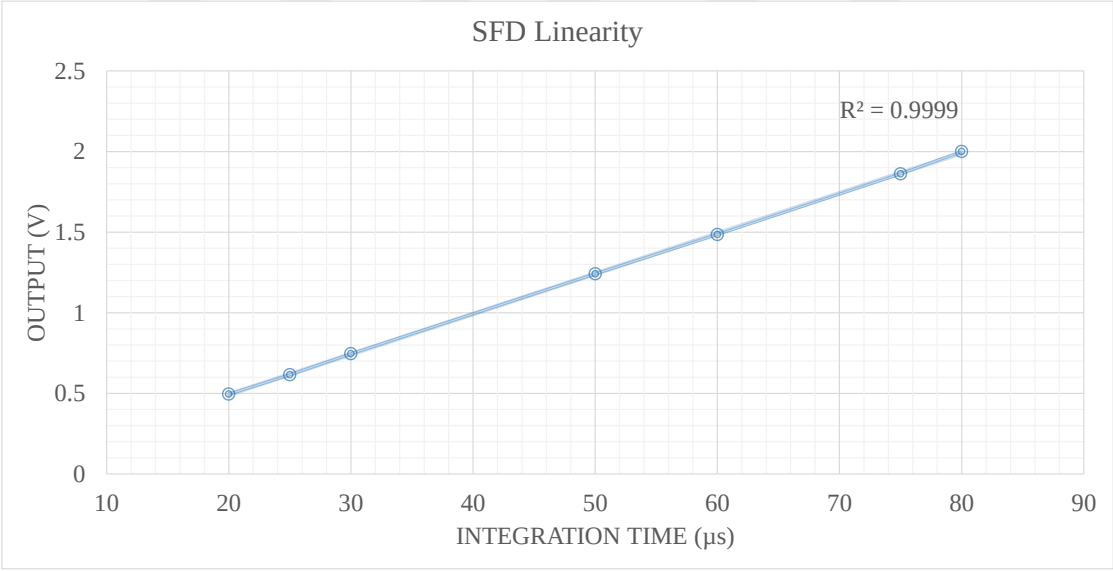


Figure 44: Linearity of the SFD amplifier.

scope is used for sampling data. 128 consecutive measurements are performed, and waveforms are saved. Extracted data is processed using MATLAB to obtain noise and signal values along with analog waveforms. Ratio of mean to standard deviation of measurements calculated:

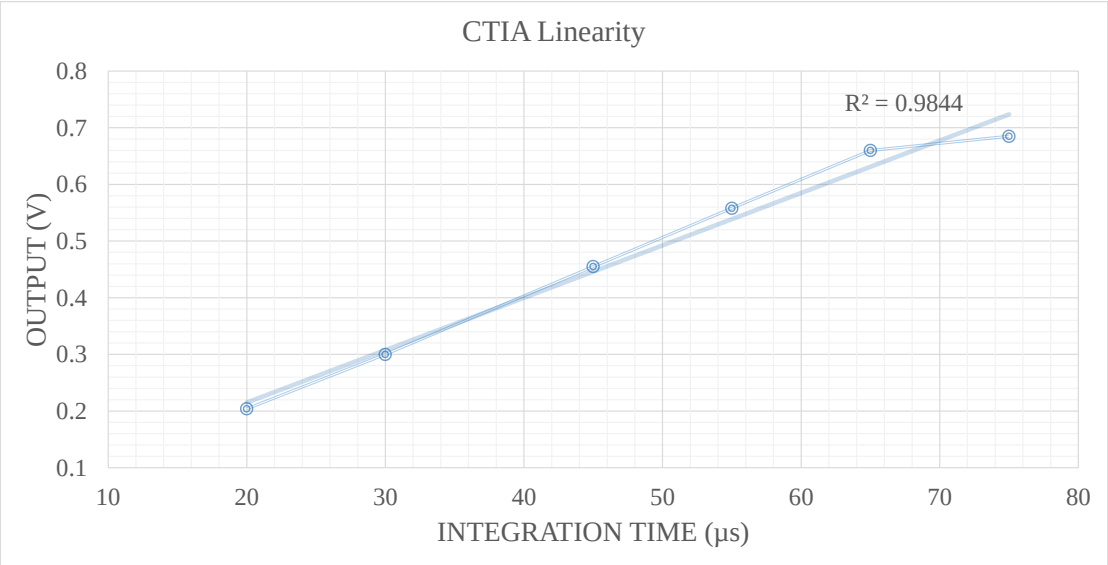


Figure 45: Linearity of the CTIA amplifier

$$SNR = \frac{\mu}{\sigma} \tag{23}$$

Fig. 46 shows SNR performances of CTIA and SFD amplifiers. As expected SNR performance of CTIA is superior due to low integration capacitance and high gain. Reasonable SNR performance obtained from SFD amplifier with its 40 fF integration capacitance. In this measurement integration time is increased until integration capacitance reaches in saturation. Just before saturation, maximum SNR values are observed. CTIA and SFD have reached 74.3 dB and 69.6 dB SNR respectively. 8.6 e^- noise is measured from CTIA amplifier with 45 K e^- charge handling capacity. Also, SFD has 252 e^- input referred noise with 764.4 K e^- charge handling capacity. Maximum charge handling capacity coming from SFD and noise level of the CTIA should be combined to calculate dynamic range of the analog readout. Since smart pixels select the best amplifier for every light level, we will have a very wide range of dynamic range which 98.9 dB. This value is highest dynamic range considering state of the art analog readouts.

In Fig. 46, approximately 300pA range seems to be the choice for threshold point between SNR and CTIA transition. Choosing threshold point for automatic selections depends on some parameters such as scene and detector performance. Detector capacity and resistance should have affect CTIA and DI performances. Also, If the threshold value is selected high, CTIA can be easily saturated before

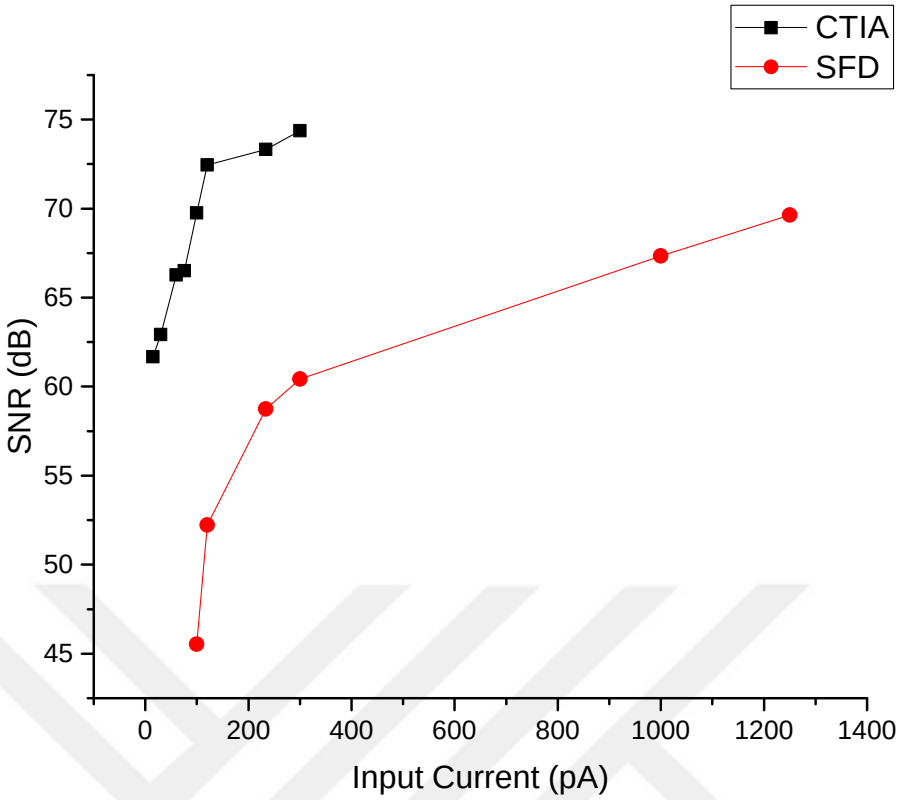


Figure 46: SNR of CTIA and SFD amplifiers

SFD.

Table 8 shows the comparison of the measured ROIC with literature. [42] and [43] are high dynamic range ROIC examples which were designed for high photocurrent levels and SWIR, respectively. [44] and [45] are using SFD and CTIA in the order given. Finally, [46] is given to compare analog ROICs with Digital ROICs.

According to the table, dynamic range is the best among analog ROICs in the literature. The ROIC has reasonable charge handling capacity for SWIR. The noise floor is again competitive among its rivals.

Regarding dynamic range [42] is quite a close competitor. [42] uses unique multiple sampling method and background suppression to reach 95.4 dB dynamic range. That architecture is inefficient for high speed and big arrays. Also, 50 μm pixel size is quite large compared to this work. [42] can use for a certain range of detectors.

[44] has a low readout noise (6 e^-) due to minimal integration capacitance and operating temperature. It is designed for astronomy measurements. Thus it has a slow frame rate (2 Hz) and low charge handling capacity (120 Ke^-). It operates

Table 8: Comparison

	This Work	[42]	[43]	[44]	[45]	DROIC [46]
Array Size	32x32	128x128	4x4	384x288	3x20	32x32
Pixel Size (μm^2)	22.5x22.5	50x50	30x30	15x15	N/A	30x30
Input Stage	CTIA, SFD	BDI	DI	SFD	CTIA	DI
Input Current	15 pA - 3 nA	20 nA - 112 nA	2 pA - 10 nA	astronomy	VLWIR	20 nA
Charge Handling Capacity (e^-)	45 K (CTIA), 764.4 K (SFD)	N/A	9.8 M	120 K	11 M	2.3 G
Frame Rate (Hz)	50	60	110	2	N/A	400
Power/Pixel	2.8 μW	1 μW w/o 14 bit ADC	800 nW	3.6 nW	11 μW	1 μW
Operating Temperature (K)	300	77	77 - 300	80 - 140	1.8 - 3	77 - 300
Readout Noise	8.6 e^-(CTIA), 252 e^-(SFD)	205 μV	350 e^-	6 e^-	1000 e^-	161 e^-
Dynamic Range (dB)	98.9	95.8	88.9	86	80	132
CMOS Technology	0.18 μm	0.35 μm	0.18 μm	0.35 μm	0.5 μm	90 nm

cryogenic temperatures. Due to very slow frame rate pixel per power consumption is extremely low (3.6 nW).

Regarding temperature, current range, dynamic range and technology, [43] performs closely to this work. Nevertheless, this work exceeds concerning dynamic range and input referred noise level but [43] has enormous charge handling capacity and low power. Another point should be taken into consideration is [43] designed for quantum dot (QDIP) detector. That is why [43] can utilize DI and handles very wide input current level (2 pA - 10 nA).

[45]'s work is similar to [44] with respect to an application. Both is designed for astronomical observations. Due to expected high dark current levels and to be able to achieve long integration times charge handling capacity is very high (11 Me^-). Moreover its the only competitor that utilizes CTIA for high dynamic range.

Finally, DROICs are the most significant development in the field of ROICs. DROICs are perfect for ultra wide dynamic range and charge handling capacity [46] is a decent example of a DROIC. It achieves 2.3 Ge^- charge handling capacity and 132 dB dynamic range. However, they are costly regarding technology node (90 nm CMOS), and their noise levels are comparable to analog ROICs [46]. This work and analog ROICs can answer most of the requirements of detectors well. Especially this work achieves better input referred noise performance compared to DROICs. Due to DROICs handle high photocurrents.

There are some drawbacks associated with DROICs that limits the availability of them in the market. There is no available commercial DROIC in the market up to now. It is incompatible with reducing pitch size trends. Reducing the pitch size increases spatial resolution. Because storage unit is digital, it takes much space. Depending on conversion size, counters take a lot of area. If integrate-while-read operation is desired as a specification, memory blocks also needed together with counters. That pushes for using 90 nm or smaller technology nodes which are very expensive. Analog ROICs are implemented in 180 nm and larger CMOS technology nodes which present a perfect balance of performance and price. Thus, analog ROICs have answers to drawbacks of DROICs. This thesis even pushes the limits of analog ROIC regarding functionality and by proposing the novel architecture. As a reply to DROICs proposed design promises high dynamic range, excellent compatibility

over 3^{rd} generation detectors and very low noise floor with high SNR.

5 Conclusion

Although, the history of the infrared detector is backed in the year of 1800 with Hershel's famous experiment that is the discovery of infrared radiation. Modern FPA's are very recent technologies. The first generation FPA's are only single-dimensional linear structures developed in the 1950s. Then, the second generation two-dimensional FPA's appeared in the 1970s. Today we are in the era of 3^{rd} generation detectors. We have the widest range of detectors before than ever. Some of the 3^{rd} generation IR detectors are MEMS, the multi quantum well, four-color FPAs, two-color type-II superlattice, two-color QDIP, two-color megapixel and less than 10 μm pitch sized HgCdTe detectors. We can summarize that research on IR Technologies has been focusing on enhancing the performance of new materials as well as well-known materials. Also, There are two principal directions into the development of detectors. One direction is upwards to obtain two or multi-color detectors by stacking materials. Another direction is inwards by increasing the array size and reducing the pitch size. Thus the development of detectors has been going faster than ROICs. Mostly same fundamental architectures are used for ROICs to answer the needs of new detectors. This thesis aims to meet new generation detector requirements such as two or multi-color, broad range spectrum, and low noise. As well as, it is intended to improve the dynamic range of analog ROICs by keeping noise floor at low.

In this thesis, a novel pixel architecture for third generation infrared detectors is proposed. This smart design introduces flux detection mechanism for the broad spectrum short wave infrared detector and dual/multicolor detectors. The basic structure can be implemented as different size and combinations of detectors.

The idea is based on the detection of the incoming flux and choosing the best input amplifier. One input amplifier is optimized for low flux levels, and another one is optimized for high flux levels. As an option user always has right to choose either of the input amplifiers. That architecture promises to improve high dynamic range which is one of the advantageous of DROICs.

The most significant development in the field of ROICs is digital ROICs. Digital ROICs promises extreme charge handling capacities like Giga electron range. That results above average SNR and ultra wide dynamic range (more than 100dB). Some

drawbacks limit the field of DROICs. There is no available commercial DROIC in the market up to now. It is incompatible with reducing pitch size trends. Because storage unit is digital, it takes much space. That pushes for using 90 nm or smaller nodes which are very expensive. Thus, analog ROICs have answers to drawbacks of DROICs. This thesis even pushes the limits of analog ROIC regarding functionality and by proposing the novel architecture. As a reply to DROICs proposed design promises high dynamic range, excellent compatibility over 3^{rd} generation detectors and very low noise floor with high SNR.

Analog ROIC's optimized to use a single preamplifier. Various sized capacitors are located inside the pixel to adapt different scenes. Those capacitors provide gain adjustment flexibility to the user. The user has to select manually to adjust target scene. Contrary proposed smart ROIC adjusts every scene automatically by giving a pixel-wise high dynamic range. Proposed architecture achieves high dynamic range that other analog ROIC cannot reach up to now.

In the array, every pixel is independent. It can choose any preamplifier according to the incoming photon flux. To understand and ease post-processing pixel provides 1-bit digital data along with analog voltage level. 1-bit data shows selected amplifier (0-low illumination and 1- high illumination optimized). Amplifiers voltage levels are different from each other. Thus, selected preamplifier information required to normalize different pre-amplifier outputs to create the best scene. Also, it is necessary for applying non-uniformity correction algorithms.

Light detection mechanism uses original timing scheme. In regular ROICs, there is reset, integration and read cycles. In this method, there are two integrations. First integration is very short compared to the second one. In the first integration, a photocurrent is integrated for a very short period. The comparator compares with threshold voltage if it exceeds that level, comparator activates high illumination optimized amplifier. Otherwise, comparator selects low light optimized amplifier. Second integration is just like typical integration; actual integration takes place in that period.

The user always has the flexibility to adjust threshold level. According to preamplifier performance, detector type or target scene; threshold can be favored to either of a preamplifier. Another flexibility is the adjustment of the first integration time.

The user may want to increase or decrease first integration time to favor one of the preamplifiers. The novel architecture is the US patented [47].

In this work, the novel smart solution is applied for SWIR range. In this range, CTIA and SFD amplifiers are chosen respectively for low, and high flux levels. CTIA provides excellent noise performance with minimal integration capacitance value. SFD works well in the upper range of SWIR.

Instead of using a dedicated comparator, CTIA is utilized as a comparator to save pixel area. Usually, CTIA is used as a single input common source amplifier. That topology both saves chip area and power. In this work, cascode differential amplifier is used as a CTIA. Cascode differential serves as a comparator in the first integration period. Another advantage is increasing bandwidth and gain improve noise performance.

32x32 prototype chip is designed in 0.18 μm XFAB technology and measured to demonstrate the idea. Instead of a detector, process and mismatch tolerant current sources are used to mimic a SWIR full range detector. 98.9 dB dynamic range is achieved with minimum 8.6 e^- input referred noise with CTIA amplifier and 764.4 Ke^- charges handling capacity with SFD.

According to the results dynamic range is the best among analog ROICs in the literature. It has reasonable charge handling capacity for SWIR. The noise floor is again competitive among its rivals. Table 8 compares the ROIC with the state of the art competitors. Regarding dynamic range [45] is quite close. [45] uses unique multiple sampling method and background suppression to reach 95.4 dB dynamic range. That architecture is inefficient for high speed and big arrays. Also, 50 μm pixel size is quite large. [44] has a great readout noise (6 e^-) due to quite small integration capacitance and operating temperature. That ROIC is designed for special purpose astronomy measurements which are the reason for quite a slow frame rate (2 Hz) and low charge handling capacity (120 Ke^-). Regarding temperature, current range, dynamic range and technology, [43] is the close competitor to this work. This work exceeds concerning dynamic range and input referred noise level but [43] has enormous charge handling capacity and low power. Another point should be taken into consideration is [43] designed for quantum dot (QDIP) detector. That is why [43] can utilize DI and handles very wide input current level well. Comparison

of this work and DROICs has already been made a couple of paragraphs above. To make it clear DROICs are perfect for ultra wide dynamic range and charge handling capacity but this work and analog ROIC can answer most of the requirements of detectors well. Especially this work achieves better input referred noise performance compared to DROICs. Due to DROICs handle high photocurrents.

In brief, a novel smart ROIC pixel architecture with significant benefits to 3^{rd} generation detectors are presented. It extends limits of analog ROIC regarding noise, dynamic range, and flexibility. It comes with a couple of drawbacks such as above average power consumption and pixel area utilization. Nevertheless, the novel approach would find itself a decent place in the state of the art for some time.

5.1 Future Works

One of the central mystery about the smart ROIC is how well it will work with an actual detector. Since, the ROIC is tested with current sources that mimics detector currents, actual performance with a real detector are not presented. There are some foreseeable complications regarding integration with a detector. Changing preamplifier may cause some bias stability problem. Also, a different preamplifier may need unique bias schemes. Those parameters are purely detector-dependent. Thus, the first future work is studying detector compatibility and performance.

Another future work is software related, and it has two branches. First switching between preamplifiers may cause glitches. Each amplifier has different voltage range. Since each pixel may change its preamplifier for each frame, creating smooth and balanced video is challenging. Secondly, high dynamic range image processing for the smart pixel can be investigated. Since it has more than one preamplifier, post processing can be challenging. Each preamplifier should be pass through nonuniformity correction individually. Their relative voltage differences should be taken into account as well.

Final future work can be an investigation of other preamplifier combinations by using same light detection mechanism. CTIA and DI combination can use for extreme wide range operation. Also, CTIA and BDI may work together well. That combination may cover SWIR-LWIR range with a single ROIC with carefully performed optimization. For, SWIR CTIA capacitance can be bigger to include full

SWIR range, and capacitance of DI should answer high large LWIR currents.

To sum up, there are three possible different challenges and future works beyond this thesis. One is related to detector and integration; other is fully software challenge and finally an alternative preamplifier selection and optimization problem.

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Appendix

```
//Verilog HDL, "digital_control" "functional"
//Digital Control Circuit

module digital_control2 #(

parameter    PIXEL_ROWS        = 6'd32   ,
PIXEL_COLS        = 6'd32   ,
PIXEL_ROWS_WIDTH = 3'd5  ,
PIXEL_COLS_WIDTH = 3'd5  ,
INT_TIME_WIDTH    = 6'd32   ,
LVL_TIME_WIDTH    = 5'd16   ,
SRL_WORD_WIDTH    = 6'd48   ,
SRL_CNTR_WIDTH    = 3'd6,
IDLE   = 2'b00  ,
LEVEL_CHK    = 2'b01  ,
INTEGRATION = 2'b11  ,
READ     = 2'b10  ,
IDLE_SRL   = 1'b0   ,
GET_SRL = 1'b1
) (

//Inputs
input            reset    ,
input          clk    ,

input          time_srl_data  ,
input          time_srl_start   ,

input     [3:0]     time_prl   ,

//Outputs
output   reg        int_time_out   ,
output   reg        lvl_chk_out    ,

output   reg    [PIXEL_COLS-1:0]     rn     ,
output   reg    [PIXEL_COLS-1:0]     g    ,
output   reg    [PIXEL_COLS-1:0]     reset_cti_sfd  ,
```

```
38 output  reg    [PIXEL_COLS-1:0]     int ,
39 output  reg    [PIXEL_COLS-1:0]     ctsf    ,
40 output  reg    [PIXEL_COLS-1:0]     ctia_cap  ,
41
42 output    [PIXEL_ROWS-1:0] row_sel  ,
43 output    [PIXEL_COLS-1:0] col_sel
44
45 );
46
47
48 //*****************************************************
49 // Internal wires and registers
50 //*****************************************************
51
52 reg [1:0]           state     ;
53 reg [1:0]           next_state    ;
54
55 reg             state_srl   ;
56 reg             next_state_srl  ;
57
58 reg [INT_TIME_WIDTH-1:0]    integ_time    ;
59 reg [LVL_TIME_WIDTH-1:0]    lvl_chk_time    ;
60
61 reg [INT_TIME_WIDTH-1:0]    integ_time_srl  ;
62 reg [LVL_TIME_WIDTH-1:0]    lvl_chk_time_srl  ;
63
64 reg [LVL_TIME_WIDTH-1:0]      cntr_lvl_chk    ;
65 reg [INT_TIME_WIDTH-1:0]      cntr_integ    ;
66
67 reg [SRL_WORD_WIDTH-1:0]    srl_data    ;
68 reg [SRL_CNTR_WIDTH-1:0]      cntr_srl_data   ;
69
70 reg [PIXEL_ROWS_WIDTH-1:0]    row_cntr    ;
71 reg [PIXEL_COLS_WIDTH-1:0]    col_cntr    ;
72
73 assign row_sel = (state == READ) ? 1<<row_cntr : {PIXEL_ROWS{1'b0}};
74 assign col_sel = (state == READ) ? 1<<col_cntr : {PIXEL_COLS{1'b0}};
75
76
```

```
77
78 //*****************************************************
79 // Main Logic
80 //*****************************************************
81
82 //******Main state machine********
83
84
85 always @(posedge clk) begin
86 if (reset)
87 state <= IDLE ;
88 else
89 state <= next_state ;
90 end
91
92 always @(*) begin
93 case (state)
94
95 IDLE   :    next_state = LEVEL_CHK;
96
97 LEVEL_CHK : if (cntr_lvl_chk == lvl_chk_time)
98 next_state = INTEGRATION;
99 else
100 next_state = LEVEL_CHK;
101
102 INTEGRATION : if (cntr_integ == integ_time)
103 next_state = READ;
104 else
105 next_state = INTEGRATION;
106
107 READ   : if (col_cntr == PIXEL_COLS-1 && row_cntr == PIXEL_ROWS-1)
108 next_state = IDLE;
109 else
110 next_state = READ;
111
112 endcase
113 end
114
115
```

```
116 //cntr_lvl_chk - Level check counter
117 always @(posedge clk) begin
118 if (reset)
119 cntr_lvl_chk <= {LVL_TIME_WIDTH{1'b0}};
120 else begin
121 case (next_state)
122 IDLE:     cntr_lvl_chk <= {LVL_TIME_WIDTH{1'b0}};
123 LEVEL_CHK: cntr_lvl_chk <= cntr_lvl_chk + {{LVL_TIME_WIDTH-1{1'b0}}, 1'
    b1};
124 default:   cntr_lvl_chk <= {LVL_TIME_WIDTH{1'b0}};
125 endcase
126 end
127 end
128
129 //lvl_chk_out - Level check outpu
130 always @(posedge clk) begin
131 if (reset)
132 lvl_chk_out <= 1'b0;
133 else begin
134 case (next_state)
135 IDLE:     lvl_chk_out <= 1'b0;
136 LEVEL_CHK: lvl_chk_out <= 1'b1;
137 default:   lvl_chk_out <= 1'b0;
138 endcase
139 end
140 end
141
142 //cntr_integ - Integration counter
143 always @(posedge clk) begin
144 if (reset)
145 cntr_integ <= 32'd0;
146 else begin
147 case (next_state)
148 IDLE:       cntr_integ <= {INT_TIME_WIDTH{1'b0}};
149 INTEGRATION: cntr_integ <= cntr_integ + {{INT_TIME_WIDTH-1{1'b0}}, 1'b1
    };
150 default:     cntr_integ <= {INT_TIME_WIDTH{1'b0}};
151 endcase
152 end
```

```
153 end
154
155 //int_time_out - Integration time output
156 always @(posedge clk) begin
157 if (reset)
158 int_time_out <= 1'b0;
159 else begin
160 case (next_state)
161 IDLE:       int_time_out <= 1'b0;
162 INTEGRATION: int_time_out <= 1'b1;
163 default:     int_time_out <= 1'b0;
164 endcase
165 end
166 end
167
168 //lvl_chk_time - Level check time register
169 always @(posedge clk) begin
170 if (reset)
171 lvl_chk_time <= {{LVL_TIME_WIDTH-2{1'b0}}, 2'd2};
172 else if (next_state == IDLE)
173 case (time_prl)
174 4'd0: if (state_srl == 1'b0)
175 lvl_chk_time <= lvl_chk_time_srl;
176 else
177 lvl_chk_time <= {{LVL_TIME_WIDTH-2{1'b0}}, 2'd2};
178 4'd1: lvl_chk_time <= {{LVL_TIME_WIDTH-8{1'b0}}, 8'd8};
179 4'd2: lvl_chk_time <= {{LVL_TIME_WIDTH-8{1'b0}}, 8'd16};
180 4'd3: lvl_chk_time <= {{LVL_TIME_WIDTH-8{1'b0}}, 8'd16};
181 4'd4: lvl_chk_time <= {{LVL_TIME_WIDTH-8{1'b0}}, 8'd32};
182 4'd5: lvl_chk_time <= {{LVL_TIME_WIDTH-8{1'b0}}, 8'd32};
183 4'd6: lvl_chk_time <= {{LVL_TIME_WIDTH-8{1'b0}}, 8'd64};
184 default:  lvl_chk_time <= {{LVL_TIME_WIDTH-8{1'b0}}, 8'd4};
185
186 endcase
187 end
188
189 //integ_time - Integration time register
190 always @(posedge clk) begin
191 if (reset)
```

```
192 integ_time <= {{INT_TIME_WIDTH-8{1'b0}}, 8'd128};
193 else if (next_state == IDLE)
194 case (time_prl)
195 4'd0: if (state_srl == 1'b0)
196 integ_time <= integ_time_srl;
197 else
198 integ_time <= {{INT_TIME_WIDTH-8{1'b0}}, 8'd128};
199 4'd1: integ_time <= {{INT_TIME_WIDTH-16{1'b0}}, 16'd64};
200 4'd2: integ_time <= {{INT_TIME_WIDTH-16{1'b0}}, 16'd64};
201 4'd3: integ_time <= {{INT_TIME_WIDTH-16{1'b0}}, 16'd128};
202 4'd4: integ_time <= {{INT_TIME_WIDTH-16{1'b0}}, 16'd256};
203 4'd5: integ_time <= {{INT_TIME_WIDTH-16{1'b0}}, 16'd512};
204 4'd6: integ_time <= {{INT_TIME_WIDTH-16{1'b0}}, 16'd2048};
205 default:  integ_time <= {{INT_TIME_WIDTH-16{1'b0}}, 16'd4096};
206
207 endcase
208 end
209
210 //col_cntr - Column counter
211 always @(posedge clk) begin
212 if (reset)
213 col_cntr <= {PIXEL_COLS_WIDTH{1'b0}};
214 else if (state == READ && col_cntr == PIXEL_COLS-1)
215 col_cntr <= {PIXEL_COLS_WIDTH{1'b0}};
216 else if (state == READ)
217 col_cntr <= col_cntr + {{PIXEL_COLS_WIDTH-1{1'b0}}, 1'b1};
218 end
219
220 //row_cntr - Row counter
221 always @(posedge clk) begin
222 if (reset)
223 row_cntr <= {PIXEL_ROWS_WIDTH{1'b0}};
224 else if (next_state == IDLE)
225 row_cntr <= {PIXEL_ROWS_WIDTH{1'b0}};
226 else if (state == READ && col_cntr == PIXEL_COLS-1)
227 row_cntr <= row_cntr + {{PIXEL_ROWS_WIDTH-1{1'b0}}, 1'b1};
228 end
229
230 //*****Output control signals********
```

```
231 always @(posedge clk) begin
232 if (reset)
233 rn <= 32'd0;
234 else begin
235 case (next_state)
236 IDLE:       rn <= 32'd0;
237 LEVEL_CHK:    rn <= 32'd0;
238 INTEGRATION: rn <= 32'hFFFFFFFF;
239 READ:     rn <= 32'hFFFFFFFF;
240 endcase
241 end
242 end
243
244 always @(posedge clk) begin
245 if (reset)
246 g <= 32'hFFFFFFFF;
247 else begin
248 case (next_state)
249 IDLE:       g <= 32'hFFFFFFFF;
250 LEVEL_CHK:    g <= 32'hFFFFFFFF;
251 INTEGRATION: g <= 32'd0;
252 READ:     g <= 32'd0;
253 endcase
254 end
255 end
256
257 always @(posedge clk) begin
258 if (reset)
259 reset_cti_sfd <= 32'hFFFFFFFF;
260 else begin
261 case (next_state)
262 IDLE:       reset_cti_sfd <= 32'hFFFFFFFF;
263 LEVEL_CHK:    reset_cti_sfd <= 32'd0;
264 INTEGRATION: reset_cti_sfd <= 32'd0;
265 READ:     reset_cti_sfd <= 32'd0;
266 endcase
267 end
268 end
269
```

```
always @(posedge clk) begin
if (reset)
int <= 32'd0;
else begin
case (next_state)
IDLE:       int <= 32'd0;
LEVEL_CHK:    int <= 32'd0;
INTEGRATION: int <= 32'd0;
READ:     int <= 32'hFFFFFFFF;
endcase
end
end

always @(posedge clk) begin
if (reset)
ctsf <= 32'd0;
else begin
case (next_state)
IDLE:       ctsf <= 32'd0;
LEVEL_CHK:    ctsf <= 32'd0;
INTEGRATION: ctsf <= 32'hFFFFFFFF;
READ:     ctsf <= 32'hFFFFFFFF;
endcase
end
end


always @(posedge clk) begin
if (reset)
ctia_cap <= 32'd0;
else begin
case (next_state)
IDLE:       ctia_cap <= 32'd0;
LEVEL_CHK:    ctia_cap <= 32'hFFFFFFFF;
INTEGRATION: ctia_cap <= 32'd0;
READ:     ctia_cap <= 32'd0;
endcase
end
end
```

```
309
310
311
312
313 //*****************************************
314 // Receive serial data
315 //*****************************************
316 always @(posedge clk) begin
317 if (reset)
318 state_srl <= IDLE_SRL;
319 else
320 state_srl <= next_state_srl;
321 end
322
323 always @(*) begin
324 case (state_srl)
325
326 IDLE_SRL: if (time_srl_start)
327 next_state_srl = GET_SRL;
328 else
329 next_state_srl = IDLE_SRL;
330
331 GET_SRL:  if (cntr_srl_data == 6'd48)
332 next_state_srl = IDLE_SRL;
333 else
334 next_state_srl = GET_SRL;
335
336 endcase
337 end
338
339 //cntr_srl_data - Serial data counter
340 always @(posedge clk) begin
341 if (reset)
342 cntr_srl_data <= {SRL_CNTR_WIDTH{1'b0}};
343 else if (cntr_srl_data == SRL_WORD_WIDTH)
344 cntr_srl_data <= {SRL_CNTR_WIDTH{1'b0}};
345 else if (next_state_srl == GET_SRL)
346 cntr_srl_data <= cntr_srl_data + {{SRL_CNTR_WIDTH-1{1'b0}}, 1'b1};
347 end
```

```
348
349 //srl_data - Serial data receive register
350 always @(posedge clk) begin
351 if (reset)
352 srl_data <= {SRL_WORD_WIDTH{1'b0}};
353 else if (next_state_srl == GET_SRL)
354 srl_data <= {time_srl_data, srl_data[SRL_WORD_WIDTH-1:1]};
355 end
356
357 //lvl_chk_time_srl - Level check serial
358 always @(posedge clk) begin
359 if (reset)
360 lvl_chk_time_srl <= {LVL_TIME_WIDTH{1'b0}};
361 else if (cntr_srl_data == SRL_WORD_WIDTH)
362 lvl_chk_time_srl <= srl_data[SRL_WORD_WIDTH-1:INT_TIME_WIDTH];
363 end
364
365 //integ_time_srl - Level check serial
366 always @(posedge clk) begin
367 if (reset)
368 integ_time_srl <= {INT_TIME_WIDTH{1'b0}};
369 else if (cntr_srl_data == SRL_WORD_WIDTH)
370 integ_time_srl <= srl_data[INT_TIME_WIDTH-1:0];
371 end
372
373 endmodule
```