A 6-Bit Time-Interleaved Asynchronous Successive Approximation Register Analog-to-Digital Converter with 1-Bit Redundancy in 90nm Technology

by

Arman Galioglu

01.08.2017

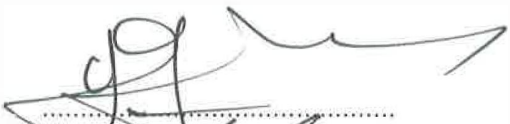
Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of
Master of Science

Sabancı University

Summer, 2017

A 6-Bit Time-Interleaved Asynchronous Successive Approximation Register Analog-to-Digital Converter with 1-Bit Redundancy in 90nm Technology

APPROVED BY

Prof. Dr. Yaşar GÜRBÜZ ..... 
(Thesis Supervisor)

Assoc. Prof. Dr. Meriç ÖZCAN ..... 

Asst. Prof. Dr. Erdinç ÖZTÜRK ..... 

DATE OF APPROVAL: 01.08.2017

Acknowledgements

First and foremost, I wish to express my deepest gratitude to my thesis advisor Professor Yaşar Gürbüz for his invaluable guidance and support during my undergraduate and master's studies at Sabancı University. I would not be where I am right now without his assistance and never-ending motivation.

Next, I would like to thank Assoc. Prof. Meriç Özcan and Asst. Prof. Erdinç Öztürk for taking their time to serve on my thesis committee and for their valuable comments. I would also like to thank them for contributing to my instruction over the years. They are excellent instructors and I sincerely appreciate their efforts.

I am extremely thankful to my colleagues in the SU Microelectronics Research group for providing such an inspiring, interesting and jovial work environment. I have been very fortunate to have been a member of this group and I express my gratitude to every single member. I am especially grateful to Shahbaz Abbasi for helping me along the way of our research and always sparing his time to answer my questions. I am forever indebted to him for his mentoring during my studies and his enlightening expertise as well as for our many discussion on ADCs and infrared imager readouts. I also would like to thank my companions in the group, Dr. Melik Yazıcı, Dr. Ömer Ceylan, Abdurrahman Burak, Eşref Türkmen, Atia Shafique, Emre Can Durmaz, Elif Gül Arsoy, Alper Güner, İlker Kalyoncu, Murat Davulcu, Can Çalışkan, and Atia Shaque for creating such a friendly working environment, including the past members Barbaros Çetindoğan, Berktuğ Üstündağ. I would also like to thank our current and past laboratory staff members Ali Kasal and Mehmet Doğan for their continuous hard work, help and friendship.

Last, but not the least, I would like to express my deepest gratitude and love to my mother Bala for her unparalleled love and support and for encouraging me to pursue electronics. Her unconditional and pure love has been my rock whenever I needed it.

A 6-Bit Asynchronous Time Interleaved Successive Approximation Register Analog-to-Digital Converter with 1 Bit Redundancy in 90nm Technology

Arman Galioglu
EE, Master's Thesis, 2017
Thesis Supervisor: Prof. Dr. Yaşar GÜRBÜZ

Keywords: Asynchronous SAR ADC, Time-Interleaving, Redundancy

Abstract

High speed ADC architectures constitute the heart of many different applications such as wireless and wireline communication systems, instrumentation systems, data acquisition systems. A 6-bit, 700MSps low power successive approximation register (SAR) analog-to-digital converter (ADC) with 1-bit redundancy has been designed and fabricated in 90nm CMOS process. The speed of 700 MSps is achieved by time-interleaving four fully differential asynchronous SAR sub-ADC channels each of which achieves approximately 178 MSps data rate. A full custom digital path that speeds up the asynchronous SAR loop control path has been implemented to achieve this single channel data rate along with 1-bit redundancy to reduce the errors from settling time of the capacitive digital-to-analog converter (CDAC). The capacitive DAC (CDAC) is based on a full differential V_{CM}-based switching scheme which reduces the overall switching energy. The time-interleaved structure includes a low-skew non-overlapping clock generation circuit to reduce possible timing skew mismatch between the interleaved channels. The ADC works with 1.2V power supplies, 1V and 0.5 V references and a 700MHz clock. Three different ADC prototypes have been implemented the single channel, two channel and four channel time-interleaved ADCs are given in this thesis. The SNDR, ENOB of the single channel ADC are 37.4dB, 5.94 bits for $f_{\text{in}} << f\mathbf{s}$ and degrades to 29.4 dB at $f_{\text{in}} = f\mathbf{s}/2$. The time interleaved circuit achieves a 0.28 LSB INL/0.24 DNL in simulation without any calibration. The Walden Figure of Merit is calculated to be 181.8 fJ/conv-step and the Schreier Figure of Merit is found to be 143.53 dB.

90nm Teknolojisinde Ekstra 1 Bit Yedek Bilgi ile 6-Bit Asenkron Ayrık Zamanlı Ardışık Yaklaşımlı Örneksel Sayısal Çevirici

Arman Galioglu
EE, Yüksek Lisans Tezi, 2017
Tez Danışmanı: Prof. Dr. Yaşar GÜRBÜZ

Anahtar Kelimeler: Ardışık Yaklaşımlı Örneksel Sayısal Çevirici, Asenkron, Ayrık Zaman Dönüşümlü Çalışma, Fazlalık Bilgi, Analog Sayısal Çevirici

Özet

Yüksek hızlı ADC mimarileri, kablosuz ve kablolu iletişim sistemleri, veri toplama sistemleri, enstrümantasyon sistemleri gibi pek çok farklı uygulamanın kalbini oluşturur. 6 bit, 700 MSps ve 1 bit fazlalıklı düşük güç ardışık yaklaşım yazmacı (SAR) analog-dijital dönüştürücü (ADC) tasarlanmış ve 90nm teknolojisinde gerçeklenmiştir. . 700MSps'in hızı, her biri yaklaşık 178 MSps veri hızı ile çalışan 4 alt blok tam diferansiyel asenkron SAR ADC kanalının yer aldığı parallelleme ile elde edilmektedir. Tam özel dijital SAR döngü kontrol yolu kanal hızları artmakta ve 1 bit fazlalık ile birlikte kapasitif dijital-analog dönüştürücü (CDAC) yatışma süresi hataları azaltılmaktadır. Kapasitif DAC (CDAC) tasarımı, anahtarlama enerjisini azaltan tam diferansiyel V_{CM}-tabanlı anahtarlama şemasına dayanmaktadır. Zaman aralıklı parallelleme yapısında kanallar arasındaki muhtemel zamanlama kaymalarının azalması için az sapmalı örtüşmeyen saat üretme devresi içermektedir. ADC, 1.2V güç kaynağı, 1V ve 0.5V referanslar ve 700 MHz saat ile çalışmaktadır. Bu tezde, tek kanallı, iki kanallı ve dört kanallı zaman aralıklı prototip ADC'ler tasarlanıp gerçeklenmiştir. $f_{\text{in}} << f\mathbf{s}$ için ADC'nin benzetim sonuçları 37.4 dB SNDR değeri, 5.94 bit ENOB değeri vermektedir, $f_{\text{in}} = f\mathbf{s}/2$ için SNDR değeri 29.4 dB'ye gerilemektedir. Dört kanallı ADC devresi kalibrasyon olmaksızın simulasyon sonuçlarında 0.28 LSB INL/0.24 DNL'ye sahiptir. ADC'nin Walden değer katsayısı 181 fJ/dönüşüm adımı, Schreier değer katsayısı ise 143.53 dB'dir.

Contents

List of Figures

List of Tables

List of Abbreviations

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DC	Direct Current
DNL	Differential Nonlinearity
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FoM	Figure of Merit
$\mathbf{FoM_S}$	Schreier Figure of Merit
$\mathbf{FoM_W}$	Walden Figure of Merit
FOM	Figure-of-Merit
INL	Integral Nonlinearity
HP	High Pass
IC	Integrated Circuit
LSB	Least Significant Bit
LP	Low Pass
MC	Monte Carlo
MCS	Merged Capacitor Switching
MDAC	Multiplying Digital-to-Analog Converter
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide-Semiconductor
MSB	Most Significant Bit
PVT	Process Voltage Temperature
RMS	Root Mean Square
SAR	Successıve Approximation Register
SFDR	Spurious Free Dynamic Range
SINAD	Signal to Noise and Distortion Ratio
SoC	System on Chip
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio
THD	Total Harmonic Distortion
TI	Time-Interleaved
UWB	Ultra Wide Band

1 Introduction

1.1 Motivation

Today, "Everything is digital" has become a motto for many electronic systems. It is true that most signal processing in electronic systems are done in the digital domain, where the discrete representation of signals in time and amplitude provide efficient digital signal processing, storage, error correction capabilities, and immunity to certain margin of distortion and noise. However, real world signals are analog, continuous in time and amplitude. We are also analog, our senses of sight and hearing are also analog. The input signals from the real world to our senses and to electronic sensors such as voice, force, temperature are also analog. As such, the analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) have a paramount importance in bridging the real world and the digital domain, and neither their proliferation nor their pervasiveness in all kinds of electronic systems is likely to come to an end in the near future. The most recent applications in instrumentation, wireline and wireless telecommunication, consumer electronics demand ever-increasing resolution, bandwidth, linearity, precision, and efficiency from ADCs. Considering that most of the chips produced today are digital, the technology scaling has been in favor of improving the economics and performance of digital chips, digital signal processing continuously becomes more efficient with respect to chip power consumption and area. Indeed, for many decades Moore's law -the empirical observation that about every 18 months the density of transistors on a given silicon area doubles- has held true. As technology scales down to nanometers, the transistors get smaller while their switching speed increases and the digital circuit performance improves considerably. However, technology scaling has imposed many challenges in analog circuits. The supply voltage continues to scale down with the gate oxide and technology node, reducing the power consumption of digital circuits but also rendering the analog signals more prone to interference, noise and signal swing issues. The mismatch between integrated circuit elements increases as we scale their areas down as noted by Pelgrom [5]. The nanoscale transistors also provide less gain and exhibit poorer flicker noise performance. Coupled with these digital

circuits are the analog interfaces and analog circuit blocks that need to deliver a similar performance improvement in data rate, efficiency and precision to avoid being the bottleneck in a System on a Chip (SoC). Furthermore, nowadays mobile and wearable applications place an emphasis on power efficient design more than ever. In this thesis, we present a low power 6-bit asynchronous four-way time-interleaved successive approximation register (SAR) ADC in 90nm technology that achieves 700 MSPs and incorporates 1-bit redundancy. The motivation in the design of this SAR ADC was to achieve a sub-ADC design as fast as possible to reduce the interleaved channels required. An ADC of this speed and resolution is suitable for ultra wide band (UWB) applications according to Federal Communications Commission (FCC) and European Telecommunications Standards Institute (ETSI) regulations.

1.2 ADC Operations

The processing of analog inputs through every ADC can be dissected into four core functions; continuous time filtering (for anti-aliasing), sampling, quantization, and coding. In this section, we will introduce these operations and briefly mention their implications for the overall ADC.

1.2.1 Sampling

A sampler maps a continuous time signal into a sampled-data point sequence. The fundamental theorem that governs the sampling operation is the Nyquist-Shannon theorem which establishes a sufficient condition for the required sampling rate that gathers all the information from a continuous time bandwidth-limited signal. In [6], Shannon states the theorem as: "If a function contains no frequencies higher than BW cycles per second, it is completely determined by giving its ordinates at a series of points spaced 1/2BW seconds apart." This criterion states that if the sampling frequency is at least more than twice the signal bandwidth, then there is a way to uniquely reconstruct the signal. To understand why this is so, a look into effects of sampling in the frequency domain is necessary. In time domain, sampling can be seen as multiplying a signal, x(t), with a uniform, equidistant pulse train equally spaced apart by the sampling period, $T_s = 1/f_s$. Assuming that the

sampling operation is instant; we can use the Dirac comb for our pulse train:

$$x_s(t) = x(t) \sum_{n=-\infty}^{\infty} \delta(t - n \cdot T_s) \tag{1}$$

Then taking the Fourier transform of the Dirac pulse train to find:

$$\mathcal{F}\left\{ \sum_{n=-\infty}^{\infty} \delta(t - n \cdot T_s) \right\} = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - n \cdot f_s) \tag{2}$$

Since the multiplication in time domain corresponds to convolution in the frequency domain, we have:

$$X_s(f) = X(f) \star \left[\frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - n \cdot f_s) \right] \tag{3}$$

$$= \int_{-\infty}^{\infty} X(k) \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - k - n \cdot f_s) \mathrm{d}k \tag{4}$$

$$= \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \int_{-\infty}^{\infty} X(k) \delta(f - k - n \cdot f_s) \mathrm{d}k \tag{5}$$

$$= \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X(f - n \cdot f_s) \tag{6}$$

The last equation reveals that the sampling operation corresponds to replication of the signal's original spectrum in the frequency domain with f_s=$1/T_s$ frequency. Therefore, reconstruction is only possible if the signal is not aliased i.e., the replicas are not overlapping. Thus, this condition calls for a sampling rate, $\mathrm{f_s}$, and a signal bandwidth (BW) to be related as stated in the Nyquist-Shannon theorem:

$$f_s > 2BW \tag{7}$$

Half of the sampling frequency is termed as the Nyquist frequency, and the interval of 0 to $f_s/2$ is referred to as the first Nyquist band. The intervals $f_s/2$ to f_s, f_s to $3f_s/2$ are the second and third Nyquist bands and so on. Following from our interpretation of equation (6), it can be seen that the second Nyquist band folds back into the first band, resulting in aliasing, after sampling. This criterion holds considering ideal filters, in practice, the sampling rate is more than twice the

bandwidth of the signal depending on the quality of the anti-aliasing filter.

1.2.2 Continuous Time Filtering

Continuous Time (CT) Filters, though not strictly part of the ADC itself, is almost always used in the signal path before an ADC to condition the signal. The primary tasks of these filters are to limit the bandwidth of the input signal to prevent aliasing and distortion, reduce integrated noise from the bandwidth, and suppress out-of-band interference. In general, the most simple and common CT filters used to accomplish the aforementioned tasks and satisfy the Nyquist criterion are CT low pass filters. Unfortunately, while discrete time filters offer attractive switched capacitor implementations and better linearity, they sample the signal themselves to operate and thus cannot be used to implement anti-alias filtering. The design of these filters are determined by the sampling frequency, input bandwidth, and the architecture choice. Specifically, the input signal bandwidth and sampling frequency determine the width of the transition band for the filter i.e., stopband attenuation must be highly effective starting from f_s-f_B, where f_s is the sampling frequency, and f_B is the signal bandwidth, which in turn determines the number of poles required for the filter. For instance, if the transition band is 1 decade wide in frequency, then a 40dB attenuation would require a 2^{nd}-order filter. It is also possible to implement digital anti-aliasing filters or incorporate undersampling methods to relax the specifications of the analog anti-aliasing filter that precedes the ADC. We refer the interested reader to [7] and [8] for a more precise treatment on this subject.

1.2.3 Quantization

Amplitude quantization is the assignment of continuous ranges of analog values to a number of discrete levels determined by the resolution. As such, an ideal linear quantizer divides its dynamic range into a number of equal quantization intervals and assigns these intervals to their respective discrete states. Therefore, in the process of converting from analog to digital, some information is lost on the analog signal considering many analog signals are represented by the same digital code. Since the each discrete level corresponds to their respective whole intervals, quantizing an input other than the mid-point of the discrete intervals will inherently lead to

this information loss which is known as the quantization error, a.k.a. quantization "noise". The quantization error for an ideal 3 bit ADC is shown in Fig. 1 below, where the Q variable corresponds to the range of one interval, least significant bit (LSB) value of the ADC.

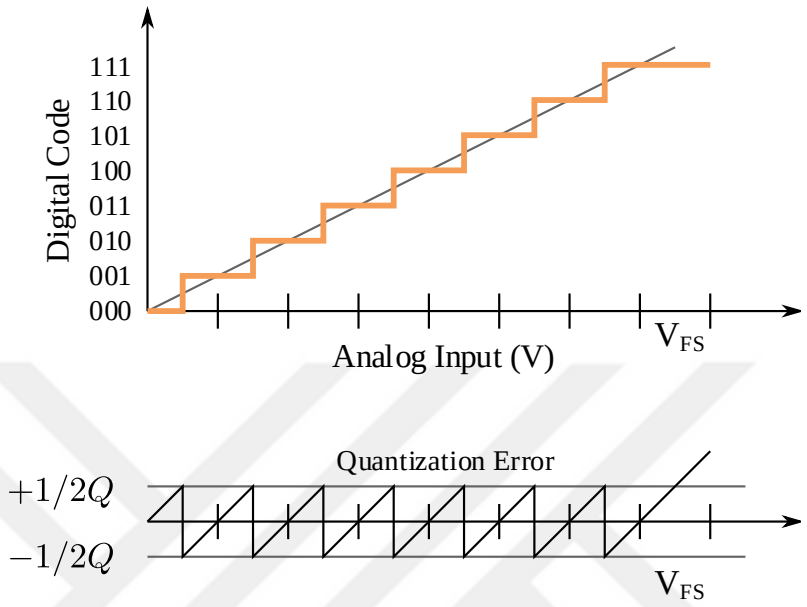


Figure 1: The Ideal ADC Transfer Characteristic

Two aspects of this quantization error need to be defined, analyzed for designers to evaluate its noise impact on the quantized signal. First, how much noise power is added to the input signal as a result of quantization? Second, what is this frequency spectrum for this added quantization noise? A first order approximation analysis for the quantization "noise" is given below. However, before we go into that to be able to treat the quantization error as noise requires some necessary conditions which are often neglected by designers and could spell disaster if not rectified. The conditions specified are: all quantization levels, meaning digital output codes, are expected to be used with equal probability and are uniform, a lot of quantization levels are available, and the quantization error is not correlated with the input signal [8]. As ADCs are typically tested with sine waves, if the ratio of the sine wave input frequency and the sampling frequency is rational, then the quantization error becomes correlated with the input and is not fully captured. We will visit the implications of this last condition during the simulation results for this work. For an ideal ADC, the staircase transfer function is given in Fig. 1. If the input is random, the error between the input and the digital output has a uniform probability density

function as shown in 2, any value of the quantization error is equally likely.

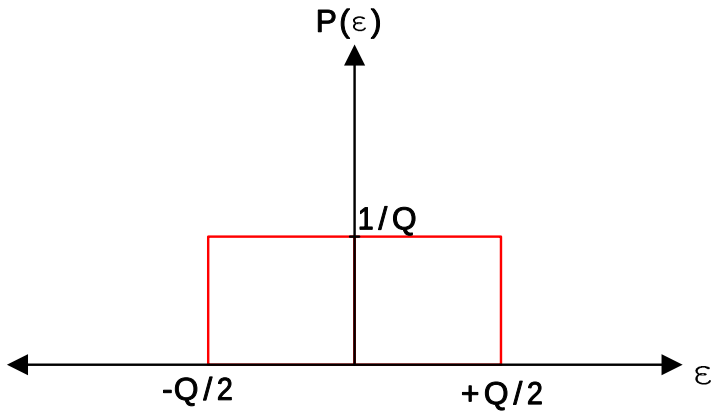


Figure 2: The Probability Distribution Function for the Quantization Error

$$P(\varepsilon) = \frac{1}{Q} \quad \text{for} \quad (\frac{-Q}{2} < \varepsilon < \frac{+Q}{2}) \tag{8}$$

Then the root-mean-square of the quantization error is

$$v_{qn} = \sqrt{\frac{1}{Q}\int_{-Q/2}^{+Q/2} x^2 dx} = \sqrt{\frac{1}{Q}\left[\frac{x^3}{3}\right]_{-Q/2}^{+Q/2}} = \sqrt{\frac{Q^2}{2^3 3} + \frac{Q^2}{2^3 3}} = \frac{Q}{\sqrt{12}} \tag{9}$$

and the quantization error noise power is

$${v_{qn}}^2 = \frac{Q^2}{12} \tag{10}$$

The sawtooth waveform, shown in Fig. 1, produces high frequency harmonics that go beyond the Nyquist bandwidth. All the same, these frequencies also fold back into the first Nyquist band and add up to produce the RMS noise voltage of $Q/\sqrt{12}$ as derived above. The root-mean-square (RMS) value of a full-scale sinusoidal input is

$$V_{rms,sine} = \frac{V_{ref}}{2\sqrt{2}} = \frac{2^N Q}{2\sqrt{2}}. \tag{11}$$

where N is the number of bits that corresponds to the resolution of the quantization. Then, the maximum SNR we can expect from a sinusoidal signal that has been quantized is

$$SNR = 20\log\left(\frac{V_{rms,sine}}{v_{qn}}\right) = 20\log\left(\frac{\frac{2^N Q}{2\sqrt{2}}}{\frac{Q}{\sqrt{12}}}\right) = 20\log\left(\frac{2^N\sqrt{12}}{2\sqrt{2}}\right) \tag{12}$$

$$= 20\log\left(2^N\right) + 20\log\left(\frac{\sqrt{6}}{2}\right) = 6.02N + 1.76(dB) \tag{13}$$

This turns out to be a quite useful relation, giving the designers an understanding of what the capabilities of an ideal ADC are with respect to signal quality. Of course, one needs to note that this equation is valid for signals that occupy the full Nyquist bandwidth of 0 to $f_s/2$. IF the signal in question has a smaller BW than the Nyquist BW, filtering and oversampling can be used to filter out the quantization noise that lies outside the signal BW. This results in a slightly modified SNR relation for ideal ADCs as shown in 14 which is valid now over the signal BW.

$$SNR = 6.02N + 1.76(dB) + 10\log\left(\frac{f_s}{2BW}\right) \tag{14}$$

1.2.4 Coding

Encoding the quantized discrete levels to be processed is the concluding operation of an ADC. The most straightforward code scheme is the Unipolar Straight Binary (USB) code, used for unipolar signals, where the first quantization level is mapped to all zeros (....0000) and the full-scale level is all ones (...1111). Complementary Straight Binary (CSB) coding scheme is the one's complement of Unipolar Straight Binary, i.e. the full-scale is mapped to all zeros this time. Bipolar Offset Binary (BOB) coding is used in systems with bipolar signals where the range of the ADC is from $-V_{FS}$ to $+V_{FS}$. The digital count begins with all zeros at the negative full-scale voltage and increases to all ones at the positive full-scale. Hence, the most significant bit (MSB) indicates the sign of the input in this coding scheme. Similarly, one's complement of this scheme is called the Complementary Offset Binary (COB) coding. The most widely used code scheme standard, primarily used in microprocessors and digital audio is Binary Two's Complement (BTC). In this scheme, the bit in the most significant bit position indicates the sign of the input, 0 for positive and 1 for negative. The positive inputs follow the same digital coding as in the USB code, where the positive full-scale is now (01...1111). The digital code corresponding

to negative full-scale is (10...0000). Likewise, a Complementary Two's Complement (CTC) coding exists that is one's complement of BTC. Virtually, the outputs of ADCs and inputs of DACs can be coded differently in many ways. However, it is trivial to convert between these coding schemes either by inverting the input of the ADC/the output of the DAC in the analog domain or inverting the individual bits at the output of the ADC/the input of the DAC in the digital domain. For instance, converting between the coding schemes that are one's complement of each other such as USB and CSB, BOB and COB, BTC and CTC only requires inverters at the output of all bits. A complete table of these conversion relations is given in Table 1.

Table 1: Conversion between coding schemes

Invert all bits	COB<->BOB	USB<->CSB	BTC<->CTC
Invert only MSB	BOB<->BTC	COB<->CTC	
Invert all bits except MSB	BOB<->CTC	COB<->BTC	

1.3 Nyquist ADC Architectures

In this section, a brief introduction to Nyquist-rate data converter architectures is given. As mentioned previously, the sampling operation of the ADC requires a limitation of the bandwidth of the input signal, where the sampling frequency of the ADC must be greater than or equal to twice the highest frequency signal in the input, practically much greater due to non-idealities of anti-aliasing filters. Unlike Nyquist-rate ADCs, oversampled data converters with noise shaping use an oversampling modulator and a decimation filter to shape the white spectrum quantization noise into out-of-band frequencies and filter it out to trade-off resolution vs. speed. The oversampled data converters are omitted in this thesis for the sake of brevity. We refer the interested readers to [9] and [10] for a deeper look into oversampled data converters. An algorithm based categorization of Nyquist ADC architectures is given in Table 2.

1.3.1 Flash ADCs

Flash ADCs are the fastest operating Nyquist ADC type, operating from hundreds of mega samples per second to tens of giga samples per second. They imple-

Table 2: Nyquist ADC Architectures

Algorithm	Nyquist ADC Architecture		
Fully Parallel Search	Flash ADC		
Binary Sequential Search	Successive Approximation ADC		
Linear Sequential Search	Integrating ADCs		
Sub-binary Sequential Search	Cyclic/Algorithmic ADC	Sub-ranging ADC	Pipeline ADC

ment an entirely parallel searching algorithm i.e., an N-bit resolution flash converter has 2^{N-1} comparators connected and working in parallel to find the discrete range input signal falls in, as shown in Fig. 3.

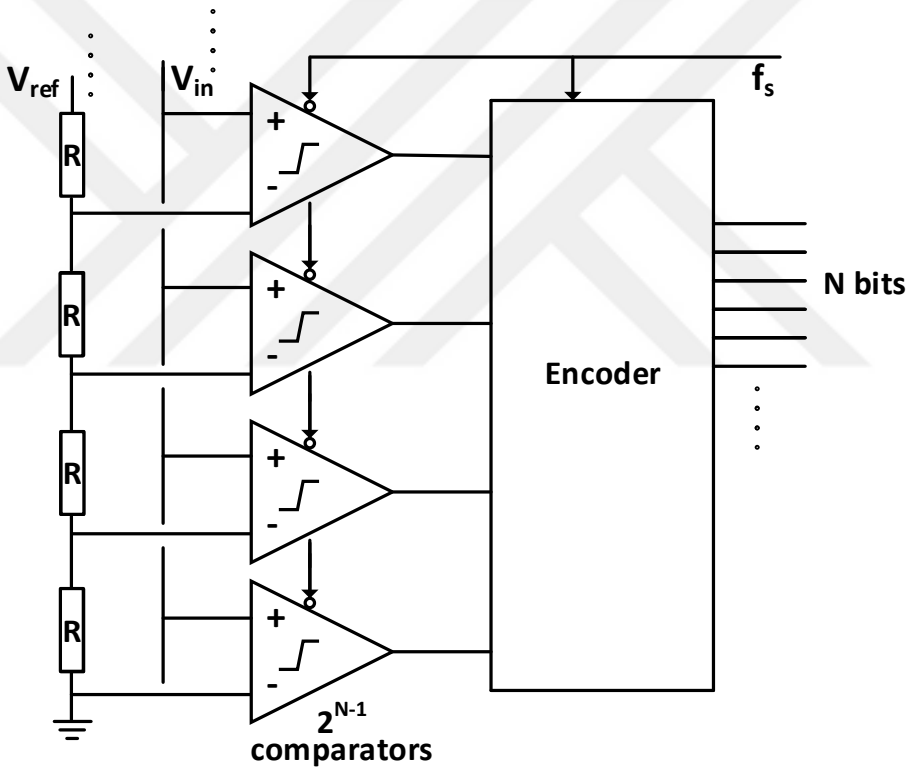


Figure 3: Generic Flash ADC Architecture

The design and complexity of a conventional flash ADC are quite simple. In addition to analog comparators, they need a reference block (usually a resistor ladder) to generate the 2^{N-1}comparison reference voltages and a conversion logic to produce a binary output from the 2^{N-1} comparator decisions which form a thermometer code as is. As such, the conversion time does not change significantly with increased resolution. Although this is the fastest ADC architecture inherently due to parallel

approach, the resolution is constrained heavily as the number of comparators scale exponentially with resolution. The excessive input capacitance, large power consumption and large silicon footprint limits this architecture to low resolution, high bandwidth applications. The matching between the 2^{N-1} comparators also directly affect the static performance and the linearity of the ADC. This often necessitates a calibration scheme to enhance accuracy. Similarly, matching and the metastability (due to imperfect settling or comparator timing mismatch) in the comparators can cause sparkle codes which require some modification to the conventional thermometer encoding blocks, usually some form of error correction or Gray coding which exhibits a more benign response to sparkle errors.

Besides, even if the comparators were to be matched in the process, the flash ADC inherently presents a nonlinear input impedance depending on the input level which introduces nonlinearities in the output. This is because a high input signal increases the input capacitance of the comparators it interfaces with, due to increased gate-source capacitances. Meanwhile, lower level signals see less input capacitance as they are not high enough to increase the source-gate capacitances of the transistors they are applied to. Furthermore, since each comparator has a different common mode in its input (as they have a fixed input from the V_{in} but varying references from the resistor string), they each will have different offset voltages, gains, C_{in} as these vary with common mode. A fully differential architecture can mitigate these effects, provide doubled V_{FS}, better common mode rejection. However, this adds the expense of more power consumption and more area to the already massive, exponentially scaling flash architecture. As such, feasible flash ADC designs are typically limited to 6-8 bits. Today, most of the state-of-the-art flash ADCs implement digital threshold calibration techniques to relax the matching requirements of the comparators, enabling low power comparators to be used [7].

1.3.2 Integrating ADCs

Integrating ADCs, also called dual-slope or multi-slope ADCs, inputs the incoming analog signal to an integrator and enables the integration to create a ramp signal. Single slope architecture and operation is shown in 4.

For a single slope architecture, the integrated voltage is then compared to a

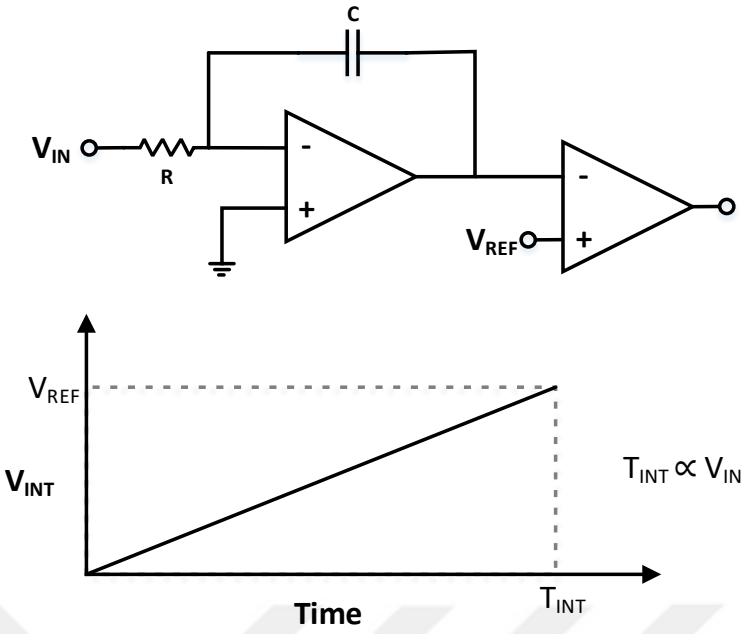


Figure 4: Single Slope Integrating ADC Architecture and Operation

reference voltage. Therefore, the time it takes to toggle the comparator decision is proportional to the average of the input signal, V_{IN}, over the integration period. So the input has to be sampled and held constant for the integration period. For a dual slope architecture, the corresponding integrated output voltage is integrated only for a fixed integration time, T_{INT}. Then, this voltage is returned to zero by applying a known opposite polarity reference voltage (V_{REF}) to the integrator. In this case, the ratio of V_{IN} to V_{REF} is proportional to the amount of time it takes to return to zero which is measured by a clocked counter. Compared to the single slope architecture, one significant advantage of this is that the conversion is not as affected by the integrator's R and C parasitics and variations as both the integrating up and integrating down phases use the same R and C. Errors caused by the offsets of the integrating amplifier and the comparator, and the gain error can be calibrated digitally by sparing cycles to measure the zero and the full-scale inputs. Overall, integrating ADCs can provide a high resolution, but they are among the slowest ADC converters due to the fact that an N bit integrating ADC takes 2^N clock cycles to count and complete its conversion.

1.3.3 Pipeline ADCs

Pipeline ADCs, consist of multiple cascaded ADC stages where each stage works on a few bits of the input sample concurrently. In other words, each stage carries out a coarse quantization, computes the residue left and relays it to the next stage. Each stage typically consists of a sample and hold circuit, a fast low-resolution flash ADC to quantize the incoming signal, a DAC to generate a reference voltage, a subtractor to determine the residue by taking the difference between the input and the reference and a residue amplifier to output the residue to the next stage. The general signal path and architecture for a pipeline ADC is shown in Fig. 5. The conversion process is essentially pipelined as the name suggests, as one stage can process the data from the previous stages at any phase of the sampling clock. One implication is that the bit results coming from the previous stages must be handled into a shift register so that digital output data is time-aligned. Indeed, unlike the flash ADC, the pipelined delay (latency) of pipelined ADCs scale with the number of stages. On the other hand, an advantage is that the throughput is set by the speed of a single stage.

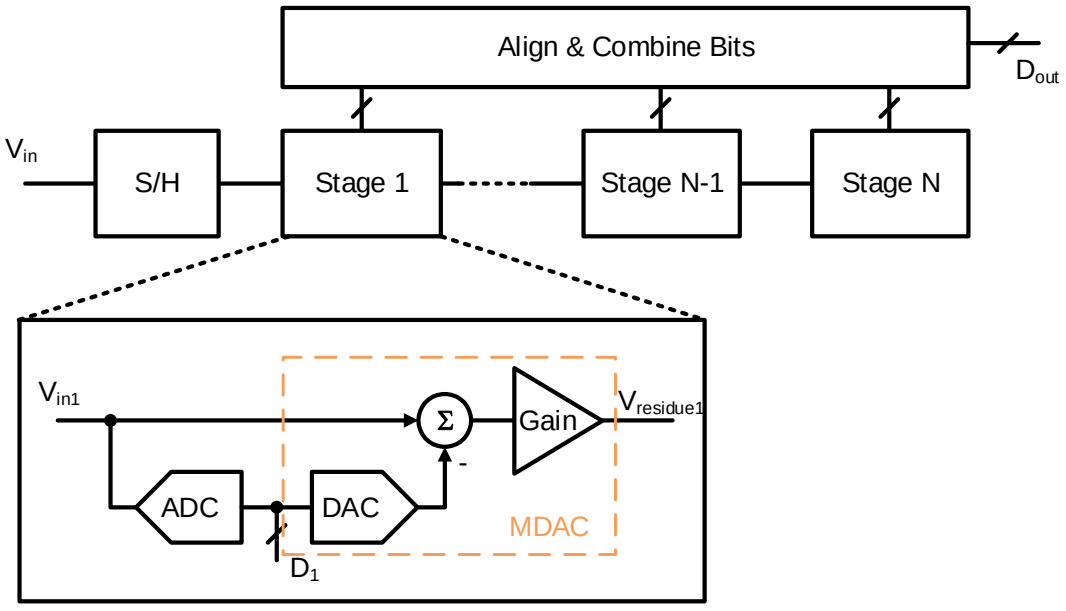


Figure 5: Pipeline ADC

Generally, multiplying-DAC (MDAC) circuits are used to implement each stage in a pipelined ADC. An MDAC performs most of the functions needed for the

pipelined ADC; the input sampling, using a DAC to get the voltage to subtract from the input, obtaining the residue (subtraction), amplification of the residue and holding it for next stage. Nowadays, most pipelined ADCs include digital error correction techniques that operate between the stages to account for the mismatch and nonlinearity in its analog components. Usually, pipelined ADCs are also branded as subranging ADCs which does not hold true always. Though most subranging ADCs can and do use pipelining to improve their throughput, not every implementation does so.

1.3.4 SAR ADCs

The SAR ADCs convert the analog input to its digital representation by a series of successive approximation steps using (typically) a binary search algorithm. It has only moderate speed on its own since successive approximation algorithm occurs serially. The binary search algorithm works by halving the search range and determining where the input lies in the range and updating the search range to that value. For the next cycle, the new range is once again halved, and the process iterates. Thus, an N bit SAR ADC requires at least N+1 cycles to complete one conversion. The architecture of the SAR ADC is shown in Fig. 6. It consists of a sample and hold circuit, a comparator, a DAC and a SAR control logic. The sample and hold circuit samples the input during the sampling phase and maintains its value during the conversion. The comparator regenerates the difference between the input voltage and the reference such that a decision can be given as digital '1' or '0'. The SAR control then registers the comparator decision and updates the DAC inputs such that the DAC now generates the new search range. The main advantage of SAR architectures is that they consume significantly lesser power compared to other architectures. It is possible to implement high speed, low-resolution converters that are not as power hungry as Flash ADCs in the SAR topology.

1.4 ADC Specifications

A plethora of specifications exist that describe different parameters of an ADC. As noted in [11], the critical parameter to consider changes depending on the application of the ADC. For instance, automatic control applications require monotonicity

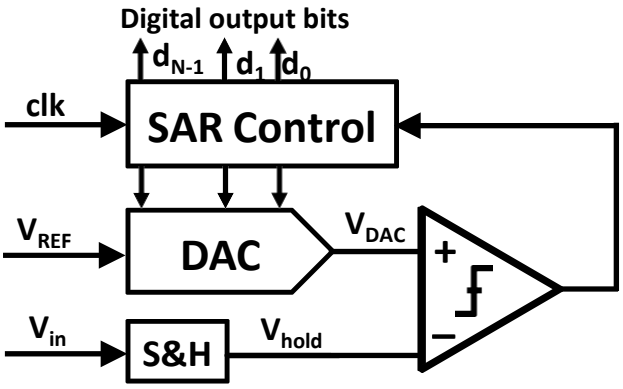


Figure 6: SAR ADC

and long-term stability; audio applications require good signal to noise and distortion ratio (SINAD) and good total harmonic distortion performance (THD). Data acquisition and digital oscilloscope type applications require wide bandwidth, low noise integrated over the bandwidth, short settling time, good SINAD and, as a consequence, good effective number of bits (ENOB). In this section and the following subsections, we give a standard yet not exhaustive definition of many ADC performance parameters for the uninitiated reader in order to define a framework for the evaluation of the ADC designed in this work.

1.4.1 Input Configuration and Range

The analog input signal to the ADC can be single-ended, differential or pseudo-differential. Single-ended signals are referenced to a common ground. Differential configuration is usually desired for the cancellation of common mode and even order harmonics and increased dynamic range. Pseudo-differential configuration also has two inputs, however, the input signals are not balanced in this case, and this offers smaller cancellation ability of common mode. There is also a fixed common mode range for the input as the ADC circuit performance can only be guaranteed for a certain input common mode range. Thus, the quantized signal range and its expected common mode is specified in terms of absolute volts. In this work, a differential ADC has been designed which quantizes a differential signal with range of 1V-0.5V with a fixed 0.75V common mode.

1.4.2 Resolution and Accuracy

Resolution of an ADC refers to a number of distinct levels the ADC is capable of producing and is shown by the output bits in an ADC. Quite often, the resolution and the accuracy of an ADC is confused and used interchangeably. However, the accuracy of an ADC actually specifies how correct the digital output bits are compared to the ideal digital output for a given input. That is to say; an N-bit ADC may not be N-bit accurate. In fact, it is often not N-bit accurate as the accuracy depends on the input frequency and amplitude, overall system noise, and linearity. For instance, in this work, the resolution is 6-bits while the accuracy is 5.9 bits.

1.4.3 Static Performance Parameters

Static performance parameters characterize the specifications of an ADC under DC or slowly varying signal conditions. These parameters can be extracted from the input-output transfer characteristics of an ADC.

1.4.3.1 Offset Error

The offset error is a shift of the ADC transfer characteristic. The offset is measured by finding the difference between the ideal first code transition point and the actual first code transition point, thus it actually tells the shift for the zero input. An example of an ideal ADC transfer characteristic and one with offset error is shown in Fig. 7. The offset error is usually described in LSBs, absolute volts or as a percent of the full-scale voltage.

1.4.3.2 Full-Scale Error

The full-scale error corresponds to the difference between the last code transition point and the ideal code transition point for an ADC.

1.4.3.3 Gain Error

Gain error is the difference in slope of the actual ADC transfer characteristic from the ideal ADC transfer characteristic as shown in Fig. 8. Generally, static gain errors can be calibrated out easily in the post-processing of the ADC. Similar

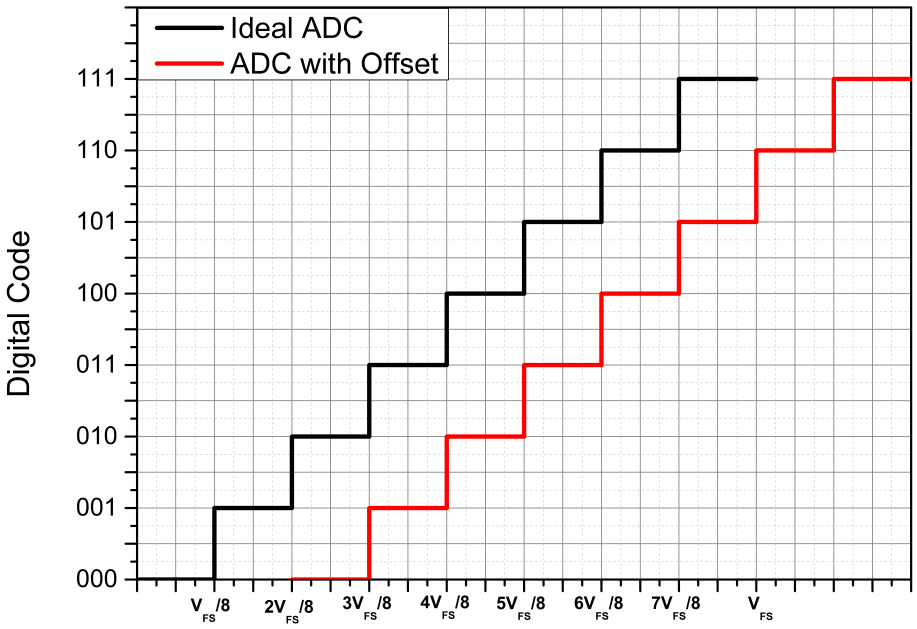


Figure 7: Ideal ADC and ADC with Offset Transfer Characteristics

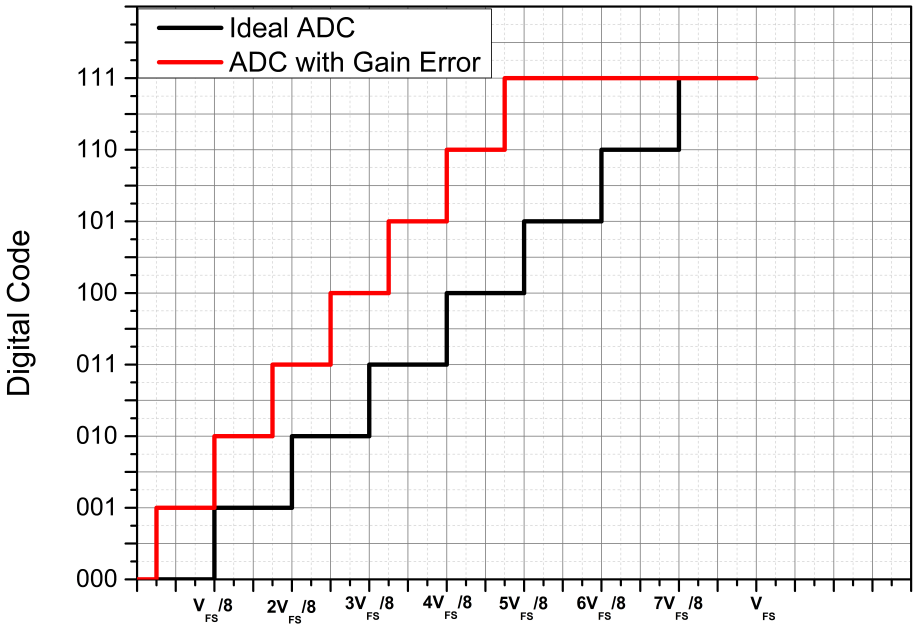


Figure 8: Ideal ADC and ADC with Gain Error Transfer Characteristics

to the offset error and the full-scale error it is expressed in LSBs or as a percent of the full-scale voltage. The offset and gain error can be factored out easily in the post-processing of ADCs. However, they present an issue in applications where a range of temperature compliance is required. As both the gain error and the offset error can have variations (expressed in ppm/°C) due to a change in ambient temperature, termed as gain error drift and offset error drift, respectively.

1.4.3.4 Differential Nonlinearity

Differential nonlinearity is one of the most important DC performance parameters as it relates the linearity of the code transitions of the converter. It is defined as the difference in code width of one LSB level from its corresponding ideal width. Ideally, a delta of 1 LSB in the digital code should correspond to exactly 1 LSB change of the analog signal. The DNL is measured for every single output code except for the first and the last codes after the offset error and the full-scale error are accounted for in the transfer characteristic.

1.4.3.5 Missing Codes

Normally, if the input voltage is swept across the whole ADC input range, all output codes should appear at the ADC output. Missing codes can be thought as an extreme case of the DNL error where the DNL is <-1 LSB for a code i.e., the actual code width is 0, meaning the code is missing from the transfer characteristic completely. A DNL error of < 1 LSB or > 1 LSB guarantees that there will not be any missing codes.

1.4.3.6 Integral Nonlinearity

The integral nonlinearity is the maximum deviation between the actual ADC output transfer characteristic and the ideal one. The deviation is measured with respect to a straight line that can be either the best fit line that minimizes the deviations or an end-point line which is drawn between the end points of the ADC transfer characteristic. Similarly to DNL, INL is calculated after offset and gain errors are accounted for in the transfer characteristic, i.e. best-fit line or end-of-points line is drawn after offset and gain are removed from the transfer characteristic.

Generally, the second method of end-point linearity is used as it is hard to objectively compare the INL resulting from the first method and this method leads to a simple summation of DNL errors to find the INL.

1.4.4 Dynamic Performance Parameters

While static performance parameters provide information on how the ADC responds to specific slowly-varying or DC inputs, dynamic performance parameters provide an understanding of the AC performance of the ADC i.e., how the ADC responds to a full-scale, time varying signal. In this section, we present a brief description of the dynamic performance parameters used throughout the industry and academia in characterizing the ADC. Readers should note that, for the sake of brevity, only some of these parameters are described in this thesis. For a more complete treatment, the readers are advised to study the works in [7], [8], and[12].

1.4.4.1 Signal-to-Noise Ratio

The Signal-to-Noise Ratio (SNR) is defined as the ratio between the power levels of the input signal and the noise. It is expressed in dB and given by:

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right)(dB) \tag{15}$$

where P_{signal} is the RMS signal power, and P_{noise} is the RMS noise power.

1.4.4.2 SNDR

The signal to noise and distortion ratio, following from the SNR, is defined as the ratio of the signal power to the total noise and distortion power at the output for a single tone input.

$$SNR = 20\log\left(\frac{P_{signal}}{P_{noise} + P_{harmonics}}\right)(dB) \tag{16}$$

or in RMS voltage levels,

$$SNR = 10\log\left(\frac{V_{signal}}{V_{noise} + V_{harmonics}}\right)(dB) \tag{17}$$

Distortion is defined as signal dependent nonlinearities that lower the signal quality. For a perfectly linear ADC, the SNDR would be equal to SNR. Circuit nonlinearities result in in-band harmonics at the output and degrade the SNDR. $V_{harmonics}$ is the RMS voltage level of the in-band harmonics in 17.

1.4.4.3 Effective Number of Bits

One precise way to characterize the dynamic performance of ADCs is to use effective number of bits (ENOB) which defines the equivalent resolution corresponding to that SNDR performance at a specific input frequency and sampling rate. The relation definition is extracted from the SNDR of an ideal ADC for a full-scale, sinusoidal input wave as shown in 18. Readers should recall that we have derived this formula in Chapter 1 while discussing the quantization noise.

$$ENOB = \frac{SNDR\,(in\ dB) - 1.76}{6.02} \tag{18}$$

The actual SNDR values of ADCs are below the ideal, full-scale sinusoidal case. For Nyquist ADCs, the ENOB is always smaller than the actual resolution. Meanwhile oversampling ADCs can boost their effective resolutions by increasing their oversampling ratio and ENOB can be much greater than the nominal resolution of the ADC as was noted in the quantization noise section of this thesis.

1.4.4.4 SFDR

Spurious Free Dynamic Range (SFDR), expressed in dB, is the ratio of the RMS value of the input signal to the RMS value of the worst spur regardless of where it falls in the spectrum. As a result, the SFDR is always better than the SNDR in an ADC as it only takes the worst spur in the denominator compared to SNDR which takes every artifact that's not the signal itself. Though the worst spur is generally a harmonic of the signal, it may not be so necessarily in the presence of interferers. In addition, in determining the worst spur component, the DC frequency bin is excluded as it just manifests as DC offset and can be removed easily.

1.4.4.5 Total Harmonic Distortion

Similar to SFDR, this is a measure of the distortion of the ADC. Every real-world ADC has some nonlinearity and, therefore, distortion on the output. Total harmonic distortion (THD) is defined as the power ratio of the single input tone (fundamental frequency) in the output signal to the sum of the harmonics of the input tone in the output signal of the ADC. Usually, the first five harmonics are taken as the sum in the literature. This is because generally as we go towards higher harmonic frequency components, their amplitude reduces. Hence, it is enough to consider only the first few harmonic components when looking at the distortion of an ADC. Typically, only harmonics within the Nyquist bandwidth are included in the measurement of THD. The THD can be calculated from:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + ... + V_n^2}}{V_1} \, dB \tag{19}$$

where the V_n is the RMS voltage of the nth harmonic and $n = 1$ is the fundamental frequency.

1.4.5 Figure of Merits

As noted in the previous sections, there are quite a lot of ADC performance parameters for an ADC that characterize different specifications which change in importance depending on the application. Assessing an ADC's performance without regard to different architectures and different specifications is not trivial. Consequently, there has been a lot of different figure of merits used in the literature to establish a single number that can be used to compare the performance of ADCs. In this section, the two most frequently used figures of merit, namely the Walden Figure of Merit and Schreier Figure of Merit, as well as recently used figures of merit are discussed.

1.4.5.1 Walden Figure of Merit

The Walden Figure of Merit (FoM_W), proposed in [13], tries to present the fundamental circuit design trade off of speed, power, resolution in its FoM. The

FoM_W is given as

$$FoM_W = \frac{P}{2f_{sig}2^{ENOB}} \tag{20}$$

where f_{sig} is the input signal frequency for which the ENOB is defined, and P is the total power consumption. The FoM_W gives the energy spent per conversion step for an ADC.

There are some limitations in the use of this metric as it was first adopted by Walden based on empirical data. According to FoM_W, each extra bit added should result in doubling the power at the same efficiency of the ADC. However, in an ADC where the system is limited by the thermal noise of $\sqrt{kT/C}$, an increase in the bit resolution requires 6dB SNR improvement. Thus, C has to quadruple to achieve this noise reduction and subsequent SNDR improvement. If the operating frequency and efficiency (read: FoM) is held constant, then the power consumption has to increase by a factor of four [14]. This factor of four tradeoff is not reflected honestly by the Walden FoM. Thus, to address this shortcoming, the Schreier Figure of Merit, explained below, has proven favorable. Nevertheless, both of the metrics are used quite heavily in the literature.

1.4.5.2 Schreier Figure of Merit

The Schreier Figure of Merit is shown in (21). As better SNR performance requires proportionally lower noise and proportionally lower thermal kT/C noise requires higher capacitances, the power consumed in the capacitors are proportionally higher. Thus, better SNR can be scaled with proportional power increase, and FoM_S stays constant. Of course, this FoM provides a useful comparison scale when the ADCs at hand are thermal noise-limited, and other noise sources are not dominant contributors.

$$FoM_S = 10\ log\frac{SNR\ \times\ BW}{P_{ADC}} = SNR\ (in\ dB) + 10\ log\frac{BW}{P_{ADC}} \tag{21}$$

Theoretical maximum of this figure of merit is interesting to consider. In [7], the minimum signal power level needed to overcome only thermal noise with a certain SNR is given as in (22).

$$P_{sig,min} = 4kT \ \times BW \times SNR \tag{22}$$

If we assume this minimum signal power needed to overcome the thermal noise floor as our ADC power consumption (which is a terribly idealistic assumption), we get FoM_S = 197.84 dB at 20° C.

Since distortion components are also ignored in SNR, some variants of the FoM_S use SNDR instead of SNR or DR. The Schreier FoM for dynamic range (DR) is [9]

$$FoM_S = DR \ \ (in \ dB) + 10 \ log \frac{BW}{P_{ADC}} \tag{23}$$

and the one with SNDR proposed by [15] is given as

$$FoM_S = SNDR \ \ (in \ dB) + 10 \ log \frac{f_s/2}{P_{ADC}} \tag{24}$$

The recent FoM_W and FoM_S performance of ADCs are given below. In Fig. 9, the FoM_W vs. sampling frequency of all ADCs published in the IEEE Symposium on Very Large Scale Integrated Circuits (VLSIC) from 1977 to 2017 are given and in Fig. 24, the same analysis is given for all ADCs published in the IEEE International Solid-State Circuits Conference (ISSCC) from 1977 to 2017. The data is obtained from the Murmann ADC survey[1]. Indeed, it seems that we are getting very close to the theoretical maximum of the FoM_S for lower frequencies. Expectedly, the performance rolls off as we go towards higher operating speeds, pushing towards lower power efficiencies for a given technology.

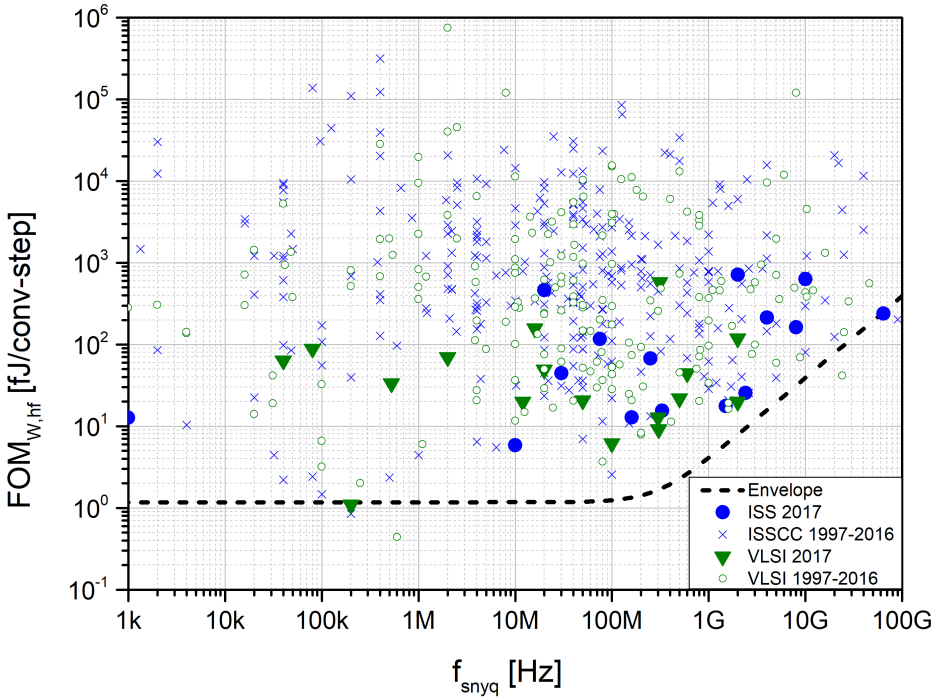


Figure 9: FoM_W for ADCs published in VLSIC and ISSCC from 1997 to 2017. Adapted from [1]

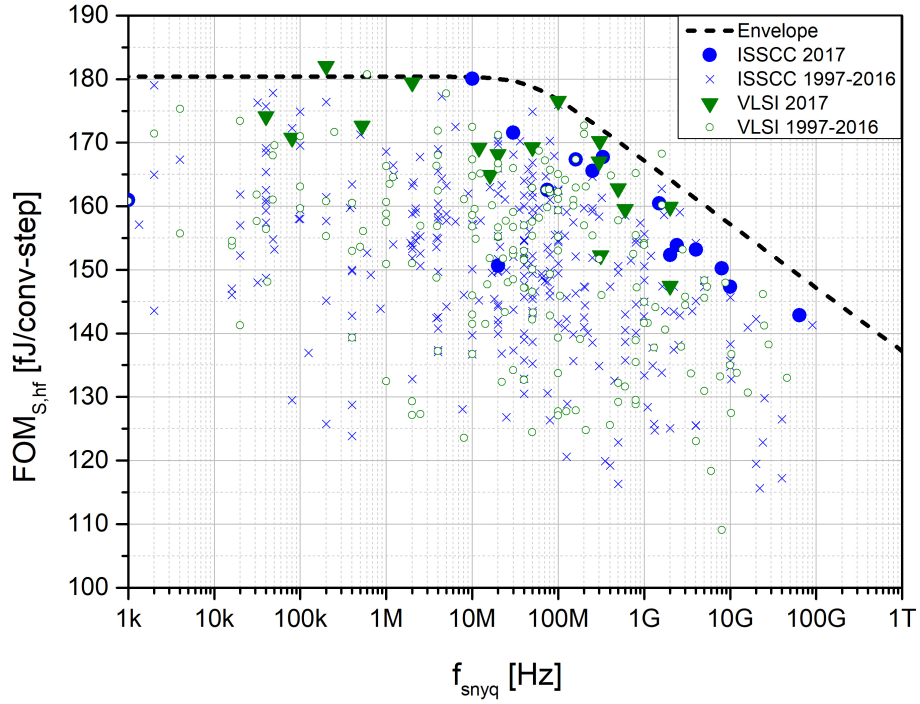


Figure 10: FoM_S for all ADCs published in VLSIC and ISSCC from 1997 to 2017. Adapted from [1].

1.5 Time-Interleaving

Time-interleaving is a technique that enables the use of multiple ADCs to process data in faster rate than the individual operating sampling rate of each sub-ADC. An individual ADC samples the incoming data on the rising or falling edge of the clock. By using two ADCs that are using exactly 180° out of phase clocks (CK_1 and CK_2 in Fig. 24), the overall sampling rate can be effectively doubled.

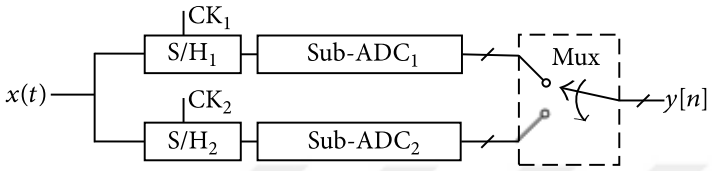


Figure 11: Time-interleaving

In fact, this technique can be generalized to N sub-ADCs with their own samplers to operate at N*f_s speeds. However, this N is quite limited even in theory; the speed increase is only a given in the case when the samplers, S/H_1, S/H_2, ... , S/HN are not the bottleneck in the system. Indeed, the amount that the time-interleaving technique adds to the conversion rate depends on the relative operation speed of the quantizer (ADC) and the sampler. Normally, the quantization process is long, so time-interleaving can be employed, but the maximum number of channels is determined ultimately by the sampler. The sampler has to work at N*f_s to be able to capture the signal correctly, unlike the sub-ADCs.

Time-interleaving technique offers more than just simply an increase in the speed, it also offers a way to achieve an optimum efficiency point for a given ADC by providing flexibility in the power-speed trade-off. It is possible to get a faster and more power efficient ADC by time-interleaving many sub-ADCs instead of designing one main ADC that satisfies the same sampling and operation speed. This is because as we approach the limits of a single ADCs speed in a given technology node, it takes substantially more power to increase the speed further, a typical case of diminishing returns. It is more power efficient to interleave moderately fast ADCs to achieve high operation rate instead of insisting on pushing the limits of a technology node. The power saving can also come from the clock distribution network as compared

to a single ADC that works at N*f_s if the clocked transistor sizes are scaled down by N in the interleaved design. This can be done to allow the settling times to increase by N as now each ADC has to be only 1/N fast. Scaling down the transistor sizes by N will also reduce their gate capacitance by N and the power consumed driving the clock into these gates will reduce.

1.5.0.1 Time-Interleaving Considerations

Time-interleaving is a powerful technique, however, it also has its practical limits on how many channels can be interleaved before it no longer returns a significant improvement. The non-overlapping clock generation for each channel and the distribution of that clock requires complex design for the routing and interconnects depending on the timing mismatch that can be tolerated. In addition, kT/C noise forces a lower limit to the sampling capacitor for each channel and interleaving increases the input capacitance. Thus, the circuit that will drive the ADC has much less SNR to work with compared to a single ADC implementation. The driver FoM for different resolutions and how it degrades with respect to the time-interleaving effects are given in [16].

For a non-interleaved single channel ADC offset, gain and timing are not that stringent as long as it is constant or exhibits low drift during its operation, SNDR, INL, DNL will be affected minimally. However, in a time-interleaved architecture, the differences between timing, gain, bandwidth and offset between the channels lead to spurious tones in the output [17] [18]. Ideally, if all of the channels were to be matched perfectly, then one could extend the time-interleaving to N channels easily, provided that sample and hold circuits still satisfy the required bandwidth. However, the reality is not so sweet. In practice, the channels will differ due to process, voltage, temperature (PVT) variations and systematic layout issues as it is hard to realize a completely symmetric channel pattern in a planar (2-D) design. Thus, this will degrade and distort the output signal. For instance, different DC offsets between the channels will result in an output pattern that repeats with N*T_s i.e., spurs will appear at f_s/N. Similarly, random gain differences between the channels, the gain mismatch, or the timing differences between the channels, the timing mismatch, will both result in spurs at $f_s/N \pm f_{in}$. In addition, the bandwidth mis-

match between the channels will also contribute towards performance degradation. A number of methods have been proposed to correct the gain and offset mismatch digitally and reduce timing mismatch and bandwidth mismatch problems. For a detailed overview, the readers are referred to [19] for a complete treatment of the interleaving errors and their calibrations. In this work, our focus was on the design of a fast sub-ADC so a calibration scheme was left out of the design, however, single channel, two channel time-interleaved, and four channel time-interleaved ADCs were designed in the case four channel time interleaving required a significant calibration.

1.6 Organization

The remainder of this thesis is organized as follows. Chapter 2 goes into introducing the SAR architecture and discusses the recent developments and the renewed interest in SAR ADC research. It is shown that SAR architectures typically achieve best power efficiencies among all ADC architectures in low-to-medium resolution architectures and, thus, are a prime candidate for time-interleaving many sub-ADCs to extend the operation speed to even higher bandwidths.

Chapter 3 describes the design process of the implemented TI-SAR ADC organized by its sub-blocks. Each of the sub-blocks operation and design are explained in this section.

Chapter 4 presents the simulation methodology and simulation results of the TI-SAR ADC implemented in this work and provides a comparison with similar works. The measurement results of the single channel ADC is also given. The TI-SAR ADC have yet to be measured as of the writing time of this thesis.

Chapter 5 concludes the thesis with a summary of the work and some additional discussion on possible future work to address the current shortcomings of the implemented ADC.

2 SAR ADCs

2.1 History of SAR ADCs and the SAR Algorithm

The now widely known binary search algorithm used in modern SAR ADCs can be attributed to the Bachet's Weights Problem [2] in the 17^{th} century. Bachet poses the following puzzle; how do you determine the least number of weights which are enough to weigh any integral number of pounds from 1 lb. to 40lbs? The solution, [20] proposed by Tartaglia in 1556, is using series of weights 1, 2, 4, 8, 16, 32 lbs to accomplish the task. In fact, this combination can weigh unknown weights more than 40 lbs up to 63 lbs. An example of weighing 45 lbs is shown in Fig. 12.The first comparison is made against the 32lbs weight, and if the unknown weight is greater, the 32 lbs weight is retained and the second weight of 16lbs is added to the next comparison otherwise 32 lbs is rejected, and next comparison is made with 16 lbs. This is the same decision algorithm used by the modern SAR ADCs.

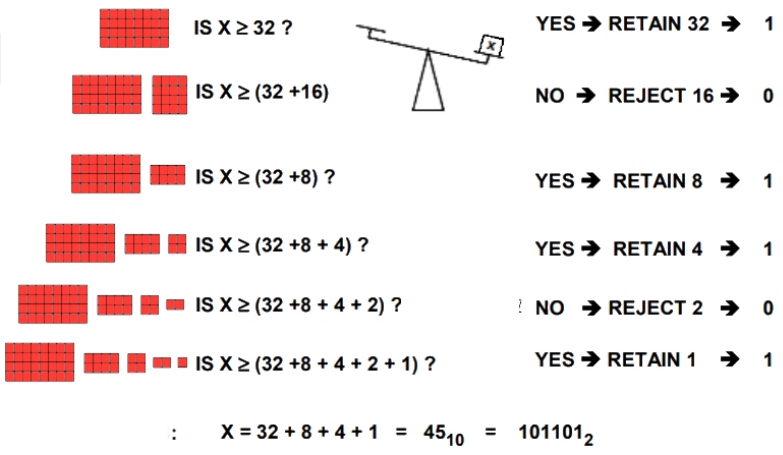


Figure 12: Bachet's Weights Problem [2]

The earliest ADC implementations are based on successive approximation are from the 1940s [21] [22]. In [22], a successive approximation ADC based on vacuum tube technology and the description of a binary DAC was made. However, in this work instead of a DAC to generate the required reference, binary switched voltage references were used. In [21], a 5 bit ADC employing successive approximation for converting audio signals into pulse code modulation outputs with 8 kSPS rate is described. It required 5 internal reference voltages, and a capacitor's charge was added or subtracted from depending on the comparison to a reference voltage.

The first commercial ADC, which was also used successive approximation, was the Epsco Engineering (now, Analogic, Inc.) "DATRAC" converter based on the pioneering work of B. M. Gordon in vacuum-tube techonology [2]. Introduced in 1954 and , it was a 11-bit 50 kSps SAR ADC that consumed 500 watts, weighted about 70 kgs and was sold for US$ 8000-9000[**?**].It also featured a sample-and-hold function and shift-programmable successive approximation architecture. The SAR logic used in this product was filed for a patent by Gordon in 1958 [23].In particular, the SAR control register function was later implemented as integrated logic chips by National Semiconductor and Advanced Micro Devices in the 1970s which were used on implementations of the SAR ADCs of the 1970s and 1980s from then on. Today, in many modern applications SAR ADCs have become the architecture of choice pushing the boundaries for energy efficiency in ADC architectures. In addition, although they implement a serial search algorithm, the architecture's compatibility with CMOS scaling has pushed the SAR ADC to a stand-out choice for time-interleaving architectures [24].

2.2 The SAR Architecture

Fig. 13 depicts a typical block diagram of a conventional SAR ADC. The SAR ADC is composed of a sample and hold circuit, a DAC, comparator and SAR control. The sample and hold is tasked with sampling the continuous input signal and holding the value for the rest of the conversion process. Then, the comparator compares the sampled input voltage V_{in} with V_{DAC}, the output of the DAC, and produces each bit according to the decision. The SAR control logic updates the DAC with respect to the decision made and this process continues successively. As mentioned previously, an N bit SAR ADC requires at least N+1 clock cycles, N comparison cycles for 1 bit per cycle and 1 cycle devoted to S/H function. As such in the SAR architecture, the resolution directly trades off with the sampling rate.

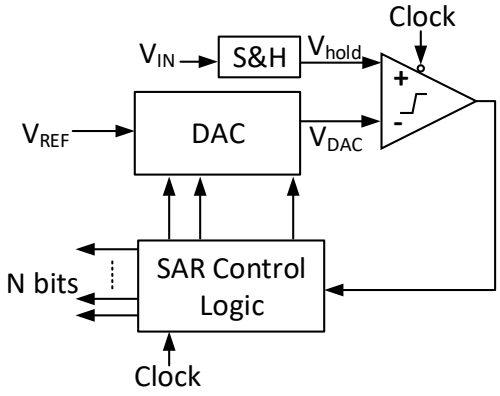


Figure 13: The SAR Architecture

2.3 Capacitive DACs

Capacitor arrays have been the most popular and effective architecture to implement the DAC as in SAR ADCs since the advent of integrated SAR ADCs as they can perform sampling and use charge redistribution (CR) or charge sharing (CS) to achieve fast and low power operation [25] [26]. However, resistor based DACs such as R-2R ladder DACs, tapped resistor string DACs and hybrid capacitor resistor DACs also exist as not as much power efficient alternatives. In this thesis, we shall refer to the output node of the DAC and the plates of the capacitors that are connected to the comparator as the top plates of the capacitors as is the convention.

2.3.1 Operating Principles of Capacitive DAC Switching Schemes

Switching schemes refer to the organization of capacitors and switches and their switching sequences in a DAC. The switching scheme of a DAC determines its energy efficiency, values of the capacitors and therefore, its size on chip. Since the advent of the CR-based ADC in [25], there has been a development of a multitude of novel switching schemes that aim to reduce the DAC capacitance and power consumption. In this section, we will cover the basic principle behind CR and CS schemes and go in detail on some of the most popular CR-schemes used in SAR ADCs today. In particular, we will also analyze the switching scheme used in this work, also known as the V_{CM}-based switching scheme.

2.3.1.1 Charge Redistribution Principle

In charge redistribution, the output of the DAC is set by switching the bottom plates of the capacitor array in a sequence according to the each step of the SAR algorithm. An example CR architecture is shown in Fig. 14. The CR principle can be stated as follows. Since there is no current path on the top plates, the total charge is conserved on the top plates irrespective of the capacitor switching. However, by switching to another voltage, the voltage level on this node can be shifted according to the SAR sequence by employing binary weighted capacitors. Since there is no current path on the top plates, the total charge is conserved on the top plates irrespective of the capacitor switching. However, since total capacitance to ground changes based on the switching events, the voltage level on this node can be set according to the SAR sequence.

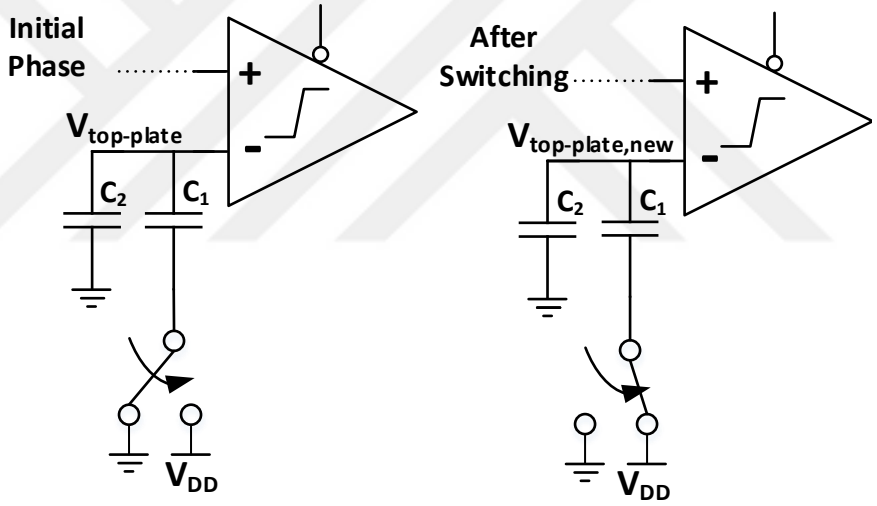


Figure 14: Charge Redistribution Operation

The analysis of the CR principle in Fig. 14 is derived as follows. Before the switching occurs, the total charge on the top plate, $Q_{top\text{-}plate}$ is given by

$$Q_{top-plate} = V_{top-plate}(C_1 + C_2) \tag{25}$$

When the switch is switched to V_{DD}, the total charge can be written as

$$Q_{top-plate,new} = V_{top-plate,new}C_2 + (V_{top-plate,new} - V_{DD})C_1 \tag{26}$$

Since CR principle holds

$$Q_{top-plate,new} = Q_{top-plate} \tag{27}$$

Then, we can find the new voltage, $V_{top\text{-}plate,new}$

$$V_{top-plate,new} = V_{top-plate} + V_{DD}\frac{C_1}{C_1 + C_2} \tag{28}$$

2.3.1.2 Charge Sharing Principle

In CS, the output of the DAC is set by switching precharged capacitors to the DAC nodes. Once again, there is no current path to the top plate node in the switching phase. Thus, voltage change is provided by the total charge on the connected capacitors divided by the new total capacitance of the connected capacitors. bottom plates of the capacitor array. An example is depicted in 15 and the analysis is given as follows. Initially, the switch S_1 connects C_1 to V_{DD} to precharge it. Before the switch changes state to share C_1's charge, total charge of each capacitor is given by Q_1 and Q_2 as:

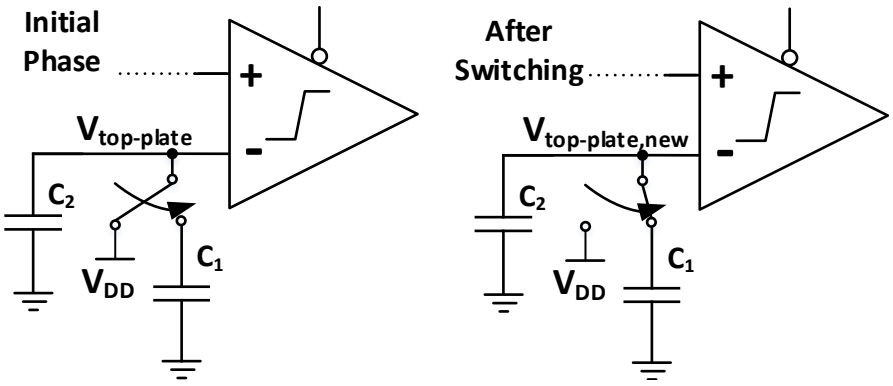


Figure 15: Charge Sharing Operation

$$Q_1 = (C_1)V_{DD} \tag{29}$$

$$Q_2 = (C_2)V_{top-plate} \tag{30}$$

After the switch connects C_1 to the top plate node, the new top plate charge,

$Q_{\text{top-plate,new}}$, is given by

$$Q_{top-plate,new} = V_{top-plate,new}(C_1 + C_2) \tag{31}$$

and due to charge conservation

$$Q_{top-plate,new} = Q_1 + Q_2 \tag{32}$$

Then, the new voltage on the top plate, $V_{\text{top-plate,new}}$ is

$$V_{top-plate,new} = \frac{C_1 V_1 + C_2 V_{top-plate}}{C1 + C2} \tag{33}$$

Compared to CR-based DACs, CS-based DACs are not used to perform the sampling operation. We will not review the CS-based architectures in this thesis for the sake of brevity. To briefly state a comparison, CS-based architectures have higher energy efficiencies and the energy consumed is constant for every code. Meanwhile CR architectures, to be studied in the following section, have their switching energy dependent on the output code. The DAC capacitance for best CS-based architectures can reduce to 1/16 of the conventional CR-based schemes while the best CR-based architectures can reduce to 1/4 of the conventional CR-based scheme. Of course, as just mentioned, only for the CR-based architectures the input capacitance of the DAC is equal to total capacitance of the DAC as S&H is featured in the architecture. For the CS-based architectures, a seperate S&H that increases area is needed. Furthermore, in CS-based schemes the DAC capacitance is dynamically changed as we switch in extra capacitances to the output node. Thus, we have more strict requirements on the comparator noise and performance that interfaces with the CS-based DAC.

2.3.2 A Summary of Charge Redistribution Schemes

In this section, we will give a review of the some of the most popular CR-based switching schemes today and explain their operation and present a comparison for the reader. For the ease of analysis and brevity, we will only give the operation of 3-bit DACs. However, scaling the analysis is trivial.

2.3.2.1 Conventional Switching

The conventional SAR switching scheme is shown in Fig. 16 for a differential 3-bit implementation. The switching scheme is given with the switching energy consumed for each cycle. As shown, the conventional switching scheme starts with bottom plate sampling in the sampling phase. The inputs are connected to the bottom plates while the V_{CM} is connected to the top plates. After sampling phase, conversion and switching phase starts and the MSB capacitor is connected to V_{REF} and the rest of the binary weighted capacitors are connected to ground. Similarly, the reverse is done for the bottom branch. Depending on the comparator decision, the switching algorithm and energy consumed follow as shown in Fig. 16. This is the most basic and least energy efficient switching scheme available for CR schemes. There has been much improvement on this conventional scheme in the literature over the years most of which we explain in this thesis.

2.3.2.2 Monotonic Switching

Proposed by Liu et al in [27], the monotonic swithcing scheme is shown in Fig. 17. The main goal of the switching is to only use discharging cycles while switching. Thus, it increases the efficiency of the switching scheme as compared to the conventional switching scheme. In addition, the top plate sampling enables the first comparison to be directly made between V_{inp} and V_{inn} inputs as it is sampled on to the DAC output node. This enables the design to remove the MSB capacitor of 2^N C, reducing the total capacitance and increasing the settling speed significantly. The operation is as follows. In the sampling phase, the differential inputs are sampled on the top plates of the arrays with bottom plates connected to the V_{REF}. The MSB is immediately resolved by the comparator. If the MSB is 1, the MSB capacitor from the more positive node (in this case, the top array) is switched to ground. If it is 0, the bottom array's MSB capacitor is switched to ground. This process iterates for each bit reducing the top and bottom arrays' top plate voltage difference i.e., the differential input to the comparator, to zero. Hence, the common mode of the signal changes significantly from $\frac{V_{inp}+V_{inn}}{2}$ to 0. This is not desired as it is a well known fact that comparator offset depends on the common mode voltage of the inputs. A varying common mode voltage introduces nonlinearity which is especially

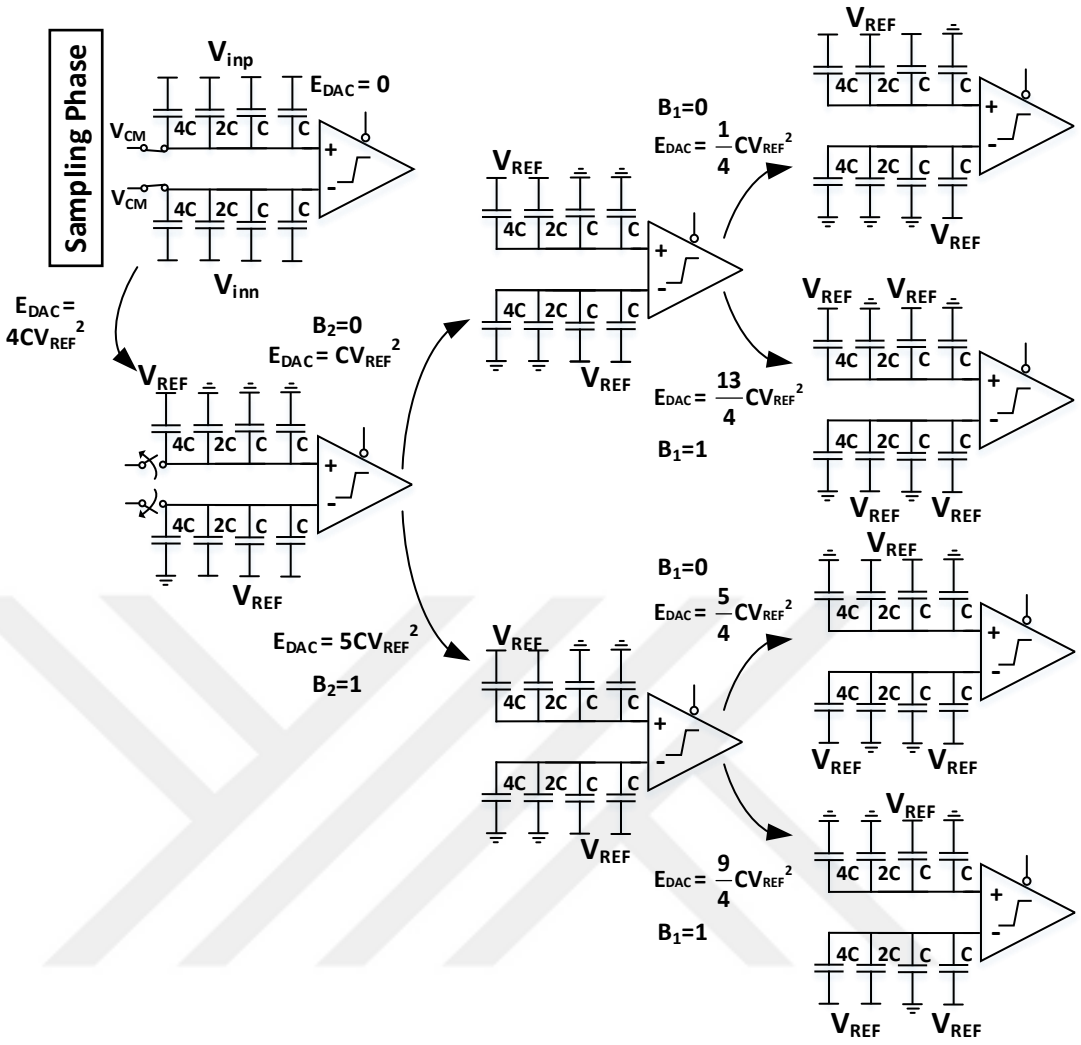


Figure 16: Conventional Switching Scheme

troublesome if the comparator offset cancellation is not implemented.

In order to solve this problem, the monotonic scheme in [3], shown in Fig. 18, decreases the common mode variation as follows. The signal is once again top-plate sampled but now bottom plates are connected to V_{CM} instead of V_{REF}. Following the MSB comparison, all bottom plates of the capacitor array with the lower voltage node i.e., if MSB is 1/0, the bottom array/top array, are switched to V_{REF}, respectively. This level shifts all the lower voltage nodes by 0.5 V_{REF} as V_{CM} is half of V_{REF}. Level-shifting does not consume any switching energy as per charge conservation rules. Then the monotonic switching scheme follows for V_{CM} to ground and for V_{REF} to V_{CM} depending on the decision. This switching scheme reduces the common mode variation by 50% compared to conventional monotonic switching. The common mode voltage of the DAC outputs approach to V_{CM} as the SAR sequence

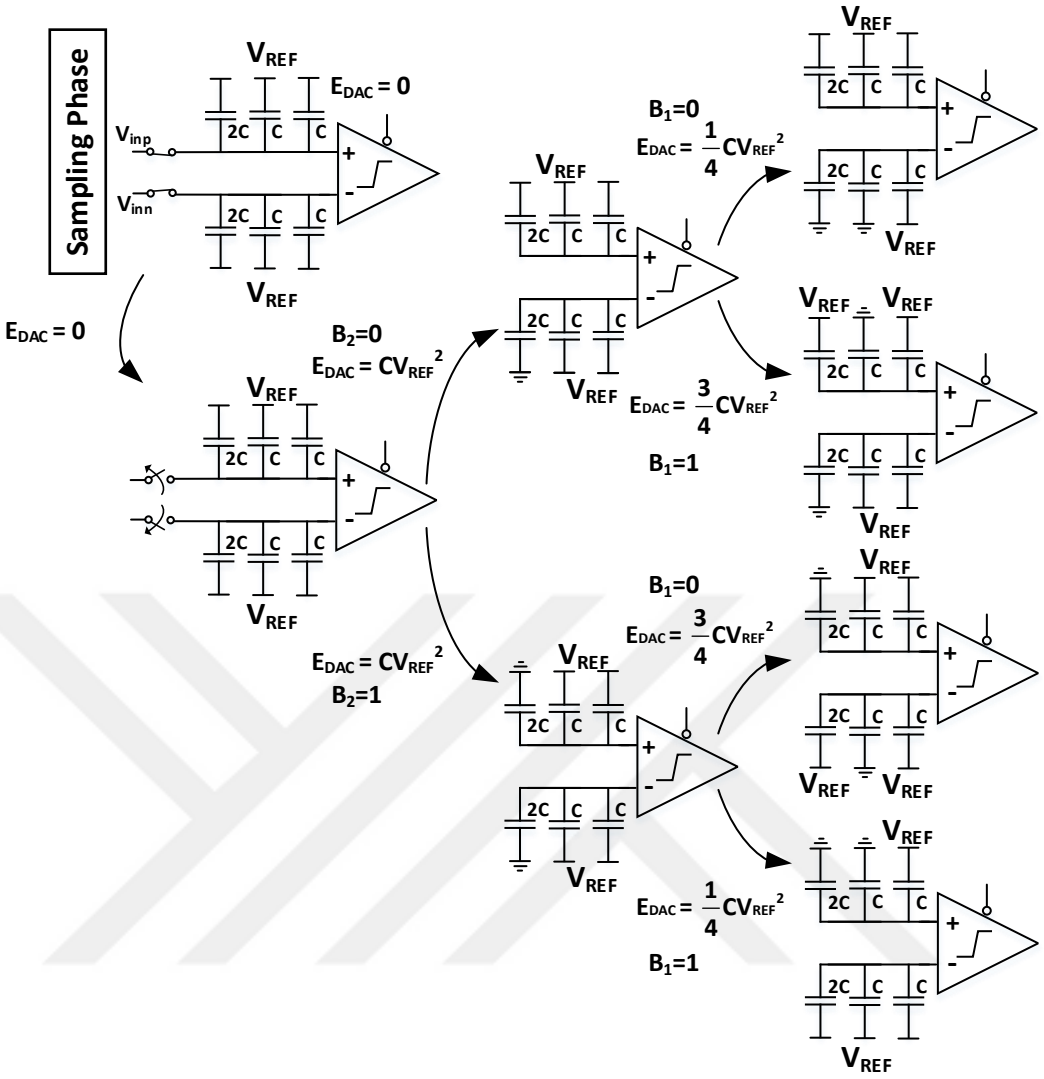


Figure 17: The Monotonic Switching Scheme

works. Furthermore, thanks to V_{CM} switching, the capacitor area is reduced by 50% compared to monotonic switching and by 75% compared to conventional switching. This scheme also reduces the switching energy significantly only at the expense of an accurate V_{CM} source (accuracy of which scales with resolution) and a tad more complicated SAR control logic.

2.3.2.3 V_{CM}-based Capacitor Switching Scheme

The V_{CM}-based capacitor switching scheme [28], also known as the merged capacitor switching (MCS) scheme [29], is depicted in Fig. 19. Similar to monotonic switching, this scheme also employs top plate sampling. As such, the first comparator decision occurs immediately after sampling. Depending on the comparator

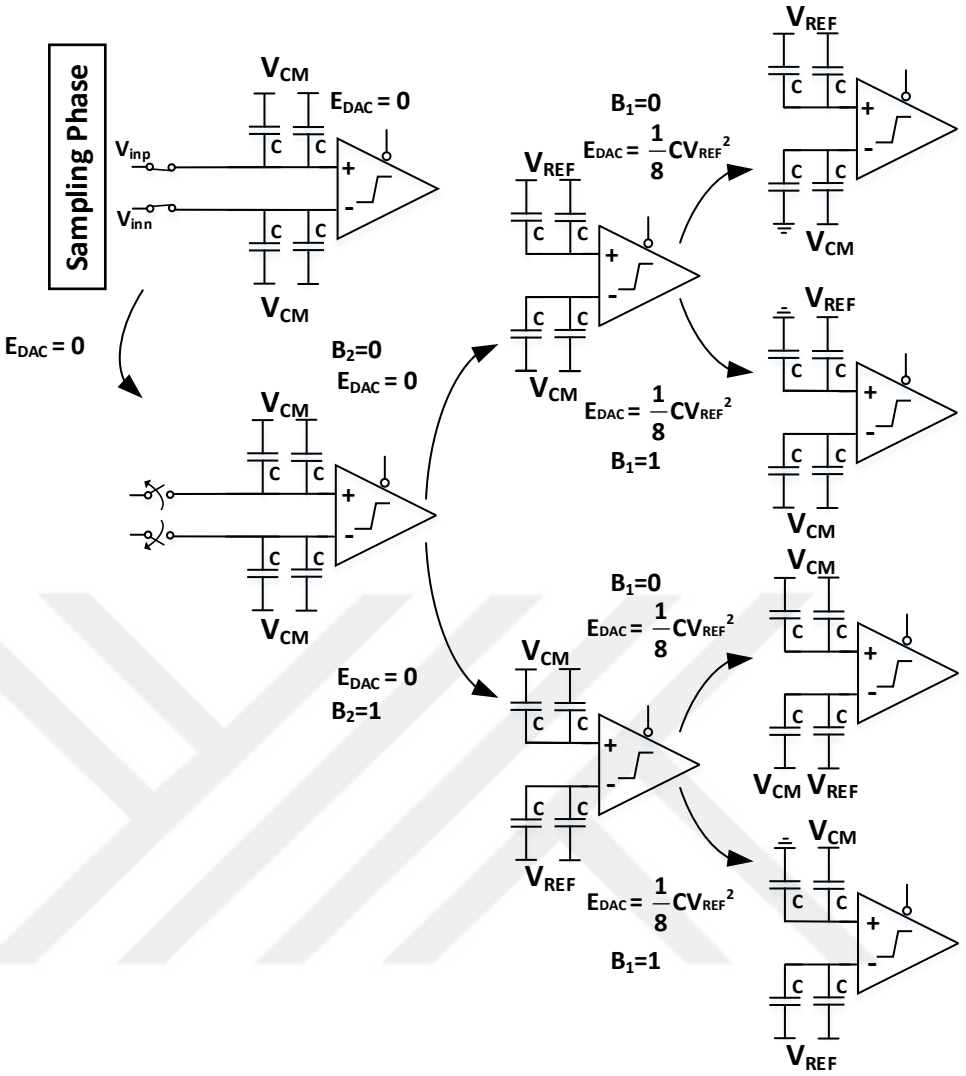


Figure 18: V_{CM}-based Monotonic Switching Scheme in [3]

decision of "1" or "0", **both** the MSB capacitors of the top array and bottom array are switched to ground/V_{REF} or V_{REF}/ground, respectively. Once again, similar to monotonic switching, V_{CM}-based switching achieves 50% reduction in capacitance compared to the conventional scheme. Even more switching energy reduction is achieved, however, thanks to changing voltages by only V_{REF}-V_{CM} instead of the whole VREF. In addition, this scheme keeps the common mode voltage constant (equal to V_{CM} throughout the entire conversion) which solves the problem of input dependent offset variation in the comparator. One advantage is that the linearity of the ADC is not sensitive to the accuracy of the V_{CM}.

In [4], an even more energy efficient V_{CM}-based switching scheme is described. The operation of the scheme is shown in Fig. 20. The main difference is that during

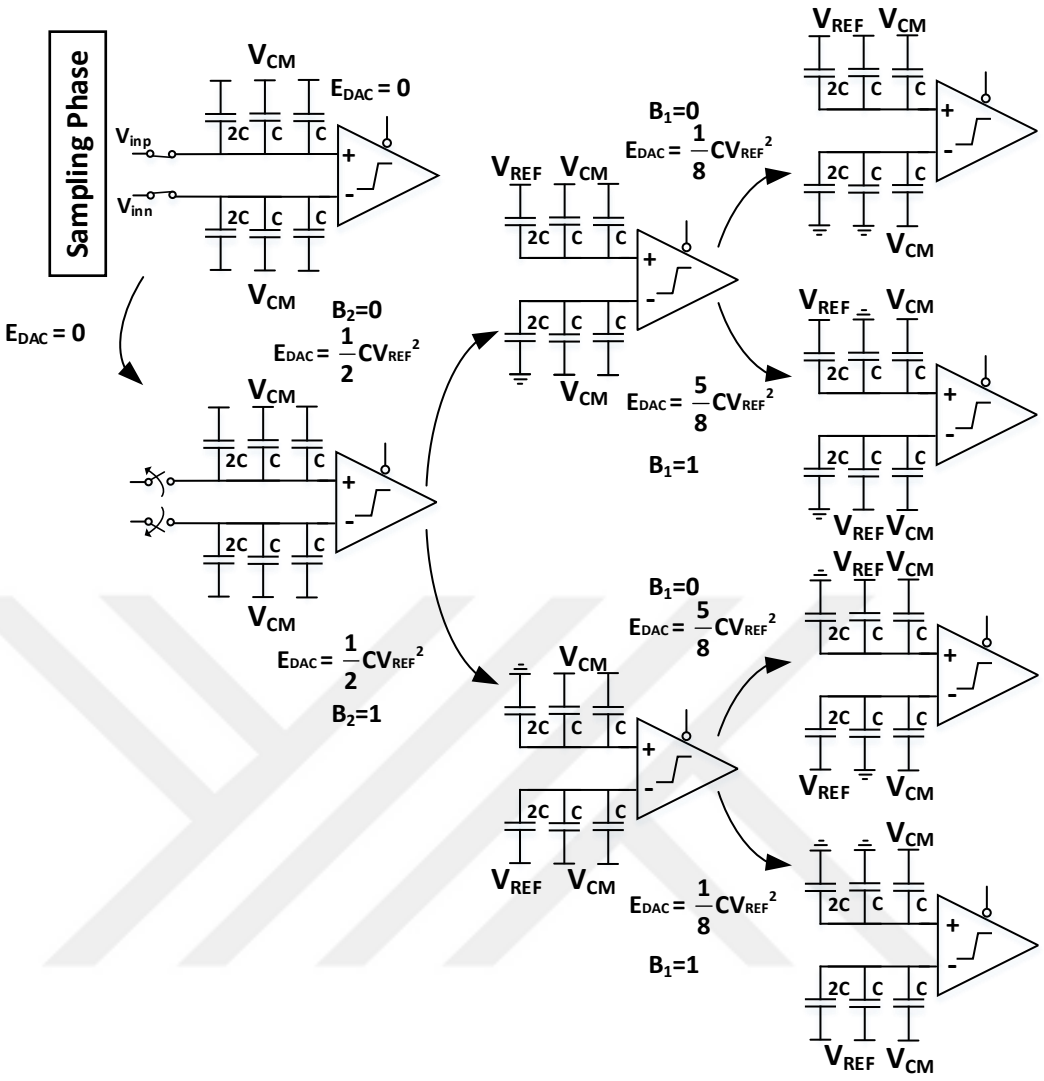


Figure 19: V_{CM}-based Capacitor Switching Scheme

the last cycle of the SAR algorithm, while determining the LSB, only one capacitor from the bottom or top arrays are switched instead of both them which leads to more energy savings.

2.3.2.4 Tri-level Switching Scheme

Taking the previous example even further, in [30], a tri-level switching scheme was proposed whose operation is shown in Fig. 21. In this case, only one capacitor is switched for each of the comparisons, not just the LSB one as in [4]. The operation is as follows. Top plate sampling is used while bottom plates are grounded in the sampling phase. After the MSB is resolved, the all of the capacitors in the lower voltage node are switched to V_{CM}. This level shifts the voltage on this array by V_{CM}

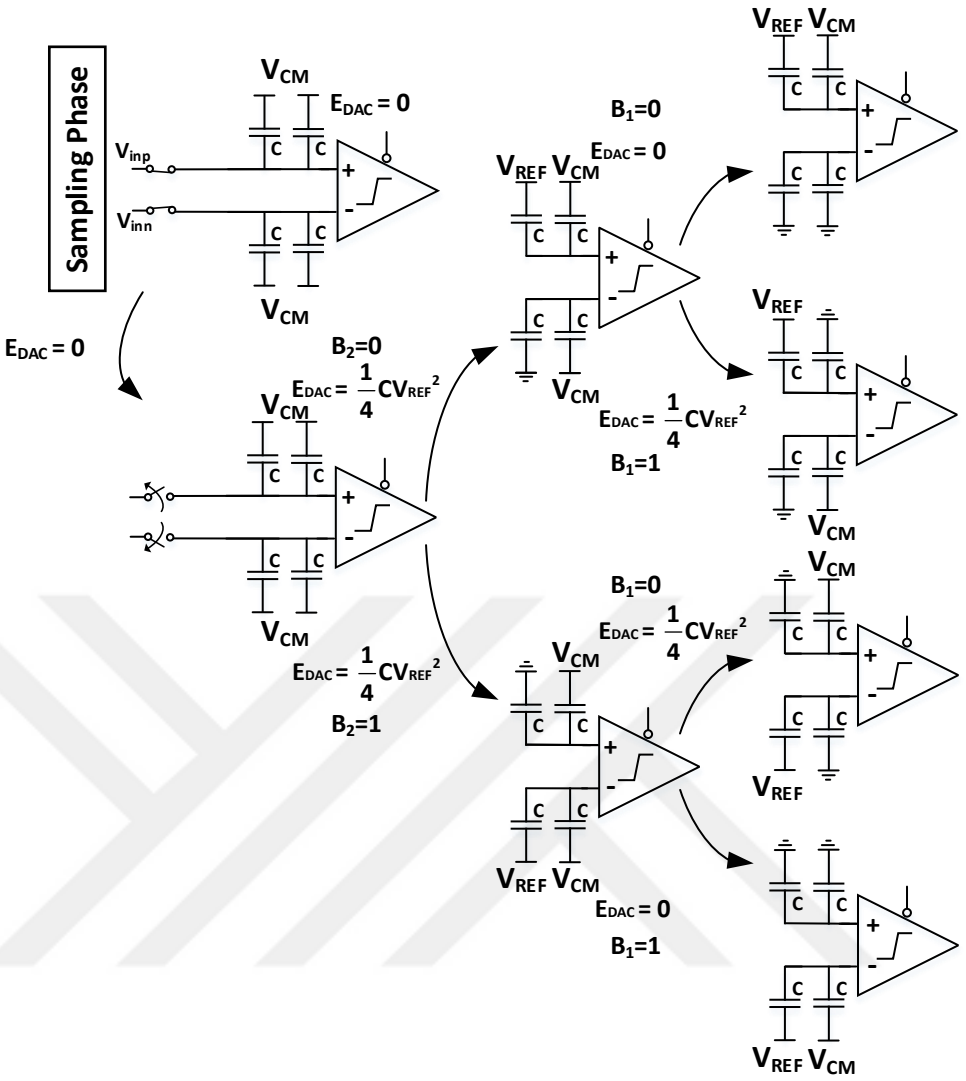


Figure 20: A different V_{CM}-based Capacitor Switching Scheme from [4]

and 2nd MSB can be resolved. From now on, the other array capacitors are not switched at all and only this one is operated upon. Depending on the comparator decision, next biggest capacitor on this array is switched to V_{REF} or ground. This process iterates until the SAR algorithm is finished and all bits are determined.

This is the most energy efficient CR-based switching scheme so far reported in the literature. However, it suffers from a large variation on the common mode voltage just like the monotonic switching scheme discussed above. This results in variations of the gain and the offset of the comparator and presents a nonlinearity. This is why in this work we chose not to implement the tri-level switching scheme despite the fact that it offers higher energy efficiency.

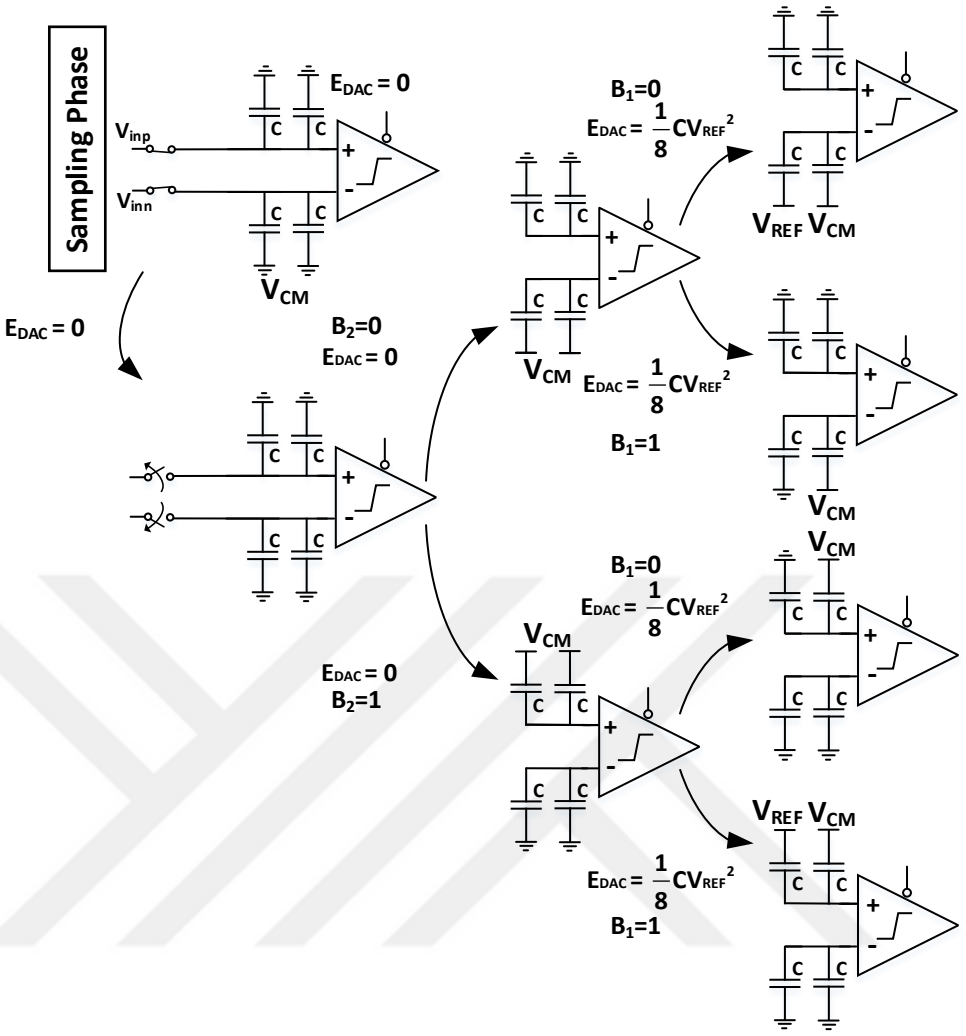


Figure 21: Tri-level Capacitor Switching Scheme

2.4 Comparators

A comparator is a circuit that compares an analog signal to another signal and outputs a binary digital signal based on the comparison. The function of an ideal comparator is depicted in Fig. 22 . The comparator compares the input values V_+ and V- and gives a logical output to determine whether V_+ is greater so smaller than V-.

Comparators are required to detect even the smallest differences at its inputs. In order to realize this, most comparators are designed with large amplification. Considering that every ADC contains at least one comparator, a wide bandwidth is necessary if the design targets high speed applications. In general, in comparator design, the accuracy and speed is juggled against power consumption to achieve an

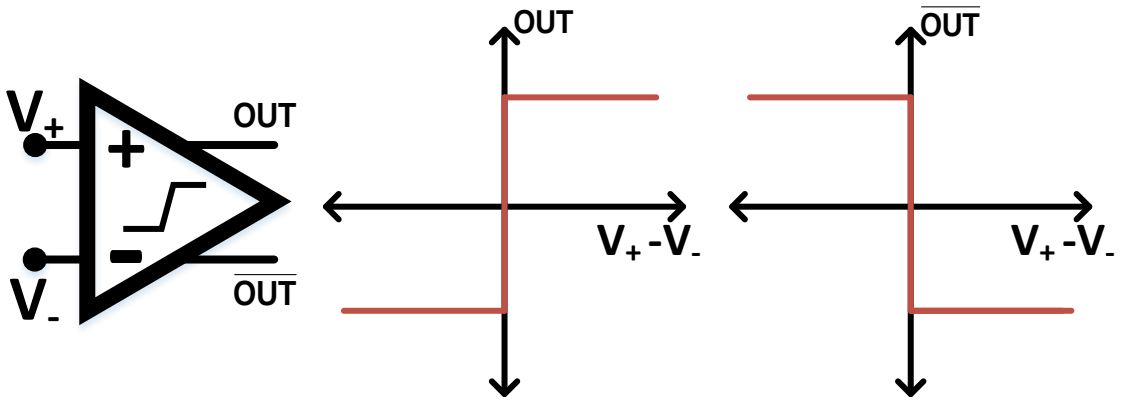


Figure 22: Ideal Comparator Operation

optimum architecture suitable to the application at hand. The comparator should be robust to noise, exhibit low offset and no memory effect from previous decisions. Moreover, these parameters need to be kept under a required specification for all process, voltage and temperature variations. Comparators can be classified by their operation time. Comparison operation can be done at discrete time intervals or continuous time. These discrete time operating comparators that operate on a clock are called clocked comparators or dynamic comparators due to their semblance to dynamic CMOS logic. We have chosen to implement the most famous dynamic comparator the StrongArm Latch [31], whose design and operation is explained in Chapter 4.

2.5 Successive Approximation Register (SAR Logic/Controller)

Th SAR control logic is tasked with updating the DAC inputs to generate the new voltages to be compared in the comparator after a new comparison decision is made. The SAR logic, therefore, is the element implementing the switching algorithms we have explained previously and can be thought as the decision-making mechanism of the successive approximation. Normally in synchronous SAR, the SAR logic and the ADC sampling is clocked by the same clock and operate synchronously.

2.5.1 Asynchronous SAR

The conventional synchronous SAR has fundamental limitations in speed. The sequential nature of the SAR algorithm dictates an additional SAR loop for each extra bit. Thus, SAR architectures go down in speed as resolution scales. In addition, the resolution increase increases the total DAC capacitance and driving a larger input capacitance limits the bandwidth even more. Since the sampling clock/comparator clock/SAR logic clock are all synchronous and use the same clock, the clock can only be as fast as the slowest cycle in the signal path. This is most apparent with the comparison cycles, where the comparison time depends on the input amplitude and for <LSB inputs comparator takes a longer time to resolve the decision. The asynchronous timing takes advantage of this and allocates more time to the critical decisions that require more time to resolve in the comparator. Furthermore, compared to synchronous clocked SARs, it also shaves off unused time from easy decisions which complete quickly. As a result, since a majority of comparator decisions in a given conversion are non-critical, the overall conversion takes much less time, and this increases the sampling speed significantly. The speed of the overall SAR is determined by the sum of the DAC settling time, the comparator decision time and the asynchronous SAR logic delay. The first asynchronous SAR prototype was demonstrated by Chen [32].

2.6 The SAR Performance Renaissance: Renewed Research Interest in SAR ADC

As we have mentioned, it is straightforward to see that the SAR ADC with its digital SAR control logic and DAC switches can take advantage of the aggressive CMOS scaling to improve its performance significantly and overcome its inherent serial conversion speed. Indeed, in last 10 years, the research interest in SAR ADCs have skyrocketed. This is illustrated by Fig. 23, in which the number of SAR ADC publications and the total number of ADC publications in VLSIC and ISSCC from 1997 to 2017 have been given. In 2017, more than half of the ADCs published have been pure SAR architectures or SAR hybrids.

In Fig.24 and 25, the FoM_S performance improvement of SAR ADCs in the

recent years can be compared, based on the data from [1]. Evidently, SAR ADCs are the architectures among all other ADC architectures pushing towards the highest efficiencies, and they are able to maintain this improving trend thanks to technology scaling and architectural innovations.

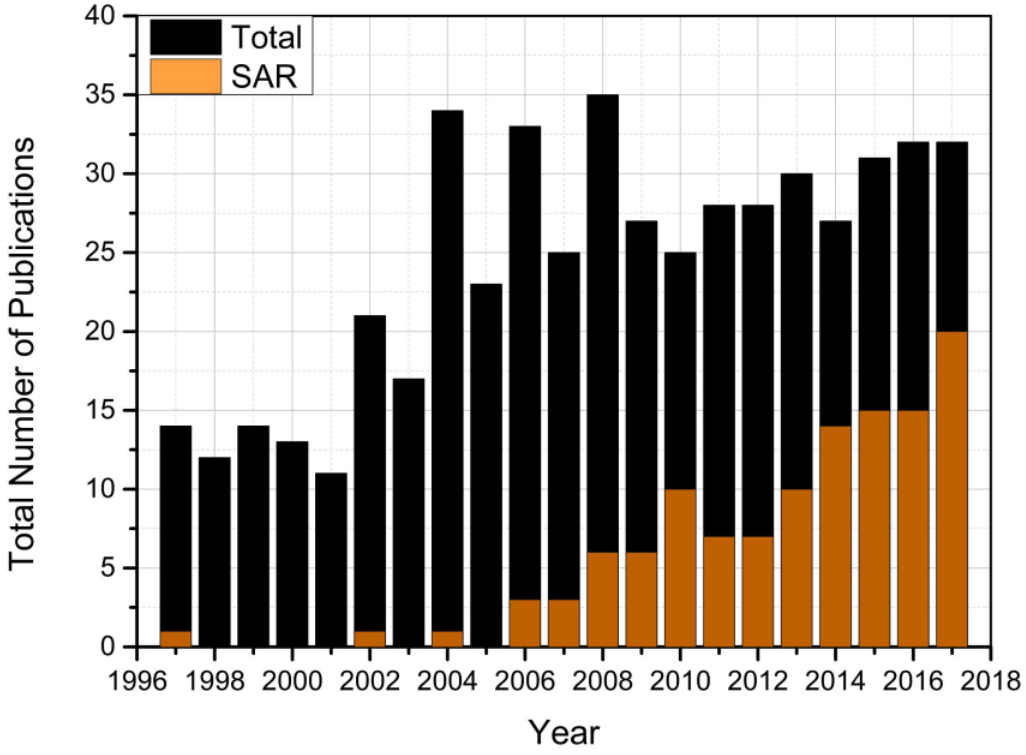


Figure 23: The ratio of SAR ADC publications to total number of ADC publications in VLSIC and ISSCC from 1997 to 2017, adapted from [1]

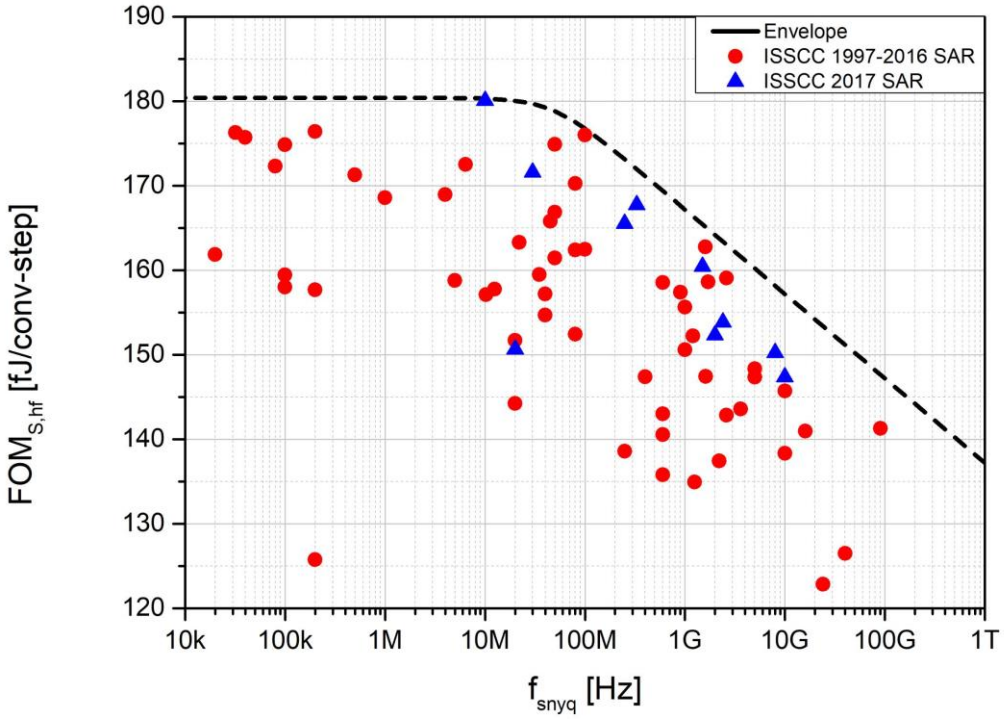


Figure 24: Recent SAR ADC FOM$_S$ performances in ISSCC, adapted from [1]

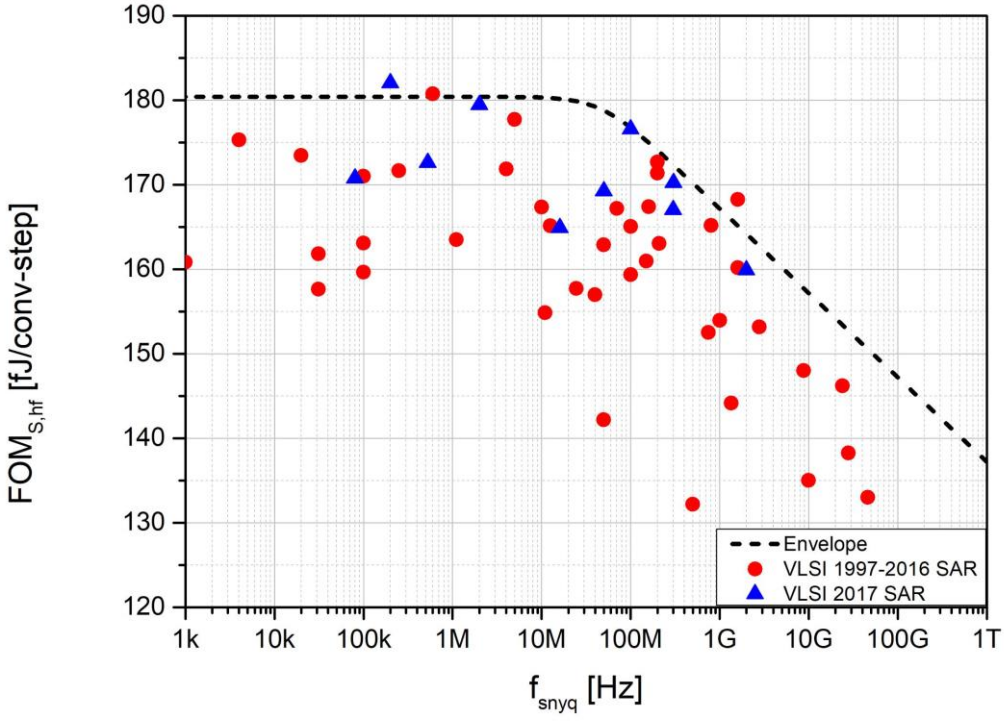


Figure 25: Recent SAR ADC FOM$_S$ performances in VLSIC, adapted from [1]

3 A 6-bit Time Interleaved Asynchronous SAR ADC with 1-bit redundancy

Up to now, a brief introduction to ADC operation, its performance metrics, and different ADC architectures have been given in Chapter 1 and SAR ADC architecture has been detailed in Chapter 2. In this chapter, we explain our implemented SAR ADC design process and circuit topology. In Fig. 26 , an overview of the implemented single channel SAR ADC is shown. The time-interleaved version features four of these ADCs as shown in its layout in Fig. 27. This chapter will focus on the design and the analysis of the implemented SAR ADC.

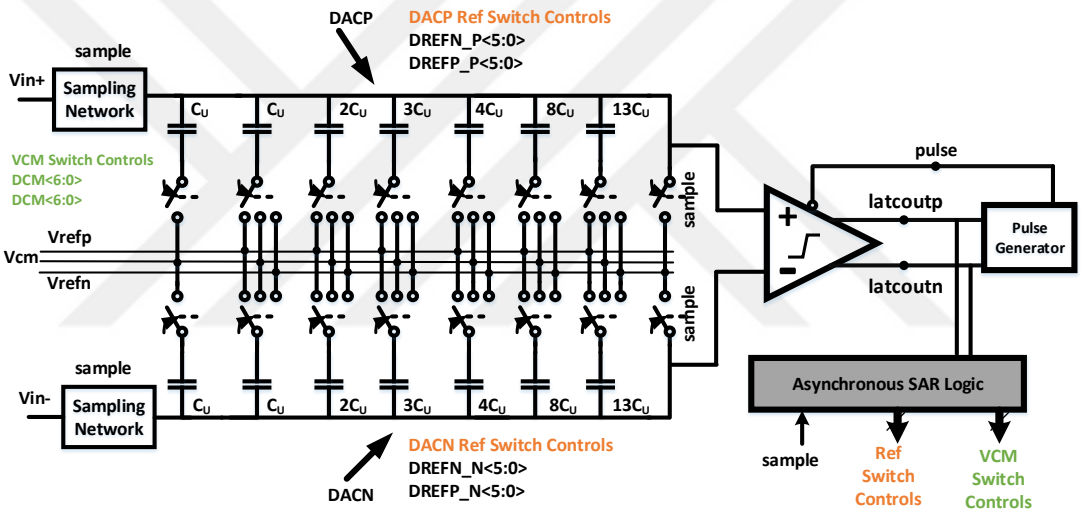


Figure 26: Implemented single channel SAR ADC schematic

3.1 V_{CM}-Based Differential Capacitive DAC with Redundancy

We have chosen to implement a V_{CM}-based switching scheme for our SAR ADC. As explained in the previous chapter, the V_{CM}-based design has a constant common mode voltage which is favorable for fixing the comparator offset and gain, reducing input dependent nonlinearity. In addition, as discussed, V_{CM} serves as an extra reference voltage to the DAC reducing the MSB capacitor size by 1 bit. We have also implemented redundancy similar to the work noted in [33].

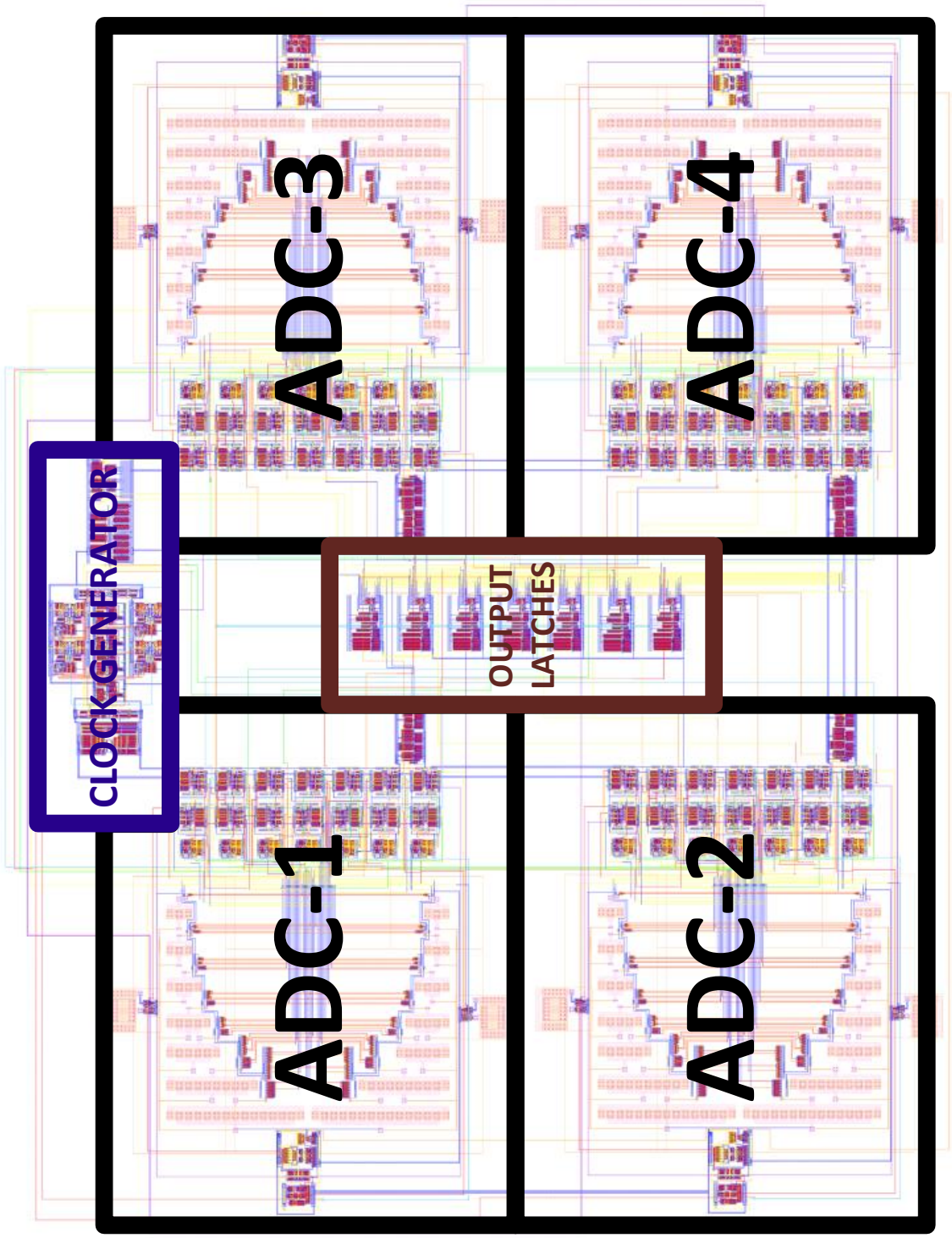


Figure 27: Four-way time-interleaved ADC layout

3.1.1 Redundancy

In Chapter 2, we discussed the traditional binary search algorithm of a SAR ADC. In the binary search algorithm, conversion errors can not be tolerated. As the search space is divided exactly by the number of bits of the ADC and each

unique search space is covered by only that bit result combination. It is possible to increase the binary successive approximation algorithm's robustness against wrong comparator decisions by implementing a non-radix 2 algorithm. In other words, the N bit ADC is implemented with more than N comparisons and more than N bit information. The search space is not divided in a binary manner, and there are overlaps between codes in the output. Meaning that the same digital output can be reached even if different (read: wrong) comparison decisions are made within a certain margin of error. The more comparisons there are, the more the comparator error can be tolerated by increasing the overlap searching range between different digital codes. However, this implements a significant trade-off with the speed since more comparisons translate to more time required for the SAR ADC serial conversion.

In our work, we have implemented 1-bit redundancy in the DAC. The redundancy in the algorithm is based on [33] and works as follows. The search space is divided into non-binary overlapping regions by changing the binary weighted capacitor array into a non-binary weighted array. Our capacitor array implements C_u, C_u, $2C_u$, $3C_u$, $4C_u$, $8C_u$, $13C_u$ capacitances instead of the typical binary weighted configuration of C_u, C_u, $2C_u$, $4C_u$, $8C_u$, $16C_u$. As one can notice in the conventional binary algorithm, the MSB capacitor ($16C_u$), makes up exactly half of the overall capacitance, thus dividing the search range exactly into 2 non-overlapping regions. In the sub-radix 2 redundancy case, the MSB capacitor is $13C_u$ while the rest of the capacitance is $19C_u$ spanning overlapping regions in the search space and improving the robustness against wrong comparator decisions. One disadvantage of this technique is that now the number of comparisons needed have increased from six to seven, potentially slowing down the ADC depending on the individual delays of the sub-blocks of DAC, comparator and SAR logic. Furthermore, as shown in [33], there is a certain mismatch factor limitation that scales down with resolution for the redundancy capacitors that can be tolerated otherwise missing codes will occur in the transfer function as sub-radix 2 search space will skip the digital codes that correspond to redundancy overlap voltage range assuming a confidence level of 3σ. For our case, since we are implementing only a 6-bit design in 90nm technology, the mismatch factor comfortably satisfies this condition.

3.1.2 Determining the Unit Capacitance

The unit capacitance is one of the most important parameters a designer has to determine to implement the DAC in a SAR ADC. The reason is actually two folds, and it is a major trade-off in the DACs. First, the DAC is generally the most area consuming part of the design as it requires an array of unit capacitors that scales exponentially with higher resolutions in the conventional designs. As mentioned in Chapter 2, conventional N-bit SAR architecture requires 2^N unit capacitors for its binary weighted DAC. We would like to have as small capacitance as possible to speed up the DAC settling time, reduce the power consumption/switching energy, and reduce the overall chip real estate occupied by the DACs. However, as with many switched capacitor designs, the capacitance's thermal noise (kT/C) and mismatch limits the linearity. The exact limit to how small a capacitor can be used depends on the DAC architecture (BWC DACs, SC DACs, Two SC DAC, Vcm-based SC DAC, ..), mismatch and thermal noise and has been the study of many papers in the recent literature. The exact calculation to determined the unit capacitance with a given confidence level on the linearity is shown in [34]. The calculation shows that 5fF unit capacitance should be enough for 6-bit resolution, however during the implementation the layout parasitics were affecting the linearity simulations too much and deviating from the intended performance with parasitics on the order of 5fF . This is why we have opted to go for the 10fF capacitor which is incidentally the smallest possible metal-insulator-metal (MIM) capacitor implemented in the 90nm technology. There are several works in SAR ADCs where custom metal-oxide-metal (MOM) capacitors on the range of 1fF have been used [35]. However these require extra careful design and routing for correct implementation, hence we have chosen not to implement them.

3.1.3 Determining the Switch Driving Strengths

The switches of the DAC that are tasked with setting the reference voltages of the bottom plates according to the decisions coming from the SAR logic. In V_{CM}-based switching, we need to be able to switch in-between V_{refn}, V_{refp} and V_{CM}. Since in our design, the reference voltages are V_{refn} = 0.5 V, V_{refp} = 1 V and V_{CM}=0.75 V, the switches are designed to be NMOS switches, PMOS switches and transmission gates,

respectively. THe important consideration here is that the switches need to switch and the resulting charge redistribution needs to settle within the LSB bit accuracy before the next comparison occurs. Thus, DAC settling time has to be designed to satisfy this condition. If we assume that the settling speed of each bit cycling will be dominated by the time Thus, these switches are sized to have sufficiently low on-resistance. Furthermore, to enable a balanced settling for all switchings, the switches are sized according to the ratio of the capacitor array, with $13C_u$ capacitor having the lowest on-resistance switches and C_u having the highest.

3.1.4 Layout Considerations

In the layout of the DAC, extreme care needs to be taken as the DAC determines the overall linearity of the SAR ADC. Typically, the capacitor arrays are implemented with unit capacitances to reduce the mismatch. Furthermore, these unit capacitances are laid out in a common centroid manner to improve matching and reduce non-linearity. We had also opted to use this layout technique for our arrays as shown in Fig. 28. However, our simulations revealed that this increases the layout area extensively and the routing gets extremely complicated and long between the capacitors as they are not laid over the capacitors to prevent parasitic contributions to intended capacitances as much as possible. The resulting effect is that the layout parasitics extensively affect the DNL/INL simulations of the ADC and is the culprit for degradation between schematic and layout simulations.

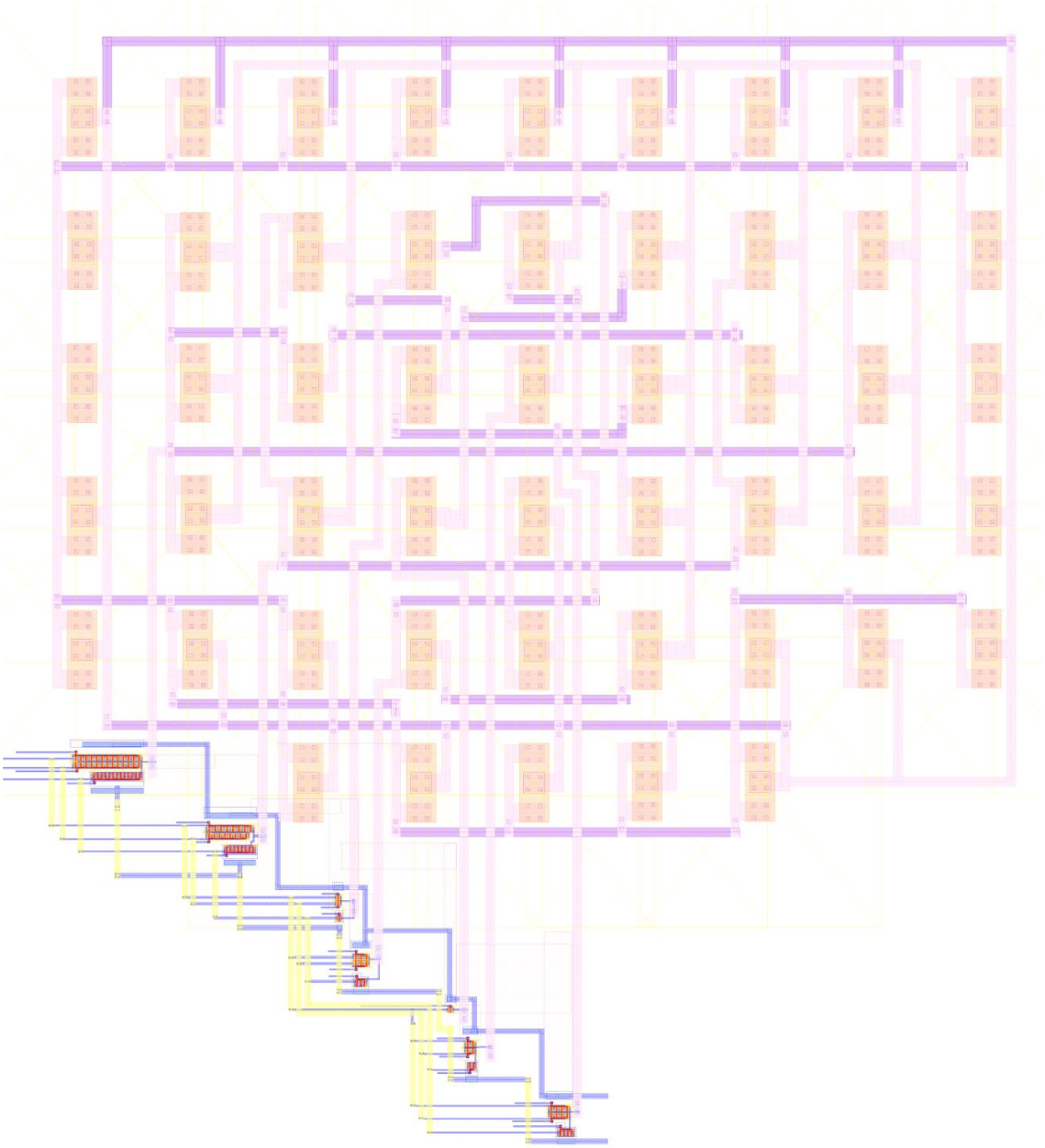


Figure 28: Common Centroid Layout of the Capacitive DAC

Thus, we have implemented another CDAC layout that minimizes routing as much as possible. Furthermore, we have increased the unit capacitance from 5fF to 10fF in order to minimize the effects of parasitics and mismatch, now that we have abandoned a fully common centroid layout. Nevertheless, we have tried to preserve symmetry as much as possible. In addition, the sensitive CDAC layout was excluded from the filler metals and layers in order to prevent any unaccounted parasitic effects. The final result yielded very good INL/DNL performance as the capacitor ratios between different bits were disturbed far less than the common

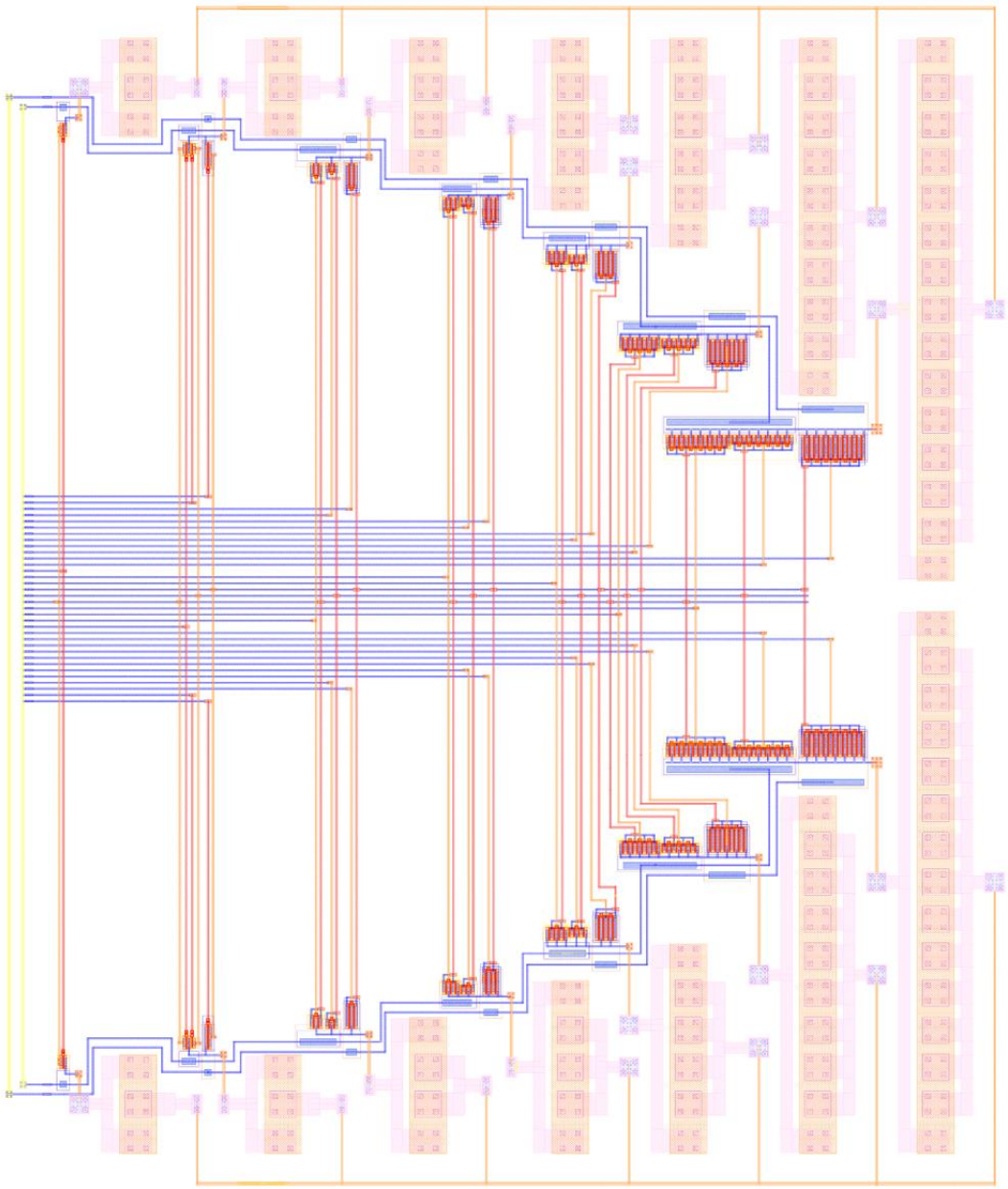


Figure 29: Final Layout of the Capacitive DAC

centroid layout. This was also confirmed by parasitic extraction tools. The final version of the layout is shown in Fig. 29

3.2 Latch-Based Comparator

As previously mentioned, the comparator block is one of the most critical blocks in SAR ADCs. This is even more true for an asynchronous implementations like in this work, as asynchronous SAR logic depends upon the comparator decisions to work. A faster comparator that resolves decisions quickly and avoids metastability

speeds up the conversion significantly as comparisons occur at least 2^N times in one conversion. Designing a fast latch-based clocked comparator that can resolve <LSB voltages requires an optimization of the regeneration time, the reset time and the amplification time. Current state-of-the-art comparators consist of two circuits: a) latches to regenerate the decision levels quickly, b) preamplifiers preceding the latches to accrue some gain and reduce the noise sensitivity of the latch. In this section, we present the latch and the preamplifier used in this work and their design methodology.

3.2.1 Preamplifier

The preamplifier is a critical part of the comparator as it provides gain to improve comparator resolution. The preamplifier used in this work is a static one stage differential amplifier with active PMOS loads. This constitutes the only static power consuming block in the ADC. Although the power consumption is increased, the static preamplifier choice is critical in this work as the preamplifier is directly connected to the DAC output nodes. Any disturbance in these nodes will warp the input and produce errors in the ADC. So as to be able to avoid the kickback noise and clock feedthrough associated with the large switching currents of the latch coming after the preamplifier and the dynamic preamplifier itself, we implement a simple one stage preamplifier. One other solution is to implement multiple stages to isolate the kickback noise coming from the next stages of the amplifier, however, this still does not solve the switching current that would come from the first stage.

3.2.2 StrongArm Latch Comparator

The latch of the comparator used in this work is based on the StrongArm Latch comparator [31]. The circuit implemented is depicted in Fig. 30. StrongArm Latch, named after its infamous use in the StrongARM microprocessors, is one of the most widely used latches in comparators. Indeed, the circuit has many advantages; it consumes no static power, can directly produce rail-to-rail outputs and the regeneration enables its offset to be primarily dominated only by the input differential pair, M1 and M2.

The circuit operates as follows. When the clock is low, the tail transistor is off

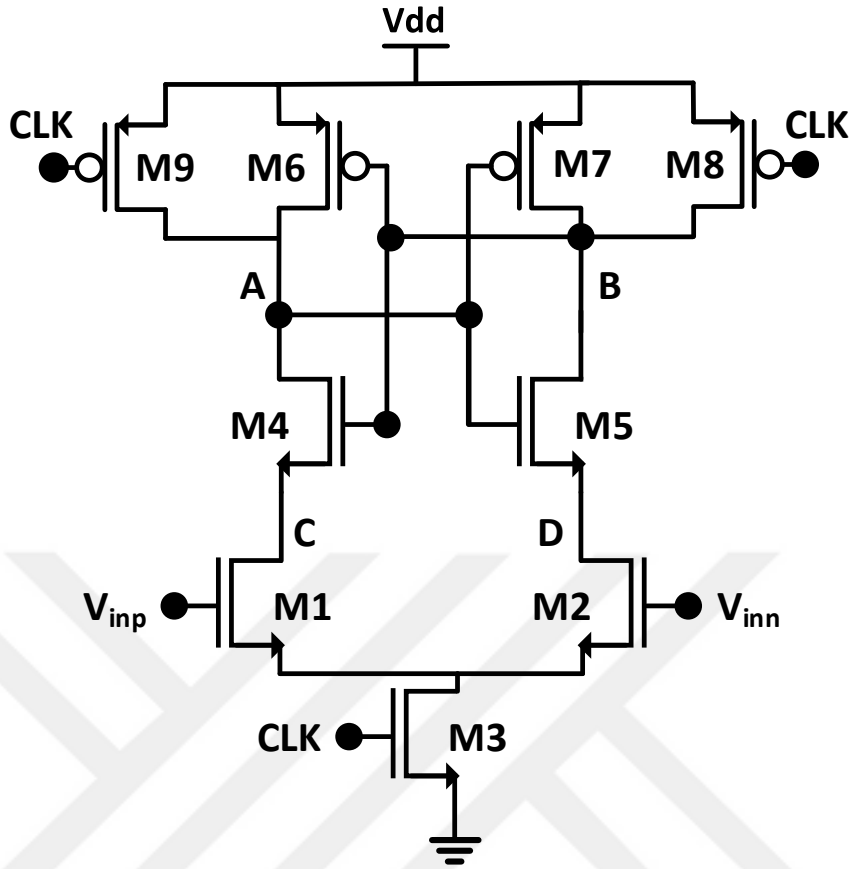


Figure 30: Latch stage of the comparator

and the A and B nodes are pulled up to V_{dd} by M8 and M9. The difference between the two input voltages, V_{inp} andV_{inn} is applied to the differential input pair, M1 and M2. At a rising clock edge, the small differential voltage on the inputs is converted to a proportional differential current through this pair. The current is drawn from the total capacitances of nodes C and D, since V_A and V_B are still high and M4 and M5 are off. Then during this phase, we can write

$$|V_C - V_D| \approx g_{m1,2}|V_{inn} - V_{inp}|/C_{C,D} \tag{34}$$

Thus, the difference applied to the input differential pair can be amplified/attenuated on the nodes C and D depending on the transconductance of the differential pair and the total capacitance on the nodes C and D. As a result, this phase is termed as the amplification phase. Once the V_C and V_D decrease to V_{dd}-$V_{t,n}$, the NMOS transistors M4 and M5 turn on, now enabling the M1 and M2 drain currents to

flow from them, enabling the regeneration of the cross-coupled latch. The amount of time it takes to turn M4 and M5 is

$$t_{amplification} = \frac{C_{C,D}}{I_{avg} V_{t,n}} \tag{35}$$

where I_{avg} is the average current drawn from the nodes C and D in this time. Then, the approximate gain in the amplification phase is [36],

$$A_v = \frac{g_{m1,2} V_{t,n}}{I_{avg}} \tag{36}$$

and the regeneration time of the cross-coupled latch to generate the output is given in [37] as

$$\tau_{reg} = \frac{C_{A,B}}{g_{m3,4}(1 - (C_{A,B}/C_{C,D}))} \tag{37}$$

Since $C_{A,B}$ is greater than $C_{C,D}$ as the latch outputs are buffered with back-to-back inverters, the cross coupled NMOS M4 and M5 offer little regeneration in this phase. The V_A and V_B nodes continue to decrease to V_{dd}-—$V_{t,p}$— at which point M5 and M6 turn on and the outputs are regenerated to the rails due to positive feedback. Once the outputs are regenerated, M3 and M4 prevent any more current flow and avoid static power consumption.

The offset and noise analysis of this comparator is given in [37]. The key contributors to offset is the mismatch between the input differential pair as the later transistor's mistmatch and noise is divided by the gain of the input differential pair. Some offset cancellation schemes have been implemented in the literature. Some of them [36], [38] aim to create an intended mismatch in the C_C and C_D by employing many small unit capacitors and connect them depending on the amount of offset to cancel the offset. In this work, we have chosen not to implement offset cancellation due to design time constraints. Since we have a constant common-mode switching scheme the comparator will always get the same common mode inputs and the offset will not vary due to common mode voltage variation.

3.2.3 Layout Considerations

Mismatch in the preamplifier or the latch greatly affects the amount of offset and non-linearity seen in the comparator.Therefore, all layout is done extremely carefully. The differential pairs and the transistors that share their gates and sources/or drains are interdigitated in a common centroid manner to minimize the mismatch of the transistors from PVT variations. Since any mismatch in the loading of the differential outputs of the latch can cause an offset to be incurred in the other input. Indeed, since the comparator is interfaced with the pulse detector and the asynchronous SAR logic. It is necessary to buffer the outputs of the comparator with simple inverters to ensure the output nodes are not disturbed differentially. Furthermore, a diligent effort is made in order to keep the signal path as symmetric as possible to ensure the common mode is rejected as much as possible. The layout of the comparator is shown in Fig. 31.

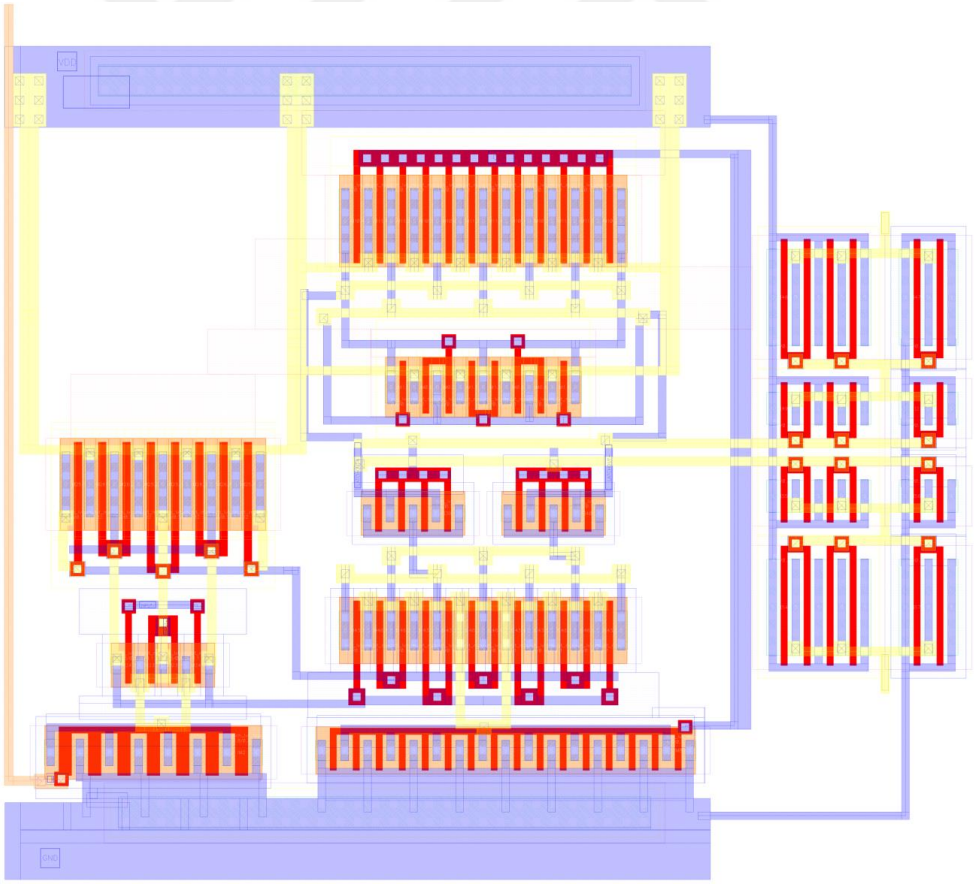


Figure 31: The comparator layout

3.3 Full-Custom Asynchronous SAR Control Logic for V_{CM}-Based Switching

An optimized full custom SAR logic for Vcm-based switching has been implemented and its schematic is depicted in Fig. 32. As shown, the pulse generator generates the comparator clock asynchronously, and the full custom control logic immediately sets the corresponding DAC switches after a comparison decision is resolved. This asynchronous flow occurs 8 times (7 for bits + 1 for sampling) during one conversion cycle and speeds up the SAR ADC considerably. A faster asycnhronous handshaking and decision logic results in even faster sampling rates as this is the most critical signal path in the conversion process that occurs N+1 times for N resolution. The signals *done*, *set* and *valid_next* make up the coordination signals among the static logic cells that enable the communication.

The important considerations of sizing of the digital control transistors is that it needs to load the comparator as little as possible to not incur any more delays in the comparator decision but still be strong enough to be able to drive the MSB capacitor in the DAC, which is half of the total capacitance of the DAC output, for the first decision.

3.3.1 DCM/DREFN/DREFP Cells

The logic cells contain control circuitry and an SRAM based 1-bit memory cell. There are two different cell types, namely DREF cell and DCM cell. These cells generate output signals to control different parts of the V_{CM}-based differential DAC circuit. No control logic, external to these cells, is required for the circuit to operate. As such the control circuit can easily scale with resolution with no modifications.The DCM cell's circuit schematic is shown in Fig.33. The primary function of this cell is to trigger the signals that control V_{CM} switches in the DAC and relay the corresponding handshaking signal to the DREFN/DREFP cells.

3.3.2 Operation and the Critical Path

The signal path of the logic circuit and its operation is shown in Fig. 32 and 35. As soon as a comparator decision is available (one of outp and outn in Fig. 35 is

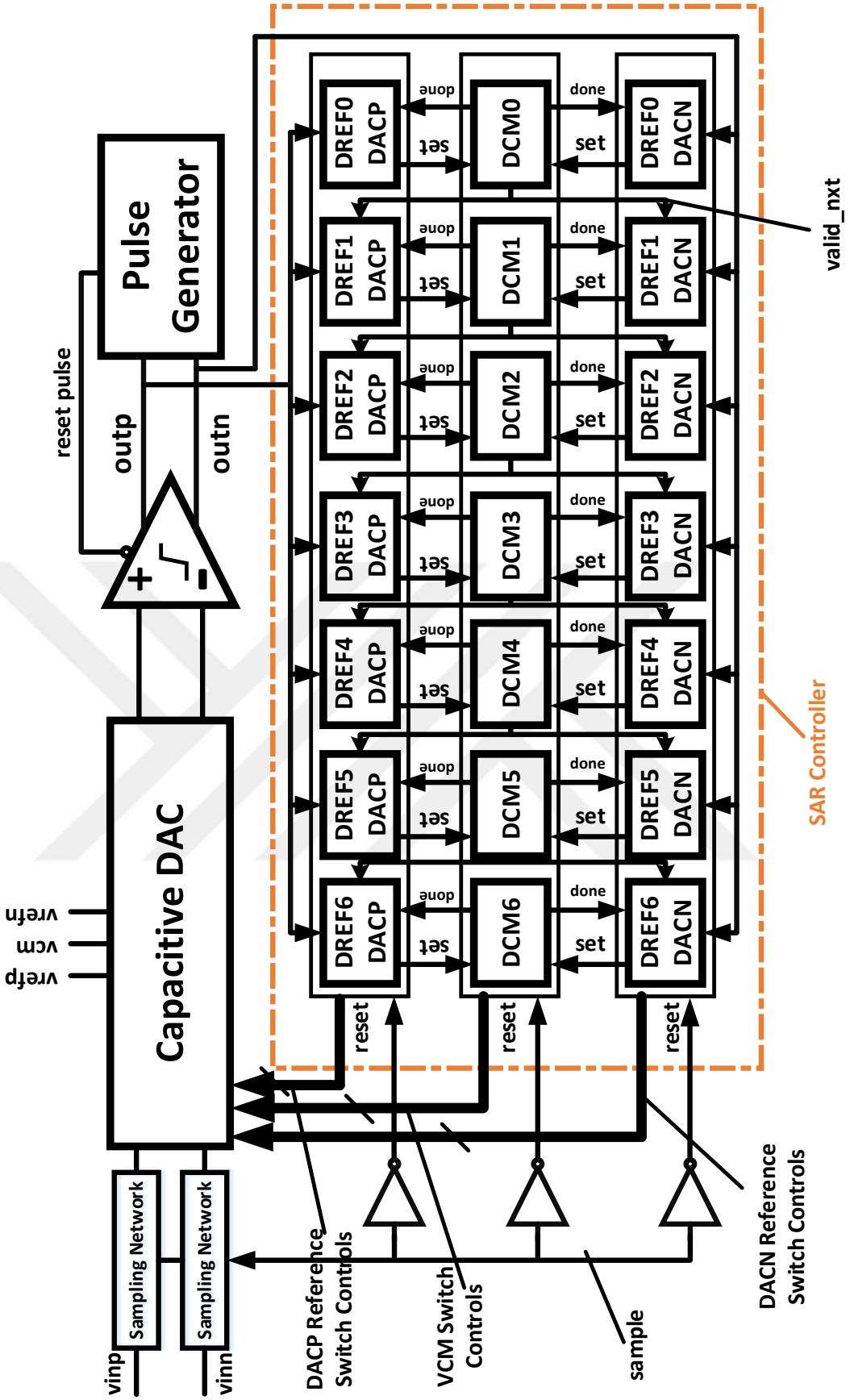


Figure 32: Full Custom SAR Logic

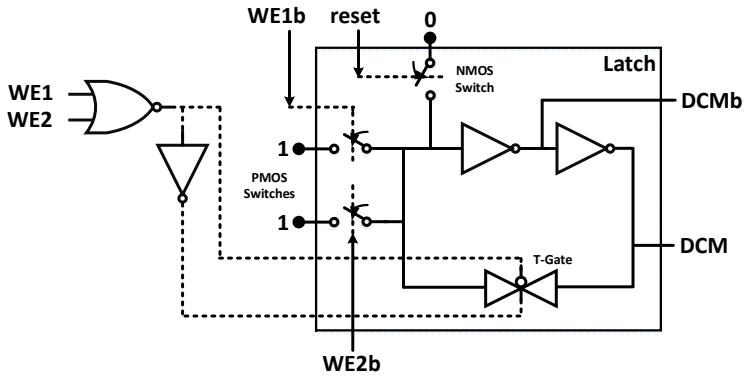


Figure 33: The DCM Cell

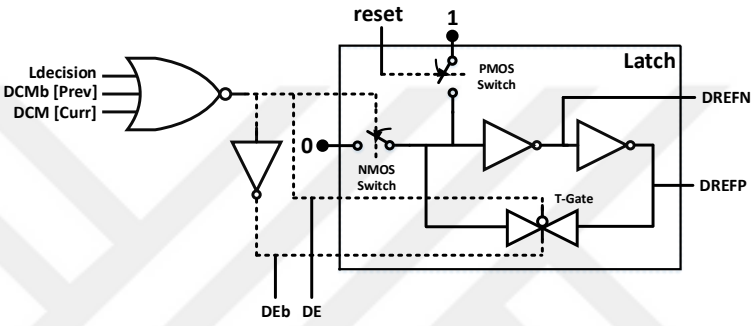


Figure 34: The DREF Cell

asserted), the set output from either DACP DREF CELL0 or DACN DREF CELL0 activates DCM CELL0. At the same time, the switch control signals for the DAC (DREFX_X<0>and DCM<0>) are set to either 0 or 1 based on the comparator decision. Furthermore, the done output from the DCM CELL is pulled high so that control signals from both the DREF and DCM cells are locked and cannot be altered when the next comparison decision is made. Moreover, to aid the progression of control signal generation for the next comparator decisions, a *valid_nxt* signal is fed to the next set of DREF CELLs. Thus, the mutual coordination between DREF and DCM logic cells enables the generation of the desired switch control signals for the V_{CM}-based differential capacitive DAC.

It should be noted that the path from outp/outn to $DCM < 0 >$ is the critical path in this logic and constitutes the critical path of the overall SAR ADC as this logic runs 7 times during one conversion. These paths have been indicated with red arrows in Fig. 35. It can be observed from the internal circuits of the DREF and DCM cells shown in Fig. 33 and Fig. 34 that this path consists of only two NOR

gates and a latch, hence incurs low delay in the signal path.

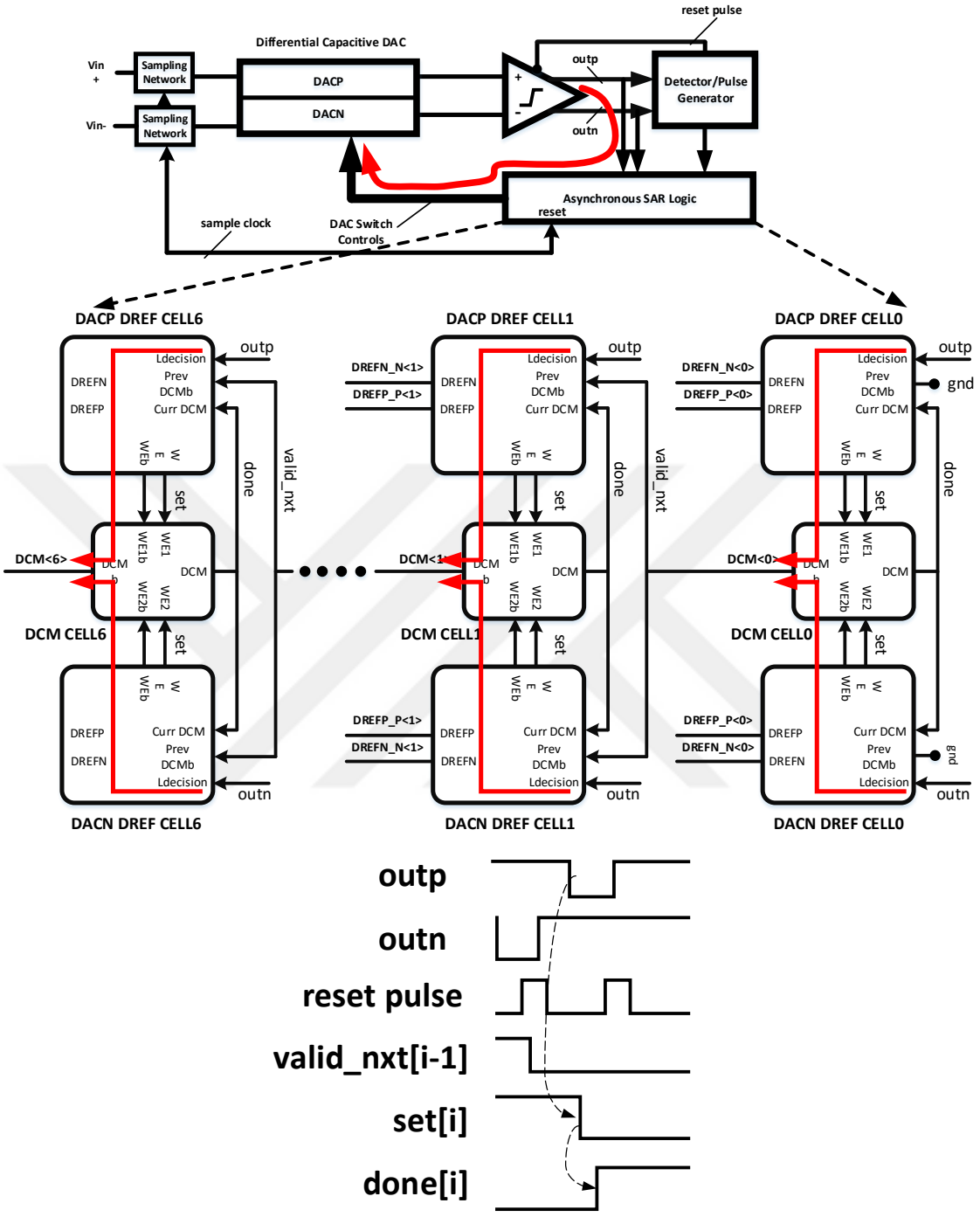


Figure 35: The Critical Path in the ADC

3.4 Asynchronous Pulse Generation

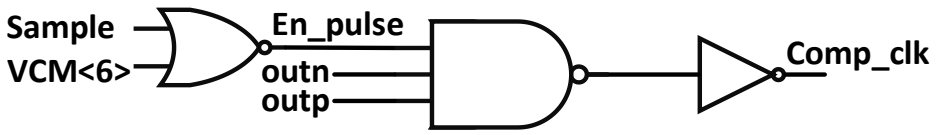


Figure 36: The Asynchronous Pulse Generator and Decision Detector

The comparator pulse detector and generator circuit is shown in Fig. 36. The operation is as follows. If the sample signal is not high or the VCM<6>is not high, the circuit is in detect mode and once it detects that one of outn and outp is high and the other is low i.e., the comparator outputs have resolved, it will produce a comparator clock that will reset the comparator to be readied for the next conversion. If the sample or VCM<6>is high i.e., the operation is in the sampling phase or the end of conversion has been reached, the comparator clock will not be generated, and the detector will be insensitive to switching of outn and outp as they get reset to get ready for the next sample. The logic gates are sized to provide the best delay times as this signal path is traversed for every comparison in a conversion.

3.5 Time-Interleaving Circuits

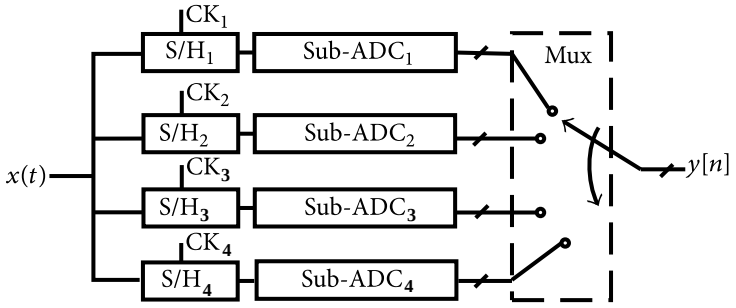


Figure 37: Time-interleaving

The 4-way time interleaving architecture employed in this work can be seen in Fig. 37. Aside from this architecture, single channel and two channel time interleaved test ADCs have also been implemented to characterize their operation

and reduce the need for calibration in case it is unavoidable for the four channel case.

3.5.1 Bootstrapped Sampling Switch

Although a sample and hold circuit exists in almost any ADC whether they are time-interleaved or not, time interleaving heavily modifies the requirements from the sampling network. An N-way time interleaved ADC which operates at F_s requires the sampling network to be able to sample at F_s, not at the F_s/N speed of sub-ADCs along with more stringent jitter requirements to avoid SNR attenuation at high frequencies. A sample and hold circuit can be separated into two blocks for design purposes, the sampling switch and the sampling capacitor. We have gone over how the value of the sampling capacitor, which is just the total DAC capacitance in this work as we are employing top plate sampling, is decided in the DAC design section in this chapter. Now that we have our total capacitance of 170fF sampling capacitor, we can determine the required on-switch resistance for the 700 MSps operation for the four-way time interleaved case. Since the other ADC designs of two-way interleaved and single channel require less speed, we opted to design a single sampling switch and use that for all 3 architectures.

The switch needs to be designed for the differential input signal range of 0.5V to 1V and maximum sampling speed. The top plate sampling increases the sampling speed by reducing the settling time in comparison to bottom plate sampling as we have seen in Chapter 2. However, top plate sampling introduces charge injection and clock feedthrough to the signal path and results in sampling non-linearity. Clock feedthrough is the cross-talk from the switching pulse of the gate of the switch which causes an instantaneous drop in the voltage of the sampling capacitor as the circuit goes from track mode to hold mode. Furthermore, as this happens, sampling switch opens, and the charge inside the sampling switch channel is injected into its source and drain nodes with a ratio depending on the source and drain impedances and the switching pulse speed and a charge amount depending on the input voltage level and the switch size. This charge introduces non-linearity and causes a change in the level of the sampling capacitor's voltage inversely proportional to the sampling capacitance. In order to reduce the switch non-linearity, a bootstrapped sampling

switch has been used based on [39] and [40]. Bootstrapping is a technique to solve the non-linearity stemming from the on-resistance variation of the switch with respect to different gate overdrive voltages which is modulated by the source voltage, V_{in}. To remedy this, a capacitor is bootstrapped between the gate and source acting as a battery to keep the gate voltage a level shifted version of the input for all inputs. The architecture of the switch is shown in Fig.38.

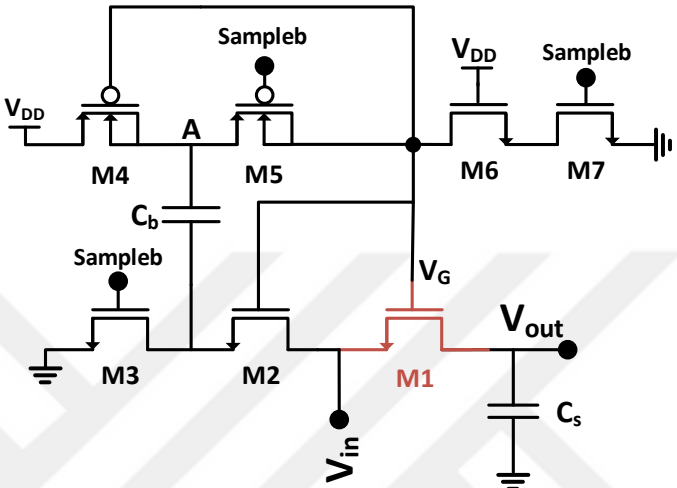


Figure 38: Bootstrapped Sampling Switch

M1 (in red) is the main sampling switch whose gate voltage, V_G, is modulated above V_{DD} to keep the gate overdrive constant in the sampling mode. In the hold mode, C_b must be recharged to V_{DD} and M1 must be turned off. M3 and M4 charge C_b to V_{DD} while M5 and M2 disconnect C_b from M11 in the hold mode i.e, when *Sampleb* is high. During the sampling phase, node A and V_G reach voltages higher than 0.5 to 1V higher than V_{DD}. To prevent M3 from turning on and discharging the node A, the gate of M3 is also bootstrapped to the same node. Since M9 is tasked with sensing and relaying the input signal to the capacitor, it is also connected to the same node to ensure linear, accurate signal transfer. Finally, as pointed out in [40], the M6 cascode reduces the stress on the M7 from high voltage on V_G that occurs during sampling.

3.5.2 Low-Skew Out of Phase Clock Generation

The low-skew out of phase clock generation circuit is shown in Fig. 39. The delay difference between the transmission gate and the inverter is "waited out" by

cross coupling their outputs and providing feedback. A single input clock is given as input and an output clk with same frequency and its inverse is generated with minimum skew to ensure that time-interleaving circuits experience as little skew mismatch as possible.

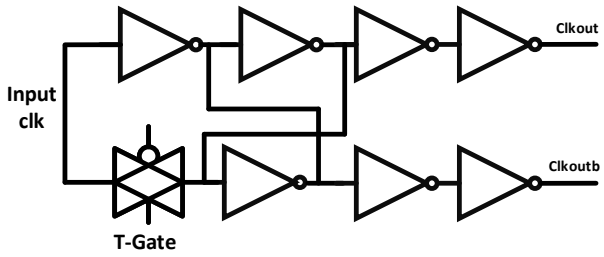


Figure 39: Low Skew Single to Differential Clock Generator

3.5.3 Non-overlapping Multiphase Clock Generation

Depicted in Fig. 40 is the circuit schematic of the non-overlapping sampling clock generator for four-way time-interleaving. The frequency of the input is divided into four by a D flipflop chain to produce the non-overlapping phases of 0 °, 90 °, 180°, and 270°. To ensure low skew between the *Sample* and *Sampleb* , once again the low skew single to differential circuit described in the previous section is used.

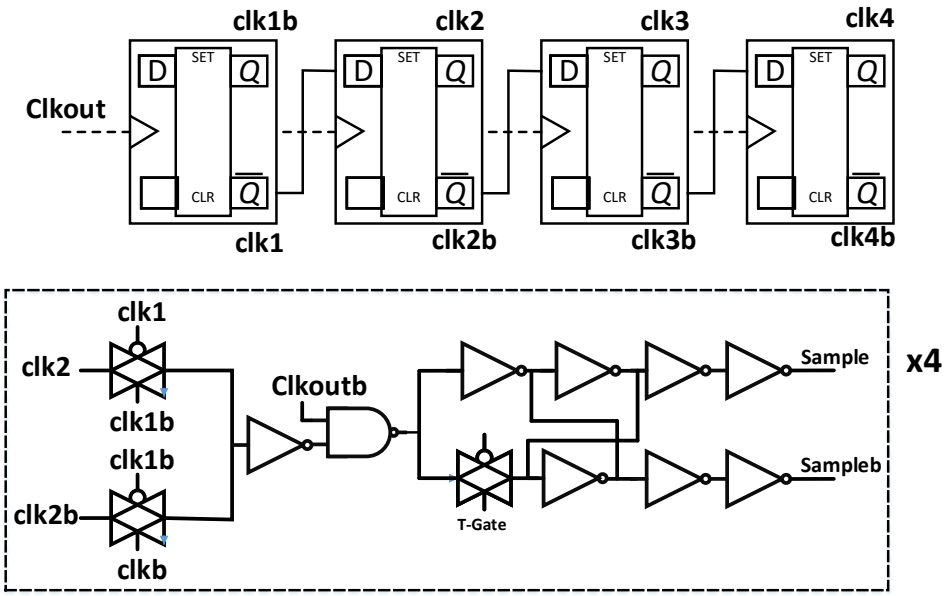


Figure 40: Non-overlapping Multiphase Clock Generator

4 Simulation and Measurement Results

4.1 INL/DNL Simulation

In this section, we report simulation results for the static parameters of the single channel, two channel and four channel SAR ADCs. The static parameters simulated are the INL and the DNL and the simulations are done as follows. In order to find the INL and DNL, every actual code width needs to determined for the ADC. This requires a complete sweep of the input to characterize the ADC. Thus, a complete histogram testing is done. To ensure that a good approximation to the code widths is obtained, each code is hit during the simulation 100 times to have a good INL/DNL resolution for a 6-bit ADC. There are two ways of performing a histogram testing. One is the linear histogram testing where the input is given as a slow ramp and every code is hit equal amount of times as the ramp traverses the input range of the ADC. Thus, any deviation from this hit count for a code represents the DNL for that code. This corresponds to $2^N \times 100$ code hits/samples to be taken for one simulation, hence the simulation time can be arduously long with increasing frequency. In our case, the simulation for 100 hits per code takes about 24 hours to simulate using 16 parallel 2.4 GHz cores. The other method is to use a sinusoidal wave and compare the resulting code hit histogram to ideally quantized sine wave histogram to obtain the DNL/INL values for each code.

The four channel INL and DNL post-layout simulation results are given in Fig. 41. The maximum INL is found to be +/- 0.28 LSB and maximum DNL is 0.24 LSB under the typical process parameters. These are excellent results even for a 6-bit SAR ADC especially if we consider the fact that there is no calibration in the DAC or in the time-interleaving architecture. Typically DNL <0.5, INL <0.5 are the targeted desirable results for ADCs as far as static parameters go.

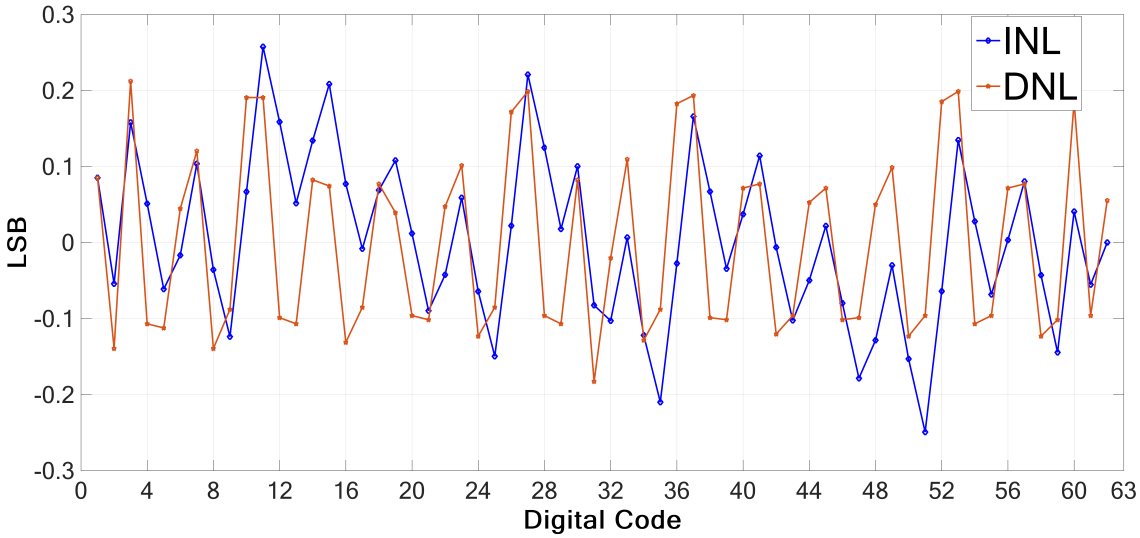


Figure 41: INL/DNL Simulation Results for 4 Channel SAR ADC with a ramp input

4.2 SFDR, SNDR Simulation

4.2.1 Simulation Setup and Results

The fast Fourier transform (FFT) analysis is the standard method to characterize the AC performance for an ADC. The FFT requires a time domain data with a number of samples, M that is a power of 2 such that the FFT spectrum is made up of the M/2 discrete bins. Since we take the FFT of the output to analyze its spectral content, we need to make sure that we are performing coherent sampling in our simulation setup, as the FFT (which is just another implementation of discrete Fourier transform) assumes that the signal within the time record repeats across the band. Otherwise, due to abrupt discontinuity, frequencies higher than the sampling rate will wreck the simulation results as the spectral content will be smeared across the spectrum. In order to sample coherently, the following needs to be strictly adhered to:

$$f_{in} = f_s \frac{M}{N} \tag{38}$$

where f_{in} is the frequency of the sinusoidal input, f_s is the sampling frequency of the ADC, M is a prime integer and N is the number of samples and a power of two.

The coherent sampling is devised for 2048 samples and the simulation has been performed for a full-scale sinusoidal input.

Schematic simulation results for the four channel time interleaved ADC is given in Fig. 42. As shown, an excellent SNR of $\tilde{3}7.7$ dB and a good SFDR of 48.7 dB is attained for an input signal of 5.5 MHz.

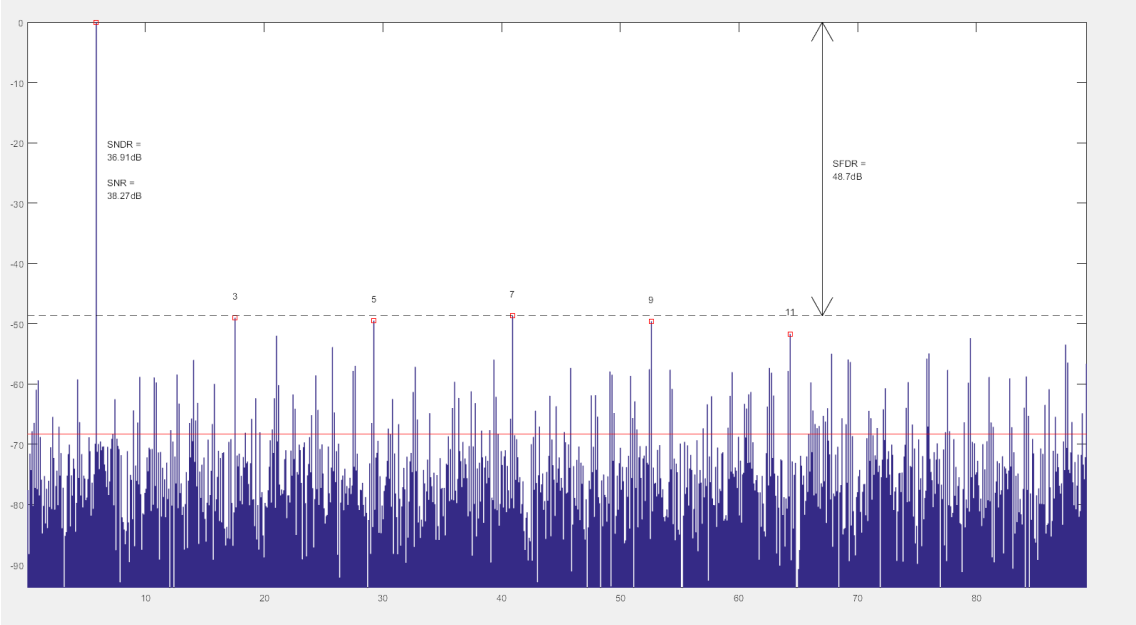


Figure 42: SNDR/SNR Simulation Results for 4 Channel SAR ADC

4.3 Measurement Setup and the Printed Circuit Board

A zoomed in view of the fabricated ADC chip can be seen in Fig. 43. The sensitive DACs for the single channel, two channel and four channel ADCs can be seen clearly in green due to the fact that all filler layers have been skipped to avoid overlap parasitics.

The chip has been bonded to a 14 mm x 20 mm, 100-pin quad flat package and for the measurement of a single channel ADC, a custom printed circuit board (PCB) has been designed in collaboration with my colleague, Shahbaz Abbasi. A two layer PCB design has been used and manufactured in-house at the university. The schematic of the ADC is given in Fig. 58 in Appendix C. First order anti-aliasing filters are implemented on the PCB board after the ADC driver outputs to band-limit the differential input of the ADC to 1 GHz. Every supply pin has decoupling capacitors that are 10 µF and 0.1 µF big. The larger capacitor provides low impedance to ground at low frequencies and the smaller capacitor provides more efficient grounding for high frequency interference. The analog and digital

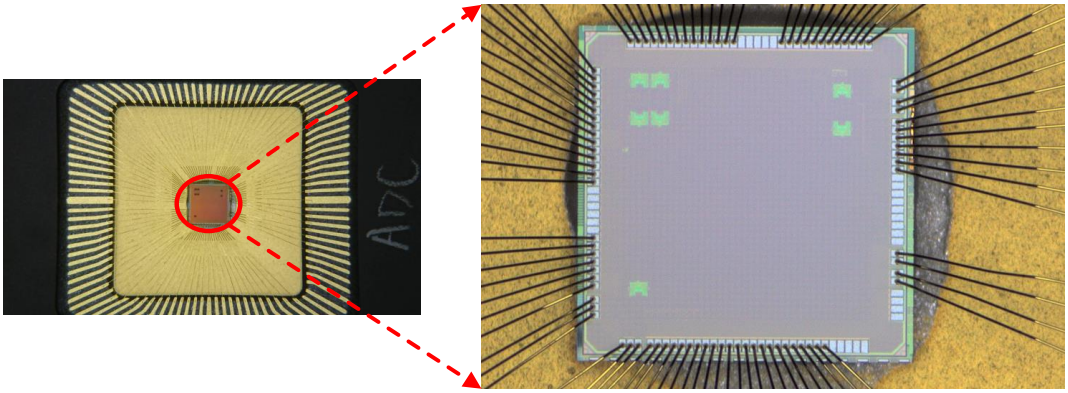


Figure 43: Fabricated Chip Photo

ground planes have been seperated and are located at the bottom and top layer of the PCB. External LDO reference generators for the generation of V_{CM} (0.75V), V_{refp} (1V) and V_{refn} (0.5V) have been used on the board. The digital and analog power supplies (1.2V) are also generated on the PCB with low drop out regulators. The supply of I/O pads is given with an SMA interface from an Agilent E3631A power supply 2.5V. The parallel outputs of the ADC are captured with an Agilent Infiniium DSO9245A oscilloscope. The clock to the ADC is given by the Agilent 81160A Pulse Function Arbitrary Generator. The digital control inputs are given from the Pattern Generator. Agilent 16702B Logic Analysis System is used to give the digital control inputs to the ADC. A picture of the measurement setup and the close-up of the PCB board under test is given in Fig.44.

4.4 Measurement Results

Measurement results for a single channel ADC are given below. The measurements of four-way time-interleaved and two-way time-interleaved architectures are not available at the time of the writing of this thesis but they are planned to be completed next. The measurements are made with DC input combinations of V_{inp} and V_{inn} equal to 0.5 V, 0.6 V, 0.7 V, 0.8 V, 0.9 V and 1 V, keeping the common mode constant at 0.75 V and setting the each sub-ADC sampling frequency to 25 MHz.

As seen from the measurement results, there is a significant shift in the bits cor-

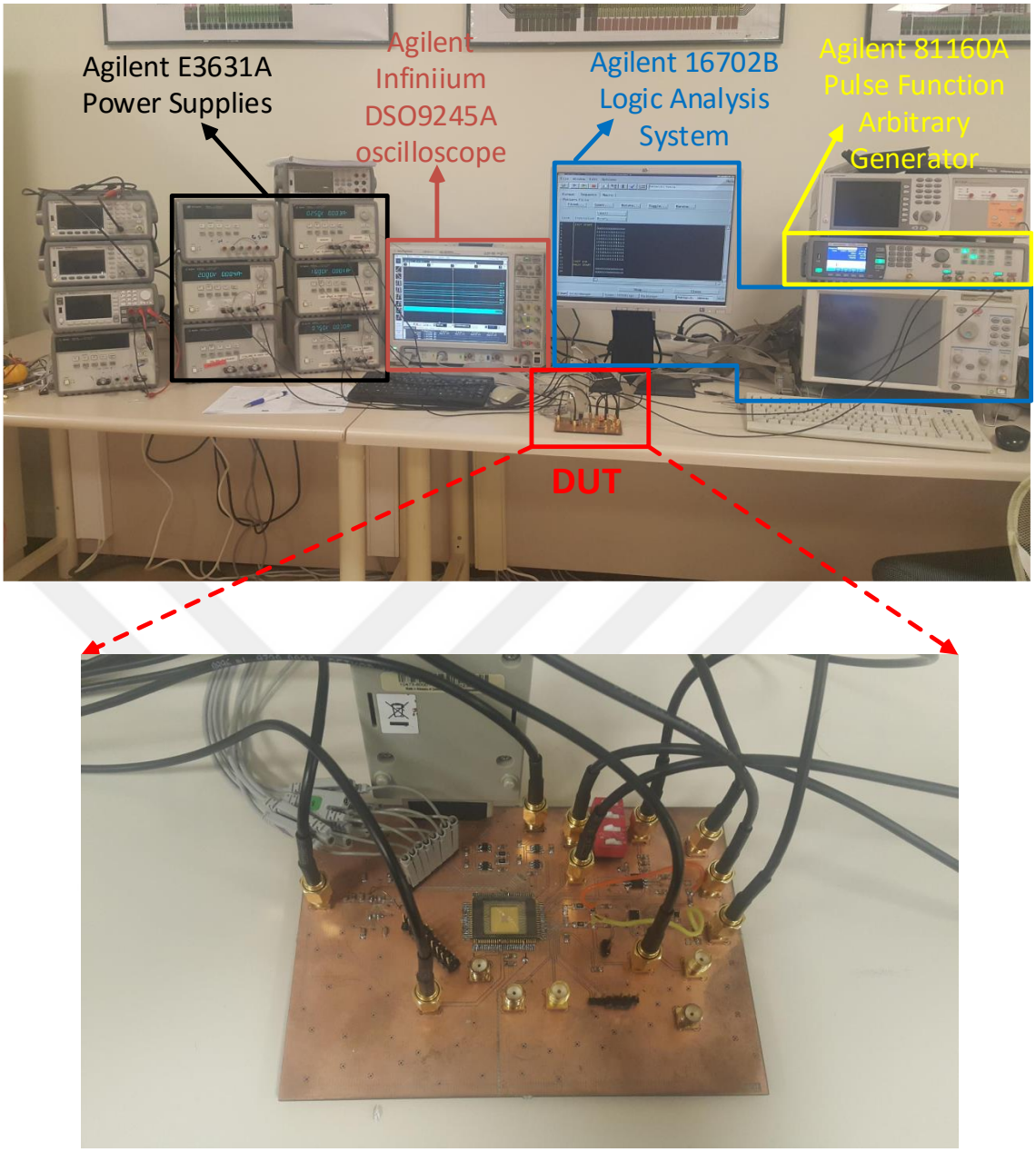


Figure 44: Measurement Setup and the ADC PCB

responding to the inputs. There is about 4-5 LSB of error as compared to expected ideal outcome. This is because the measurement PCB has significant grounding noise which couples to the V_{CM}, V_{refp}, V_{refn} references and the inputs of the ADC. Thus, the measurement is shifted by an amount of 6 LSBs. For instance, 45 is the lowest possible input given to the ADC, the expected outcome is all zeros, however, the real outcome is '0000100', this corresponds to about 2 LSB of error in the 6 bit translation.

So far, these measurement results have been given for 400 ns. In order to fix

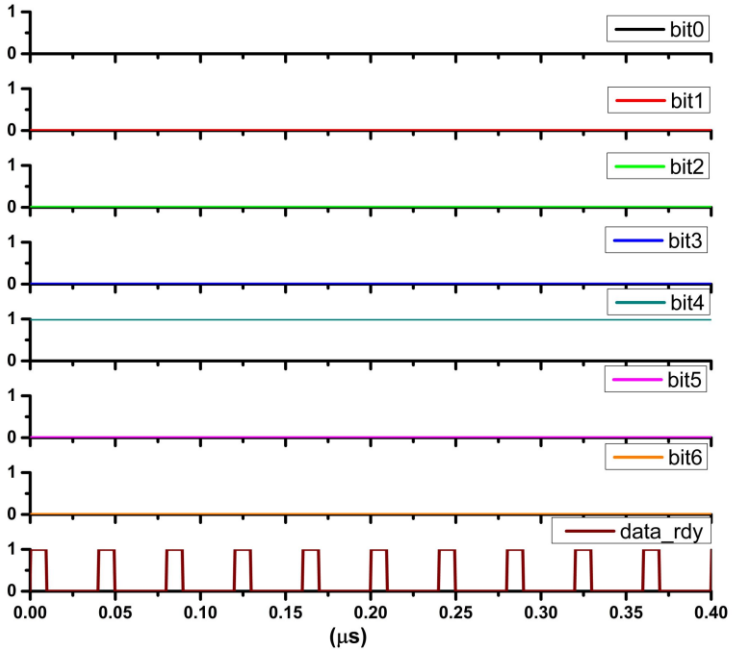


Figure 45: Initial Transient Measurement Result for V_{inp}=0.5V, V_{inn}=1V, resulting in '0000100'

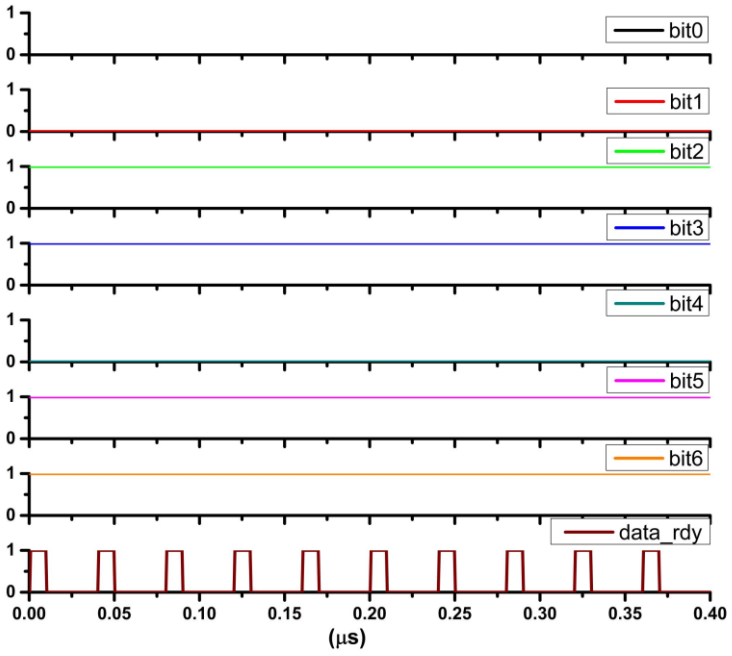


Figure 46: Initial Transient Measurement Result for V_{inp}=0.6V, V_{inn}=0.9V, resulting in '0000100'

the underlying noise coming from the PCB, we modified the PCB manually, cutting away unnecessary clock paths that were implemented to test other circuits such as test clock generator circuits and four way time-interleaved test circuits, testing

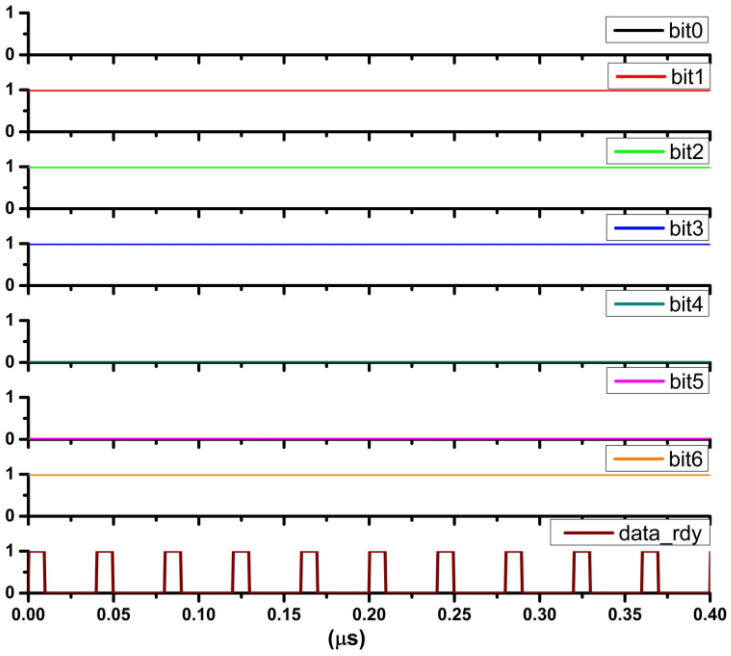


Figure 47: Initial Transient Measurement Result for V_{inp}=0.7V, V_{inn}=0.8V, resulting in '0111001'

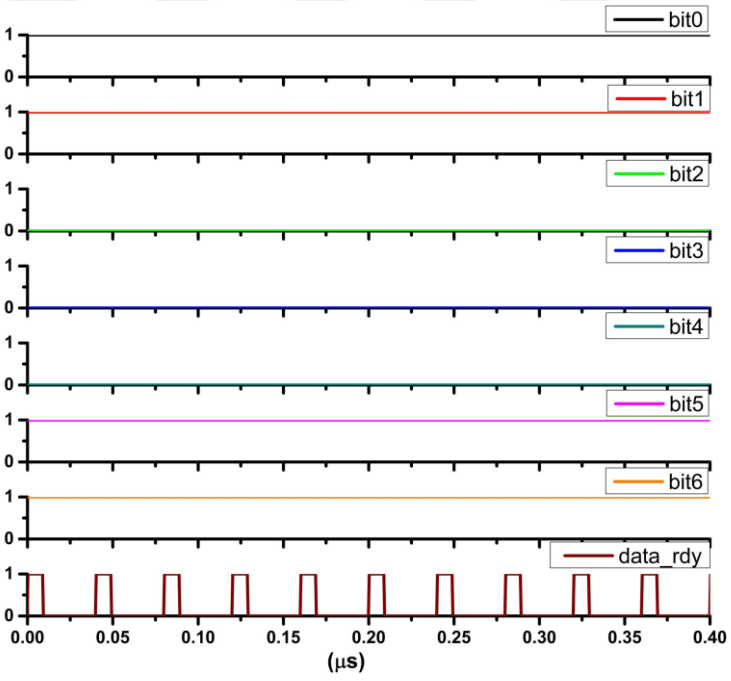


Figure 48: Initial Transient Measurement Result for V_{inp}=0.8V, V_{inn}=0.7V, resulting in '1100011'

only single channel. The new measurement results for the same clock frequency of 100 MHz (25MHz operation) and same input cases have been taken for longer times (in the order of ms) to confirm the output is stable. These cases are shown

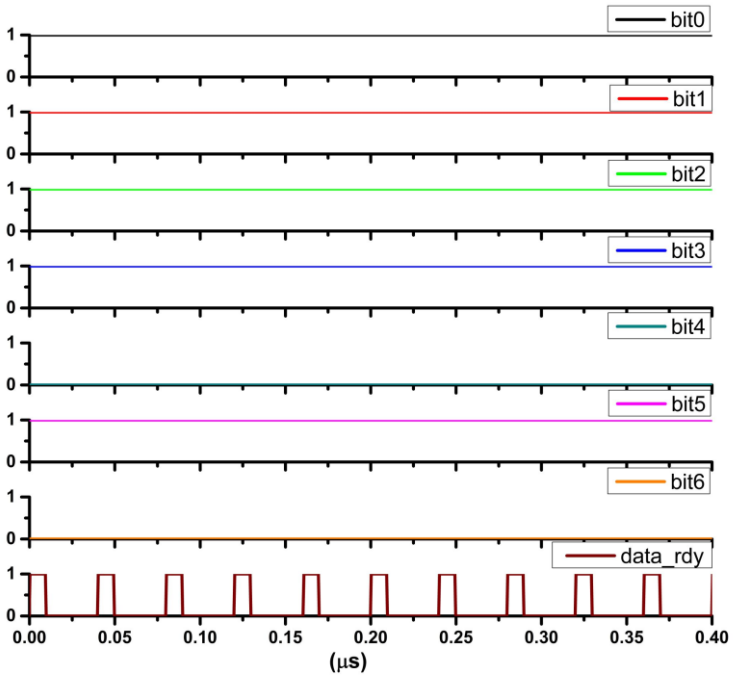


Figure 49: Initial Transient Measurement Result for V_{inp}=0.9V, V_{inn}=0.6V, resulting in '1111010'

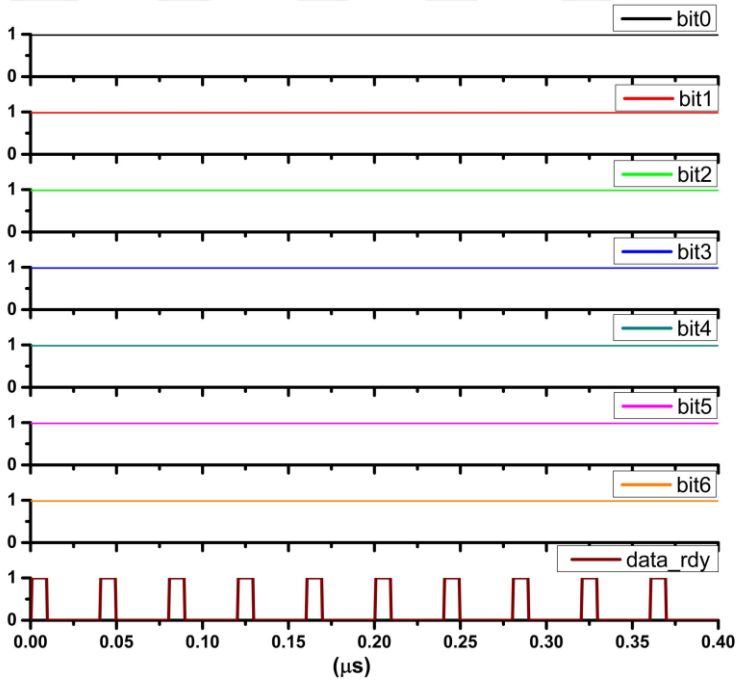


Figure 50: Initial Transient Measurement Result for V_{inp}=1V, V_{inn}=0.5V, resulting in '1111111'

in Fig. 52, Fig. 53, Fig. 54, Fig. 55, Fig. 56 and Fig. 57, respectively. The noise evidently reduced significantly, and is stable for the long capture times. However, measurement setup is extremely sensitive to outside interference and movement of

the digital oscilloscope probe tips.

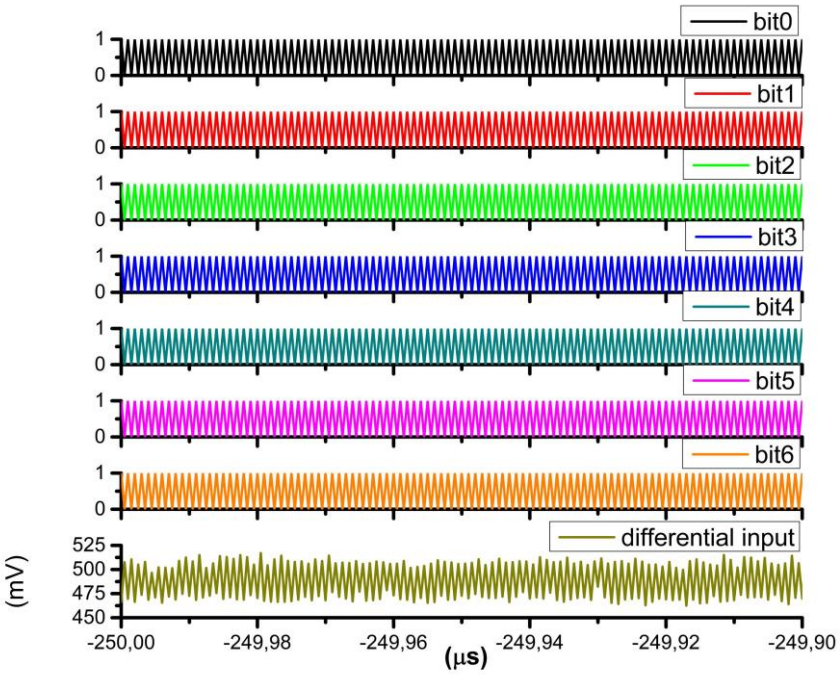


Figure 51: Noisy and Corrupted Transient Measurement Result for V_{inp}=1V, V_{inn}=0.5V with 500 MHz clock input (125MHz Operation)

Indeed, the noise can still be seen on the inputs to the ADC. The exaggerated version with 500MHz clock input results in about 75mV V_{pp} high frequency noise on the differential ADC input as shown in Fig. 51. All the bits are greatly coupled to the noise in the input, which is actually given as 0.5V DC but corrupted by the digital noise. This effect is still under investigation as of the time of the writing of this thesis as this severe toggling only occurs at high operating frequencies, 100MHz clock input does not suffer as severely.

As seen from Fig. 52, the biggest input case of 500mV is now converted correctly to the highest digital code.

In Fig.53, for a 300mV differential input of 0.9V-0.6V, we see that we obtain 1111100 which actually corresponds to 437.5mV differential input.

In Fig.54, for a 100mV differential DC input of 0.8V-0.7V, we see that we obtain 1110000 which actually corresponds to 281.3mV differential input.

In Fig.55, for a -100mV differential DC input of 0.8V-0.7V, we see that we obtain 0001111 which actually corresponds to -296.9mV differential input.

In Fig.56, for a -300mV differential DC input of 0.6V-0.9V, we see that we obtain

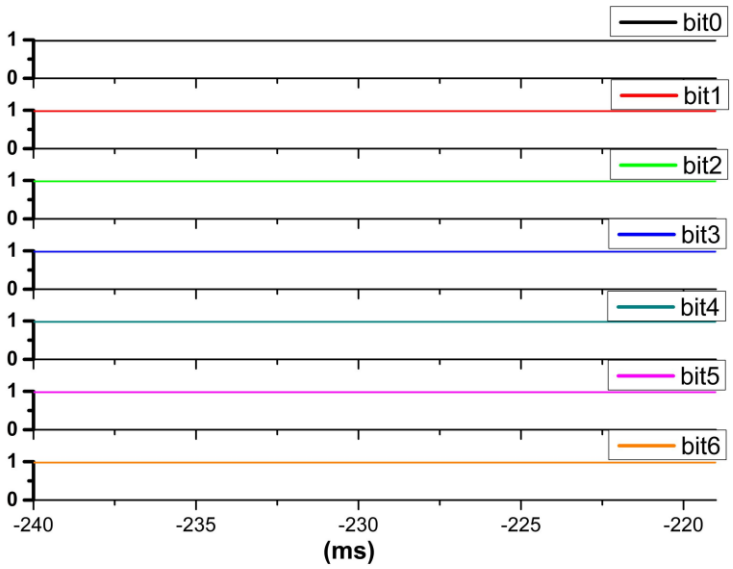


Figure 52: Final Transient Measurement Result for V_{inp}=1V, V_{inn}=0.5V, resulting in '1111111'

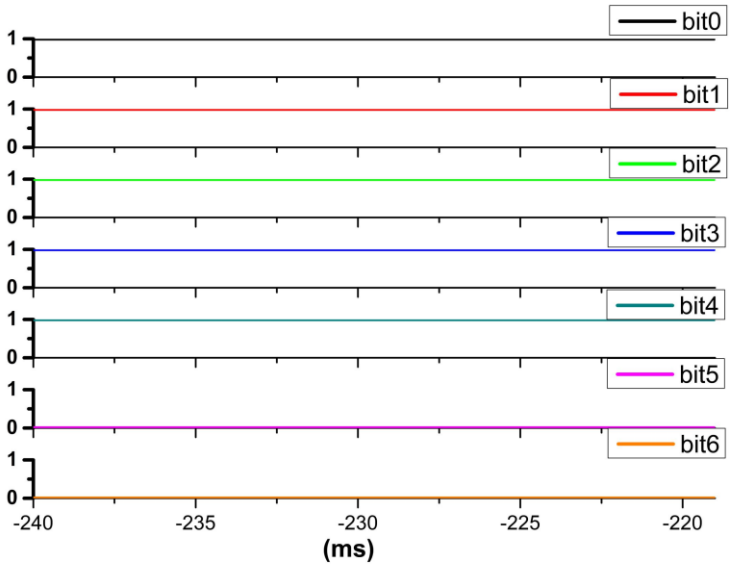


Figure 53: Final Transient Measurement Result for V_{inp}=0.9V, V_{inn}=0.6V, resulting in '1111100'

0001111 which actually corresponds to -453.1mV differential input.

In Fig.57, for a -500mV differential DC input of 0.5V-1V we see that we obtain 0000000 which is the correct code.

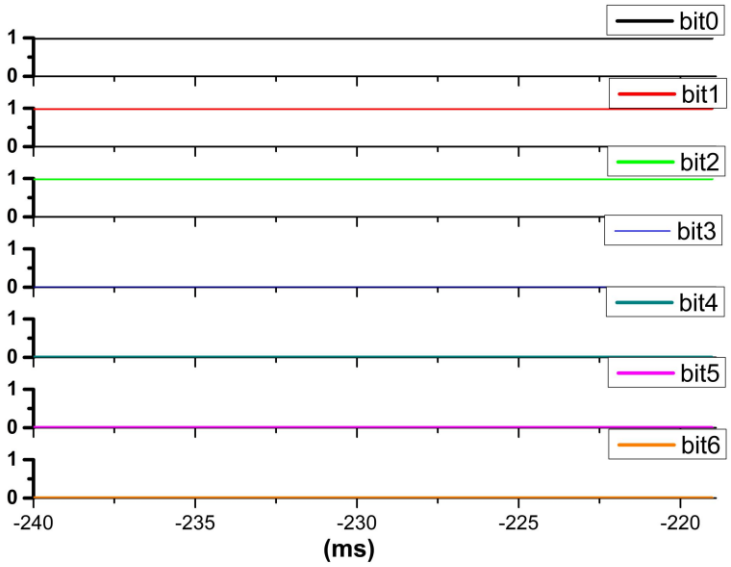


Figure 54: Final Transient Measurement Result for V_{inp}=0.8V, V_{inn}=0.7V, resulting in '1110000'

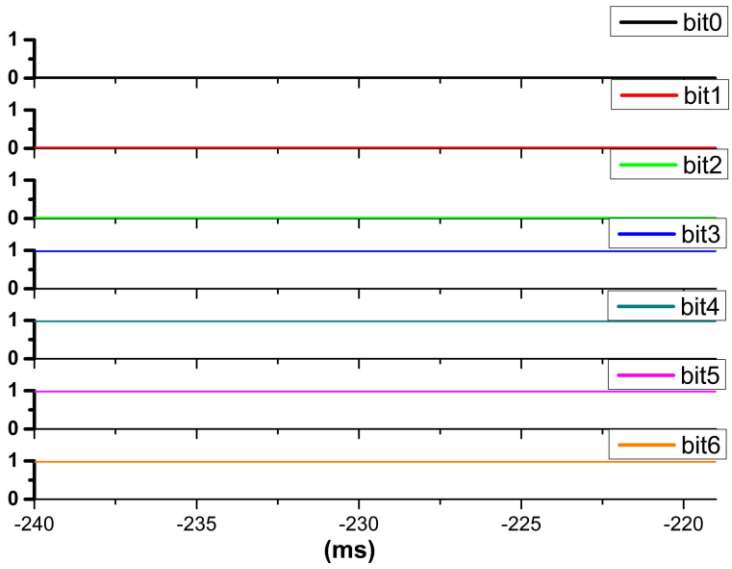


Figure 55: Final Transient Measurement Result for V_{inp}=0.7V, V_{inn}=0.8V, resulting in '1111111'

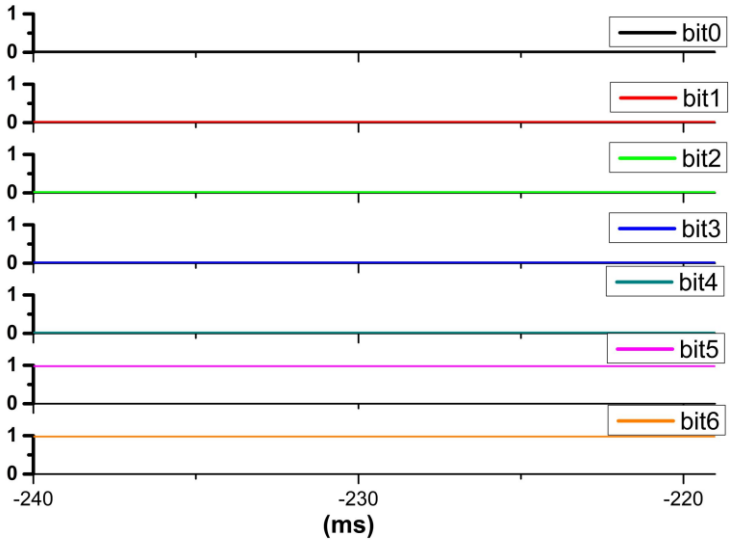


Figure 56: Final Transient Measurement Result for V_{inp}=0.6V, V_{inn}=0.9V, resulting in '0000011'

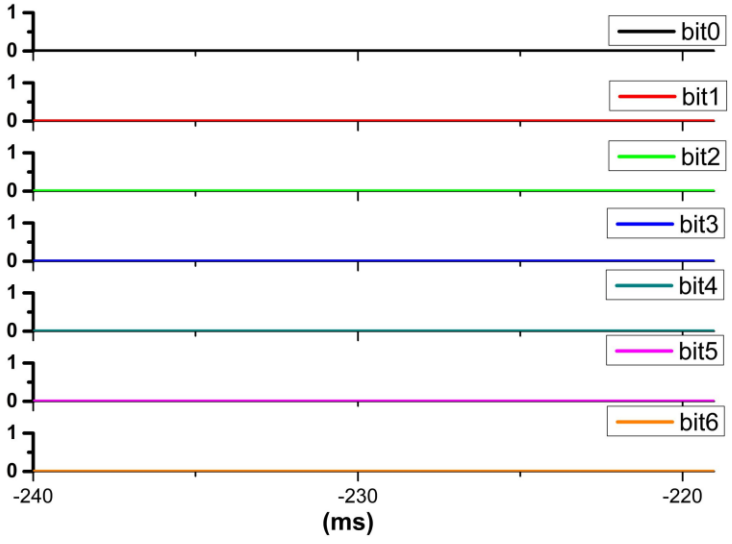


Figure 57: Final Transient Measurement Result for V_{inp}=0.5V, V_{inn}=1V, resulting in '0000000'

5 Conclusion & Future Work

5.1 Summary of Work

The SAR ADCs have benefited a boom in research thanks to their easily scalable digital circuitry which takes full advantage of aggressive CMOS scaling. Indeed, the SAR architectures have become the choice for not only low power applications but also for moderate resolution and high speed applications via time interleaving. In this work, a 6-bit SAR ADC has been designed and fabricated in 90nm. It has been time-interleaved up to four channels with each channel capable of operating at 178MHz. The implemented ADC features redundancy in the SAR algorithm for V_{CM} based switching architecture with top plate sampling and full custom asynchronous control logic that enables faster loops in the SAR to increase the single channel speed. A single channel sampling speed of 178 MHz is achieved in simulations and the simulation results show +/- 0.28 LSB INL and 0.24 LSB DNL and 7.6 mW power consumption. From these parameters FoM_W is calculated to be 181 fJ/conv and the FoM_s is calculated to be 143.53 dB.

5.2 Future Work

The future work includes the complete characterization of the dynamic characteristics of the ADC experimentally. This has not been possible due to the significant ground noise in the PCB corrupting the measurements, however, it will be done as soon as possible with a new PCB design shortly. One significant shortcoming of this thesis is that the time-interleaving was done without gain/timing/bandwidth calibration schemes aside from extra careful low skew differential design and routing of non-overlapping clocks. Consequently, the current design is limited in its time-interleaved channel count and may degrade beyond acceptable limits in its dynamic and static performance. As discussed, the time-interleaving method comes with diminishing returns in speed enhancement. It becomes a necessity to implement good calibration schemes with increasing channel counts to avoid performance degradation. However, the overhead associated with calibration is also limited as the current calibration schemes can only go so far. This is why further enhancement of the sub-

ADC single channel speed/performance needs to be pursued, as was done in this thesis to improve the time-interleaved ADC performance even more. As the SAR architecture scales very well with switching speed, it is also possible to implement a higher speed time-interleaved ADC directly without any modification to the design, just by upgrading the technology node which comes with increased cost.

As a long-term future work, trimming can be implemented to improve linearity and the total harmonic distortion. The DNL error shown in the measurements can be decreased by improving the ADC grounding on the PCB and reducing the coupling from the fast clock signals. If the new PCB to be designed is not sufficient, then the analog components of the design can be moved to an isolated NWELL to separate its substrate as much as possible from the noisy one in the next iteration of the design.

A Appendix

In this appendix, the MATLAB code used for characterizing the SAR ADC's static parameters of INL and DNL as well as its input-output transfer characteristics is given. The following code reads the output bits (in a .csv format) that were generated by applying a ramp test signal and then processes the histogram of the code hits, creating the corresponding ADC transfer characteristic with actual code widths and calculating the DNL and INL for each width.

clear; clc; p = [13 8 4 3 2 1];
data = csvread(śar_data_100u_inl_dnl_may18__POSTLAYOUT_4channel1.csv');
data = data(1:end,:); len = length(data); vin = data(:,1)-data(:,2); bits = data(:,3:end);
a = transpose((2*bits(:,1:end-1)-1).*repmat(p,len,1));
dout = 32+transpose(sum(a))+bits(:,end)-1; figure(1); plot(vin, dout); h=histogram(dout,0:64);
counts = h.Values; counts = counts(2:end-1); avg = mean(counts); dnl = (counts/avg)
- 1; inl = cumsum(dnl); figure(2); plot(inl); hold on; plot(dnl); hold off; legend('INL','DNL') export_fig -pdf; figure(3); plot(dout);

B Appendix

In this appendix, the Verilog-A codes used for capturing the SAR ADC's output bits during static and dynamic simulations are given. Verilog-A is a hardware description language for analog circuits designed for the Spectre simulator.

module write_data_to_file (dcm6, bits, vinp, vinn); input dcm6;
input [6:0] bits;
input vinp;
input vinn;
voltage [6:0] bits;
voltage dcm6;
voltage vinp;
voltage vinn;
integer fname;
integer bit;
analog begin
//Initialization
@(initial$_s tep$)*begin*
$fname$ =fopen("SNDRRealTrial.csv"); $//fwrite(fname, "I'm\ in\ Initialization")$;
end//*Writing event*
@($cross(V(dcm6) - 0.6, +1)$)*begin*
//fwrite(fname, "I'm in the event");
$fwrite(fname, "generate\ x\ (0, 6)\ begin$
$bit = (V(bits[x]) > 0.7)?1 : 0;$
fwrite(fname, "if (x ¡ 6)
$fwrite(fname, ",");$
end
fwrite(fname, "");end
//Close file
//@(final$_s tep$)
//fclose(fname);

```
end
endmodule `include "constants.vams" `include "disciplines.vams"
   module write_data_to_file (dcm6, bits, vinp, vinn); input dcm6;
input [6:0] bits;
input vinp;
input vinn;
voltage [6:0] bits;
voltage dcm6;
voltage vinp;
voltage vinn;
integer fname;
integer bit;
analog begin
//Initialization
@(initial_step)begin
fname =fopen("SNDRRealTrial.csv"); //fwrite(fname,"I'm in Initialization");
end//Writing event
@(cross(V(dcm6) - 0.6, +1))begin
//fwrite(fname, "I'm in the event");
fwrite(fname,"generate x (0,6) begin
bit = (V(bits[x]) > 0.7)?1 : 0;
fwrite(fname, "if (x < 6)
fwrite(fname,",");
end
fwrite(fname, "");end
//Close file
//@(final_step)
//fclose(fname);
end
endmodule
```

C Appendix

The schematics of the PCB designed for evaluating the single channel ADC is given here.

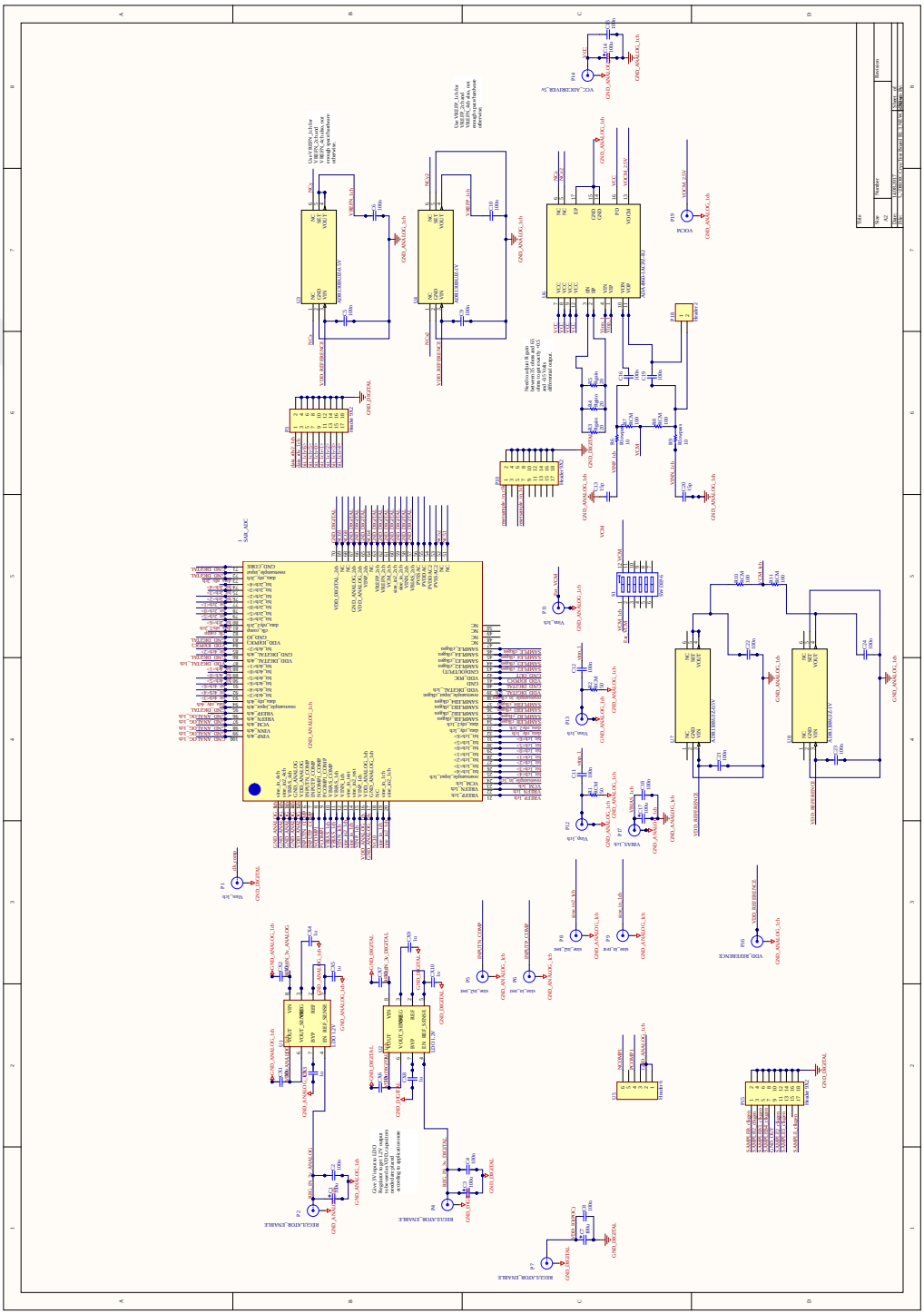


Figure 58: ADC Evaluation Board

References

[1] B. Murmann, ‘‘Adc performance survey 1997-2017, [online]. available: http://web.stanford.edu/ murmann/adcsurvey.html,’’ 2017.

[2] W. Ball and H. Coxeter, *Mathematical Recreations and Essays*. Dover Recreational Math Series, Dover Publications, 1987.

[3] Z. Zhu, Y. Xiao, and X. Song, ‘‘Vcm-based monotonic capacitor switching scheme for sar adc,’’ *Electronics Letters*, vol. 49, pp. 327--329, February 2013.

[4] E. Rahimi and M. Yavari, ‘‘Energy-efficient high-accuracy switching method for sar adcs,’’ *Electronics Letters*, vol. 50, pp. 499--501, March 2014.

[5] M. J. Pelgrom, A. C. Duinmaijer, and A. P. Welbers, ‘‘Matching properties of mos transistors,’’ *IEEE Journal of solid-state circuits*, vol. 24, no. 5, pp. 1433--1439, 1989.

[6] C. E. Shannon, ‘‘Communication in the presence of noise,’’ *Proceedings of the IRE*, vol. 37, pp. 10--21, Jan 1949.

[7] M. Pelgrom, *Analog-to-Digital Conversion*. Springer International Publishing, 2017.

[8] F. Maloberti, *Data Converters*. Springer Publishing Company, Incorporated, 1st ed., 2010.

[9] S. Pavan, R. Schreier, and G. Temes, *Understanding Delta-Sigma Data Converters*. IEEE Press Series on Microelectronic Systems, Wiley, 2016.

[10] M. Bolatkale, L. Breems, and K. Makinwa, *High Speed and Wide Bandwidth Delta-Sigma ADCs*. Analog Circuits and Signal Processing, Springer International Publishing, 2014.

[11] ‘‘Ieee standard for terminology and test methods for analog-to-digital converters,’’ *IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000)*, pp. 1--139, Jan 2011.

[12] K. H. Lundberg, ‘‘Analog-to-digital converter testing,’’

[13] R. H. Walden, ‘‘Analog-to-digital converter survey and analysis,’’ *IEEE Journal on Selected Areas in Communications*, vol. 17, pp. 539--550, Apr 1999.

[14] B. Murmann, ‘‘A/d converter trends: Power dissipation, scaling and digitally assisted architectures,’’ in *2008 IEEE Custom Integrated Circuits Conference*, pp. 105--112, Sept 2008.

[15] A. M. A. Ali, A. Morgan, C. Dillon, G. Patterson, S. Puckett, P. Bhoraskar, H. Dinc, M. Hensley, R. Stop, S. Bardsley, D. Lattimore, J. Bray, C. Speir, and R. Sneed, ‘‘A 16-bit 250-ms/s if sampling pipelined adc with background calibration,’’ *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2602--2612, Dec 2010.

[16] B. Razavi, ‘‘Design considerations for interleaved adcs,’’ *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 1806--1817, Aug 2013.

[17] W. C. Black and D. A. Hodges, ‘‘Time interleaved converter arrays,’’ *IEEE Journal of Solid-State Circuits*, vol. 15, pp. 1022--1029, Dec 1980.

[18] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, ‘‘Explicit analysis of channel mismatch effects in time-interleaved adc systems,’’ *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, pp. 261--271, Mar 2001.

[19] S. Louwsma, E. van Tuijl, and B. Nauta, *Time-interleaved Analog-to-Digital Converters*. Analog Circuits and Signal Processing, Springer Netherlands, 2010.

[20] N. Tartaglia, *General Trattato di numeri et misure di Nicolo Tartaglia*. No. v. 4, 1560.

[21] W. M. Goodall, ‘‘Telephony by pulse code modulation,’’ *The Bell System Technical Journal*, vol. 26, pp. 395--409, July 1947.

[22] S. C, ‘‘Code modulation communication system,’’ Nov. 9 1948. US Patent 2,453,461.

[23] B. M. Gordon and E. T. Colton, ‘‘Signal conversion apparatus,’’ Aug. 22 1961. US Patent 2,997,704.

[24] B. Murmann, ‘‘The successive approximation register adc: a versatile building block for ultra-low- power to ultra-high-speed applications,’’ *IEEE Communications Magazine*, vol. 54, pp. 78--83, April 2016.

[25] J. L. McCreary and P. R. Gray, ‘‘All-mos charge redistribution analog-to-digital conversion techniques. i,’’ *IEEE Journal of Solid-State Circuits*, vol. 10, pp. 371--379, Dec 1975.

[26] R. E. Suarez, P. R. Gray, and D. A. Hodges, ‘‘All-mos charge-redistribution analog-to-digital conversion techniques. ii,’’ *IEEE Journal of Solid-State Circuits*, vol. 10, pp. 379--385, Dec 1975.

[27] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, ‘‘A 10-bit 50-ms/s sar adc with a monotonic capacitor switching procedure,’’ *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 731--740, April 2010.

[28] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins, and F. Maloberti, ‘‘A 10-bit 100-ms/s reference-free sar adc in 90 nm cmos,’’ *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1111--1121, June 2010.

[29] V. Hariprasath, J. Guerber, S. H. Lee, and U. K. Moon, ‘‘Merged capacitor switching based sar adc with highest switching energy-efficiency,’’ *Electronics Letters*, vol. 46, pp. 620--621, April 2010.

[30] C. Yuan and Y. Lam, ‘‘Low-energy and area-efficient tri-level switching scheme for sar adc,’’ *Electronics Letters*, vol. 48, pp. 482--483, April 2012.

[31] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, ‘‘A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture,’’ *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 523--527, Apr 1993.

[32] S. W. M. Chen and R. W. Brodersen, ‘‘A 6-bit 600-ms/s 5.3-mw asynchronous adc in 0.13-$muhboxm$ cmos,’’ *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2669--2680, Dec 2006.

[33] A. H. Chang, H. S. Lee, and D. Boning, ‘‘A 12b 50ms/s 2.1mw sar adc with redundancy and digital background calibration,’’ in *2013 Proceedings of the ESSCIRC (ESSCIRC)*, pp. 109--112, Sept 2013.

[34] X. Yue, ‘‘Determining the reliable minimum unit capacitance for the {DAC} capacitor array of {SAR} {ADCs},’’ *Microelectronics Journal*, vol. 44, no. 6, pp. 473 -- 478, 2013.

[35] P. Harpe, B. Busze, K. Philips, and H. de Groot, ‘‘A 0.47 x2013;1.6mw 5bit 0.5 x2013;1gs/s time-interleaved sar adc for low-power uwb radios,’’ in *2011 Proceedings of the ESSCIRC (ESSCIRC)*, pp. 147--150, Sept 2011.

[36] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. V. der Plas, ‘‘Noise analysis of regenerative comparators for reconfigurable adc architectures,’’ *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, pp. 1441--1454, July 2008.

[37] B. Razavi, ‘‘The strongarm latch [a circuit for all seasons],’’ *IEEE Solid-State Circuits Magazine*, vol. 7, pp. 12--17, Spring 2015.

[38] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, ‘‘A 10-b 50-ms/s 820- muw sar adc with on-chip digital calibration,’’ *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, pp. 410--416, Dec 2010.

[39] H. Wei, P. Zhang, B. D. Sahoo, and B. Razavi, ‘‘An 8 bit 4 gs/s 120 mw cmos adc,’’ *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1751--1761, Aug 2014.

[40] B. Razavi, ‘‘The bootstrapped switch [a circuit for all seasons],’’ *IEEE Solid-State Circuits Magazine*, vol. 7, pp. 12--15, Summer 2015.