

**Design and Fabrication of Electrostatically Actuated
Nanotweezers by Guided Self-assembly**

by

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This is to certify that I have examined this copy of a master's thesis by

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ABSTRACT

Nano-Electro-Mechanical Systems (NEMS) with nano-scale end-effectors, which are capable of interacting with objects with nano-metric precision, have many applications in nano-science and technology. Among these, nanotweezers have a significant importance, which enable handling and manipulation of nano-scale objects such as DNA molecules, carbon nanotubes, nanowires and nano particles.

This M.S. thesis deals with the design and fabrication of electrostatically actuated nanotweezers with nanowire end-effectors fabricated by guided self-assembly. Primary aim is to achieve the integration of nanowires into microelectronics in a single batch process, reducing process complexity and enabling possible design variations. Secondary aim is the design of an actuation mechanism with nano-scale end-effectors and providing a high-precision control.

Major accomplishments of this research can be listed as (1) optimization of the electro-deposition process for nanowire fabrication by guided self-assembly, (2) design and analysis of an electrostatically driven comb actuation mechanism for the nanotweezers, (3) design and analysis of an alternative thermal actuation mechanism for the nanotweezers and (4) fabrication of the nanotweezers in the Department of Micro and Nanotechnology (MIC) at Technical University of Denmark (DTU), in Copenhagen and mechanical testing and characterization of nanotweezers again at MIC and Koç University (KU) cleanroom facilities.

Keywords: NEMS, nanotweezers, nanowire, self-assembly, electro-deposition, comb actuator, thermal actuator.

ÖZET

Objelerle nano metrik hassasiyetle etkileşim kabiliyeti olan nano ölçekli uçlara sahip Nano-Elektro-Mekanik Sistemlerin (NEMS) nano bilim ve teknoloji alanlarında pek çok uygulaması bulunmaktadır. Bunların arasında, DNA molekülleri, karbon nano tüpler, nano teller ve nano parçacıklar gibi nano ölçekli objelerin tutulmasını ve hareket ettirilmesini mümkün kılan nano cımbızların önemi büyüktür.

Bu yüksek lisans tezi, elektrostatik hareket prensibi ile çalışan ve yönlendirilmiş kendinden birleşme metodu ile üretilen nano tel uçlara sahip nano cımbızların tasarım ve üretimi ile ilgilidir. Başlıca amaç, işlem karmaşıklığını azaltacak ve olası tasarım değişikliklerini mümkün kılacak şekilde, nano tellerin mikro elektronik ile tek bir üretim serisi içerisinde bütünleşmesini sağlamaktır. İkinci bir amaç ise, yüksek hassasiyetle kontrol sağlayan ve nano ölçekli uçlara sahip bir hareket mekanizmasının tasarımınıdır.

Bu tezin ana başarıları, (1) yönlendirilmiş kendinden birleşme yöntemi ile nano tel üretimi için elektrodepozisyon işleminin optimizasyonu, (2) elektrostatik prensiple hareket eden taraklardan oluşan bir hareket mekanizmasının tasarım ve analizi, (3) nano cımbızlar için alternatif bir termal hareket mekanizmasının tasarım ve analizi, (4) nano cımbızların Kopenhag'daki, Danimarka Teknik Üniversitesi (DTU) Mikro ve Nano Teknoloji Departmanı'nda (MIC), üretilmesi ve (5) nano cımbızların mekanik test ve karakterizasyonunun yine MIC ve Koç Üniversitesi (KU) temiz oda tesislerinde gerçekleştirilmesi şeklinde sıralanabilir.

Anahtar kelimeler: NEMS, nano cımbızlar, nano teller, kendinden birleşme, elektrodepozisyon, tarak hareket mekanizması, termal hareket mekanizması.

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NOMENCLATURE

C	Total capacitance between a pair of interdigitated comb fingers
C_x, C_y	Capacitances due to interaction of the lateral and longitudinal comb faces
h	Height of the actuator device
w	Width of comb fingers
t	Zero voltage overlap length between comb fingers
g_x, g_y	Gap distances between comb fingers in x- and y-directions
x	Displacement in x-axis
ε	Permittivity
ε_0	Permittivity of free space ($= 8.854 \times 10^{-12}$ F/m)
C_{total}	Total capacitance between a comb actuator pair
N_f	Number of comb fingers on a comb actuator
W_{es}	Capacitive energy
V	Applied potential difference
F_{es}	Electrostatic force
$k_{es,x}$	Electrostatic spring constant in x-axis
$k_{mech,x}$	Mechanical spring constant in x- axis
$k_{mech,y}$	Mechanical spring constant in y- axis
$k_{mech,z}$	Mechanical spring constant in z- axis

k_x, k_y, k_z	Spring constants of a double-folded cantilever beam in x-, y- and z-axes
E_s	Modulus of elasticity of a spring
h_s	Height of a spring
w_s	Cantilever width of a spring
l_{s1}, l_{s2}	Long and short cantilever lengths of a spring
l_s	Cantilever length of a spring, where $l_{s1} = l_{s2} = l_s$
F_{mech}	Mechanical force
F_{net}	Total force
$L_{c,i}$	Length of the i^{th} cantilever of a three-beam thermal actuator due to a current passed through
L_c	Original cantilever length of a three-beam thermal actuator
T_i	Average temperature of the i^{th} cantilever of a three-beam thermal actuator
α	Coefficient of thermal expansion
F_i	Force applied to the i^{th} cantilever of a three-beam thermal actuator by the end bar
$k_{c,i}$	Tensile spring constant of the i^{th} cantilever of a three-beam thermal actuator
d	End-displacement of a three-beam thermal actuator due to a current passed through
θ	Bending angle of a three-beam thermal actuator
w_c	Cantilever width of a three-beam thermal actuator
ΔT	Beam average temperature difference between hot and cold beams of a three-beam thermal actuator
$T(x)$	Temperature distribution equation

$J(x)$	Current density
ρ	Electrical conductance
κ	Heat conductivity
I	Current
T_{max}	Maximum temperature of a three-beam thermal actuator due to a current passed through
g_c	Gap between cantilever beams in a three-beam thermal actuator
E	Electric field
∇	Gradient operator
V_0	Operation voltage
M	Anode metal in an electroplating reaction
n	Number of electrons involved in an electroplating reaction
Q	Electric charge
Z	Electrochemical equivalent (Constant of proportionality)
w_d	Deposit weight
t_e	Elapsed time
F	Faraday's constant ($= 96,487 \text{ C mol}^{-1}$)
N_A	Avogadro's number ($= 6.0225 \times 10^{23} \text{ mol}^{-1}$)
e	Charge of a single electron ($= 1.6021 \times 10^{-19} \text{ C}$)
w_{eq}	Fraction of a molar (atomic) unit of reaction for transporting one electron
A_{wt}	Atomic weight
h_d	Deposit thickness
V_d	Deposit volume
a	Electroplating area

ρ_d	Deposit density
t_d	Deposit thickness
σ_f	Initial film stress
E_s	Young's modulus of the substrate
ν_s	Poisson's ratio of the substrate
h_s	Substrate thickness
h_f	Film thickness
$1/R_1$	Initial radius of curvature
$1/R_2$	Final radius of curvature

Chapter 1

INTRODUCTION

1.1. Introduction

Handling and manipulation of nano-scale objects, such as DNA molecules, carbon nanotubes (CNTs), nanowires and nanoparticles, is among the most important problems faced by nanotechnology. Furthermore, achieving physical interaction with such objects will certainly yield to great advancements in both elementary and applied science applications.

Solution to this problem will probably be revealed by the emerging field of Nano Electro Mechanical Systems (NEMS). As an example, *nanotweezers*, composed of a pair of nano-scale end-effectors for interaction with matter and an actuation mechanism with nanometric precision, are promising devices due to their operational simplicity and wide variety of applications. However, there two main challenges hindering the progress in the field of nanotweezers: fabrication of nano-scale end-effectors, mostly in the form of nanowires or nanotubes, and their integration with the actuation mechanism.

An alternative nanotweezers fabrication method will be proposed in this thesis, which constitutes a bridge between top-down and bottom-up nanofabrication techniques and hence, makes integration of nanotechnology with Micro-Electro-Mechanical Systems (MEMS) by utilizing *Guided Self-assembly* in the fabrication of nanowire end-effectors, possible.

In this chapter, position of nanotweezers among other alternative manipulation tools, such as atomic force microscope (AFM) or optical tweezers will be discussed, together with current nanotweezers and their demands, initially. Then, possible application areas of nanotweezers in both elementary and applied sciences will be presented. Afterwards, challenges encountered in the fabrication of nano-scale end-effectors, using top-down and bottom-up approaches, will be introduced, pointing out the advantages of guided self-assembly over both fabrication philosophies. Finally, various actuation alternatives for nanotweezers, including electrostatic, thermal, electromagnetic and piezoelectric actuators, will be compared and the chapter will be concluded with outline of the thesis.

1.2. Possible Applications of Nanotweezers

1.2.1. Applications in Elementary Sciences

Chemical composition, microstructure and dimensions of a material, as well as their relationship with resulting electrical, mechanical, magnetic, thermal and optical properties become indeterminate at nano-scale. Although it is possible to perform chemical composition and microstructure measurements easily, by means of various microscopic techniques, measurement of transport properties is rather challenging due to difficulties in achieving interaction with test samples. If succeed, nanotweezers will be promising tools for science world, making basic research at nano-scale possible.

Considering mechanical point of view, existing methods utilized in performing tension tests on CNTs rely on the attachment of a single nanotube to an Atomic Force Microscope (AFM) tip by difficult means. Afterwards, either the nanotube is transferred to a MEMS device, where testing will be performed [1], or tension test is performed directly between two nanotube ends [2] (Figure 1.1).

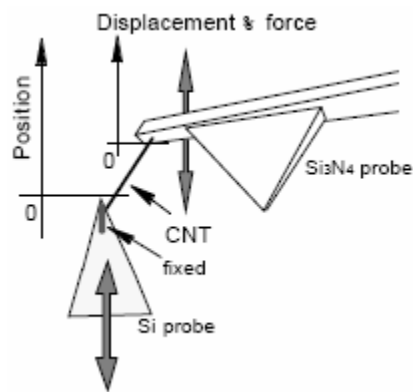


Figure 1.1 Schematic illustration of a force curve measurement [2]

In both methods, selection of a single nanotube and firmly attachment of this nanotube to AFM tips, which relies on either Van der Waals forces [1] or welding of a nanotube to the AFM tip via an amorphous carbon coating using electron beams [2, 3], are critical. First method is a coincidental approach since controlling the number of CNT's adhering to the AFM tip or the period that they remain attached is hardly possible. Second method is rather time consuming, where half of the prepared samples were reported to have result in failure [3]. Using a tweezers-like NEMS tool instead of an AFM tip will enable both selection of a specific nanotube among many others and its precise assembly to the MEMS device, on which the tension test will be performed.

Similarly, such devices as nanotweezers will be quite beneficial for electrical measurements carried out at nano-scale, where conductivity becomes quantized rather than obeying Ohm's Law due to reduced dimensions. Furthermore, importance of characterization of metallic or semi-conducting behaviors of nanowires will add to the value of electrical measurements. Many experimental tools, including electrodes for electrical connection [4] (Figure 1.2) or nano-scale probes [5], are necessary in order to perform such conductivity measurements on nanowires.

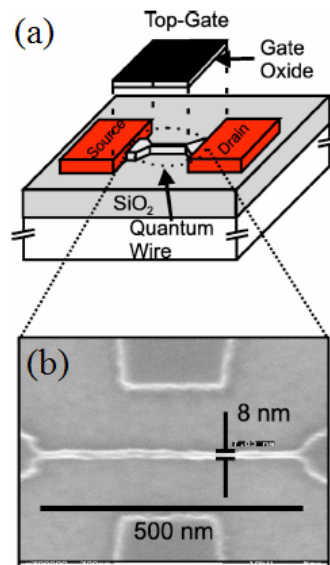


Figure 1.2 (a) Schematic illustration of a SOI nanowire where the metallic top gate is separated by a SiO₂ layer with (b) SEM micrograph of the nanowire in the inset [4]

Current technology requires either fabrication of electrodes together with nanowires by difficult means as e-beam lithography, or cutting of remaining nanowires by focusing an ion beam so that only a single nanowire is left between two electrodes [6].

Applying the same philosophy suggested for mechanical applications to the electrical point of view, nanotweezers will enable electrical measurements on nanowires by transporting them one by one to a MEMS measurement device, on which the testing will be performed, and removing them away from the device afterwards. In addition to being time effective, this method will make testing of an individual nanowire on more than one device or using the same testing device for a number of nanowires (Figure 1.3(a)), possible. In the first method, comparison of measurements for various samples will yield reliable results since the device remains stationary, where the second method will enable measurement of both mechanical and electrical properties of an individual sample or calibration of testing devices using a device, which is calibrated using a standard sample.

Furthermore, since nano-scale end-effectors can serve as nanoprobes, four-point resistivity measurements will become easier by contacting the same nanowire at four different locations, with two nanotweezers at the same time (Figure 1.3(b)).

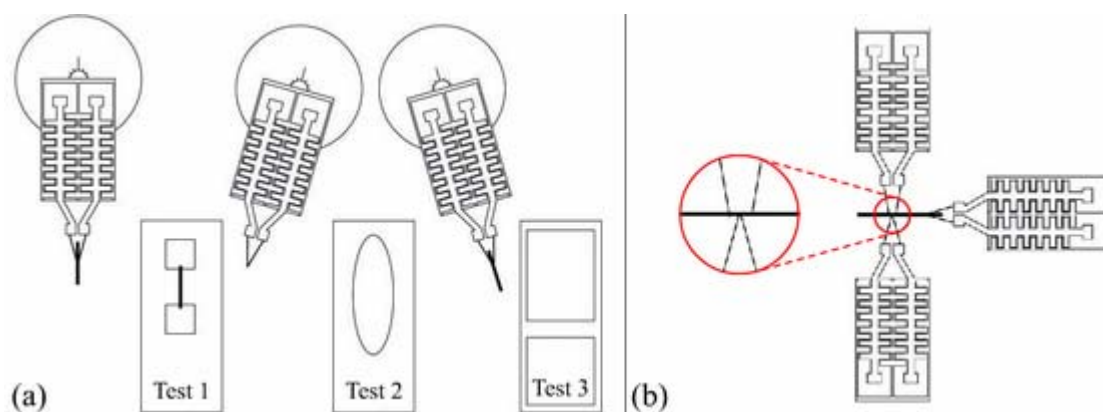


Figure 1.3 Schematic illustration of two potential applications of nanotweezers in elementary sciences: (a) a series of measurements on the same sample and (b) four-point resistivity measurement [7]

1.2.2. Applications in Applied Sciences

In the field of molecular electronics, it is possible to constitute various devices by combining 1D construction elements, such as nanowires, nanotubes and DNA molecules. Transistors, which are built by crossing two semi-conducting nanowires [8] (Figure 1.4) or two carbon nanotubes (CNTs) [9] (Figure 1.5) over each other and DNA-based photo-detectors [10] can be given as examples.

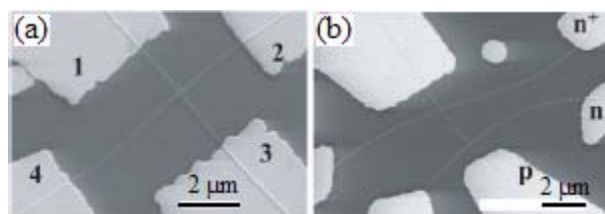


Figure 1.4 FESEM images of (a) a crossed Si nanowire junction with Al/Au contacts and (b) Si nanowire bipolar transistor with three wires labeled as n^+ , p, and n used as emitter, base, and collector, respectively [8]

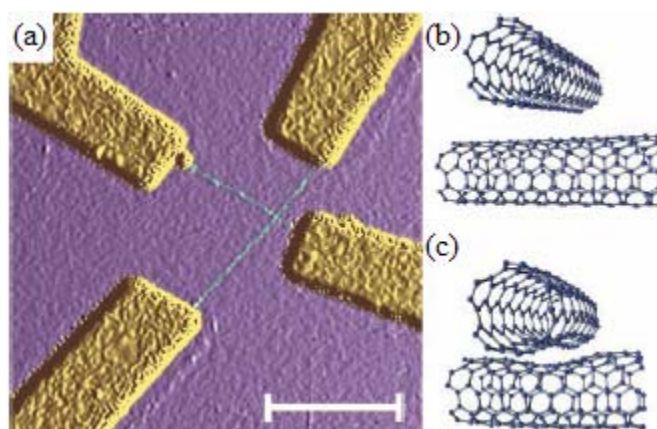


Figure 1.5 (a) Tapping mode AFM image (amplitude signal) of a crossed SWNT device where two single-walled carbon nanotubes (green) span between the Cr/Au electrodes (yellow) and ((b) and (c)) structures used in conductance calculations [9]

In addition to these existing applications, nanotweezers are likely to yield noteworthy revolutions in various fields, such as manipulation and position control at nano-scale in robotics and assembly (Figure 1.6(a)), gene repair in biological systems (Figure 1.6(b)), high density data storage environments in computer technology or artificially made perfect materials with high-strength in material science.

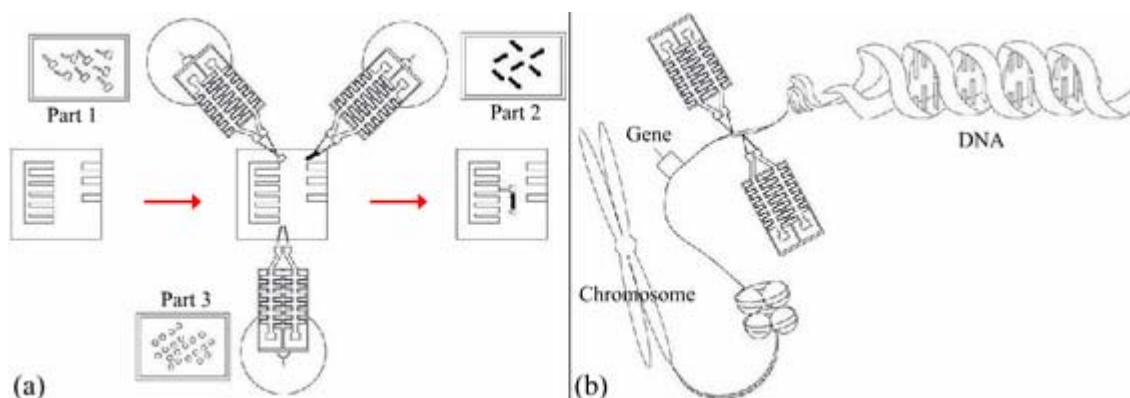


Figure 1.6 Schematic illustration of two potential applications of nanotweezers in applied sciences: (a) robotic nano-assembly and (b) gene recovery by means of functionalized end-effectors [7]

However, the most challenging problem hindering the advancement in the field of nanotweezers is that, nano-scale end-effectors in the form of either nanowires or nanotubes are grown selectively, i.e. with their orientation and chemical composition being suitable for device design, and attached to an actuation mechanism. As an example, it is a quite difficult fabrication process to grow two different nanotubes, i.e. Boron- and Phosphorus-doped, on the same chip respectively, and attaching these to metal electrodes after intersecting them with each other.

In today's technology, this problem can be solved by initially functionalizing the surface, on which nanowires or nanotubes are to be placed, using electron beam (e-beam) lithography or an AFM tip. However, these methods are inconvenient for parallel processing.

As an example, NH_2 templates are prepared on the surface and nanotubes are formed sticking on these templates due to electrostatic attraction [11] (Figure 1.7). If DNA-based photo-detectors mentioned in [9] are considered as a second example, Au electrodes, which are bridged by DNA molecules, are to be fabricated again by e-beam lithography.

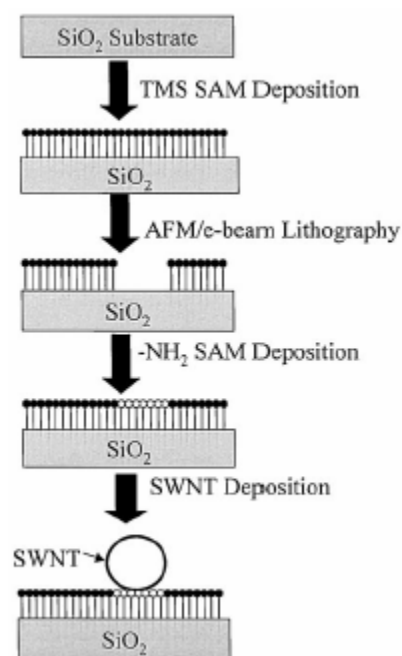


Figure 1.7 Schematic illustration of controlled deposition of SWNT on chemically functionalized lithographic patterns [11]

Similarly, Si nanowires used in building pH sensors are to be placed precisely between two metal electrodes [12].

In conclusion, there exist serious deficiencies in the field of constructing complex circuits or multiple-gate devices by combining nano-scale structures, i.e. *nano-assembly*, and nanotweezers offer promising tools in complementing these. Moreover, it will even be possible to constitute assembly lines, which are similar to the ones used in macro-scale fabrication, using a set of nanotweezers programmed individually with different tasks and operate in a synchronous manner. Of course, placement of these robot-like devices along the assembly line is again to be achieved using a self-assembly-based method, such as chemically functionalizing the platforms, on which they are to be established.

Such issues as, haptic applications, automation of devices and achieving device-to-device communication, give birth to thrilling fields, which require interdisciplinary research.

1.3. Position of Nanotweezers Among Alternative Manipulation Tools

1.3.1. Atomic Force Microscope (AFM)

Atomic force microscope (AFM) tips are the oldest and most common tools used for the purpose of nano-manipulation. In this method, nano-scale objects, which are randomly distributed in the environment, are arranged to have an order by being pushed individually using a tip with a sharpness of atomic order. Pushing of colloidal Au nanoparticles with dimensions in the order of 15 to 30 nm on a mica substrate in non-contact atomic force microscope mode [13] (Figure 1.8) can be given as an example.

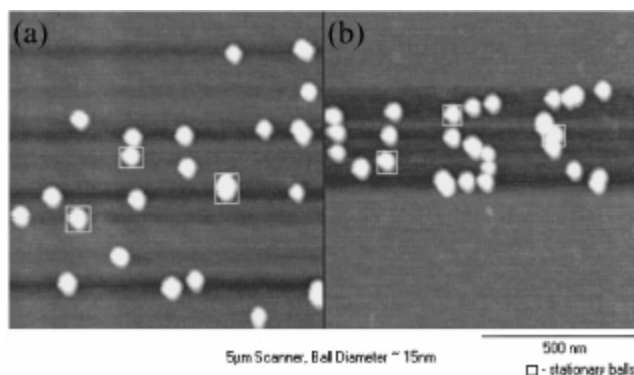


Figure 1.8 (a) Random pattern of 15 nm Au balls and (b) “USC” pattern obtained by a sequence of pushing commands [13]

Furthermore, works, in which nano-scale samples, such as DNA molecules and viruses [14] (Figure 1.9) or carbon nanotubes (CNTs) [15] (Figure 1.10), are manipulated by pushing in a similar manner, are often reported.

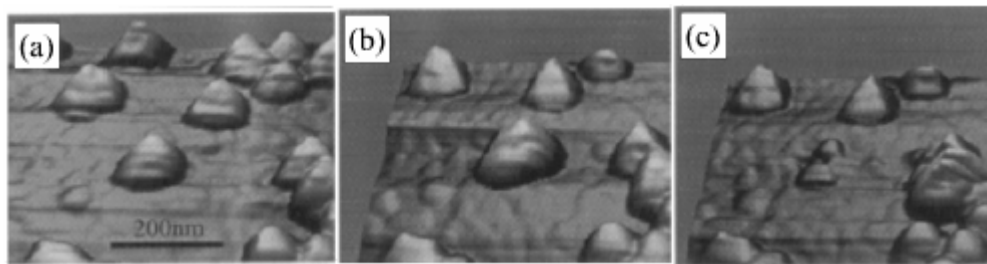


Figure 1.9 ((a), (b) and (c)) Images of manipulation of a virus on Si in nanopure water, where the virus in the center of the image in (a) is pushed to the right with two viruses above serving as fiducial marks [14]

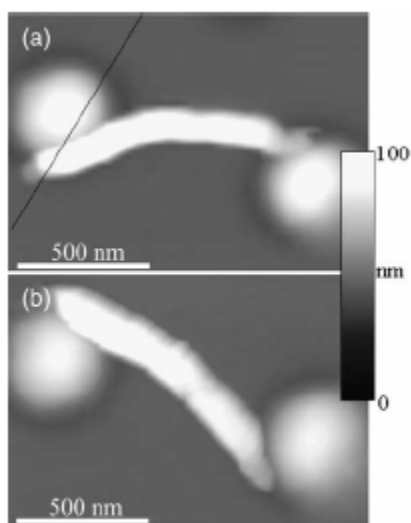


Figure 1.10 Contact mode AFM images of a CNT that switches from (a) one side of a Ge dot (b) to the other [15]

Since the method is based on mechanical pushing, it enables an assembly freedom, which is only limited to surface manipulation. For example, it is not possible to constitute a 3D structure by arranging the Au particles mentioned in [13] on top of each other. Furthermore, forming structures by pushing objects is a quite challenging process, even in 2D space. This can be considered to be a major disadvantage.

Moreover, due to the fact that usage of the same tip for both imaging (topography measurement) and mechanical pushing is not possible, either manipulation is to be carried out without seeing and switching from imaging mode to pushing mode each time reduces functionality or difficult means, such as real-time feedback, are utilized [16].

1.3.2. Optical Tweezers

Operation principle of optical tweezers relies on the interaction between a focused laser beam and small particles. Momentum change of the photons, which are either refracted or scattered from the particles, influences the particle in the opposite direction with the same amount as a result of the Law of Conservation of Momentum. Due to the fact that light intensity changes throughout the particle, reaction forces induced as a result of this momentum change are not cancelled, yielding to a net force on the particle towards the mid-plane, i.e. the brightest plane, of the beam and the particle is trapped. This method is generally utilized in grabbing and manipulation of dielectric spheres, viruses, bacteria and DNA molecules attached to spheres.

One major disadvantage of this method is that, it is hindered to only biological applications since particles are to be dispersed in a solution for the purpose of increasing their mobility. However, gripping and manipulation abilities are limited even in this field. As an example, it is not applicable to coil-shaped DNA molecules due to the fact that, induced optical force is too small to overcome thermal Brownian motion. In such cases,

DNA molecules are manipulated either indirectly being attached to latex beads by chemical alteration, which are manipulated using a laser beam, or being mechanically trapped among more than one bead [17] (Figure 1.11).

Two other disadvantages of optical tweezers are that (1) they are either not suitable for batch fabrication or they require expensive fabrication processes and (2) they can hardly be miniaturized.

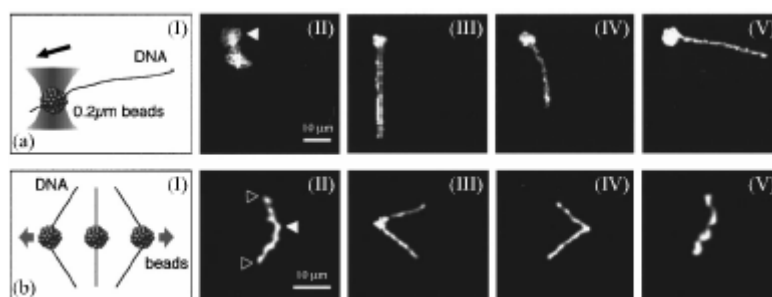


Figure 1.11 (I) Schematic illustrations and (II, III, IV and V) sequential images showing manipulation of a single DNA molecule, i.e. tandem lambda DNA, using laser clustering of 0.2 μm latex beads by laser trapping (a) from one end and (b) from center where both ends anchored to a coverglass [17]

Furthermore, if electrical or mechanical properties are to be measured using optical grabbing method, the necessity of using an additional probe arises. However, in similar cases, where AFM tips or mechanical tweezers are utilized, end-effectors, which provide gripping action and manipulation, also serve as measurement probes.

1.3.3. Current Nanotweezers and Their Demands

The reporting of tweezers-like devices, which are capable of manipulating nano-scale objects and performing measurements on them, started in 1999 [18]. However, due to the approach arising from conventional MEMS fabrication techniques, top-down methods are followed in the fabrication of most of these tweezers, resulting in fabrication yields and operation performances less than those expected.

Reasons for the insufficiencies in the field of nanotweezers can be explained as follows: With current MEMS technology, fabrication of mechanical and electrical structures used in the actuation of nano-scale end-effectors, such as an electrostatic actuation mechanism, is possible in a common manner. Most important parts of a pair of nanotweezers are the nano-scale end-effectors, which perform the gripping action. However; challenges in both the technique used in their fabrication and the approach followed in their integration with MEMS can be considered as major factors hindering the performance of nanotweezers.

In current technology, the actuation mechanism is fabricated initially, and afterwards, nano-scale end-effectors are grown on this mechanism one-by-one. Length, relative position and orientation of the nano-tips are all determined according to top-down fabrication approach, by the operator of the growth process, which is well applicable at both macro- and micro-scales. However, in order for a technique to be successful at nano-scale it should, at least partly, be based on a bottom-up approach, where formation happens naturally by *self-assembly*. Otherwise, the necessity of growing thousands and even millions of nano-scale end-effectors on a single chip using time consuming and expensive methods, which are to be performed in a vacuum environment, will hinder the advancements in the field of nanotechnology.

When current nanotweezers fabrication techniques are considered, mostly top-down approaches are encountered. One method, which is commonly used, is growing the nano-

scale end-effectors at tips of a previously fabricated MEMS device as mentioned above. This growth process can be performed by focusing either an ion [19] (Figure 1.12) or an electron [20] (Figure 1.13) beam on a surface. On this surface, where the beam is focused, carbon-based reactants decompose and participate, generally in the form of solid carbon, at the location.

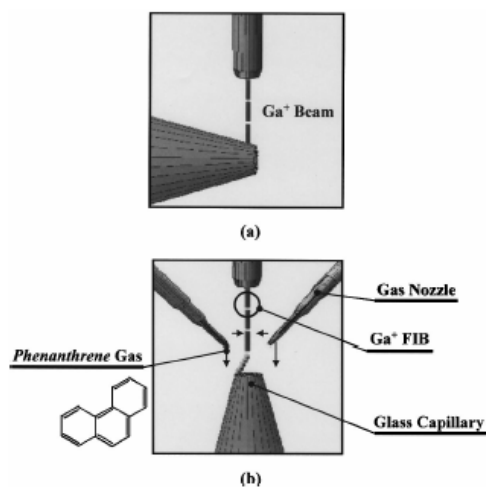


Figure 1.12 (a) Schematic illustration of tip surface smoothing of glass capillary by focused ion beam (FIB) etching and (b) nanomanipulator fabrication by FIB-CVD [19]

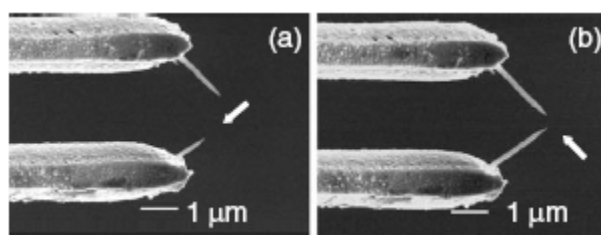


Figure 1.13 Nanofabrication process: (a) an electron beam is focused on the end of the micro cantilever and a narrow tip grows in the direction of the beam and (b) the growth proceeds in smaller and smaller steps [20]

As an alternative, metal deposition can be performed by making use of a metalorganic gas present in the environment [21] (Figure 1.14) and a nanowire is formed along the path of the beam, which is slowly moved. The major disadvantage of this method is that, it does not provide a parallel processing possibility and each nanowire is to be fabricated individually, requiring an accurate alignment between the material and the beam.

Electron and ion beam techniques mentioned above are not generally preferred in fabrication of nanotweezers, since they are time consuming and continuity of manpower and equipment is necessary.

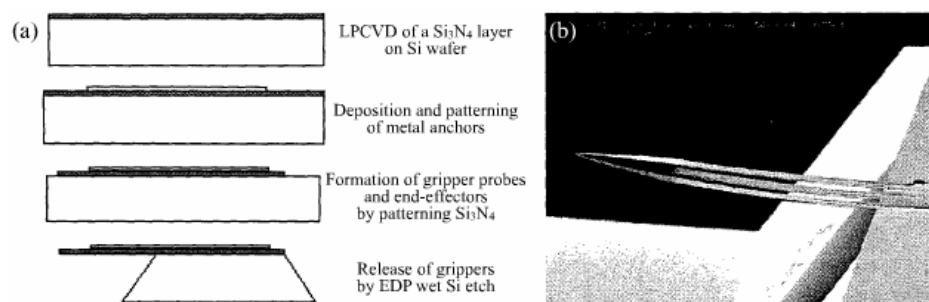


Figure 1.14 (a) Schematic illustration of the fabrication process and (b) an SEM micrograph of a nanogripper having 300 μm -long probe beams with nano-scale end-effectors [21]

Another possibility is attaching previously prepared nanowires to tip locations of tweezers instead of growing them afterwards. This method requires getting precisely closer to both tip locations of the tweezers and corresponding nano-scale end-effectors and achieving contact between each tip and a single nanowire only. Integration of the nanowires and the actuator device is obtained either by means of a direct current or by making use of an amorphous carbon thin film, which is obtained via decomposition of hydrocarbon gasses present in the environment with the help of an electron beam [22] (Figure 1.15).

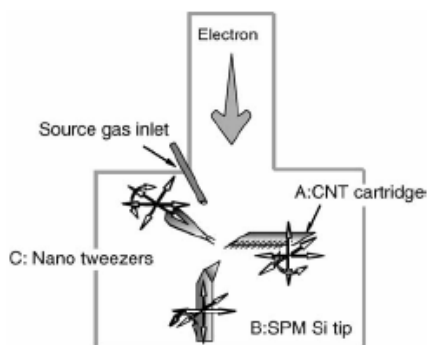


Figure 1.15 Schematic illustration of a SEM equipped with three stages and a gas source inlet for e-beam-induced deposition of thin films [22]

There are also examples where bonding process is performed under an optical microscope by using adhesive carbon tapes [18] (Figure 1.16). Although researches claim that the yield is greater than 50% and the time required to making a working device by attaching nanotubes to electrodes is less than 2 hours, no observations were reported. Furthermore, it is impossible to avoid variations between samples since the method is hand-made.

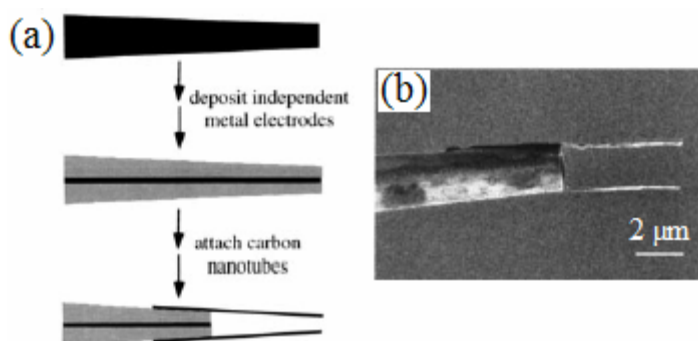


Figure 1.16 (a) Schematic illustration of fabrication of carbon nanotube (CNT) nanotweezers and (b) an SEM image of nanotweezers after two multi-walled nanotube bundles are attached on each electrode [18]

Another completely top-down method, which can be considered as unsuccessful in adapting conventional MEMS fabrication approach to nano-scale world, is degradation or sharpening by etching. In such an example, a smaller part is obtained from a larger one via focused ion beam (FIB) etching [19], disadvantages of which were mentioned above.

Another alternative is obtaining AFM tip-like structures by anisotropic etching of single crystal Si in an acid solution [23]. Since this method relies on wet etching, results are highly time-dependent and the repeatability is low. Furthermore, sharpness of the end-effectors prevents the usage of the device for gripping. In order to overcome this problem, it is possible to chemically activate these sharp end-effectors and objects. However, as in the case where DNA molecules are held this way, the number of sticking molecules is undetermined.

In addition to absence of a method, which is well-suitable for the fabrication of nano-scale end-effectors, there are also deficiencies related to the actuation mechanism. Although there are MEMS, which enable actuation of each tip independently with a nanometric precision, nano-scale end-effectors independently are to be grown on a stationary component and actuation is achieved via attraction or repulsion between the end-effectors due to the application of a direct current [18, 22].

1.4. Alternative Actuation Mechanisms

Both actuation principal and operational requirements of nanotweezers are similar to that of their micro-scale equivalents, i.e. microgrippers. However, precision and reliability of actuation and size of the actuation mechanism gain more importance at nano-scale. Furthermore, material of the actuation mechanism should be compatible with the method chosen for the fabrication of the nano-scale end-effectors, i.e. guided-self-assembly, in order to achieve successful integration of these two.

In the following subsections, electrostatic and thermal actuation methods will be discussed mainly, where other actuation alternatives will be mentioned just briefly, by giving examples from the literature.

Electrostatic Actuation:

Electrostatic actuation is based on attractive forces induced, as a result of an applied potential difference between two parallel plates, i.e. electrodes, which are separated by a dielectric medium. Electrostatic actuators are generally preferred due to their compatibility with conventional MEMS processes, low power requirement and short response time. One disadvantage of electrostatic actuators is the requirement of high operation voltages, which might be up to a few hundred volts.

What makes electrostatic actuators more popular for micro- and nanomanipulation applications is speed and high precision of actuation. Furthermore, the possibility of grounding the actuator arms by applying operation voltage to static electrodes prevents passing of a current through the grabbed object. There are various electrostatically actuated microgrippers reported in the literature with different designs such as parallel actuator electrodes [24, 25] (Figure 1.17(a)) or comb-drive structures [26-29] (Figure 1.17(b)). Electrostatically actuated microgrippers are also commercially available by Nascatec (Figure 1.18).

Furthermore there are electrostatically actuated nanotweezers, which are mentioned in previous sections, where gripping is achieved by the motion of nano-scale end-effectors, rather than a micro-scale actuation mechanism [2, 19, 23].

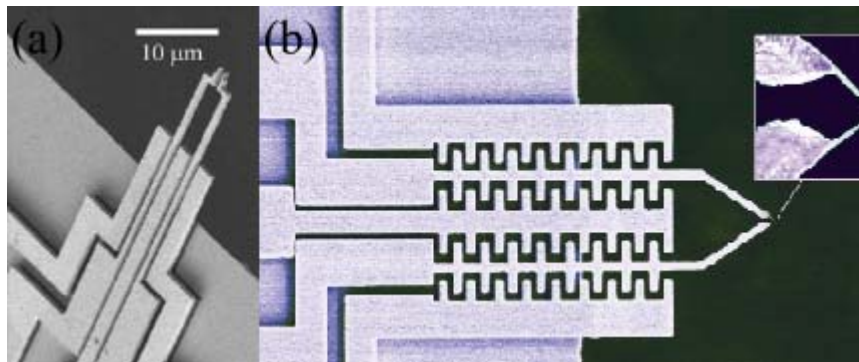


Figure 1.17 SEM images of two different electrostatically driven microtweezers with (a) straight actuator electrodes [25] and (b) a comb-drive actuation mechanism [29]

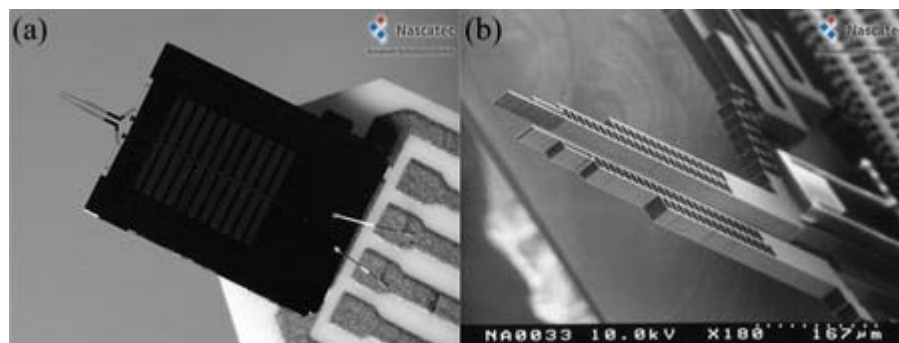


Figure 1.18 (a) A pair of electrostatically actuated microgrippers, which are commercially available by Nascatec with (b) a more detailed view of the actuator tips [30]

Thermal Actuation:

Thermal actuation is based on thermal expansion of solids due to resistive heating as a result of a current passed through. Advantages of electro-thermal actuators can be listed as low operation voltage, availability of large forces, and hence displacements. However, thermal actuation is relatively slow, i.e. response time is long.

Linear thermal actuators, which are composed of either a cascaded [32] or a parallel arrangement of cantilever beams [32, 33] (Figure 1.19), are commonly preferred in

micromanipulation applications. There are also thermally actuated microgrippers commercially available by Zyvex (Figure 1. 20).

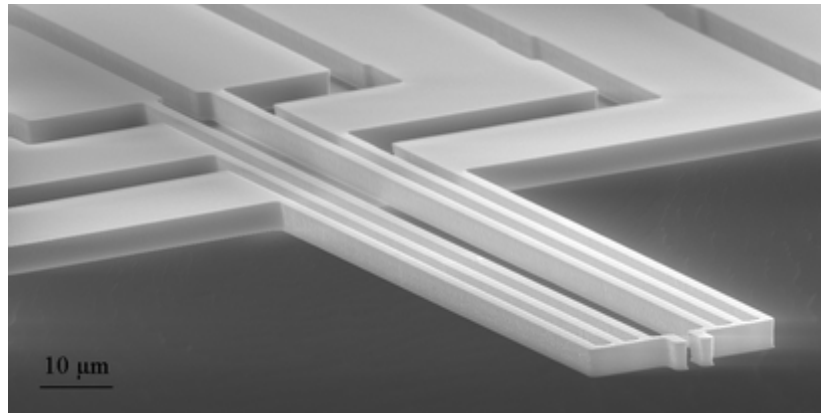


Figure 1.19 SEM image of a pair of electro-thermally driven microgrippers consisting of three parallel beams connected by an end bar [34]

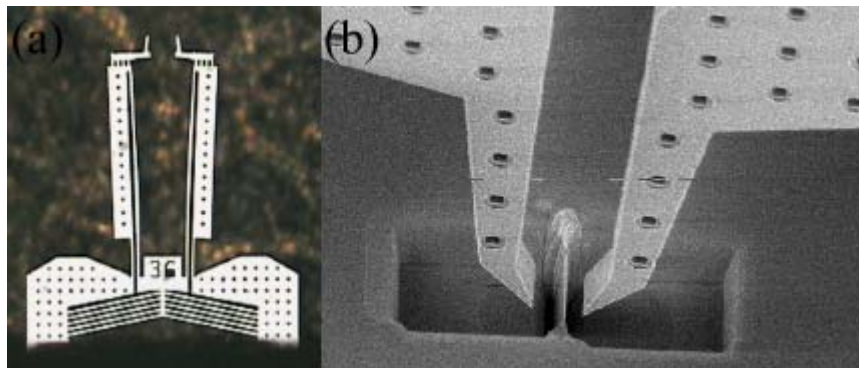


Figure 1.20 A pair of thermally actuated microgrippers, which are commercially available by Zyvex with (b) a more detailed view of the actuator tips [35]

High temperatures reached at device tips during operation can be considered as the major disadvantage of electro-thermal actuators, which might lead to damage on the object to be manipulated or influence material properties of the sample during testing applications.

Despite of the disadvantage mentioned above, parallel-beam thermal actuators are still favorable since their design is well-suitable for providing force feedback, which is an important requirement for advancements in the fields of micro- and nanomanipulation [33].

Another thermal actuation possibility is adopting bimetallic thermal actuators, which rely on the mismatch between coefficients of thermal expansion (CTE) of two different metals, to be used in microgrippers. However, bimetallic thermal actuators are more preferable in applications where lateral displacement is necessary [36, 37]. Furthermore, introduction of a second structural material adds to the complexity of the process, for this reason this actuation method is not well-suitable for the purpose of micro-nano integration.

Other Actuation Possibilities:

Examples of different actuation principles used in microgrippers are listed below:

- Shape memory alloys (SMA) were also used in fabricating microgrippers [38], where actuation is based on formation of an antagonistic pair due to the movement of two integrated actuation units of a stress-optimized shape in opposite directions as a result of a selective heat treatment. However, they are not suitable for nano-scale manipulation due to their relatively high response time.
- Microgrippers with a piezoelectric actuation mechanism was reported in [39, 40], where grippers are attached to an actuation bar and actuation is achieved by connecting this bar to a macro-scale piezoelectric strip actuator. Piezoelectric actuation is not favorable for nano-scale manipulation due to the fact that it is expensive to miniaturize piezoelectric crystals, such as aluminum nitride or zinc oxide.
- There are many ways of implementing electromagnetic actuators to microgripper applications. However, they are more suitable for large scale manipulation purposes. As an example, NiTi superelastic alloy can be used for the construction of a microactuator [41].

- Electro-active polymers can be useful in sensing and manipulation in aqueous solutions, as in the case, where a Nafion-based ionic conducting polymer films (ICPF) was used for developing two-finger actuators [42].

More information on tools for in-situ manipulation and characterization of nanostructures can be found in [43], together with an extensive comparison of grippers for micro- and nanomanipulation.

1.5. A New Approach: Fabrication of Nanotweezers by Guided Self-assembly

1.5.1. Motivation

Problems encountered in fabrication of nanotweezers using currently available methods, which are mainly related to either growth of nano-scale end effectors or design of the actuation mechanism, were explained in detail in the previous section.

In order to summarize, on one hand there are top-down fabrication techniques, through which it is possible to obtain highly-oriented nanowires. However, it is not possible to achieve successful integration of nano-scale end-effectors with an actuation mechanism in the fabrication of nanotweezers, due to the fact that all these methods are quite expensive and time consuming, where none of them are compatible with batch processing. On the other hand, bottom-up fabrication techniques are more cost effective, but it is not possible to control the orientation of resulting nanowires precisely. Furthermore, separation of nano-scale structures among many others after the synthesis is extremely difficult, as well as their assembly.

In this thesis, a new approach, which constitutes a bridge between top-down and bottom-up fabrication methods, is presented: *Nanotweezers Fabrication by Guided Self-assembly*. The method simply relies on fabrication of nano-scale end-effectors in the form of nanowires using a self-assembly-based bottom- technique and integration of these with an actuation mechanism, which has a nano-metric precision, in a batch-compatible manner.

In following subsections, basics of nanowire fabrication by guided self-assembly will be introduced and fabrication procedures of both nanowire end-effectors and actuator devices will be described, briefly.

1.5.2. Fabrication of Nanowires

In a circumstance, where all necessary conditions are satisfied, structures with desired size and shape form naturally by themselves, eliminating the need for fabricating each part individually. An example for this is the electrodeposition of highly ordered hexagonal arrays of metallic nanowires using an anodized aluminum oxide (AAO) film with hexagonal-close-packed nano-channels as a deposition template [44] (Figure 1.21(a) and (b)). These nano-channels grow along the thickness of the AAO film in a parallel manner, resembling a well-arranged set of nano-scale wells if looked from top. It should be noted that, it is extremely difficult to obtain such structures with a wide-range diameter distribution at nano-scale, using a top-down approach.

However, this method is not suitable for nanotweezers fabrication since nanowires entangle with each other and form bundles after the removal of the AAO template (Figure 1.21(c) and (d)) hence, it becomes impossible to pull a single nanowire out. This is a common problem encountered in almost all bottom-up nanowire fabrication approaches, including vapor-liquid-solid (VLS) method [45] (Figure 1.22).

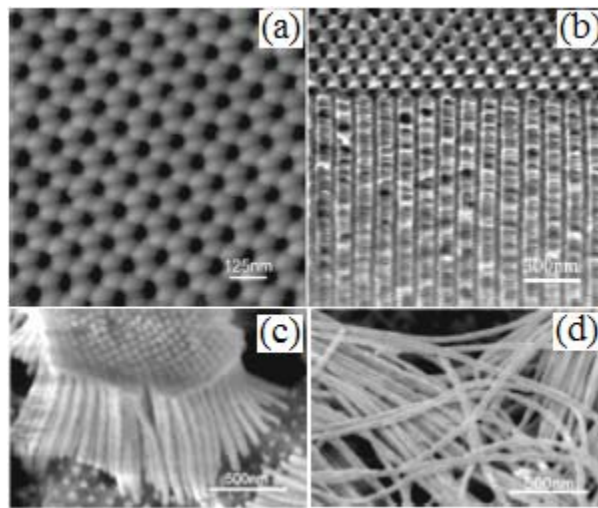


Figure 1.21 (a) An AFM tapping mode image (b) a cross-sectional SEM image of the AAO film after anodization with SEM images of nanowire bundles after (c) 2 μm - and (d) 25 μm -long AAO templates are partially dissolved [44]

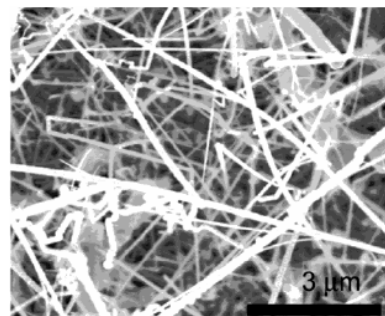


Figure 1.22 A HRSEM image of Ge nanowires grown VLS method [45]

Basic idea behind the method offered in this work for the solution of the above mentioned problem is forming thermally induced cracks at predetermined locations in a sacrificial thin film layer, where end-effectors are to be placed, and using these cracks as molds for nanowire fabrication. When the method was first reported in [46] (Figure 1.23), it was based on creating cracks in a sacrificial SiO_2 layer on a Si wafer and filling them

with electroless nickel. Nanowires fabricated in this work were 50 nm or less in width, with lengths of several μm 's.

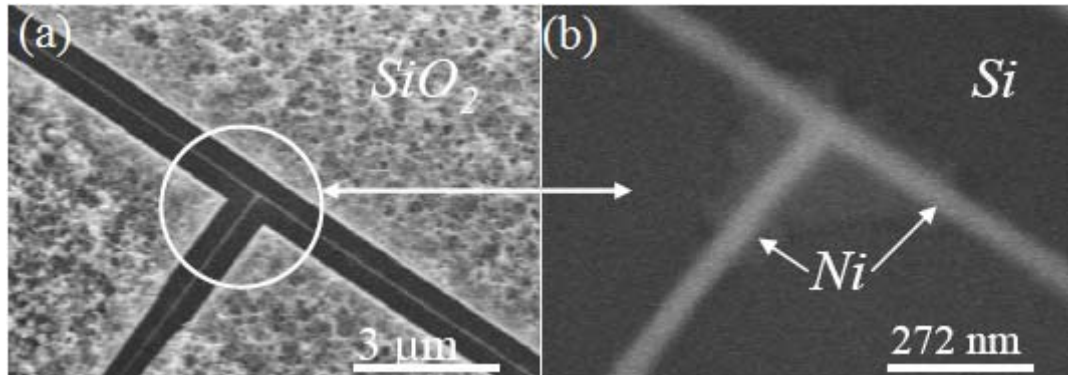


Figure 1.23 (a) SEM image of a Ni wire after widening of the crack mold with (b) a more detailed view of the location where two nanowires intersect [49]

Major developments presented in [47] and [48] (Figure 1.24) enabled control over number, direction and orientation of the resulting nanowires, by etching crack initiation and termination sites, in the form of triangles, squares and circles in the Si substrate through inductively coupled plasma-deep reactive ion etching (ICP-DRIE) prior to oxide deposition. Hence, either crack propagation continues along a straight path until they arrest at another etched feature or crack diverts and approaches to a nearby channel perpendicularly.

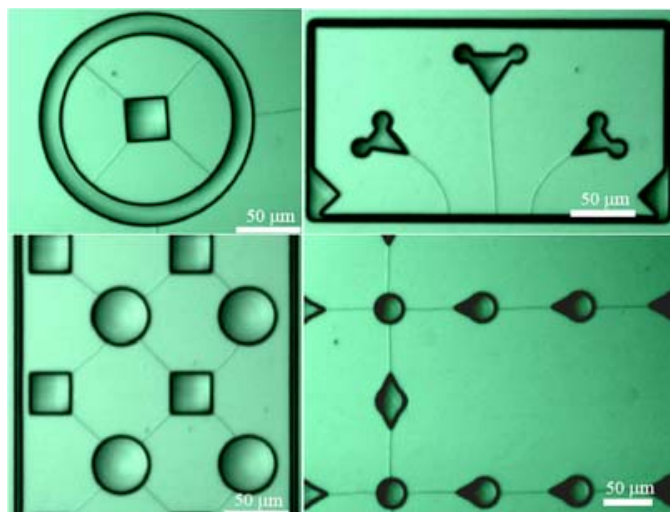


Figure 1.24 Examples of self-assembled crack patterns [49]

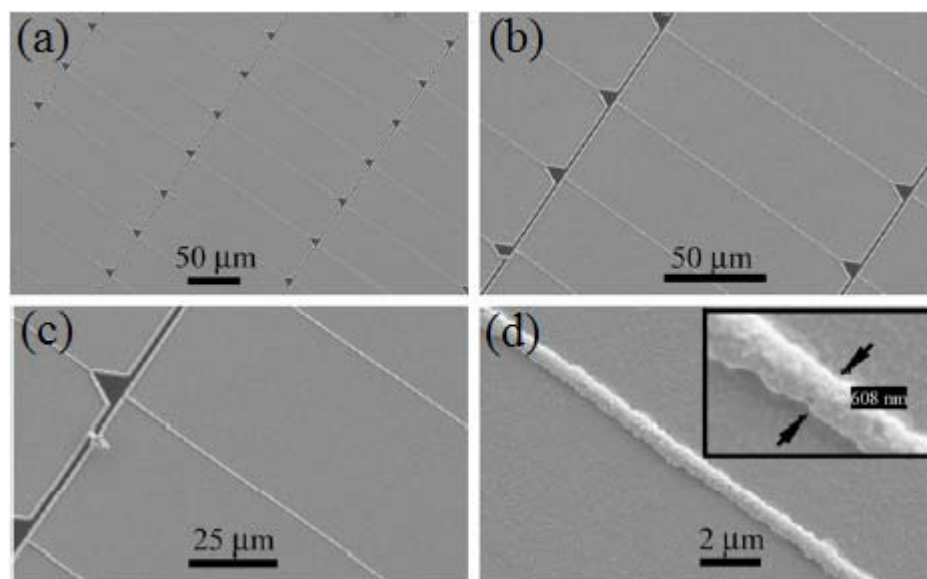


Figure 1.25 ((a), (b) and (c)) Gradually zoomed-in SEM images of a NiFe nanowire network, where ICP-DRI etched crack initiation and termination trenches are visible and (d) a single nanowire with close-up view in the inset [50]

As a recent improvement, the method is extended to employ electroplating in the deposition of the nanowires, enabling the fabrication of nanowires of various alloys, such as NiFe [50] (Figure 1.25). This novel feature provides the opportunity of controlling material properties of the resulting nanowires

Procedure for nanowire fabrication by guided self-assembly is as follows (Figure 1.26):

- Deposition of a PECVD SiO₂ thin film as a sacrificial layer,
- Formation of cracks by proper heat treatment,
- Widening of cracks by wet etching, in order to obtain a sufficiently large and oxide-free plating area,
- Deposition of nanowires into nano-molds by electroplating,
- Removal of the sacrificial layer by wet etching,
- Release of nanowires by wet etching.

1.5.3. Fabrication of an Actuation Mechanism

Fabrication of the actuator devices will be performed by electroplating. Procedure can simply be described as follows: After deposition of nanowires into nano-molds by electroplating, sacrificial layer is not removed and it is covered with a relatively thin metal seed layer. The purpose is to obtain a conductive plating base for device deposition, over the sacrificial layer, which is non-conducting. Then, the wafer surface is patterned with a photoresist mold using simple optical lithography and actuator devices are deposited into this mold by electroplating, similar to the case in nanowire fabrication.

Removal of the sacrificial layer and release of nanowire end-effectors can be performed after removing the photoresist mold and the metal plating base, respectively.

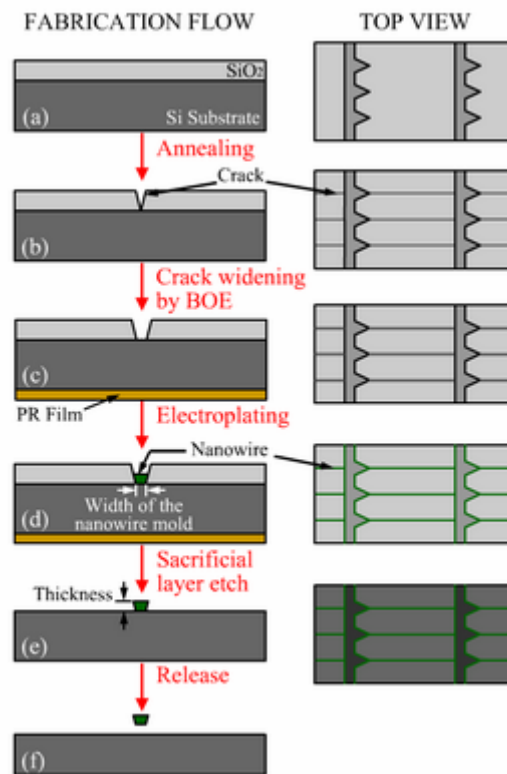


Figure 1.26 Fabrication process of nanowires

1.6. Outline

In Chapter 2, design procedures of two different actuator mechanisms for nanotweezers, an electrostatic comb-drive structure and a thermally actuated cantilever beam structure, will be explained in detail, together with end-effector design and different methods used in FEA of each actuation mechanism will be described and analysis results will be presented.

In Chapter 3, basic process flow will be introduced initially, followed by the design procedure of all masks used in fabrication, mentioning also the issues related to arrangement of individual chips within the wafer and alignment marks.

In Chapter 4, basics of Electroplating, which is the main process of the self-assembly-based fabrication technique, will be introduced initially and fabrication sequence for the electrostatically actuated nanotweezers will be explained in detail, using schematic illustrations, in terms of six main steps as: *Etching of the Crack Initiation Patterns, Fabrication of Nanowires, Preparation of a Layer for Integration, Fabrication of Devices, Cutting of Nanowire Ends and Release.*

In Chapter 5, experimental procedure followed in determination of a PECVD process recipe for the sacrificial SiO₂ layer, which is used as a mold in self assembly-based fabrication of the nanowires, will be explained in detail initially, and results of two fabrication batches performed will be given for all of the six main steps, followed by proper optimization of process parameters where necessary.

In Chapter 6, experimental setup used in actuation and static characterization of the fabricated devices will be explained and results will be presented, together with a comparison with the theory.

In Chapter 7, two alternative fabrication methods for increasing the yield of integration will be proposed, together with a design alternative, including a bilayer thermal actuator as a third-gripping arm, which enables a better gripping capability.

In Chapter 8, design, fabrication and characterization results will be discussed and conclusions will be drawn.

Chapter 2

DEVICE DESIGN AND ANALYSIS

2.1. Introduction

MEMS design is an advanced procedure, including not only the design of the physical system but also such concepts as finite element analysis, layout design and design of the fabrication process. Design of the physical system, namely the MEMS device, constitutes the very basis of the design process and of prime importance for achieving useful device operation with the desired functionality.

Recent advancements in finite element analysis (FEA) tools enable simulation of the behavior of a physical system during operation at the design step, making design optimization and improvement possible and eliminating repeated fabrication trials.

In this chapter, design procedures for devices with two different actuation mechanisms, an electrostatic comb-drive structure and a thermally actuated cantilever beam structure, will be explained in detail. Afterwards, issues related to design of the end-effectors, such as shape of the nanowires and their position and orientation with respect to actuator tips, will be introduced. Finally, different methods used in FEA of each actuation mechanism will be described and results will be presented.

2.2. Actuator Design

2.2.1. Design of an Electrostatic Actuation Mechanism

Electrostatically-driven comb drives with double-folded cantilever beam flexures are chosen as the actuation mechanism for the nanotweezers. Comb-drive actuation is based on the electrostatic force generated due to the application of a potential difference between two comb structures, one movable and the other fixed. Advantages of electrostatic actuation can be listed as low power requirement, precision of actuation, independency of actuation force from displacement and fabrication simplicity.

Apart from the nano-scale end-effectors located at device tips, actuation mechanism for the nanotweezers can be considered to be similar to that of a microgripper. The simplest design possibility for any electrostatically actuated microgripper is composed of three combs (Figure 2.1(a)) [51]. The comb in the middle is fixed since it is completely anchored to the substrate, where two combs on each side of it are movable, being anchored to the substrate via double-folded cantilever flexures. Gripping action, i.e. closing the gripping ends, is achieved by applying a voltage to the comb in the middle. However, due to the fact that electrostatic forces are always attractive, motion in the opposite direction is not possible with a three-comb structure. Opening the gripping ends, becomes possible with the addition of two fixed combs on exterior side of both movable combs (Figure 2.1(b)).

Note that, device parts to be released, such as movable combs or ends of cantilever flexures should be designed in the form of trusses rather than solid structures in order to ensure complete release. Hence, weight of the devices decreases and bending down of long structures under the influence of gravitational forces is prevented. Furthermore, mechanical acceleration sensitivity of the actuators is also reduced.

Design of Comb-Drives:

First step in the design of an electrostatic actuation mechanism is the calculation of an electrostatic spring constant, in order to determine the range for the mechanical spring constant, which yields to the required displacement and optimizing design parameters such as longitudinal and transverse gap distances between comb fingers or width and height of each comb finger.

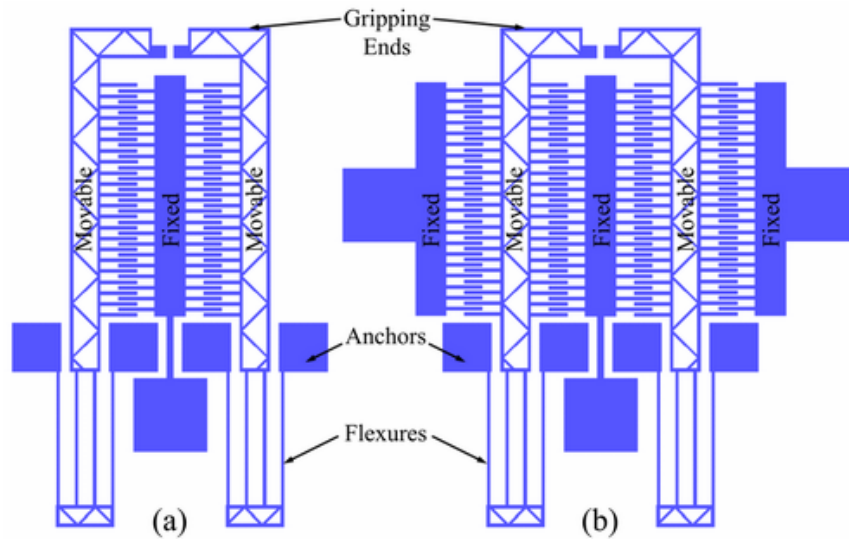


Figure 2.1 Schematic illustration of two basic electrostatic actuation mechanisms for nanotweezers with (a) three combs and (b) five combs anchored from one end

The total capacitance between a pair of interdigitated comb fingers (Figure 2.2) can be written as the sum of the capacitances due to interaction of the lateral and longitudinal comb faces as [52]:

$$C = C_x + C_y = 2\epsilon h \left(\frac{w}{g_x - x} + \frac{t + x}{g_y} \right) \quad (2.1)$$

In the above expression, h is height of the actuator device, w is width of each comb finger, t is the zero voltage overlap length between the fingers, g_x and g_y are gap distances in x- and y-directions respectively, and x is the displacement in x-direction. Permittivity, ϵ , can simply be taken as the permittivity of the free space, $\epsilon_0 = 8.854 \times 10^{-12}$ F/m, since relative permittivity of air is equal to 1.

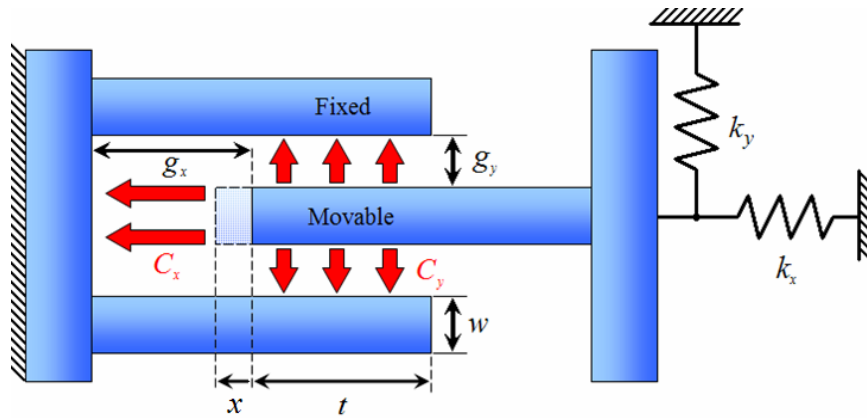


Figure 2.2 Schematic illustration of close-up view of a single pair of interdigitated comb fingers

Then, total capacitance between a comb actuator pair can be calculated simply by multiplying Equation 2.1 by the number of comb fingers on each comb, N_f , as:

$$C_{total} = C_x + C_y = 2N_f \epsilon_0 h \left(\frac{w}{g_x - x} + \frac{t + x}{g_y} \right) \quad (2.2)$$

Capacitive energy stored due to the application of a potential difference of, V , between two combs can be determined from:

$$W_{es} = \frac{C_{total}V^2}{2} \quad (2.3)$$

Expression for the resulting electrostatic force can be obtained by the derivation and simplification of the energy expression given above, as follows:

$$F_{es} = -\frac{dW}{dx} = -\frac{d}{dx} \left[N_f \epsilon_0 h \left(\frac{w}{g_x - x} + \frac{t+x}{g_y} \right) V^2 \right] \quad (2.4.a)$$

$$F_{es} = -N_f \epsilon_0 h \left(\frac{w}{(g_x - x)^2} + \frac{1}{g_y} \right) V^2 \quad (2.4.b)$$

Then, electrostatic spring constant yielding to a displacement, x , can be determined according to Hooke's Law as:

$$k_{es,x} = \frac{F_{es}}{x} \quad (2.5)$$

Design of Flexures:

Second step in the design of an electrostatic actuation mechanism is the determination of the design parameters for the double-folded cantilever flexures, such as beam lengths and widths, which yields to a mechanical spring constant, $k_{mech,x}$, that matches the electrostatic spring constant, $k_{es,x}$, calculated for the desired displacement range.

A double-folded cantilever beam is a linear combination of two folded cantilever beam structures, which are composed of two cantilever beams with different lengths. Spring structure can be fixed either from inside (Figure 2.3(a)) or outside (Figure 2.3(b)) with the shorter beams connected to the anchors.

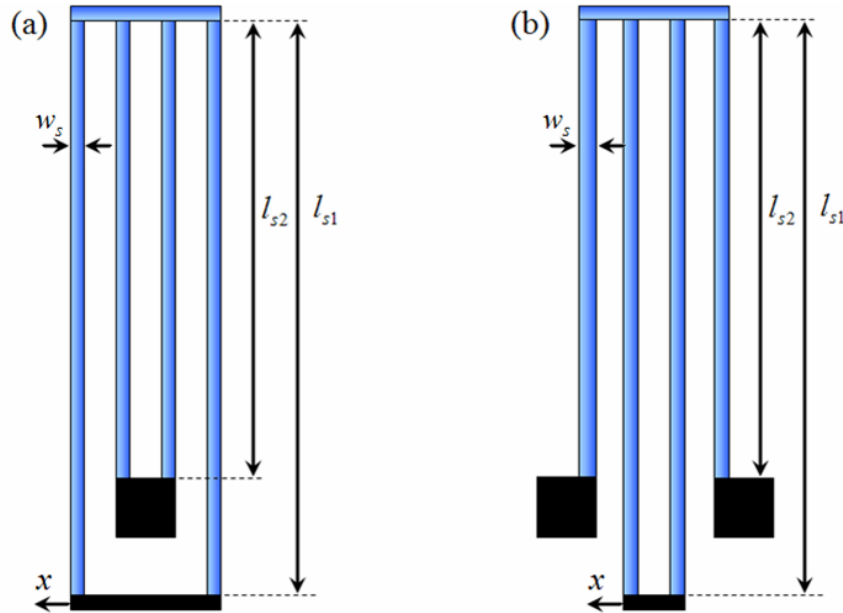


Figure 2.3 Schematic illustration of two different double-folded spring arrangements:
Anchored from (a) inside and (b) outside

For a double-folded cantilever beam, the spring constant in x-direction is given by [53]:

$$k_x = \frac{4E_s h_s w_s^3}{l_{s1}^3 + l_{s2}^3} \quad (2.6)$$

In the above expression, E_s is the modulus of elasticity ($E_{Ni} = 204 \text{ GPa}$), h_s is the height of the spring (same as actuator device height, h , mentioned above) and w_s is the

cantilever width of the spring, where l_{s1} and l_{s2} are the lengths of long and short cantilever beams of the structure, respectively.

Designing the springs with cantilever lengths being equal, i.e. $l_{s1} = l_{s2} = l_s$, spring constant in x-direction can be calculated as:

$$k_x = 2 \frac{E_s h_s w_s^3}{l_s^3} \quad (2.6)$$

Spring constant in z-direction is similarly:

$$k_z = \frac{2E_s h_s^3 w_s}{l_s^3} \quad (2.7)$$

Mechanical spring constant for devices anchored from only one end, as illustrated in Figure 2.1, is simply equal to k_x and:

$$k_{mech,x} = k_x \quad (2.8)$$

Another possibility is anchoring the devices from both ends (Figures 2.4(a) and (b)), which yields to more stable devices and better levitation control. The overall spring constant for such devices anchored from both ends is then:

$$k_{mech,x} = 2k_x \quad (2.9)$$

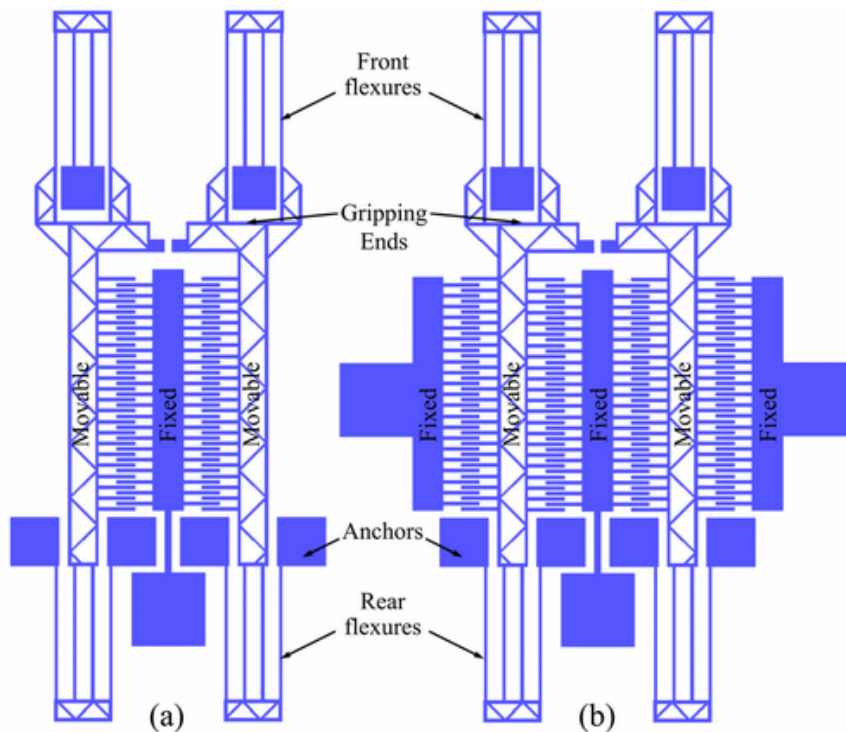


Figure 2.4 Schematic illustration of two basic electrostatic actuation mechanisms for nanotweezers with (a) three combs and (b) five combs anchored from both ends

Stability Analysis:

One stability issue related to flexure design is *lateral instability*. In addition to longitudinal forces between the comb fingers, there exist also lateral forces, which normally balance out. However, at high operating voltages, these lateral forces become considerably large and might lead to sudden collapsing of combs even due to a small disturbance. In order to increase lateral stability, C_y / C_x ratio is to be high (i.e. at least ≥ 40) and zero voltage overlap, t , is to be as small as possible.

Another stability issue related to flexure design is *in-plane instability*. Any displacement of movable combs along z-direction leads to electrostatic forces arising in this direction due to the change in the in-plane area. In order to eliminate this, stiffness of

the flexures in z-direction should be much higher than that in x-direction, i.e. $k_{mech,z} / k_{mech,x}$ ratio is to be high.

Pull-in Analysis:

The most important issue with electrostatic design is the phenomena of *pull-in*. Electrostatic force increases proportional to the inverse square of the increasing gap distance, where mechanical restoring force increases linearly. Hence, electrostatic force becomes dominant after beyond a certain voltage limit, yielding in the collapse.

At the point of pull-in, net force is equal to zero [52]:

$$F_{net} = F_{es} + F_{mech} = 0 \Rightarrow -N_f \epsilon_0 h \left(\frac{w}{(g_x - x)^2} + \frac{1}{g_y} \right) V^2 + k_{mech,x} x = 0 \quad (2.10)$$

It is known that gradient of the above force expression is also equal to zero:

$$\frac{dF_{net}}{dx} = 0 \Rightarrow -2N_f \epsilon_0 h \left(\frac{w}{(g_x - x)^3} \right) V^2 + k_{mech,x} = 0 \quad (2.11)$$

Then, voltage and displacement values, at which pull-in occurs, can be determined simply by solving two expressions given above simultaneously.

Parameter Selection:

Due to the fact that, gripping range for a pair of nanotweezers is on the order of a few micrometers and considering operational requirements together with possible restrictions

due to fabrication processes, following design parameters were chosen for both comb-drives and double-folded cantilever flexures:

Number of Comb Fingers	N_f	30, 40 or 50
Device Height	h	7 μm
Finger Width	w	5 μm
Zero Voltage Overlap	t	30 μm
Longitudinal Gap Distance	g_x	30 μm
Lateral Gap Distance	g_y	4 μm

Table 2.1 Comb-drive design parameters

Spring Height	h_s	7 μm
Spring Width	w_s	3 or 4 μm
Cantilever Beam Length	l_s	300, 400, 500 or 600 μm

Table 2.2 Flexure design parameters

Analytically calculated electrostatic stiffness values corresponding to a displacement of 2 μm , which can be considered as an average gripping requirement, are 1.525 N/m, 2.034 N/m and 2.542 N/m for devices 30, 40 and 50 comb fingers, respectively. Note that, electrostatic force induced by each comb finger pair at a displacement of 2 μm is 0.1017 μN .

Stiffness of devices vary in the range 0.306 N/m for a single pair of 3 μm x 600 μm double-folded cantilever beams to 13.54 N/m for two pairs of 4 μm x 300 μm double double-folded cantilever beams. Corresponding k_z/k_x ratios are 4 and 3.063, respectively. Note that, as long as pull-in and other stability issues are satisfied, devices with stiffness

values greater than maximum electrostatic stiffness, i.e. 0.877 N/m can be actuated at higher operation voltages, where those with stiffness values smaller than minimum electrostatic stiffness, i.e. 0.526 N/m can be actuated at lower operation voltages than 80V, which is the design voltage.

Due to various issues related to fabrication processes, such as lithographic resolution, devices with 5 μm -wide flexures were also included in the fabrication mask, to be on the safe side. Furthermore, during fabrication, electroplating time corresponding to a deposition thickness of 6 μm was used instead of 7 μm , which is the design thickness, in order to minimize over- or under-deposition effects as a result of the non-uniform current density over the wafer.

2.2.2. Design of a Thermal Actuation Mechanism

In addition to electrostatically actuated nanotweezers, thermally actuated nanotweezers, with either two- or three-beam structures, were also designed as alternatives. Design procedure for the three-beam thermal actuation mechanism is presented in [33] and a similar approach can be followed in the design of a two-beam thermal actuation mechanism.

Theory of Operation:

Thermal actuation is based on resistive heating of parallel cantilever beam structures, which are composed of either two beams of different widths or three beams of equal width, passing a current through them (Figure 2.5). Motion is achieved to unequal thermal expansion of individual beams, as a result of the temperature difference between the ends.

There are various actuation possibilities with three-beam structures, depending on the configuration of voltages applied to the cantilever ends (Figure 2.5(a) and (b)).

Furthermore, motion in the opposite direction is also possible by reversing the order of voltages applied.

Operation principle of two-beam structures is similar to that of three-beam structures; however it is possible to achieve motion only in one direction (Figure 2.5(c)).

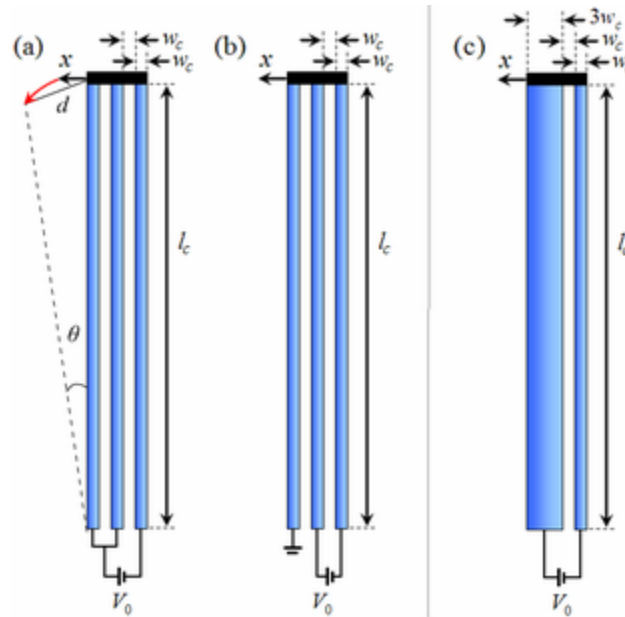


Figure 2.5 Schematic illustration of ((a) and (b)) three-beam and (c) two-beam thermal actuator arrangements

Mechanical Analysis:

For three-beam structures, length of each beam due to the application of a current through the actuator ends, i.e. $L_{c,i}$, can be calculated according to [33] as:

$$L_{c,i} = L_c (1 + \alpha T_i) - \frac{F_i}{k_{c,i}}, i = 1, 2, 3 \quad (2.12)$$

In the above expression, T_i is the average beam temperature, α is the coefficient of thermal expansion, F_i is the force applied to each beam by the end bar and $k_{c,i}$ is the tensile spring constant of each individual beam.

For small actuations, i.e. $d \ll \theta$, the following approximation can be made, where $\theta = (L_1 - L_2)/4w_c$ and w_c is the cantilever width of a three-beam thermal actuator:

$$d = L_c \theta \quad (2.13)$$

Assuming mechanical equilibrium, the above expression can be written in terms of the beam average temperature difference between hot and cold beams, i.e. $\Delta T = T_3 - T_1$, as:

$$d = \alpha \frac{L_c}{4w_c} \Delta T \quad (2.14)$$

Thermal Analysis:

Average temperature of inner and outer beams, i.e. beams 1 and 3, of a three-beam structure can be determined by solving the temperature distribution equation, $T(x)$, which is obtained from the steady-state continuity equation given below:

$$T''(x) = -C(x) = -\frac{J^2(x)\rho}{\kappa} \quad (2.15)$$

In the above expression, $J(x)$ is the current density, which is constant for each beam, ρ is the electrical conductance and κ is the heat conductivity of the beams. Note that, temperature distribution due to an applied current, I , was determined by [33], where

convective and radiative heat losses were neglected and the expression for the maximum temperature was found as follows:

$$T_{max} = \frac{9I^2\rho}{32\kappa w_c h_c} \quad (2.16)$$

Then, temperatures in beams 1 and 3 can be averaged as follows:

$$\Delta T = \frac{I^2\rho}{16\kappa w_c h_c} \quad (2.17)$$

Hence, actuation can be determined as a function of the applied current as follows:

$$d = \frac{\alpha\rho}{\kappa} \frac{L_c^2}{64w_c^2 h_c} I^2 \quad (2.18)$$

Note that, a current limit can be determined for either maximum actuation distance or melting temperature using the above expression.

A simple pair of thermally actuated nanotweezers can be designed by combining two opposing thermal actuators in a gripper setup (Figure 2.6(a) and (b)). Actuation is achieved by passing a current through cantilever arms by applying a voltage difference between their ends. Note that, both opening and closing actions are possible with thermally actuated devices with three-beam structure, where those with two-beam structure can only be closed.

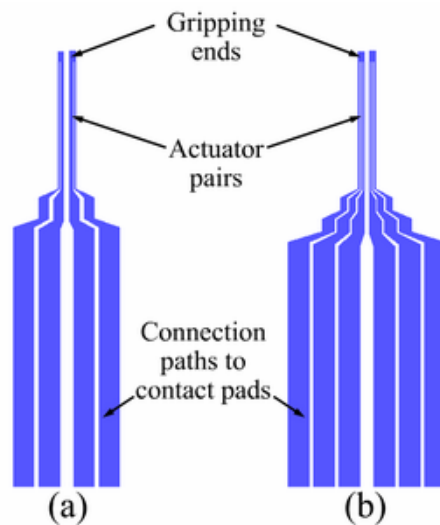


Figure 2.6 Schematic illustration of thermally actuated nanotweezers with (a) two- and (b) three-beam structures

Parameter Selection:

In addition to operational requirements, compatibility of design parameters for thermal actuation mechanisms with the process requirements for the electrostatic actuation mechanism, which is the main interest of this thesis, was also considered in the selection of the following design parameters for two- and three-beam thermal actuation mechanisms:

		Two-beam Structures	Three-beam Structures
Cantilever Beam Width	w_c	3 μm / 9 μm or 4 μm / 12 μm	3 μm or 4 μm
Gap Between Cantilever Beams	g_c	3 μm or 4 μm	
Device Height	h_c	7 μm	
Cantilever Beam Length	l_c	100, 200, 300 or 400 μm	

Table 2.3 Thermal actuator design parameters

Similar to the case in electrostatically actuated devices, thermally actuated devices with 5 μm - and 5 μm /15 μm - wide cantilever beams were also included in the fabrication mask, considering various issues related to fabrication processes, such as lithographic resolution.

Note that, due to time limitations and the fact that electrostatically actuated devices are the main focus of this thesis; analytical calculations were not carried out for the thermally actuated devices. Instead, only finite element analyses were performed in order to determine whether required displacement can be achieved properly with the structures designed, or not.

2.3. End-Effector Design

Design of nano-scale end-effectors is based on determination of position, orientation, shape and thickness of nanowires. Considering operational conditions and requirements for easy interaction with objects, nanowire end-effectors are designed to be located on outer corners of rectangular tip regions of both movable combs (Figure 2.7(a)). In the simplest case nanowires are fabricated using a similar approach as in [46] and [47], being straight in shape and pointing along 45° directions so that, they intersect at a 90° angle (Figure 2.7(b)).

Such nanotweezers, with end-effectors in the form of straight nanowires, enable interaction with any object, through any specific point. From this respect, they can be considered as perfect tools for various sensing, measurement and testing applications (Figure 2.7(c)). However, they are not well suitable for applications, where an object is to be gripped firmly or it is to be picked and placed. The reason for this is the difficulty of fabricating a 100% symmetric device due to challenges in fabrication processes. Furthermore, an instantaneous lateral instability, either mechanical or electrical, during operation might also lead to misalignment and engagement with the object might be lost (Figure 2.7(d)).

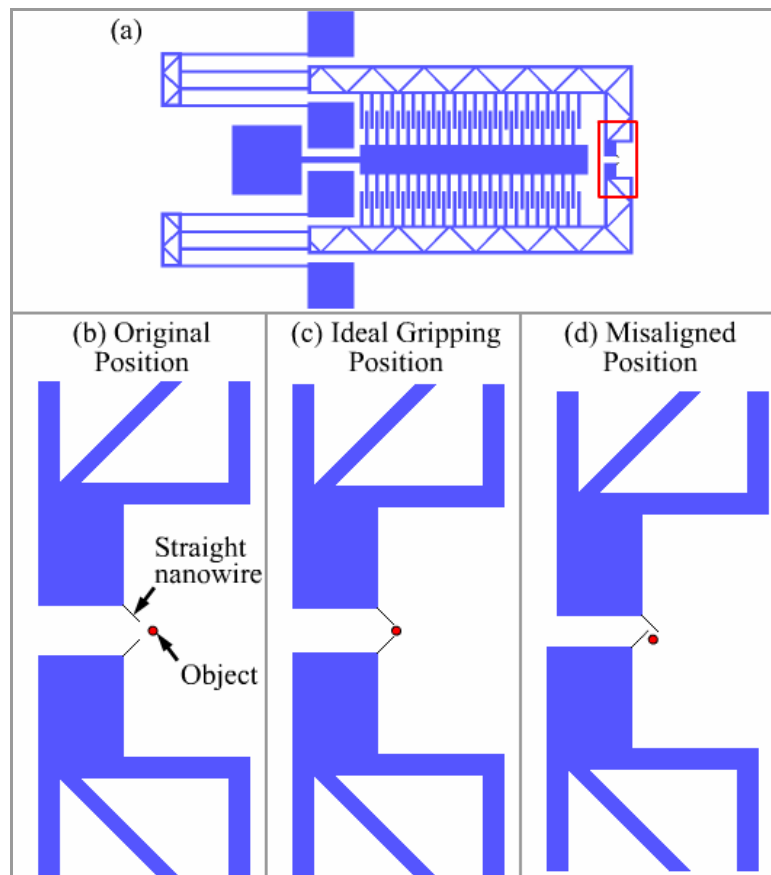


Figure 2.7 (a) A pair of nanotweezers with end-effectors in the form of straight nanowires and detailed views of the tip at: (b) original (c) ideal gripping and (d) misaligned positions

The problem of lateral misalignment can be solved by nanotweezers with end-effectors in the form of curved nanowires, fabricated using a similar approach as in [48] (Figure 2.8(a)). Gripping will be possible with devices, which have a reasonable amount of lateral misalignment, as well as an ideal device that is almost 100% symmetric (Figure 2.8(b)), (Figure 2.8(c)).

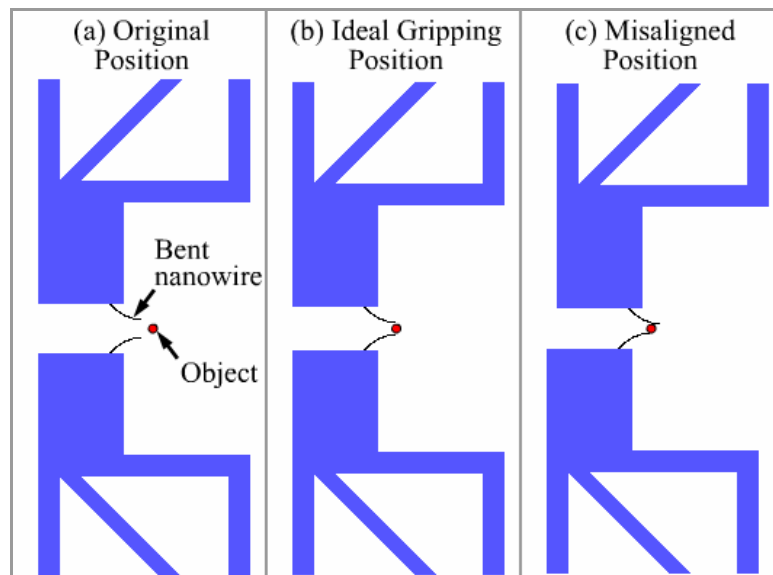


Figure 2.8 Detailed views of the tip of a pair of nanotweezers, similar to that of Figure 2.7(a), with end-effectors in the form of curved nanowires at: (a) original (b) ideal gripping and (c) misaligned positions

Although any lateral misalignment can successfully be eliminated with nano-scale end-effectors in the form of curved nanowires (Figure 2.9(a)), an out-of-plane misalignment may also be present due to various reasons again either during fabrication or operational instabilities.

If nano-scale end-effectors are in the form of typical nanowires, with a relatively small aspect ratio (Figure 2.9(b)), both nanowire-ends should be more or less at the same level in order to achieve ideal gripping of an object (Figure 2.9(c)). However, if there is a considerable amount of in-plane misalignment existing between nanowire-ends, it may not be possible to even catch the target object (Figure 2.9(d)).

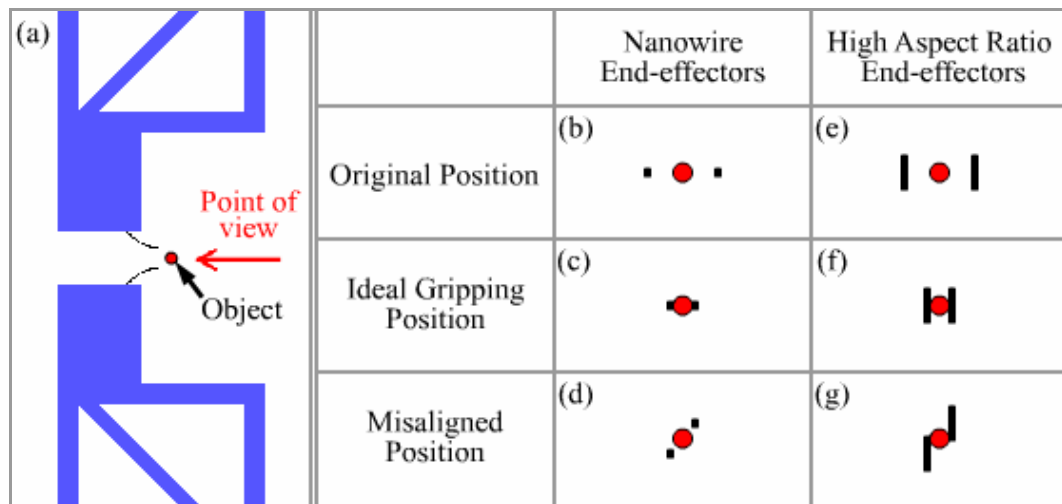


Figure 2.9 (a) Detailed top view given in Figure 2.8(a) with front views of end-effectors in the form of ((b), (c) and (d)) nanowires or ((e), (f) and (g)) high aspect ratio nanostructures at original, ideal gripping and misaligned positions

The problem of out-of-plane misalignment can be solved by nanotweezers with end-effectors in the form of high aspect ratio structures rather, which may be termed as *nanoribbons* (Figure 2.9(e)). Hence, gripping will be possible not only with ideal devices, which have nanowire-ends exactly at the same level (Figure 2.9(f)), but also with devices, which have nanowire-ends with a reasonable amount of out-of-plane misalignment (Figure 2.9(g)).

Placement of crack inducers with respect to actuator tips will be explained in detail in *Mask Design* chapter, i.e. Chapter 3.

2.4. Finite Element Analysis

2.4.1. Analysis of the Electrostatic Actuation Mechanism

After performing the analytical design, tip displacements corresponding to a chosen operation voltage of 80 V were determined by performing finite element simulations of different design possibilities. Two different software packages, FEMLAB and MATLAB with SUGAR add-in, were used for this purpose since complexity of FEMLAB model increases due to loss of symmetry about x-axis in devices anchored from single end.

Double-Anchored Devices:

Coupled electro-mechanical analysis of nanotweezers, which are anchored from both rear and front ends, was performed using FEMLAB as a finite element analysis tool by following a procedure that is similar to the one presented in a relevant FEMLAB tutorial [54]. Taking the advantage of symmetries about x- and y-axes, 2D model was defined being composed of only one quarter of a comb pair: a fixed comb and a movable comb with a double-folded cantilever flexure at the end (Figure 2.10).

Upper comb and the anchor of the double-folded cantilever beam were defined to be fixed in both directions, where edges of both combs, through which axis of symmetry passes, were defined to be fixed only in x-direction.

On the contrary to the real case, an electric potential equal to operating voltage was applied to the movable comb, where the fixed comb was grounded. Surrounding air was defined as a rectangle, within which following equation was solved in order to determine the induced electric field, E :

$$-\nabla \cdot (\epsilon \nabla V) = 0 \quad (2.12)$$

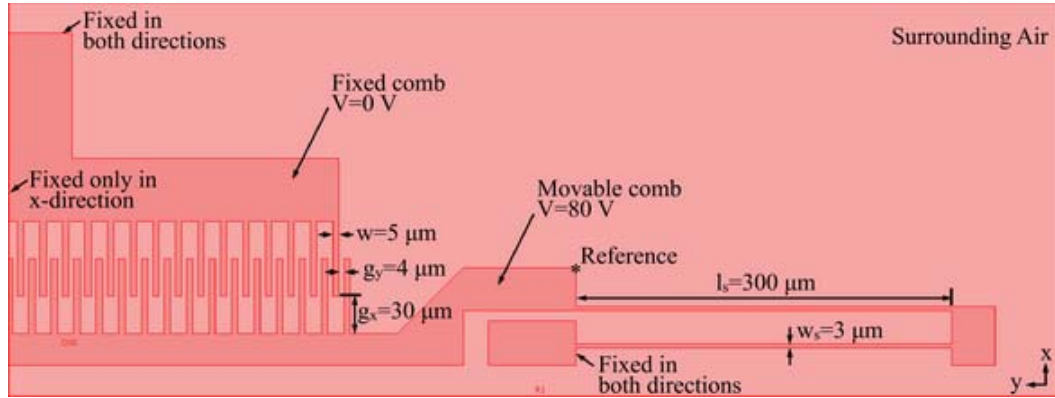


Figure 2.10 Example of a comb drive geometry defined in FEMLAB model:
a double-anchored device with $3 \mu\text{m} \times 300 \mu\text{m}$ beams and 30 fingers

In the above expression, ∇ is gradient operator and V is electric potential, where the relationship in-between is $E = -\nabla V$. Resulting electrostatic force was defined as a boundary load exerting on the movable comb, which is equal to the force density as:

$$F_{es} = \frac{\epsilon E^2}{2} \quad (2.13)$$

Starting from a zero voltage level, above expressions were solved for both resulting electric field and corresponding electrostatic force with 2 V increments and displacement of the structure due to an operation voltage of 80 V was calculated by FEMLAB solver. Note that, since displacement along y-axis is negligible, only x-displacement results were considered in analyzes (Figure 2.11).

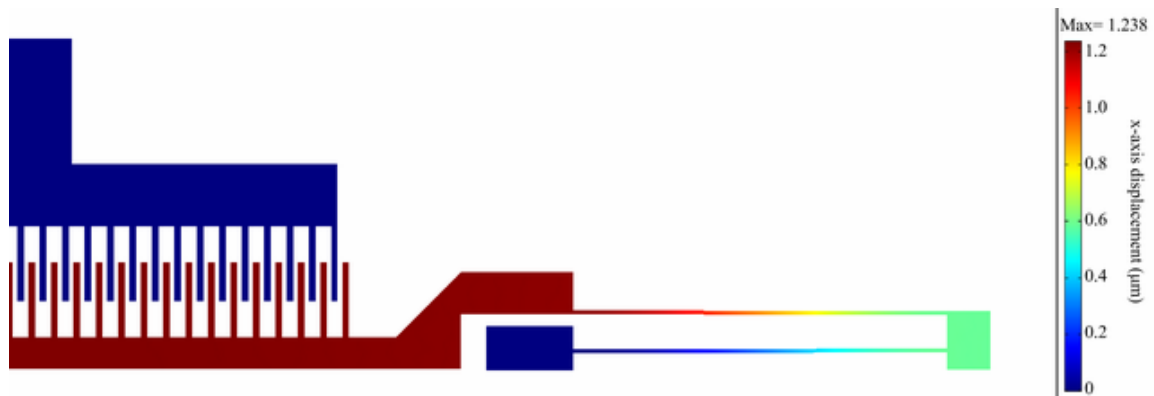


Figure 2.11 Displacements inside the comb drive due to application of an operation voltage of 80 V to the movable comb with color scale representing x-axis displacements

Furthermore, it is possible to plot the displacement of any point (i.e. reference point illustrated in Figure 2.1) on the comb drive as a function of the operation voltage (Figure 2.12). Note that, relationship between x-axis displacement and voltage is almost linear for mid-range voltages.

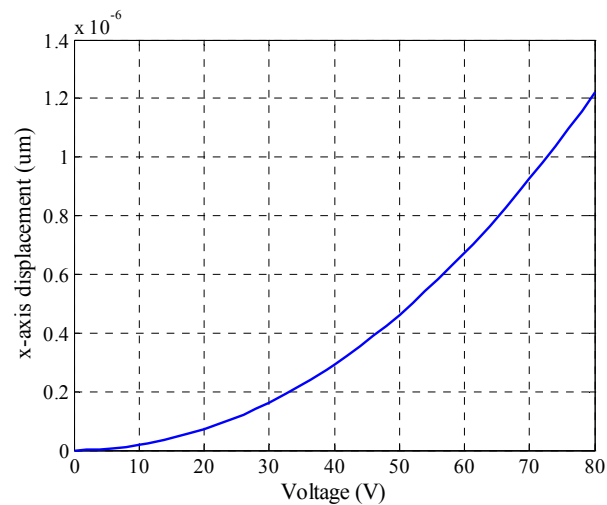


Figure 2.12 Displacement of a reference point as a function of the actuation voltage

In addition to total displacement and displacements in both x- and y-axes, it is also possible to plot the resulting electric potential field (Figure 2.13) and deformed mesh network (Figure 2.14) due to the application of an operation voltage of 80 V to the movable comb.

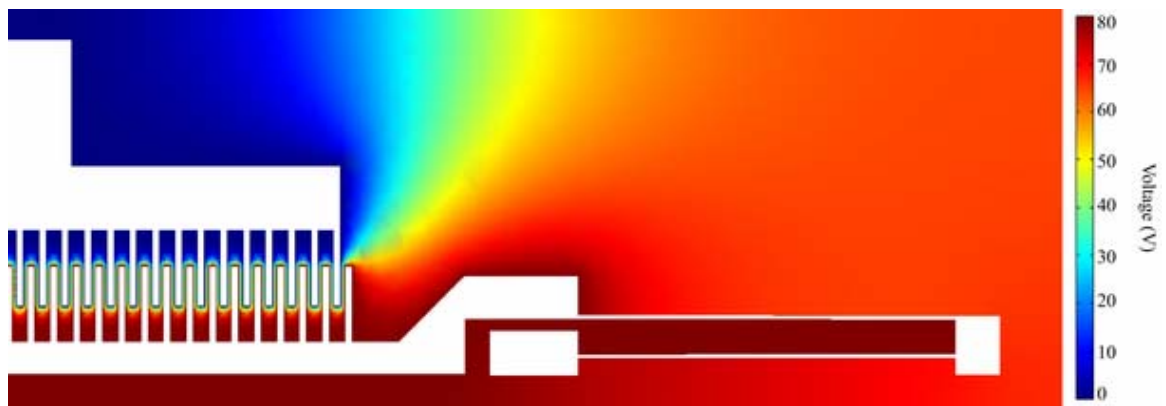


Figure 2.13 Electric potential field due to application of an operation voltage of 80 V to the movable comb

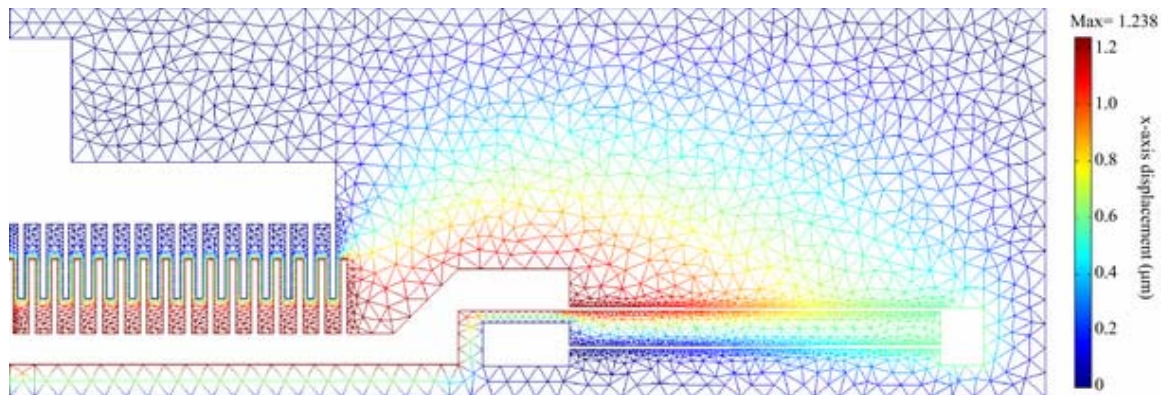


Figure 2.14 Deformed mesh network due to application of an operation voltage of 80 V to the movable comb with color scale representing displacements in x-direction

Tip displacement results, i.e. maximum y-displacement values due to the application of an operation voltage of 80 V, obtained for all design possibilities, except three, with double-spring arrangement are presented in Table 2.4.

$V_0 = 80 \text{ V}$	$N_f = 30$		$N_f = 40$		$N_f = 50$	
	$w_s = 3 \text{ } \mu\text{m}$	$w_s = 4 \text{ } \mu\text{m}$	$w_s = 3 \text{ } \mu\text{m}$	$w_s = 4 \text{ } \mu\text{m}$	$w_s = 3 \text{ } \mu\text{m}$	$w_s = 4 \text{ } \mu\text{m}$
$l_s = 300 \text{ } \mu\text{m}$	1.238 μm	X	1.754 μm	0.735 μm	2.185 μm	0.961 μm
$l_s = 400 \text{ } \mu\text{m}$	2.851 μm	1.299 μm	3.917 μm	1.792 μm	4.812 μm	2.343 μm
$l_s = 500 \text{ } \mu\text{m}$	5.287 μm	2.603 μm	6.450 μm	3.268 μm	7.475 μm	4.126 μm
$l_s = 600 \text{ } \mu\text{m}$	7.481 μm	4.109 μm	X	5.306 μm	X	6.239 μm

Table 2.4 Maximum x-axis displacement results for double-anchored devices at an operating voltage of 80 V

In the above table, results highlighted with yellow indicate displacements corresponding to a possible operation range. Hence, 80 V can be considered as a reasonable operating voltage for these designs, where others should be operated either lower or higher voltages than 80V. Note that, “X” represents designs, for which simulations were not performed since results can be estimated.

Single-Anchored Devices:

Due to the loss of symmetry about x-axis, complexity of the FEMLAB model for single-anchored devices increased since number of mesh elements is doubled. For this reason, a simpler analysis method, MATLAB with SUGAR add-in, was used for performing finite element analyzes of these devices. In SUGAR, devices can be defined being composed of nodes, cantilever beams and anchors and forces can be applied either as

point loads acting at nodes by writing a computer code. It is also possible to perform coupled simulation for simple comb-drive structures.

Since the mechanism for the nanotweezers is composed of a number of trusses, it was not possible to use the second method. Consequently, both movable combs were modeled, being composed of nodes, cantilever beams and anchors as mentioned above (Figure 2.15(a) and (b)). In addition to two movable combs, fixed combs on their both sides were also included to the SUGAR model as references, in order check the relative position of comb fingers with respect to other.

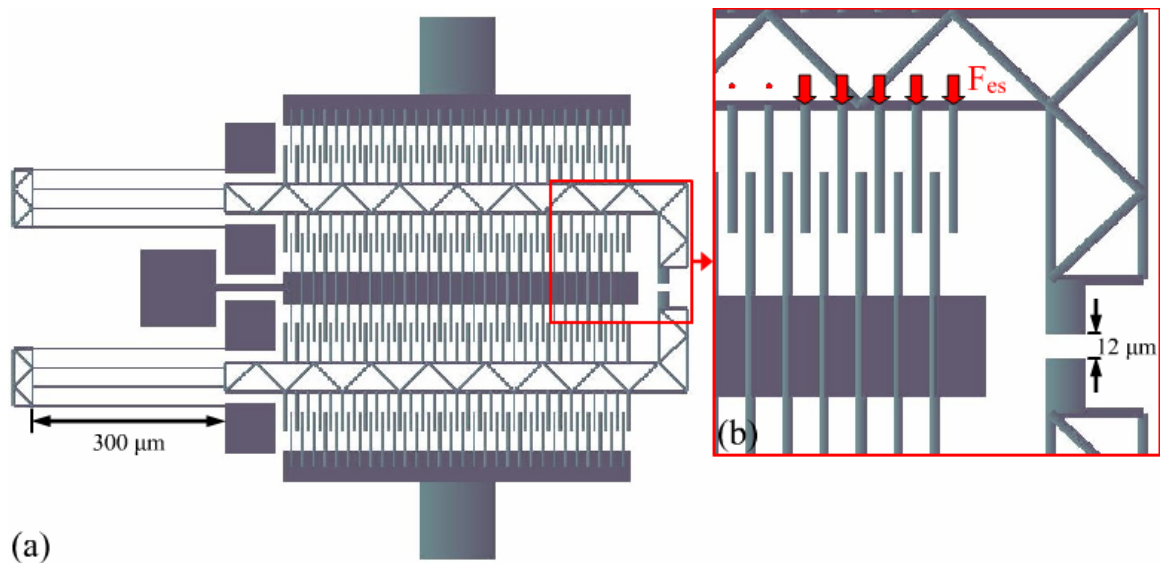


Figure 2.15 An example comb-drive geometry defined in SUGAR:

- (a) a five-comb single-anchored device with $3\ \mu\text{m} \times 300\ \mu\text{m}$ beams and 30 fingers and (b) detailed view illustrating application points for the electrostatic load

Point loads, with magnitudes equal to that of the analytically calculated electrostatic force induced by each comb finger pair due to the application of an operation voltage, were applied at end nodes of all comb fingers on both movable combs in opposite directions

(Figure 2.16(a) and (b)). It should be noted that, value of the electrostatic force slightly varies with displacement, being $0.1017 \mu\text{N}$ at a displacement of $2 \mu\text{m}$ and $0.1023 \mu\text{N}$ at a displacement of $5 \mu\text{m}$. For this reason, the value corresponding to $2 \mu\text{m}$ is used in simulations.

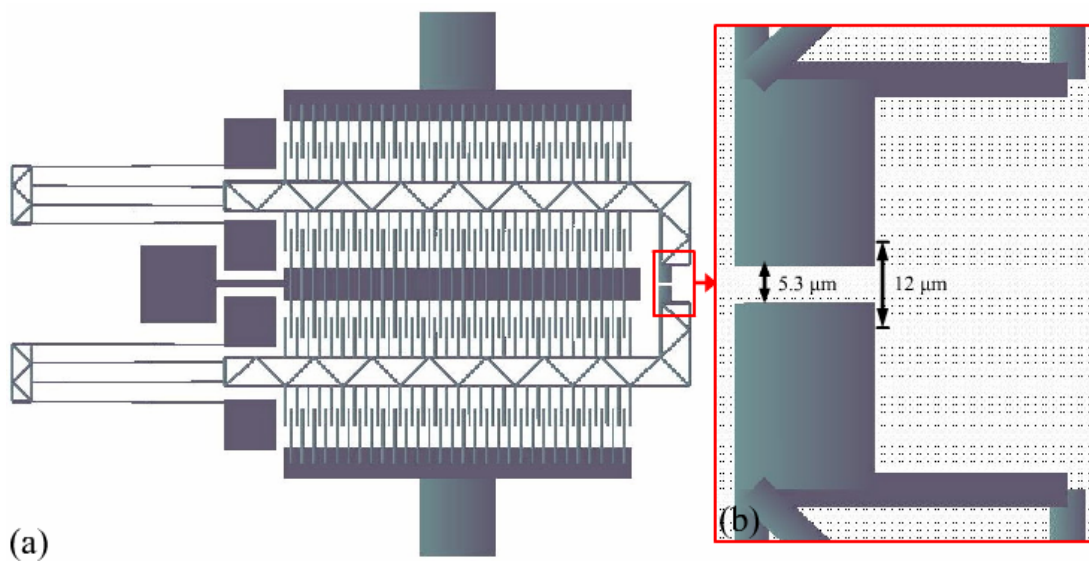


Figure 2.16 (a) Deformed state of the example comb-drive geometry of Figure 2.11(b) with (b) a more detailed view of the actuator tips

Tip displacement results, i.e. maximum x-displacement values due to the application of an operation voltage of 80 V , obtained for all design possibilities with single-spring arrangement are presented in Table 2.5.

$V_0 = 80 \text{ V}$	$N_f = 30$		$N_f = 40$		$N_f = 50$	
	$w_s = 3 \text{ } \mu\text{m}$	$w_s = 4 \text{ } \mu\text{m}$	$w_s = 3 \text{ } \mu\text{m}$	$w_s = 4 \text{ } \mu\text{m}$	$w_s = 3 \text{ } \mu\text{m}$	$w_s = 4 \text{ } \mu\text{m}$
$l_s = 300 \text{ } \mu\text{m}$	3.35 μm	1.72 μm	4.08 μm	2.57 μm	5.00 μm	3.65 μm
$l_s = 400 \text{ } \mu\text{m}$	6.28 μm	3.46 μm	10.11 μm	4.98 μm	13.25 μm	6.76 μm
$l_s = 500 \text{ } \mu\text{m}$	13.59 μm	8.55 μm	18.64 μm	8.78 μm	24.05 μm	11.61 μm
$l_s = 600 \text{ } \mu\text{m}$	23.93 μm	10.36 μm	31.19 μm	14.30 μm	39.87 μm	18.61 μm

Table 2.5 Maximum x-axis displacement results for single-anchored devices at an operating voltage of 80 V

As in Table 2.4, results highlighted with yellow again indicate displacements corresponding to a possible operation range and 80 V can be considered as a reasonable operating voltage for these designs, where others should be operated either lower or higher voltages than 80V.

Note that, in order to cross-check the reliability of the procedure used in the SUGAR analysis, a similar method is conducted also for double-anchored devices and it was concluded that the procedure is valid due to the close-agreement of the results obtained using FEMLAB.

2.4.2. Analysis of the Thermal Actuation Mechanism

In order to determine whether it is possible to achieve proper actuation with design parameters selected for the thermal actuation mechanisms, or not, finite element simulations of the structures were performed using CoventorWare as the software package.

Coupled electro-thermo-mechanical analyses of nanotweezers, with either two- or three- beam arrangements were performed by following a procedure that is similar to the

one presented in a relevant CoventorWare tutorial [55]. 3D solid models of a single actuator arm for all design possibilities were created using CoventorWare Designer (Figure 2.17(a)).

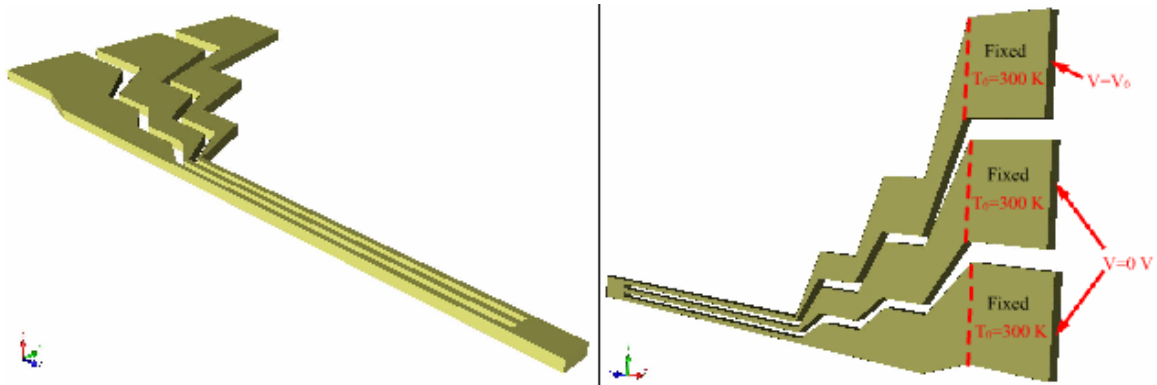


Figure 2.17 Example of a thermal actuator geometry defined in CoventorWare solid model: a three-beam structure with $3\ \mu\text{m} \times 200\ \mu\text{m}$ beams

Then, mesh models were created from the solid models and patches, at which thermal, mechanical and electrical boundary conditions were defined using CoventorWare Preprocessor.

Bottom of the rectangular regions at cantilever beam-ends were defined to be fixed in all x-, y- and z-axes as the only mechanical boundary condition (Figure 2.17(b)). Similarly, initial temperatures at these regions were set to 300 K as the only thermal boundary condition. Electrical boundary conditions were applied by setting the potential at the rear faces of the rectangular regions at the cantilever-ends to either zero or operation voltage, depending on actuator type and operation mode.

Then, simulations were performed using MemMech Solver of CoventorWare MEMS Module in Electro-thermo-mechanical mode and results were observed using CoventorWare Visualizer (Figure 2.18(a) and (b)).

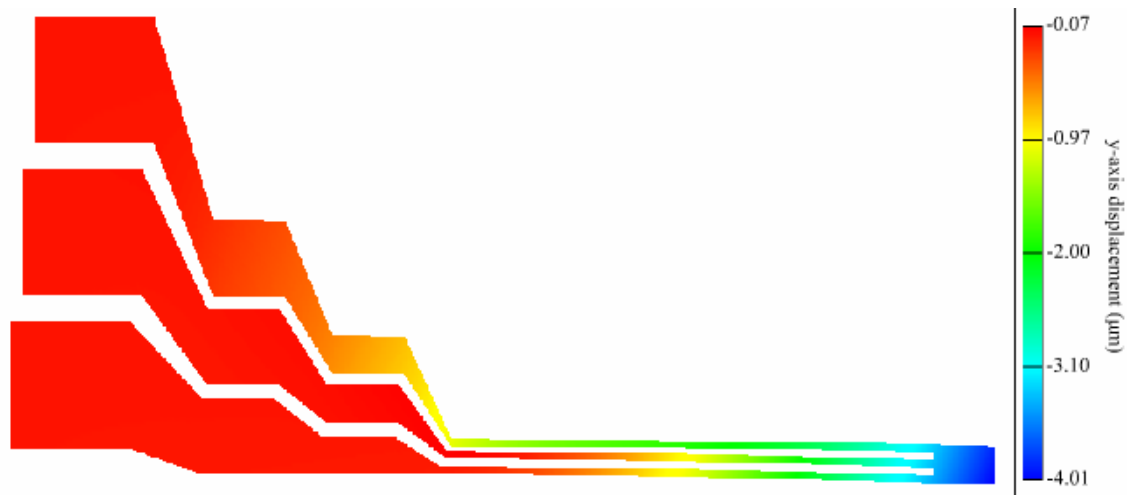


Figure 2.18 Displacements inside the three-beam thermal actuator due to application of an operating voltage of 0.20 V to the outmost cantilever beam with color scale representing y-axis displacements

Tip displacement results, i.e. maximum y-displacement values due to the application of an operation voltage of 0.20 V, obtained for all design possibilities of thermal actuation mechanisms are presented in Table 2.6.

$V_0 = 0.20 \text{ V}$	Two-beam Structures		Three-beam Structures	
	$w_c = 3 \text{ } \mu\text{m}$	$w_c = 4 \text{ } \mu\text{m}$	$w_c = 3 \text{ } \mu\text{m}$	$w_c = 4 \text{ } \mu\text{m}$
$l_c = 100 \text{ } \mu\text{m}$	0.91 μm	0.91 μm	2.11 μm	1.98 μm
$l_c = 200 \text{ } \mu\text{m}$	3.18 μm	2.73 μm	4.10 μm	3.58 μm
$l_c = 300 \text{ } \mu\text{m}$	6.66 μm	6.38 μm	6.83 μm	5.73 μm
$l_c = 400 \text{ } \mu\text{m}$	10.23 μm	9.69 μm	10.51 μm	8.41 μm

Table 2.6 Maximum y-axis displacement results thermal actuation mechanisms at an operating voltage of 0.20 V

It should be noted that actual operation voltage is not 0.20 V, but higher. However, a large amount of the applied voltage is dissipated at the connection paths beyond actuator devices, contact pads and probes. For this reason, performing the simulations by applying constant current densities instead of constant voltages at the rear faces of the rectangular regions at the cantilever-ends will yield more beneficial results in terms of operation conditions.

In addition to lateral displacement along y-axis, cantilever structures also elongate longitudinally along x-axis. Maximum longitudinal displacement results are presented in Table 2.7.

$V_0 = 0.20 \text{ V}$	Two-beam Structures		Three-beam Structures	
	$w_c = 3 \text{ }\mu\text{m}$	$w_c = 4 \text{ }\mu\text{m}$	$w_c = 3 \text{ }\mu\text{m}$	$w_c = 4 \text{ }\mu\text{m}$
$l_c = 100 \text{ }\mu\text{m}$	1.25 μm	1.37 μm	1.32 μm	1.41 μm
$l_c = 200 \text{ }\mu\text{m}$	1.84 μm	1.97 μm	1.97 μm	2.06 μm
$l_c = 300 \text{ }\mu\text{m}$	2.42 μm	2.61 μm	2.63 μm	2.72 μm
$l_c = 400 \text{ }\mu\text{m}$	2.88 μm	3.17 μm	3.38 μm	3.28 μm

Table 2.7 Maximum longitudinal displacement results for thermal actuation mechanisms at an operating voltage of 0.20 V

In addition to maximum displacement values, current density, electric potential and temperature distributions can also be visualized. Maximum temperature value reached at an operation voltage of 0.20 V turned out to be 990.6 K. Note that, convection effect of the surrounding air was not included in finite element simulations, i.e. similar to operation in vacuum.

Chapter 3

MASK DESIGN

3.1. Introduction

Mask design is among the most important points in MEMS design, including various issues to be considered due to process limitations. As the number of masks to be used in a process increases, complexity of mask design also increases, leading to a decrease in both yield and success rate of the fabrication process due to added requirements as alignment of each mask with respect to the previous ones. Fabrication of the nanotweezers is such a complex process including four subsequent masking steps for *Crack Initiation*, *Crack Widening*, *Electroplating* and *Wire Cutting*, respectively.

In this chapter, basic process flow will be introduced initially. Following that, issues considered in the design of each mask will be explained in detail, together with the design procedure for individual chips within the wafer and alignment marks.

3.2. Basic Process Flow

Fabrication process for the electrostatically actuated nanotweezers, illustrated in Figure 3.1, starts with a low-resistivity (i.e. $< 0.0025 \Omega \text{ cm}$) (100) silicon wafer, which is 500-550 μm -thick and 4-inch in diameter. The purpose of using a low-resistivity wafer is to reduce the resistance of the substrate during the electroplating of the nanowires.

First step is the etching of 5.5 to 10 μm -deep grooves with either sharp edges or straight surfaces into the substrate via Inductively-Coupled Plasma Deep-Reactive Ion Etching (ICP-DRIE) (Figure 3.1(a)). These grooves serve as initiation and termination sites for crack propagation in the sacrificial SiO_2 film, and they are to be used as molds for nanowire formation. The mask to be used in the DRIE process is a 1.5 μm -thick photoresist film, patterned using “Crack Initiation Mask”.

Next step is the fabrication of the nanowires via guided self-assembly [47-50]. For this purpose, a 4.5 μm -thick SiO_2 layer with an altered chemistry is deposited on the substrate, by means of a low-temperature plasma-enhanced chemical vapor deposition (PECVD) process (Figure 3.1(b)). Afterwards, cracks are formed at the pre-specified locations by cyclic annealing at 500° C for 40 minutes (Figure 3.1(c)). In order to achieve a uniform electric field distribution through low substrate resistance during electroplating, a thin layer of chromium and gold is deposited on the wafer at the back, which is then covered with a photoresist film to prevent any deposition on it. Since the opening at the Si- SiO_2 interface is on the order of only a few nanometers, the cracks should be widened slightly by etching in buffered hydrofluoric acid (BHF) just before electroplating (Figure 3.1(d)) and nanowires are deposited inside these widened cracks using a nickel electroplating bath (Figure 3.1(e)).

Prior to electroplating of the devices, it is necessary to deposit a plating base (i.e. seed layer). In order to make use of this layer also for achieving the integration of nanowire end-effectors with device tips, portions of crack openings overlapping with device tips (i.e. nanowire-actuator interface) should further be widened by wet etching in BHF so that seed layer atoms can easily penetrate inside and adhere to the nanowire surface at these locations. For this purpose, a 1.5 μm -thick photoresist film is spun on the wafer and patterned using “Crack Widening Mask” (Figure 3.1(f)). This mask prevents the etching of the sacrificial SiO_2 layer in BHF completely, exposing only the regions corresponding to the device tips. Then, a 10 nm/200 nm-thick Cr/Au layer is deposited on the wafer by evaporation, which not

only provides the connection between nanowire end-effectors and devices, but also serves as a plating base for device deposition (Figure 3.1(g)).

After the seed layer deposition, a 9.5 μm -thick photoresist film is spun on the wafer and patterned using “Electroplating Mask”. Hence, a mold defining the chip boundaries, actuator devices and their position within the wafer is prepared and device deposition is performed using a standard Ni electroplating bath (Figure 3.1(h)).

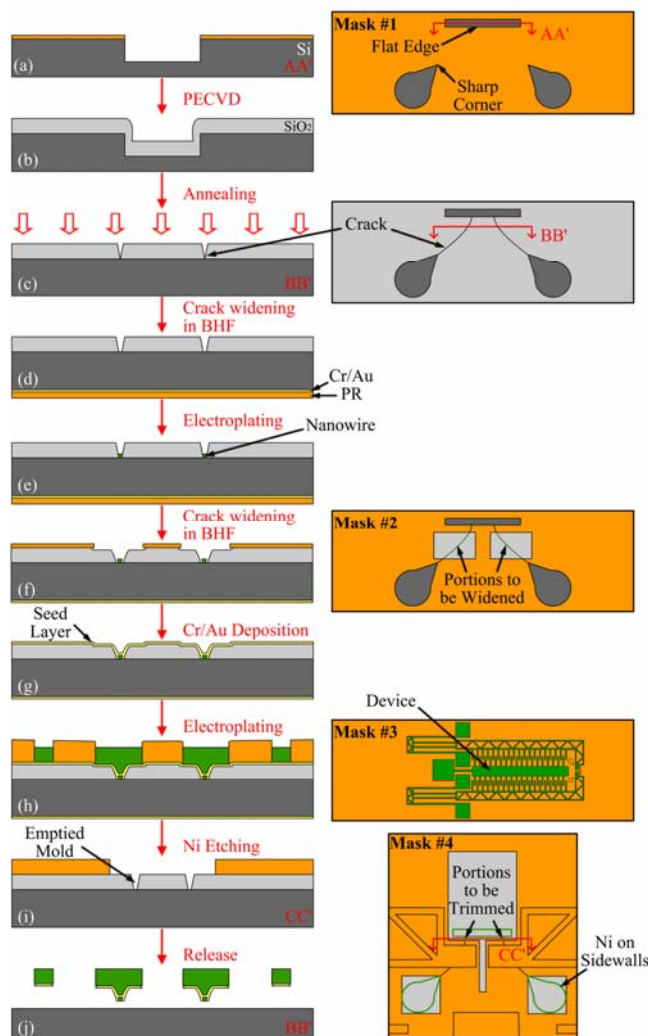


Figure 3.1 Basic fabrication process

Last step before the release process is separating the nanowire ends from crack initiation and termination sites and cutting them to a desired length. This can be done by wet etching of Ni in nitric acid using a 6.2 μm -thick photoresist mask patterned with “Wire Cutting Mask” (Figure 3.1(i)). This mask exposes only the Ni deposited on the side walls and the portions of the nanowires to be cut. Finally, nanotweezers are to be released by removing the entire sacrificial SiO_2 layer in BHF and lowering the Si surface underneath in KOH, respectively (Figure 3.1(j)).

3.3. Design of the Mask for “Crack Initiation”

Crack Initiation Mask (i.e. Mask #1 in Figure 3.1) is the first mask of the fabrication process for the nanotweezers, which is used in etching of the crack initiation patterns in the form of deep grooves with either sharp edges or flat surfaces into the Si substrate by ICP-DRIE. Sharp corners of these patterns designate the initiation sites for cracks forming in the sacrificial SiO_2 layer when annealed, where flat edges serve as termination sites determining the crack form and orientation. Beyond the oxide chemistry, geometry and position of the crack patterns is of vital importance in nanowire fabrication by guided self-assembly.

Design rules for Crack Initiation Mask can be listed as follows:

- Tips of crack indenters should be neither too steep, nor too obtuse,
- Tips of crack indenters should be at least 15 μm -long,
- Distance between mating crack indenters should be greater than 20 μm ,
- Angle between pointing directions of mating crack indenters should be 90° ,
- Crack indenters should be placed as close as possible to points, where the wires are to be connected to device tips.

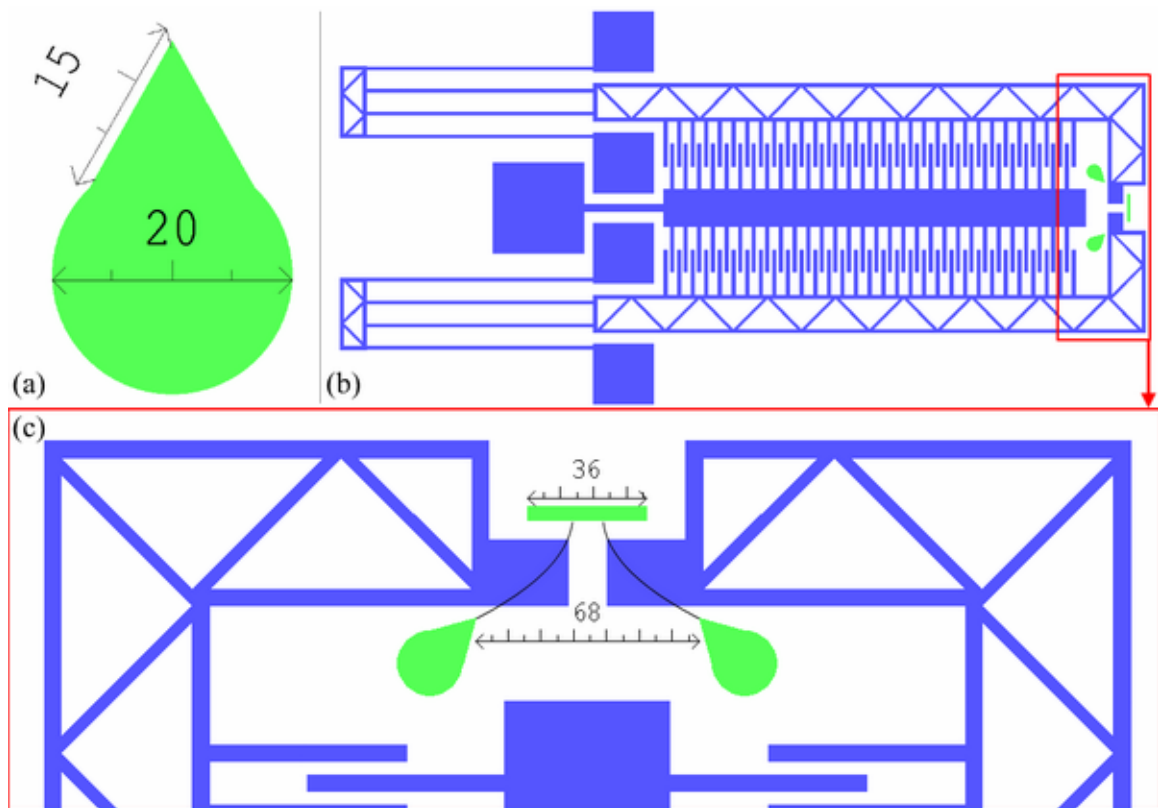


Figure 3.2 (a) A single crack inducer, (b) position of a pair of crack inducers with respect to the device and (c) detailed view of crack initiation and termination sites showing proposed crack paths including dimensions in μm 's

Considering first two design rules mentioned above, geometry of a single crack indenter is designed being composed of a circle, which is 20 μm in diameter, and an equilateral triangle, with 15 μm edge-length, as shown in Figure 3.2(a).

Position of two mating crack indenters with respect to each other along with their position with respect to the device tip is determined according to the last three design rules, as shown in Figure 3.2(b).

As a second design possibility, curved nanowires can be fabricated in addition to straight nanowires by etching groves with flat surfaces in front of a crack indenter pair (Figure 3.2(c)).

Note that, lower surface of the $4\ \mu\text{m}$ by $36\ \mu\text{m}$ rectangle serves as a crack termination site, at which cracks initiating from sharp tips of the crack indenters tend to approach with right angles and bend consequently.

3.4. Design of the Mask for “Crack Widening”

Crack Widening Mask (i.e. Mask #2) is the mask to be used in the protection of the sacrificial SiO_2 layer from completely being etched during the widening of crack openings at nanowire-device interfaces, exposing only these regions to BHF.

Design rules for Crack Widening Mask are simple:

- Portions of crack openings, which overlap with actuator tips should be fully covered,
- Exposed regions should not exceed overlap areas in order to eliminate further metal deposition at nanowire ends.

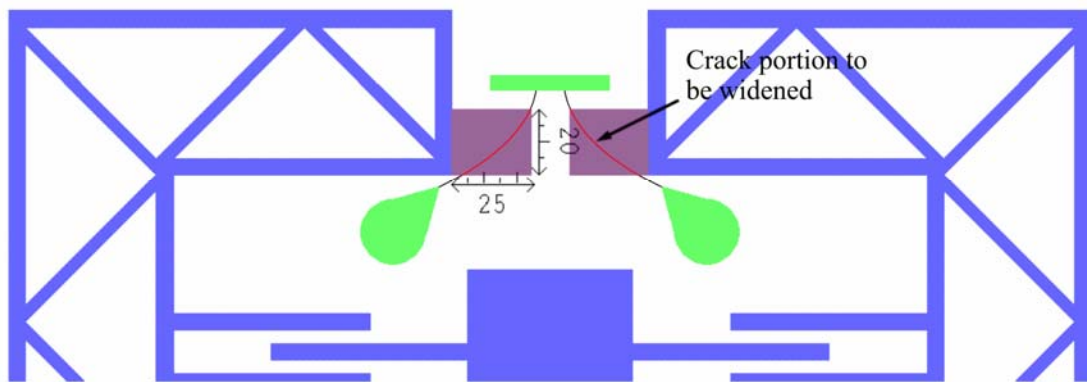


Figure 3.3 Relative position of crack widening patterns with respect to device tip showing crack portions to be widened including dimensions in μm 's

Considering the above rule, crack widening openings are designed as 20 μm by 30 μm rectangles covering the device tips, exposing any portion of a nanowire coinciding with this region (Figure 3.3).

3.5. Design of the Mask for “Electroplating”

Electroplating Mask (i.e. Mask #3) is the mask, which defines shapes of Ni structures and actuator devices together with their positions within the wafer. Positions of features within other masks are adjusted according to the devices after their placement within this mask.

Design of the Electroplating Mask is mainly based on chip design, which involves the arrangement of devices, contact pads and labels within individual chips.

Design rules for the Electroplating Mask can be listed as:

- Chips should be large enough for easy processing and handling after dicing,
- Chips should be framed with a metal band for device protection during dicing,
- No metal should be deposited along dicing corridors (i.e. spacing between neighboring chips, covered by all etching masks),
- Contact pads should be located on one side of each chip, where devices should be located on the other with their tips pointing out for the ease of wire bonding process and characterization using a probe station,
- Device labels, contact pad labels and paths connecting device anchors to pads should be large enough to remain anchored,
- Any dimension of a feature to be anchored should be greater than 25 μm , which is the maximum dimension to be released.

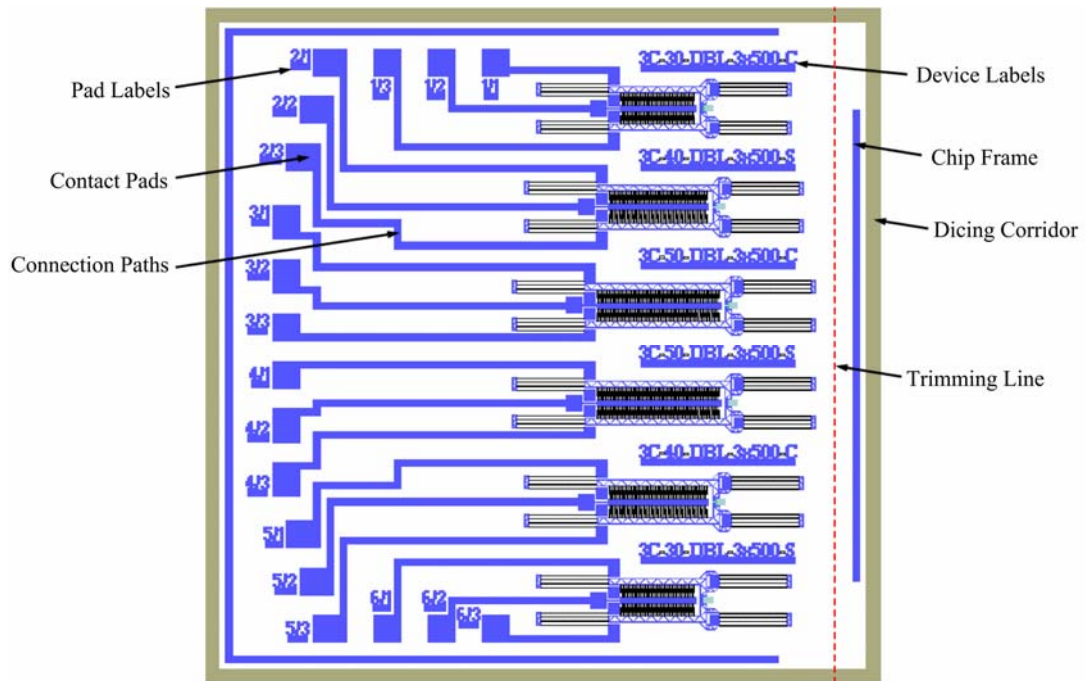


Figure 3.4 Layout of a square chip for 3-comb devices

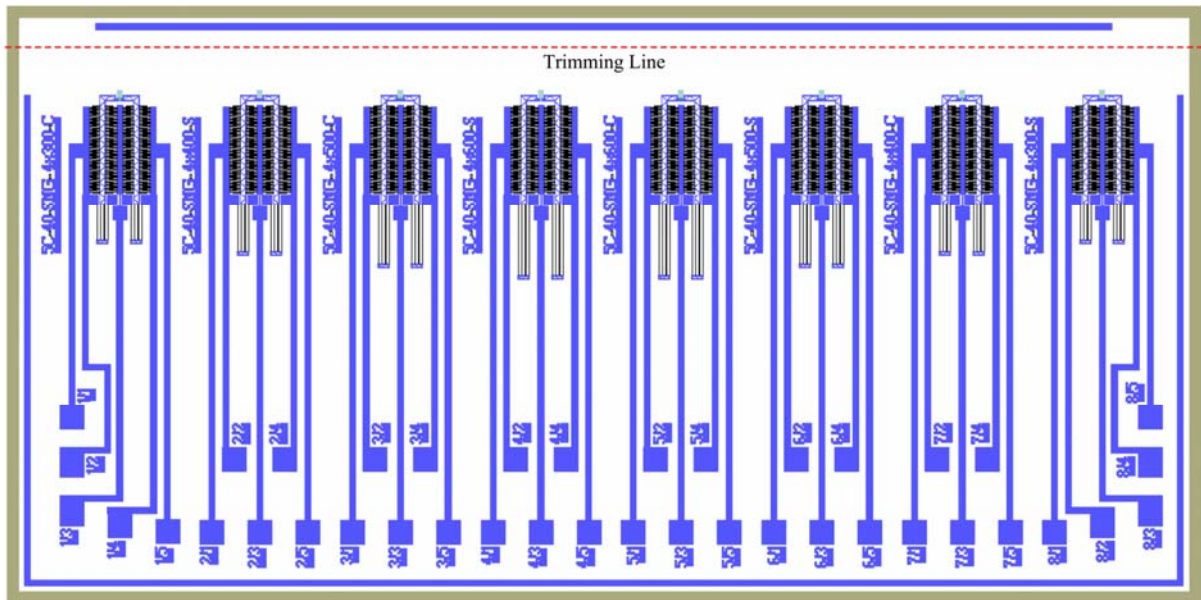


Figure 3.5 Layout of a rectangular chip for 5-comb devices

Two different chip types, with square and rectangular shapes, are designed for according to the rules stated above. Square chips are 5mm on one side and contain six devices with 3-comb arrangement (Figure 3.4), where rectangular dies are 5 mm by 10 mm in dimension and contain eight devices with 5-comb arrangement (Figure 3.5).

There exist 200 μm wide dicing corridors between neighboring chips and each chip is surrounded by a 50 μm wide metal frame. Two corners of this frame, those on the device side, are left open to enable trimming of chips for easy access to the operation region of the devices during characterization.

Contact pads are 200 μm by 200 μm each and they are connected to device anchors via 50 μm wide metal paths. Both pads and devices are labeled in order to identify devices during characterization. Although line thickness of the fonts for the labels is 25 μm , which is smaller than the maximum width to be released, 50 μm wide line is inserted at the bottom of each label in order to make sure that it will remain anchored after release.

3.6. Design of the Mask for “Wire Cutting”

Final mask to be used in the fabrication process is the Wire Cutting Mask (i.e. Mask #4). It exposes excess Ni layer on sidewalls of the crack initiation patterns and nanowire ends to HNO_3 while protecting the rest of the Ni structures from being etched. The purpose is detaching nanowires from the metal layer deposited on walls of the crack initiation pattern and trimming them into the desired length (i.e. $\sim 2 \mu\text{m}$).

Two design rules for the Wire Cutting Mask are:

- Area exposed should be as large as possible to account for different outcomes of crack propagation and mask misalignment,
- Area exposed should not be too close to Ni structures to prevent any possible damage on them.

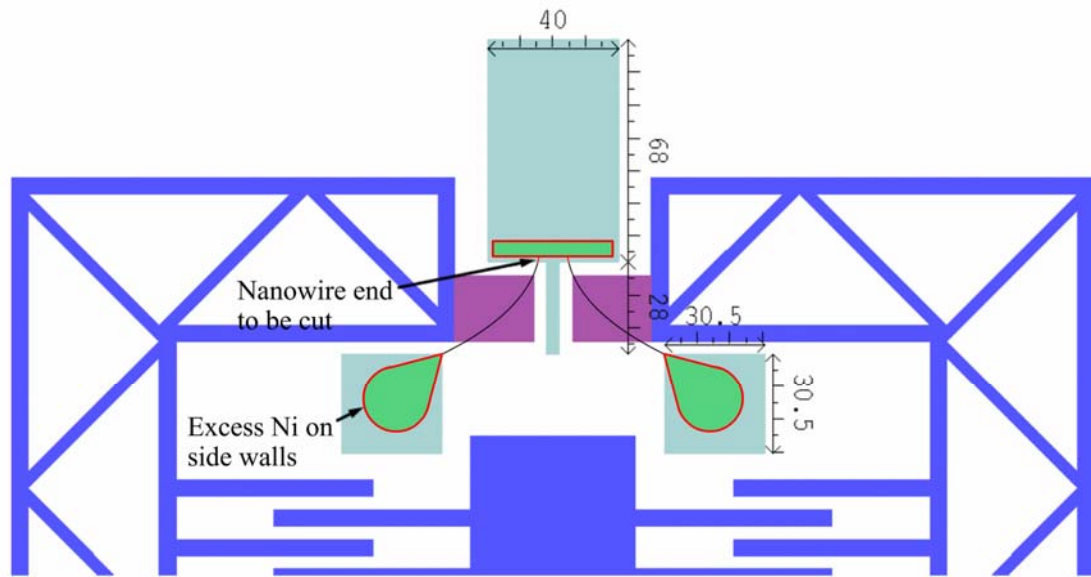


Figure 3.6 Relative position of wire cutting patterns with respect to device tip showing nanowire portions to be trimmed including dimensions in μm 's

Considering the rules stated above, wire cutting openings are designed in the form of rectangular regions covering nanowire ends, crack initiation and termination patterns, also extending through the operation area of the device (Figure 3.6).

3.7. Design of Nanowire Test Structures

Two different test structures are designed in order to characterize mechanical and electrical properties of nanowires, as well as the material properties such as Young's modulus or density.

First test structure is designed to fabricate clamped-clamped nano-beams with lengths ranging from $10\ \mu\text{m}$ to $160\ \mu\text{m}$ (Figure 3.7(a)). It is composed of an inclined groove with triangular crack inducers of $50\ \mu\text{m}$ periodicity on one side, and a matching straight groove to serve as a free surface for crack termination on the other. Both initiation and termination

points are covered with 50 μm wide metal layers in order to make sure that they will remain anchored after release.

Second test structure is designed to fabricate free-standing nano-cantilevers, again with lengths ranging from 10 μm to 160 μm (Figure 3.7(b)). It is composed of a straight groove with triangular crack inducers of 50 μm periodicity on one side and similarly, a matching straight groove to serve as a free surface for crack termination on the other. Only initiation sites are covered with the 50 μm wide metal layer, where termination sites are covered with the a triangular region in the Wire Cutting Mask in order to detach nanowires from one end and trim them into desired lengths.

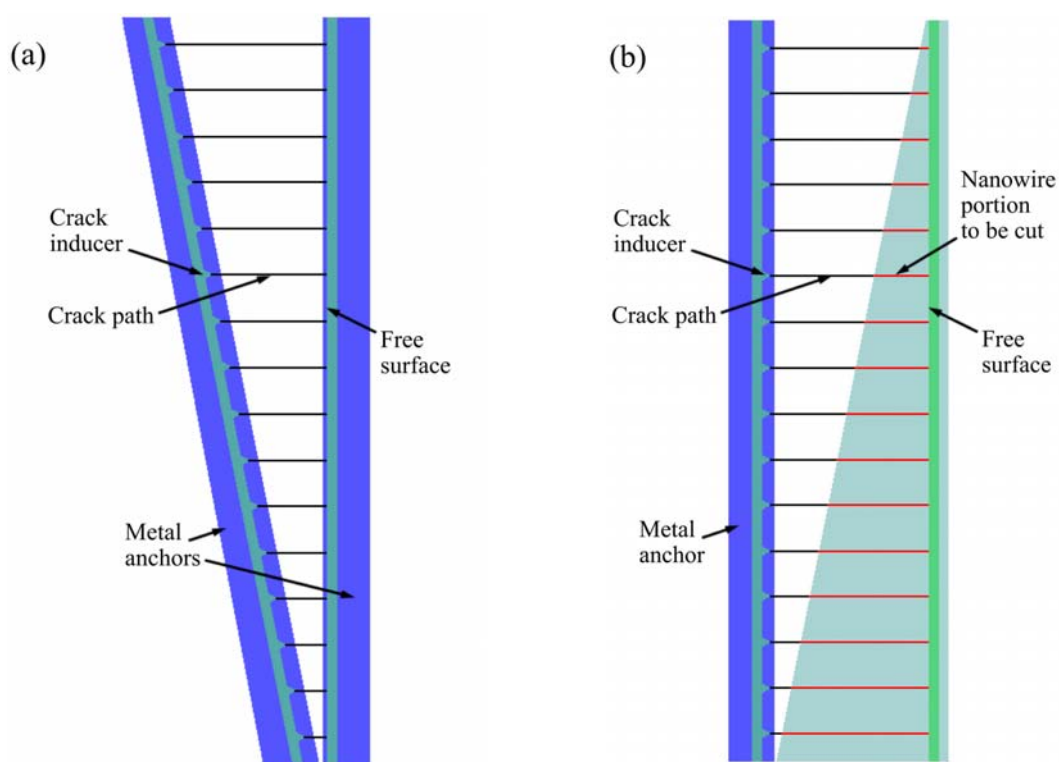


Figure 3.7 Nanowire test structures for (a) clamped-clamped nano-beams and (b) free-standing nano-cantilevers with proposed crack paths

3.8. Design of Alignment Marks

Fabrication process for the nanotweezers includes four subsequent masking steps, where precise mask alignment is essential due to the small size of nanowires and importance of their orientation with respect to device tips for practical usage.

Design rules related to alignment marks can be listed as follows:

- Area occupied by each alignment mark should not exceed 400 μm by 300 μm ,
- Pattern of alignment mark should be different for all masks to avoid confusion,
- Features on the reference should be ~ 40 μm on one edge,
- Features on the mask to be aligned should be ~ 5 to 10 μm smaller than those on the reference,
- Distance between the features should be ~ 30 to 50 μm .

Considering the design rules stated above alignment marks on Mask #1 are designed being composed of an array of nine squares with 30, 35 or 40 μm edge lengths (Figure 3.8). Horizontal distance between each feature is 40 μm for all masks. However, vertical distance changes between 30 to 50 μm within the columns of all masks and form a different pattern, so that alignment mask of each mask can easily be distinguished from others.

In addition to alignment marks, lithography test patterns in the form of lines, squares and rectangular shapes with dimensions ranging from 1 μm to 10 μm are inserted on each mask, in both negative and positive manner (Figure 3.9). The purpose is optimizing process times for each lithography step according to the minimum line width that is completely transferred on the photoresist layer exposure and development.

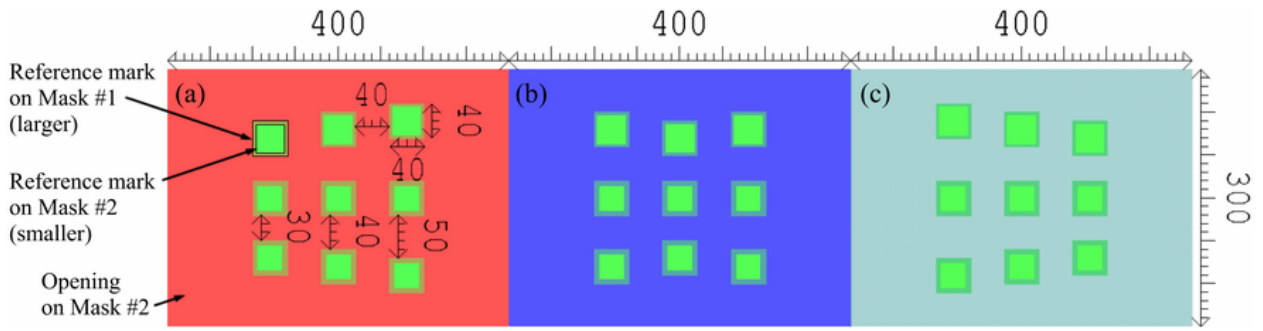


Figure 3.8 Alignment marks for (a) Mask #2, (b) Mask #3 and (c) Mask #4 with respect to Mask #1 including dimensions in μm 's



Figure 3.9 Lithography test patterns on Mask #1

Lithography test patterns are located above alignment marks in a test chip, which is dedicated for wafer alignment (Figure 3.10).

3.9. Wafer Layout

After both device and test chips are designed, final issue with the mask design is the arrangement of individual chips within the wafer considering the basics of all fabrication processes together with the following dicing process.

Some rules to be considered when determining the wafer layout can be listed as follows:

- Chips on the same row should have the same height,
- Chips on the same column should have the same width,
- Important chips should be located away from wafer edge,
- Two alignment chips should present on the wafer,
- Alignment chips should be located just above or below the vertical center line, being ~ 10 mm inside from both right and left sides,
- Electrical contact points of holder to be used in electroplating should remain open in the Electroplating Mask.

Wafer layout designed considering above rules can be seen in Figure 3.11.

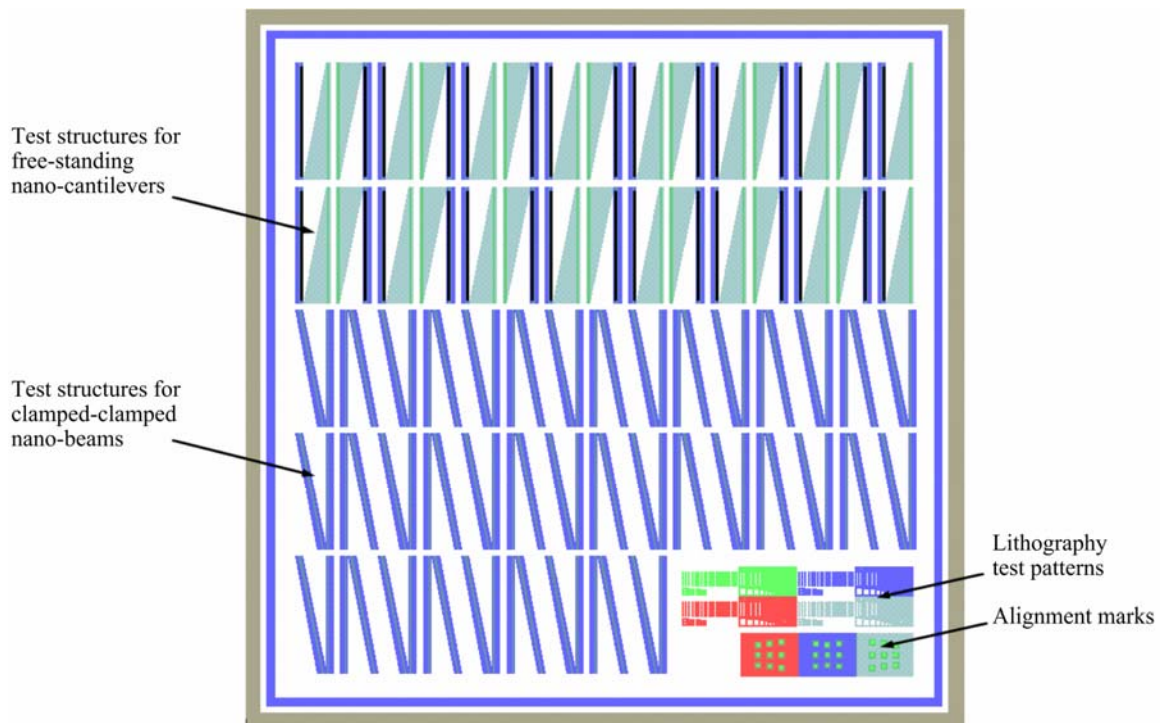


Figure 3.10 Layout of a test chip including alignment marks

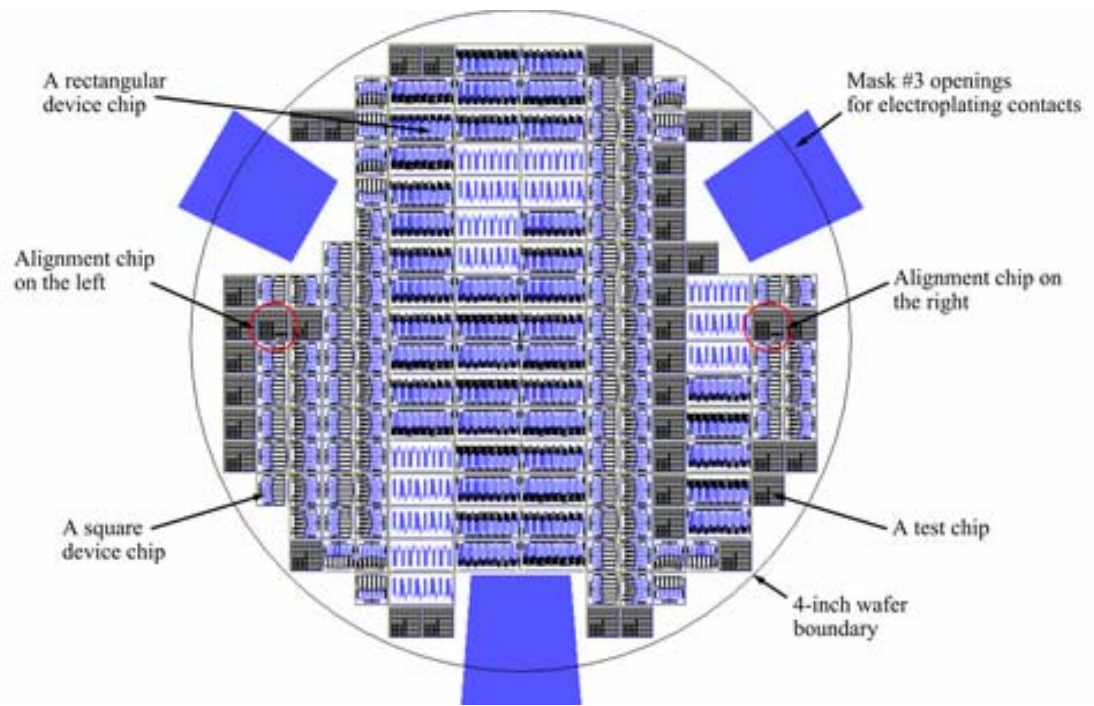


Figure 3.11 Layout of the wafer

Chapter 4

FABRICATION

4.1. Introduction

Technique employed in the fabrication of electrostatically actuated nanotweezers is a novel approach based on a batch-compatible method, which enables the integration of nano-scale end effectors to a microelectronic actuation mechanism. For this reason, design of the fabrication sequence is a complex procedure, which involves consideration of many aspects such as compatibility of processes with each other, availability of equipment and effect of heat treatment or chemicals used at subsequent steps on previously fabricated layers. Therefore, a good understanding of all processes employed in the fabrication is necessary.

In this chapter, being the main process of the self-assembly-based fabrication technique, theory of Electroplating will be introduced initially. Then, fabrication sequence for the electrostatically actuated nanotweezers will be explained in detail, using schematic illustrations, in terms of six main steps as:

- Etching of the Crack Initiation Patterns,
- Fabrication of Nanowires,
- Preparation of a Layer for Integration,
- Fabrication of Devices,
- Cutting of Nanowire Ends,
- Release.

4.2. Electroplating Basics

A typical metal electroplating bath is illustrated in Figure 4.1.

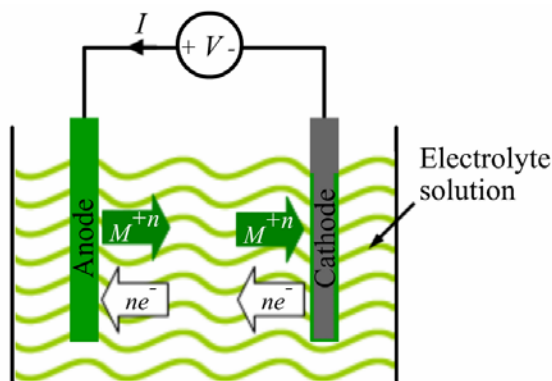


Figure 4.1 Schematic illustration of a metal electroplating bath

Anode is a pure metal electrode, where cathode is a conductive substrate, on which a complementary surface of the anode metal forms due to the application of a positive voltage to the anode. Both anode and cathode are dipped into an aqueous electrolyte solution, through which an electric current is carried due to the motion of metal ions from the anode. Following equation occurs as a result of the voltage difference between two electrodes [56]:



where, M is the anode metal and n is the number of electrons involved in the reaction.

Reaction from right to left is an oxidation reaction, which occurs at the anode, resulting in a loss of electrons and reaction from left to right is a reduction reaction, which occurs at the cathode resulting in a gain of electrons.

Faraday's law states that, the amount of electrochemical reaction that occurs at an electrode is proportional to the quantity of electric charge, Q , passed through an electrochemical cell. Hence, weight of an electrolysis product w_d can be determined as:

$$w_d = ZQ \quad (4.2)$$

In the above equation, Z is the electrochemical equivalent or the constant of proportionality and Q can be written in terms of current in Amperes, I , and elapsed time in seconds, t_e , as $Q = It_e$.

According to Faraday's law, charge required for production of one gram equivalent of a product at the electrode can be calculated using:

$$F = N_A e \quad (4.3)$$

where, N_A is Avogadro's number ($6.0225 \times 10^{23} \text{ mol}^{-1}$), e is the charge of a single electron ($1.6021 \times 10^{-19} \text{ C}$) and F is called the Faraday's constant, which is equal to $96,487 \text{ C mol}^{-1}$.

Fraction of a molar (atomic) unit of reaction that corresponds to the transport of one electron is denoted with w_{eq} , which can be calculated in terms of atomic weight of the deposited metal, A_{wt} , and number of electrons involved in the deposition reaction, n , as:

$$w_{eq} = \frac{A_{wt}}{n} \quad (4.4)$$

Since the electrochemical equivalent, Z , is the weight in grams produced or consumed by one Coulomb (one Ampere second):

$$Z = \frac{w_{eq}}{F} \quad (4.5)$$

Finally, substituting Equations 4.4 and 4.5 into Equation 4.2:

$$w_d = \frac{A_{wt}}{nF} It_e \quad (4.6)$$

Hence, deposit thickness can be evaluated in terms of volume of the deposit, V , as:

$$h_d = \frac{V_d}{a} = \frac{w_d}{a\rho_d} \quad (4.7)$$

where, a is the plated surface area and ρ is the density of the deposit.

Hence, given the current density, $J = I/a$, time required to obtain the desired deposit thickness, t_d , can be calculated by substituting Equation 4.7 into 4.6 and rearranging as follows:

$$t_d = \frac{nF\rho_d h_d}{JA_{wt}} \quad (4.8)$$

Electrode reaction for Ni electroplating is:



Applying Faraday's law to Ni electroplating, time in seconds corresponding to a desired deposit thickness of h in μm 's, can be calculated in terms of current density of J in A/dm^2 as:

$$t_d = \frac{(2)(96,487 \text{ C mol}^{-1})(8.907 \text{ g cm}^{-3})}{(58.69 \text{ g mol}^{-1})} \frac{h_d}{J} = (2.93 \times 10^{-4}) \frac{h_d}{J} \quad (4.10)$$

Note that above derivations are for ideal deposit conditions and effect of various electroplating conditions, such as anode or cathode efficiencies, should also be considered in determination of the required deposition time.

It can be inferred from Equation 4.9 that deposit thickness is directly proportional to current density. A uniform current density is essential in order to achieve a uniform deposition over the area to be plated.

Further information on Ni electroplating can be found elsewhere [57, 58].

4.3. Detailed Fabrication Sequence

4.3.1. Etching of the Crack Initiation Patterns

First step in the fabrication process for the electrostatically actuated nanotweezers is etching of crack initiation patterns into a silicon substrate, which is composed of lithography and DRIE sub steps. A low-resistivity (i.e. $< 0.0025 \Omega \text{ cm}$) (100) silicon wafer with 500-550 μm -thickness and 4-inch diameter is chosen for this purpose, due to the fact that, decreasing the resistivity of the substrate improves the adhesion of Ni ions on its surface and eliminates the need for using a seed layer during the electroplating of nanowires.

Before processing, native oxide on the wafer is removed by wet etching in BHF for 30 seconds in order to enhance the adhesion of the photoresist on the substrate during

lithography (Figure 4.2(a)). Front side of the wafer is spin coated by a $1.5\ \mu\text{m}$ -thick layer of AZ 5214 E resist, which is then baked at 90°C for 60 seconds (Figure 4.2(b)). Before being exposed, the wafer is left to absorb water vapor from air for about 15 minutes in order to enhance the exposure sensitivity. Then, it is exposed to UV light for 7 seconds using *Crack Initiation Mask* on a wafer scale contact aligner in hard contact mode (Figure 4.2(c)). Being the first mask of the fabrication process, this mask should only be aligned with respect to the wafer flat. Afterwards, exposed resist is developed in a 1:5 mixture of AZ 351 and deionized (DI) water at 20°C for 70 seconds (Figure 4.2(d)).

Crack initiation sites in the form of $6.5\ \mu\text{m}$ -deep grooves are etched into the Si substrate using a high-power DRIE recipe for 6 minutes (Figure 4.2(e)). Finally, remaining photoresist layer on the wafer surface is removed in Acetone for 5 minutes (Figure 4.2(f)) and the wafer is then rinsed in DI water for 2 minutes.

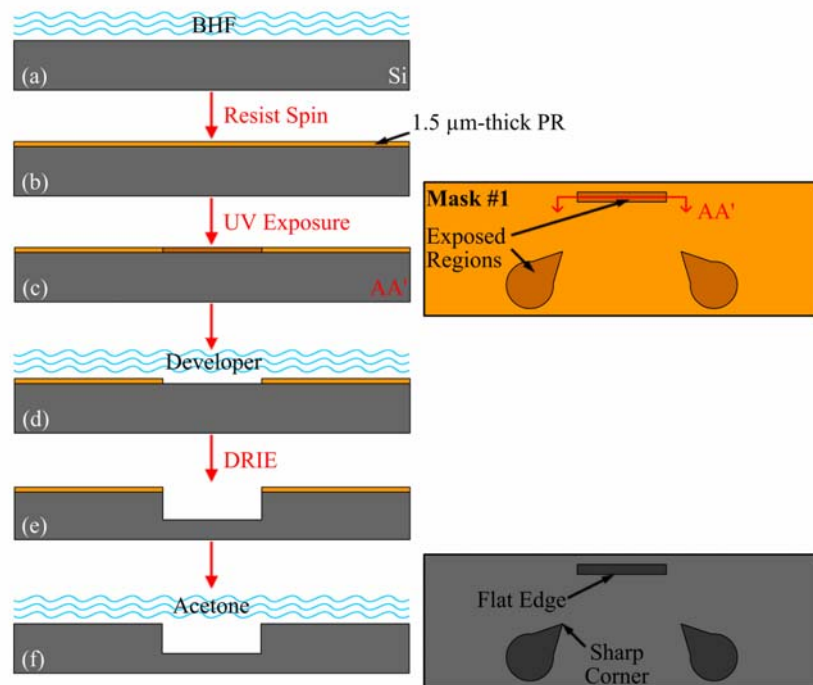


Figure 4.2 Process sequence for etching of crack initiation patterns into Si substrate

4.3.2. Fabrication of Nanowires

Most challenging step in the fabrication of electrostatically actuated nanotweezers is guided self-assembly-based fabrication of the nanowires, which is mainly composed of masking of the wafer surface via deposition of a sacrificial PECVD SiO₂ layer followed by a proper heat treatment and electroplating.

Initially, 4.6 μm-thick layer of sacrificial SiO₂ is deposited on the patterned wafer surface by means of a low temperature PECVD process (Figure 4.3(a)). After waiting for at least 24 hours after deposition, the wafer is annealed at 500 °C for 40 minutes and cracks initiate in the PECVD SiO₂ film, originating from sharp corners of the crack initiation patterns (Figure 4.3(b)). Since crack length is not sufficient after first annealing step, same heat treatment is repeated one more time, so that cracks propagate and terminate either at a matching crack or at a free surface.

In order to decrease the resistivity and enhance the electric field distribution over the wafer surface during electroplating step, a 10 nm/200 nm-thick Cr/Au layer is deposited on the wafer surface at the back by e-beam evaporation. This layer is then spin coated by a 2.2 μm-thick layer of AZ 5214 E photoresist in order to eliminate any Ni deposition on it (Figure 4.3(c)). An opening should be left on the resist close to wafer edge for electrical contact, either by sticking a small piece of blue tape during resist spin or by swapping off of the resist with Acetone afterwards.

Since width of the Si/SiO₂ interface area at the crack bottom is on the order of a few nanometers, cracks should be widened by wet etching in BHF for 30 seconds in order to obtain sufficient Si surface area for wire deposition on (Figure 4.3(d)). Note that, width of resulting nanowires is determined by the etch time at this step. In order to eliminate formation of any native oxide on the Si surface, either electroplating step should be carried immediately after BHF etch or the wafer should be dipped into a diluted acid bath for just a few seconds prior to nanowire deposition.

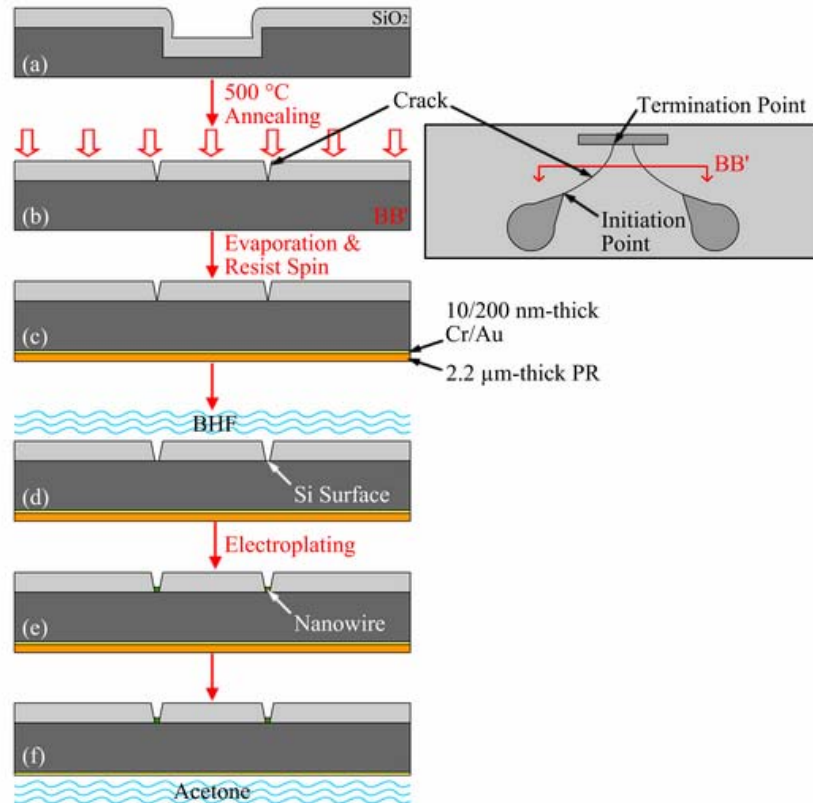


Figure 4.3 Process sequence for nanowire fabrication

Wafer is clamped to a single-contact wafer holder (Figure 4.4) at the location where resist opening is left in order to achieve electrical contact with the wafer through the Cr/Au layer at the back. After dipping the wafer into the electrolyte solution, wafer holder is electrically connected to the anode and current is gradually increased to 160 mA. Hence, Ni starts depositing on the wafer surface inside the crack molds forming Ni nanowires (Figure 4.3(e)). In order to enhance the uniformity over the wafer, electrolyte solution is circulated either by means of a magnetic stirrer or purging air using a pump during the process. After 35 seconds, which corresponds to a deposition thickness on the order of 500 nm, current is decreased to zero again gradually and wafer is taken out of the plating bath.

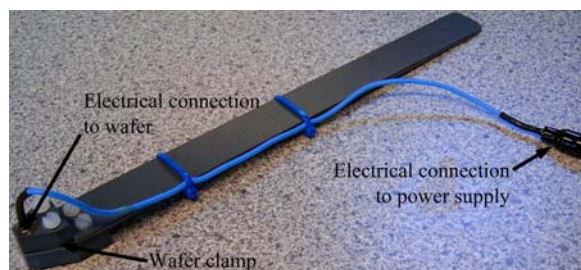


Figure 4.4 Single-contact wafer holder

Finally, the wafer is rinsed in DI water for 2 minutes, photoresist layer at the back is removed in Acetone for 5 minutes (Figure 4.3(f)) and rinsing step is repeated one more time.

4.3.3. Preparation of a Layer for Integration

Since the sacrificial SiO_2 layer is not electrically conductive, it is necessary to deposit a plating base prior to device electrodeposition. This layer also serves as a layer for integration between nanowires and device tips. For this reason, crack openings at the locations corresponding to the nanowire portions, which overlap with device tips, should be further widened by wet etching in BHF, for seed layer atoms to penetrate inside more easily reaching nanowire surfaces. However, remaining SiO_2 layer should be prevented from being etched completely by using a suitable photoresist mask.

As a first step, a hexamethyldisilazane (HMDS) (i.e. $[(\text{CH}_3)_3\text{Si}]_2\text{NH}$) heat treatment at 150°C should be performed on the wafer for $32\frac{1}{2}$ minutes, in order to enhance adhesion of the photoresist layer on the surface (Figure 4.5(a)). Then, a $1.5\ \mu\text{m}$ -thick layer of AZ 5214 E photoresist is spun on the wafer surface (Figure 4.5(b)) and it is baked at 90°C for 60 seconds. After waiting for 15 minutes for it to absorb water vapor from air, the wafer is exposed to UV light for 7 seconds using *Crack Widening Mask* in hard contact mode (Figure 4.15(c)). This mask is aligned with respect to the *Crack Initiation Mask*, which is the first mask of the fabrication process, with precision being not that critical. Afterwards, the

exposed resist layer is developed in a 1:5 mixture of AZ 351 and DI water at 20°C for 70 seconds (Figure 4.5(d)). Then, crack openings at the tip locations are widened by wet etching of the sacrificial SiO₂ layer in BHF for 3½ minutes (Figure 4.5(e)). Etch time at this step can be further increased in order to make sure that crack openings reach to a sufficient width.

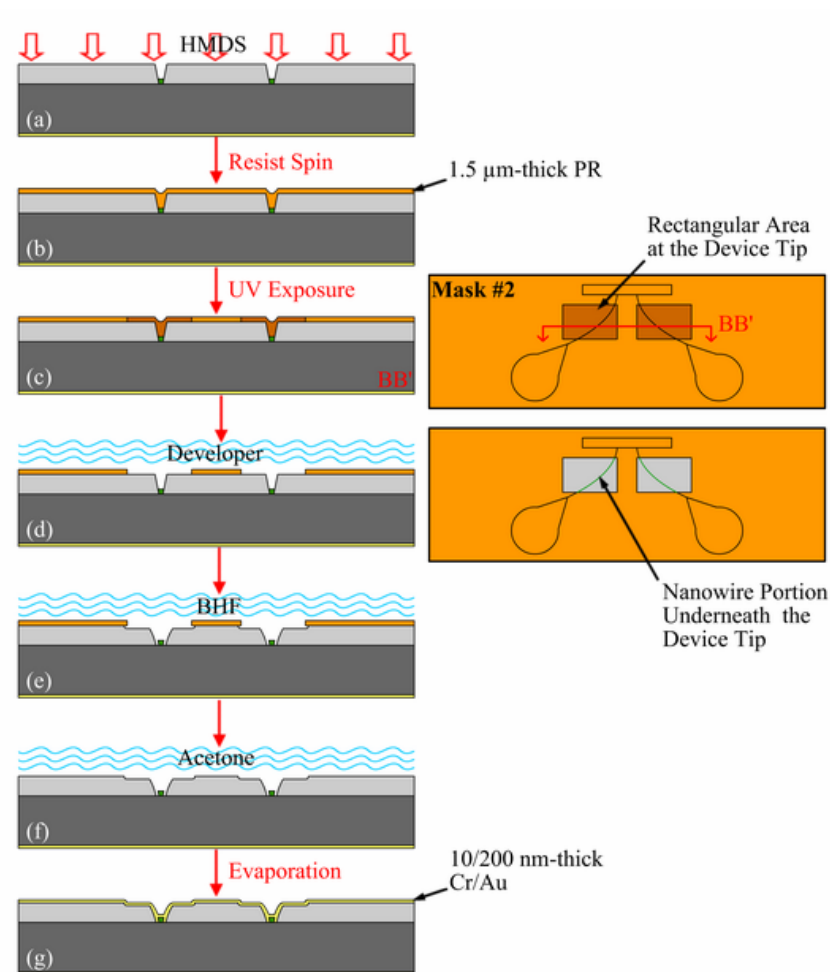


Figure 4.5 Process sequence for integration layer preparation

Following the removal of the photoresist mask in Acetone for 5 minutes and rinsing of the wafer in DI water for 2 minutes (Figure 4.5(f)), a 10 nm/200 nm Cr/Au layer is deposited on the front side of the wafer by e-beam evaporation (Figure 4.5(g)).

4.3.4. Fabrication of Devices

Device electroplating is the main step of the fabrication process, which is quite straightforward being composed of lithography and electroplating sub-steps.

Similar to all lithographic processes, an HMDS heat treatment at 150 °C is performed on the wafer for 32½ minutes, in order to enhance adhesion of the photoresist layer on the surface (Figure 4.6(a)).

Then, a 9.5 µm-thick layer of AZ4562 photoresist is spun on the wafer surface (Figure 4.6(b)) and the wafer is exposed to UV light for 50 seconds using *Electroplating Mask* in hard contact mode after waiting for about 15 minutes (Figure 4.6(c)). As the final step of the lithography sub step, the exposed resist layer is developed in a 1:5 mixture of AZ 351 and DI water at 20°C for 270 seconds (Figure 4.6(d)). In order for resulting devices to be functional, nanowire end-effectors should be precisely aligned with respect to device tips by perfect alignment of *Electroplating Mask* with respect to *Crack Initiation Mask*, which is the first mask of the fabrication process.

Prior to device electrodeposition, wafer is put into DI water for 3 minutes in order for softening of the photoresist mask by absorbing sufficient amount water. Rest of the procedure is similar to the case in “Nanowire Fabrication” step: Wafer is clamped to a three-contact wafer holder (Figure 4.7) and electrical connection with the Cr/Au plating base is achieved from resist opening locations defined by *Electroplating Mask*.

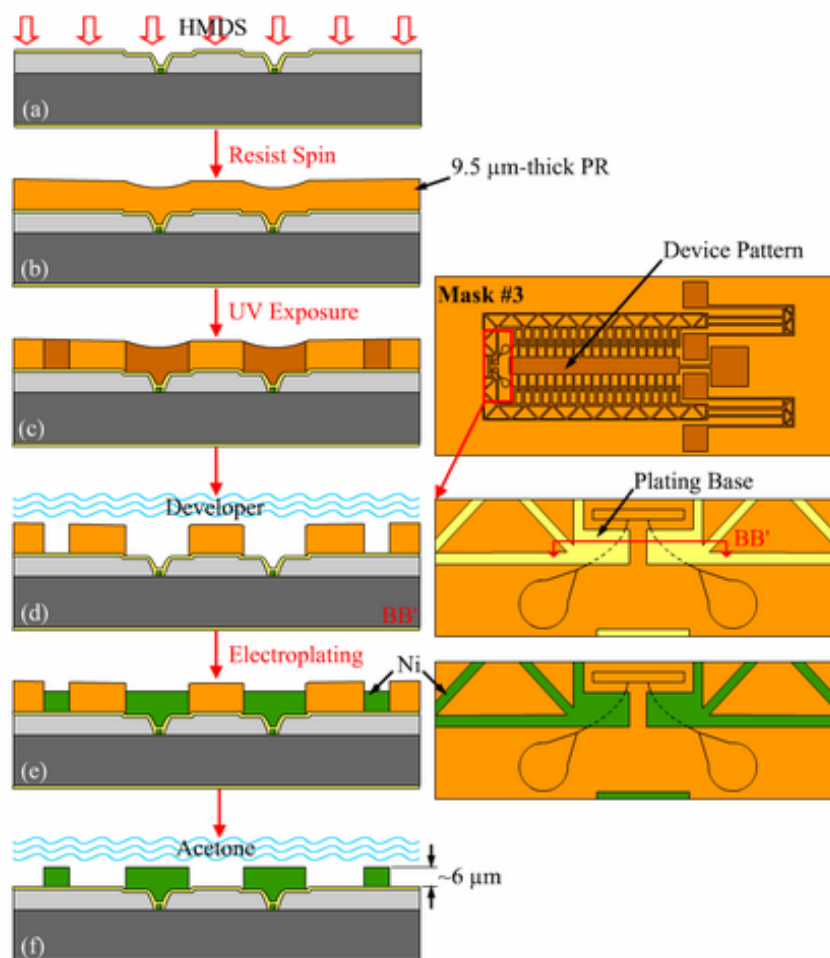


Figure 4.6 Process sequence for device fabrication

After dipping the wafer into the electrolyte solution, wafer holder is electrically connected to the anode and current is gradually increased to 250 mA. Ni deposition starts taking place on Cr/Au seed layer inside the photoresist mold, forming device structures (Figure 4.6(e)). Electrolyte solution is circulated either by means of a magnetic stirrer or purging air using a pump during the process. Uniformity at the edges can further be enhanced by using a current thief, in other words, connecting a dummy electrode in the form of a ring surrounding the wafer to a secondary cathode. After 30 minutes, which correspond to a

deposition thickness of 6 μm , current is decreased to zero again gradually and wafer is taken out of the plating bath.

Finally, the wafer is rinsed in DI water for 2 minutes, 9.5 μm -thick photoresist layer in front is removed in Acetone for 5 minutes (Figure 4.6(f)) and rinsing step is repeated one more time.

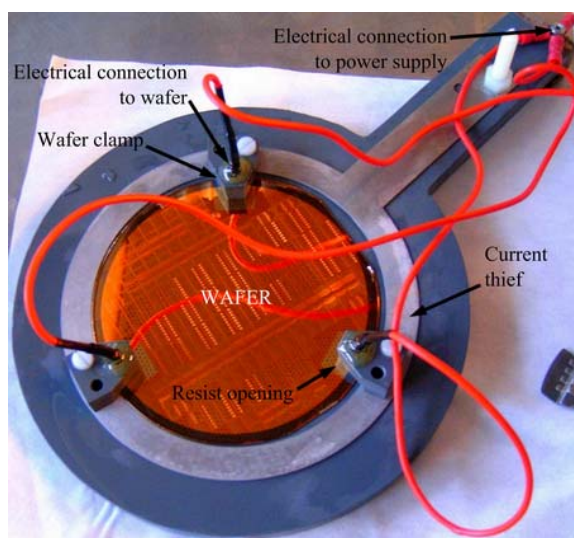


Figure 4.7 Three-contact wafer holder

4.3.5. Cutting of Nanowire Ends

Prior to lithography sub step to be performed for determining areas to be exposed to Ni etchant, Cr/Au seed layer covering all over the wafer surface, including both the sacrificial SiO_2 layer and nanowire surfaces, should be removed. For this purpose, 200 nm-thick Au layer is removed in Entreat for 18 minutes (Figure 4.8(a)) and the wafer is rinsed in DI water for 5 minutes. The reason for choosing Entreat is that, it does not attack Ni, however it is highly toxic.

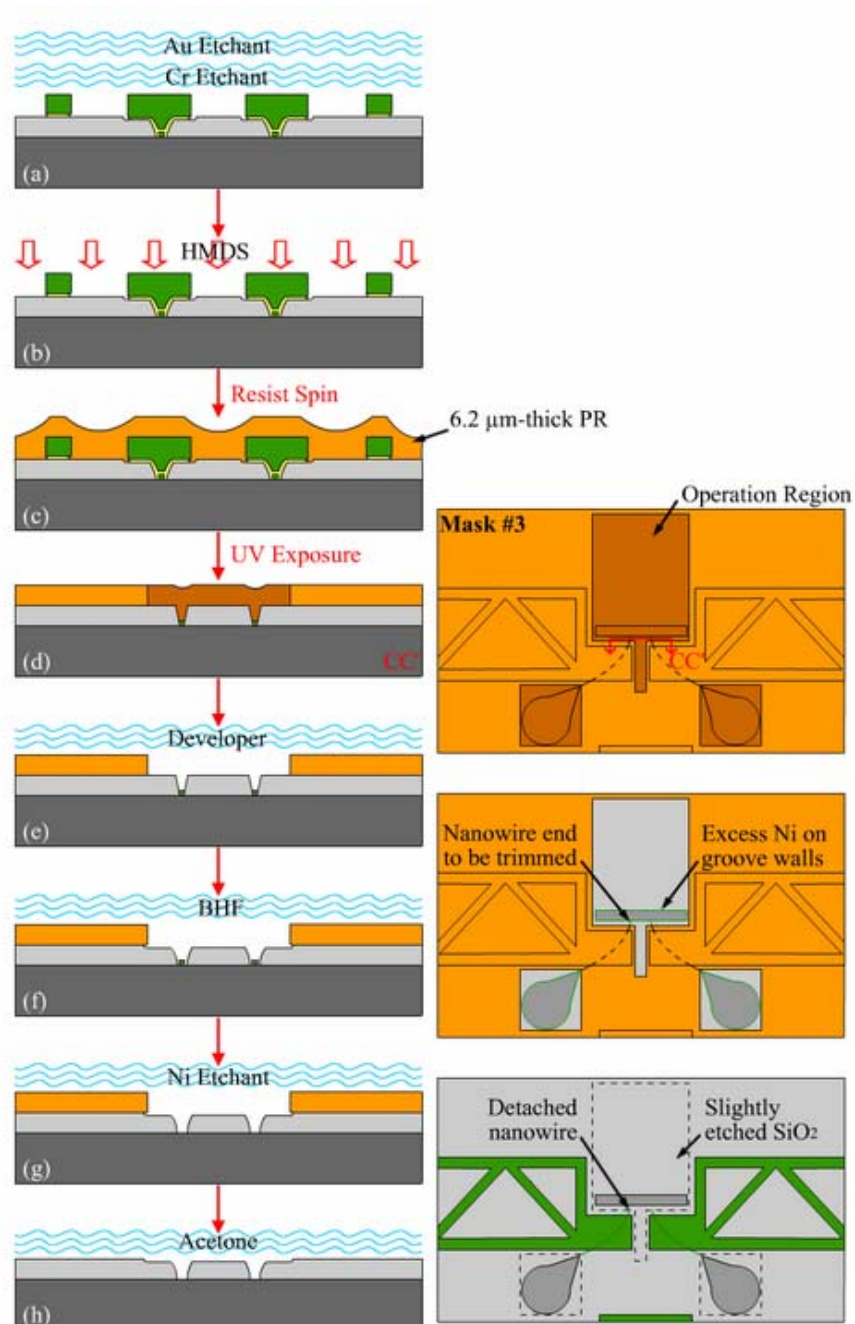


Figure 4.8 Process sequence for cutting nanowire ends

Then, 10 nm-thick Cr layer is removed in a commercial Cr etchant for 40 seconds in a similar manner. Note that, Cr etchant also attacks Ni with a relatively low etch rate but Ni structures are not damaged since etch time is too short. Over etch should be prevented in both Au and Cr etch steps for both nanowires to remain attached to device tips and devices to remain anchored on the substrate.

Being the first step of all lithographic processes except the first one, an HMDS heat treatment at 150 °C is performed on the wafer for 32½ minutes, in order to enhance adhesion of the photoresist layer on the surface (Figure 4.8(b)).

Mask for Ni etching should be thick enough in order to make sure that Ni structures will not be damaged. For this purpose, a 6.2 µm-thick layer of AZ4562 photoresist is spun on the wafer surface (Figure 4.8(c)) and the wafer is exposed to UV light for 35 seconds using *Wire Cutting Mask* in hard contact mode after waiting for about 15 minutes (Figure 4.8(d)). In order not to damage device tips and prevent nanowire-end effectors from completely being etched, this mask should be precisely aligned with respect to *Crack Initiation Mask*, which is the first mask of the fabrication process. Note that, alignment of Electroplating Mask, at the previous step is of crucial importance to achieve success in nanowire cutting process. Finally, the exposed resist layer is developed in a 1:5 mixture of AZ 351 and DI water at 20°C for 180 seconds (Figure 4.8(e)) and the mask is ready for Ni etch.

In order to make sure that Ni etchant reaches to nanowire surfaces at portions to be etched, cracks corresponding to these locations are further widened by wet etching the sacrificial SiO₂ layer in BHF for 3½ minutes (Figure 4.8(f)) and the wafer is rinsed in DI water for 5 minutes.

Afterwards, both Ni deposited on the walls of the crack initiation grooves and nanowire ends are etched in a 20% solution of nitric acid (HNO₃) for 6½ minutes (Figure 4.8(g)) and the wafer is rinsed in DI water for 2 minutes.

If dicing of individual chips is necessary depending on the application, this process should be carried out before the 6.2 µm-thick resist is removed, in order to eliminate any

possible damage on devices due to either vibration or Si particles formed by the saw during dicing. Rest of the process continues at chip level.

Finally, the 6.2 μm -thick photoresist layer in front is removed in Acetone for 5 minutes (Figure 4.8(h)) and rinsing step is repeated once again, devices are ready to be released.

4.3.6. Release

Last step in the fabrication of the electrostatically actuated nanotweezers is the release of the devices. For this purpose, sacrificial SiO_2 layer is completely removed by wet etching in BHF for 24 minutes (Figure 4.9(a)) and followed by 5 minute rinsing step.

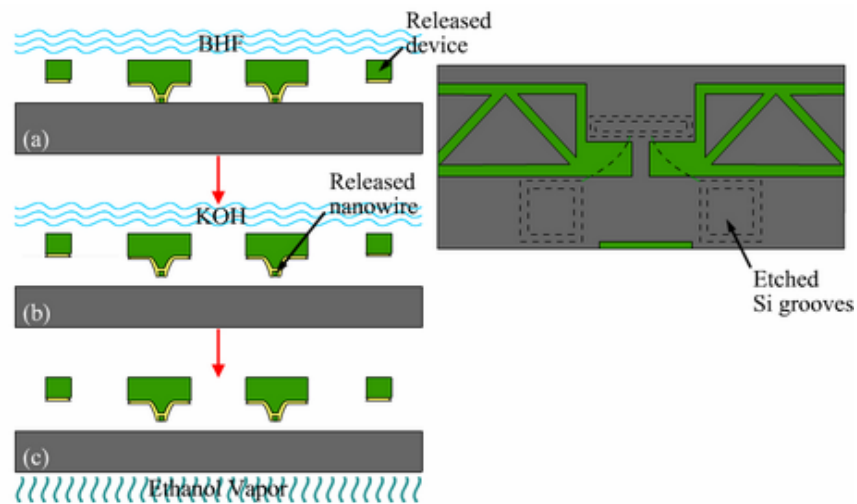


Figure 4.9 Process sequence for release

Although devices are completely released after removal of the sacrificial SiO_2 layer, nanowire end-effectors still lie on the substrate surface. For this purpose, Si surface underneath is etched in a 33 wt% KOH solution (750 grams of KOH and 1500 ml of DI water) at 60 $^{\circ}\text{C}$ so that nanowires are also released (Figure 4.9(b)). Note that, etch rate of the

35 wt% KOH solution is 0.54 $\mu\text{m}/\text{minute}$ at 60 $^{\circ}\text{C}$ and a 10 minutes etch time is sufficient for functional devices.

Note that, prevention of over etch is extremely important in etching of both BHF and KOH etching in order for devices to remain anchored on the substrate surface. However, under etching of the sacrificial SiO_2 layer should also be eliminated so that device tips are completely released.

In order to prevent sticking of the released devices on the substrate surface under the influence of capillary forces, which arise during the evaporation of water, devices should be dried in Ethanol vapor at 72 $^{\circ}\text{C}$ after being rinsed in DI water for 5 minutes (Figure 4.9(c)).

Chapter 5

FABRICATION RESULTS AND PROCESS OPTIMIZATION

5.1. Introduction:

As mentioned before, proposed fabrication technique is a novel approach, which enables integration of nano-scale end effectors to a microelectronic actuation mechanism. It requires modification of conventional PECVD process for depositing a sacrificial SiO₂ layer with special chemistry and well optimization of RIE parameters for obtaining crack initiation sites with sharper corners in order to enhance process yield.

Furthermore, although effective plating area for device deposition is well defined by a photoresist mold, effective plating area for nanowire deposition is not exactly known. For this reason, parameters to be used in nanowire deposition should be optimized separately in order to obtain nano-scale end-effectors with desired size and quality.

In this chapter, experimental procedure followed in determination of a PECVD process recipe for the sacrificial SiO₂ layer to be used as a mold in self assembly-based fabrication of the nanowire end effectors will be explained in detail. Then, results of two fabrication batches performed will be given for all of the six main steps, followed by proper optimization of process parameters where necessary.

5.2. Determination of a PECVD Recipe for Sacrificial SiO₂ Layer

5.2.1. Introduction and Motivation

Thin films are of prime importance in microelectronics and micro-electro-mechanical systems (MEMS) due to their wide variety of applications in optical, electrical, and mechanical fields. Depending on the material type, thin films serve the purposes of surface passivation or electrical isolation/connection. Furthermore, they can be used as a structural layer in MEMS devices or as a sacrificial or a mask layer for micro/nanofabrication processes such as electroplating, etching or doping. Some applications include optical coatings [59] and MEMS devices such as micromotors [60] or gyroscopes [61].

There are two main approaches for thin film deposition processes. On one hand, there exist processes such as chemical vapor deposition (CVD), electrodeposition, epitaxy and thermal oxidation, where depositions result from a chemical reaction. On the other hand, are processes such as physical vapor deposition (PVD) and casting, where the deposited material is physically moved on to the substrate. Among these, plasma-enhanced chemical vapor deposition (PECVD) is a special CVD technique, which utilizes an RF-induced plasma in the transfer of energy into the reactant gases, allowing the substrate to remain at lower temperatures than in other CVD processes [58].

PECVD is generally preferred due to the possibility of controlling the chemistry, hence mechanical properties, of the resulting film by changing process parameters. As an example residual stresses in a thin film, either compressive or tensile, are highly process-dependent. Furthermore, formation of residual stresses due to thermal loading conditions is the major concern for proper operation and reliability of MEMS structures.

SiO₂ thin film used in the fabrication of the electrostatically actuated nanotweezers serve the purpose of a sacrificial layer for the guided self-assembly-based fabrication of nanowire end-effectors, using the approach proposed in [50].

Note that, chemistry of the sacrificial SiO₂ layer is of prime importance in order to obtain the cracks by means of a proper heat treatment, which serve as molds for nanowire fabrication. Therefore, PECVD process recipe to be used should be well optimized by investigating effects of deposition parameters on both fracture mechanics and stress behavior of the SiO₂ films due to cyclic annealing, initially. For this purpose, a similar procedure as in [62] and [63] is followed and various SiO₂ films are deposited on standard Si wafers using different deposition parameters. Then, initial residual stresses in the resulting films are determined utilizing *substrate curvature method*. The method simply relies on Stoney formula [64], which relates the average film stress to the substrate curvature assuming that the film is much thinner than the underlying substrate. Then, films are exposed to a series of heat treatment steps, repeating the stress measurements after each annealing step.

5.2.2. Experimental Method and Initial Measurements

Experiments were performed on wafers which are similar to those used in nanowire fabrication and SiO₂ films were deposited on low-resistivity, 500 μm-thick 4 inch (100) silicon wafers, which were RCA cleaned. Radius of curvature measurements were performed on all wafers using Tencor P-1 stylus, storing data in a PC connected to the measurement unit for each of them separately, in order to calculate stress states of deposited films. Then, various depositions were performed with different process parameters using PECVD unit of PECVD part of STS Cluster System, which operates at 13.56 MHz.

Mainly three recipes are investigated:

- First recipe is a modified version of the one proposed in [49] varying only in that helium flow is eliminated due to its unavailability in the PECVD chamber. This recipe is studied thoroughly by changing deposition pressure and deposition power at temperatures both above and below the temperature suggested by the article (i.e. 200 °C and 300 °C), which is 250 °C.
- Second recipe is a recipe based on flow rates proposed in [63] using maximum gas flow rates available in the system, with 300 °C deposition temperature instead of 400 °C. Also power is maximized and pressure is minimized since they are not supplied in the article. This recipe is not studied as much as the first one due to time limitations.
- Third recipe is the standard recipe used in calibration of the PECVD system.

Radius of curvature measurements were performed on the wafers using Tencor P-1 stylus initially and following each deposition, thickness and refractive index values of the resulting SiO₂ layers were measured using a Prism Coupler and deposition rates of all recipes were calculated simply by the ratio of film thickness to deposition time. Secondary radius of curvature measurements were performed on the wafers and initial stresses in the SiO₂ films, σ_f , were determined using Stoney formula as:

$$\sigma_f = \frac{E_s h_s^2}{6(1-\nu_s) h_f} \left(\frac{1}{R_2} - \frac{1}{R_1} \right) \quad (5.1)$$

In the above equation, E_s and ν_s are Young's modulus and Poison's ratio values for the substrate, h_s and h_f are thicknesses of substrate and film, and $1/R_1$ and $1/R_2$ are initial and final radii of curvature, respectively.

Process parameters and initial measurement results are presented in Table 5.1, together with calculated deposition rates:

Recipe		Temp (°C)	Press (mT)	Power (W)	Gas Flow Rates (sccm)			Deposition Rate(Å/min)		Refractive Index	Initial Stress (MPa)
					SiH ₄	N ₂ O	N ₂	The	Act		
Recipe 1	LT	200	900	115	11.7	288	213	760	770	1.478	-24.9
	LT/LPre		300	115					1050	1.477	-17.8
	LT/HPw		900	350					1035	1.453	-50.1
	HT	300	900	115					1100	1.482	-52.5
	HT/LPre		300	115					980	1.493	-87.6
	HT/HPw		900	350					1260	1.462	-206.2
	HT/HPw+N ₂		900	350					853	1360	1.461
Recipe 2		300	700	30	950	950	1000	3800	1.466	-82.9	
Standard		400	380	17	1600	1600	1765	2000	1.463	-153.9	

Table 5.1 Deposition parameters for the recipes and initial measurement results

It was observed that, deposition rate is highly influenced by all deposition parameters. SiH₄ flow rate has the most significant effect and deposition rates for Recipe 2 and Standard Recipe are higher than those for all versions of Recipe 1 mainly due to increased SiH₄ flow rate.

It should be noted that, deposition conditions have a little influence on the refractive index value of the resulting SiO₂ film since all values measured vary in the range from 1.45 to 1.50, which is typical for stoichiometric oxide (Figure 5.1). However, it was observed that, refractive index increased with increasing deposition temperature and decreasing deposition pressure, whereas it decreased with increasing deposition power.

According to initial stress measurements, all films turned out to be in compression (Figure 5.2). It was observed that increasing deposition power and deposition temperature strongly enhanced compressive stresses in the resulting SiO_2 film, where decreasing pressure did not have that much influence on the initial stress state. Furthermore, increasing flow rate during deposition decreased initial compressive stresses considerably.

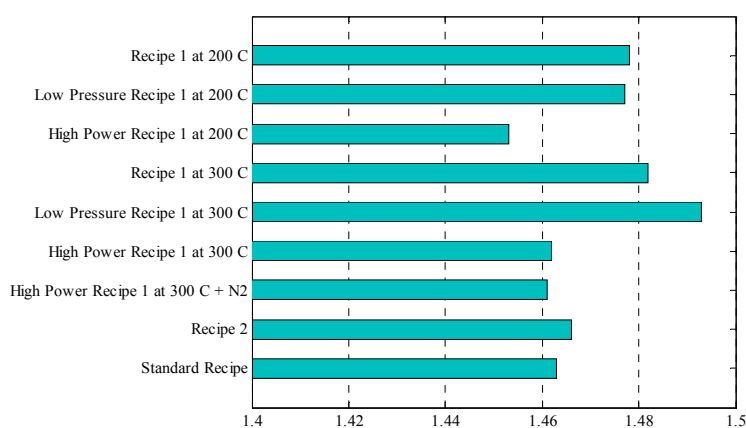


Figure 5.1 Refractive index values for the recipes

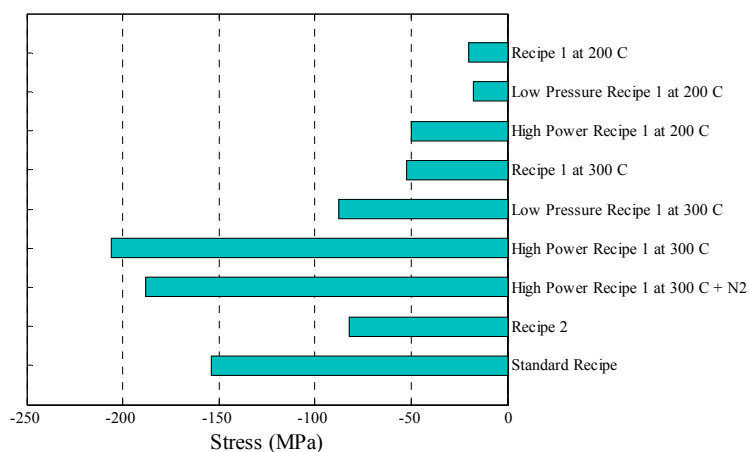


Figure 5.2 Initial stress state of the PECVD SiO_2 films

5.2.3. Thermal Cycling Experiments

In order to investigate behavior of PECVD SiO₂ films under cyclic annealing, heat treatments were performed at 500 °C for 40 minutes and stress measurements were carried out on the wafers after every annealing step, in a repeated manner.

Evolution of residual stresses in PECVD SiO₂ films deposited using different recipes at different temperatures under cyclic annealing is plotted in Figure 5.3. Since effects of heat treatment steps become insignificant after 3rd annealing step, only three cycles were carried out during the rest of the experiments.

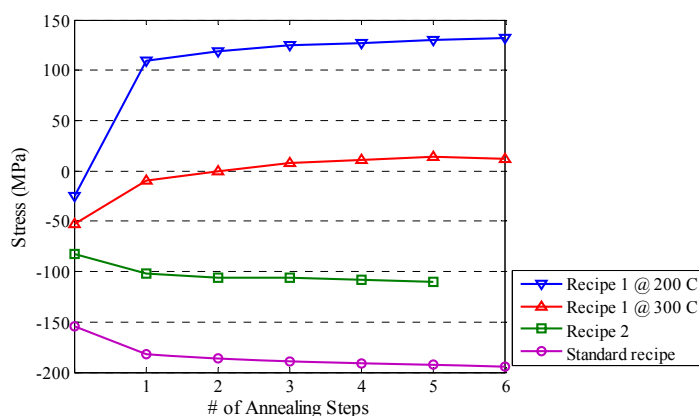


Figure 5.3 Stress behavior of SiO₂ films due to repeated annealing steps

Results for Recipe 1:

Initially, influence of deposition temperature is investigated on Recipe 1 by performing depositions at 200 °C and 300 °C, respectively. As tabulated in Table 5.1, both deposition rate and refractive index of the resulting film decreased when the deposition temperature was increased from 200 °C to 300 °C. Furthermore, initial stress state of both films turned

out to be compressive, with stress magnitude for the film deposited at 200 °C being less than that of the one deposited at 300 °C.

Annealing 4.5±0.1 μm-thick films deposited at both temperatures at 500 °C for 40 minutes for the first time, a considerable change was observed in the residual stress state of the film deposited at 200 °C, becoming tensile instead of compressive, with a gradient of about 140 MPa (Figure 5.4) per first cycle. However, stress state of the film deposited at 300 °C remained compressive, only with a 40 MPa reduction in the magnitude.

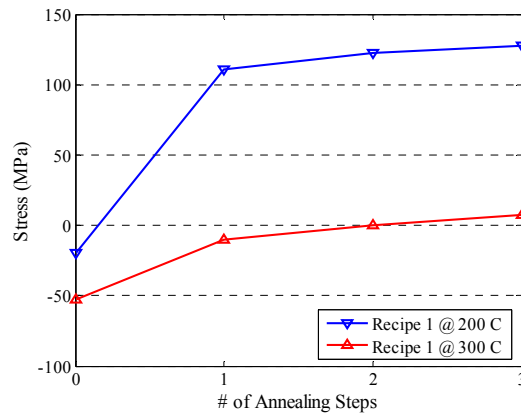


Figure 5.4 Effect of deposition temperature on Recipe 1

Effects of 2nd and 3rd annealing steps were similar for films, being on the order of 10 MPa and 5 MPa, respectively. It was observed that, the film deposited at 300 °C achieved almost a stress-free state, with a tensile stress of a negligible amount, after 2nd step. Further annealing made a little influence of the residual stresses of the films as stated above.

Secondly, influence of deposition pressure was investigated by decreasing it to 300 mT from 900 mT and performing depositions at both 200 °C and 300 °C. Referring to Table 5.1, it can be observed that decreasing deposition pressure considerably increased deposition rate for low temperature depositions, where the effect was the opposite for high

temperature depositions with change in the magnitude being one third of the previous case. It can be concluded that, deposition pressure does not have much influence on the refractive index for depositions performed at 200 °C, however values slightly increased for depositions performed at 300 °C.

Effect of deposition pressure on the magnitude of initial compressive stresses in the films was similar to that on refractive index values. Note that, low temperature films deposited at 200 °C were 3.7 μm and 4.9 μm -thick, respectively and the above mentioned difference between two cases might be due to this fact.

After 1st annealing step, magnitude of compressive stresses in both low temperature and high temperature cases increased by amounts of 140 MPa (Figure 5.5(a)) and 100 MPa, respectively (Figure 5.5(b)). Orders of change in the stress magnitude at 2nd and 3rd steps are more or less similar, their sign being opposite.

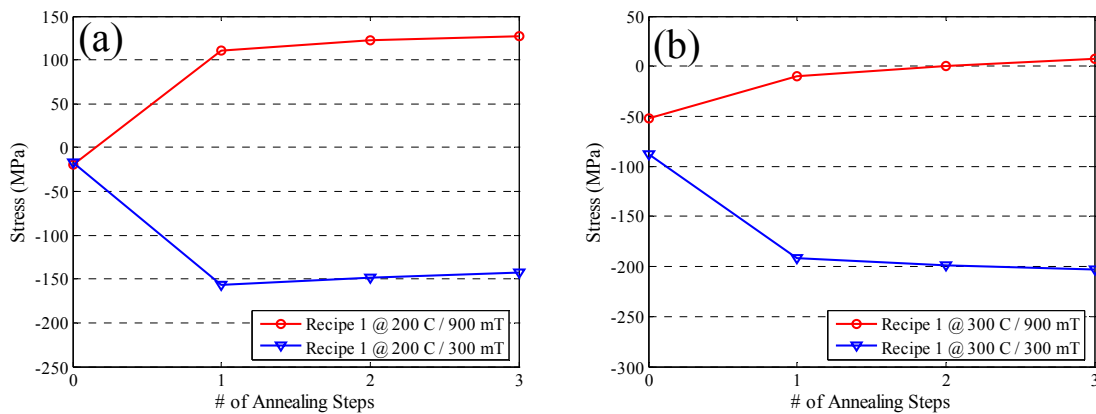


Figure 5.5 Effect of deposition pressure on Recipe 1 at (a) 200 °C and (b) at 300 °C

Effect of deposition power was investigated using the same procedure as for deposition pressure by increasing it to 350 W from 115 W and again performing depositions at both

200 °C and 300 °C. Note that, a deposition power of 115 W corresponds to 255 W/cm² for the resulting films.

Initial stress state was again compressive, but with a 20 MPa reduction in the magnitude. Influence of 1st annealing step was the same except that reduction in compressive stresses is about 85 MPa, being less than the case with a lower N₂ flow rate (Figure 5.6). Behaviors of both films due to further annealing were similar.

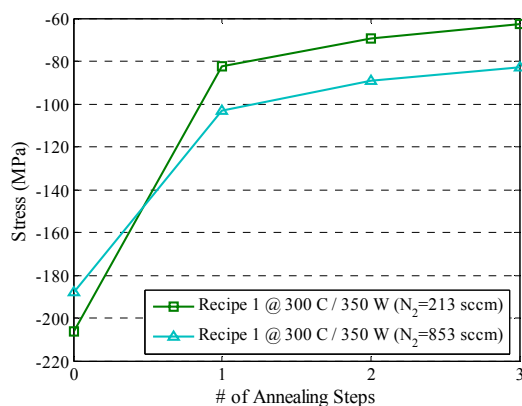


Figure 5.6 Effect of deposition temperature on Recipe 1

A small difference was observed between magnitudes of initial compressive stresses of PECVD SiO₂ films deposited at 200 °C and 300 °C. As stated above, this might be due to fact that the thicknesses of the compared films were not the same. For this purpose, effect of film thickness on Recipe 1 is investigated by performing cyclic annealing experiments on films of various thicknesses, deposited using same deposition parameters.

Both magnitudes of initial compressive stresses and behaviors of 2.7 μm and 4.6 μm-thick films deposited using Recipe 1 at 200 °C turned out to be similar due to repeated heat treatment steps (Figure 5.8(a)). However, when 3.7 μm and 4.6 μm-thick films deposited using Recipe 1 at 300 °C are considered, although their behavior upon cyclic annealing was

similar, it was observed that stress state of the thinner film was more compressive than that of the thicker one initially (Figure 5.7(b)).

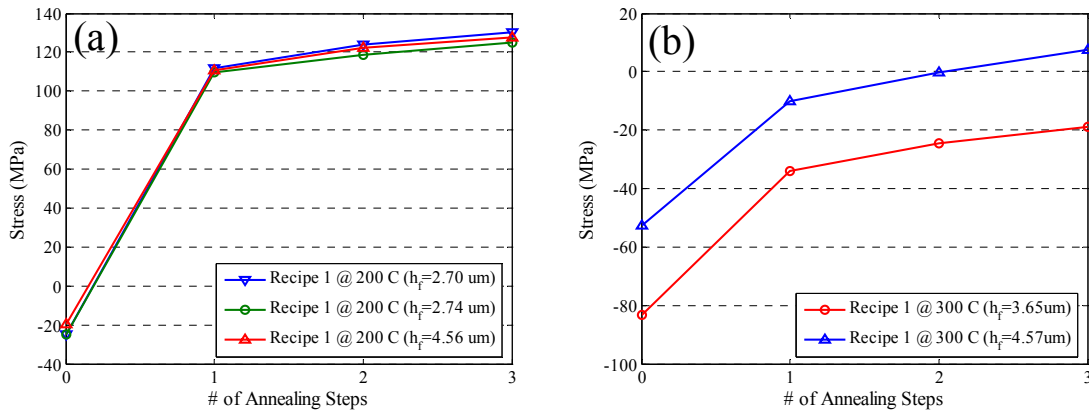


Figure 5.7 Effect of film thickness on Recipe 1 at (a) 200 °C and (b) at 300 °C

This explains previously observed differences in the initial stress states of films deposited at 300 °C from those deposited at 200 °C using same deposition parameters (i.e. Figures 4.5 and 4.6) relying on the fact that that thicknesses of compared films are not always the same since deposition rate was not known prior to deposition.

Finally, the effect of annealing time is investigated by performing three depositions using Recipe 1 at 300 °C, using exactly the same parameters and annealing the resulting films at different times: 1 day, 1 week and 1 month after deposition.

Although magnitudes of initial compressive stresses in both films were similar, reduction in the stress magnitude after 1st annealing was about 5 MPa less for the film annealed 1 week after deposition than that annealed just 1 day after (Figure 5.8). Furthermore, evolution of internal stresses due to repeated heat treatment turned out to be different for the two films.

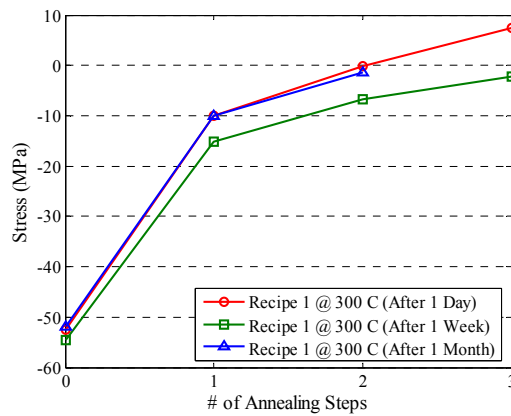


Figure 5.8 Effect of initial annealing time on Recipe 1 at 300 °C

However, a similar film annealed after 1 month showed almost the same behavior as the one annealed just 1 day after deposition due to both 1st and 2nd annealing steps.

Results for Recipe 2:

Deposition rate of Recipe 2 turned out to be the highest mainly due to maximized gas flow rate values. Refractive index values of films deposited using this recipe were all about 1.47 and initial stress state of these films were compressive with magnitudes about 82 MPa (Figure 5.3).

Due to time limitations during the study, only effect of film thickness on Recipe 2 at 300 °C was investigated, by comparing both magnitude of initial compressive stresses and evolution of internal stresses due to cyclic annealing in two PECVD SiO₂ films with 3.8 μm and 4.9 μm thicknesses.

Magnitude of initial compressive stresses in the thicker film turned out to be slightly larger than that in the thinner one (Figure 5.9). After 1st annealing step, compressive stresses in 4.9 μm-thick film increased by an amount of 15 MPa, where the increase was about 20 MPa for the 3.8 μm-thick one. The difference became more significant after 2nd

annealing step with values being 5 MPa and 10 MPa for thicker and thinner films, respectively.

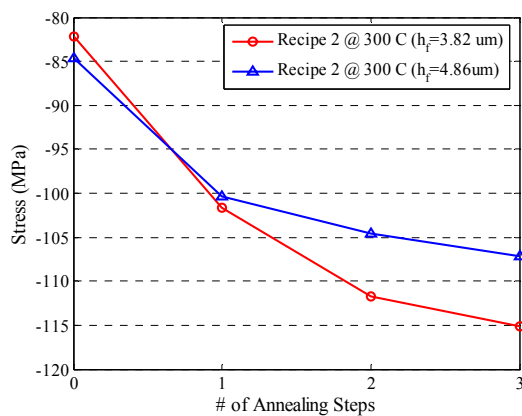


Figure 5.9 Effect of film thickness on Recipe 2 at 300 °C

Behavior of both films due to further annealing became similar after 3rd annealing step. This recipe can be further investigated in a similar manner with Recipe 1 in other studies.

Results for Standard Recipe:

Deposition rate and refractive index values of Standard Recipe were 2000 Å/min and 1.46, respectively. Similar to all films investigated above, initial stress state of PECVD SiO₂ films, which were deposited using Standard Recipe, turned out to be compressive with a magnitude of 150 MPa (Figure 5.3).

After 1st annealing step, compressive stresses in the film increased by an amount of 30 MPa and this increase continued also due to 2nd and 3rd annealing steps, with magnitudes about 5 MPa and 3 MPa, respectively. The behavior was similar to that of Recipe 2, differing only in the magnitude of initial compressive stresses, due to low deposition pressures used for both recipes.

5.2.4. Parameter Selection

In order for cracks to initiate in the sacrificial SiO₂ layer, internal stresses should be highly tensile, at least on the order of 100 MPa [49]. Hence, it can be inferred that, a 3-5 μm-thick PECVD SiO₂ film deposited on a pre-patterned wafer at 200 °C using Recipe 1 will probably yield cracking after either 1st or 2nd 40-minute heat treatment step performed at 500 °C. For this reason, process parameters to be used in deposition of the sacrificial SiO₂ layer were selected as follows:

Temp (°C)	Press (mT)	Pow (W)	Gas Flow Rates (sccm)			Deposition Rate (Å/min)	Deposition Time (min)
			SiH ₄	N ₂ O	N ₂		
200	900	115	11.7	288	213	760	60

Table 5.2 PECVD process parameters

5.3. Results and Process Optimization

5.3.1. Etching of the Crack Initiation Patterns

In order for process optimization to be done, two wafers were masked by 1.5 μm- and 2.2 μm-thick photoresist layers, initially. Note that, exposure time for both resists was 7 seconds, but development times were 70 seconds and 90 seconds for 1.5 μm and 2.2 μm thicknesses, respectively. Minimum feature size for both wafers turned out to be about 1 μm (Figure 5.10).

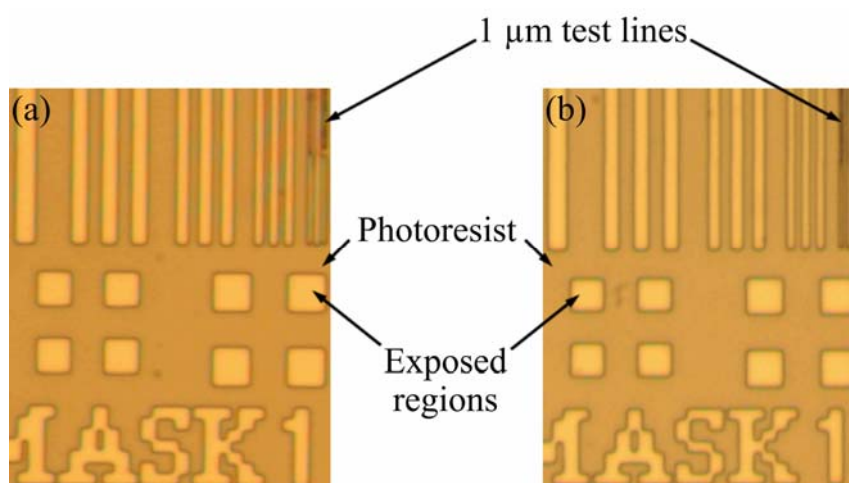


Figure 5.10 Positive lithography test lines for (a) 1.5 μm - and (b) 2.2 μm -thick photoresist films

Furthermore, sharpness of the crack initiation patterns seemed to be well sufficient before DRIE process (Figure 5.11(a)).

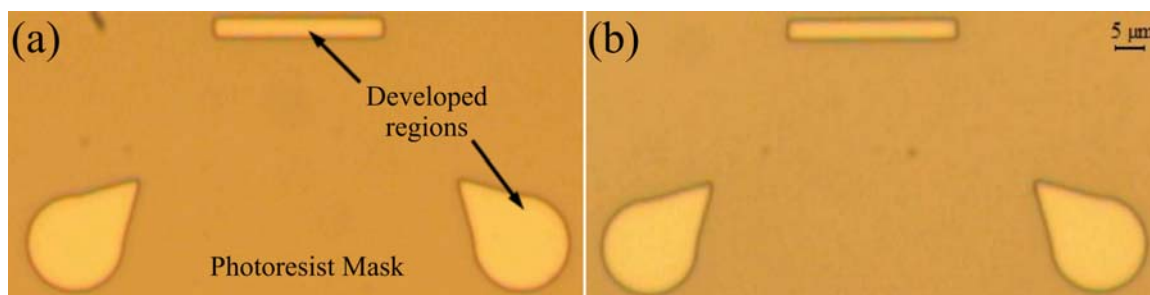


Figure 5.11 Comparison of crack initiation patterns on (a) 1.5 μm - and (b) 2.2 μm -thick photoresist masks

Initially, standard DRIE recipe was used for 22½ minutes in order to etch 10 μm -deep grooves into the Si substrate. At the end of the process, it was observed that 1.5 μm -thick photoresist was completely removed, where 2.2 μm -thick photoresist layer survived,

resulting in exactly 10 μm -deep grooves. However, corners of the crack initiation patterns were not sharp enough for crack initiation in future steps (Figure 5.12).

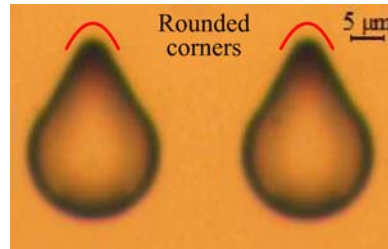


Figure 5.12 10 μm -deep crack initiation patterns etched using standard DRIE recipe

As a result, power of the standard DRIE process increased from 30 W to 60 W in order to enhance the anisotropy during etching. Also minimum resist thickness should be preferred since precision of the pattern transfer decreases with increasing thickness of the resist layer. However, photoresist mask to be used in the etching of crack initiation sites into the substrate should be thick enough to survive a high-power DRIE process due to increased etch rate. In order for process optimization, shallower grooves were etched using the high-power DRIE recipe for 6, 7 and 8 minutes with 1.5 μm -thick photoresist mask (Figure 5.13).

Note that, etch rate of the high-power DRIE recipe turned out to be 0.93 $\mu\text{m}/\text{min}$ and 6, 7 and 8 minute processes resulted in 5.5 μm , 6.5 μm and 7.5 μm deep-grooves, respectively. As can be observed from figures, sharpness of the corners decreases with increasing etch time. It can be concluded that optimum etch time is 6 minutes considering also the groove depth. Furthermore, color changes indicate reducing thickness of the photoresist film.

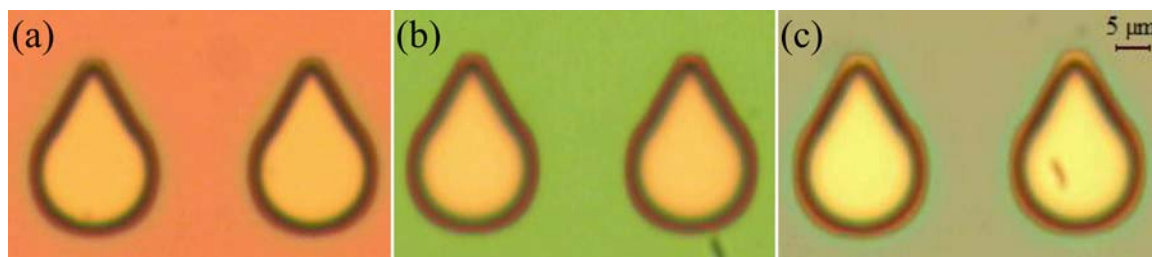


Figure 5.13 Crack initiation patterns etched using high-power DRIE recipe for (a) 6 minutes, (b) 7 minutes and (c) 8 minutes

5.3.2. Fabrication of Nanowires

Perhaps the most challenging step in the fabrication of electrostatically actuated nanotweezers is guided self-assembly-based fabrication of the nanowires, requiring proper optimization of process parameters at each step. It is composed of two sub-steps: (1) preparation of nano-scale molds in a sacrificial SiO_2 film by stress-assisted cracking and (2) deposition of nanowires into these molds by electroplating.

Preparation of Nanowire Molds:

Sacrificial SiO_2 layers were deposited by means of a 60-minute PECVD process with parameters given in Table 5.2, resulting in film thicknesses in the range from 4.5 μm to 4.7 μm . After waiting for 24 hours after deposition, wafers were annealed at 500°C for 40 minutes and cracks initiated in all sacrificial SiO_2 layers after this 1st annealing step. However, although the sacrificial SiO_2 layer started peeling-off at the wafer edge, crack length was not sufficient (Figure 5.14 (a)) and not many crack inducers yielded cracking yet. Furthermore, cracks also initiated unexpectedly from corners of rectangular grooves, which serve the purpose of a free surface for crack termination at some locations (Figure 5.14(b)).

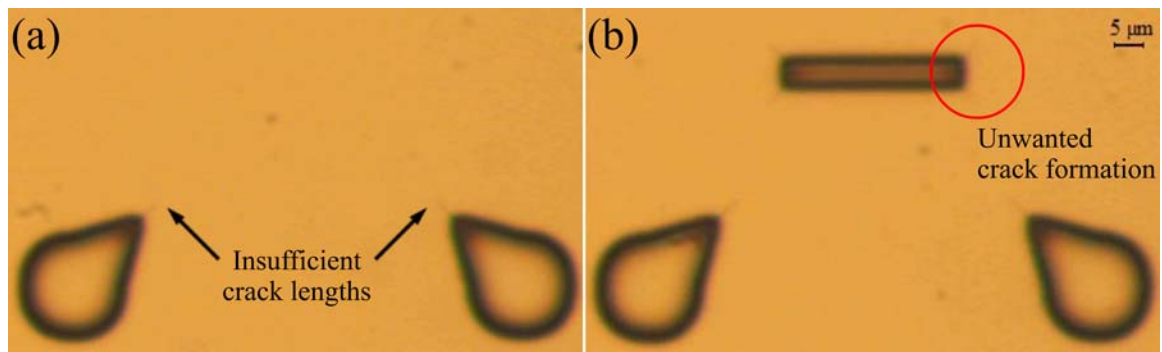


Figure 5.14 Crack initiation from sharp corners after 1st annealing step (a) with and (b) without the presence of a free surface

When the wafers were annealed under same conditions for a 2nd time, cracks propagated and reached to a desired length at most locations (Figure 5.15 (a)). However, although bent cracks were achieved and some cracks terminated at free surfaces, crack propagation was hindered by unwanted cracks at many locations (Figure 5.15(b)).

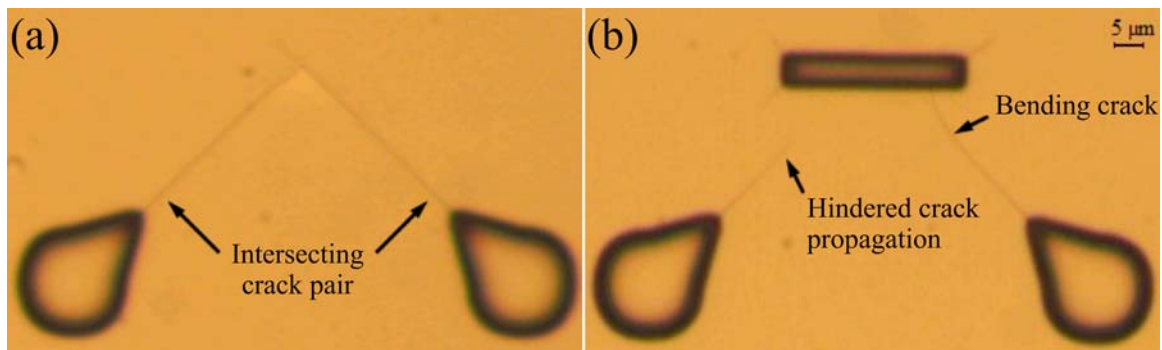


Figure 5.15 Crack propagation after 2nd annealing step (a) with and (b) without the presence of a free surface

Furthermore, it was observed that, although most crack inducers on the right side of the wafer yielded cracking, there was not any crack formation at some locations on the left side

of the wafer. This can be explained due to the fact that deposition gases are introduced from right in the PECVD chamber; hence chemistry of the SiO_2 film may be different on this side of the wafer as a result of more OH formation taking place in the presence of more reaction gases.

In order to find out whether, remaining inducers will yield cracking or not, a 3rd annealing process was carried out on one of the wafers. After this additional annealing step, it was observed that, crack propagation was drastically enhanced. However, resulting cracks were wider and delaminated cracks. Furthermore, they were propagating in a helical manner and were excessively long (Figure 5.16(a)). Also new cracks initiated at some locations previously yielded cracking (Figure 5.16(b)). However, there were still some cracks with desired length and some inducers, which did not yielded cracking yet.

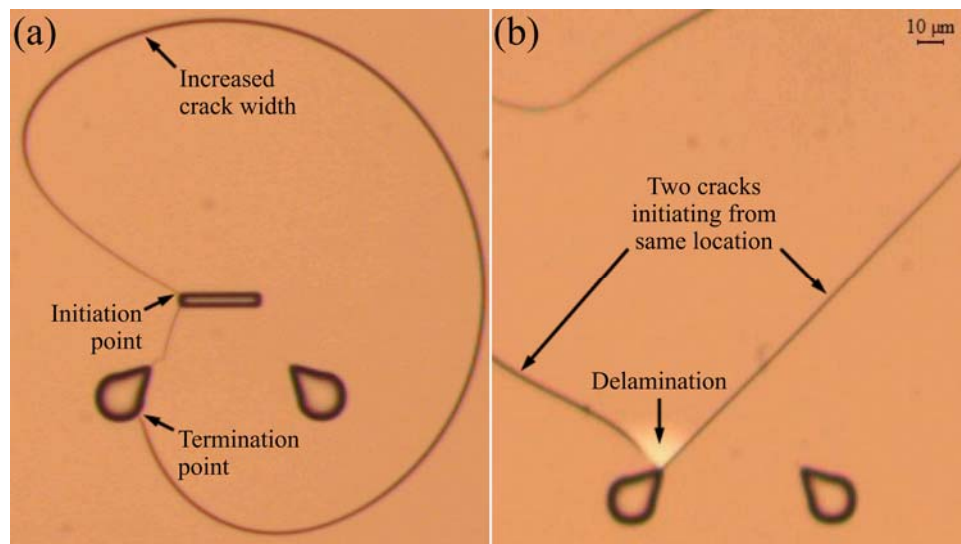


Figure 5.16 (a) Helical or (b) excessive and delaminated crack formation after 3rd annealing step

When, clamped-clamped and cantilever beam test structures are considered, neither of them resulted in desired cracking. There were a few triangular tips those yielded cracking after both 1st and 2nd annealing step. Furthermore, cracks were following a bent path rather than propagating in a straight manner (Figure 5.17(a)). Reason for this behavior might be the fact that crack propagation is more preferable along any $\langle 100 \rangle$ direction of the underlying Si substrate as proposed in [49]. Delaminated and excessive cracking was observed also in these test structures after 3rd annealing step (Figure 5.17(b)).

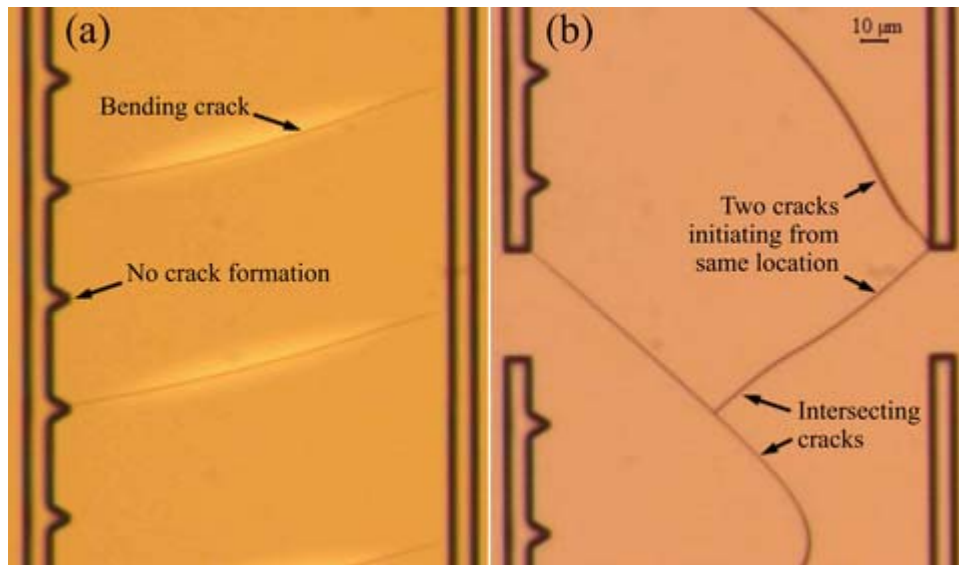


Figure 5.17 Test structures after (a) 2nd and (b) 3rd annealing steps

In order to eliminate both excessive cracking and peeling-off of the sacrificial SiO₂ layer at the wafer edge, annealing temperature was decreased to 400 °C. This eliminated peeling-off phenomenon as expected, however no crack formation occurred even after 4th annealing step. Increasing annealing time from 40 minutes to 60 minutes, again at 400 °C, did not make any difference and no cracks observed.

Deposition of Nanowires:

It is not possible to deposit a seed layer on wafer surface, which is masked by the sacrificial PECVD SiO₂ layer; hence deposition of Ni nanowires takes place directly on Si substrate. Instead, a 10 nm/200 nm Cr/Au layer was deposited on the wafer surface at the back in order to enhance the adhesion of nanowires to the substrate surface in front. This layer was then spin coated by a 1.5 μm-thick photoresist film for eliminating any Ni deposition on it. However, it was observed that thickness and uniformity of the photoresist layer was not sufficient for this purpose and some Ni deposition took place at the back during nanowire deposition. For this reason, thickness of the photoresist film spun at the back was decreased to 2.2 μm for second batch wafers, resulting in no Ni deposition at the back.

Side walls and bottom of crack initiation grooves are not fully covered by the sacrificial SiO₂ layer. Furthermore, both crack length and crack width vary at different locations on the wafer. Consequently, it is not possible to calculate effective plating area for nanowire deposition exactly and this directly influences both deposition rate and surface quality of the resulting nanowires.

In order to optimize both deposition current and deposition time, trial depositions on test samples were carried out initially. For this purpose, the wafer that became useless for further processing due to excessive cracking as a result of the 3rd annealing step performed was cleaved into four quarters. Then, four different depositions are performed on each quarter using 40 mA and 60 mA deposition currents for 1 minute and 2 minutes, respectively. Afterwards, sacrificial SiO₂ layers on all deposition samples were removed for investigation under scanning electron microscope (SEM). It was observed that, width of the resulting nanostructures were in the range 350 nm to 450 nm (Figure 5.18(a)).

2-minute depositions yielded “nano-sheets” rather than nanowires with an aspect ratio greater than 6, where 1-minute depositions yielded more reasonable structures with thicknesses on the order of 1 μm (Figure 5.18(b)).

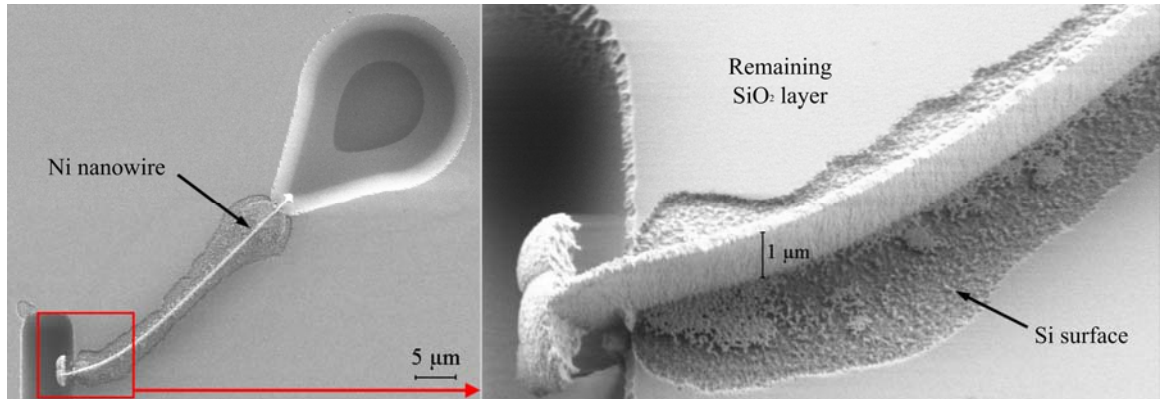


Figure 5.18 SEM images showing (a) a bent nanowire from top and (b) 45° tilted view of the nanowire end as a result of a 1-minute Ni deposition performed at 40 mA

Surface quality of nanostructures deposited at 40 mA and 60 mA were all similar. However, as previously mentioned, the wafer used in test depositions was excessively cracked with longer and delaminated cracks resulting in a larger effective plating area. For this reason, 40 mA was chosen instead of 60 mA per wafer quarter and nanowire depositions were performed at 160 mA for 35 seconds, for 500 nm to 600 nm-thick nanowires.

After release, it was observed that, thickness of nanowires vary in the range from 500 nm to 600 nm as expected. However, nanowire thickness exceeds 1 μm at some locations where excessive deposition occurred during device electroplating step, due to either misalignment of Mask #3 with respect to Mask #1 or air bubbles trapped between the photoresist mask and the sacrificial SiO₂ layer at crack openings.

Example SEM images of resulting nanowires will be presented in “Release” section.

5.3.3. Preparation of a Layer for Integration

Precision and alignment of the mask used in crack widening is not that critical since BHF etching of the sacrificial SiO_2 layer is an isotropic process, resulting in an undercut. However, photoresist mask should be thick enough to survive the wet etching process and a photoresist thickness of $1.5\ \mu\text{m}$ turned out to be well sufficient (Figure 5.19(a)).

Most important parameter to be optimized at this step is the time of BHF etch, which yields to a crack width that is sufficient for seed layer atoms to penetrate inside crack openings, reaching nanowire surfaces at locations overlapping with device tips.

BHF etch time for the first fabrication batch was $3\frac{1}{2}$ minutes, resulting in $1.5\ \mu\text{m}$ to $2\ \mu\text{m}$ -wide cracks. However, the difference between unwidened and widened crack portions was hardly visible. So, BHF etch time is increased to 5 minutes for the second fabrication batch, in order to make sure that crack openings are wide enough for the penetration of seed layer atoms to the inside. As a result, widened crack portions became well observable under optical microscope, being greater than $2.5\ \mu\text{m}$ (Figure 5.19(b)).

E-beam evaporation of a $10\ \text{nm}/200\ \text{nm}$ Cr/Au plating base was a straightforward process, which does not need any optimization.

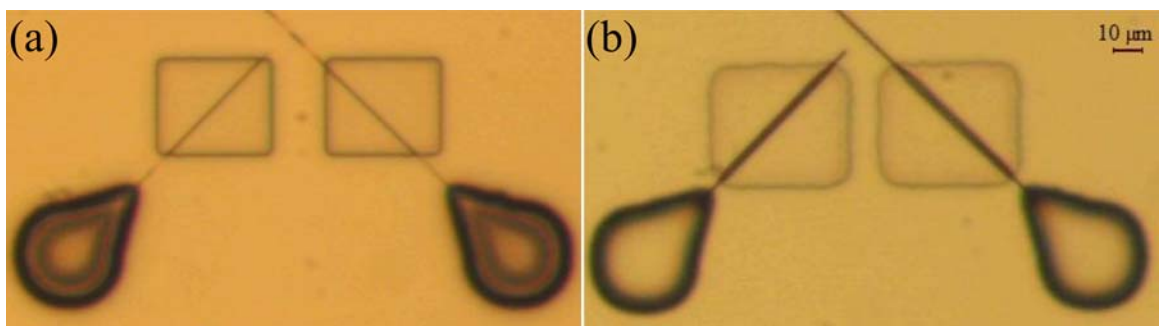


Figure 5.19 Optical microscope image of (a) a crack pair with Mask #2 on and (b) a similar crack pair after a 5-minute BHF etch and removal of Mask #2

5.3.4. Fabrication of Devices

Photoresist layer to be used as a mold for device electrodeposition should be thick enough to avoid over deposition and mushroom shaped devices. However, both resolution and accuracy of the lithography step decreases with increasing photoresist thickness, resulting in larger or smaller dimensions and rounded edges. Best resolution achieved at this lithography step was about 2 μm for both positive (Figure 5.20(a)) and negative patterns (Figure 5.20(b)).

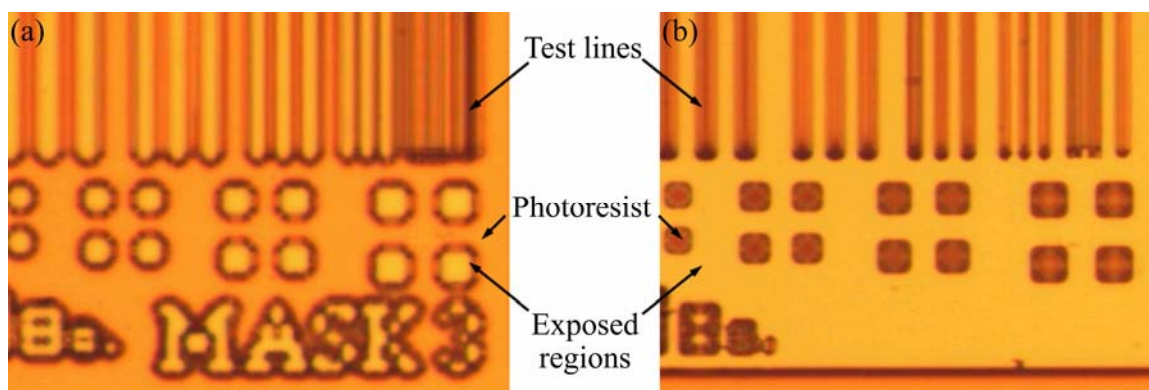


Figure 5.20 (a) Positive and (b) negative lithography test lines for 9.5 μm -thick photoresist

In wafers fabricated during first batch, there was a considerable misalignment between Electroplating Mask and Crack Initiation Mask, which resulted in just “Microgrippers” rather than “Nanotweezers” due to disorientation of nano-scale end-effectors with respect to device tips (Figure 5.21(a)). However, misalignment effect is eliminated for some devices, which point to the opposite direction (Figure 5.21(b)).

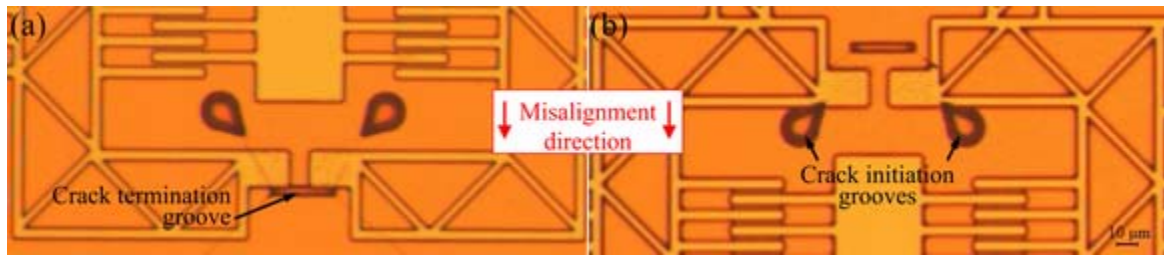


Figure 5.21 Misalignment between Mask #1 and Mask #3 at device tips pointing to a direction (a) same as and (b) opposite to the direction of misalignment

This problem is solved for second batch wafers by taking the advantage of advanced features of the mask aligner such as precision contact and using fine alignment buttons with a step size factor of $1.25\ \mu\text{m}$ instead of the joystick for control. Furthermore, separation distance between substrate and mask during alignment is decreased to $35\ \mu\text{m}$ from $50\ \mu\text{m}$ and almost perfect alignment is achieved.

As a result of issues related with both resolution and precision of the lithography step, actual dimensions and shapes turned out to be different than those designed. There is also a variation between individual chips at different locations within the wafer.

Dimensions of most electrostatically actuated nanotweezers were reasonable, being slightly greater than those designed. Considering a 3-comb single anchored device as an example (Figure 5.22(a)), thickness of comb fingers, which were designed as $5\ \mu\text{m}$, came out to be $6.5\ \mu\text{m}$ resulting in a lateral gap of $2.5\ \mu\text{m}$ instead of $4\ \mu\text{m}$ (Figure 5.22(b)). Similarly, this enlargement of dimensions also yielded in a longitudinal gap of $27.7\ \mu\text{m}$ rather than $30\ \mu\text{m}$. Thickness of the double-folded cantilever flexures for the same device turned out to be $5\ \mu\text{m}$ instead of $4\ \mu\text{m}$ (Figure 5.22(c)).

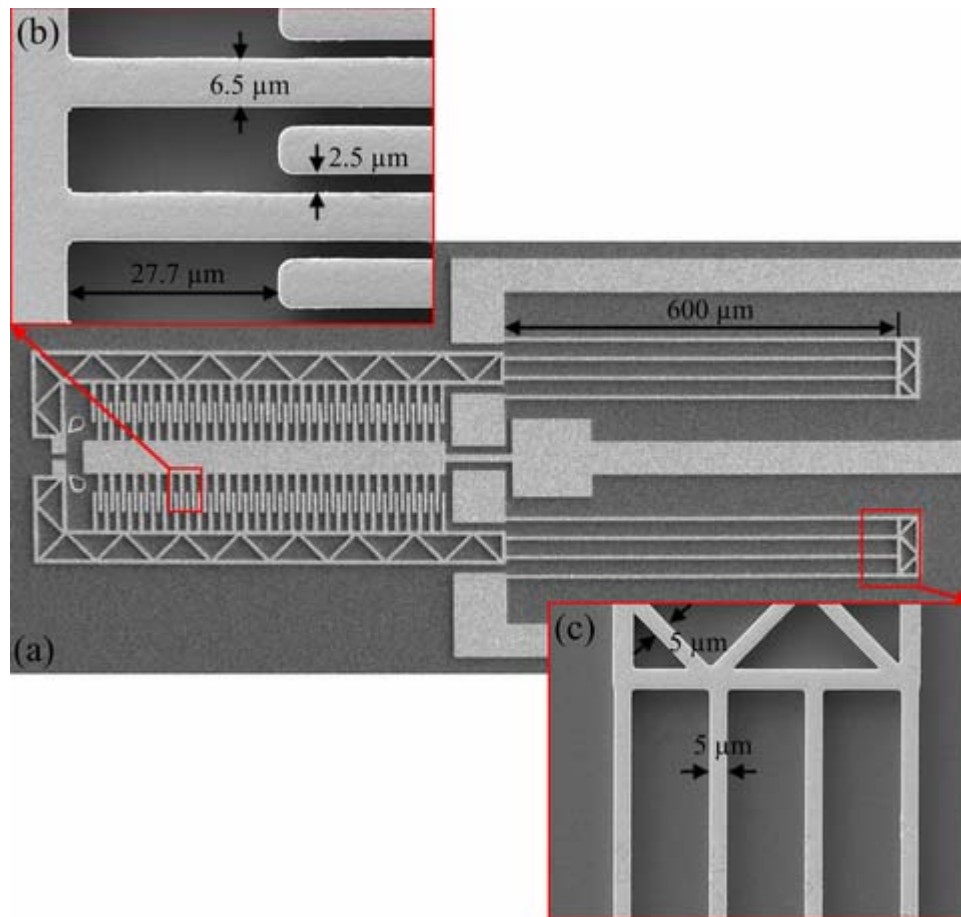


Figure 5.22 SEM image of an electrostatically actuated (a) 3-comb single-anchored device before release with detailed views of (b) comb fingers and (c) double-folded cantilever flexures

Considering another device at a different location on the same wafer, which is a 3-comb double-anchored device (Figure 5.23(a)), although dimensions were even closer to those designed, edges of both comb fingers and device tips were round (Figure 5.23(b)). However, this rounding effect is not expected to have much influence on either electrostatic behavior or proper operation of the device.

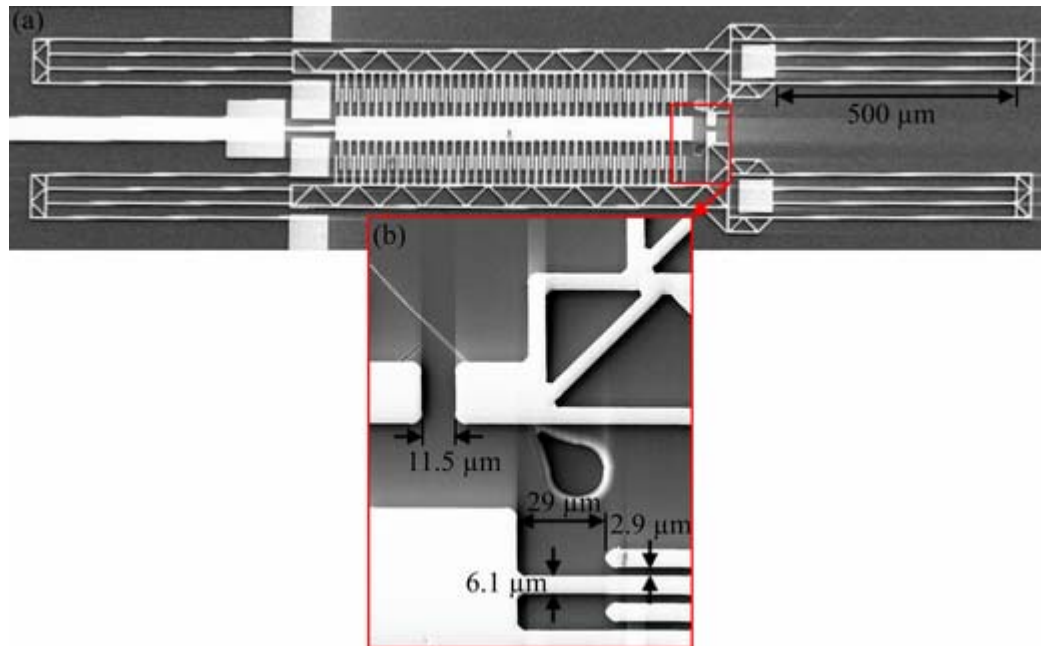


Figure 5.23 SEM image of an electrostatically actuated (a) 3-comb double-anchored device before release with (b) a detailed view from the tip

Note that, ideal deposition rate for Ni is $0.2 \mu\text{m}/\text{min}$ at $1.0 \text{ A}/\text{dm}^2$ and process parameters used correspond to a device thickness of $6 \mu\text{m}$ for the active electroplating area defined by Electroplating Mask. Although it was observed that thickness of most devices vary in the range from $5.5 \mu\text{m}$ to $6 \mu\text{m}$ after release, device thickness was considerably varying at some locations within the wafer.

On one extreme, there are over-deposited devices such as a 3-comb double anchored device (Figure 5.24(a)), which is located close to wafer edge. This excessive deposition yielded in a mushroom shaped structure (Figure 5.24(b)) and merged comb fingers (Figure 5.24(c)) and the resulting device is completely useless.

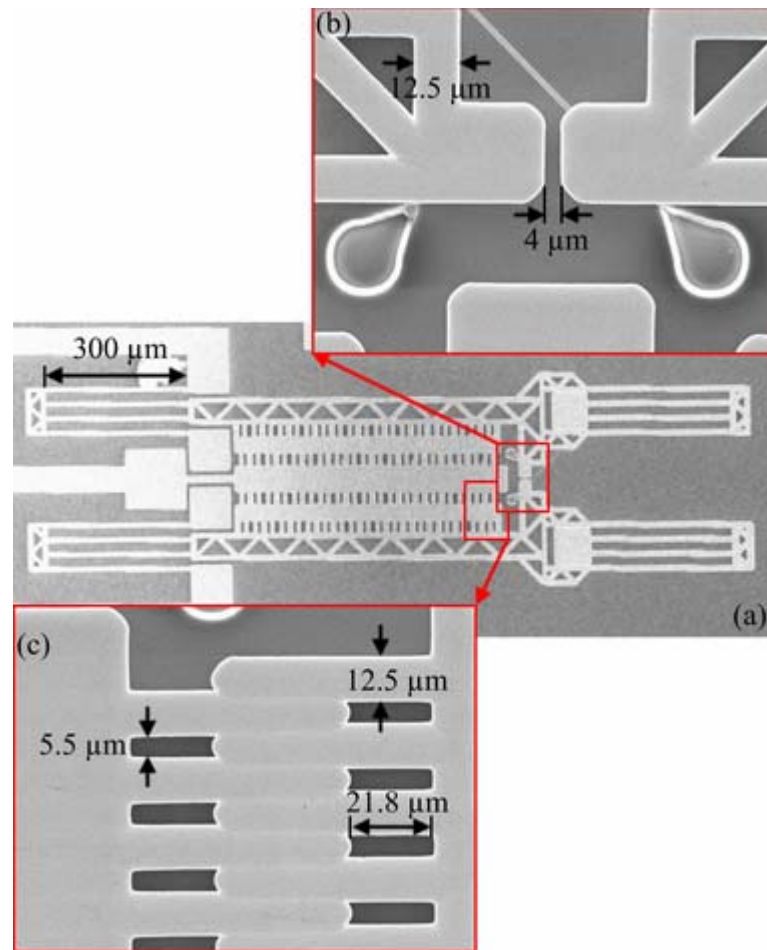


Figure 5.24 SEM image of an electrostatically actuated (a) 3-comb single-anchored device before release with detailed views of (b) device tip and (c) merged comb fingers

On the other extreme there are under-deposited devices such as a 3-comb single anchored device, which is thin in the form of a metal sheet (Figure 5.25(a)). Although its dimensions were close to ideal, the device was so thin that portions of crack openings overlapping with device tips can be well observed from above (Figure 5.25(b)).

Such problems related to deposition thickness can be eliminated by connecting a current thief, which is a dummy electrode in the form of a ring surrounding the wafer, to a secondary cathode.

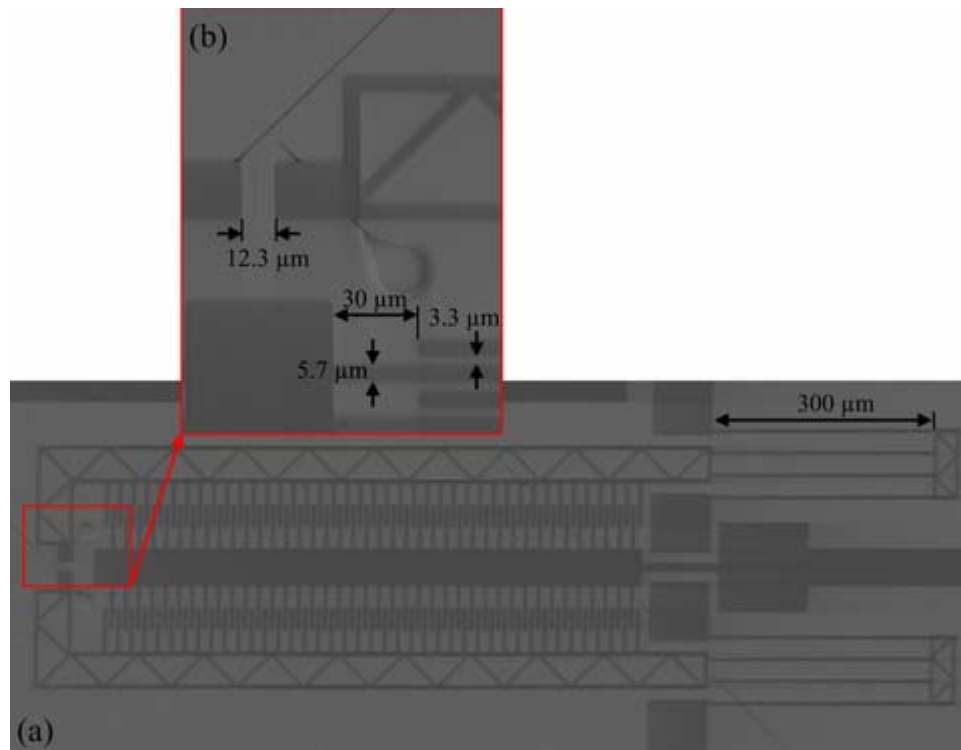


Figure 5.25 SEM image of an electrostatically actuated (a) 3-comb single-anchored device before release and seed layer removal with (b) a detailed view from the tip

Problems similar to those mentioned above were also observed for thermally actuated nanotweezers. However, dimensions of most devices were again reasonable for both 2- and 3-beam devices (Figure 5.26(a)) with beam widths slightly being larger than designed. As an example, beams designed as 4 μm turned out to be 4.7 μm, resulting in a smaller gap of 3.3 μm instead of 4 μm, in between (Figure 5.26(b)).

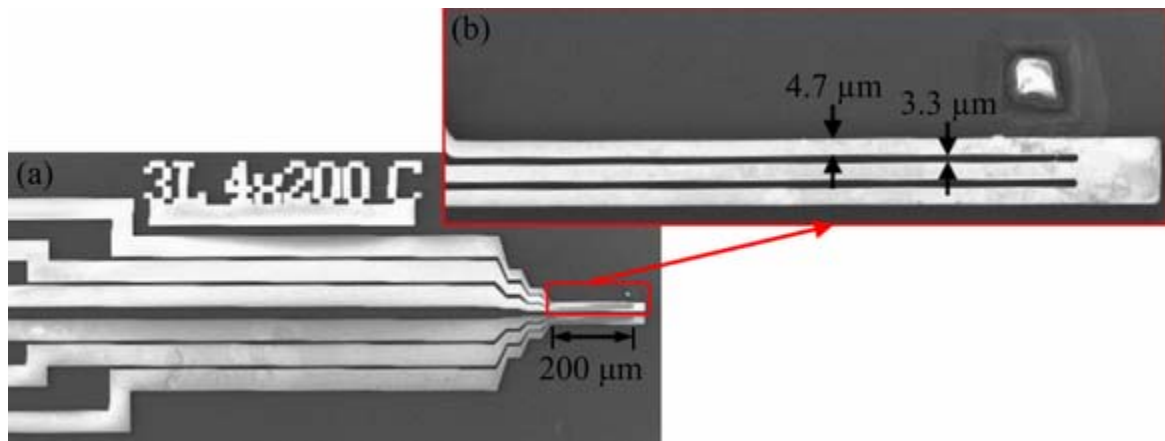


Figure 5.26 SEM image of a thermally actuated (a) 3-beam device after release with (b) device tip in detail

One insignificant problem at this step is that devices might contain defects (Figure 5.27(a)) or missing features (Figure 5.27(b)) due to under exposure or development during lithography sub-step.

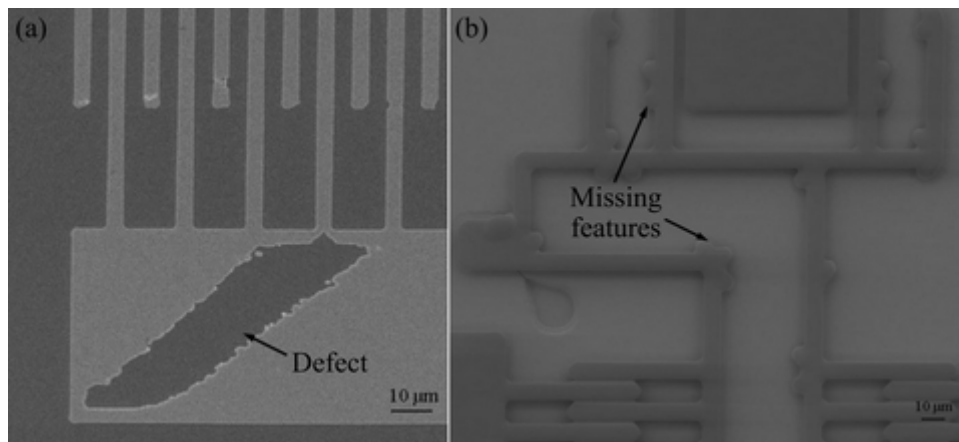


Figure 5.27 SEM image of devices with (a) defects and (b) missing features due to lithographic problems

Note that, ideal deposition rate for Ni is $0.2 \mu\text{m}/\text{min}$ at $1.0 \text{ A}/\text{dm}^2$ and process parameters used correspond to a device thickness of $6 \mu\text{m}$ for the active electroplating area defined by Electroplating Mask. Actual thickness of devices will be investigated after dicing of the chips and release.

5.3.5. Cutting of Nanowire Ends

Initially a $9.5 \mu\text{m}$ -thick photoresist film was used in masking of the wafer for cutting of nanowire ends. After exposure and development, air bubbles were observed in the photoresist film as a result of irregular topography of the wafer surface (Figure 5.28).

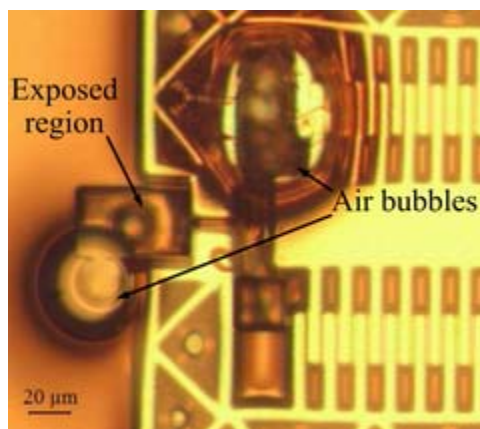


Figure 5.28 Air bubbles in $9.5 \mu\text{m}$ -thick photoresist film

These air bubbles should be eliminated since they might result in complete etching of nanowire end-effectors or damaged actuator devices when exposed to nitric acid. Decreasing the thickness of the photoresist layer to $6.2 \mu\text{m}$ solved the problem and uniformity was achieved over the wafer.

One problem for the first batch wafers was the misalignment between Mask #3 and Mask #4 due to the previously mentioned misalignment between Mask #1 and Mask #3. Hence, it was not possible to achieve perfect alignment of nanowire cutting patterns with respect to device tips using alignment marks. Problem was partially solved by misaligning Mask #4 in the direction of the initial misalignment, approximately with the same amount (Figure 5.29). However, it is not possible to eliminate misalignment completely unless alignment is performed with respect to two devices close to alignment marks instead.

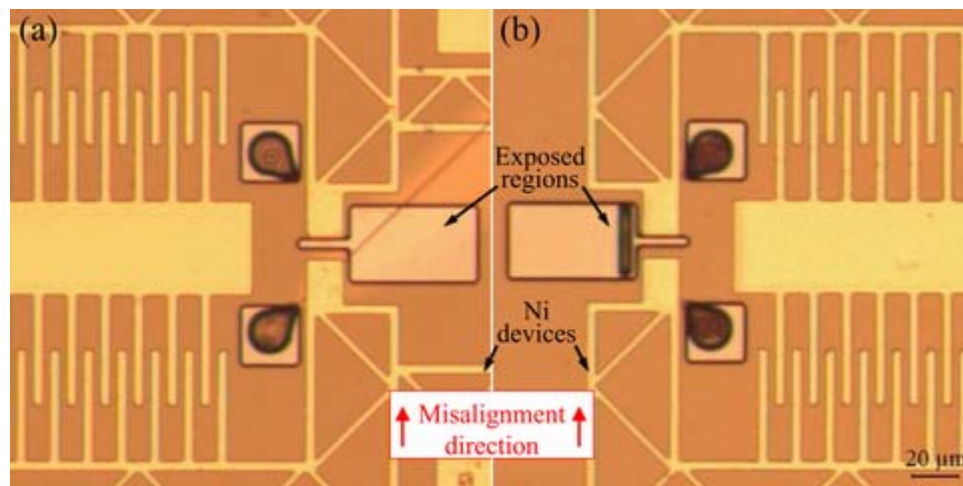


Figure 5.29 Misalignment between Mask #3 and Mask #4 at device tips pointing to opposite directions perpendicular to misalignment direction (a) without and (b) with the presence of a free surface

Since Mask #3 was perfectly aligned with respect to Mask #1, this problem did not exist for second batch wafers (Figure 5.30).

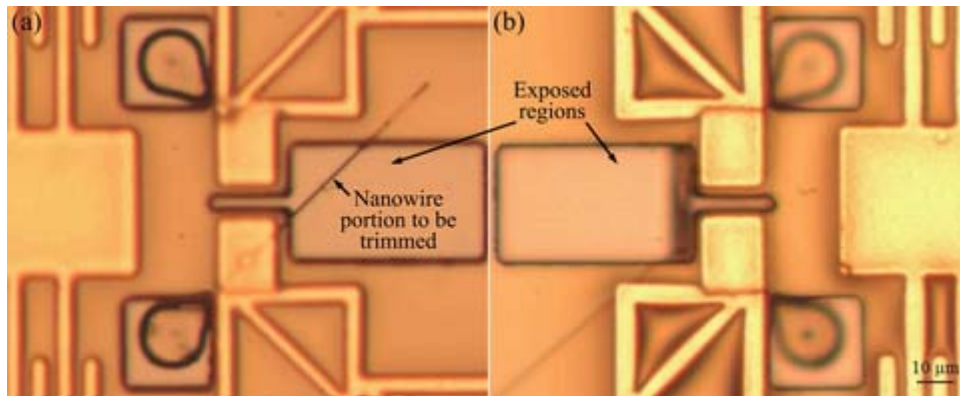


Figure 5.30 Perfect alignment between Mask #3 and Mask #4 at device tips pointing to opposite directions (a) without and (b) with the presence of a free surface

Although it was known that, Ni etch rate of 20% nitric acid solution is 5 $\mu\text{m}/\text{hour}$, a 10% nitric acid solution was prepared initially, with a Ni etch rate of about $2\frac{1}{2}$ $\mu\text{m}/\text{hour}$, in order not to lose nanowires completely in the first trial.

One of the first batch wafers was put into this Ni etching solution for 2 minutes. When the wafer is investigated after release it was observed that, regions at tips of over-deposited devices, which overlap with openings on Nanowire Cutting Mask (i.e. Mask #4) as a result of the misalignment mentioned above, were slightly etched (Figure 5.31(a) and (b)); however, nanowires were not influenced by the nitric acid solution and they were connected to either a matching nanowire or excess Ni deposited on crack inducer walls.

For this reason, etch time is increased to 4 minutes for a second wafer. When the wafer is investigated after release it was observed that, in spite of the increased etch time, nanowires were either not even influenced or merely etched by the nitric acid solution (Figure 5.32). As a result, it was inferred that crack openings were not wide enough for the liquid etchant to diffuse inside and reach nanowire surfaces in such a short amount of time.

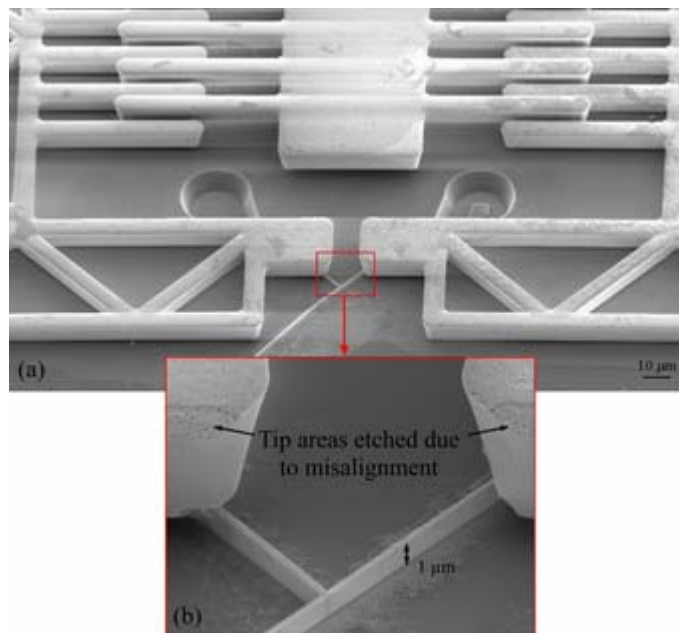


Figure 5.31 SEM image showing 45° tilted front view of (a) a pair of nanotweezers after etching of the sacrificial SiO_2 layer with (b) merged nanowire end-effectors in detail

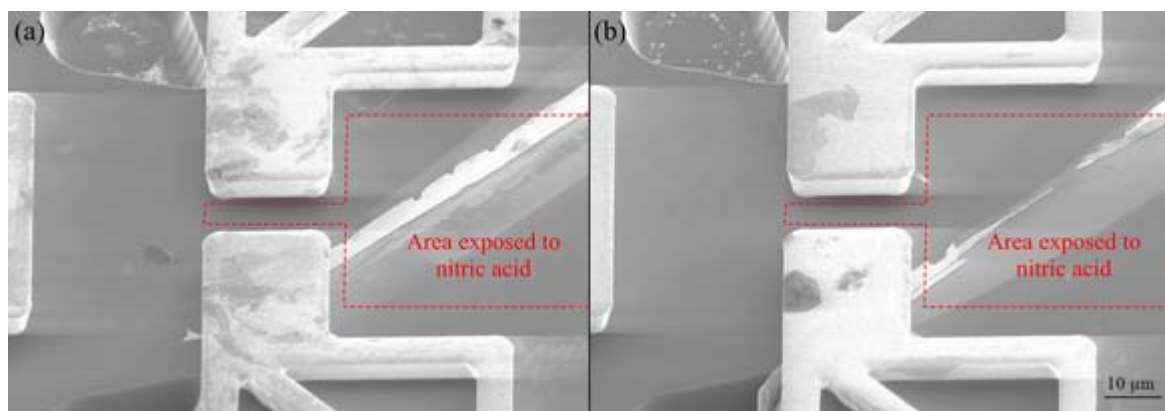


Figure 5.32 SEM images showing 45° tilted side views of nanotweezers after etching of the sacrificial SiO_2 layer with nano-scale end-effectors (a) not influenced and (b) influenced by Ni etchant

One solution might be further increasing the etch time. However, this would certainly result in a considerable amount of etching at device tips. Instead, crack openings were further widened in BHF for 3½ minutes before putting the wafer into nitric acid solution for second batch wafers. Furthermore, since alignment was almost perfect for this set, concentration of the nitric acid solution was increased to 20% and etch time was increased to 6½ minutes, which corresponds to a etch thickness slightly larger than 500 nm. When wafers were investigated after release, it was observed that nanowires were successfully detached from both the matching nanowire and excess Ni deposited on crack inducer walls (Figure 5.33).

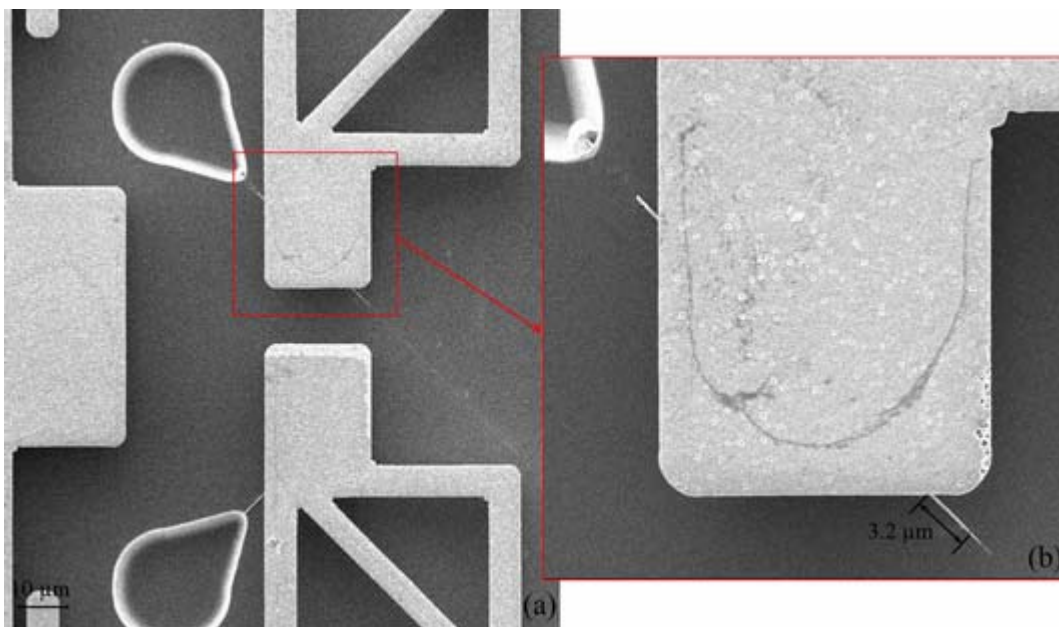


Figure 5.33 SEM image showing (a) a pair of nanotweezers after etching of the sacrificial SiO₂ layer with (b) the single nanowire end-effector successfully detached from both ends after Ni etch in detail

Another solution might be cutting nanowire end-effectors to a desired length by focusing an ion beam, i.e. FIB; however, the process was not available at Danchip's National Cleanroom Facility.

5.3.6. Release

Release step is performed at wafer level for two of three first batch wafers, where third first batch wafer and all three second batch wafers were diced after nanowire cutting step, when 6.2 μm -thick photoresist masks were still on.

Assuming that 10 nm-thick Cr will be removed together with 200 nm-thick Au layers on both sides of all wafers during a 15- to 20-minute Entreat etch, first of the first batch wafers was put into BHF solution right after removal of the seed layer. However, it was observed that, although crack openings were slightly widened, sacrificial SiO_2 layer was still remaining even after a sufficiently long amount of time. When the wafer is investigated under SEM, the presence of a thin Cr foil, which prevents the sacrificial SiO_2 layer from being etched, was realized (Figure 5.34).

This might also be the reason why nanowire end-effectors first of first batch wafers were not influenced by the nitric acid solution. Hence, 10 nm-thick Cr layers were also etched by putting the wafers into Cr etchant for 40 seconds before nanowire cutting step.

Another hindrance, which protected the sacrificial SiO_2 layer from being etched, might be the presence of a thin photoresist film that remains after Mask #4 is removed in acetone. This problem was eliminated for all remaining wafers by repeating resist removal procedure twice with the addition of an isopropanol (IPA) rinse in between and by refreshing acetone used.

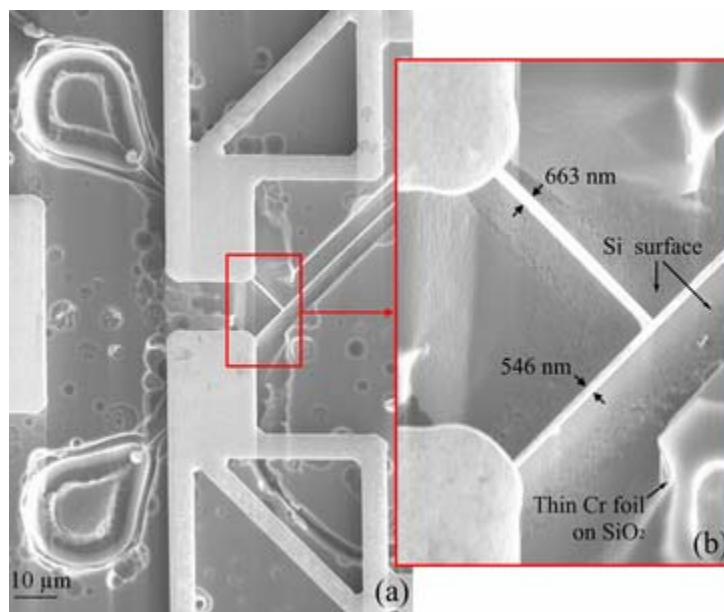


Figure 5.34 SEM image showing (a) a pair of nanotweezers after partial etching of the sacrificial SiO_2 layer with (b) nanowire end-effectors without Cr etch in detail

After removal of the sacrificial SiO_2 layer, it was observed that most of the devices on the initial first batch wafer were successfully released with nano-scale end-effectors, mostly in the form of merged nanowires, still lying on the Si substrate as previously demonstrated in Figure 5.31. However, some nanowires were detached from actuator tips and moved from their original positions during wet etching of the sacrificial SiO_2 layer in BHF (Figure 5.35).

Furthermore, some devices were stuck to the substrate surface due to capillary forces arising when the wafer was dried after being rinsed in DI water (Figure 5.36). Note that, a design error found out at this step is that, some label features failed to remain anchored during BHF etch since they were not wide enough.

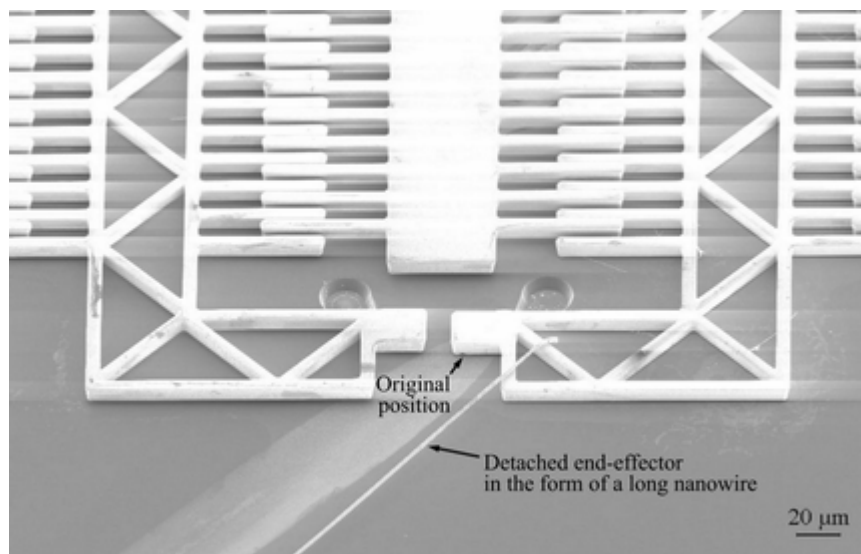


Figure 5.35 SEM image showing 45° tilted front view of a pair of nanotweezers stuck on the substrate surface after etching of the sacrificial SiO₂ layer

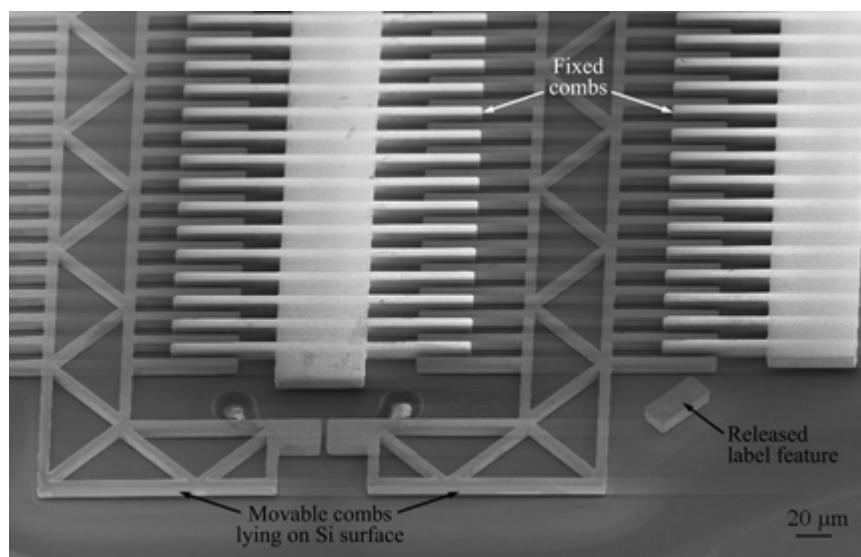


Figure 5.36 SEM image showing 45° tilted front view of a pair of nanotweezers stuck on the substrate surface after etching of the sacrificial SiO₂ layer

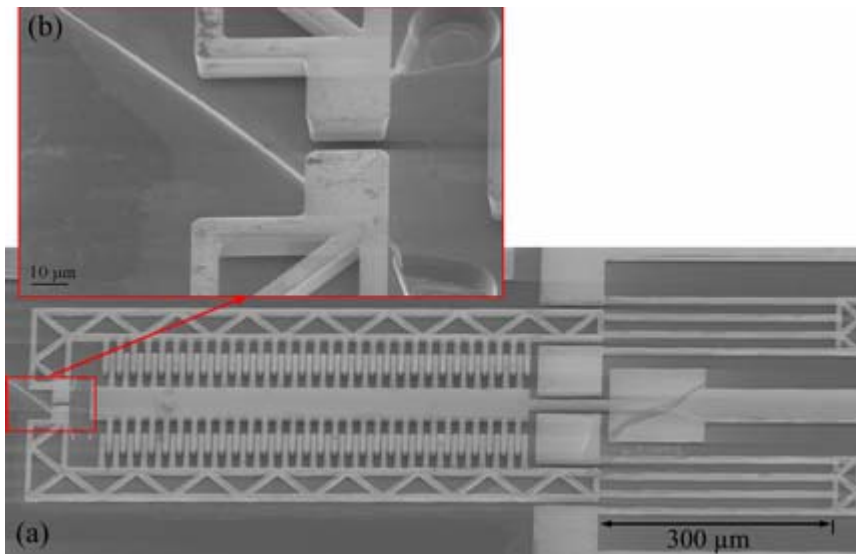


Figure 5.37 SEM image showing 45° tilted side view of (a) a pair of nanotweezers after etching of the sacrificial SiO₂ layer with (b) the single end-effector in the form of a long nanowire in detail

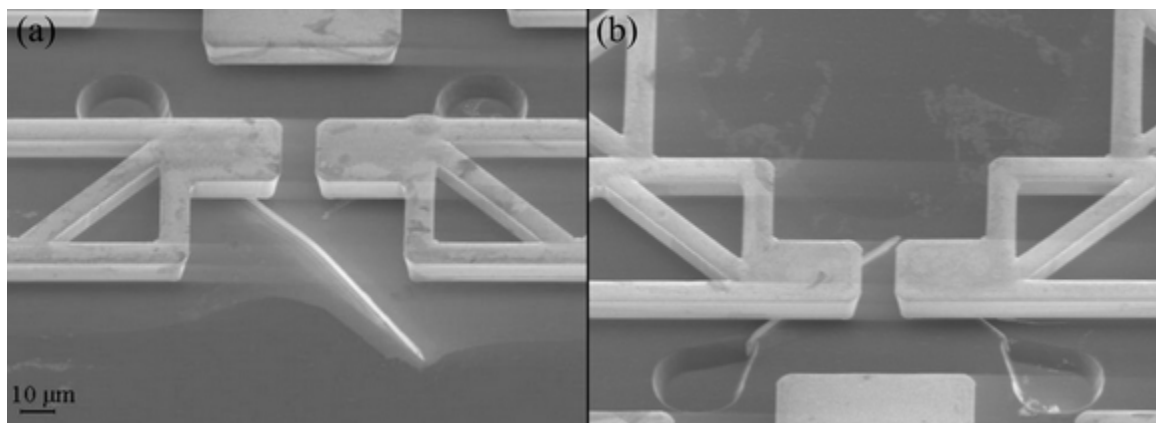


Figure 5.38 SEM image showing 45° tilted (a) front and (b) rear views of nanotweezers with end-effectors in the form of short nanowires after etching of the sacrificial SiO₂ layer

After removal of the sacrificial SiO₂ layer on the second first batch wafer, it was observed that, most nano-scale end-effectors were not merged unlikely to the first one. They were in the form of either a long nanowire on only one of the actuator tips (Figure 5.37) or shorter nanowires on both (Figure 5.38).

Sacrificial SiO₂ layer etching processes of remaining wafers were carried out at chip level and results were more or less similar those mentioned above. One such example was previously demonstrated in Figure 5.33.

Complete release, by wet etching the substrate surface in KOH, was performed for only first of the first batch wafers and some chips from either second batch or last of the first batch wafers.

Devices sticking on the surface of the initial first batch wafer were successfully released after etching of Si underneath by an amount of 5.4 μm, in a 33 wt% KOH solution at 60°C. However, resulting surface was rather rough. Furthermore most nanowire end-effectors were detached from actuator tips and washed away during the harsh KOH etching process.

Successful integration of nano-scale end effectors with actuator devices were achieved for many devices on first batch wafers #1 and #2 after complete release. One example from the first batch wafer #1 is an electrostatically actuated 3-comb double anchored device with merged nano-scale end effectors in the form of “nanoribbons” (Figure 5.39(a)). Although actuator tips were at their original positions initially, they were closed due to electrical charging when being investigated under SEM (Figure 5.39(b)).

In order to understand whether nano-scale end-effectors were connected or not, the wafer was cleaved into smaller pieces, so that further tilting the device could be possible while investigating under SEM. It was observed that the device has returned to its original position, either when taken out from SEM or during cleaving.

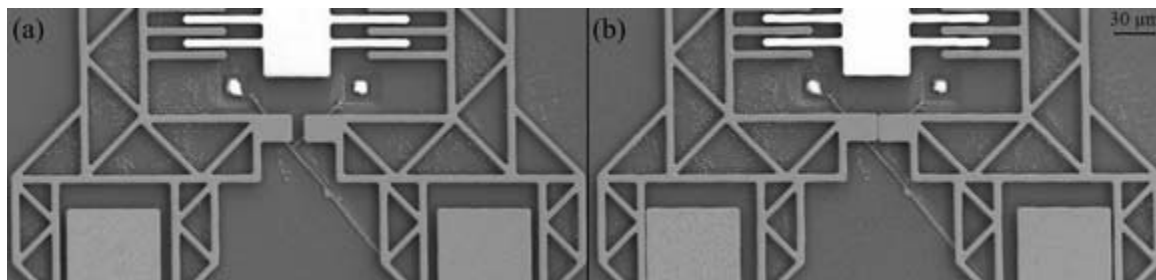


Figure 5.39 SEM image showing top view of a pair of nanotweezers with nano-scale end-effectors in the form of merged nanoribbons at (a) original and (b) closed positions after complete release

Looking from front side of the device, it was gradually tilted to 45° (Figure 5.40(a)), 80° (Figure 5.40(b)) and finally 89° (Figure 5.40(c)).



Figure 5.40 SEM images showing (a) 45° (b) 80° and (c) 89° tilted front views of a pair of nanotweezers with nano-scale end-effectors in the form of merged nanoribbons after complete release

When zoomed in, it was observed that nano-scale end effectors in the form of merged nanoribbons were completely released and attached to the actuator tip on the left (Figure 5.41). It can be inferred that nano-scale end-effectors were also attached to the actuator tip on the right; however, the connection in between might have been broken when actuator tips were closed.

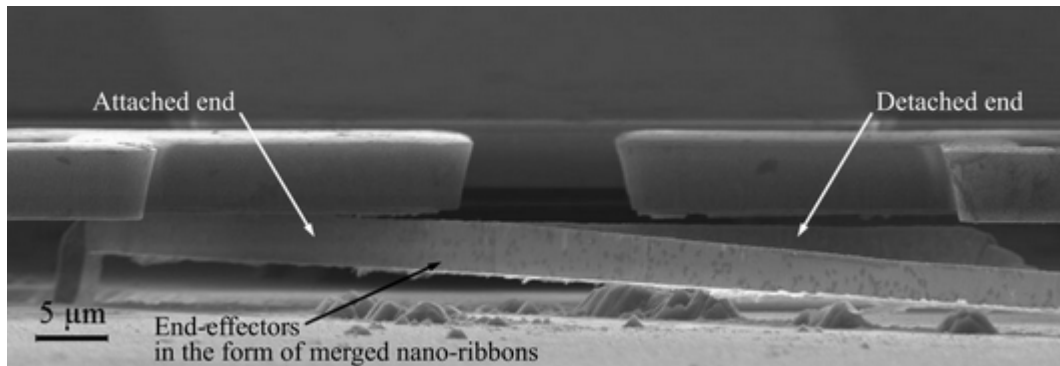


Figure 5.41 SEM image of the pair of nanotweezers demonstrated in Figure 5.36(c) with nano-scale end-effectors in detail

There are more examples on the first batch wafer #2, generally with a single end-effector on only one actuator tip, which is in the form of either a relatively long nanoribbon not influenced by the nickel etchant (Figure 5.42), or a shorter one that is partially etched (Figure 5.43).

Heights of the high-aspect-ratio nano-scale end-effectors vary in the range from 2.5 μm to 4.5 μm. Note that, although their widths are in the range from 230 nm to 300 nm, most of these nano-scale end-effectors have over deposited upper portions. Hence, they seem to be wider, i.e. with widths in the range 600 nm to even 1.5 μm when looked from top.

There is an interesting device, which was similar to the example device on the first batch wafer #1 (Figures 5.39 to 41) initially, in the sense that it has end-effectors in the form of merged nanoribbons (Figure 5.44). However, end-effectors are separated either due to etching during “Cutting of the Nanowires” or by breaking during “Release”.

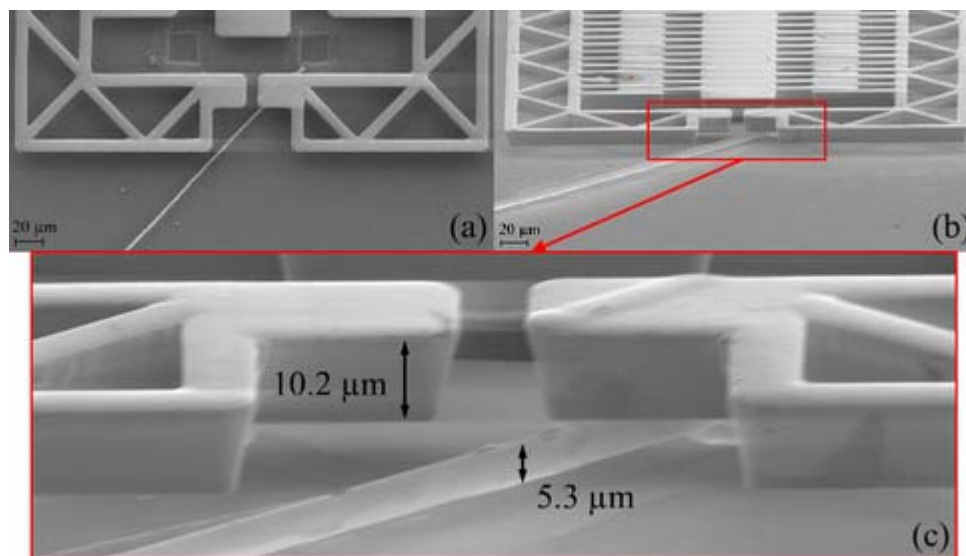


Figure 5.42 SEM images showing (a) top and (b) 75° tilted front views of the tips of a pair of nanotweezers with (c) a more detailed view showing the single end-effector in the form of long nanoribbon

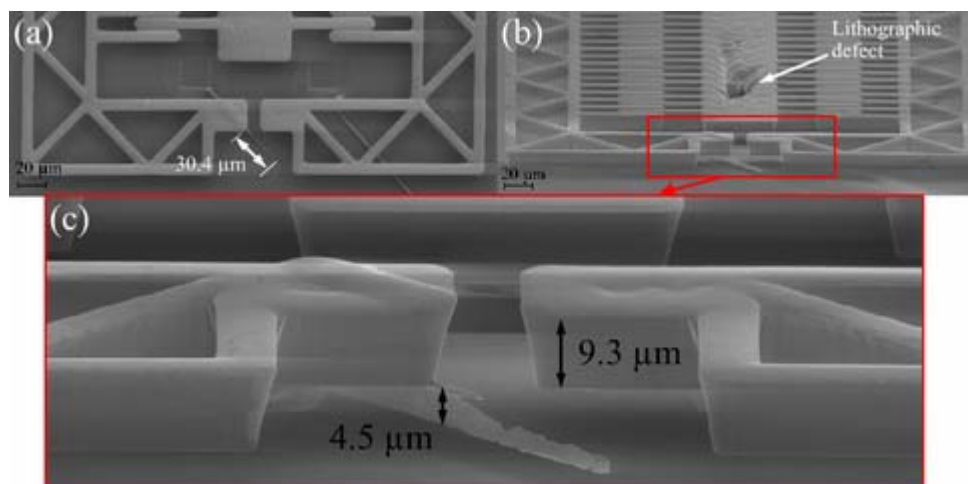


Figure 5.43 SEM images showing (a) top and (b) 75° tilted front views of the tips of a pair of nanotweezers with (c) a more detailed view showing the single end-effector in the form of an etched nanoribbon

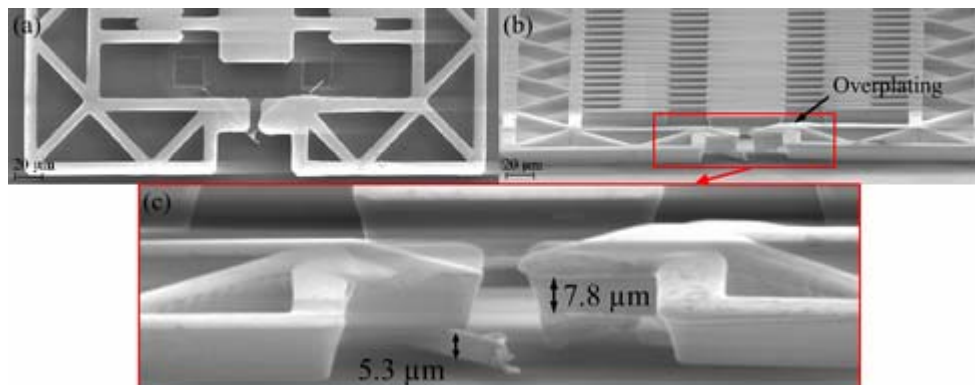


Figure 5.44 SEM images showing (a) top and (b) 75° tilted front views of the tips of a pair of nanotweezers with (c) a more detailed view showing end-effectors in the form of a pair of broken nanoribbons

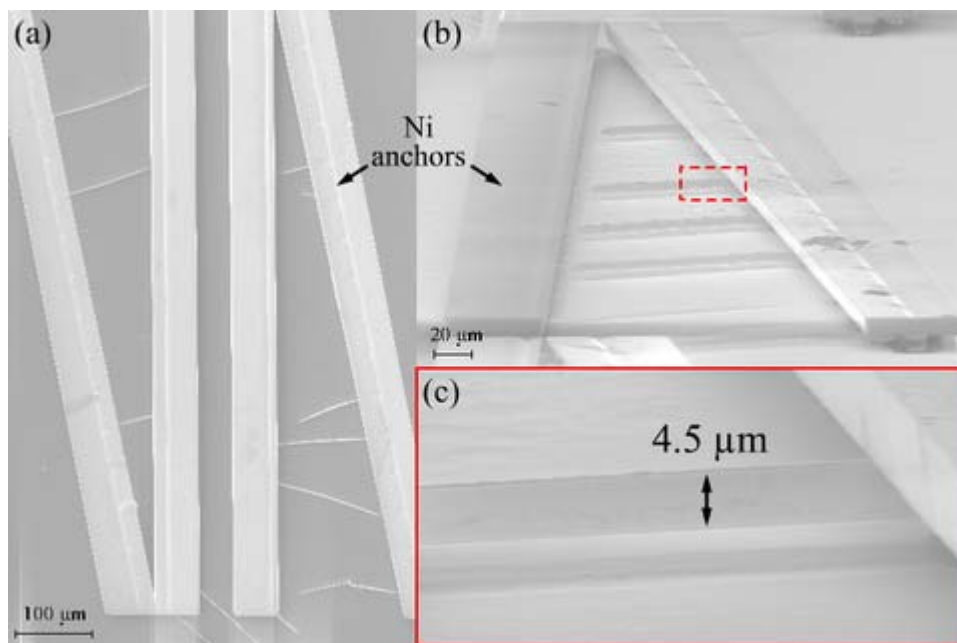


Figure 5.45 SEM images showing (a) top view of a nanowire test structure and (b) a 85° tilted side view of a similar one with (c) a single high-aspect-ratio nanostructure in detail

Although not all nanowire test structures on test chips also yielded efficient cracking, there are various arrays of free standing high-aspect-ratio nanostructures, which are fixed to nickel anchors (Figure 5.45). Note that, such kind of structures might be useful in many applications as mass flow or chemical sensors and mechanical switches.

However, integration has not been observed for devices in chips, which were diced from either second batch or third one of first batch wafers yet (Figure 5.46). One reason for this might be that nano-scale end-effectors has never been connected to actuator tips as a result of seed layer atoms not diffusing inside crack openings due to improper BHF etch time prior to this step. Another possibility is that, although integration has been achieved initially, nano-scale end-effectors might have been detached from actuator tips, as a result of excessive etch time during etching of the seed layer.

Furthermore, when actuator tips were investigated under SEM, with a 80° tilt angle and in a similar manner mentioned above, it was observed that the sacrificial SiO_2 layer underneath actuator tips were not completely etched. Consequently, it can be concluded that, BHF etch time during release etch should slightly be increased.

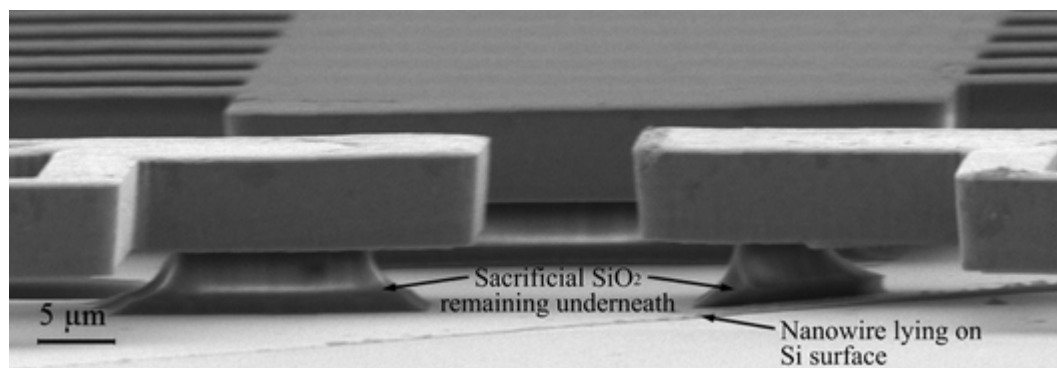


Figure 5.46 SEM image showing unattached nano-scale end effectors of a pair of nanotweezers in a same manner as in Figure 5.37 with a 80° tilt angle

Chapter 6

ACTUATION AND DEVICE CHARACTERIZATION

6.1. Introduction

This thesis mainly focuses on *design* and *fabrication* of the nanotweezers, where characterization and testing are subjects of future studies. However, in order to demonstrate that fabricated devices are functional and proposed fabrication method is valid; actuation and static characterization of both electrostatically and thermally actuated devices were performed.

In this chapter, static characterization setup will be described initially. Then, actuation results will be presented for both electrostatic and thermal nanotweezers and compared with theory.

6.2. Actuation and Static Characterization Setup

Static characterizations of the Nanotweezers were performed in air and at wafer-level, using a Karl Suss probe station. Actuation setup is quite simple (Figure 6.1), wafer is fixed to the vacuum chuck of the probe station and electrical connection with the device to be tested is achieved through its bonding pads via probing. Note that, wafer is also probed during the characterization of electrostatically actuated devices since both the substrate and movable combs should be at the same potential in order to prevent any interaction between

these two. Afterwards, the microscope of the probe station, which has a camera connected to a PC, is focused to the actuator tips and probes are electrically connected to a DC power supply.

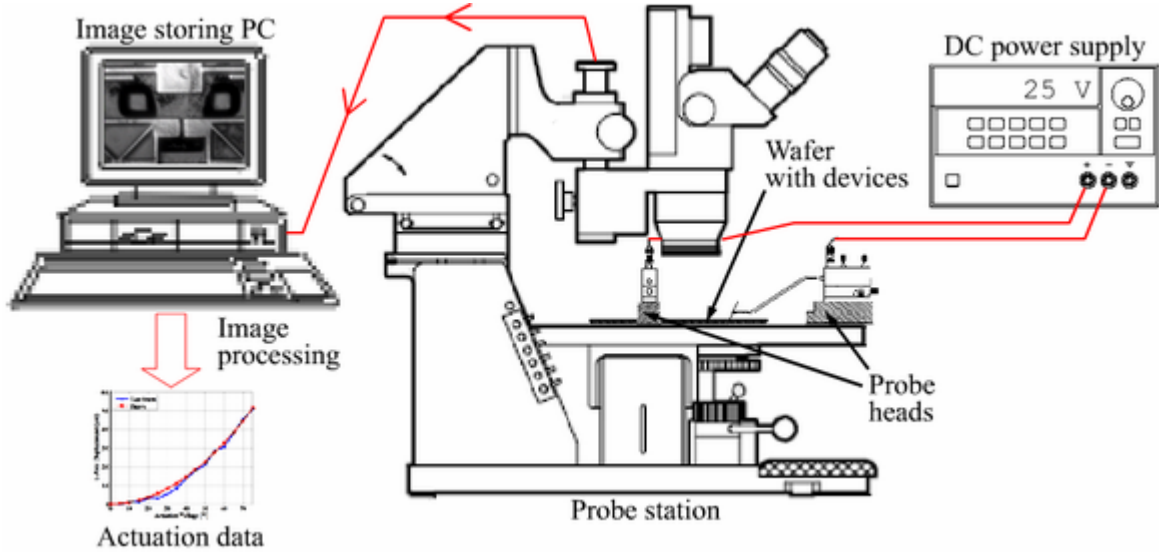


Figure 6.1 Setup used for actuation and static characterization of nanotweezers

After capturing an image of the actuator tips in the absence of any potential difference and stored in the PC, voltage is gradually increased until the maximum deflection voltage is reached, with 5 V steps for electrostatically actuated devices and 0.1 V steps for thermally actuated devices, and data is collected by repeating the image grabbing at each step.

Then, grabbed images were processed, using a photo editing software such as ACD Photo Editor or even Microsoft Paint, and tip-displacement data is obtained in terms of pixels. Knowing resolution of the image, magnification of the microscope and scale factor of the camera, pixel values are converted to μm 's and actuation curve is obtained as a function of the applied voltage.

6.3. Actuation and Static Characterization Results

Results for Electrostatically Actuated Devices:

Displacement results for three electrostatically actuated devices with single-sided flexure arrangements, a 50-comb device with 4 $\mu\text{m} \times 400 \mu\text{m}$ beams (Figure 6.2), a 30-comb device with 4 $\mu\text{m} \times 500 \mu\text{m}$ beams (Figure 6.3) and a 50-comb device with 4 $\mu\text{m} \times 500 \mu\text{m}$ beams (Figure 6.4), are plotted below, together with theoretical displacement curves obtained by inserting actual device dimensions to the below formula:

$$x = \frac{F_{es}}{k_{mech,x}} = -\frac{1}{2} \frac{N_f \epsilon_0 h_s^3}{E_s h_s w_s^3} \left(\frac{w}{(g_x - x)^2} + \frac{1}{g_y} \right) V^2 \quad (6.1)$$

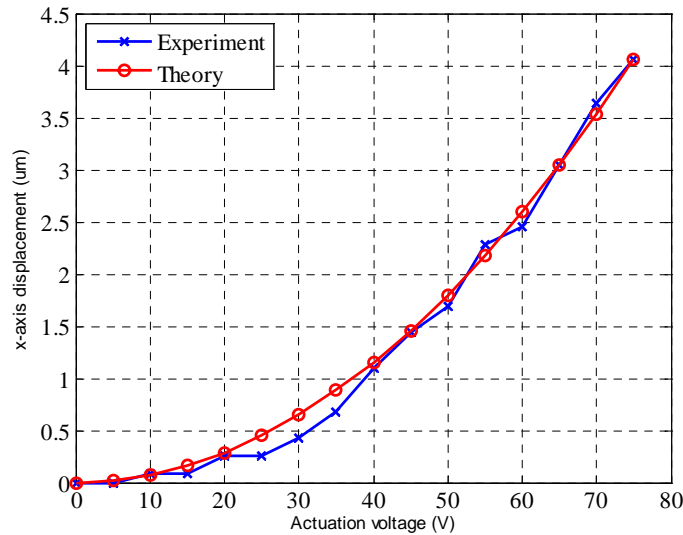


Figure 6.2 Actuation data for a 50-comb electrostatically actuated device with single-sided 4 $\mu\text{m} \times 400 \mu\text{m}$ flexure arrangement

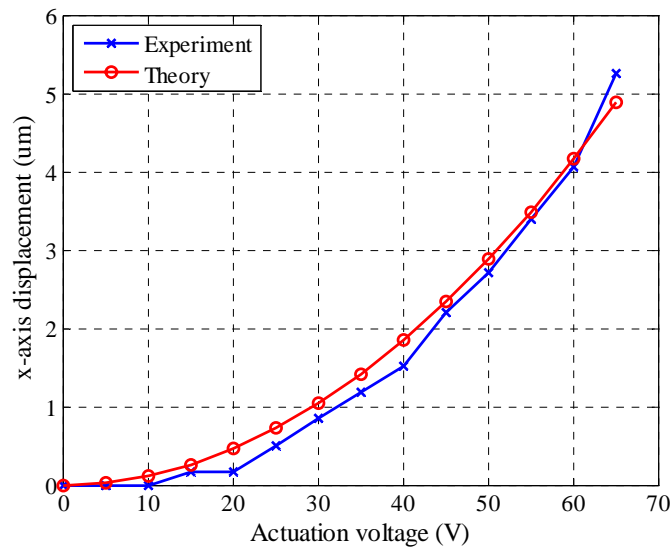


Figure 6.3 Actuation data for a 30-comb electrostatically actuated device with single-sided $4\ \mu\text{m} \times 500\ \mu\text{m}$ flexure arrangement

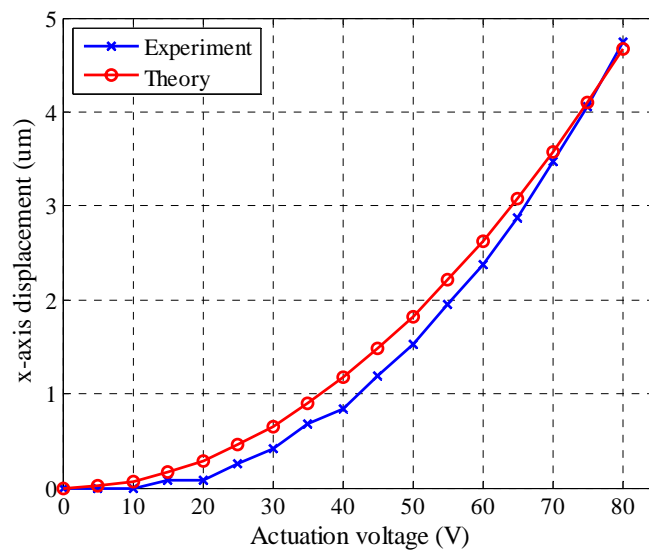


Figure 6.4 Actuation data for a 50-comb electrostatically actuated device with single-sided $4\ \mu\text{m} \times 500\ \mu\text{m}$ flexure arrangement

Note that, Equation 6.1 is for single-anchored devices and it should be multiplied by 2 for double-anchored devices.

Results for Thermally Actuated Devices:

Displacement result for two thermally actuated devices with three-beam structures, having $4\ \mu\text{m} \times 200\ \mu\text{m}$ (Figure 6.5) and $4\ \mu\text{m} \times 400\ \mu\text{m}$ (Figure 6.6) cantilever beams, are plotted below, together with theoretical displacement curves obtained using actual device dimensions.

Note that, both devices were actuated using the voltage configuration shown in Figure 2.5(b) of Chapter 2.

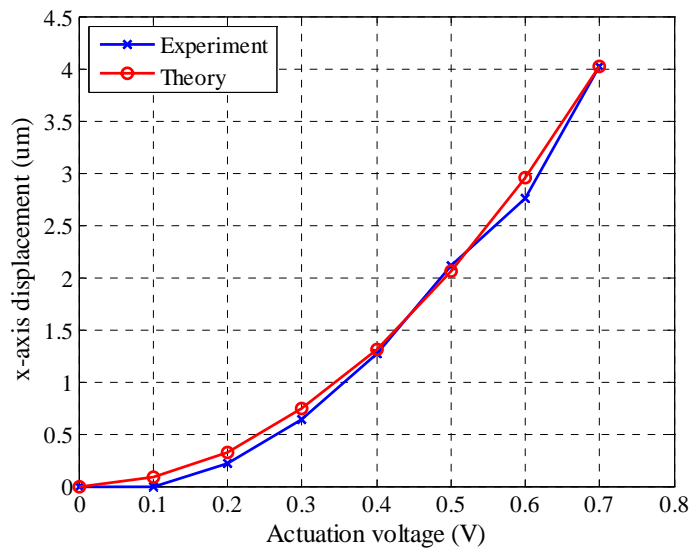


Figure 6.5 Actuation data for a three-beam thermally actuated device with $4\ \mu\text{m} \times 200\ \mu\text{m}$ cantilever beams

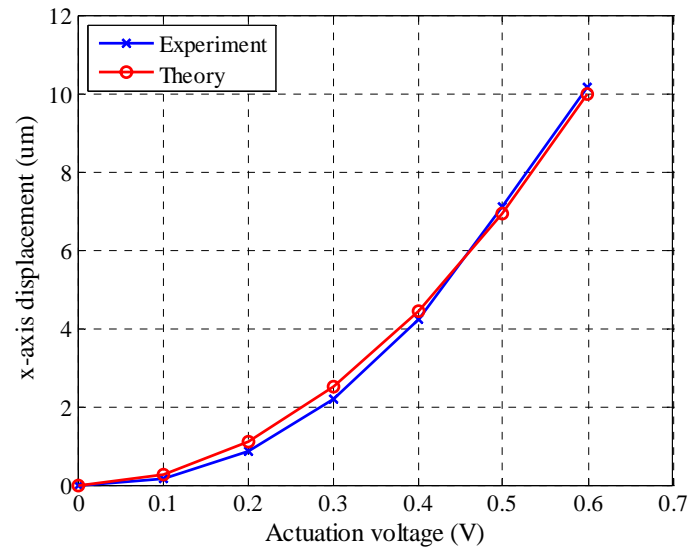


Figure 6.6 Actuation data for a three-beam thermally actuated device with $4\ \mu\text{m} \times 400\ \mu\text{m}$ cantilever beams

Chapter 7

FABRICATION AND DESIGN ALTERNATIVES

7.1. Introduction

After proving the feasibility of the proposed fabrication method by achieving successful integration even in the first fabrication batch, next step is to increase the fabrication yield and enhance the performance of the devices by proposing some fabrication and design alternatives.

In this chapter, three alternative fabrication sequences, which are mainly modified versions of the original procedure, and a design alternative, which includes the addition of a bi-layer thermal actuator as a third gripping arm, will be proposed.

7.2. Alternative Fabrication Sequences

For the purpose of increasing fabrication yield, three fabrication alternatives can be put forward. First two alternatives differ from the original fabrication procedure only in “Preparation of a Layer for Integration” step, i.e. Step 3, where remaining fabrication steps are to be performed exactly as described in Chapter 4. The idea behind both methods is to insert an additional metal plate of either Ni or Cr/Au on nanowire portions, which overlap with actuator devices, for extending the interface area in-between.

The last alternative is similar to first two alternatives, however; it includes complete removal of the sacrificial SiO_2 layer prior to fabrication of actuator devices by electroplating.

Alternative Fabrication Method #1:

As the first sub step of the first alternative fabrication method, i.e. Method #1, Step 3 is performed by only increasing photoresist thickness to $6.2\ \mu\text{m}$ from $1.5\ \mu\text{m}$, and increasing the BHF etch time to 20 minutes from $3\frac{1}{2}$ minutes (Figure 7.1(b) and (e)).

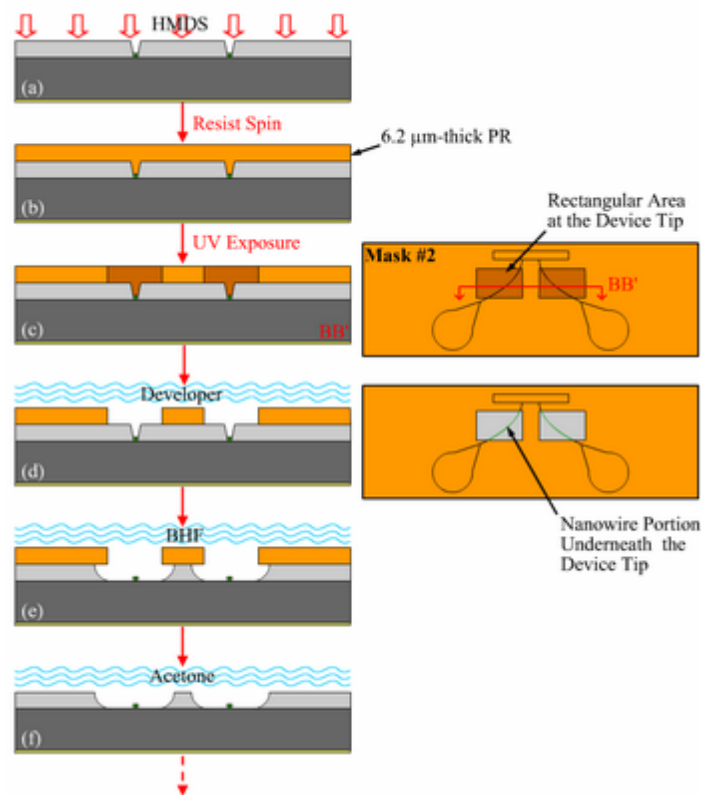


Figure 7.1 Modified version of the fabrication sequence for “Preparation of a Layer for Integration”, i.e. Step 3

The reason for increasing the resist thickness is to ensure the survival of the mask to a 20 minute-BHF and the reason for increasing the BHF etch time is to completely remove the sacrificial SiO₂ layer at locations where metal plates are to be deposited.

Afterwards, the wafer surface is again masked using *Crack Widening Mask*, i.e. Mask #2, but with a thicker photoresist layer this time. For this purpose, a 32½-minute hexamethyldisilazane (HMDS) (i.e. [(CH₃)₃Si]₂NH) heat treatment at 150 °C is performed (Figure 7.2(a)) on the wafer and a 9.5 µm-thick layer of AZ4562 photoresist is spun on the wafer surface (Figure 7.2(b)).

After waiting for about 15 minutes, a 50-second UV exposure is performed on the wafer using Mask #2 (Figure 7.2(c)), which is followed by a 270-second development in a 1:5 mixture of AZ 351 and DI water at 20°C (Figure 7.2(d)). Note that, alignment of Mask #2 with respect to *Crack Initiation Mask*, i.e. Mask #1, becomes essential in order to obtain device tips with proper shapes at the end. Then, the 10 nm/200 nm Cr/Au layer at the back is spin coated with a 2.2 µm-thick layer of AZ 5214 E photoresist in order to eliminate any Ni deposition on this side (Figure 7.2(e)) and an opening on the resist close to wafer edge is left for electrical contact, following the similar procedure described in “Nanowire Deposition” step mentioned in Chapter 4.

As usual, wafer is put into DI water for 3 minutes prior to electrodeposition, in order to soften the photoresist mask by absorbing sufficient amount of water and rest of the procedure is quite similar to the case in nanowire deposition step: Wafer is clamped to the single-contact wafer holder (Figure 4.4) at the location where resist opening is left in order to achieve electrical contact with the wafer through the Cr/Au layer at the back. After dipping the wafer into the electrolyte solution, wafer holder is electrically connected to the anode and current is gradually increased to 410 mA. Hence, Ni starts depositing on the wafer surface inside the photoresist mold forming Ni plates (Figure 7.2(f)).

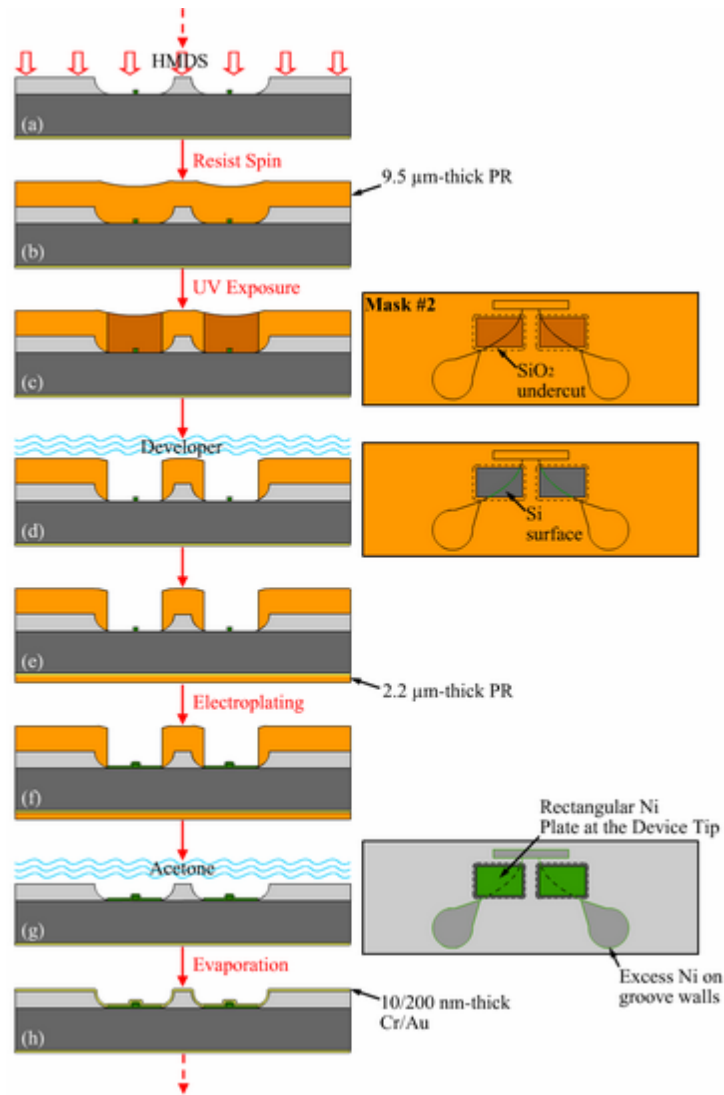


Figure 7.2 First alternative method to be appended to the modified fabrication sequence for “Preparation of a Layer for Integration”, i.e. Step 3

In order to enhance the uniformity over the wafer, electrolyte solution is circulated either by means of a magnetic stirrer or purging air using a pump during the process. After

60 seconds, which corresponds to a deposition thickness on the order of 200 nm, current is decreased to zero again gradually and wafer is taken out of the plating bath.

The wafer is then rinsed in DI water for 2 minutes and photoresist layers on both front and back sides are removed in Acetone for 5 minutes (Figure 7.2(g)) and rinsing step is repeated one more time. As a last step of the newly proposed Step 3, a 10 nm/200 nm Cr/Au layer is deposited on the front side of the wafer by e-beam evaporation and “Fabrication of Devices”, “Cutting of Nanowire Ends” and “Release” steps are performed in exactly the same manner as described in Chapter 4.

Alternative Fabrication Method #2:

When Method #1 is used, there is a possibility of obtaining bulky structures rather than 200 nm-thick smooth Ni plates at the exposed portions of the nanowires since Ni deposition is more likely to start at nanowire surfaces instead of the exposed Si surface due to the drastic increase of the current density at these locations. Such structures might result in deformed actuator tips, which do not function properly.

As a second alternative, Cr/Au plates can be deposited using e-beam evaporation instead of depositing Ni plates via electroplating and hence, a conformal coating of the exposed Si surface can be achieved, together with nanowire ends corresponding to these locations.

First sub step of the second alternative fabrication method, i.e. Method #2, is the same as that of the first alternative fabrication method (Figure 7.1). Furthermore, the wafer surface is again patterned with a 9.5 μm -thick photoresist mask using Mask #2, following exactly the same procedure as Method #1 (Figure 7.3(a) to (d)). Being not necessary, spinning of a 2.2 μm -thick photoresist layer on the wafer surface at the back is eliminated and a 10 nm/200 nm-thick Cr/Au layer is deposited on the patterned wafer surface in front, forming rectangular plates at the exposed regions (Figure 7.2(e)). Then, the photoresist

mask is removed in Acetone for 5 minutes, together with the Cr/Au layer deposited on it (i.e. lift-off) (Figure 7.2(f)), and the wafer is rinsed in DI water.

Finally, a 10 nm/200 nm Cr/Au layer is deposited on the front side of the wafer by e-beam evaporation (Figure 7.2(g)) and rest of the process continues again exactly the same as described in Chapter 4.

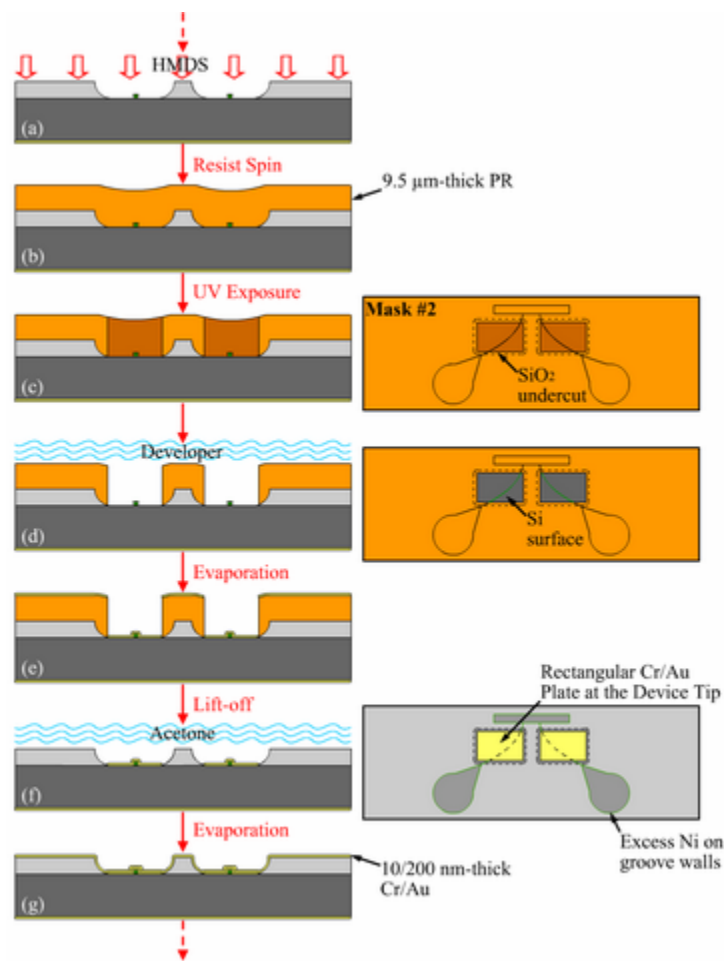


Figure 7.3 Second alternative method to be appended to the modified fabrication sequence for “Preparation of a Layer for Integration”, i.e. Step 3

7.3. Design of a Multi-layer Thermal Actuator as a Third Gripping Arm

In order to enhance the gripping capability of the nanotweezers, a third gripping arm, in the form of a thermally-driven bi-layer thermal actuator, which lies on the fixed comb in the middle projecting over the operation area, can be included to the design (Figure 7.4). The idea is to assist the gripping action of the nanowire end-effectors by either pushing or pulling the object to be manipulated, and hence compensate any misalignment that might occur such as the cases illustrated in Figures 2.7 and 2.9 of Chapter 2.

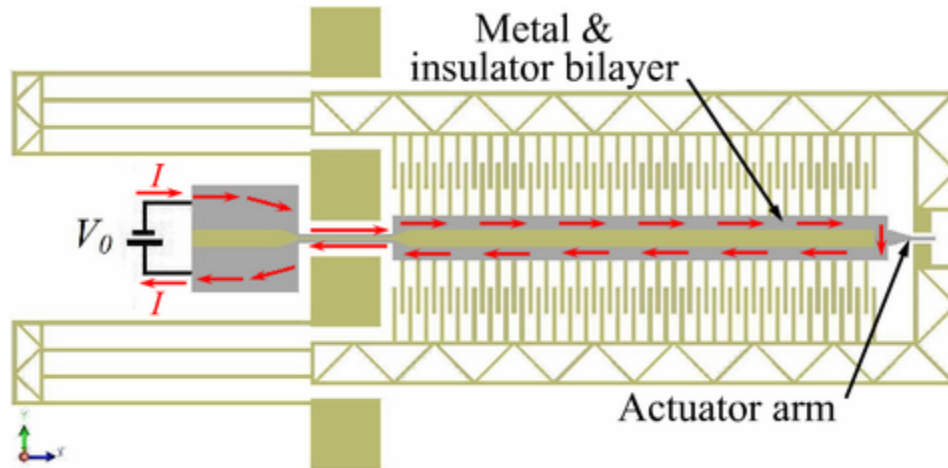


Figure 7.4 Top view of a 3-comb electrostatically actuated nanotweezer, with a bi-layer thermal actuator inserted on the fixed comb in the middle as a third actuating arm, simply illustrating the operation principle

Bi-layer is composed of a metal-insulator pair, such as Parylene and Pt [65], with different coefficients of thermal expansion (CTE) values (Figure 7.5(a)). When a current is passed through as illustrated in Figure 7.4, two layers expand with different amounts and as a result, the actuator arm at the end bends down as a function of the applied voltage due to this elongation mismatch (Figure 7.5(b)).

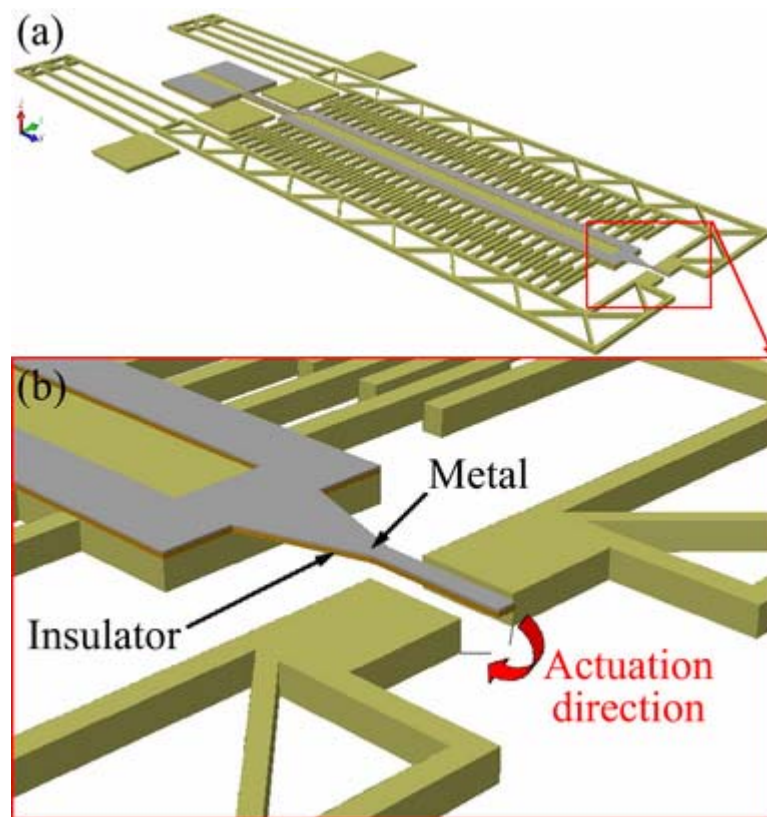


Figure 7.5 (a) Isometric view of a 3-comb electrostatically actuated nanotweezer of Figure 7.4 with (b) a more detailed view of the tips illustrating the direction of actuation

More information on bi-layer (or multi-layer) thermal actuators can be found elsewhere [65-68].

Chapter 8

DISCUSSION AND CONCLUSION

8.1. Introduction

In this thesis, design procedure and self-assembly based fabrication technique for both electrostatically and thermally actuated nanotweezers have been presented. Design procedure for the devices are quite straightforward, however; proposed fabrication technique is a novel approach enabling the integration of nano-scale structures with MEMS devices in a batch compatible manner.

This last chapter includes discussions and conclusions related to results or necessities of the three main stages of the thesis, i.e. *design*, *fabrication* and *characterization*, separately.

8.2. Design

As the first stage of the thesis, electrostatic actuation mechanisms with different comb-drive and flexure arrangements were designed for the nanotweezers.

There are two variations related to comb-drives: number of comb structures in a design and number of comb fingers on each comb structure. There are three-comb devices, where tips can only be closed, as well as five-comb ones, which enable both opening and closing

actions. There are also devices with 30, 40 and 50 comb fingers, with 30-finger devices being the most compact and 50-finger devices being the strongest designs.

Similarly, there are also two variations related to flexures: arrangement and dimensions of double-folded cantilever springs. There are single-anchored devices, with flexures only on the rear ends of the movable combs, as well as double anchored ones, with flexures on both rear and front ends. Although double-anchored devices are more stable, they are not well-suitable for in-situ pick-and-place applications since they are immobile. However, they are useful for static testing applications, where sample is carried by another device with a single-anchored flexure arrangement. Finally, there are flexures with 3, 4 or 5 μm -wide cantilever beams, which are 300, 400, 500 or 600 μm -long.

In addition to devices with electrostatic actuation mechanisms, devices with parallel-beam thermal actuators were also designed and included to the fabrication layout as alternatives. There are again two variations related to the thermal actuators: number and dimensions of cantilever beams.

There are devices with two-beam actuators, where tips can only be closed, as well as ones with three-beam actuators, which enable both opening and closing actions. Devices with three-beam actuators are more suitable for both manipulation and testing cases since they enable force-feedback.

Finally, there are actuators with 3, 4 or 5 μm -wide cantilever beams, which are 100, 200, 300 or 400 μm -long. Note that, width of the wider beam in a two-beam structure is equal to three times that of the thinner one.

8.3. Fabrication

Since the fabrication technique proposed in this thesis is a novel approach, various problems were encountered during the first fabrication batch. Although the majority of the processes were quite straightforward including optical lithography, electroplating and evaporation, most challenging steps were DRIE, used in etching of the crack initiation patterns into the substrate, and PECVD, used in the deposition of the sacrificial SiO₂ layer, which serves as a mold for nanowire fabrication.

Initially, PECVD recipe to be used in the sacrificial layer deposition was optimized by depositing SiO₂ films using different deposition parameters and performing stress measurements on the deposited films, both before and after repeated heat treatment steps. However, cracks were not achieved in the first trial performed using the optimized recipe, in which tensile stresses exceed 100 MPa even after first annealing step. Hence, it was concluded that, corners of the crack initiation grooves were not sharp enough to yield cracking. Hence, DRIE process was also improved by increasing process power and decreasing thickness of the photoresist mask used and successful cracking was achieved.

However, unexpected cracks formed initiating from corners of the crack termination grooves, which hindered propagation of the desired ones. This problem can be solved by rounding the corners of crack termination grooves in the layout of “Crack Initiation Mask” in future designs.

Furthermore, cracking was not as efficient as expected in nanowire test structures. This problem can be solved again by rotating the nanowire test structures in the layout of “Crack Initiation Mask”, so that triangular tips of these structures will point to 45° directions of the Si wafer. Hence, crack initiation will be enhanced and cracks will follow a straight path since crack propagation is more preferable along 45° directions. Another solution might be increasing the thickness of the sacrificial SiO₂ layer used.

After release of the first batch wafers, it was observed that, nano-scale end effectors were not etched to the desired length during “Cutting of Nanowire Ends” and hence, Ni etching time at this step should be optimized. Another solution to this problem might be eliminating Ni etch step completely and performing “Cutting of Nanowire Ends” by utilizing a focused ion beam (FIB) process instead.

And after release of some chips, which were diced from second batch wafers, it was observed that, successful integration of the nano-scale end-effectors with the actuator devices was not achieved in any of the chosen chips. This can be as a consequence of increased BHF etching time for further widening the crack molds during the “Preparation of a Layer for Integration” step.

Despite all problems mentioned above and even it was the first fabrication trial, successful integration of nano-scale end-effectors were achieved in the first batch wafers, which demonstrates that batch-compatible integration of nanostructures with MEMS devices is possible using the self-assembly based fabrication technique proposed in this thesis.

8.4. Characterization

Actuation and static characterization experiments were performed on devices without nano-scale end-effectors, in order to further investigate and characterize these nanostructures in the form of nanowires or nanoribbons.

Actuation data obtained for both electrostatically and three-beam thermally actuated devices were compared with the data calculated analytically and all results turned out to be in close agreement with the theory. However, not all design possibilities were characterized due to time limitations or problems related to testing equipment.

Static characterization results can be verified by extracting C-V and C-t curves of devices using HP4280A with an external pulse generator in an appropriate setup [69]. Furthermore, dynamic characterization and frequency analysis of the devices can also be performed using a gain phase analyzer such as HP 4194A [69].

Concluding, this thesis is a proof of availability of integration of nanostructures with MEMS devices in a batch compatible manner, using the proposed self-assembly-based fabrication technique. Furthermore, it has been quite useful in gaining a considerable knowledge and experience on micro- and nano-scale manipulation and fabrication techniques.

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Self-assembly-based batch fabrication of nickel–iron nanowires by electroplating

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Abstract

The reason behind the majority of difficulties encountered in the integration of nanoscale objects with microelectromechanical systems can almost always be traced back to the lack of batch-compatible fabrication techniques at the nanoscale. On the one hand, self-assembly products do not allow a high level of control on their orientation and numbers, and hence, their attachment to a micro device is problematic. On the other hand, top-down approaches, such as e-beam lithography, are far from satisfying the needs of mass fabrication due to their expensive and serial working principle. To overcome the difficulties in micro–nano integration, a batch-compatible nanowire fabrication technique is presented, which is based on fabricating nanowires using simple lithographic techniques and relying on guided self-assembly. The technique is based on creating cracks with a predetermined number and orientation in a thin SiO₂ coating on Si substrate, and then filling the cracks with an appropriate material of choice. After the SiO₂ coating is removed, nanowires remain on the Si surface as a replica of the crack network. The technique, previously confined to electroless deposition, is now extended to include electroplating, enabling the fabrication of nanowires of various alloys. As an example, arrays of NiFe nanowires are introduced and their magnetic behaviour is verified.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The progress in the field of integration of microelectromechanical systems (MEMS) with nanoscale features such as nanowires has been hampered so far by a lack of batch-compatible fabrication techniques. Nanoscale features are fabricated using either self-assembly-based techniques or top-down methods. Limiting the scope of the discussion to nanowires, available self-assembly techniques can be summarized as follows:

- Filling of porous media such as anodic alumina [1–3], ion track-etched polymers [4] or selectively etched diblock copolymers [5] with a second material using techniques such as electrochemical deposition, chemical vapour deposition or pressure injection;
- Vapour–liquid–solid (VLS) method or derivatives of it, where whisker growth takes place through precipitation at

the solid/liquid interface at a supersaturated alloy in the form of a nanodroplet [6–11];

- Coating of biological molecules such as peptides [12] or DNA [13–15] with metal or conductive polymers;
- Step-edge decoration on graphite surfaces [16];

Although these methods are successfully used to fabricate a variety of nanowires, they cannot provide the level of control on the directionality and the number of nanowires required for integration with MEMS. At present, these self-assembly products are integrated with micro structures using one of the following techniques:

- (1) Imparting directional growth into self-assembly by using external electrical fields [17] or selective deposition of nucleation sites [18],
- (2) Using conventional self-assembly and then removing nanowires from their fabrication sites, such as alumina templates. These nanowires are dispersed in an

appropriate medium, such as isopropyl alcohol. Dispersed wires are then aligned with respect to micro structures using electric [1] or magnetic [19] fields, microfluidic alignment [20], complementary surfaces with appropriate functionalization, for example, using DNA [13, 21, 22] or electrostatic attraction [23] and the Langmuir–Blodgett technique [24, 25] among many other methods. Sometimes amorphous carbon films are used to increase the adhesion between the nano extension and the main structure [26].

In the latter technique, micro structures and nanowires are fabricated separately and nanowires are attached to the micro structure using external fields or secondary forces, whereas in the first technique, the micro structure is fabricated first and nanowires are grown on top of the micro structure. It is clear that none of these solutions provide the required level of order. For example, placing a single nanowire at a particular location on a MEMS that would serve as a robotic arm or a manipulation tool is out of the scope of these techniques.

On the other extreme, of course, are the top-down methods which are used more frequently than self-assembly techniques due to the obvious reasons of perfect control on directionality and number of nanowires. Electron-beam lithography [27, 28], direct growth of nano extensions on MEMS using focused-ion-beam chemical vapour deposition [29] or electron-beam deposition [30, 31] are most widely used micro–nano integration techniques. Etching micron-level structures down to the nanoscale using focused ion beam is also reported [32]. However, no matter how precise the end-product turns out to be, the need to eliminate serial processes from the fabrication flow is crucial for mass production. It is clear that the ideal technique for micro–nano integration would involve a self-assembly-based bottom-up process for nanofabrication that is, at the same time, compatible with the philosophy of batch fabrication. On the one hand, this enables the fabrication of microscale features along with their interfaces with the macro world using well-known techniques such as photolithography and wire bonding, and on the other hand, an appropriately designed self-assembly method will realize the growth of nanoscale features on the micro device. In this way, a marriage between MEMS and nanofabrication can be accomplished within the boundaries of batch fabrication.

In this study, we present the results of a fabrication technique that is based on fabricating nanowires using simple lithographic techniques and relying on guided self-assembly. The technique relies on creating crack networks in a thin coating on Si, where the number and direction of cracks are predetermined. The cracks then serve as moulds to be filled with a second material. In principle, this technique is similar to SNAP, where, instead of cracks, selective etching of a superlattice results in a mould for parallel nanowires with a chosen periodicity [33, 34].

The fact that a variety of materials can be used, including NiFe, imparts a second aspect to the implications of the study in addition to facilitating micro–nano integration: made of a magnetic alloy, oriented nanowires themselves can be used as actuators and sensors when placed in an external magnetic field. Verification of the magnetic behaviour of NiFe nanowires will be given at the end of the paper after the fabrication technique is discussed and examples of resulting nanowire networks are presented.

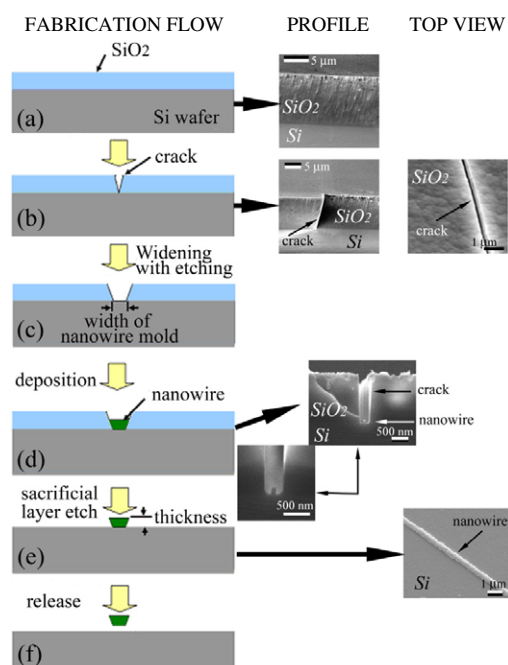


Figure 1. Fabrication process of nanowires and micrographs of resulting structures at each step: (a) deposition of a 5 μm -thick oxide layer; (b) formation of cracks by heat treatment; (c) HF etch of the cracks to obtain a wider and oxide-free plating base; (d) electroplating of NiFe in the nano moulds; (e) oxide strip by HF etch; (f) KOH etch for final release of the devices. Note: scanning electron micrographs are added for descriptive purposes. They do not necessarily belong to the same batch.

2. Experimental method

The fabrication technique based on electroplating is illustrated in figure 1. A thin sacrificial layer is deposited on Si substrate, which develops tensile stresses upon appropriate heat treatment. When tensile stresses are high enough, they lead to fracture in the thin film. These cracks are then filled with a second material. When the sacrificial layer is removed, a replica of the crack network is obtained.

This crack network would be of little use if the location of cracks and their orientation cannot be determined *a priori*. It is indeed observed that in the absence of any intervention, cracks follow the (100) orientation of the underlying Si wafer, as shown in figure 2 for a plasma-enhanced chemical vapour deposited (PECVD) SiO_2 film, and their location and number are completely random. Similar behaviour is also observed for other films on Si, including xerogel silica [35]. As a consequence, a successful integration with MEMS cannot be realized as is the case with similar fracture studies [36].

Therefore, when the method was first introduced [37], it was emphasized that crack paths can indeed be dictated by etching (i) sharp corners as crack initiation sites and (ii) free edges in the form of deep trenches for crack attraction sites within Si, prior to sacrificial layer deposition, as seen in figure 2. This patterning can be carried out by conventional photolithography. Upon sacrificial layer deposition and thermal treatment, a network of nanoscale cracks evolves guided by stress distribution due to this simple, microscale

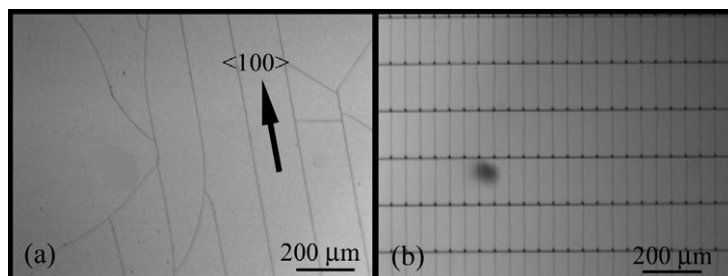


Figure 2. Effect of patterning. (a) Micrograph showing an unpatterned sample where the crack network is highly influenced by the anisotropy of the underlying substrate. Cracks in SiO₂ follow the $\langle 100 \rangle$ orientation of the Si substrate. Si, having the minimum stiffness along this direction, allows cracks to maximize their widths, and thereby release the maximum amount of energy in the strained structure. (b) Micrograph showing the crack network of a patterned sample at the same magnification, where a high level of control on both the direction and number of cracks is visible. Cracks initiate at sharp corners and terminate at free edges both etched in Si prior to SiO₂ deposition.

patterning. The number and orientation of etched corners and trenches determine the final distribution of cracks.

The surface density of nanowires is limited by stress effects. First, if two cracks are brought too close to each other, the stress states around them will be disturbed due to the existence of the neighbouring crack, and as a result, they will divert from their original paths. The 50 μm distance between cracks in figure 2(b) is sufficient to screen cracks from this effect. In our studies, we observed that reducing crack spacing from 50 μm down to 25 μm does not divert cracks within the first 30 μm of their trajectory, after which secondary cracks take a turn and meet already existing cracks perpendicularly.

The second aspect, regarding the density of nanowires is concerned with the question of how close a crack can be initiated next to an existing one where the energy of the strained medium is already released. Apart from keeping the straight trajectory, this aspect is concerned with the fundamental limitations, which is not studied further here. It is to be noted that for integration purposes with MEMS, the length scale in the first aspect (25–50 μm) is satisfactory. The fundamental limit would be of interest if one tries to fabricate a diffraction grating or a nanomechanical resonator with this technique.

In this study, Si in the form of 4 in-diameter, 500–550 μm -thick, n-doped, 0.1–0.5 $\Omega\text{ cm}$ resistivity $\langle 100 \rangle$ wafers is used as the substrate. The patterns of crack initiators and terminators are etched to a depth of 10 μm using inductively-coupled plasma deep reactive ion etching (ICP-DRIE). SiO₂ deposited using the PECVD technique is chosen as the sacrificial layer due to the ease of altering SiO₂ chemistry and the reasonably well understood mechanism of tensile stress generation [38] and fracture [39]. Deposition conditions of silicon dioxide are reported elsewhere [37]. Heat treatment is carried out at 400 °C for 20 min under nitrogen flow. The occurrence of cracking is observed to be almost 100%, i.e. each crack initiator is observed to lead to cracking. As a novelty, electroplating without any seed layer is introduced for filling cracks as opposed to electroless Ni deposition that was used previously [37]. This improvement enables the fabrication of nanowires of various alloys, such as NiFe, where magnetic properties can be controlled by changing deposition parameters, which again is not possible with electroless deposition. The sacrificial SiO₂ layer also serves as

a natural mask for electrodeposition without raising the need for subsequent lift-off.

After annealing, cracks are observed to initiate at sharp corners terminating at free edges. From a process optimization point of view, the sharpness of the corners of the crack initiation sites is an important issue for the success of the technique. For this purpose, a high-power RIE recipe is necessary in order to achieve anisotropic etching and eliminate round corners. In addition to the RIE parameters, the sharpness can also be retained by using a thinner resist because it helps both in exposure and development processes. However, it should be kept thick enough to survive the RIE process. On the other hand, as the thickness of the sacrificial oxide layer increases, tensile stresses induced due to annealing also increase and crack initiation is facilitated further [40]. If oxide thickness exceeds the depth of the crack initiation sites, no cracking will be observed. The effect of the depth of crack initiation sites is not studied further and it is kept constant at 10 μm .

After cracking, back side of the wafer is masked by a 0.2 μm -thick blanket resist layer to prevent deposition of a NiFe permalloy film on this side. Since the width of the cracks is on the order of a few nanometers at the SiO₂/Si interface, the cracks are widened to a desired dimension by wet etching in hydrofluoric acid (HF) just before electroplating. Etching also helps create an oxide-free plating base for the deposition step. Electrodeposition is performed using a standard permalloy bath [41]. Saccharine is added to the electrolyte to reduce residual stress which may lead to buckling of the nanowires. During deposition Si walls of etched patterns are also covered with NiFe, acting as anchors for the nanowires. After deposition, the remaining oxide layer is completely removed by wet etching in HF. Finally, the nanowires are released by KOH etching of the Si from underneath.

3. Nanowire networks

Figure 3 shows scanning electron microscopy images of the resulting nanowire network and single nanowires before being released. Nanowires are well aligned following the original crack pattern shown in figure 2. They are 250 μm long, and they have a periodicity of 50 μm . Figure 4 shows the atomic force microscopy results of the same network. The heights of

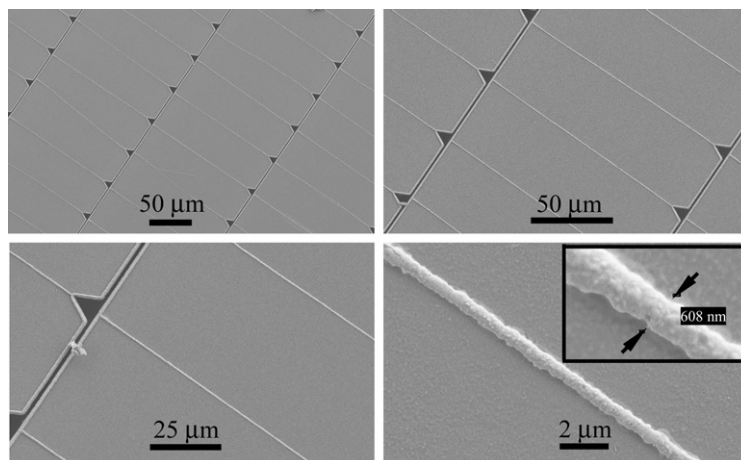


Figure 3. Scanning electron micrographs of NiFe nanowire networks with close-up views of single nanowires. The crack network of figure 2 is replicated here with metallic lines. $10\ \mu\text{m}$ -deep, ICP-DRI etched triangular crack initiators and crack terminators, in the form of deep trenches, are visible.

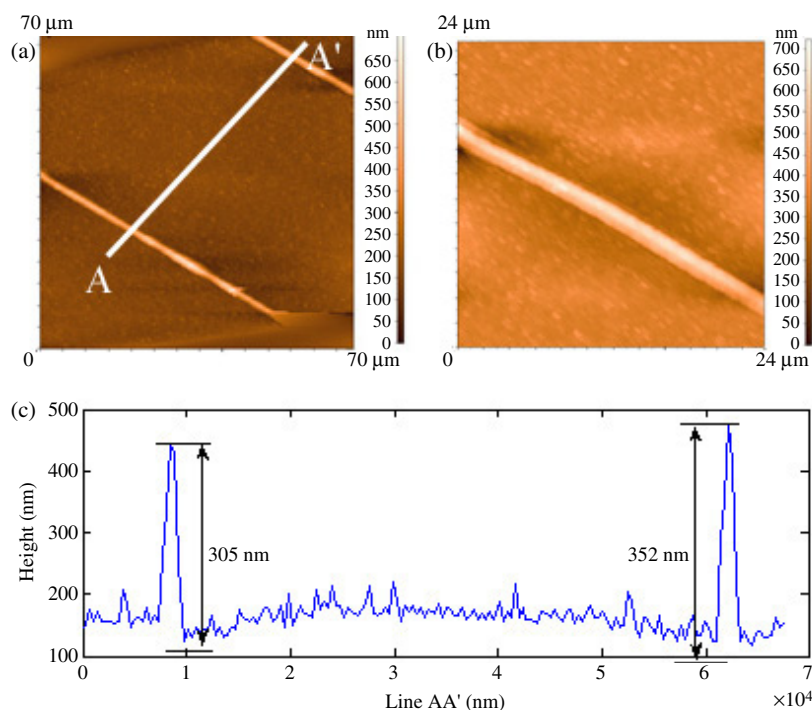


Figure 4. (a) AFM image of two nanowires. (b) Blow-out view of the nanowire on the left. (c) Surface profile along the line AA'.

both nanowires in the figure are of the order of 300 nm as a result of a 1 min deposition.

Nanowires with widths down to 100 nm were previously fabricated with this method using electroless deposition [37]. The width of the nanowires is, of course, determined by the width of the nanowire mould, i.e. the amount of the exposed silicon surface at the crack bottom, and the width of the oxide mould opening at the top. These dimensions depend on the amount of wet etching of the sacrificial oxide layer carried out before the electroplating step. On the other hand, the fundamental limitation of the process is related to the question of how small an opening can be filled with a crystalline material. Depending on the size of the opening and the type

of material, there is a critical length scale beyond which the normal nucleation and diffusion process for crystal formation is interrupted, and discontinuities appear along the nanowires. This critical size is measured to be 7 nm for electroplated gold [42]. It should be possible to reach similar dimensions with cracking, as demonstrated by a nanowire growth study in cracks in Teflon-AF films on graphite [36].

Similarly, the thickness variation exhibited by AFM measurements in figure 4 is not related to any fundamental phenomenon, but to experimental limitations and details of the electroplating process. As all deposition work is carried out at chip level, sample dimensions barely exceeded 4 mm by 4 mm, and electrical contact was established at one spot

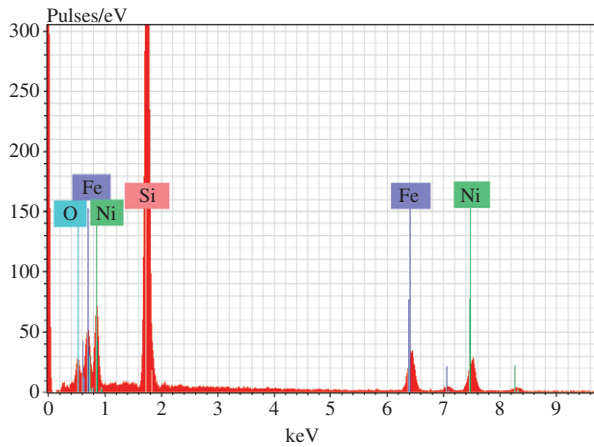


Figure 5. EDS point analysis of a nanowire showing elements existing in the structural layer material. Si and O are due to the surrounding sacrificial layer and the substrate.

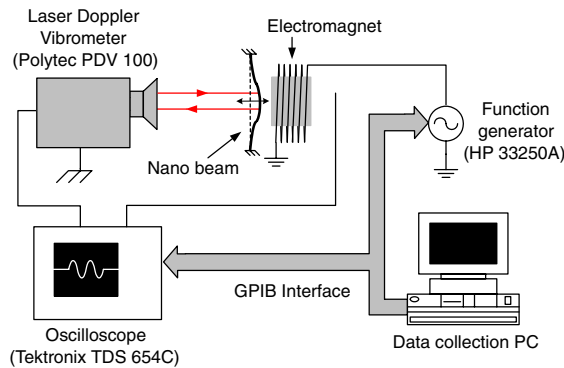


Figure 6. Mechanical characterization setup. The deflections of nanowires under an external magnetic field are picked up by a laser Doppler vibrometer (LDV). A laser spot size of $30\ \mu\text{m}$ ensures that deflection data is collected from a single nanowire.

only. Under these conditions, obtaining a uniform electric field over the entire chip is very difficult. A possible solution to enhance the uniformity of nanowire thickness would involve working at wafer level with multiple contact points, and using a current thief, i.e. an extra dummy cathode for obtaining a uniform electric field near the edges.

EDS results in figure 5 indicate that the atomic Ni/Fe ratio for the nanowires is about 3 at a current density of $40\ \text{mA cm}^{-2}$. Before we proceed with KOH release and measurement of the resulting magnetic behaviour of nanowires, let us mention that the optimization of plating parameters is important for tailoring the constitution of the nanowire material. To reach optimum plating conditions, an exact calculation of the exposed Si area should be carried out in addition to using a current thief. The Si area to be calculated includes the side walls of crack initiation sites in addition to Si exposed at the bottom of cracks. This way the required current corresponding to the ideal current density can be determined. The relation between deposition parameters and the resulting magnetic behaviour is left for further study.

4. Characterization of nanowires

Mechanical behaviour of the nanowires is characterized through a clamped–clamped (CC) nanobeam, which is actuated using an electro coil. Vibration of the beam is detected by a laser Doppler vibrometer (LDV). The LDV can measure the velocity of the point where the laser beam is focused, and it has a minimum laser spot size of $30\ \mu\text{m}$, which allows one to focus on a single nanowire. The electro-coil induces a magneto motive force (mmf) on the device, and as the structural material of the nanowire is magnetic, the mmf is translated into a magneto static force. This magneto static force is used to deflect the nanobeam in the out-of-plane direction. The magneto static force is proportional to the product of the mmf (and therefore the magnetic field), the magnetization of

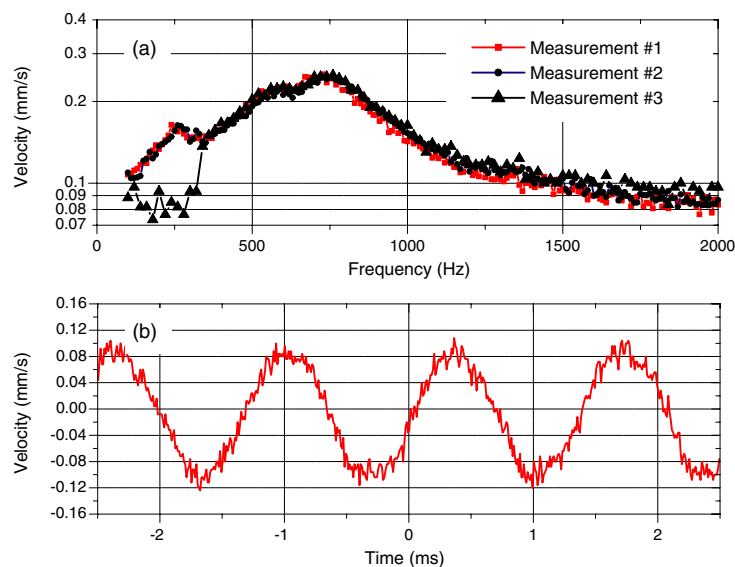


Figure 7. LDV characterization results of a clamped–clamped nanobeam (a) Force-to-velocity transfer function of the device with a frequency varying magnetostatic actuation. (b) Velocity response of the device to a magnetostatic excitation force at 740 Hz.

the permalloy, and the volume of the nanobeam [43]. When the frequency of the magneto motive force is in vicinity of the pass-band of the resonance peak, mechanical quality-factor-amplified vibrations are observed.

Figure 6 shows the details of the experimental setup used for the mechanical characterization of the device. A function generator driven electro-coil excites the nanobeam by inducing a frequency-dependent magneto static force. Both the function generator and oscilloscope are controlled by a custom computer program through a general purpose interface bus (GPIB, IEEE 488) communication interface. Figure 7(a) shows the mechanical transfer function of the beam, where three different measurements are plotted in the same graph. The transfer function relates the velocity of the nanobeam to the excitation force, and can be approximated to the response of a second-order band-pass filter transfer function. The average peak-to-peak displacement of the nanobeam at the fundamental resonance is measured as 50 nm. Figure 7(b) is a typical time response of the single CC nanobeam to a sinusoidal electromagnetic excitation force at 740 Hz. Due to the tiny width of the nanobeam (~ 600 nm), only a fraction of the laser spot ($0.6 \mu\text{m} \times 30 \mu\text{m}$ out of the circular spot with a diameter of $30 \mu\text{m}$) is used to obtain the signal, which leads to measurement noise in the sinusoidal response.

5. Conclusion

Using the example of nanowires, it is shown that batch-compatible fabrication for nanoscale objects is possible with serious consequences regarding the progress in the integration of microelectromechanical systems with nanoscale extensions. The technique eliminates the drawbacks of both self-assembly-based and top-down approaches by using simple lithography and guided self-assembly in the fabrication of nanowires, which allows one to decide the number and orientation of nanowires on the chip. Furthermore, the fact that the technique is based on electroplating facilitates the use of various alloys in nanowire fabrication with the possibility of tailoring their constitution for property optimization. The technique is demonstrated with NiFe as the nanowire material, and the resulting magnetic behaviour is verified by actuating free-standing nanowires.

Acknowledgments

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Batch Fabrication of Self-assembled Nickel-Iron Nanowires by Electrodeposition

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Abstract— Lack of batch-compatible fabrication techniques can be considered as the most important challenge in the integration of nanostructures with microelectromechanical systems (MEMS). A solution to the micro-nano integration problem is offered by introducing a batch-compatible nanowire fabrication technique based on basic lithographic techniques and guided self-assembly. The basic principle is obtaining cracks at predetermined locations in a sacrificial SiO₂ layer on Si and filling these cracks with a suitable metal by electrodeposition. The technique is demonstrated by using Nickel-Iron as the deposition material and verifying the magnetic behavior of resulting nanowires.

Keywords—nanofabrication; nanowires; electroplating; micro-nano integration; batch-compatibility; guided self-assembly

I. INTRODUCTION

The absence of batch-compatible fabrication techniques for nanoscale objects is the major challenge faced by researchers working on micro-nano integration issues. Techniques used in the fabrication of nanostructures utilize either top-down techniques or bottom-up approach mainly based on self-assembly. Due to inadequate control over the orientation and number of nanoscale objects, bottom-up approach does not facilitate integration with MEMS structures. On the other hand, top-down approach yields highly precise end products, however, none of them is compatible with batch fabrication due to serial processing philosophy.

We present important improvements in our self-assembly-based nanowire fabrication method, enabling future integration of MEMS with nanometer-scale extensions in a single batch process. When the method was first reported in MEMS 2003 [1] and 2004 [2], it was based on creating cracks in a sacrificial plasma-enhanced chemical vapor deposited (PECVD) SiO₂ layer on Si and filling them with electroless Ni. In principle, it is similar to (SNAP) process, where, instead of a cracked sacrificial layer, a selectively-etched superlattice is used [3].

Since cracks arrest at SiO₂/Si interface, they serve as nanometer-scale molds, and SiO₂ layer is a natural mask for electroless deposition. Upon removal of the sacrificial SiO₂, nanowires are observed at crack sites. Furthermore, the number and direction of cracks can be imposed by simple photolithography allowing nanofabrication with microscale patterning. As a novel feature, the method is now extended to include electroplating technique without using any metallic seed layer between Si and SiO₂. This enables one to fabricate nanowires with various alloys, such as NiFe, where magnetic properties can be controlled by changing deposition parameters, which is not possible with electroless deposition. In this work, the fabricated NiFe nanowires are released as

clamped-clamped (CC) nanobeams and the nanobeams are electromagnetically actuated for mechanical characterization.

II. EXPERIMENTAL METHOD

Basic idea behind the self-assembly based fabrication technique, illustrated in Fig. 1, is obtaining cracks in a thin sacrificial layer due to thermally induced internal stresses and using these cracks as molds for nanowire fabrication. Upon the removal of the sacrificial layer, nanowires in the form of the replica of the crack network remain on the substrate surface.

Crack propagation in the SiO₂ film is observed to take place along <100> direction of the underlying Si substrate. However, it is possible to control the position and orientation of cracks by etching grooves - with either sharp corners for crack initiation or flat surfaces for crack attraction - into the substrate before the sacrificial layer is deposited [4]. This can be accomplished by using conventional optical lithography and Inductively-Coupled Plasma Deep-Reactive Ion Etching (ICP-DRIE) for patterning and etching, respectively. After carrying out the appropriate heat treatment following sacrificial layer deposition, cracks are observed to initiate at sharp corners and terminate at flat edges. Hence, crack paths can be guided by this simple micro-scale patterning, and position, orientation and the number of the resulting cracks can be predetermined.

III. FABRICATION

Fabrication process, illustrated in Fig. 1, starts with a low-resistivity (0.1-0.5 Ωcm) n-doped <100> Si wafer, which is 500-550 μm-thick and 4-inch in diameter. First step is the etching of crack initiation and termination patterns, in the form of 10 μm-deep grooves, into Si substrate via ICP-DRIE. Then, a 5 μm-thick SiO₂ layer, with an appropriate chemistry [4], is deposited on the substrate surface as the sacrificial layer. PECVD technique is chosen for this purpose due to the ease of altering SiO₂ chemistry by manipulating deposition temperature, RF power and gas flow rates. Deposition recipe for the sacrificial SiO₂ layer is reported elsewhere [4]. A 20-minute heat treatment at 400°C under nitrogen flow yields crack initiation from sharp corners of the crack initiation patterns. These cracks propagate in a straight manner and terminate at flat surfaces. The sacrificial SiO₂ layer acts as a natural mask for nanowire fabrication, eliminating the need for subsequent lift-off.

Instead of electroless deposition technique utilized previously [4], electroplating without any use of a seed layer is introduced as an inventive achievement, which enables the fabrication of nanowires of various alloys with the possibility

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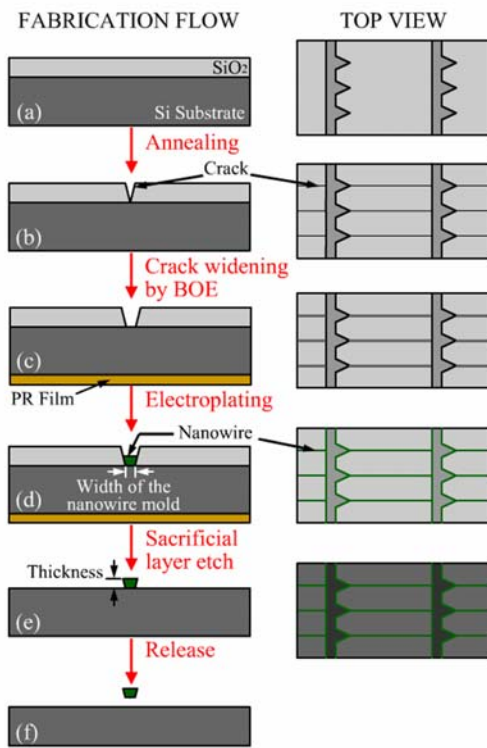


Figure 1. Fabrication process for the nanowires: (a) Deposition of a 5 μm -thick PECVD SiO₂ layer, (b) crack formation by heat treatment, (c) widening of the cracks by wet etching in HF, (d) electroplating of NiFe nanowires into crack molds, (e) removal of the sacrificial SiO₂ layer in HF, (f) release of the clamped-clamped nanobeams by KOH etch.

of changing their composition simply by altering deposition parameters. For example, nanowires with desired magnetic properties can be fabricated as in the case of NiFe.

One issue related to process optimization is the sharpness of the corners of the crack initiation sites, which is essential for the efficiency of the technique. A high-power RIE recipe leads to a more anisotropic etching and thus sharper corners. Furthermore, decreasing the thickness of the photoresist film used at the lithography step as much as possible enhances accuracy of the features due to improved exposure and development.

Increasing the thickness of the sacrificial SiO₂ layer further enhances the thermally induced tensile stresses [5] and crack initiation consequently. However, it should be noted that, SiO₂ thickness must not exceed the depth of the grooves determining the crack initiation. In this study, the oxide thickness and the depth of the reactive ion etched grooves are kept constant at 5 μm and 10 μm , respectively.

Following crack formation, a thin layer of photoresist film is spun on the back side of the wafer in order to prevent any metal deposition here. Crack-width is estimated to be on the order of a few nanometers at the Si/SiO₂ interface, initially. Hence, they should be widened in a 5% hydrofluoric acid (HF) solution just before electroplating is carried out. This wet etching process also removes any native oxide on the Si surface at the crack

bottom and provides an oxide-free plating base for the deposition step. The width of the resulting nanowires can be varied by controlling this initial HF etch-time.

A standard Permalloy bath [6] is utilized for the electroplating of nanowires. Any residual stress, which may lead to distortion of the nanowires after release, may be eliminated by the addition of saccharine into the electrolyte solution.

After the removal of the sacrificial SiO₂ layer in 5% HF solution, nanowires are completely released by wet etching of the underlying Si layer in a KOH solution at 60°C. NiFe deposited on the walls of the reactive ion-etched grooves act as anchors, resulting in clamped-clamped “nanobeams” after release.

IV. NANOWIRE NETWORKS

Scanning electron microscopy (SEM) images of a nanowire network, which is the replica of the crack pattern shown in Fig. 2(a), can be seen in Fig. 2(b). Nanowires are 160 μm -long and periodicity of the network is 50 μm . Fig. 3 shows SEM images a close-up view of the nanowire network and a single nanowire from this network with different magnifications. The width of nanowires is determined by the width of crack molds, which depends on the duration of wet etching of the sacrificial SiO₂ layer in HF before electrodeposition. Fabrication of nanowires with widths down to 100 nm using electroless deposition was previously reported [4].

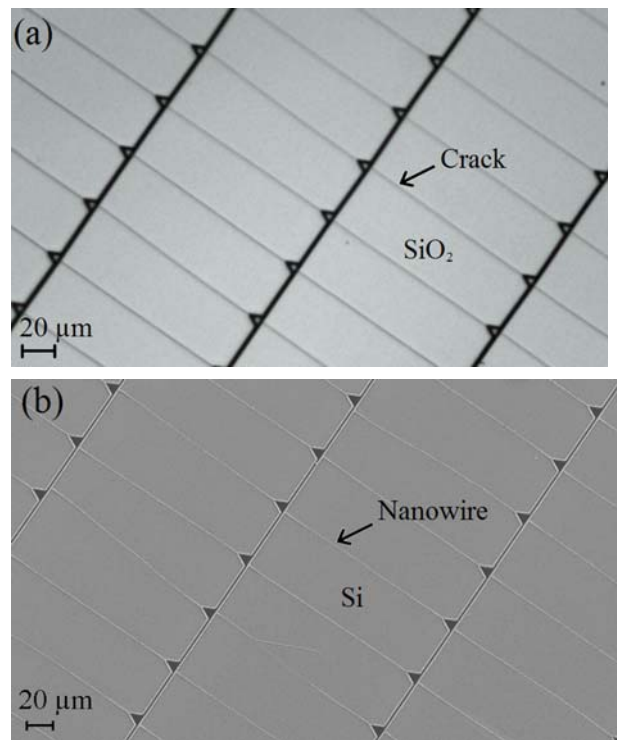


Figure 2. (a) Optical image of the crack array before electrodeposition. (b) SEM image of the nanowire network after removal of the sacrificial SiO₂ layer

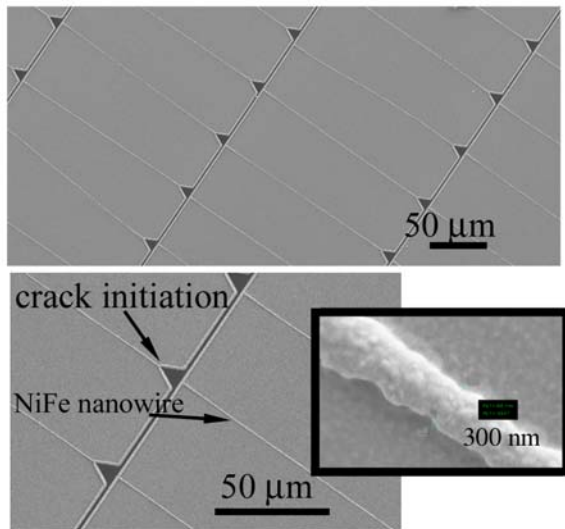


Figure 3. SEM images of various magnifications showing a close-up view of the nanowire network of Fig. 2 (b), with 10 μm -deep DRI-etched trenches for crack initiation and termination visible and a close-up view of a single nanowire.

The fundamental limit for the minimum width is related to the minimum gap-size that can be filled with a crystalline material together with the type of this material. There exists a critical length scale beyond which crystal formation due to normal nucleation and diffusion processes is interrupted resulting in discontinuities along nanowires. This critical size is measured as 7 nm for electroplated Au [7] and dimensions reached with cracking are on the same order, as reported in the study with cracks in Teflon-AF films on graphite [8].

Similarly, the thickness of the nanowires depends on the electrodeposition time. Fig. 4 shows the atomic force microscopy result of a single nanowire, with a 300 nm thickness obtained after a 1-minute NiFe deposition.

EDS results indicate that the atomic Ni/Fe ratio for the nanowires is 3:1 at a current density of 40 mA/cm². Before further proceeding with the release and characterization of the nanowires, it should be noted that optimization of the plating parameters is essential for monitoring the properties of the nanowire material. For this purpose, total Si area that is exposed should be calculated, including both crack bottoms and the side walls of the grooves determining the crack initiation and termination sites, and corresponding amount of current for the ideal current density should be determined accordingly. The effect of deposition parameters, as current density and time, on the resulting magnetic behavior is left for a further study.

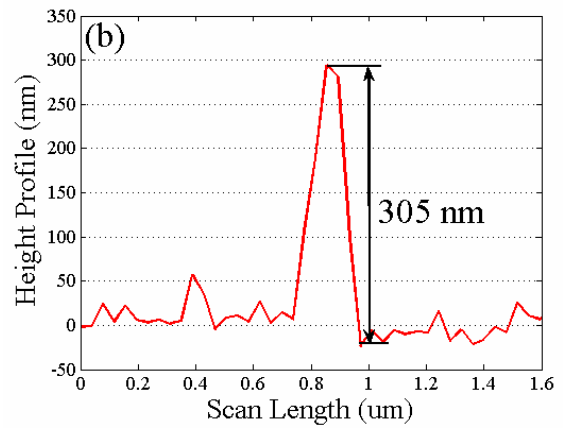
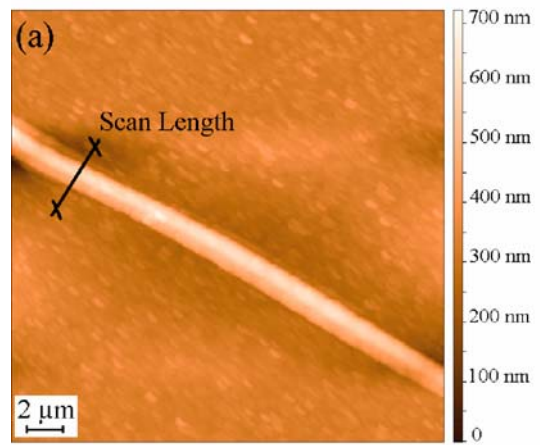


Figure 4. (a) Atomic force micrograph of a single nanowire (b) Surface profile along the scan line shown in (a).

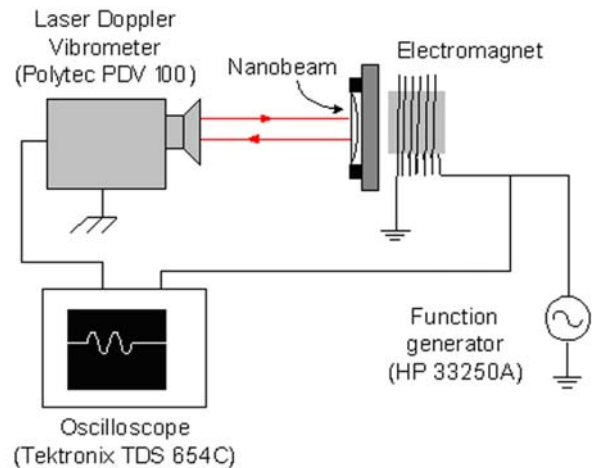


Figure 5. Mechanical characterization setup. The deflections of nanowires under an external magnetic field are picked up by a laser Doppler vibrometer (LDV). A laser spot size of 30 μm ensures that deflection data is collected from a single nanowire.

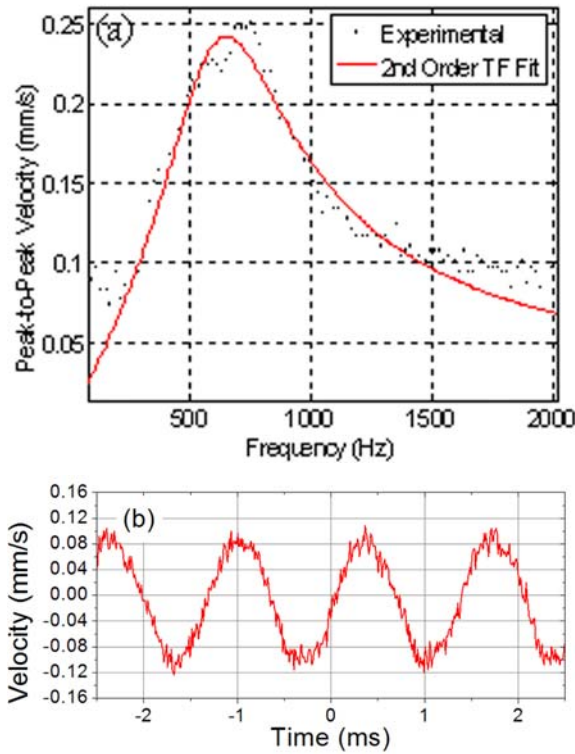


Figure 6. LDV characterization results of a CC nanobeam (a) Force-to-velocity transfer function. (b) Velocity response to an electromagnetic excitation force at 740Hz.

V. CHARACTERIZATION

Characterization of the fabricated clamped-clamped beam is performed by utilizing magneto static actuation and optical detection method. Since the structural material of the device is magnetic, a time varying magnetic force can be exerted on the device to create mechanical vibrations. In order to create an out-of-plane magnetic actuation force, a current controlled electro coil is placed beneath the device. By sweeping the frequency of the current, therefore the induced magneto motive force (mmf), and detecting the mechanical vibrations with a laser Doppler vibrometer (LDV), frequency spectrum of the mechanical deflection can be obtained. The LDV measures the vibration velocity of the point where its laser is spotted. When the frequency of the actuation signal approaches to the mechanical resonance of the device, velocity of the device increases according to the second order (spring-mass-dashpot) system response.

Fig. 5 sketches the experimental setup used for dynamic mechanical characterization. In the setup, electro-coil is driven by the PC controlled function generator, and can form a frequency-dependent magneto static force on the nanobeam. Vibration of the beam is sensed by the LDV and translated into an electrical signal and monitored by an oscilloscope.

The mechanical transfer function of the beam is shown in Fig. 6(a). The transfer function relates the velocity of the nanobeam to the excitation force, and can be approximated to the response of a second-order band-pass filter transfer function.

The average peak-to-peak displacement of the nanobeam at the fundamental resonance is measured as 50 nm. Fig. 6(b) is a typical time response of the single CC nanobeam to a sinusoidal electromagnetic excitation force at 740 Hz. The tiny width of the nanobeam (~600 nm) effects the quality of the read-out signal, since only a fraction of the laser spot ($0.6 \mu\text{m} \times 30 \mu\text{m}$) out of the circular spot with a diameter of $30 \mu\text{m}$ is used to obtain the signal.

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