ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

PhD THESIS

Mehmet Uğraş CUMA

DIGITAL SIGNAL PROCESSOR BASED IMPLEMENTATION OF CUSTOM POWER DEVICE CONTROLLERS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ADANA, 2010

ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

DIGITAL SIGNAL PROCESSOR BASED IMPLEMENTATION OF CUSTOM POWER DEVICE CONTROLLERS

Mehmet Uğraş CUMA

PhD THESIS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

We certify that the thesis titled above was reviewed and approved for the award of degree of the Doctor of Philosophy by the board of jury on 12/08/2010.

…….....	……..	…….....
Prof. Dr. Mehmet TÜMAY	Prof. Dr. Tankut YALÇINÖZ	Assoc.Prof.Dr. İlyas EKER
SUPERVISOR	MEMBER	MEMBER
...…….....	...……..	
Assoc.Prof.Dr. Ulus ÇEVİK	Asst.Prof.Dr. Kamil Çağatay BAYINDIR	
MEMBER	MEMBER	

This PhD Thesis is written at the Department of Electrical and Electronics Engineering of Institute of Natural and Applied Sciences of Çukurova University.

Registration Number:

Prof. Dr. İlhami YEĞİNGİL
Director
Institute of Natural and Applied Sciences

ABSTRACT

PhD THESIS

DIGITAL SIGNAL PROCESSOR BASED IMPLEMENTATION OF CUSTOM POWER DEVICE CONTROLLERS

Mehmet Uğraş CUMA

ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Supervisor :Prof. Dr. Mehmet TÜMAY
Year: 2010, Pages: 218
Jury :Prof. Dr. Mehmet TÜMAY
:Prof. Dr. Tankut YALÇINÖZ
:Assoc. Prof. Dr. İlyas EKER
:Assoc. Prof. Dr. Ulus ÇEVİK
:Asst. Prof. Dr. Kamil Çağatay BAYINDIR

Custom power can be explained as the power supplied to the customers who do not tolerate any power quality problems that may occur in supplied power using custom power devices. Dynamic Voltage Restorer (DVR) is one of the custom power devices that is connected in series to the system. DVR detects the voltage sags and injects missing portion of voltage to the load. By this way, the load is not affected by voltage sags on the supply. Another custom power device is the Static Transfer Switch (STS) that transfers the supply of the voltage sensitive loads of customers who have two different feeders. When a sag or interruption occurs on one of the feeders, the loads are transferred to the healthy feeder in the shortest time possible. Shunt Active Power Filter (SAPF) is used to eliminate the current harmonics. The purpose of SAPF is to minimize the harmonic level of the source current by generating the harmonics required by the non-linear loads.

Power electronics switching devices are widely used in the realization of custom power devices such as DVR, STS and SAPF. To control the power electronic equipments, controller design and development are needed. In this study, the controllers of DVR, STS and SAPF are designed, developed and implemented using Digital Signal Processors (DSP). A new sag detection and voltage compensation method is proposed for the DVR. The sag detection algorithms are also applied to the control of STS. In the implementation of SAPF, the problems caused by the voltage unbalance in instantenous reactive power method are solved. The design of custom power devices are explained in detail. Control algorithms and codes developed are presented.

Key Words: Digital Signal Processor, Dynamic Voltage Restorer, Static Transfer Switch, Shunt Active Power Filter

ÖZ

DOKTORA TEZİ

ÖZEL GÜÇ CİHAZ KONTROLCÜLERİNİN SAYISAL SİNYAL İŞLEMCİ KULLANILARAK UYGULANMASI

Mehmet Uğraş CUMA

ÇUKUROVA ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ
ELEKTRİK ELEKTRONİK MÜHENDİSLİĞİ ANABİLİM DALI

Danışman :Prof. Dr. Mehmet TÜMAY
Yıl: 2010, Sayfa: 218
Jüri :Prof. Dr. Mehmet TÜMAY
:Prof. Dr. Tankut YALÇINÖZ
:Doç. Dr. İlyas EKER
:Doç. Dr. Ulus ÇEVİK
:Yrd. Doç. Dr. Kamil Çağatay BAYINDIR

Özel güç, sağlanan güçte oluşabilecek herhangi bir güç kalitesi problemine tahammülü olmayan müşteriler için özel güç cihazları kullanılarak sağlanan güç olarak açıklanabilir. Bu cihazlardan Dinamik Gerilim İyileştiricisi (DGİ), sisteme seri olarak bağlanmakta ve oluşabilecek gerilim düşümlerini tespit edip, eksik olan kısmı üreterek yüke sunmaktadır. Böylece yük, beslemede oluşan gerilim düşümlerinden etkilenmemektedir. Diğer bir cihaz, Statik Transfer Anahtarı (STA) olup iki farklı besleme hattına sahip müşterilere ait hassas yükleri besleme hattının herhangi birinde oluşabilecek gerilim düşümü veya kesilmeleri durumunda sorunsuz olan besleme hattına en kısa zamanda transfer edilmesini sağlamaktadır. Akım harmoniklerinin temizlenmesinde ise Paralel Aktif Güç Filtresi (PAGF) kullanılmaktadır. Bu cihaz harmonik oluşturan yükün ihtiyaç duyduğu harmonikleri üreterek, kaynak tarafından çekilen harmonikli akımı azaltmayı amaçlamaktadır.

DGİ, STA ve PAGF gibi özel güç cihazlarının gerçekleştirilmesinde güç elektroniği anahtarlama elemanları kullanılmaktadır. Güç elektroniği elemanlarını kontrol etmek için ise kontrolcü tasarımı ve geliştirilmesi gerekmektedir. Bu çalışmada DGİ, STA ve PAGF kontrolcülerinin Sayısal Sinyal İşlemciler kullanılarak tasarlanması, geliştirilmesi ve uygulanması gerçekleştirilmiştir. DGİ için yeni bir gerilim düşümü tespiti ve gerilim kompanzasyonu metodu önerilmiştir. STA'da da yeni gerilim düşümü metodunun uygulanması gösterilmiştir. PAGF'de anlık reaktif güç yöntemindeki gerilim dengesizliklerinin neden olduğu sorunlar giderilmiştir. Çalışmada özel güç cihazlarının tasarımı detaylı olarak anlatılmış ve geliştirilen kontrol algoritma ve kodları sunulmuştur.

Anahtar Kelimeler: Sayısal Sinyal İşlemci, Dinamik Gerilim İyileştiricisi, Statik Transfer Anahtarı, Paralel Aktif Güç Filtresi

ACKNOWLEDGEMENTS

I wish to express my sincere gratitude to my supervisor Prof. Dr. Mehmet TÜMAY for his guidance, encouragement and support during my studies. His leadership and motivation have been a source of inspiration and a model for me to follow.

I would like to thank Prof. Dr. Süleyman GÜNGÖR for his valuable suggestions and providing a good working environment.

I would like to thank Asst.Prof.Dr. Kamil Çağatay BAYINDIR his great support. His advices let me to finish this thesis.

I am very grateful to Prof.Dr. Tankut YALÇINÖZ, Assoc.Prof.Dr. İlyas EKER and Assoc.Prof.Dr. Ulus ÇEVİK for their endless support.

I am also grateful to Ahmet TEKE, Mehmet Emin MERAL, Adnan TAN and Lütfü SARIBULUT for their support and friendship.

I would like to thank and acknowledge the financial support from TÜBİTAK for our research project. This thesis is a part of the research project entitled as "Modeling and Implementation of Custom Power Park (106E188)" supported by Electrical, Electronics and Informatics Research Group of Scientific and Technological Research Council of Turkey. This project also supports two other PhD studies namely "Unified Power Quality Conditioner: Design, Simulation and Experimental Analysis" and "Voltage Quality Enhancement with Custom Power Park".

Dr. Alper TERCİYANLI never refused to help me during my studies and I am very appracited. His ideas are kindly welcome.

My wife Gaye and my daughter Günce are always supported and encouraged me, I am very grateful to them all times.

CONTENTS **PAGE**

LIST OF TABLES **PAGE**

LIST OF FIGURES **PAGE**

LIST OF SYMBOLS

BRK	Breaker
C_f	Filter capacitance
C_s	Snubber capacitance
CT	Current transducer
e(t)	The error signal
E_d	Nominal DC source voltage
F	Farad
f_o	Cutoff frequency
f_r	Fundamental frequency
f_s	Switching frequency
G_1	Gate signal for the first IGBT
h	Harmonic order
H	Henry
I_{aALT}	Alternate feeder phase A current
I_{aPREF}	Preferred feeder phase A current
I_{aRef}	Active filter reference current
I_c	Capacitor current
I_o	Load current
I_s	Source current
K	Filter factor
k	Modulation index
L_f	Filter inductance
M	Mega
m	milli
Mag(t)	Amplitude
ms	Milliseconds
PhA	Phase A
PhB	Phase B
PhC	Phase C

R_s	Snubber resistance
STS_a	Alternate side of the STS
Tr_A	Injection transformer for phase
u(t)	Input signal to the PLL
U_n	Nominal voltage
V_a	Phase A voltage
V_{ABalt}	Alternate feeder line to line AB voltage
V_{ABpref}	Preferred feeder line to line AB voltage
V_{alt}	Alternate feeder fault signal
V_b	Phase B voltage
V_c	Phase C voltage
V_d	d component of voltage
V_{DC}	DC offset voltage
V_{dif}	Real reference voltage for the PLL
V_{error}	Ideal reference voltage value for the PLL
V_o	Load voltage
V_{oav}	Total harmonic of the load V_o
V_p	Voltage phasor
V_{peak}	Peak value of voltage
V_{phase}	Phase voltage
V_{pref}	Preferred feeder fault signal
V_{pref_conv}	Preferred feeder fault signal with conventional method
V_{pref_prop}	Preferred feeder fault signal with proposed method
V_q	q component of voltage
V_{rms}	RMS value of voltage
V_s	Output voltage of the PWM inverter
VT	Voltage transducer
w_o	Angular frequency
x(t)	p.u. sinusoidal voltage output of the PLL
y(t)	Output of the PLL
Z_a	Load A impedance

ZC	Detection of zero current transition
α	Alpha component
β	Beta component
$\theta(t)$	Phase angle of the tracked signal
μ	Micro
Ω	Ohm

LIST OF ABBREVIATONS

AC	Alternating current
ADC	Analog to Digital Converter
APF	Active Power Filter
ASIC	Application Specific Integrated Circuit
CAP	Capture
CMPA	Counter-Compare A
CMPB	Counter-Compare B
CP	Custom Power
CPU	Central Processing Unit
DAC	Digital to Analog Converter
DC	Direct Current
DSP	Digital Signal Processors
DVR	Dynamic Voltage Restorer
EMTDC	Electromagnetic Transients for DC
ePWM	Enhanced Pulse Width Modulation
EV	Event Manager
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Arrays
GP	General Purpose
GPIO	General Purpose Input Output
IEEE	Institute of Electrical and Electronics Engineers
IRPT	Instantaneous Reactive Power Theory
MAC	Multiply and Accumulate
MIPs	Million Instruction Per Second
MM	Mathematical Morphology
PCB	Printed Circuit Board
PI	Proportional Integral
PLL	Phase Locked Loop

PQ	Power Quality
PU	Per Unit
PSIM	Power Simulator
PWM	Pulse Width Modulation
RISC	Reduced Instruction Set Computing
RMS	Root Mean Square
QEP	Quadrature Encoder Pulse
SAPF	Shunt Active Power Filter
SCI	Serial Communication Interface
SHEPWM	Selective Harmonic Elimination Pulse Width Modulation
SPI	Serial Peripheral Interface
STS	Static Transfer Switch
UPS	Uninterruptible Power Supplies
VSC	Voltage Source Converter
VSD	Variable Speed Drive
VSI	Voltage Source Inverter

1. INTRODUCTION

As commercial and industrial customers become more and more reliant on high quality and high reliability electric power, utilities have considered approaches that would provide different options or levels of "premium power" for those customers who require something more than what the bulk power system can provide. Recent surveys suggest that power quality and power reliability related events cost in lost productivity and profitability. These effects indicate a clear need to bridge the gap between what the electric power system can provide and the level of immunity to power disturbances that electronic equipment must be capable of withstanding (Dorr and Perry, 2003).

The term "custom power" has been coined to describe distribution system level power conditioning products. This is primarily because the market for these multi megawatt power conditioning solutions is nowhere near the size of the market for traditional facility level power quality and reliability, such as uninterruptible power supplies and surge protectors. The main custom power configurations are:

Dynamic Voltage Restorer provides ride through for sags by injecting a signal to offset the voltage lost during the sag. Backup stored energy provides ride through for sags and momentary interruptions by using stored energy.

Static Transfer Switch provides ride through for momentary interruptions and most voltage sags by quickly switching between two different utility feeders.

Reactive power and harmonic compensation devices, Active Power Filters provide dynamic compensation to the power system when temporary corrections are required to support varying loads and power system stability conditions.

Power electronics has already shown its importance as an indispensable solid-state technology for industrial process applications after decades of evolution and advance. The key element of power electronics is the control of the switching converters. The raw input power is processed under the controller and generates the desired output power. In general, power electronics controllers can be classified as analog controller and digital controller. Until now, the control of power converters is usually based on analog solutions. The main advantages of an analog solution are

low price and ease of use. With the development of the control techniques and algorithms, the control becomes more and more complex. Although there are still several analog commercial ICs for solving this type of control problems, the cost reduction and improving performance of a digital controller have made it an ideal solution for the power converter control applications. The digital controller can also reduce the designing time and has the following advantages (Zhang, 2006):

1. A digital controller can reduce the number of circuit elements. A digital controller can be integrated on a single chip which provides the same functions with analog counter part.

2. Since a digital controller reduces the number of auxiliary elements, the total cost of the controller is also reduced.

3. The compact structure of a digital controller helps to improve system reliability and to eliminate drift and electromagnetic interference problems. It appears to be both cost and time consuming for an analog controller to solve such problems (Zhang, 2006).

4. Digital control brings the flexibility of software. One can easily add or remove several features to a digital controller in a very short duration.

5. There are many software which can simulate the system environment and control block, for both the analog and digital controllers. But for the analog controller design, most supported software can only do simulation. Designers must rebuild the circuits with the simulation results. The design of digital controller is different. The simulation program can directly or easily be rearranged to the supported software and downloaded to the digital chip. It significantly saves the time of building the real circuit and also provides reliability for the controller performance through simulation results (Zhang, 2006).

6. Testing and debugging is much easier in digital circuits compared to analog ones.

As it is described above, the digital control is selected to control the custom power devices; Dynamic Voltage Restorer, Static Transfer Switch and Shunt Active Power Filter in this study. To implement a digital controller, there are several options that a designer can choose. Digital Signal Processors (DSP), Microcontrollers and

Field Programmable Gate Arrays (FPGA) are the most important ones. A DSP controller is chosen as it offer dedicated peripherals to control power electronic devices, C language optimized performance and well suited for extremely complex math intensive tasks as the control algorithms includes a lot of maths.

In Chapter 1, an introduction to the custom power and custom power devices is presented. Then digital control of the power electronic devices is investigated. The advantages of using the digital controllers are listed. Lastly, why a DSP is chosen to control these devices is explained.

Chapter 2 summarizes the power quality concept and most important power quality problems are discussed. The custom power devices that are implemented in the study are introduced. Their basic topology is pictured and simple expressions about their control are presented. Literature reviews about the DVR, STS and SAPF are given.

In Chapter 3, an introduction to controllers used in custom power devices is given. Two different DSP controllers used in this study are TMS320F2812 and TMS320F28335. The peripherals and control registers and use of these registers are described. A comparison is made between these controllers.

Chapter 4 deals with the implementation of DVR that injects the missing voltage to the load if sag occurs on the supply voltage. A new control algorithm based on enhanced Phase Locked Loop (ePLL) is proposed for both sag detection and voltage compensation. The proposed methods are validated through simulation and experimental studies. The simulations are performed using PSCAD/EMTDC program. The chapter also includes the experimental setup and results of the DVR.

In Chapter 5, the design and implementation of STS is performed. A STS is used to transfer the supply of a voltage sensitive load from one feeder to another one. The sag detection method proposed is also used in STS. The conventional and proposed sag detection methods are compared. Simulation and experimental results are given. The simulations are performed using PSCAD/EMTDC program.

Chapter 6 is reserved for the design and implementation of SAPF. The duty of the SAPF is to calculate the current harmonics and eliminate them by injecting a current reverse in phase and same in harmonic content. By this way, source currents

are filtered from the harmonics caused by nonlinear loads. Instantaneous Reactive Power Theory (IRPT) is used to generate the compensating currents and hysteresis current control is chosen to generate switching patterns. To remove the effects of source voltage harmonics and unbalances, one of the phase-to-phase source voltages is measured and a virtual voltage is generated in the DSP that is phase shifted. The simulation and experimental results for 220 V_{rms} and 380 V_{rms} line-to-line are given. The simulation cases are performed using PSCAD/EMTDC program.

In Chapter 7, conclusions on the DSP based control of DVR, STS and SAPF are given. The some recommendations for future work are also presented.

Tables in Appendix A summarize the basic features of TMS320F2812 and TMS320F28335 controllers.

Appendix B is reserved for the C code listing for DVR, STS and SAPF. B.1. is the C code of DVR, B.2. is the C code for STS and B.3. is the C code of SAPF.

In Appendix C, the circuit diagrams for signal conditioning board of SAPF are given.

2. INTRODUCTION TO CUSTOM POWER DEVICES

Custom Power Devices play an important role to solve the power quality problems. Before introducing these devices, it will be much better to summarize the power quality concept. Voltage sags, swells, harmonics and interruptions are the most severe disturbances faced in industry today.

All electrical devices are prone to failure or malfunction when exposed to one or more power quality problems. The electrical device might be an electric motor, a transformer, a generator, a computer, a printer, communication equipment or a household appliance. Power quality is a set of electrical boundaries that allows a piece of equipment to function in its intended manner without significant loss of performance or life expectancy (Sankaran, 2002).

Both electric utilities and end users of electric power are becoming increasingly concerned about the quality of electric power. There are four major reasons for the increased concern:

• Newer generation load equipment, with microprocessor-based controls and power electronic devices, is more sensitive to power quality variations than was equipment used in the past.

• The increasing emphasis on overall power system efficiency has resulted in continued growth in the application of devices such as high efficiency, adjustable speed motor drive and shunt capacitors for power factor correction to reduce losses. This results in increasing harmonic levels on power systems and has many people concerned about the future impact on system capabilities.

• End users have an increased awareness of power quality issues. Utility customers are becoming better informed about issues as interruptions, sags and switching transients and are challenging the utilities to improve the quality of power delivered.

• Many things are now interconnected in a network. Integrated processes mean that the failure of any component has much more important consequences (Dugan et al., 2002).

The electronic devices are very sensitive to disturbances such as voltage dips, voltage swells, interruption and harmonics as shown in Figure 2.1.

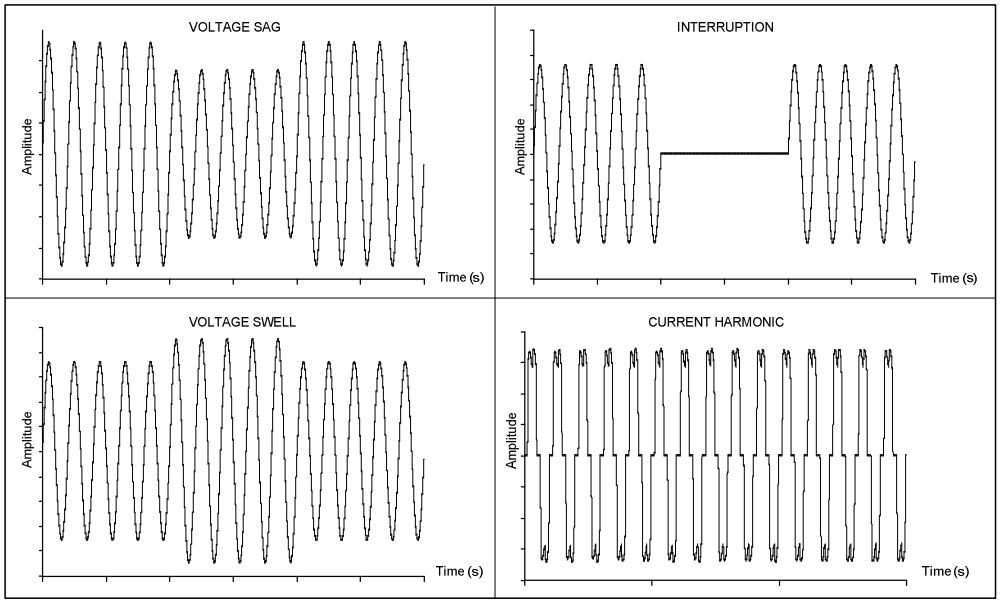

Figure 2.1. Most common types of power quality disturbances

Voltage sags are considered one of the most severe disturbances to the industrial equipments. The definition of voltage sag by IEEE Standards is as follows: voltage sag is a decrease of voltage or current in rms. at the rated frequency to the range between 0.1 per unit (pu) and 0.9 pu and lasting 0.5 cycles to 1 minute. Voltage sags are caused by faults on the transmission or distribution system or by switching of loads with large amounts of initial starting or inrush current such as motors, transformers and large dc power supply. Voltage sags can cause the following effects:

The equipment may be disconnected by a protective system or may operate in an improper manner. The economic consequences of such an event can be of considerable significance. They include loss of production, costs of restarting the technological process (this is particularly significant for continuous processes, where the time needed for restarting is, as a rule, very long), damaged

equipment and materials, delayed delivery, reduced customer satisfaction, a decrease in the power delivered to the user, etc (Baggini, 2008).

The definition of voltage swell by IEEE Standards is as follows: An increase in the rms voltage in the range of 1.1 to 1.8 pu for a duration greater than half a mains cycle and less than 1 minute. Voltage swells are caused by system faults, load switching and capacitor switching. Swells and over voltages can cause over heating tripping or even destruction of industrial equipment such as motor drives.

An interruption is defined as a reduction in the supply voltage or load current, to a level less than 0.1 pu for a time of not more than 1 minute. Interruptions can be caused by system faults, system equipment failures or control and protection malfunctions, hurricanes, tornadoes and ice storms, pole-line accidents and tree contact with power lines. Interruptions can cause tripping of protection devices, loss of information and malfunction of data processing equipment, stoppage of sensitive equipment, such as adjustable speed drives, personal computers and programmable logic controllers.

The proliferation of different nonlinear loads such as rectifiers and cyclo-converters has resulted in a variety of undesirable phenomena in power distribution systems. The most significant among these are voltage disturbances, unbalance, harmonic contamination and increased reactive power demands. Generally, current harmonics and asymmetries increase losses in AC power lines, transformers, rotating machines. Furthermore, harmonics and unbalance cause oscillatory torque, leading to mechanical stress and malfunctions in sensitive equipment, whereas transient disturbances interfere with the communication circuits.

Electronic equipments are very sensitive loads against harmonics because their control depends on either the peak value or the zero crossing of the supplied voltage, which are all influenced by the harmonic distortion (Devaraju et al., 2010). Harmonic load currents are generated by all non-linear loads. These include switched mode power supplies, electronic fluorescent lighting ballasts, small uninterruptible power supplies (UPS) units, variable speed drives, large UPS units. There are several common problem areas caused by harmonics such as overloading of neutrals,

overheating of transformers, nuisance tripping of circuit breakers, over-stressing of power factor correction capacitors and skin effect (Chapman, 2001).

In order to overcome these power quality problems such as voltage sags/swells, interruption and current harmonics, the concept of custom power devices is introduced recently. Custom power is a strategy, which is designed primarily to meet the requirements of industrial and commercial customer. The concept of custom power is to use power electronic or static controllers in the medium voltage distribution system aiming to supply reliable and high quality power to sensitive users (Devaraju et al., 2010). Power electronic valves are the basis of those custom power devices such as the static transfer switch, active filters and dynamic voltage restorer.

The term "Custom Power" is usually used to describe advanced technologies that can be applied to the utility system for improving the power quality delivered to end use customers (McGranaghan and Roettger, 2003). The concept of custom power is the employment of power electronic or static controllers in medium voltage distribution systems for the purpose of supplying a level of reliability and/or power quality that is needed by electric power customers sensitive to power quality variations. Custom power devices or controllers, include static switches, inverters, converters, injection transformers, master control modules and/or energy storage modules that have the ability to perform current interruption and voltage regulation functions in a distribution system to improve reliability and/or power quality (Sabin and Sannino, 2003).

Custom Power embraces a family of devices, which together make up a toolbox to provide power quality solutions at the distribution system voltage level (Taylor, 1995). These technologies include the DVR, APF, STS, Static Series Compensator and Distribution Static Compensator. Throughout the PhD study, the controllers for each of the following custom power devices were implemented using Digital Signal Processors:

- Dynamic Voltage Restorer
- Static Transfer Switch
- Shunt Active Power Filter

2.1. Review of Dynamic Voltage Restorer

Voltage sags and swells are vital power quality problems and the Dynamic Voltage Restorer is known as an effective device to mitigate voltage sags and swells (Errabelli et al., 2006). The Dynamic Voltage Restorer is a power electronic device that is used to inject three phase voltages in series and in synchronism with the distribution feeder voltages in order to compensate for voltage sag (Ramasamy et al., 2005).

The basic topology of the DVR that was examined is given in Figure 2.2. The AC source is feeding the load through the series injection transformers of the DVR. The power circuit of the DVR consists of three single phase H bridge IGBT inverters.

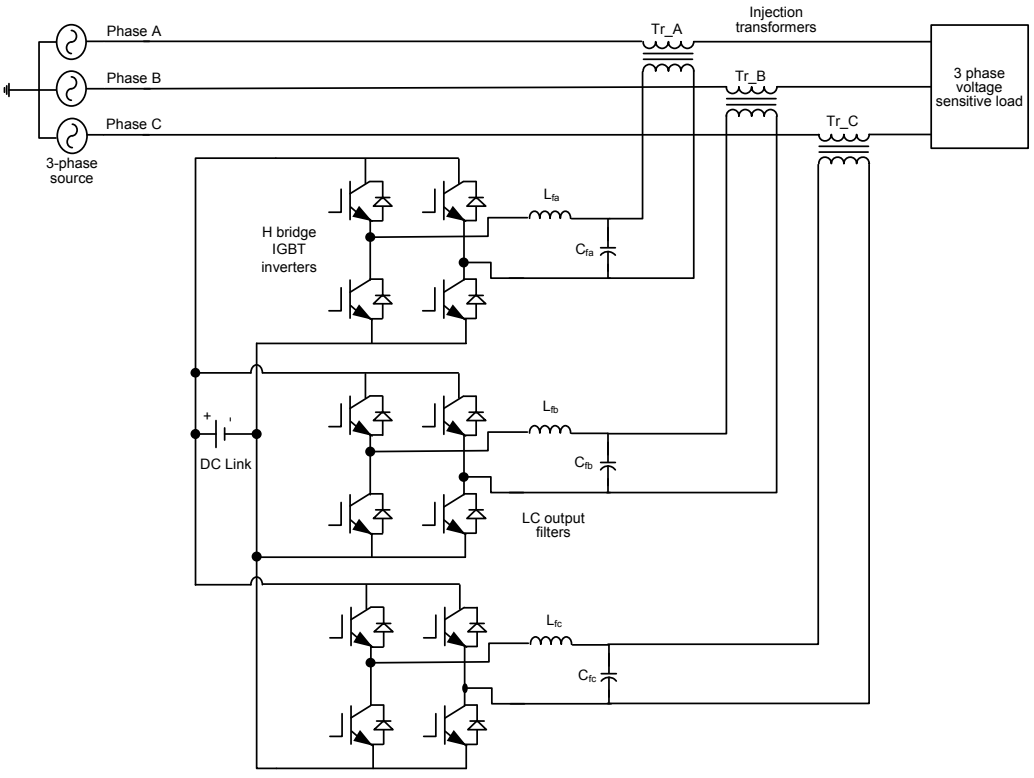

Figure 2.2. Basic topology of DVR

Each inverter output is filtered out by a LC filter to eliminate the higher order harmonics generated by the inverter itself. The filtered output of the IGBT inverters are connected to the primary side of the injection transformers thus enabling the injection of the missing voltage to the load. The injection transformer is a specially designed transformer that attempts to limit the coupling of noise and transient energy from the primary side to the secondary side (Benachaiba and Ferdi, 2008).

With the DVR installed on a critical load feeder, the line voltage is restored to its nominal value within the time of a few milliseconds thus avoiding any power disruption to the load (Ramasamy et al., 2005). A DVR basically consist of a controller, injection transformers, voltage source inverters, harmonic filters and DC power supply unit. The output filter inductors and capacitors are used to eliminate voltage harmonic at the switching frequency (Chiang et al., 2006).

The performance of a Dynamic Voltage Restorer is determined solely by its controller. The design of high performance control algorithms for DVR control with improved robustness and desirable steady state and transient characteristics is therefore an important area of study (Li et al., 2007a).

Kim et al. (2004) discusses how to calculate the compensation voltages in DVR by use of PQR power theory. Directly sensed three phase voltages are transformed to p-q-r coordinates without time delay, then the reference voltages in p, q and r coordinates have DC form. The controlled variables in p-q-r coordinates are then inversely transformed to the original a-b-c coordinates instantaneously generating reference compensation voltages to DVR.

A robust control scheme with an outer H∞ voltage control loop and an inner current control loop is designed and implemented (Li et al., 2007b). Through a simple selection of weighting functions, the synthesized H∞ controller would exhibit significant gains in the variety of positive and negative sequence fundamental frequencies and therefore it would be able to regulate both positive and negative sequence components effectively, with explicit robustness in the face of system parameter variations.

Ho et al. (2008) presents a fast dynamic control scheme for capacitor supported single phase Dynamic Voltage Restorers for inductive loads. The scheme

used consists of two main control loops. The inner loop is used to dictate the gate signals for the switches in the DVR. The outer loop is used to generate the DVR output reference for the inner loop. A 500 VA, 110V, 60 Hz prototype has been built and tested with nonlinear inductive loads.

Chiang et al. (2006) presents reduced switch count inverter in the single phase system to compensate voltage disturbance for low power applications. Also, three phase DVR system with three single phase full bridge inverters is also presented to against the abnormal utility voltage conditions such as voltage sag, swell, flicker, harmonics and unbalance voltage.

Selective harmonic elimination pulse width modulation (SHEPWM) method is used in (Zhao, 2008). Based on the feature of harmonic distribution of the SHEPWM pulses, the paper presents design principle of inverter filter. The experimental result of 200 kVA DVR using SHEPWM indicates that the inverter can effectively restrain the harmonics and has good dynamic performance in all the range of output voltage.

Komatsu et al. (2008) presents a development platform with reduced power for DVR and flexible alternating current distribution systems applications and development. The proposed equipment allows testing control algorithms, hardware behaviors as well as the strategy applied in the development of the power circuitry. The paper emphasizes the implementation of a DVR topology and its results.

A digital adaptive controller based on the Generalized Minimum Variance control approach for high performance single phase inverters capable of maintaining very low harmonic distortion in the presence of unknown loads which could be linear or nonlinear (Deng et al., 2004). Simulation and experimental results are presented to verify the feasibility of the proposed approach and also its performance.

A mathematical morphology (MM) theory based low pass filter to preprocess the single phase voltage sag signal to filter out noise and any other interferences in the sampled signal is introduced (Zhou et al., 2008). A comparison between the MM filter and traditional low pass filter is carried out to analyze the applicability and accuracy of the MM filter. Software simulation results are given to verify the practicability of the algorithm.

A soft phase lock technology based on instantaneous reactive power theory was suggested to solve the synchronization, phase lock, voltage breadth value make constant and frequency change etc. and also discussed the harmonics definition, calculating method on situation of frequency change (Fang et al., 2004).

A new voltage disturbance detector with delta rule of the neural network is presented (Chung et al., 2007). Through the proposed method, the peak value of each phase voltage under the severe unbalance voltage conditions can instantaneously tracked.

A fast detection algorithm for sags, swells and interruptions is developed (Gonzales et al., 2006). The proposed method is based on the combination of the digital root mean squate (RMS) technique and the Kalman filter. The union of these methods allows using the advantages of Kalman filter and RMS technique and helps rejecting the extreme drawbacks of Kalman filter.

An open loop double feed forward controller is proposed in (Shi and Tang, 2008). The open loop structure guarantees the fast dynamic response and the double feed forward eliminates the influences of both utility voltage and the load current.

A simple structure feed forward neural network is presented for the separation of negative sequence components from fundamental sequence components in unbalanced voltage sag. In addition, a new control strategy based adaptive neural network is proposed to inject minimum energy for DVR during compensation. Simulation results are carried out using PSCAD/EMTDC (Banaei et al., 2006).

A control method for eliminating DC magnetic flux from the series transformer of a Dynamic Voltage Restorer is proposed (Jimichi et al., 2008). The method is characterized by intentionally injecting no compensation voltage during one-sixth line cycle. The paper confirms the effectiveness and viability of the proposed method on a 200V, 5kW laboratory prototype.

2.2. Review of Static Transfer Switch

A thyristor-based static transfer switch provides a continuous supply for a voltage sensitive load through fast transfer between two sources when the main source does not meet load voltage requirements (Mokhtari and Iravani, 2007).

If an alternate feeder exists or can be provided to the critical load at reasonable cost, STS can transfer quickly enough the voltage supply to an alternate source and sensitive load experiences only a shallow sag of short duration. Obviously, STS is not effective in the event of a utility outage and cannot provide power conditioning (Burke et al., 1990).

The basic topology of Static Transfer Switch is given in Figure 2.3. The load which is sensitive to the variations in the utility supply voltage is normally fed from the preferred source. If a problem occurs on the preferred source, the supply of the load is transferred to the alternate source by the use of the thyristor pairs. The disturbances will be detected by continuously monitoring both the preferred and alternate source voltage and currents.

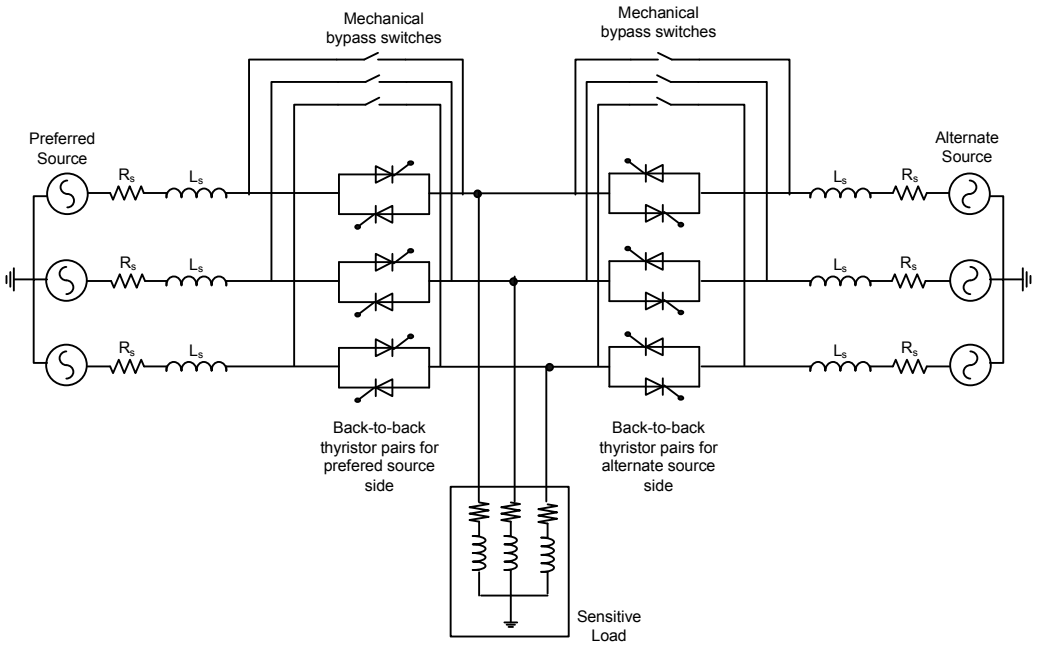

Figure 2.3. Basic topology of STS

As seen in Figure 2.3, the load can be supplied from any of the two sources using mechanical switches manually. These switches also help the servicing of the STS under a failure. R_s and L_s are resistance and inductance of the line, respectively.

An analytical model of STS is proposed and its performance is verified using electromagnetic transients for DC (EMTDC) simulation package in (Moschakis and Hatziargyriou, 2003). Simulations using this model are performed in order to handle voltage sags based on real measurements on an actual industrial customers' supply voltage.

Gregory et al. (2002) describe a computationally efficient detection algorithm for power quality disturbances which uses less computational effort. The static transfer switch presented in the paper is intended to be used on a three phase system. The method presented reduces the amount of information to be processed by utilizing the alpha-beta space vector technique (Zhan et al., 2001). These considerations have been validated using PSCAD/EMTDC simulations.

The effect of regenerative load on a static transfer switch performance is investigated in (Mokhtari et al., 2001). The transfer time and total load transfer time of a STS is determined and worst case in which maximum transfer time occurs is identified. A low voltage experimental setup is used to demonstrate the STS performance. The simulations are performed using the PSCAD/EMTDC package.

Mokhtari et al. (2002) report a thorough analysis of the transfer time of a STS system. Those system parameters which impact the commutation process and the transfer time are identified. Analytical expressions are derived to estimate STS transfer time for RL loads under various operating conditions and disturbance scenarios. For a medium voltage STS system, analytically calculated STS transfer times, under various operating conditions and fault scenarios are validated by the results obtained from digital simulation of the system. The PSCAD/EMTDC software package is used for simulation studies. A laboratory experimental STS system is set up to verify the analytical and simulation results. The investigation concludes the followings.

• The transfer time which is determined by the commutation process between the thyristor switches, depends on the STS control strategy, the system parameters and fault/disturbance characteristics.

• The maximum transfer time occurs in the phase in which the commutation between the incoming and outgoing thyristor fails. The commutation fails when the voltage drop across the incoming thyristor and the corresponding line current have opposite polarity.

• The transfer time increases as the load power factor decreases.

The operation of the static transfer switch is analyzed and maximum detection times are calculated (Sannino, 2001). Control system requirements for performing fast transfer between two power supplies without affecting the operation of the healthy source are explained. Conditions for make-before-break switching are analytically evaluated, depending on amplitude and phase of the two source voltages and on the load to be protected. Calculations are also validated by example cases realized in simulation with ATP-EMTP.

Schwartzenberg and De Doncker (1995), presents the development and operation of a three phase medium voltage static transfer switch system. The system is a 15 kV class switch system rated at a continuous current of 600 A. To achieve the design ratings, a series string of nine AC thyristor switch modules are used. Parallel thyristors are used to increase the surge current rating of the AC switch. Under normal loading conditions, the thyristors are under very light load for their size. Each module consists of the thyristors, gate drivers, snubber and metal oxide varistors.

The performance of STS for feeder reconfiguration has been assessed and evaluated (Mahmood and Choudhry, 2006a). STS restorers the voltage to prefault conditions. The sensitive loads are fed by preferred feeder but in case of disturbances, the loads are transferred to alternate feeder. Different simulation cases were performed for optimum installation of STS to obtain the required voltage quality. The simulations are performed using PSCAD/EMTDC package. The simulation results of various case studies show that the quality of power is poor for preferred network feeder without STS. The simulation results show that using STS,

voltage disturbances can be eliminated and power quality improvement can be achieved effectively and efficiently.

In (Mahmood and Choudhry, 2006b), two different feeders namely primary and secondary having different impedances and loads are reconfigured using static transfer switch, when voltage sag/fault occurs. Mainly, sensitive loads are fed by primary feeder network. The load power factor is considered as 0.9 lagging. In case of voltage sag/interruption, the control circuit of static transfer switch transfers the sensitive loads to secondary feeder network. Hence, the reliability and quality of electric power can be significantly improved for sensitive/critical loads. PSCAD/EMTDC program has been used for modeling and analysis of the considered distribution network feeders. For optimum location of STS and power quality improvement, many simulation studies have been performed without and with STS.

Mokhtari and Iravani (2007) investigate the impact of phase difference between the corresponding voltages of two sources on the load transfer performance achieved by an STS. The studies are performed on the IEEE benchmark STS-1 system using the PSCAD/EMTDC simulation software. The studies indicate that the impact of phase difference on the STS load transfer time is insignificant when sensitive load is a passive load. The results also show that the effect of phase difference on load transfer time can be neglected when the main source is subjected to unsymmetrical faults. It is also shown that the phase difference can affect the cross current phenomenon during a transfer process.

A technique for an on-line remote and automatic switching and rearrangement of consumer connection for optimal performance of a secondary distribution network feeder has been presented in (Popoola et al., 2007). The proposed scheme addresses the problems of phase current and voltage imbalances due to uneven distribution of loads in a secondary distribution system feeder. The system is practically realizable, although only its operating characteristics have been demonstrated through a MATLAB simulation.

STS consists of two thyristor blocks per phase at the preferred and alternate feeders to connect load to the two alternate sources. Each thyristor block has two thyristor switches connected in opposite direction. Two thyristors per phase has been

used to allow load current to flow in both positive and negative directions (Mahmood and Choudhry, 2006).

2.3. Review of Shunt Active Power Filter

An active power filter is a power electronic device used to effectively eliminate the harmonic current generated by nonlinear loads. The operational principle of the APF is to inject a harmonic current with the same magnitude and a 180 phase shift in parallel with the load, so that the source can supply the fundamental component of a load current only (Han et al., 2005). Shunt filters have the advantage of carrying only the compensation current plus a small amount of active fundamental current supplied to compensate for system losses. It is also possible to connect several filters in parallel to cater for higher currents, which makes this type of circuit suitable for a wide range of power ratings (El-Habrouk et al., 2000).

The basic topology of the voltage source Shunt Active Power Filter is presented in Figure 2.4. The APF consist three phase IGBT inverter, interface reactors, DC link capacitor.

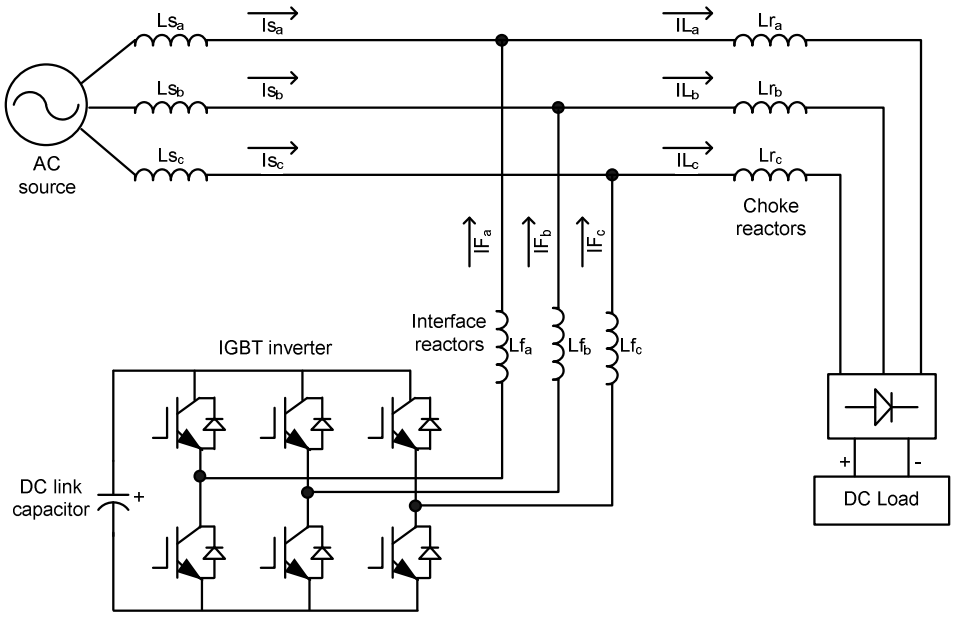

Figure 2.4. Basic topology of SAPF

Choke reactors are used to prevent the current overlap in the diode rectifier load. Interface reactors are used to eliminate the dominant harmonics of the IGBT inverter. DC link supplies the required power to the inverter.

Rahimi et al. (2009) presents an adaptive detection approach of current harmonics on the basis of the configuration and learning algorithm for the shunt active power filter and the realization scheme of an analog circuit of the system is discussed. Power simulator (PSIM) software is used for the simulation studies.

Rahmani et al. (2009) present a nonlinear control technique for a three phase shunt hybrid power filter. d-q transformation is used. d-q frame model is divided into two separate loops for current and DC voltage control. Proportional-integral (PI) controllers are utilized to control filter currents and DC bus voltage. The effectiveness of the control technique is demonstrated through simulation and experimental studies.

Voltage source and current source active power filters are compared in (Routimo et al., 2007). The comparison includes main circuits, space vector modulation techniques and digital control systems. The filtering performance of the system with different nonlinear loads is examined. The comparisons made are based on the experimental prototypes.

An analysis between results from applications of the p-q and the p-q-r theories in the shunt active power filters are made in (Aredes et al., 2009). A new control method based on the p-q theory is presented. The method presented has the advantage of avoiding the alpha-beta to p-q-r transformation.

Many non ideal factors, such as limited bandwidth of output current loop, the time lag of signal sensing circuit and generation of reference currents will deteriorate the compensative effect of active power filters. PI controller cannot be used simply to control the output current without any steady-state error due to its limited current tracking capability. A new control method named zero steady-error control is proposed in (Wei et al., 2009) and verified by theoretical analysis and experimental results.

Cirrincione et al. (2009) present a single phase shunt active power filter for current harmonic compensation based on neural filtering. Current controlled inverter

is used in the filter. A neural adaptive notch filter is used to generate the reference signals. The filter's parameters are made adaptive with respect to the grid frequency fluctuations. Both simulation and experimental studies are presented.

Costa-Castello et al. (2007) analyze the dynamics of a DC bus split capacitor boost converter used as an active filter and proposes a control system which guarantees the desired closed loop performance. The paper describes the analytical design of the controller and presents some experimental results.

An efficient steady-state compensation method and a conceptual design for sizing the three phase three wire shunt active power filter under non-sinusoidal source voltages is presented in (Chang et al., 2006). An optimization based solution algorithm is proposed to determine active power filter current injections to meet different constraints with an optimal filter size. Results obtained by simulations with MATLAB/Simulink show that the proposed approach is very flexible and effective for compensating harmonic currents generated by the nonlinear load.

Ramos-Carranza et al. (2009) present the application of a real time simulation technique to shunt active power filter compensation of the harmonics currents and reactive power in the power system. real time windows target of MATLAB/Simulink is used. It is possible to obtain simulation conditions that are close to the real time environment under study using only a single computer giving accurate results with relatively low cost hardware.

Uyyuru et al. (2009) present an optimization based control algorithm for the compensation of steady-state load under distorted supply voltage. The algorithm gives the best power factor while satisfying the constraints such as total harmonic distortion. MATLAB and its optimization toolbox are used for the simulation studies. TMS320F2812 is used in the lab prototype.

A current detection algorithm based on the time domain approach for three phase shunt active power filter to eliminate harmonics, correct power factor and balance asymmetrical loads is analyzed in (Li et al., 2005). Simulation results obtained by using MATLAB and results are tested by an experimental setup.

Chen and Xu (2004) present the control and design issues of a shunt active power filter with consideration for the unbalanced loads. Some details about the

digital controller using a DSP based on the synchronous reference frame including hardware synchronization, software design and fast start up are also presented. Experimental results obtained from a 15 kVA prototype are used for verification.

A modification is made on the Fryze's algorithm in (Petit et al., 2007) to control the shunt active power filter. The aim of the method is to mitigate the harmonics components and to improve the power factor. The results obtained in the experimental setup are given to show the correct performance of the algorithm.

Thirumoorthi et al. (2009) present a shunt active power filter mainly for source current harmonics elimination. The method proposed is based on instantaneous reactive power theory. The proposed method requires measuring the source currents with reduced number of current sensors than existing methods. MATLAB/Simulink power system toolbox is used to simulate the proposed system.

Khadkikar et al. (2009) deal the single phase p-q theory for the purpose of active power filtering in the case of single phase loads. A systematic study is presented by realizing both direct and indirect current control techniques. The simulation as well as the DSP based experimental results is discussed.

Wei et al. (2009) present a new DSP based control of a shunt active power filter. Compared to analog based methods, the DSP based control provides a flexible and cheaper method to control the active filter. Compensating currents are determined by using artificial neural networks.

3. CONTROLLERS USED IN CUSTOM POWER DEVICES

The accurate measurement of power disturbance in real time circumstance is a key element of protection, control, fault diagnosis, power quality monitoring and power metering in electric power systems. A variety of measurement techniques have been developed to measure the instantaneous electrical quantities such as amplitude, phase angle, frequency and power of the fundamental and harmonic components in a non-stationary power disturbance waveform. The performance of these techniques in different service conditions directly determines the result of fault diagnosis, the clearance of electrical faults and the effect of power disturbance mitigation (Lin and Domijan, 2006).

The disturbance detection techniques for real time applications of custom power devices can be implemented using the controllers such as DSP, FPGA, microcontroller or combination of them. They can generate sag/swell detection signal, reference voltage signal and perform protection for DVR applications. They can generate reference current signal and perform protection for APF applications. They can generate transfer and protection signals for STS applications. The controllers used in the experimental control of APF are FPGA (Li et al., 2007), DSP (Fernandes et al., 2009), combination of DSP-FPGA (Baros and Silva, 2010) and micro-controller based system (INTEL-8031) (Wang and Venkataramanan, 2005). The controller used in the experimental control of DVR are combination of DSP-microcontroller system (Dai et al., 2008), DSP (Radzi and Rahim, 2009), PowerPC–based board (DS1103) (Henning et al., 2008) and combination of DSP-FPGA (Kumar and Agarwal, 2003). The controllers used in the experimental control of STS are Universal High-Performance digital controller (Mokhtari et al., 2000) and DSP (Mokhtari et al., 2002).

To control the power electronics switching devices, analog and digital controllers can be used. However, the design and maintenance of analog controllers are relatively bulky and complex. With the development of digital systems, design of control systems became easier and economical as the reduction of auxiliary

equipments used. Nowadays, digital controllers are most widely used in control applications.

There are numerous architecture options available for implementing the digital control functionality in most control systems. These are DSP, custom application specific integrated circuit (ASIC) solution, FPGA and even a general purpose processor implementation. Dedicated multiply accumulator (MAC) unit in hardware, the control loops that needs to be implemented uses heavy computations that need to be completed in a finite interval of time. Most general purpose processors do not have the MAC unit and as a result consume precious multiple cycles for executing the MAC operation. Although ASIC implementations would yield the best performance for a given application, the development cycle time is rarely justified. Certain FPGAs do contain MAC units, but this requires additional device resources to be consumed for implementation (Godbole, 2008). The main advantage of DSPs is their software flexibility, whereas FPGAs provide higher performances in repetitive and massive computations (Fratta et al., 2004).

In this thesis, TMS320F2812 and TMS320F28335 DSP kits are chosen to implement the controllers of DVR, STS and SAPF. These two devices are grouped in C2000 digital controller platform of Texas Instruments which provides an optimized combination of DSP performance and microcontroller integration of digital control systems. The control of DVR, STS and SAPF includes lots of algorihms that relies on multiply and accumulate operations. To gather the performance of a device which has dedicated MAC units, DSPs are chosen to implement controllers of custom power devices. Chosen DSP controllers also have pulse width modulation units and analog to digital converters that is a must in control applications.

3.1. Digital Signal Processors used in the Thesis

The DSP phenomenon is part of the overall microprocessor success story. Like the high-end Reduced Instruction Set Computing (RISC) engines used in computers and the medium-range RISC microcontrollers in embedded systems, DSPs are becoming increasingly differentiated, designed to handle the processing tasks of specific types of applications (Frantz, 2008).

Although DSPs are similar to RISC engines in some respects, they are fundamentally different in other ways. These difference date from the earliest microprocessor architectures and they will continue to influence the development of DSPs and their applications in the years ahead. Essentially, DSPs are designed for number crunching. Early computer theorist realized that many interesting mathematical functions could be performed by a series of high speed multiplications and additions. Since many of these math functions are useful for transforming and manipulating along signals in the digital realm, a machine that would perform them efficiently would be extremely valuable as a DSP. Accordingly, certain microprocessor architects designed their processor around hardware dedicated to performing multiply-accumulate functions and DSPs were born (Frantz, 2008).

In the early DSP designs, designers seized on the Harvard architecture, with its separate buses, but they used in the idea in a novel way. In addition to adding a bus for instructions, designers provided separate buses for each multiply-accumulate operand. Thus, data and instructions could be loaded and a complete multiply-accumulate performed during every cycle (Frantz, 2008).

Since DSPs are used for processing continuous signals that come from and often go back into, the real world, they are constrained to operate in real time. This constraint is another key difference between DSPs and other microprocessors, not only in application, but also in underlying architecture.

TMS320C2000 digital signal controller platform combines the control peripheral integration and ease of use of a microcontroller and processing power and C efficiency (Texas Instruments, 2008). C2000 digital signal processors are well

suited for industrial applications such as digital motor control, digital power supplies and intelligent sensor applications.

Digital control of power conversion systems results in lower overall cost due to the consolidation of functions into a single programmable controller in place of dedicated discrete components. A single C2000 digital signal processor can provide full loop control at over 2 MHz switching frequencies or control multiple output levels and simplify the sequencing of multiple supplies through software rather than dedicated components. A software based solution enables intelligent monitoring of load conditions in real time and can lead to system reliability, efficiency and operating cost. C2000 DSP controllers are suitable for applications such as uninterruptible power supplies, solar inverters and industrial equipments (Texas Instruments, 2008).

Two different digital signal processor kits with the same core are used during this study. These are Texas Instruments TMS320F2812 and TMS320F28335 DSP kits. TMS320F2812 kits are used in the implementation of Dynamic Voltage Restorer and Static Transfer Switch. TMS320F28335 kit is used in Shunt Active Power Filter. The reason for using two different controllers is that when the study began, only fixed point TMS320F2812 kit was available in the market. TMS320F28335 which is capable of dealing floating point numbers with its floating point unit was released after the work on Dynamic Voltage Restorer and Static Transfer Switch had completed. In other words, TMS320F28335 is the advanced and faster version of TMS320F2812. Although they are using the same C2000 central processing unit, they have differences in their usage because of newly added peripherals to the F28335. For that reason, they are discussed in the following subsections separately.

3.1.1. TMS320F2812 Digital Signal Processor Kit

The F2812 ezDSP is a stand alone card allowing evaluators to examine the TMS320F2812 DSP to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the

TMS320F2812 processor. The F2812 ezDSP is shipped with a TMS320F2812 DSP. The F2812 ezDSP allows full speed verification of F2812 code. Two expansion connectors are provided for any necessary evaluation circuitry. To simplify code development and shorten debugging time, a C2000 Tools Code Composer driver is provided. In addition, an onboard JTAG connector provides interface to emulators, operating with other debuggers to provide assembly language and 'C' high level language debug (Spectrum Digital, 2003). Figure 3.1 shows the F2812 ezDSP kit. Table A.1 in Appendix A summarizes the basic features of the TMS320F2812 digital signal processors.

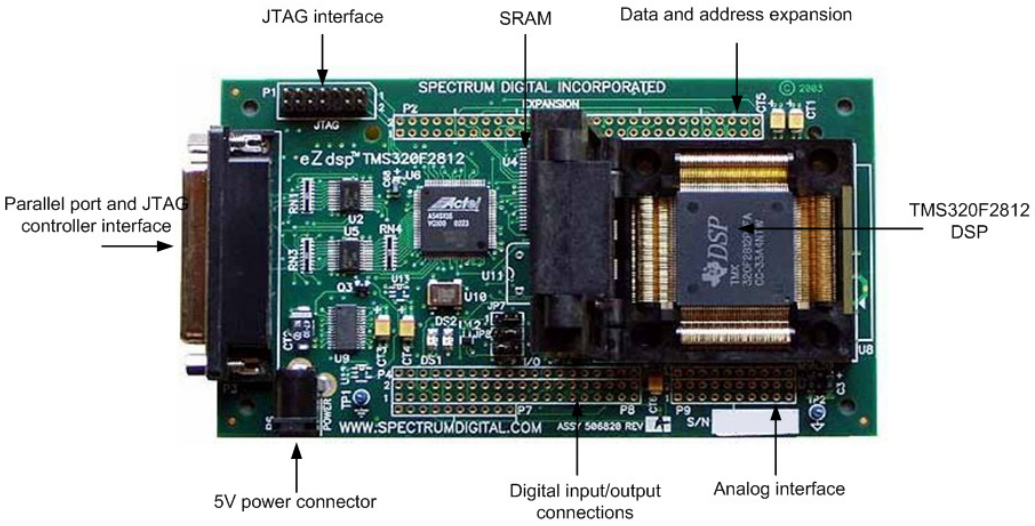

Figure 3.1. The view of ezDSP F2812 kit

TMS320F2812 DSP architecture is given in Figure 3.2. The box named Central Processing Unit (CPU) at the left bottom shows the core of the DSP. This core offers single cycle 32x32 bit multiply and accumulate (MAC) operations or dual 16x16 bit MAC. It's atomic Arithmetic Logic Unit is capable of single cycle read-modify-write operations. The DSP core has three 32 bit timers.

The memory subsystem offers 100-120 million instruction per second (MIPs) speed and 150 MIPs for time critical operations. The DSP has two Event Managers, 12 bit, 16 channels Analog to Digital Converter (ADC). DSP can communicate with

multiple standard communication ports such as multi channel buffered serial port (McBSP), serial peripheral interface (SPI) and serial communication interface (SCI).

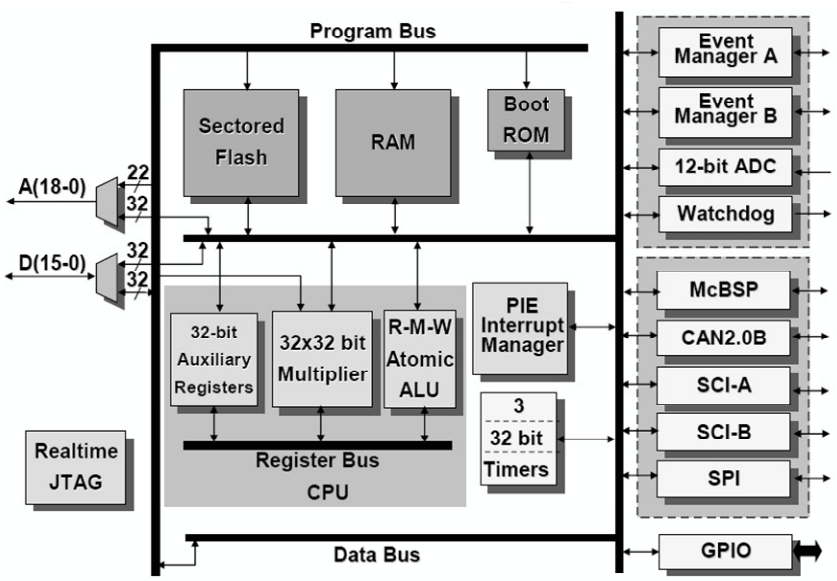

Figure 3.2. Architecture of TMS320F2812 DSP (Bormann, 2006)

There are lots of features that a single digital signal controllers offers to it's users. But often, it is not necessary to use all of them in a single project. In this study, clocking, general purpose input output module, interrupt system, event managers and analog to digital converter module of the TMS320F2812 are used and detailed explanations are given in the following sections.

3.1.1.1. Clocking and Timers

Like all modern processors, the F2812 is driven outside by a slower external oscillator to reduce electromagnetic disturbances. An internal Phase Locked Loop (PLL) circuit generates the internal speed. The ezDSP kit has 30 MHz external clock. To achieve internal frequency of 150 MHz, PLL Control Register must be set. The clock speed setup module of the DSP is illustared in Figure 3.3. SYSCLKOUT is the internal speed.

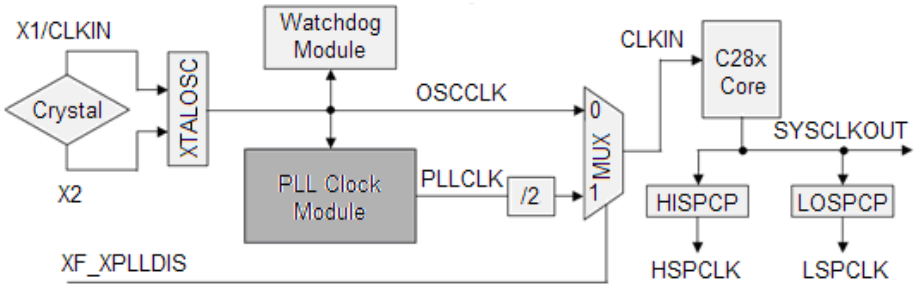

Figure 3.3. Adjustment of internal clock speed (Bormann, 2006)

The available speeds that can be selected by using phase locked loop control register (PLLCR) register is given in Table 3.1. The bits 15:4 are reserved. Last 4 bits determine the value of SYSCLKOUT. OSCCLK is the external oscillator clock speed.

Table 3.1. PLLCR register (Texas Instruments, 2010a)

Bit 3	Bit 2	Bit 1	Bit 0	SYSCLKOUT	SYSCLKOUT (For 30 MHz OSCCLK)
0	0	0	0	OSCCLKx1/2 (No PLL)	15 MHz (No PLL)
0	0	0	1	OSCCLKx1/2	15 MHz
0	0	1	0	OSCCLKx2/2	30 MHz
0	0	1	1	OSCCLKx3/2	45 MHz
0	1	0	0	OSCCLKx4/2	60 MHz
0	1	0	1	OSCCLKx5/2	75 MHz
0	1	1	0	OSCCLKx6/2	90 MHz
0	1	1	1	OSCCLKx7/2	105 MHz
1	0	0	0	OSCCLKx8/2	120 MHz
1	0	0	1	OSCCLKx9/2	135 MHz
1	0	1	0	OSCCLKx10/2	150 MHz

High Speed Clock Prescaler (HISPCP) and Low Speed Clock Prescaler (LOSPCP) are used as additional clock dividers. The outputs of the two prescalers are used as the clock source for the peripheral units. HSPCLK drives high speed peripherals where LSPCLK drives the low speed peripherals. The available speed values that can be selected using HISPCP and LOSPCP (Bormann, 2006) are given in Table 3.2.

Table 3.2. Determination of peripheral clock frequency (Texas Instruments, 2010a)

HI/LOSPCP2	HI/LOSPCP1	HI/LOSPCP0	Peripheral Clock Frequency
0	0	0	SYSCLKOUT/1
0	0	1	SYSCLKOUT/2
0	1	0	SYSCLKOUT/4
0	1	1	SYSCLKOUT/6
1	0	0	SYSCLKOUT/8
1	0	1	SYSCLKOUT/10
1	1	0	SYSCLKOUT/12
1	1	1	SYSCLKOUT/14

The PLLCR register will be used for the adjustment of internal speed of DSP controller. HISPCP determines the base clock speed going to the ADC of the DSP.

There are 3 timers on C28x core; Timer 0, Timer 1 and Timer 2. CPU-Timer 0 and CPU-Timer 1 can be used in user applications. Timer 2 is reserved for DSP operating system. If the application is not using DSP operating system, then Timer 2 can be used in the application.

3.1.1.2. Digital Input and Output

All the peripheral units of the F2812 are memory mapped into the data memory space of its Harvard architecture machine. This means that the peripheral units are controlled by accessing data memory addresses. All peripheral registers are grouped together into what are known as “Peripheral Frames”, PF0, PF1 and PF2. Peripheral Frame PF0 includes register sets to control the internal speed of the FLASH memory, as well as the access timing to internal SARAM. Flash is the internal non-volatile memory, usually used for code storage and for data that must be present at boot time. Peripheral Frame 1 contains most of the peripheral unit control registers, whereas Peripheral Frame 2 is reserved for the Controller Area Network register block. All digital input and outputs are grouped into ports called GPIOA, GPIOB, GPIOD, GPIOE, GPIOF and GPIOG. GPIO means “general purpose input output”. F2812 is equipped with so many internal units, that not all features could be connected to dedicated pins of the device package at any one time. The solution is multiplexing. This means, one single physical pin of the device can be used for 2 or 3

different functions and it is up to the programmer to decide which function is selected (Bormann, 2006).

3.1.1.3. Interrupt System

Interrupts are defined as asynchronous events, generated by an external or internal hardware unit. This event causes the DSP to interrupt the execution of the current program and start a service routine, which is dedicated to this event. After the execution of this interrupt service routine the program, that was interrupted, will be resumed (Bormann, 2006).

The core interrupt system of the F2812 consists of 16 interrupt lines; two of them are called “Non maskable”. The other 14 lines are “maskable”, means that the programmer can allow or disallow interrupts from these 14 lines. A mask is a binary combination of “1” and “0”. A “1” stands for an enabled interrupt line, a “0” for a disabled one. By loading the mask into register “Interrupt Enable Register”, which interrupt lines will be allowed to request an interrupt could be selected (Bormann, 2006).

The interrupt system of F2812 is shown in Figure 3.4. All 16 lines are connected to a table of “interrupt vectors”, which consists of 32 bit memory locations per interrupt. It is the responsibility of the programmer to fill this table with the start addresses of the dedicated interrupt service routines.

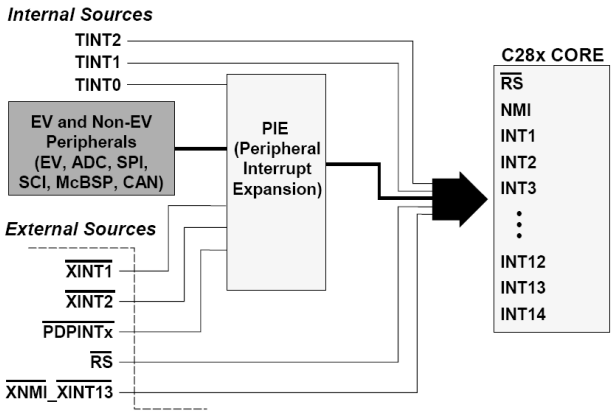

Figure 3.4. Interrupt system of F2812 (Bormann, 2006)

As seen in Figure 3.4, a single INT line is used for multiple sources. Each interrupt line is connected to its interrupt vector, a 32 bit memory space inside the vector table. This memory space holds the address for the interrupt service routine. In case of multiple interrupts this service routine must be used for all incoming interrupt requests. This technique forces the programmer to use a software based separation method on entry of this service routine. Peripheral Interrupt Expansion unit expands the vector address table into a larger scale, reserving individual 32 bit entries for each of the 96 possible interrupt sources. All 96 possible sources are grouped into 12 PIE lines, 8 sources per line. To enable/disable individual sources, PIEIFR and PIEIER registers must be programmed. The interrupt assignment table is given in Table 3.3.

Table 3.3. Interrupt assignment table (Texas Instruments, 2010a)

	INTx.8	**INTx.7**	**INTx.6**	**INTx.5**	**INTx.4**	**INTx.3**	**INTx.2**	**INTx.1**
INT1	WAKEINT	TINT0	ADCINT	XINT2	XINT1		PDPINTB	PDPINTA
INT2		T1OFINT	T1UFINT	T1CINT	T1PINT	CMP3INT	CMP2INT	CMP1INT
INT3		CAPINT3	CAPINT2	CAPINT1	T2OFINT	T2UFINT	T2CINT	T2PINT
INT4		T3OFINT	T3UFINT	T3CINT	T3PINT	CMP6INT	CMP5INT	CMP4INT
INT5		CAPINT6	CAPINT5	CAPINT4	T4OFINT	T4UFINT	T4CINT	T4PINT
INT6			MXINT	MRINT			SPITXINTA	SPIRXINTA
INT9			ECAN1INT	ECAN0INT	SCITXINTB	SCIRXINTB	SCITXINTA	SCIRXINTA

3.1.1.4. Event Managers

An Event Manager (EV) is an unit that is able to deal with different types of time based procedures. There are two event manager units called Event Manager A and Event Manager B. The EV modules provide a broad range of functions and features that are particularly useful in motion control and motor control applications. The EV modules include general-purpose (GP) timers, full compare Pulse Width

Modulation (PWM) units, capture units and quadrature encoder pulse circuits. The block diagram of Event Manager A is illustrated in Figure 3.5.

The GP Timers 1 and 2 are two 16 bit timers. Compare Units 1, 2 and 3 are used to generate up to 6 PWM signals using GP Timer 1's time base. A large number of technical applications require exactly 6 control signals. Three independent capture units CAP1, 2 and 3 are used for speed and time estimation. An incoming pulse on one of the CAP lines will take a "time stamp" from either GP Timer 1 or 2. This time stamp is proportional to the time between this event and the previous one. The Quadrature Encoder Pulse unit redefines the 3 input lines CAP1, 2 and 3 to be used as sensed edge pulses and a zero degree index pulse for an incremental encoder (Bormann, 2006).

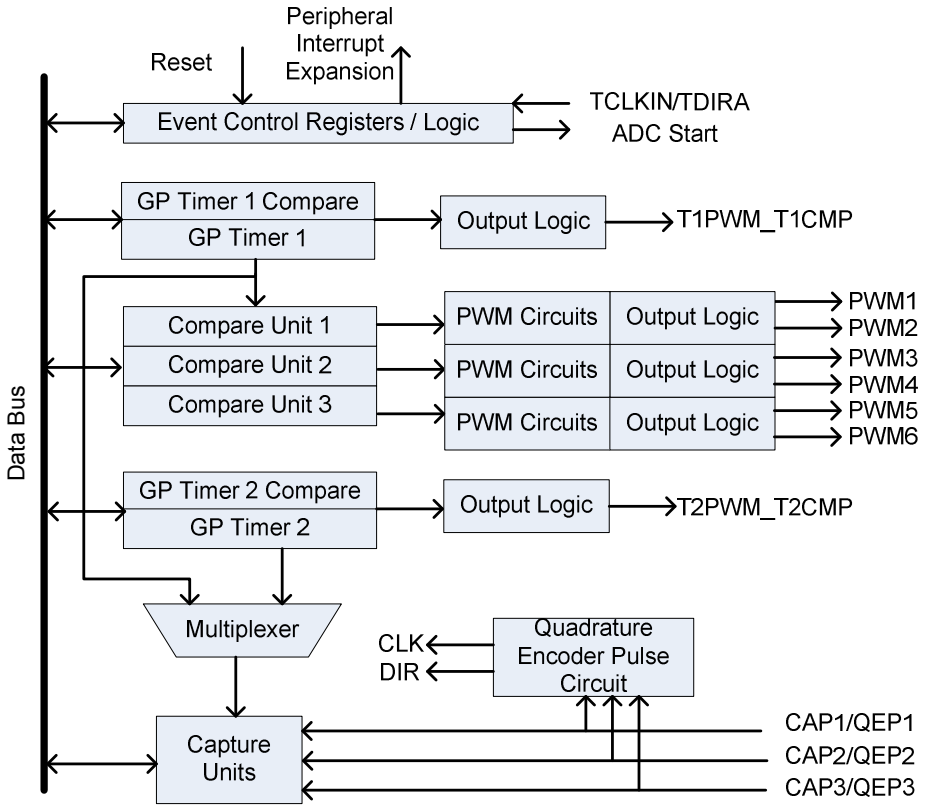

Figure 3.5. Block diagram of Event Manager A (Bormann, 2006)

The central logic of a General Purpose Timer is its Compare Blocks. This unit continually compares the value of a 16-bit counter (TxCNT) against two other registers: Compare (TxCMPR) and Period (TxPRD). If there is a match between counter and compare, a signal is sent to the output logic to switch on the external output signal (TxPWM). If counter matches period, the signal is switched off (Bormann, 2006). Compare and PWM units were extremely used during the study to drive the power electronic switches in the Custom Power Devices.

3.1.1.5. Analog to Digital Converter

One of the most important peripheral units of an embedded controller is the ADC. This unit provides an important interface between the controller and the real world. The purpose of the ADC is to convert analog voltage in a digital number. The relationship between the analog input voltage (V_{in}), the number of binary digits to represent the digital number (n) and the digital number (D) is given by:

$$V_{in} = \frac{D(V_{REF+} - V_{REF-})}{2^n - 1} + V_{REF-} \tag{3.1}$$

V_{REF+} and V_{REF-} are reference voltages and are used to limit analog voltage range. Any input voltage beyond these reference voltages will deliver a saturated digital number. In case of F2812 ezDSP, V_{REF-} is 0V, V_{REF+} is 3V. The internal ADC has a 12 bit resolution (n=12) for the digital number D. Thus giving:

$$V_{in} = \frac{D * 3V}{4095} \tag{3.2}$$

The F2812 is equipped with 16 dedicated input pints to measure analog voltages. These 16 signals are multiplexed internally, that means they are processed sequentially (Bormann, 2006).

3.1.2. TMS320F28335 Digital Signal Processor Kit

The TMS320C28335 is a 32 bit microcontroller that specializes in high performance control applications such as, robotics, industrial automation, mass storage devices, lighting, optical networking, power supplies and other control applications needing a single processor to solve a high performance application. It has a floating point unit in its architecture. The TMS320F28335 ezDSP controller kit is shown in Figure 3.6.

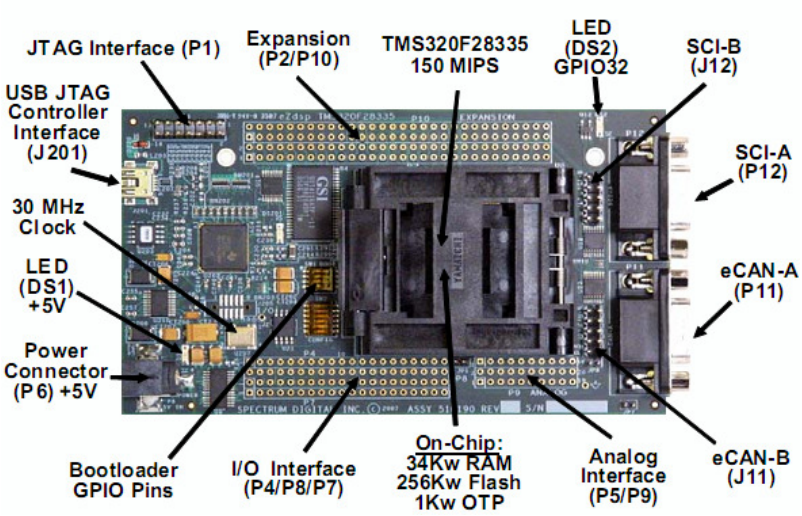

Figure 3.6. The view of ezDSP F28335 kit (Texas Instruments, 2009a)

Table A.2 in Appendix A summarizes the basic features of the TMS320F28335 digital signal processors. The main difference between TMS320F2812 and TMS320F28335 is that the second has a floating point unit that increases the performance of the controller.

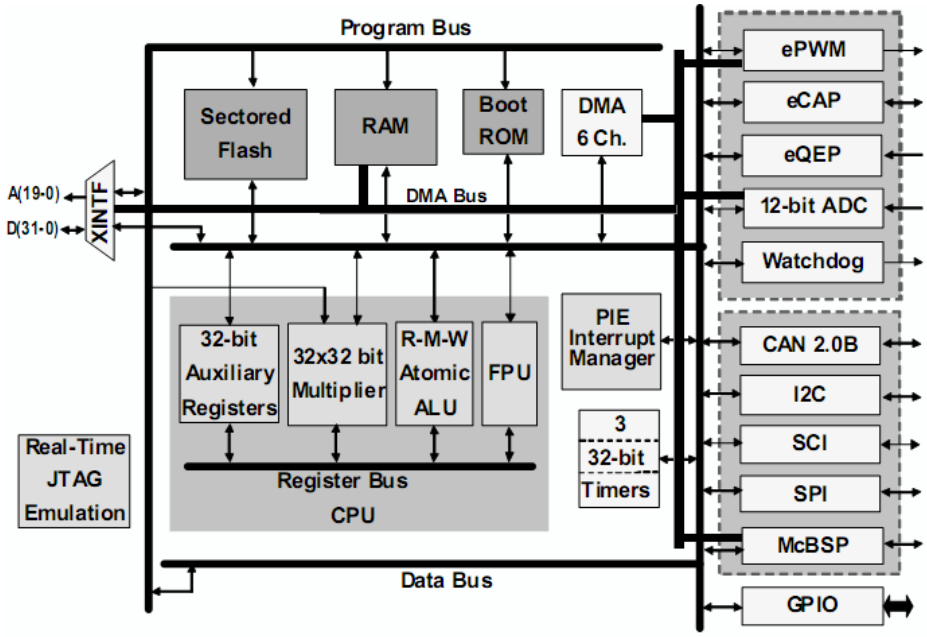

Figure 3.7. Block diagram of TMS320F28335 (Texas Instruments, 2009a)

The architecture of TMS320F28335 DSP is given in Figure 3.7. Although it looks similar with F2812, they are differentiating in some peripherals. Enhanced PWM, enhanced CAP and enhanced QEP are the upgraded peripherals in F28335. And floating point unit is the main source of its performance. As the two DSPs use the same core, identical modules are not explained again. In the following subsections, detailed explanations of the enhanced modules of TMS320F28335 are given.

3.1.2.1. Floating Point Unit

The addition of floating-point brings performance improvements to control type algorithms for the C2000 family. Floating-point has the following advantages over fixed-point (Heustess, 2007):

• Many algorithms used in control applications see a performance boost from native floating-point. Those algorithms such as square root, division, sin, cos, Fast Fourier Transform (FFT) has a floating point nature.

• Coding is simplified as one can easily use float data type and use it in control algorithms.

• The scaling and saturation burden seen in fixed point is removed.

The floating point unit of F28335 follows the Institute of Electrical and Electronics Engineers (IEEE) 754 format for single precision floating point math.

3.1.2.2. Enhanced Pulse Width Modulation (ePWM) Module

PWM is a method for representing an analog signal with a digital approximation. The PWM signal consists of a sequence of variable width, constant amplitude pulses which contain the same total energy as the original analog signal (Texas Instruments, 2009a).

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipments. These systems include digital motor control, switch mode power supply control, UPS and other forms of power conversion. The ePWM peripheral performs a digital to analog (DAC) function, where the duty cycle is equivalent to a DAC analog value; it is sometimes referred to as a Power DAC (Texas Instruments, 2009b). The multiple PWM modules are shown in Figure 3.8. The module includes the sub-modules of Time-Base Module, Counter Compare Module, Action Qualifier Module, Dead-Band Generator Module, PWM Chopper (PC) Module, Trip Zone Module and Event Trigger Module.

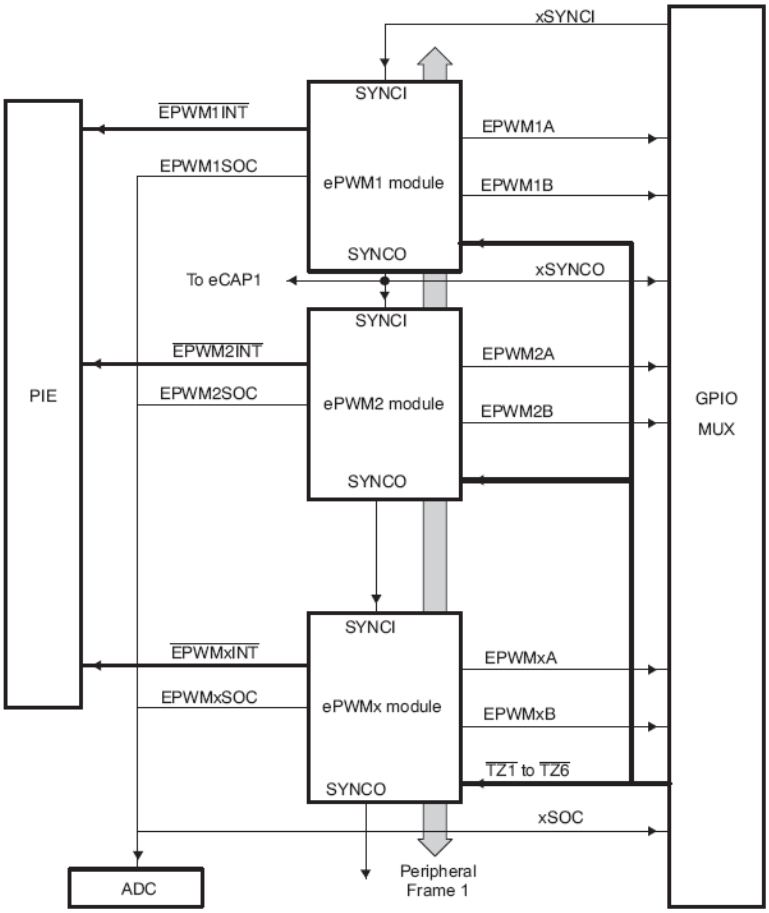

Figure 3.8. Block diagram of multiple PWM modules (Texas Instruments, 2009b)

The ePWM abbreviation is used to represent a complete PWM channel composed of two PWM outputs; EPWMxA and EPWMxB, where x indicates a generic ePWM instance on a device. TMS320F28335 has six ePWM modules. Each ePWM module has the following features (Texas Instruments, 2009b):

• Dedicated 16-bit time-base counter with period and frequency control

• Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:

- Two independent PWM outputs with single-edge operation
- Two independent PWM outputs with dual-edge symmetric operation
- One independent PWM output with dual-edge asymmetric operation

• Asynchronous override control of PWM signals through software

• Programmable phase-control support for lag or lead operation relative to other ePWM modules

• Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis

• Dead-band generation with independent rising and falling edge delay control

• Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions

• A trip condition can force either high, low or high-impedance state logic levels at PWM outputs

• All events can trigger both CPU interrupts and ADC start of conversion

• Programmable event prescaling minimizes CPU overhead on interrupts

• PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives.

The internal structure of an ePWM module is given in Figure 3.9. There are five types of signals used in these modules; PWM output signals (EPWMxA, EPWMxB), trip zone signals (TZ1 to TZ6), time base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals, ADC start of conversion signals (EPWMxSOCA, EPWMxSOCB) and peripheral bus signals. A more detailed picture of an ePWM module is illustrated in Figure 3.10. The figure shows the ePWM Submodules and critical internal signal interconnections.

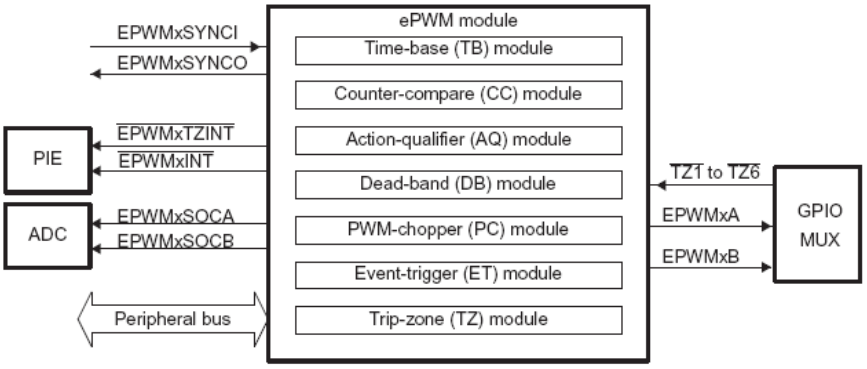

Figure 3.9. Internal structure of an ePWM module and its connections (Texas Instruments, 2009b)

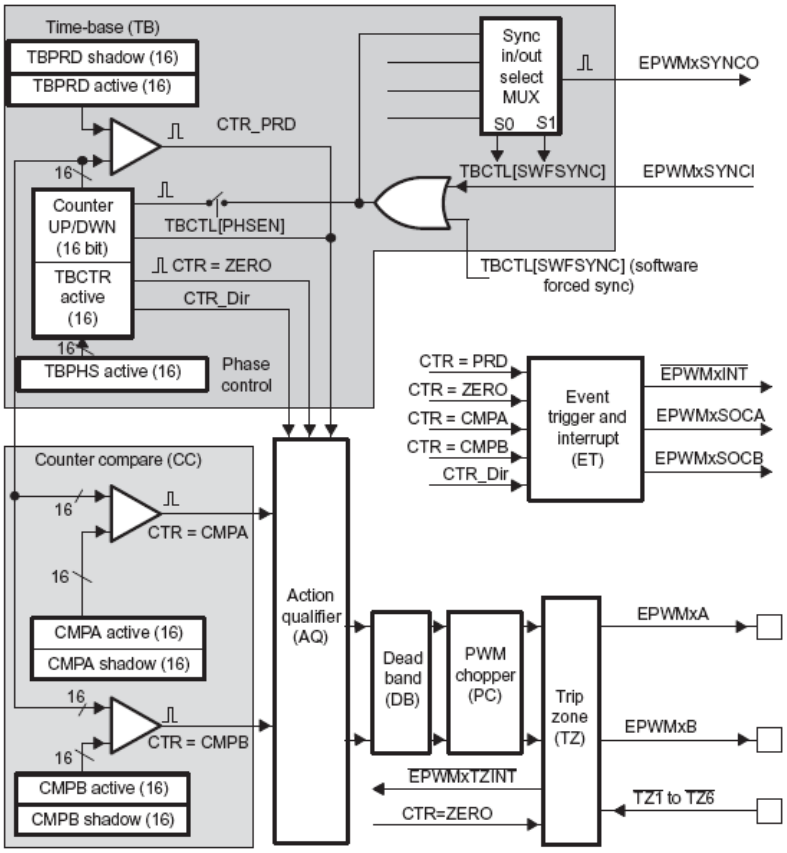

Figure 3.10. ePWM submodules (Texas Instruments, 2009b)

3.1.2.2.(1). Time Base Module

Each ePWM module has its own time-base submodule that determines all of the event timing for the ePWM module. Built-in synchronization logic allows the time-base of multiple ePWM modules to work together as a single system. The Time Base module's place within the ePWM is illustrated in Figure 3.11. The purpose of the time base module is listed below (Texas Instruments, 2009b).

• Specify the ePWM time-base counter (TBCTR) frequency or period to control how often events occur.

• Manage time-base synchronization with other ePWM modules.

• Maintain a phase relationship with other ePWM modules.

• Set the time-base counter to count-up, count-down or count-up-and-down mode.

• Generate the following events:

- CTR = PRD: Time-base counter equal to the specified period (TBCTR = TBPRD) .

- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000).

• Configure the rate of the time-base clock; a prescaled version of the CPU system clock (SYSCLKOUT). This allows the time-base counter to increment/decrement at a slower rate.

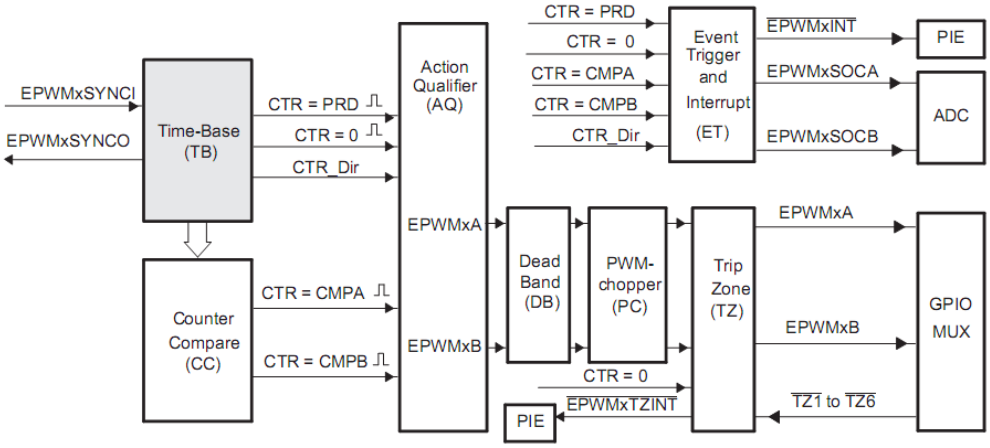

Figure 3.11 Time base submodule block diagram (Texas Instruments, 2009b)

3.1.2.2.(2). Counter-Compare Sub Module

The counter-compare sub module takes as input the time-base counter value. This value is continuously compared to the counter-compare A (CMPA) and counter-compare B (CMPB) registers. When the time-base counter is equal to one of the compare registers, the counter-compare unit generates an appropriate event. The counter-compare module (Texas Instruments, 2009b):

• Generates events based on programmable time stamps using the CMPA and CMPB registers.

- CTR = CMPA: Time-base counter equals counter-compare A register (TBCTR = CMPA).
- CTR = CMPB: Time-base counter equals counter-compare B register (TBCTR = CMPB)

• Controls the PWM duty cycle if the action-qualifier sub module is configured appropriately.

• Shadows new compare values to prevent corruption or glitches during the active PWM cycle.

The block diagram of counter-compare sub module is shown in Figure 3.12.

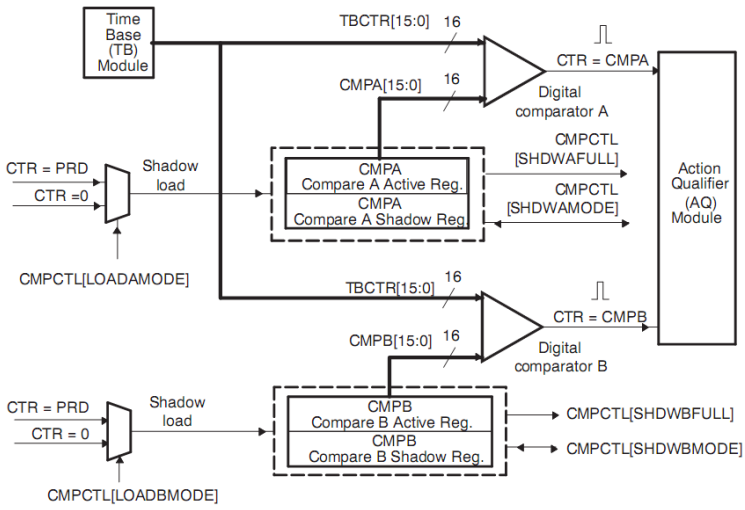

Figure 3.12. Block diagram of counter-compare submodule (Texas Instruments, 2009b)

3.1.2.2.(3). Action Qualifier Sub Module

The action-qualifier submodule has the most important role in waveform construction and PWM generation. It decides which events are converted into various action types, thereby producing the required switched waveforms at the EPWMxA and EPWMxB outputs. The purpose of the Action Qualifier submodule (Texas Instruments, 2009b):

• Qualifying and generating actions (set, clear, toggle) based on the following events:

– CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).

– CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)

– CTR = CMPA: Time-base counter equal to the counter-compare A register (TBCTR = CMPA)

– CTR = CMPB: Time-base counter equal to the counter-compare B register (TBCTR = CMPB)

• Managing priority when these events occur concurrently

• Providing independent control of events when the time-base counter is increasing and when it is decreasing.

3.1.2.2.(4). Dead-Band Generator Sub Module

If the more classical edge delay-based dead-band with polarity control is required, then the dead-band submodule should be used. The key functions of the dead-band module are (Texas Instruments, 2009b):

• Generating appropriate signal pairs (EPWMxA and EPWMxB) with dead-band relationship from a single EPWMxA input

• Programming signal pairs for:

– Active high (AH)

– Active low (AL)

– Active high complementary (AHC)

– Active low complementary (ALC)

• Adding programmable delay to rising edges (RED)

• Adding programmable delay to falling edges (FED)

• Can be totally bypassed from the signal path

3.1.2.2.(5). PWM Chopper Sub Module

The PWM-chopper sub module allows a high-frequency carrier signal to modulate the PWM waveform generated by the action-qualifier and dead-band sub modules. The purposes of PWM Chopper sub module are (Texas Instruments, 2009b):

- Programmable chopping (carrier) frequency
- Programmable pulse width of first pulse
- Programmable duty cycle of second and subsequent pulses
- Can be fully bypassed if not required

3.1.2.2.(6). Trip Zone Sub Module

Each ePWM module is connected to six trip zone (TZ) signals (TZ1 to TZ6) that are sourced from the GPIO MUX. These signals indicate external fault or trip conditions and the ePWM outputs can be programmed to respond accordingly when faults occur (Texas Instruments, 2009b).

3.1.2.2.(7). Event Trigger Sub Module

The event-trigger sub module manages the events generated by the time-base sub module, the counter-compare sub module and the digital-compare sub module to generate an interrupt to the CPU and/or a start of conversion pulse to the ADC when a selected event occurs.

3.2. Comparison of TMS320F2812 and TMS320F28335

The features of the two digital signal controllers are compared in Table 3.4. It is seen that F28335 offers floating point unit, greater random access and flash memory, 32 bit external interface, 18 channels PWM, 2 channels McBSP, 3 UART, 2 CAN and 88 GPIO pins.

Table 3.4 Comparison of TMS320F2812 and TMS320F28335

Feature	**TMS320F2812**	**TMS320F28335**
Generation	28x fixed point series	28x fixed point series
Central Processing Unit	C28x core	C28x core
Floating Point Unit	None	Yes
Operating Frequency	150 MHz	150 MHz
Random Access Memory	36 KB	68 KB
OTP ROM	2 KB	2 KB
Flash Memory	256 KB	512 KB
External Memory Interface	16 bit single interface	32/16 bit interface
Number of PWM Channels	16 channels	18 channels
Number of CAP Channels	6 channels	6 channels
Number of QEP Channels	2 channels	2 channels
Analog to Digital Converter	16 channel,12 bits	16 channel,12 bits
ADC Conversion Time	80 nano seconds	80 nano seconds
Number of McBSP	1	2
Number of UART	2	3
Number of SPI	1	1
Number of CAN Peripheral	1	2
Timers	3x 32 bit, 1 Watchdog	3x 32 bit, 1 Watchdog
Number of GPIO	56	88

4. IMPLEMENTATION OF DSP BASED DYNAMIC VOLTAGE RESTORER

The simulation model of DVR is developed by the use of PSCAD/EMTDC program. Ideal parameters are used for all of the components initially. The parameters are updated after the experimental study as ideal parameters does not give adequate results that a real system can give.

4.1. Design of Dynamic Voltage Restorer

This section covers the design of control algorithms and power circuit of DVR. A new sag detection and voltage compensation method is adopted. Sinusoidal PWM is used to generate the firing pulses. Following sections presents the software and hardware design details.

4.1.1. Controller Design of Dynamic Voltage Restorer

Simple and effective control algorithms for both voltage compensation and sag detection are developed. The algorithms are based on the nonlinear adaptive filter (Karimi and Iravani, 2002). It is shown that the filter could be used as a phase locked loop. The filter has the ability of peak detection, harmonics extraction and signal decomposition. The overall controller block diagram is given in Figure 4.1.

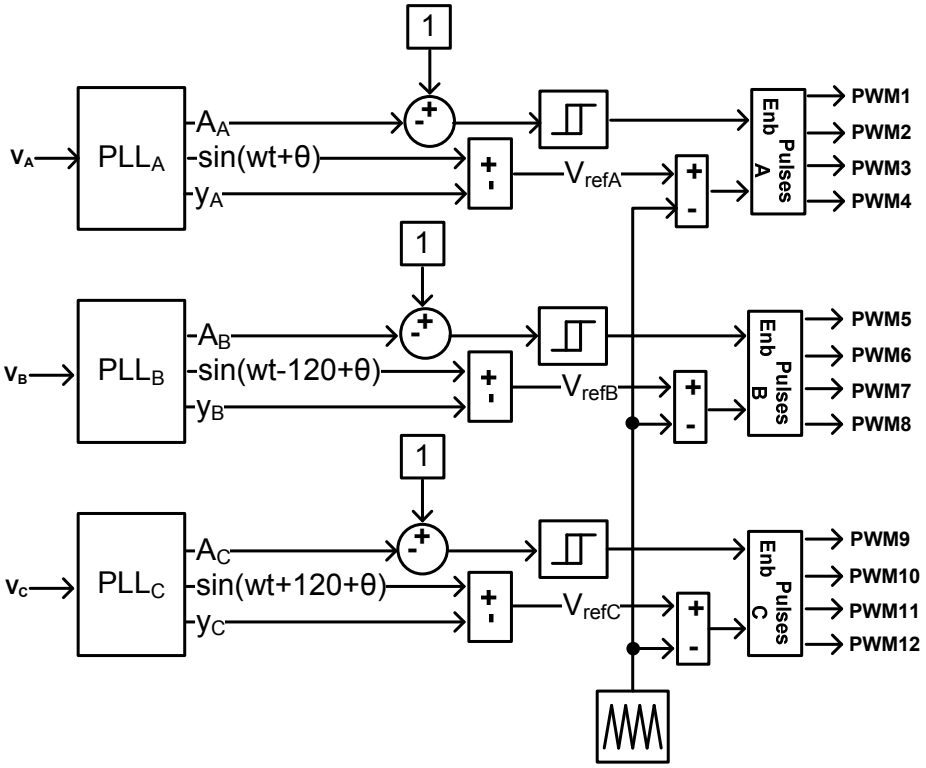

Figure 4.1. The overall DVR controller block diagram

4.1.1.1. Software Phase Locked Loop

PLL is comprised of a phase detector, a loop filter and a voltage controlled oscillator. The block diagram of the PLL is given in Figure 4.2. PLL tracks a specific component of the input signal and simultaneously extracts its amplitude and phase. The error signal represents the deviation of the input signal from the output signal.

"u(t)" is the input signal to the PLL that will be tracked while "y(t)" is the output. "A(t)" is the amplitude and "θ(t)" is the phase angle of the tracked signal "e(t)" is used to represent the error signal which represents the difference between input signal and output signal. The "w0" determines the frequency of the output signal. The generated output signal "y(t)" is both in phase and amplitude with the input signal "u(t)". In other words, "y(t)" is a copy of "u(t)".

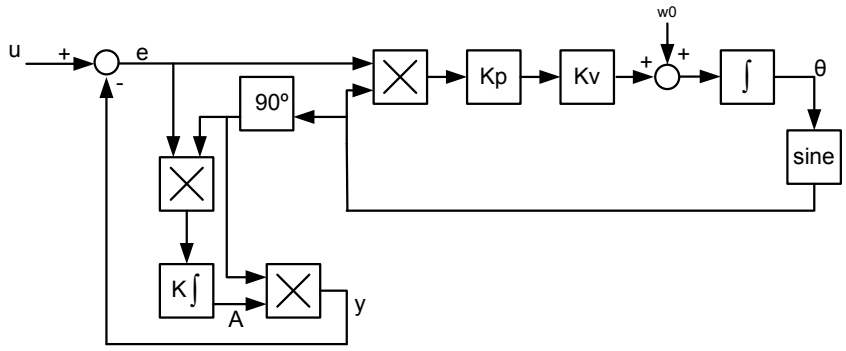

Figure 4.2. The block diagram of phase locked loop (Karimi and Iravani, 2002)

Stability of the filter is analyzed in (Karimi and Iravani, 2002) and is shown that the speed of the response is determined by parameters K, K_p and K_v. Rate of convergence is increased by increasing K_p and K_v. The parameters, K_v and K_v control transient as well as steady state behavior of the filter. This feature of the filter makes it suitable for a variety of applications. PLL provides the following advantages:

• The extracted output is not only coherent with the input signal; it is also synchronized with the desired component of the input.

• Online estimation of the amplitude, total phase, constant phase and their corresponding time-derivatives of the pre-selected component of the input signal are provided.

• The structure is robust with respect to internal parameter variations and external noise pollution.

4.1.1.2. Sag Detection Method

A new sag detection method is developed in the study. To show the superiority of the proposed sag detection method, it is compared with the conventional d-q transformation based sag detection. In the d-q method, the phase-to-neutral voltages V_a, V_b and V_c are subjected to transformation given in Equation (4.5). With the use of Equation (4.6) the phasor is obtained.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ \sin\theta & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.5}$$

$$V_s = \left|1-\sqrt{{V_d}^2+{V_q}^2}\right| \tag{4.6}$$

The block diagram of the d-q transformation based sag detection method is shown in Figure 4.3. After the three phase set of voltages are transformed into d and q components, the square root of the sum of squares of these components is obtained. The value obtained is subtracted from the reference value of 1 and then the absolute value of the resulting variable is filtered out with a 50 Hz low pass filter. The filtered output is subjected to a hysteresis comparator and the output of this comparator is the sag detection signal. The signal is high when a sag occurs, low otherwise.

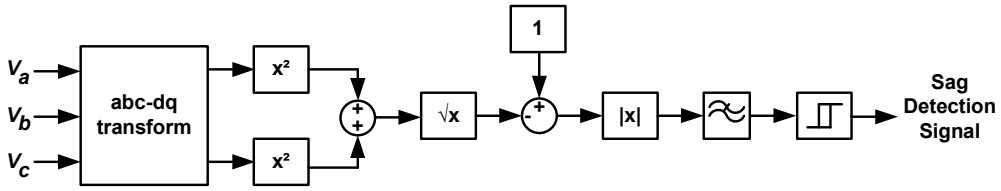

Figure 4.3. Block diagram of the d-q sag detection method

This method is able to detect the three phase balanced voltage sags with an acceptable performance. However, the most important disadvantage of this method is that it uses three phase voltage measurements for the sag detection. The method is unable to detect the voltage sags lower than a definite level. As an instance, a single phase to ground fault resulting in 20% of voltage sag cannot be determined by this method because the method used the average of the three phase voltage and sees the single phase voltage sag as an average value of 6-7% if the voltage sag detection limit is selected to be 10%. Besides another restriction of this method is the use of low pass filter tuned at 50 Hz. This filter reduces the response speed of the detection scheme.

To overcome the disadvantages of the d-q sag detection method, the PLL explained in the previous section is used. With the method, the controller is able to detect balanced, unbalanced and single phase voltage sags without an error. In the method, three PLLs are used to track each of the three phases.

The signal "A" shown at the bottom of the Figure 4.4 gives the amplitude of the tracked signal shown at the top. As an instance, if the amplitude of the measured signal is 220 V_{rms}, the signal "A" is obtained as continuous 1 pu. If the amplitude falls to the 176 V_{rms}, the amplitude of the signal "A" falls to 0.85 pu. In Figure 4.4, the signal at the top shows a measured signal of amplitude 192 V_{rms} transformed into pu equivalent corresponding to 0.87 pu. The signal obtained for this measured voltage is given at the bottom of the figure.

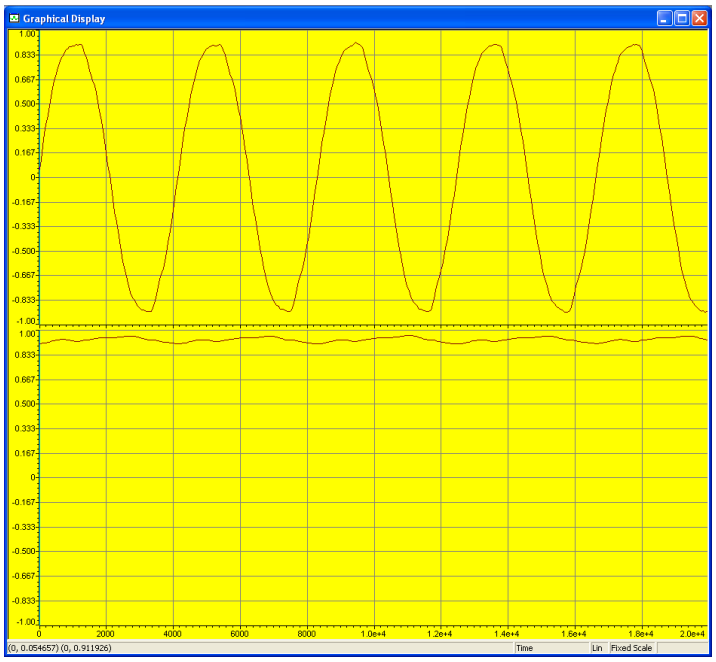

Figure 4.4. The measured signal and the corresponding amplitude signal "A"

By subtracting the signal "A" from the ideal voltage level, 1 pu, the voltage sag could be detected. The comparison of this value with the limit value of 10% (0.1 pu) points to a voltage sag. V_s is the voltage sag level. The voltage sag detection using PLL is illustrated in Figure 4.5. As it can be seen, the voltage sag detection can

be easily done with this method. When the value of "(1-A)" raises above the hysteresis threshold of 0.1, the sag detection signal is activated.

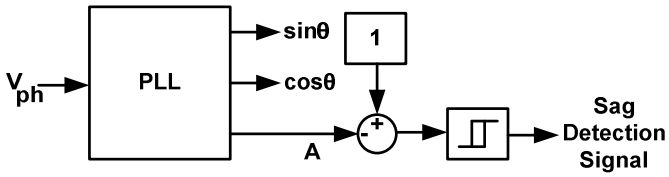

Figure 4.5. Block diagram of PLL sag detection method

4.1.1.3. Voltage Compensation Method

When the supply voltage is unbalanced and contains harmonics, most of the methods in literature have drawbacks. A simple control algorithm for DVR is developed. With the method, DVR is not affected from unbalanced voltages or harmonics. The method used the study directly calculates compensation voltages without time delay, compensates for the faulted voltages dynamically in the time domain. For the voltage compensation, another property of the PLL is used. As it was, the output "y(t)" is an extracted signal from the input "u(t)" having the amplitude "A" and phase "Φ" of the input "u(t)". In this way, distortions in the supply line are perfectly filtered. Measured supply voltage "u(t)" is shown in the upper part and extracted "y(t)" is shown in the lower part of Figure 4.6.

In the proposed method "y(t)" and a reference sinusoidal signal "x(t)" having 1 pu magnitude and "Φ" as the phase angle is used. "x(t)" having 1 pu magnitude and "Φ" as the phase angle is shown in the upper part and extracted "y(t)" is shown in the lower part of Figure 4.7.

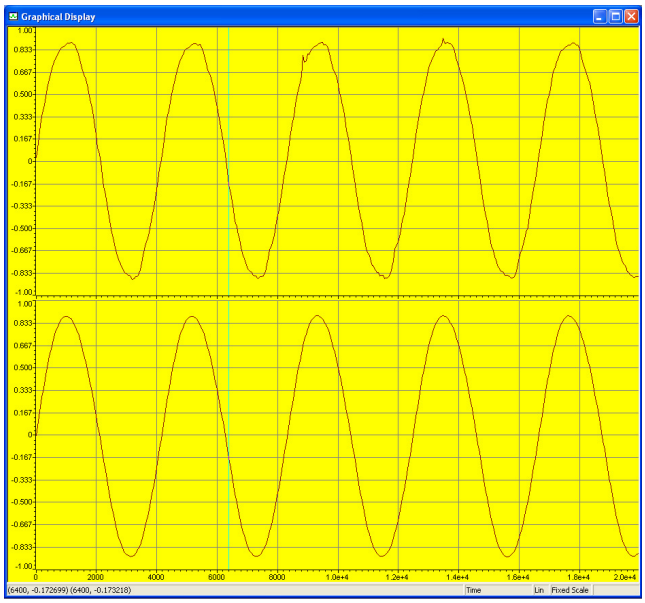

Figure 4.6. Measured supply voltage “u(t)” and extracted “y(t)”

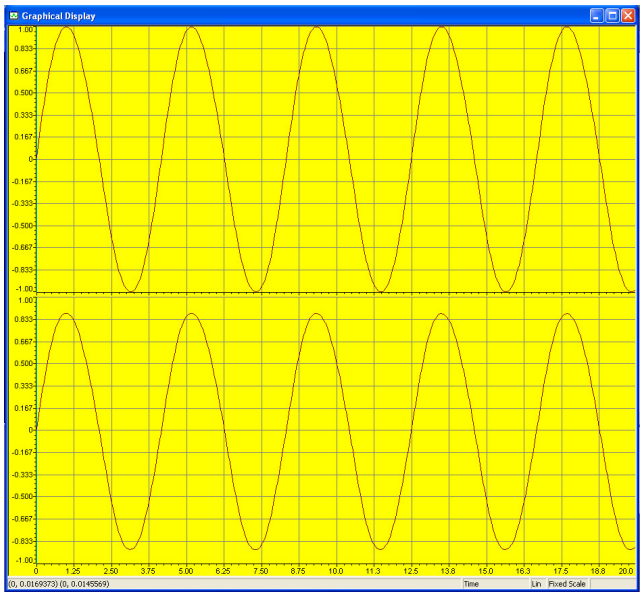

Figure 4.7. Reference signal “x(t)” (top) and extracted “y(t)” (bottom)

Reference voltage compensation signal is generated from the difference of “y(t)” and “x(t)”. Equation (4.7) gives the reference voltage.

$$V_{ref} = x(t) - y(t) \tag{4.7}$$

This reference voltage compensation signal is compared with a fixed frequency carrier wave to generate the PWM firing pulses for the IGBTs. In this way, the voltage in the same phase with supply generated by the DVR voltage source inverter is injected to the line and is added over the sagged voltage to avoid the load being affected from the source side sag.

4.1.1.4. DSP Software Flowcharts for Dynamic Voltage Restorer

TMS320F2812 ezDSP board is used in the experimental study. This board has built in ADC module and PWM modules to control the DVR. All the required coding is made in C language. The flowcharts for the proposed control algorithm and explanatory information are given in this section.

The processor timer of F2812 DSP is used to generate the timing interrupts to determine the sampling time. The control algorithm starts with a "main" function and then waits for the timer interrupt.

The flowchart of the proposed control algorithm is given in Figure 4.8. The processor starts with C_int0 interrupt and runs the "main" function given in the left hand side of Figure 4.8. In the main function, first of all the global variables that will be used through out the entire control algorithm is defined and initialized. Then software modules that let the programmer to develop the algorithms by the use of object oriented approach are initialized. Here after, the processor timer (CPU Timer 0), is adjusted to determine the sampling interval. The sampling time is selected to be 20 μs. The PWM modules are then set to give the required outputs. The carrier wave frequency of PWM modules are also set to be 10 KHz. In the last step, to get the voltage measurements, ADC module is initialized. After the completion of all required initialization work, the processor sits for an endless loop and waits for processor timer interrupt, INT1.

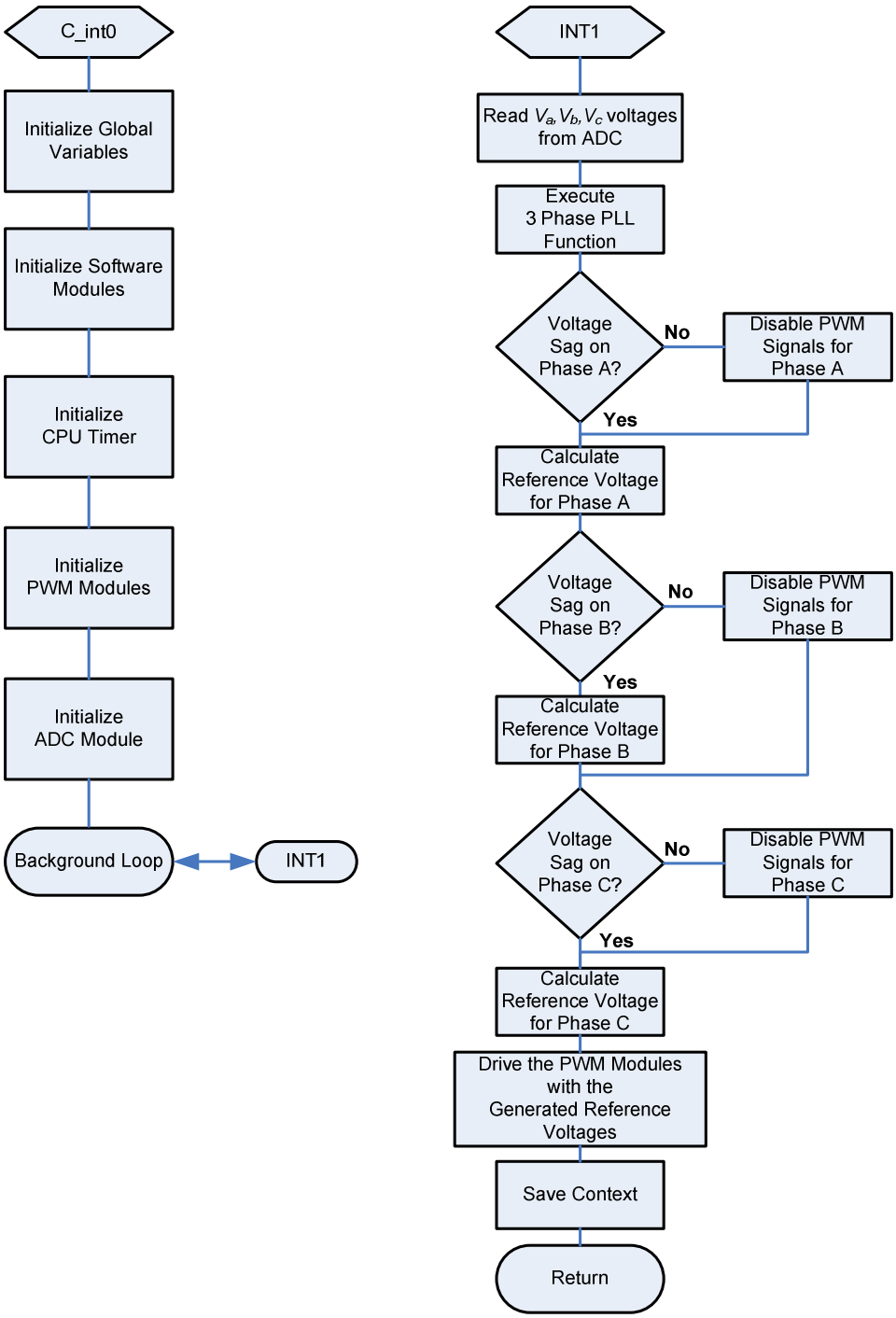

Figure 4.8. The flowchart for the proposed control algorithm of DVR

The CPU Timer calls the interrupt service routine INT1 shown in the right hand side of the Figure 4.8 periodically at each 20 μs. In this routine, the ADC module is driven to read the three phase set of voltages and converts them in per unit equivalents. Then these converted voltages are subjected to three phase PLL function. Using the values obtained from PLL function, each phase is controlled for a sag by sag detection function and whenever a sag detected, the reference signal for that phase is calculated otherwise the PWM module for that phase is disabled during that sampling interval. Finally, the calculated reference signals for the phases, that a sag detected, is compared with the PWM carrier wave and PWM gate pulse signals for those phases are generated.

The flowchart of the three phase PLL function is shown in Figure 4.9. The function takes the measured phase-to-ground voltages as parameter. Then the error signals for each phase are determined. The values for the sine and cosine are calculated. Next the amplitudes for phases are determined. Product of the amplitude "AA" with "sinwt" gives the "ya" that is the filtered copy of phase A generated by PLL. Likewise "yb" and "yc" is calculated. The phase angles are determined next. Each phase angle is restored to zero after a period of 2π.

ea, eb and ec: error signals determined for phases A, B and C respectively.

ua, ub and uc: measured phase-to-ground voltages in pu.

ya, yb and yc: filtered copy of phases A, B and C.

AA, AB and AC: calculated amplitudes for phases A, B and C.

phiA, phiB and phiC: calculated phase angles for A, B and C phases.

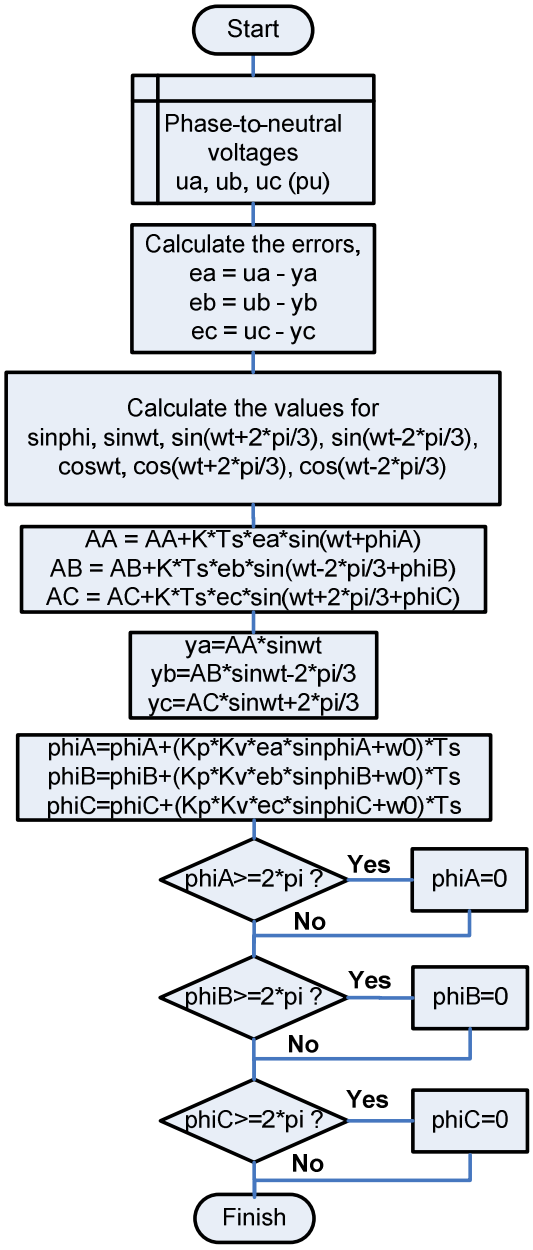

Figure 4.9. The flowchart of the three phase PLL function

Figure 4.10 shows the flowcharts for sag detection function on the left hand side and on the right hand side the hysteresis function used in sag detection function. As it explained before, the sag detection function is based on PLL variables. Each of the phase amplitudes “AA”, “AB” and “AC” obtained from PLL is subjected to the

hysteresis function and the sag is determined by the result coming from the hysteresis function.

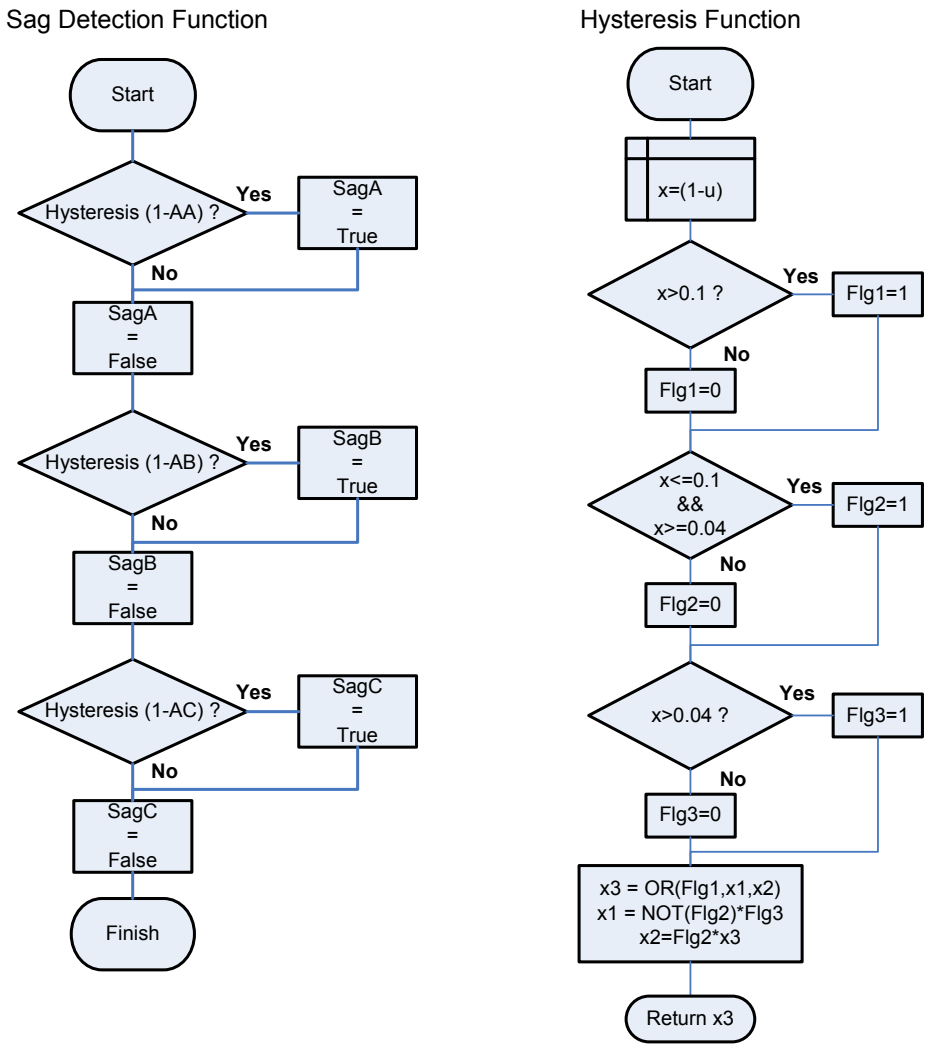

Figure 4.10. Flowcharts for sag detection and hysteresis functions

Hysteresis function has the duty of stabilizing the sag signals. Because harmonics and measurement noises affect the stability of the sag detection. The sag signal is set when the input signal to the hysteresis function exceeds the 0.1 sag limit and reset when the signal falls below 0.04. The functional block diagram of the hysteresis function is given in Figure 4.11.

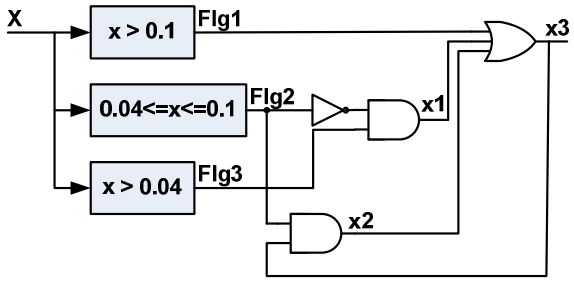

Figure 4.11. Block diagram of hysteresis function

To conclude, the control algorithm periodically reads the supply voltage and determines the voltage sags on each phase independently. If it detects a sag on a phase, it drives the H-bridge inverter of that phase only. The C implementation of DVR controller is given in Appendix B, Listing B.1. In the following section, the experimental results are discussed.

4.1.2. Hardware Design of DSP based Dynamic Voltage Restorer

In this section, experimental setup of the DVR is described and equipments used in the study are explained. Then control algorithms developed for DVR are presented. Required explanatory information about the experimental results is also given.

The power circuit of the DVR is composed of voltage source converters, DC power supply, LC filters and injection transformers as shown in Figure 4.12. A regulated constant DC power supply is employed as energy storage. Three single-phase H-bridge PWM inverters consisting of IGBT switches are used in the voltage source converter circuit. Use of single-phase H-bridge PWM inverters in DVR power circuit makes possible the injection of positive, negative and zero sequence voltages. The inverter side filtering is preferred in this study. Using this filtering scheme, the higher order harmonic currents are prevented from penetrating into the series transformer, thus reducing the voltage stress on the transformer. Voltage Source Inverter (VSI) rating is relatively low in voltage and high in current due to the use of step-up injection transformers.

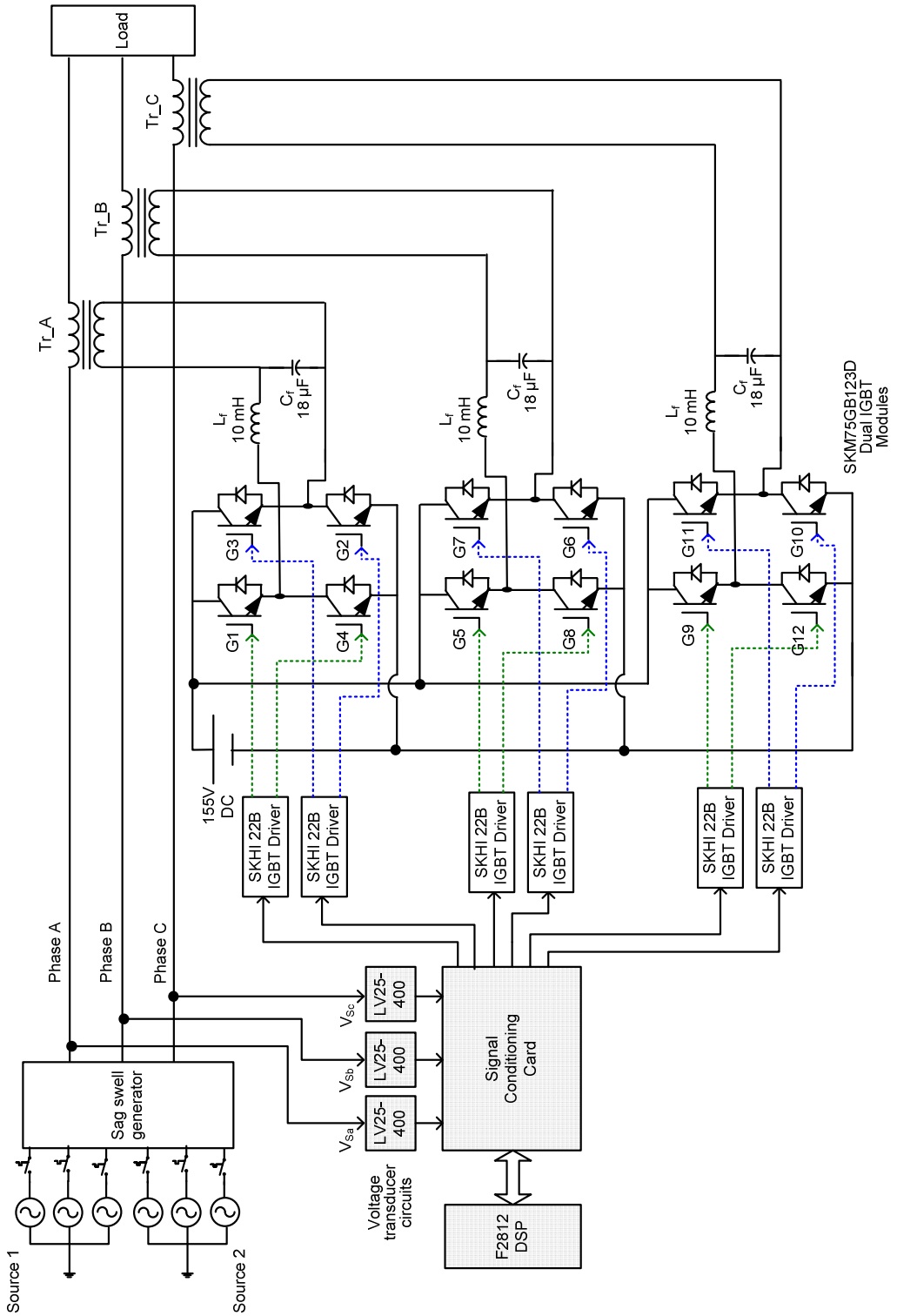

Figure 4.12. Experimental block diagram of DVR

Voltage sag/swell generator is feeding the load through the series injection transformers of the DVR. Each inverter output is filtered out by an LC filter to eliminate the higher order harmonics generated by the inverter itself. The filtered output of the IGBT inverters are connected to the primary side of the injection transformers thus enabling the injection of the missing voltage to the load.

Three LEM LV25-400 voltage transducer cards are used to measure the source voltages. Signal conditioning board is responsible for input and output signal conditioning for DSP controller. Six SKHI 22B IGBT driver circuits drive six Semikron SKM75GB123D dual IGBT modules.

The parameters of designed DVR are given in Table 4.1.

Table 4.1. Parameters of proposed DVR

Description	Value / profile
Fixed Source	Phase to neutral 220 V_{rms}
Variable Source	Phase to neutral 0-220 V_{rms}
Load impedance / per phase	48 Ω
Injection transformer	Single phase, 1:1, 1 kVA
Filter capacitor and inductor	18 μF and 10 mH
Voltage source inverter of DVR	Three single phase H-bridge inverter
DC source of DVR	155 V
Sample time	20 μs

4.1.2.1. Voltage Transducers

The three phase set of voltages are measured from the source side by using LEM LV25-400 transducer cards. A transducer card is used for each phase. The card is adjusted to read 220 V_{rms} and convert it into 1.5 V_{pk}. LEM LV25-400 is a standard measurement card built by using LV25-P voltage transducers. One can think that it as a current transformer of ratio 10mA (primary)/25mA (secondary). In other words, when a current flows in the primary side of voltage transducer as a result of applied voltage, the transducer outputs a current from the secondary side 2.5 times greater than the primary current flows through it. The rated primary current is 10 mA, in the case of LV25-400 the peak value of measured voltage is 400V. To limit the primary current to 10 mA where the applied voltage is 400V, a 40K resistor is used to reduce

the primary current to the desired level. The transducer card used in the study is shown in Figure 4.13.

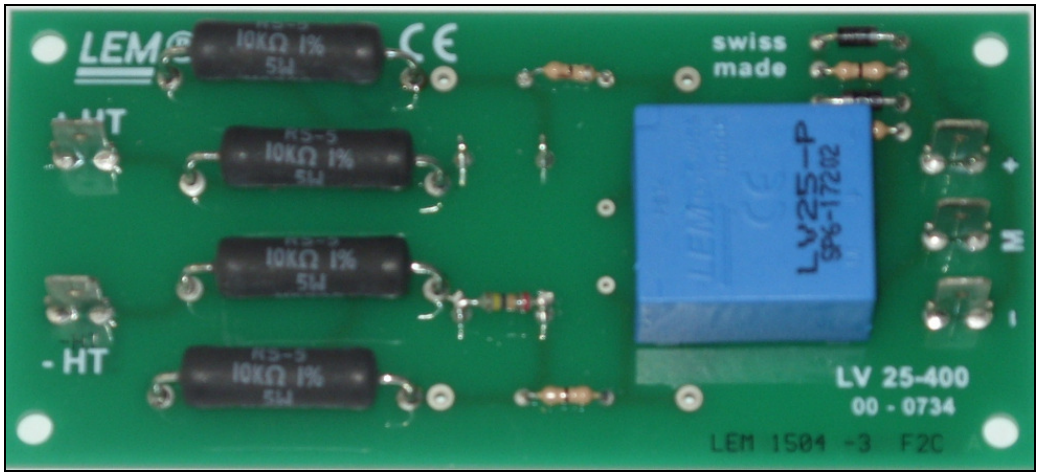

Figure 4.13. LEM LV25-400 voltage transducer cards

The output of the transducer card of a phase when the applied voltage is $220V_{rms}$ is given in Figure 4.14. As the output of the transducer is current, it is converted into voltage by the use of a resistor.

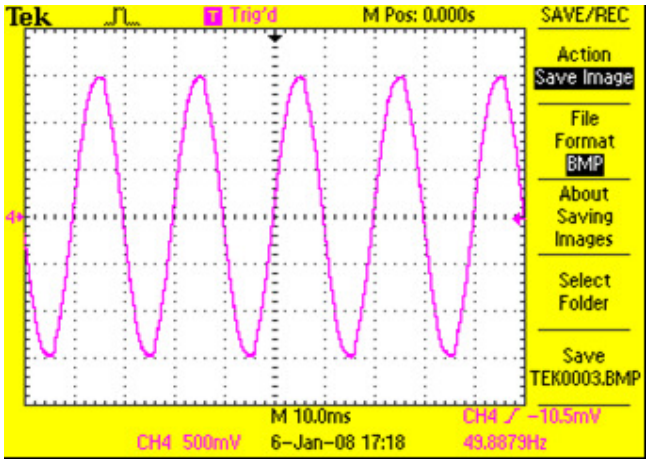

Figure 4.14. Output waveform for the voltage transducer card of a phase

4.1.2.2. TMS320F2812 DSP Controller Outputs

The digital outputs of the F2812 are rated at 0-3.3V_{pk} as the supply voltage of the controller is also 3.3V. Each output can deliver 2 mA of current. The digital output waveform of the DSP is shown in Figure 4.15.

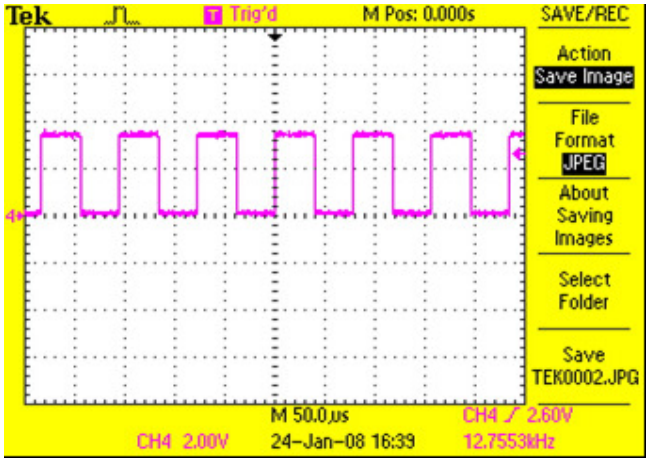

Figure 4.15. Waveform of a digital output of DSP

4.1.2.3. Signal Conditioning Card

F2812 DSP controller analog inputs are rated at 0-3 V_{pk}. However, as it can be seen from the Figure 4.12, the voltage transducers output 1.5V_{pk} sinusoidal. The signal conditioning card is used to add 1.5 V_{dc} offset to the transducer outputs and buffering DSP outputs. By this way, the analog input signals are increased to the 0-3V_{pk} level and 3.3V_{pk} outputs of DSP is increased to 3.9V_{pk} level.

The circuit diagram of input section of signal conditioning card is shown in Figure 4.16. The output of each voltage transducer is connected to the input section of signal conditioning card as can been seen from the left side in Figure 4.16. Voltage transducers outputs a current proportional to voltage applied to its primary. This current is converted into voltage as the analog inputs needs voltage signals by the use of a scaling resistor. For buffering and protection, a voltage follower is used to after the scaling resistor. Voltage follower shows very high impedance to its

primary and nearly zero to its secondary. The required $1.5V_{dc}$ offset voltage is generated by a voltage divider and than buffered with a second voltage follower. A non inverting adder is used to add the $1.5V_{dc}$ offset and measurement signal. The output of the non inverting adder which is in the range of $0\text{-}3V_{pk}$ is applied to analog inputs of DSP controller.

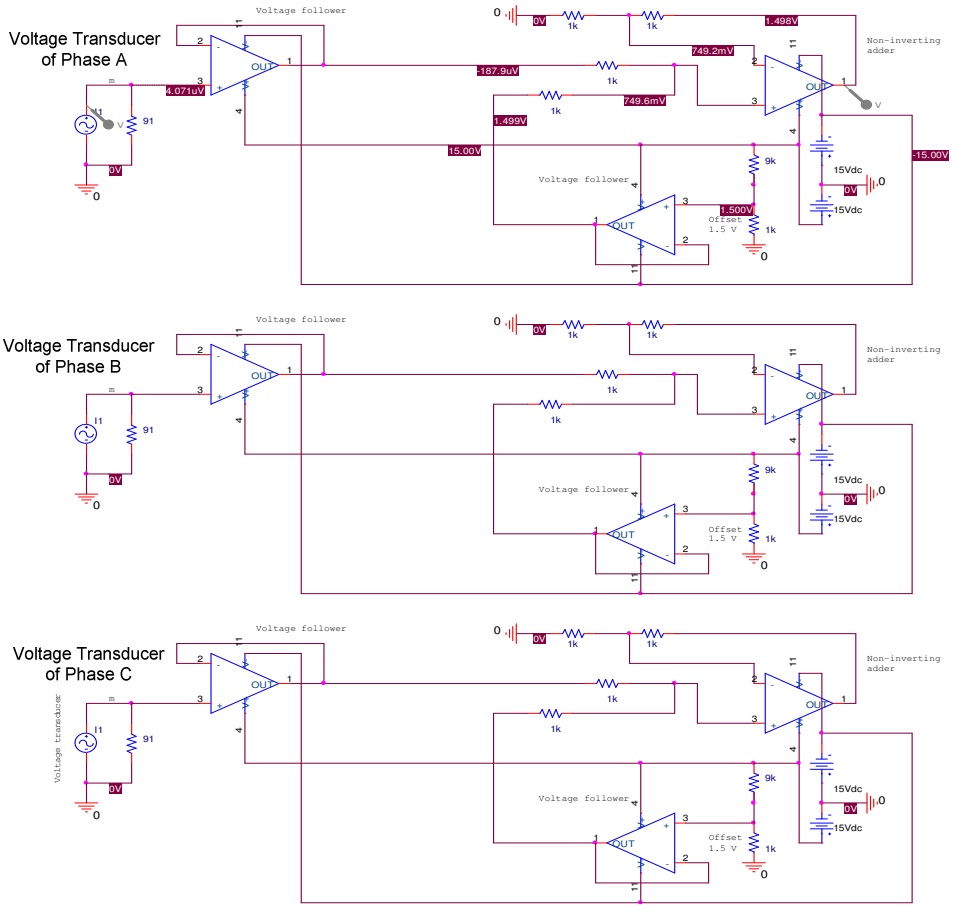

Figure 4.16. Circuit diagram of input section of signal conditioning card

The printed circuit board (PCB) of the card is presented in Figure 4.17. In Figure 4.18, the output waveform for input section of signal conditioning card is shown.

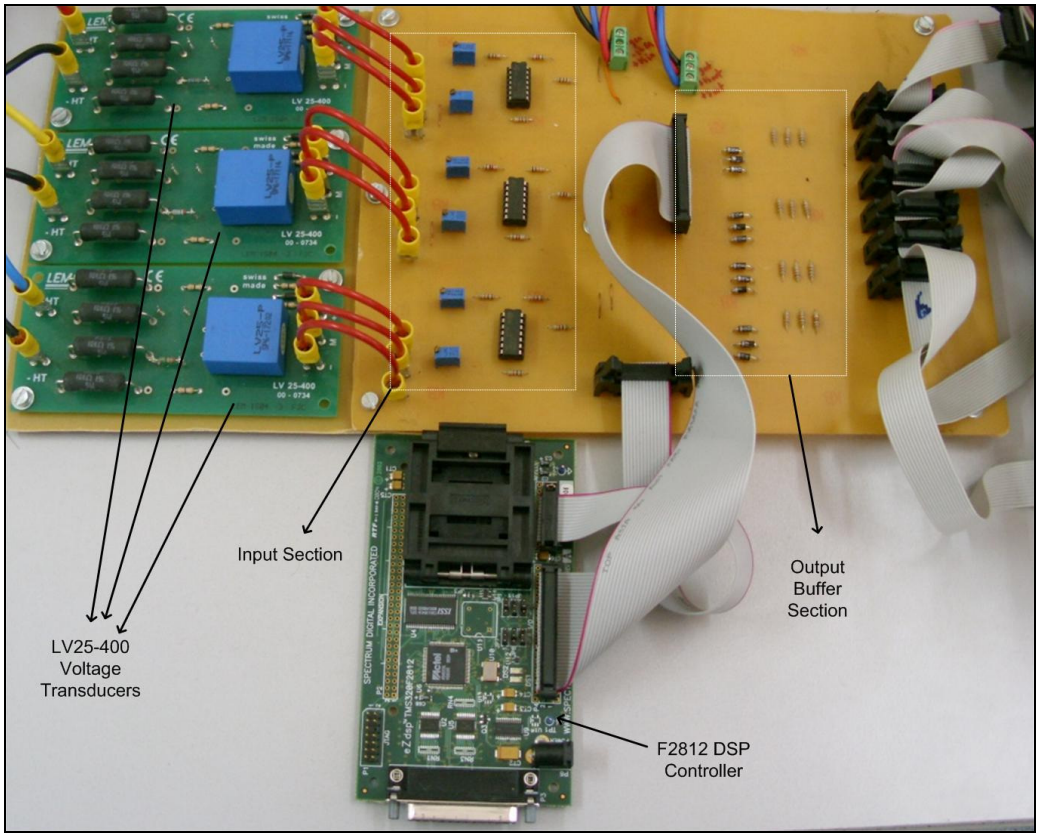

Figure 4.17. Picture of signal conditioning card

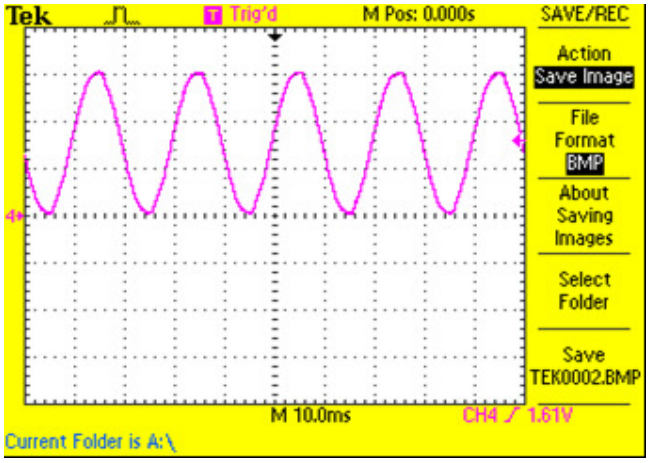

Figure 4.18. Output of input section of signal conditioning card

IGBT driver circuit inputs are 0-5V_{pk} CMOS compatible. However, the digital outputs of the DSP are rated at 0-3.3V_{pk}. To overcome this issue, an output

buffer is designed and used. Figure 4.19 shows the circuit diagram of output buffer section of signal conditioning board for phase A. The output buffer uses very simple principle and it is an efficient and easy way to interface 3.3V level to 5V level. The 0.6 V diode voltage drop is used to increase the output voltage level to 3.9 V that is permissible by the IGBT driver cards. PWM_1, PWM_2, PWM_3 and PWM_4 are the DSP outputs and Vo_1, Vo_2, Vo_3 and Vo_4 are the buffer card outputs, respectively. 1K resistors are used to limit the current. The output waveform of the output buffer section of the card is given in Figure 4.20.

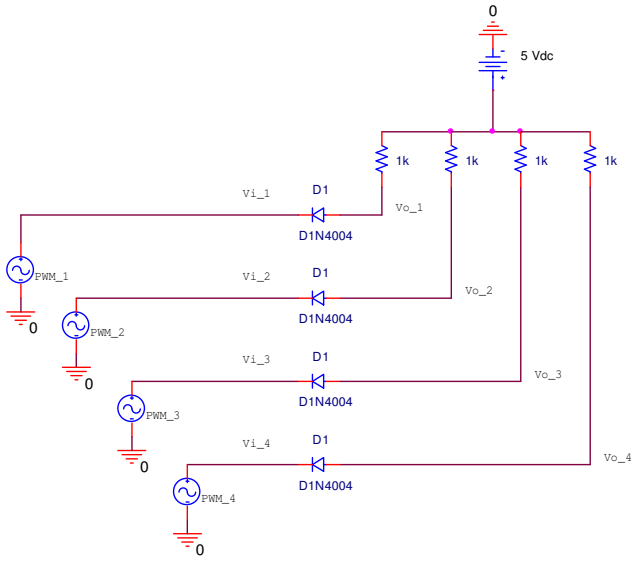

Figure 4.19. Circuit diagram of output buffer card for phase A

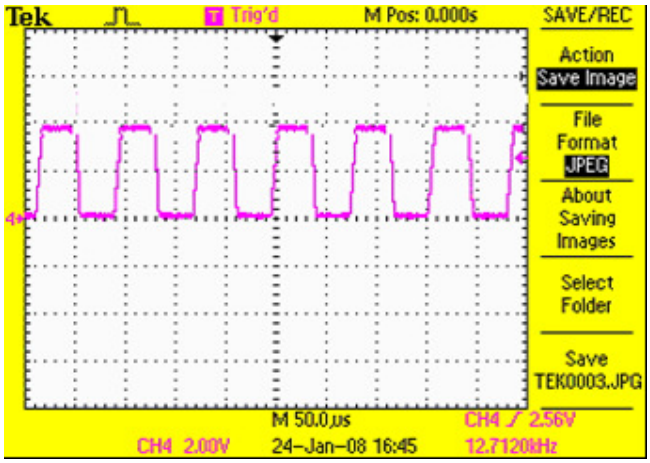

Figure 4.20. Output waveform of buffer card

4.1.2.4. IGBT Driver Circuits

Semikron SKHI22B H4 IGBT drivers are used in this study. These cards output (-7)V - (+15) V_{pk} that are needed to turn off and turn on an IGBT, respectively. Each of the IGBT driver drives two IGBTs on the same leg of the inverter. These drivers have several integrated features such as IGBT over voltage and over current protection, dead band generation, top and bottom IGBT isolation. The block diagram of IGBT drivers is illustrated in Figure 4.21. In this study, SKPC22 circuit board which is available in the market is used to construct the IGBT driver circuits. SKPC22 board gives the opportunity of using the IGBT driver in different configurations.

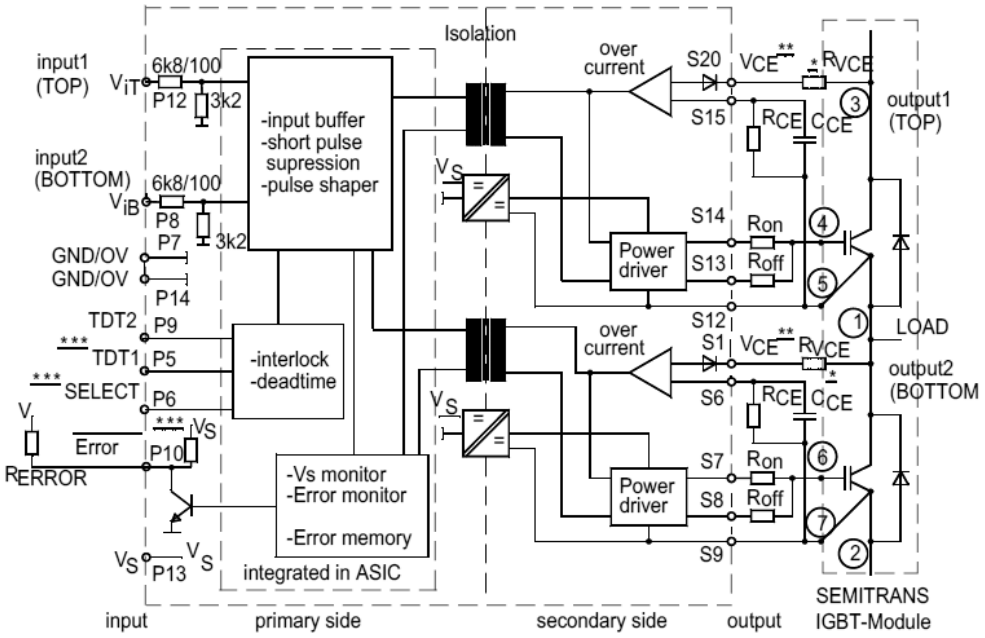

Figure 4.21. Semikron SKHI 22B H4 IGBT driver block diagram (Semikron, 2008)

Figure 4.22 shows an SKPC22 board with SKHI22B H4. The 14 pin connector on the left hand side is connected to the output buffer card and the two 4 pin connectors on the right side is connected to an IGBT module.

Figure 4.22. A picture of IGBT driver circuit

The IGBT drivers apply +15V to the gate-emitter of an IGBT when the input signal is logic high and -7V when the input signal is logic low. The gate resistors are selected as 22 ohms. The output waveform of an IGBT driver circuit is given in Figure 4.23.

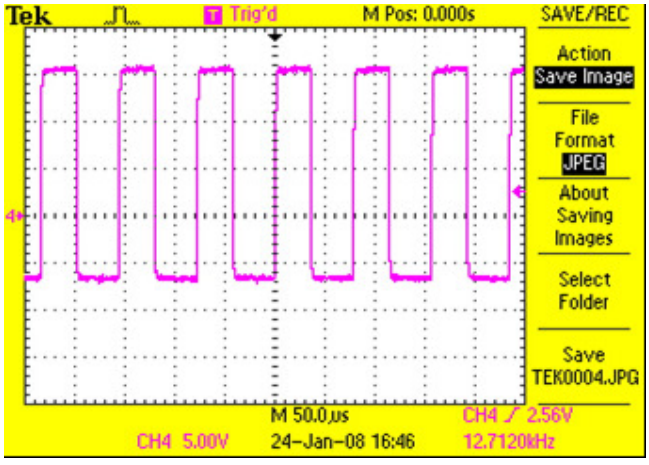

Figure 4.23. Output waveform of an IGBT driver circuit

4.1.2.5. H Bridge Inverters

The circuit diagram of a single phase H bridge inverter is given in Figure 4.24. Semikron SKM75GB123D IGBT modules are used to construct the H bridge inverters. Each IGBT module consists of two IGBTs connected in top bottom configuration. The inverters are fed from a 155 V_{DC} source and output 110 V_{AC}. These voltages are filtered and injected to the lines through injection transformers. The three phase H-bridge inverters used in the study are shown in Figure 4.25.

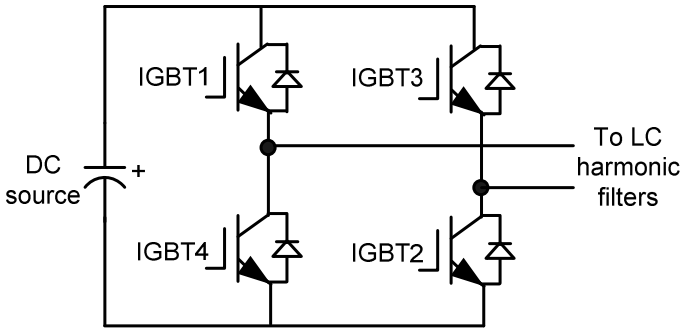

Figure 4.24. Single phase H bridge IGBT inverter

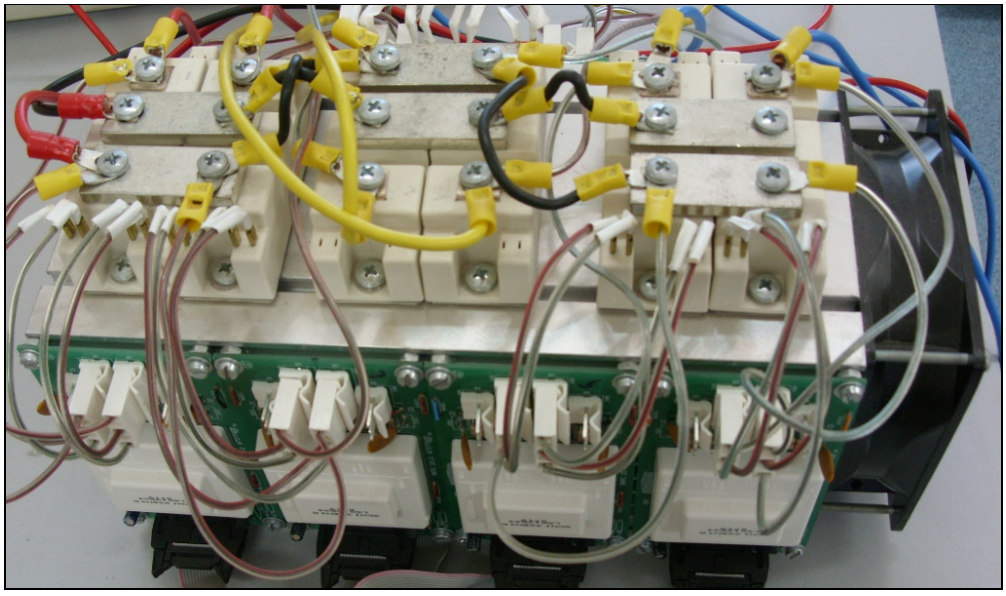

Figure 4.25. Three phase H bridge IGBT inverter used in DVR

4.1.2.6. LC Output Filter

To filter out the harmonics generated by the H bridge inverters of the DVR, a LC filter is added in the output of each single phase inverter. The values of filter inductor L_f and filter capacitor C_f is determined by the method presented in (Dohano et al., 1995). The modulation index and a K factor is used to calculate the filter inductance and capacitance.

$$k = \sqrt{2}\frac{V_o}{E_d} \tag{4.1}$$

where E_d is the DC source voltage and V_o is the nominal load voltage. k is the modulation index.

$$K = \sqrt{\left(\frac{k^2 - \frac{15}{4}k^4 + \frac{64}{5\pi}k^5 - \frac{5}{4}k^6}{1440}\right)} \tag{4.2}$$

Equation (4.3) gives an optimum value for filter inductance and Equation (4.4) is used to calculate the value of filter capacitance.

$$L_f = \frac{V_o}{I_o f_s}\left\{K\frac{E_d}{V_{o,av}}\left[1 + 4\pi^2\left(\frac{f_r}{f_s}\right)^2 K\frac{E_d}{V_{o,av}}\right]\right\}^{1/2} \tag{4.3}$$

f_s is the switching frequency, $V_{o,av}$ is the total harmonic of the load voltage, f_r is the fundamental output frequency.

$$C_f = K\frac{E_d}{L_f f_s^2 V_{o,av}} \tag{4.4}$$

Using the above equations 4.3 and 4.4, L_f is calculated as 10 mH and C_f as 18 μF.

4.2. Simulation of Dynamic Voltage Restorer

The simulation model of DVR is given in Figure 4.26. All parameters used in simulation model are set by measuring the real values of laboratory prototype. This lets the results of simulation and experimental works be nearly same. Below, the components of the DVR are described.

In left side of Figure 4.26, voltage sag/swell generator could be seen. The voltage sag/swell generator is used to generate voltage sags and swells to test the DVR. It is formed by using two different AC sources adjusted to different voltage levels. A timed logic is used to open and close the required breakers to form the voltage sags. These breakers are used to change the power supply of the test load. Power supply voltages are measured from the output of the sag/swell generator. The sensitive load is supplied via series injection transformers of DVR.

Three single phase H bridge IGBT inverters are used to generate the missing voltage to the load. The outputs of the IGBT inverters are voltage pulses, to generate a sine wave from these pulses; a LC filter is used at the outputs of each inverter. Those filtered outputs are used to supply the primaries of injection transformers.

DVR controller is responsible to detect the voltage sags and swells. Also it is responsible to generate the missing voltage by using sinusoidal pulse width modulation technique.

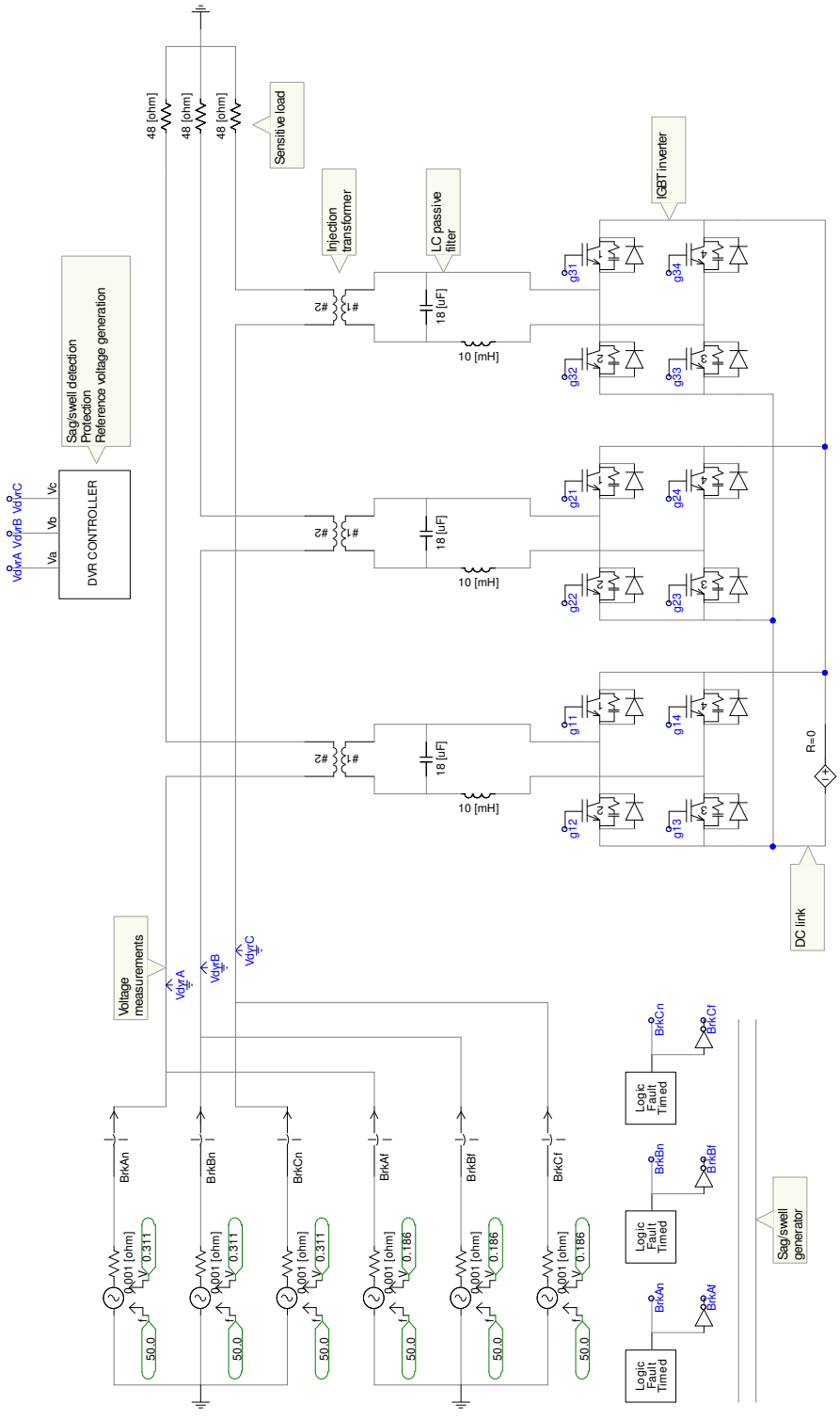

Figure 4.26. Simulation model of DVR

4.2.1. Simulation Results of Dynamic Voltage Restorer

In this section, the simulation results are analyzed and discussed. Several case studies are created that are the single phase 20% voltage sag, three phase 20% voltage sag, single phase 40% voltage sag and three phase 40% voltage sag.

4.2.1.1. Case 1: Single Phase, 20% Voltage Sag

During this case, the single phase fault starts at 0.2 seconds and lasts for 0.3 seconds. The rms trend of load voltage for 0.5 seconds duration is presented in Figure 4.27. As it can be seen from the figure, the load voltage was not affected from the single phase voltage sag.

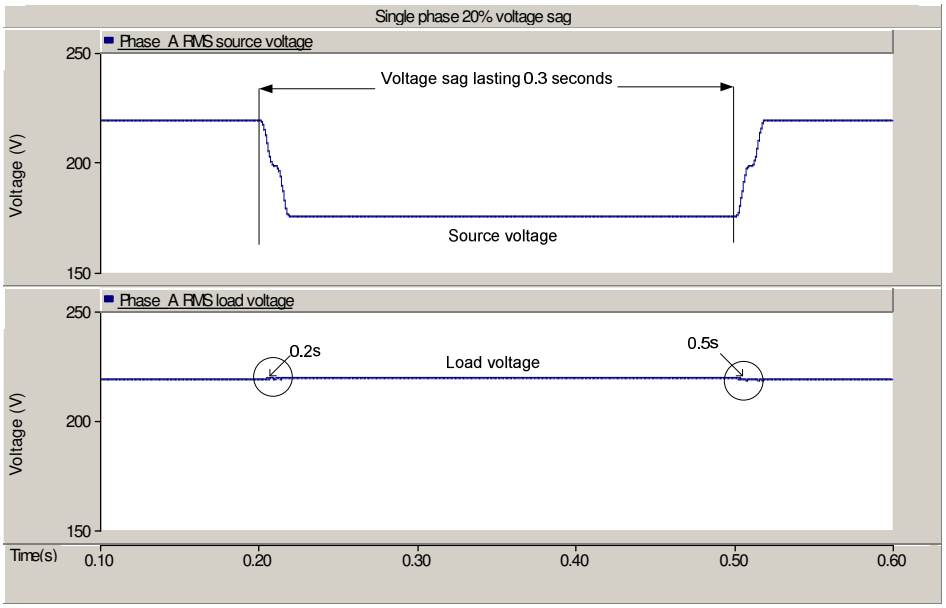

Figure 4.27. Rms voltage trend for phase A of load voltage for Case 1

In Figure 4.28, the waveforms of the source, injected and load voltages and load current waveforms are given. DVR injected a series voltage to the line which equals to the missing voltage. The load voltage is the sum of the source voltage and DVR output voltage. The load currents were not affected from the voltage sag.

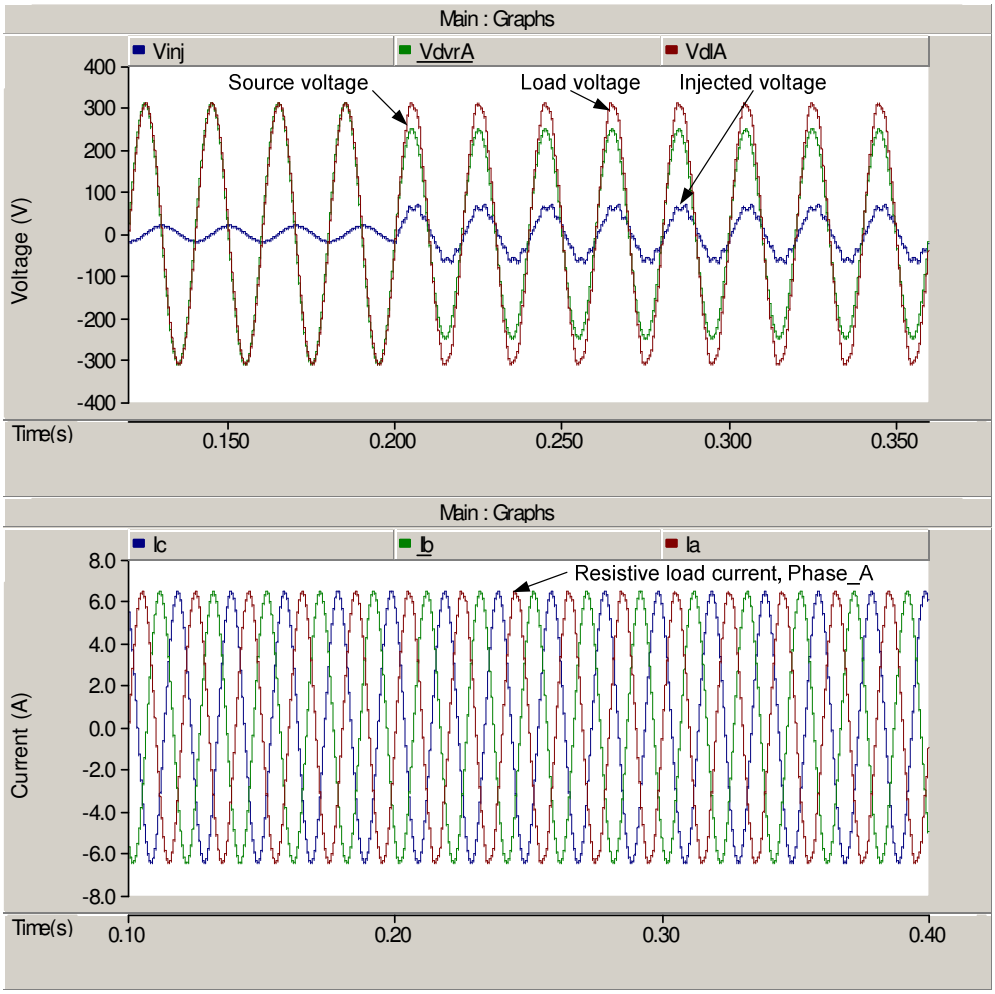

Figure 4.28. Waveforms of load currents and phase A voltages for Case 1

4.2.1.2. Case 2: Three Phase, 20% Voltage Sag

During this case, the three phase fault starts at 0.2 seconds and lasts for 0.3 seconds. Figure 4.29 shows the rms value of load current for 0.5 seconds duration. As it can be seen from the figure, the load current was not affected from the voltage sags occurred. DVR compensated the missing voltages.

Figure 4.30 shows the waveforms of source voltages and load currents during three phase balanced fault.

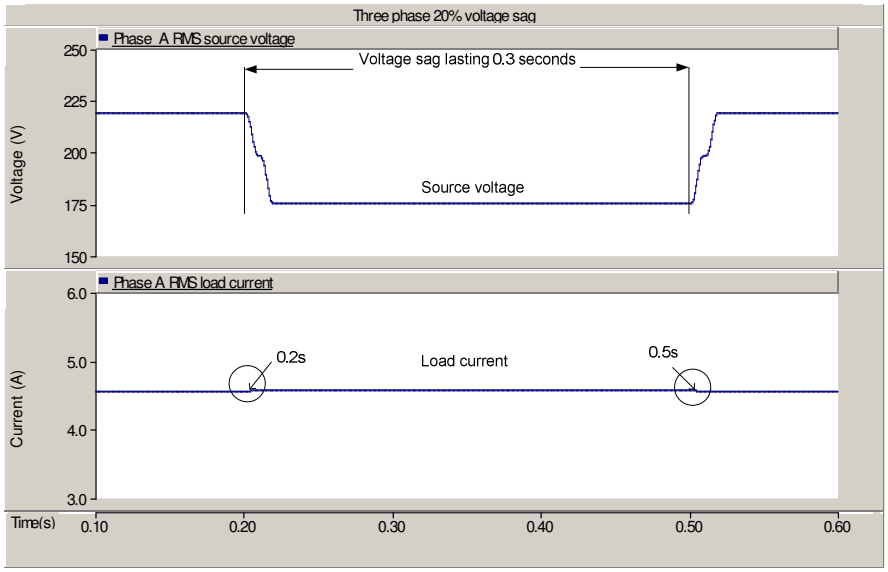

Figure 4.29. Rms values of load current of phase A for Case 2

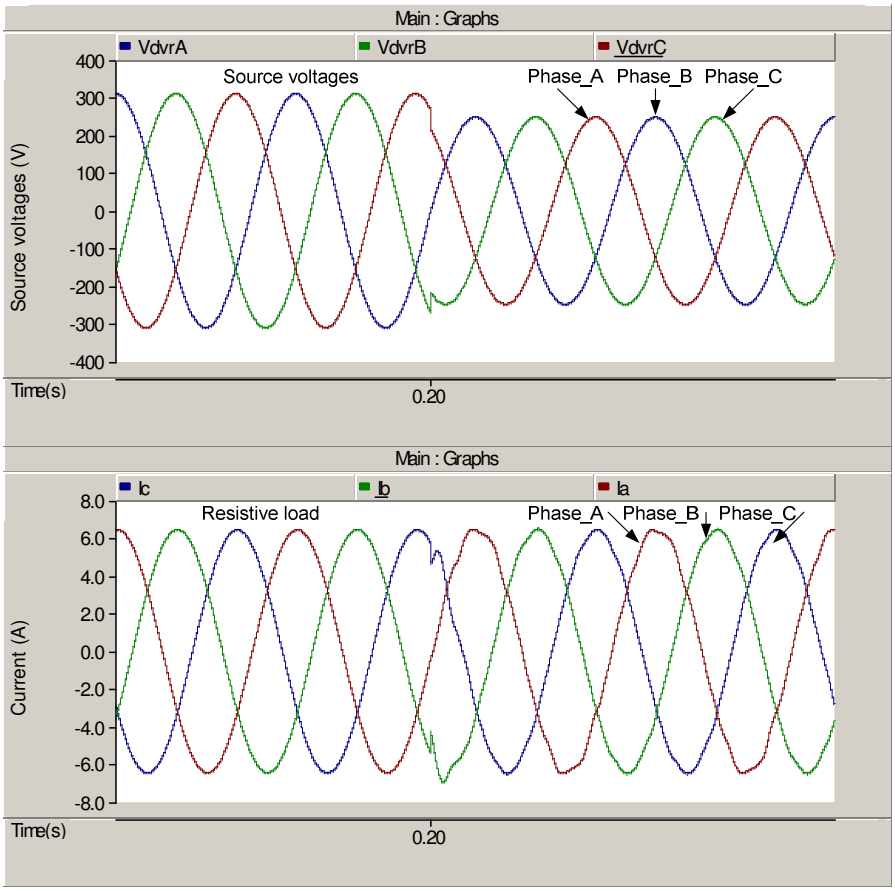

Figure 4.30. Waveforms of source voltages and load currents for Case 2

4.2.1.3. Case 3: Single Phase, 40% Voltage Sag

In this case, a single phase 40% voltage sag is applied to the Dynamic Voltage Restorer for 0.3 seconds of duration. And the rms trend for the phase A is illustrated. The rms trend of phase A during the simulation is shown in Figure 4.31.

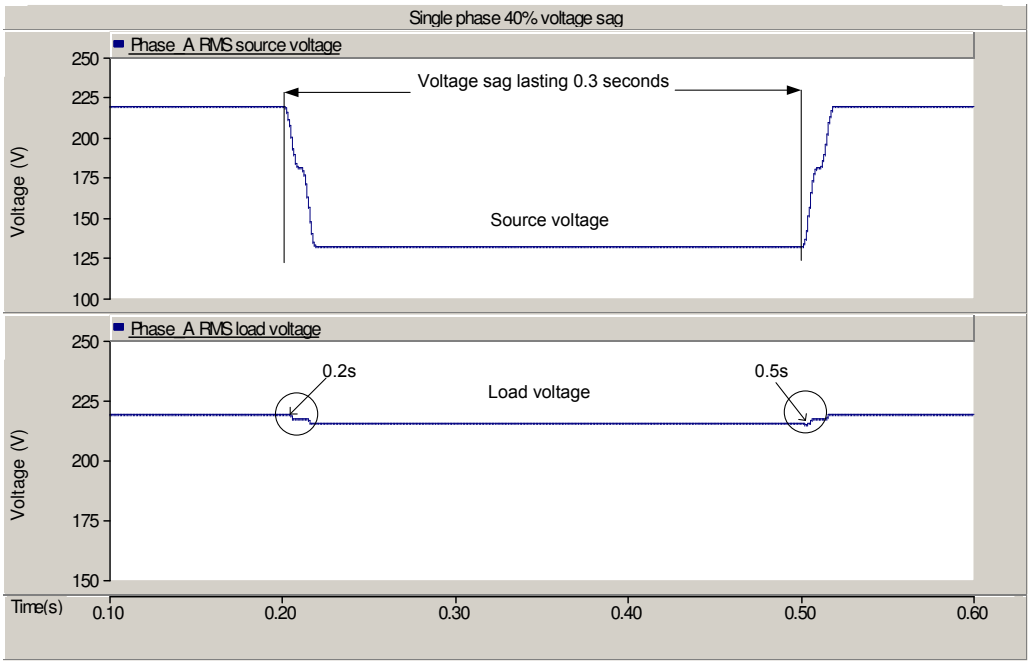

Figure 4.31. Rms values of source and load voltage for phase A for Case 3

For a sag in this interval, the source voltage, injected voltage and load voltage is given in Figure 4.32. Dynamic Voltage Restorer is also able to inject the missing voltage to the line for the 40% sag case. If the DVR voltage in Figure 4.32 investigated before the fault occurs, a voltage drop is seen. This voltage drop is caused by the secondary side of the injection transformers as the inverters are short circuiting the primary side. Although it is not important in laboratory studies, it becomes important when the time to market comes. To reduce this voltage drop, special design injection transformers must be used.

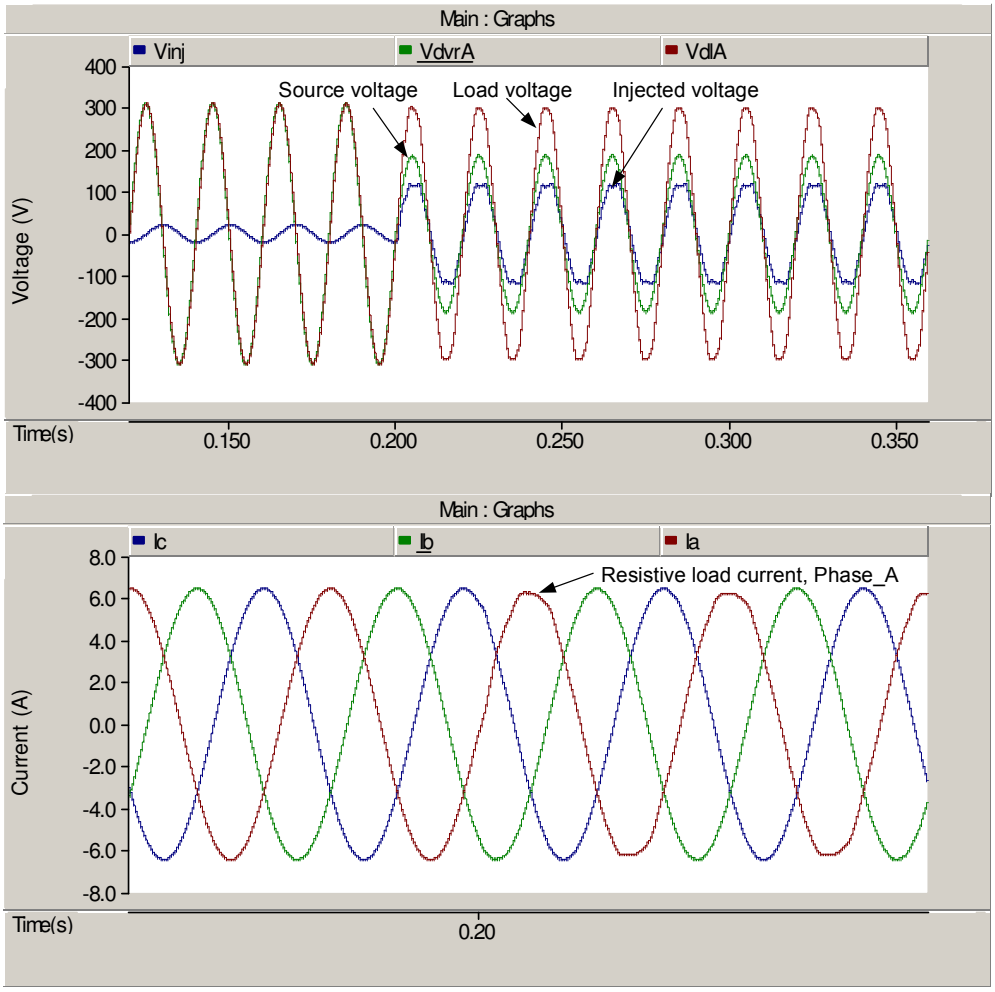

Figure 4.32. Source, injected, load voltage for phase A and currents for Case 3

4.2.1.4. Case 4: Three Phase, 40% Voltage Sag

The last case presents the 40% three phase voltage sag. Figure 4.33 is the rms trend of load current for phase A. DVR immediately starts to inject the missing voltage to the system whenever the voltage sag is detected. The three phase source voltages and compensated load currents are presented in Figure 4.34.

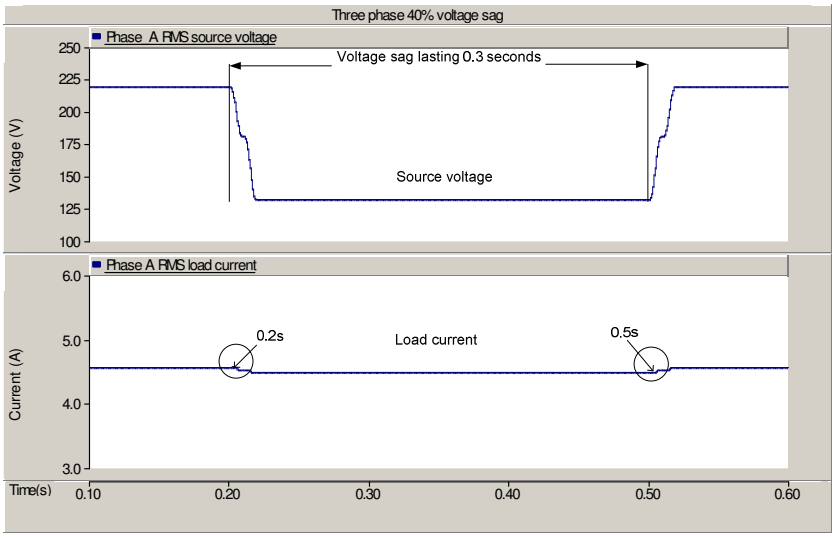

Figure 4.33. Rms values of load current for phase A for Case 4

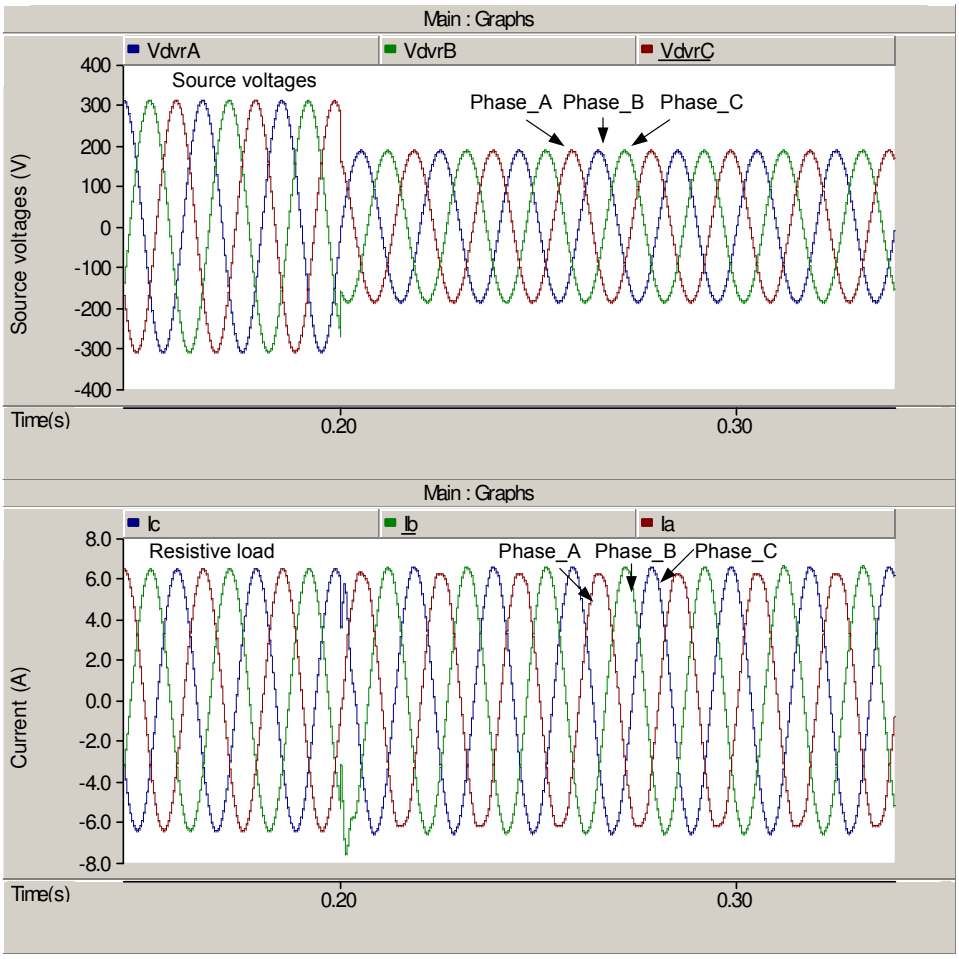

Figure 4.34. Source voltages and load currents for Case 4

4.3. Experimental Results of Dynamic Voltage Restorer

The experimental results taken are discussed in this section. Several case studies are realized. These case studies include single phase 20% voltage sag, three phase 20% voltage sag, single phase 40% voltage sag and three phase 40% voltage sag. The performance of Dynamic Voltage Restorer is evaluated through out the voltage sag tests each of which last 40 seconds. The experimental results are taken from the project "Modeling and Implementation of Custom Power Park" which is supported by Scientific and Technological Research Council of Turkey with project number of 106E188. HIOKI 3196 Power Quality Analyzer is used to record the current and voltage waveforms in the case studies. It has 4 voltage and 4 current channels. For this reason, it is not allowed to record both three phase voltages on source and load side at the same time. However, the load side currents are measured to show the DVR operation. And another limitation of the power quality software is that it can show the rms trend of a measurement only for one phase at a time.

4.3.1. Case 1: Single Phase, 20% Voltage Sag

Figure 4.35 shows the rms values of source voltage on the upper part and load voltage on the bottom part for 40 seconds duration respectively. As it can be seen from the figure, the load voltage was not affected from the voltage sags occurred. In Figure 4.36, source, injected, load voltage and current waveforms are given. The Dynamic Voltage Restorer injected a series voltage to the line which equals to the missing voltage. The load voltage is the sum of the source voltage and DVR output voltage.

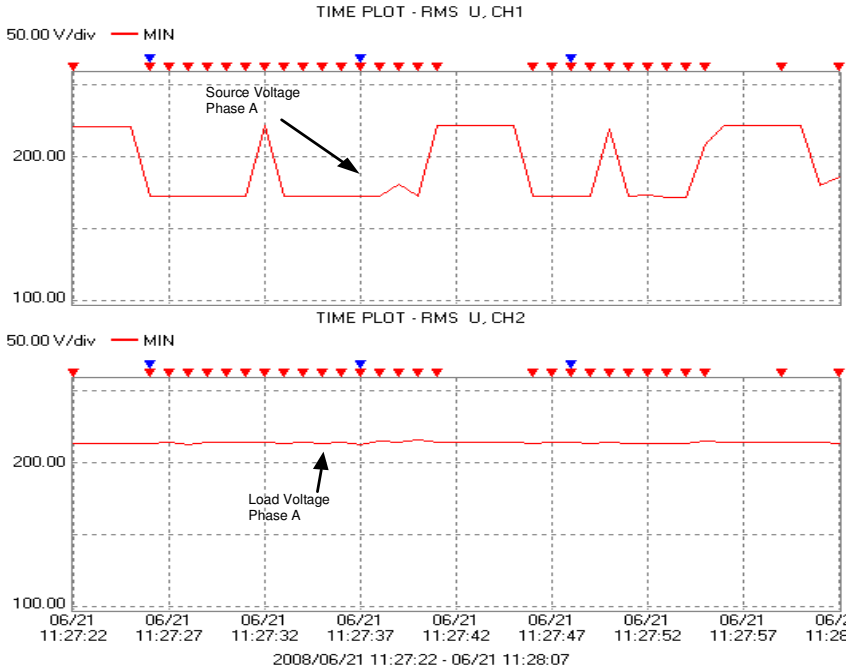

Figure 4.35. Rms values of source and load voltage for phase A for Case 1

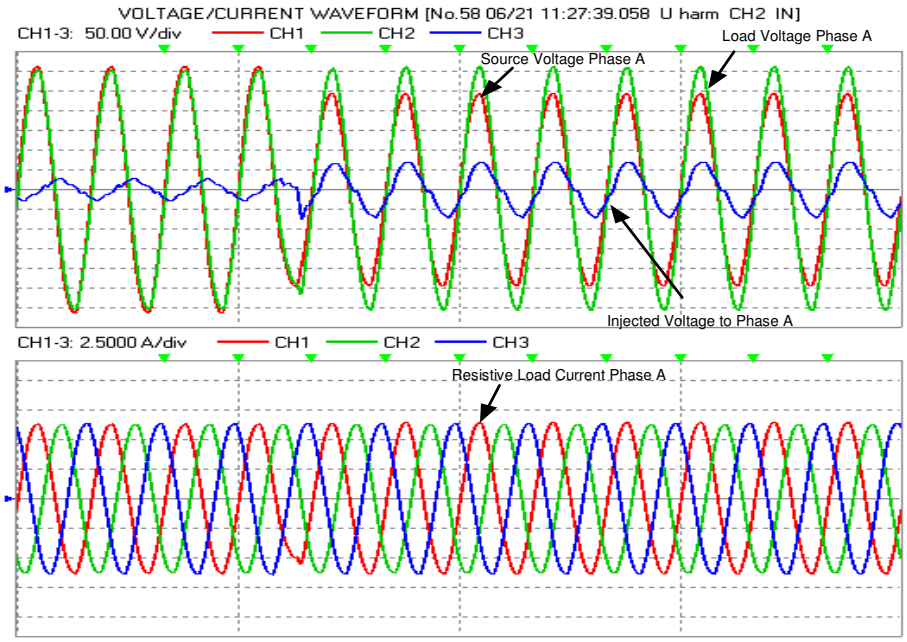

Figure 4.36. Source, injected, load voltage for phase A and currents for Case 1

4.3.2. Case 2: Three Phase, 20% Voltage Sag

Three phase, 20% voltage sag is investigated in case 2. Again, rms trends for the source voltage and load current of phase A is recorded for 40 seconds of duration. In Figure 4.37, only rms values for phase A voltage are shown for the case. Figure 4.38 shows the source voltages on the top and compensated load currents on the bottom.

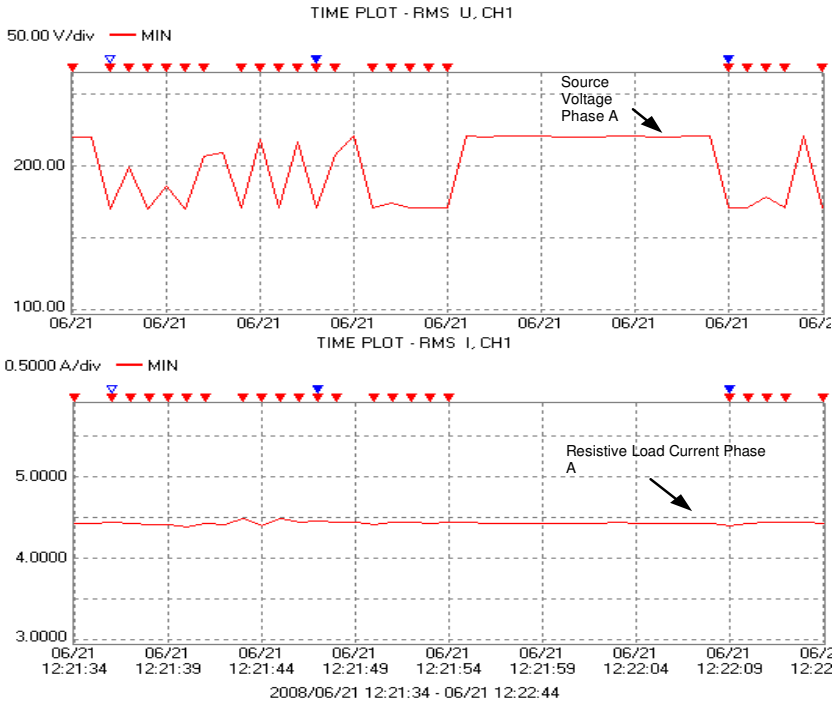

Figure 4.37. Rms values of source and load voltage of phase A for Case 2

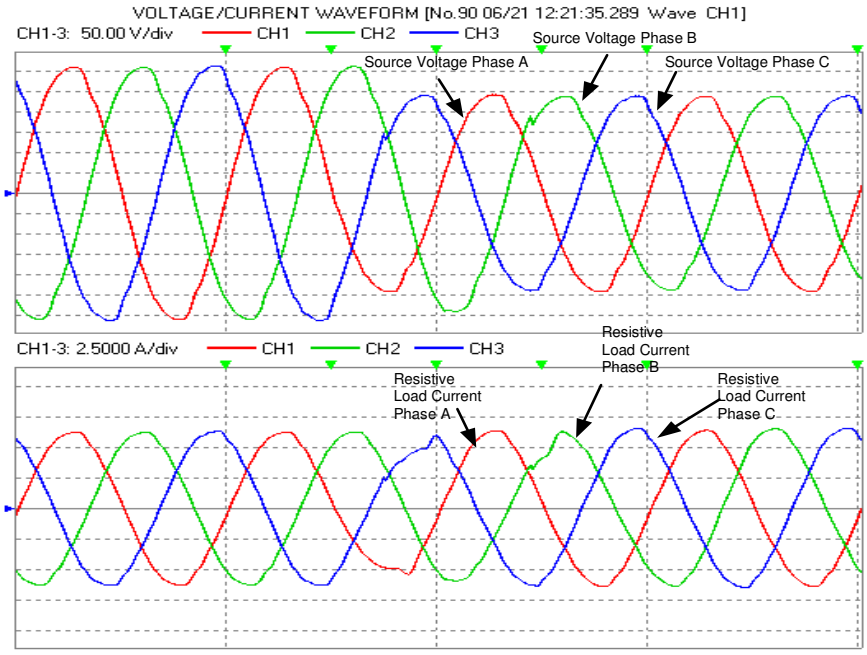

Figure 4.38. Source voltages and load currents for Case 2

4.3.3. Case 3: Single Phase, 40% Voltage Sag

In this case, a single phase 40% voltage sag is applied to the Dynamic Voltage Restorer for 40 seconds of duration and the rms trend for the phase A is recorded. The rms trend of phase A under the test is given Figure 4.39. For a sag in this interval, waveforms of the source voltage, injected voltage and load voltage are shown in Figure 4.40. The Dynamic Voltage Restorer is also able to inject the missing voltage to the line for the 40% sag.

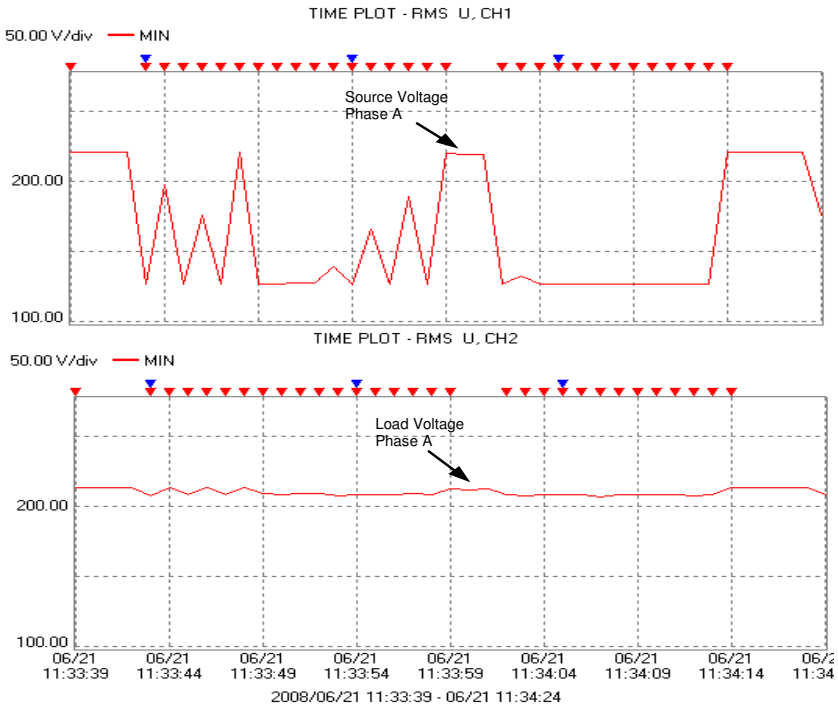

Figure 4.39. Rms values of source and load voltage of phase A for Case 3

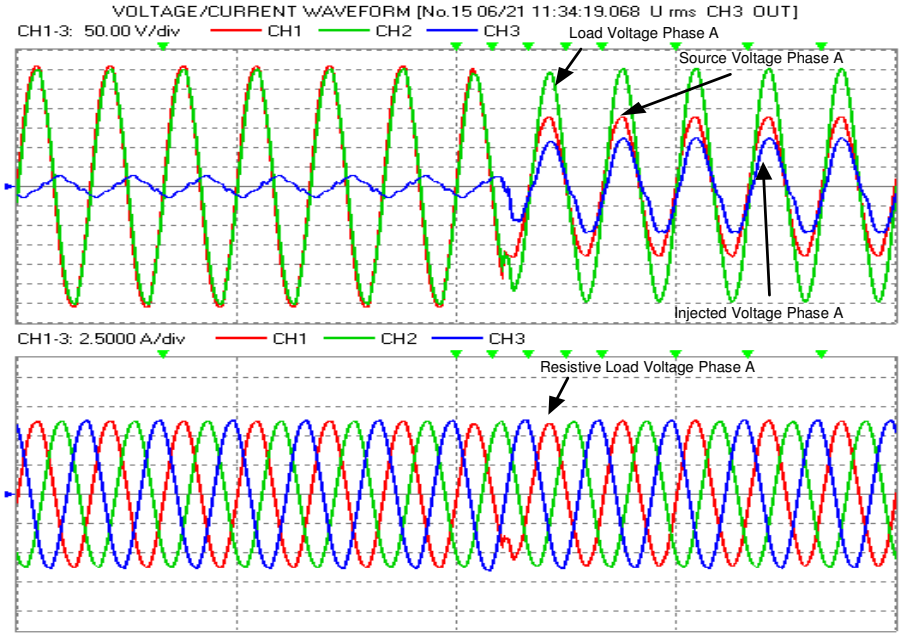

Figure 4.40. Source, injected, load voltage for phase A and currents, Case 3

4.3.4. Case 4: Three Phase, 40% Voltage Sag

The last case presents the 40% three phase voltage sag. Figure 4.41 is the rms trend of source and load voltage for phase A. Figure 4.42 shows the three phase source voltages and compensated load currents for a sag in the investigated interval.

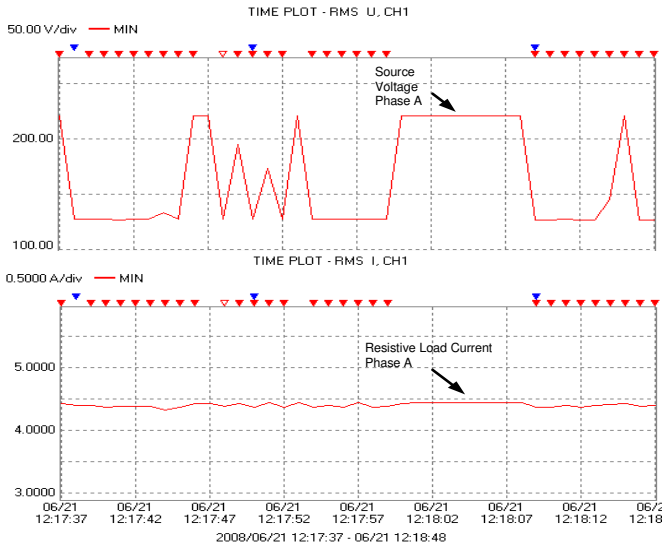

Figure 4.41. Rms values of source voltage and load voltage of phase A for Case 4

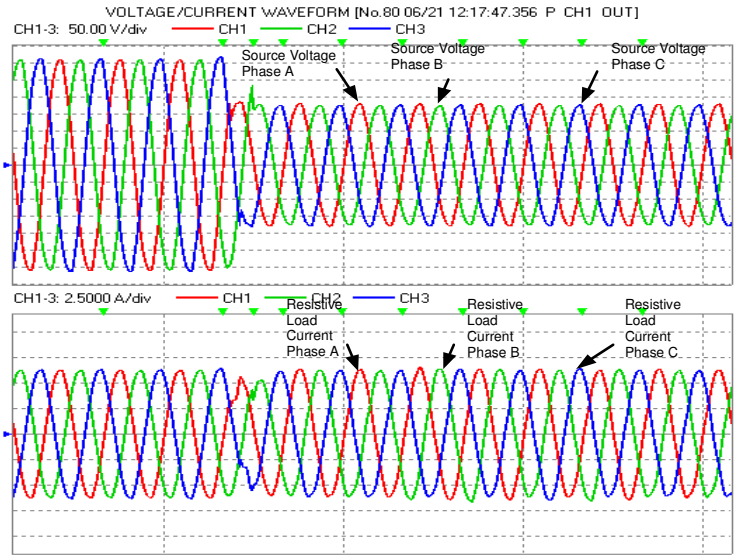

Figure 4.42. Source voltages and load currents for Case 4

5. IMPLEMENTATION OF DSP BASED STATIC TRANSFER SWITCH

The simulation model of STS is developed by the use of PSCAD/EMTDC program. Ideal parameters are used for all of the components initially. The parameters are updated after the experimental study as ideal parameters does not give adequate results that a real system can give. Following sections presents both software and hardware design of STS and results of the study.

5. 1. Design of Static Transfer Switch

This section covers the design of control algorithms and power circuit of STS. In the control of STS, two different sag detection approaches are used. The software and hardware design details are presented.

5.1.1. Controller Design for Static Transfer Switch

In the following sections, the DSP control algorithm flowcharts are given and investigated in detail. Two different approaches for sag detection are used in the algorithms one of which the traditional dq transform based method and proposed PLL based method. The PLL based method is depend on the nonlinear adaptive filter presented in (Karimi and Iravani, 2002).

5.1.1.1. Control Block Diagrams of Static Transfer Switch

The phase locked loop presented by (Karimi and Iravani, 2002) is used in the development of the STS control strategy. By this way, a new method is proposed for sag detection in STS. The block diagram of STS using PLL based sag detection is shown in Figure 5.1. The block diagram of STS using dq transformation based sag detection method is shown in Figure 5.2.

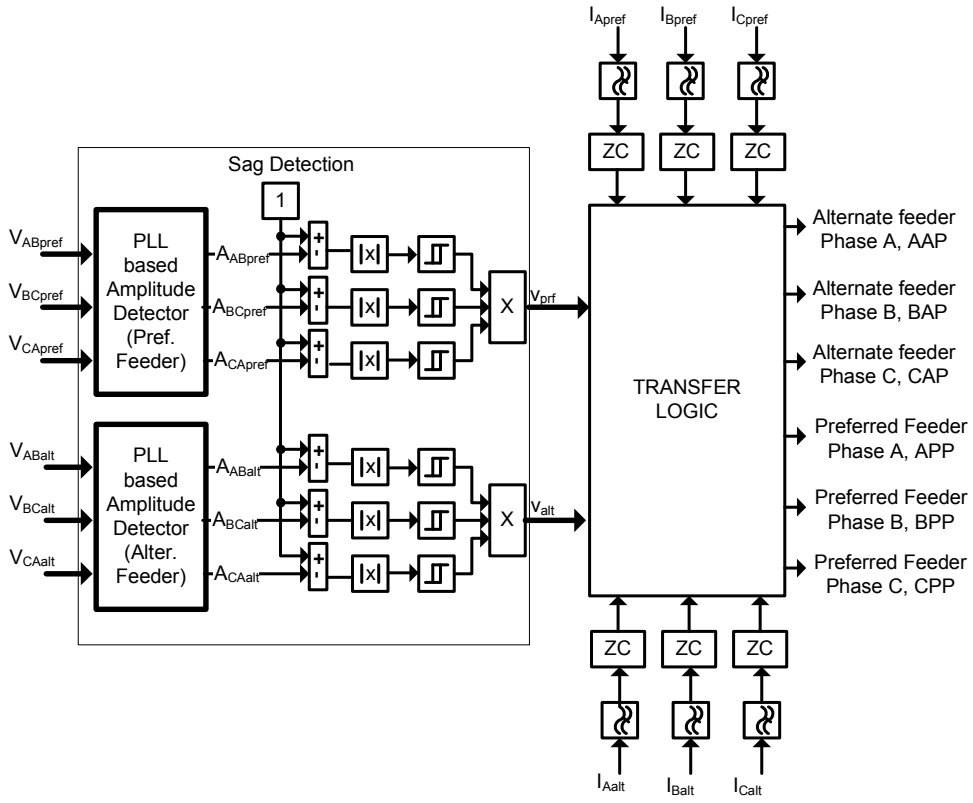

Figure 5.1. Control block diagram of STS based on PLL sag detection

The phase to phase voltage and line current measurements taken from preferred and alternate feeders are used in both transfer strategies. In the PLL based method, preferred feeder voltages V_{ABpref}, V_{BCpref}, V_{CApref}, alternate feeder voltages V_{ABalt}, V_{BCalt}, V_{CAalt} are subjected to two three phase PLL based amplitude detector functions. The amplitude detection property of PLL is shown in (Karimi and Iravani, 2002). Calculated preferred feeder amplitudes are A_{ABpref}, A_{BCpref}, A_{CApref} and alternate feeder amplitudes are A_{ABalt}, A_{BCalt}, A_{CAalt}, respectively. These values are subtracted from the reference rated voltage amplitude of 1 pu and the absolute values of the results of subtraction are sent to the hysteresis function of limit 0.1 pu. When the amplitude of a sag on any phase of preferred feeder gets a value greater than 0.1 pu, the sag detection signal of preferred feeder, "V_{prf}", becomes "0" which is "1" in normal operation. Similarly, when a sag is detected on any phase of alternate feeder, the sag detection signal of alternate feeder, "V_{alt}", is changed from "1" to "0". As a

summary, a sag on preferred feeder sets the "V_{prf}" signal to "0" and a sag on alternate feeder sets the "V_{alt}" signal to "0". In other words, "V_{prf}" of "0" means there is a sag on preferred feeder and "V_{alt}" of "0" means there is a sag on alternate feeder.

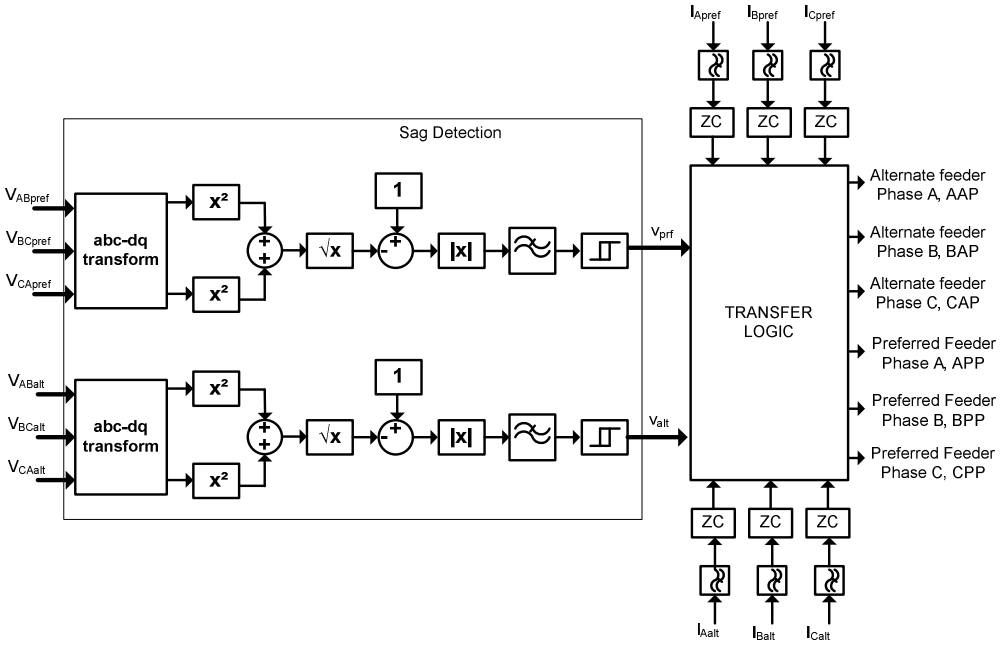

Figure 5.2. Control block diagram of STS based on dq transformation method

After the sag is detected on a feeder, the same transfer logic is applied in both control strategies. With this logic, the control signals to thyristor drivers of preferred feeder and alternate feeder are generated. In the transfer logic, the current measurements of preferred feeder and alternate feeder are processed. To commit the transfer operation, current measurements are first filtered and then zero crossings (ZC) of those signals are detected. ZC blocks in both Figures 5.1 and 5.2 are used to show that the zero crossing detection is made.

The signals going to the preferred feeder thyristor drivers, are named as "APP", "BPP" and "CPP", respectively. The signals going to the alternate feeder thyristor drivers, are named as "AAP", "BAP" and "CAP". These signals are sent to each of the anti-parallel thyristor pairs in both preferred and alternate feeder phases. As an instance, changing the value of "APP" to "1" means that the anti-parallel

thyristor pair of preferred feeder phase A is triggered. This lets a current to flow through phase A of preferred feeder to the load. Similarly, a value of "1" in "BPP" and "CPP" means that the thyristors in phases B and C of preferred feeder are triggered. The same is true for alternate feeder.

The transfer logic used to determine the states of "APP", "BPP" and "CPP" of preferred feeder and "AAP", "BAP" and "CAP" of alternate feeder is given below.

• If there is no sag or swell in preferred feeder phases, "APP", "BPP" and "CPP" saves their states of "1" and the load is supplied from preferred feeder.

• If a sag or swell is detected in preferred feeder and the alternate feeder is healthy, the load is transferred to the alternate feeder phase by phase at the zero crossings of preferred feeder phase currents.

• If the sag or swell in preferred feeder is cleaned, the load is transferred back to the preferred feeder. This time, the zero crossings of alternate feeder phase currents are waited to complete the transfer.

• If there are sag or swells in both feeders, it is continued to supply the load from preferred feeder.

5.1.1.2. DSP Software Flowcharts for Static Transfer Switch

The control flowcharts for both PLL based sag detection and dq transform based sag detection are given in this section. The voltages and currents of preferred and alternate feeders are read by the analog to digital converter of DSP controller. Those values read by the controller are listed below.

- Preferred feeder, line-to-line voltage of A-B, V_{ABpref},
- Preferred feeder, line-to-line voltage of B-C, V_{BCpref},
- Preferred feeder, line-to-line voltage of C-A, V_{CApref},
- Alternate feeder, line-to-line voltage of A-B, V_{ABalt},
- Alternate feeder, line-to-line voltage of B-C, V_{BCalt},
- Alternate feeder, line-to-line voltage of C-A, V_{CAalt},
- Preferred feeder, phase A current, I_{Apref},

- Preferred feeder, phase B current, I_{Bpref},
- Preferred feeder, phase C current, I_{Cpref},
- Alternate feeder, phase A current, I_{Aalt},
- Alternate feeder, phase B current, I_{Balt},
- Alternate feeder, phase C current, I_{Calt}

There are 56 programmable general purpose input-output pins on the F2812 DSP controller. 6 of them are used as output to sent the control signals to thyristor drivers. As it is mentioned before, these signals are "APP", "BPP" and "CPP" for preferred feeder, "AAP", "BAP" and "CAP" for alternate feeder. In Figure 5.3, the flowchart of main control algorithm using the PLL based sag detection is given. The flowchart of main control algorithm using the dq transformation based sag detection is given in Figure 5.6.

The CPU calls the main function with C_int0 interrupt. In this function, first the global variables are defined and initial values for those variables are assigned. Then software modules are initialized. Thereafter, the CPU timers are initialized to adjust the sampling time. Next, six of the general purpose input output pings are assigned to be outputs to control the thyristor drivers. Finally, ADC module of DSP controller is initialized. After the completion of these steps, DSP controller runs a background loop and waits for INT1 interrupt generated by CPU timer. The C implementation of STS controller is given in Appendix B, Listing B.2.

5.1.1.2.(1) Control Flowchart using PLL based Sag Detection

Within the INT1 interrupt service routine, V_{ABpref}, V_{BCpref}, V_{CApref}, V_{ABalt}, V_{BCalt}, V_{CAalt}, I_{Apref}, I_{Bpref}, I_{Cpref}, I_{Aalt}, I_{Balt}, I_{Calt} are read from ADC and converted into per unit equivalents. These values are then sent to PLL based amplitude detectors and the voltage amplitudes of preferred feeder A_{ABpref}, A_{BCpref}, A_{CApref} and the voltage amplitudes of alternate feeder A_{ABalt}, A_{BCalt}, A_{CAalt} are calculated.

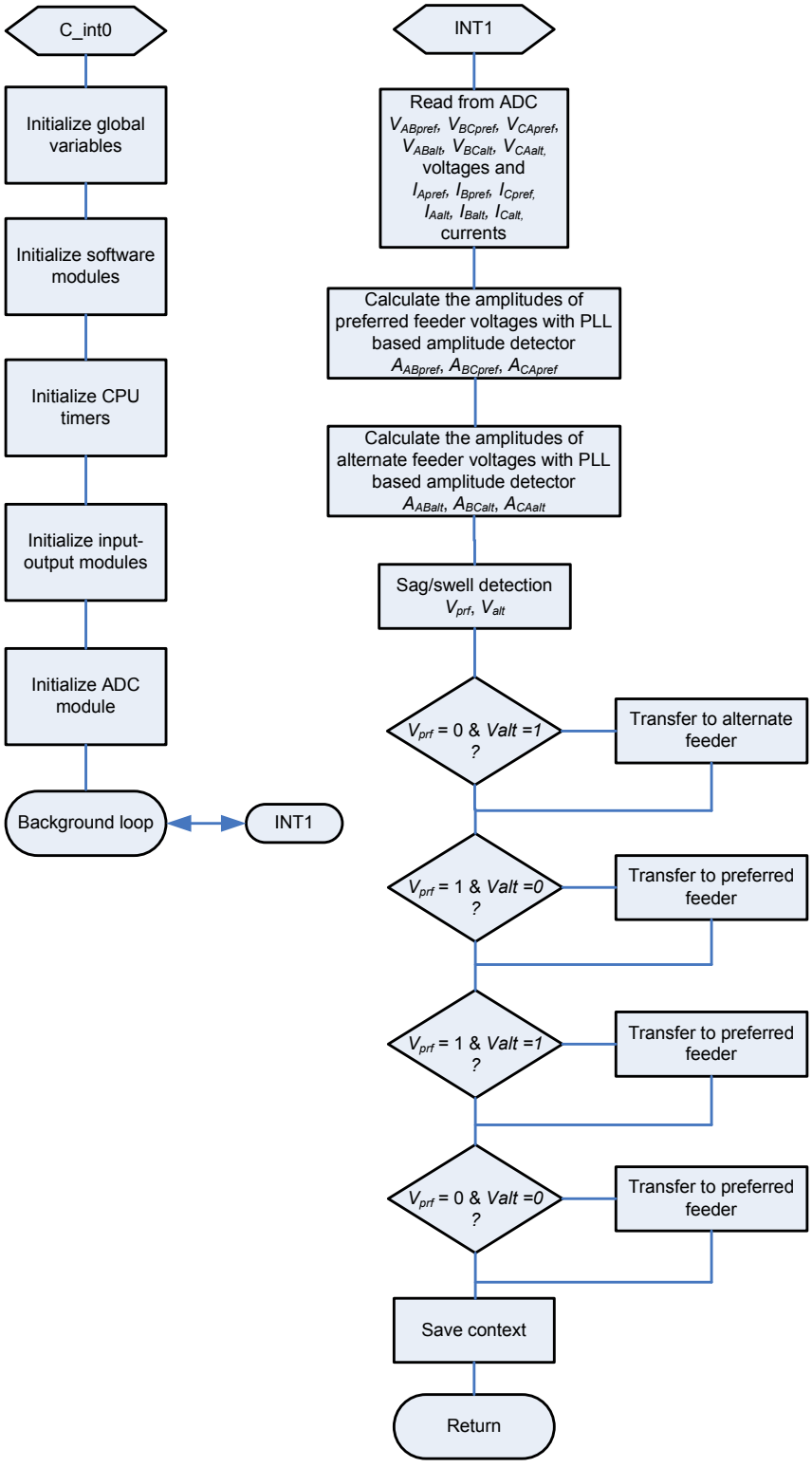

Figure 5.3. The control algorithm flowchart of STS using PLL based sag detection

The flowchart of PLL based amplitude detector is given in Figure 5.4. Two PLL based amplitude detectors are used one for preferred feeder and one for alternate feeder. The flowchart is same for both detectors except the variable names. Figure 5.4 shows the one for preferred feeder.

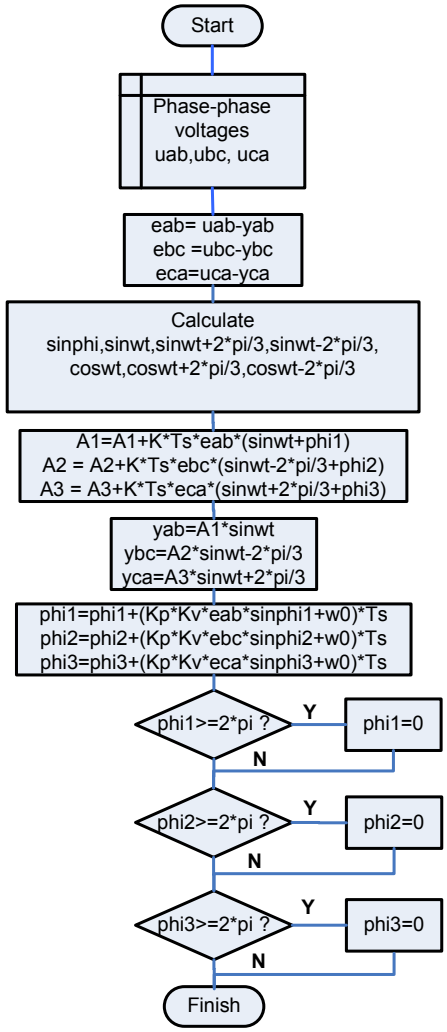

Figure 5.4. Flowchart of PLL based amplitude detector

Phase-to-phase feeder voltages are sent to the functions as parameters. “eab”, “ebc”, “eca” are the errors that are the difference between the actual feeder voltages “uab”, “ubc”, “uca” and the PLL outputs “yab”, “ybc”, “yca”. The aim of the PLL is to approximate these errors to “0”. A “0” value means that the PLL outputs are in the

same phase and magnitude with feeder voltages. “A1”, “A2”, “A3” values are the voltage amplitudes calculated by phase locked loop. These values correspond to A_{ABpref}, A_{BCpref}, A_{CApref} for preferred feeder and A_{ABalt}, A_{BCalt}, A_{CAalt} for alternate feeder in Figure 5.3. After the calculation of the amplitudes of both feeders, these values are subjected to a sag-swell detection function to find the values of “V_{prf}” and “V_{alt}”. The flowchart of this function is given in Figure 5.5.

As it can be seen from Figure 5.5, the amplitude values calculated by PLL based amplitude detectors are subtracted from the reference value of 1 pu and the result is sent to a hysteresis function. The flowchart of the hysteresis function is also given on the right hand side of Figure 5.5. The working principle of the hysteresis function is; the output is set when the input exceeds the 0.1, the output is reset when the input falls below 0.04. With this method, the effects of oscillations in input values are suppressed. By the results of hysteresis comparisons, “flgpA” for phase A, “flgpB” for phase B, “flgpC” for phase C of preferred feeder are adjusted. “flgaA”, “flgaB” and “flgaC” are adjusted for alternate feeder with a similar fashion. Lastly, in the sag swell detection function, “V_{prf}” and “V_{alt}” are calculated by using the “flg” variables.

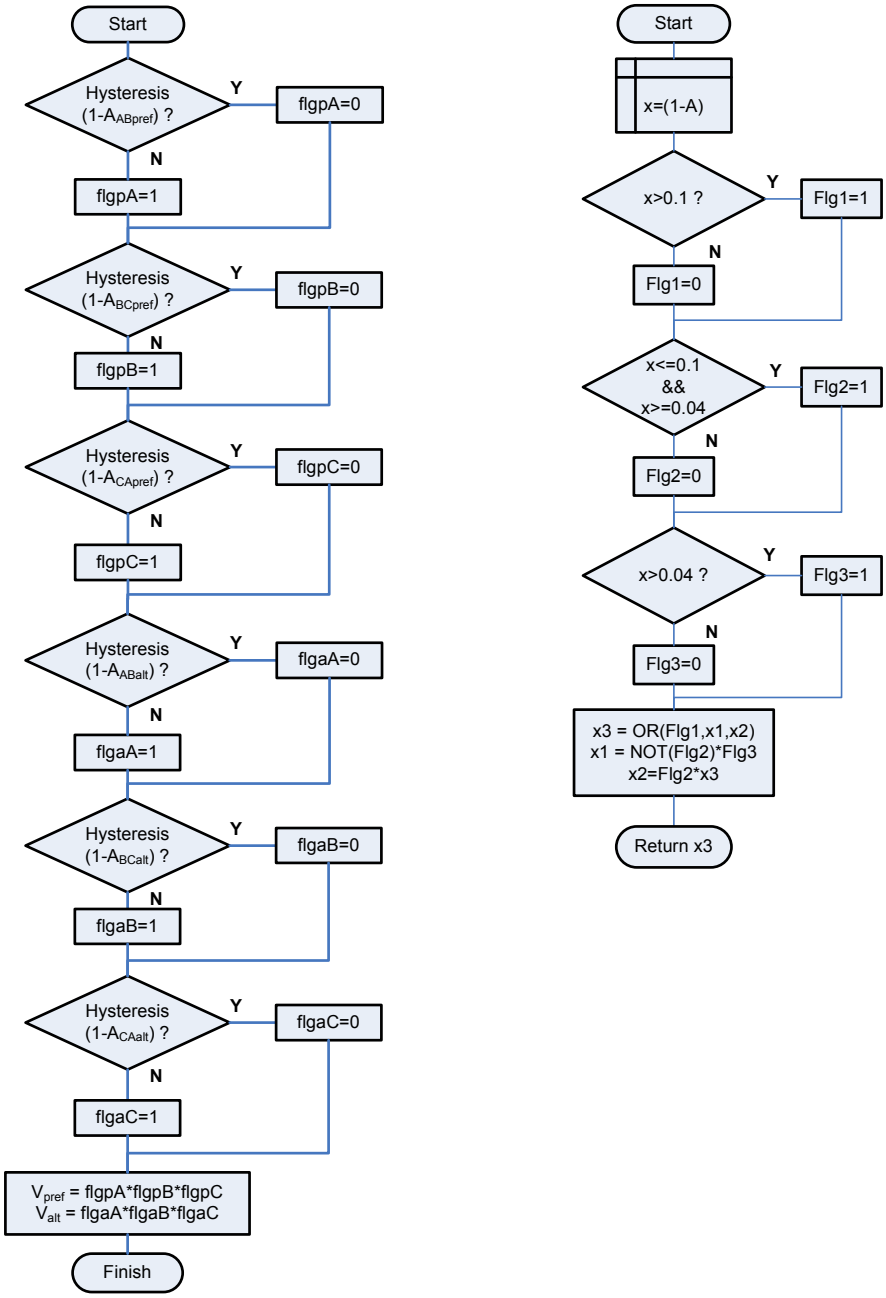

Figure 5.5. Flowchart for sag-swell detection function and hysteresis function

5.1.1.2.(2). Control Flowchart using d-q based Detection

Within the INT1 interrupt service routine, V_{ABpref}, V_{BCpref}, V_{CApref}, V_{ABalt}, V_{BCalt}, V_{CAalt}, I_{Apref}, I_{Bpref}, I_{Cpref}, I_{Aalt}, I_{Balt}, I_{Calt} are read from ADC and converted into

per unit equivalents. The control flowchart with dq sag detection is shown in Figure 5.6. These values are then sent to dq transformation based sag detection function. The flowchart of this function is given in Figure 5.7.

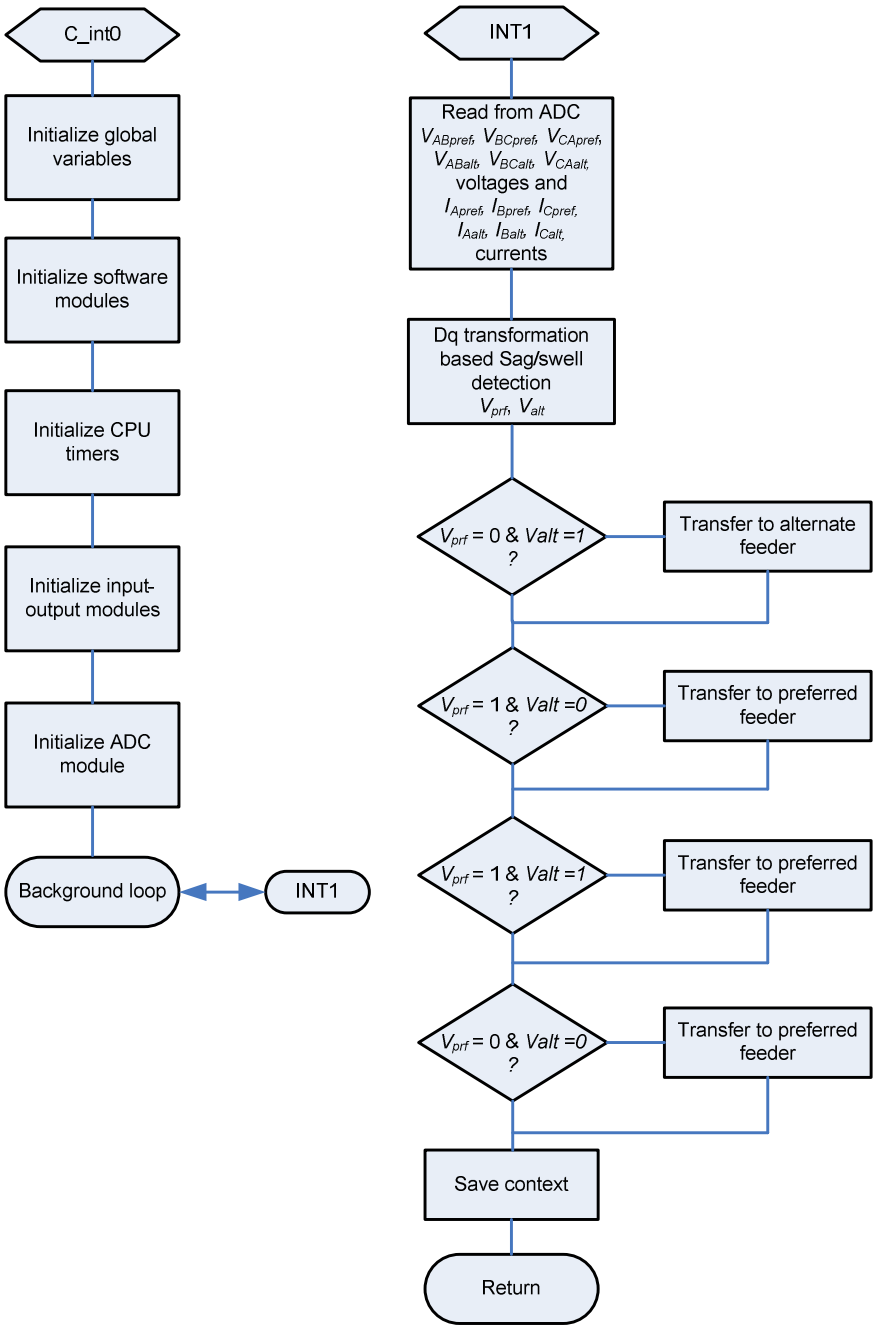

Figure 5.6. The control algorithm flowchart of STS using dq transformation

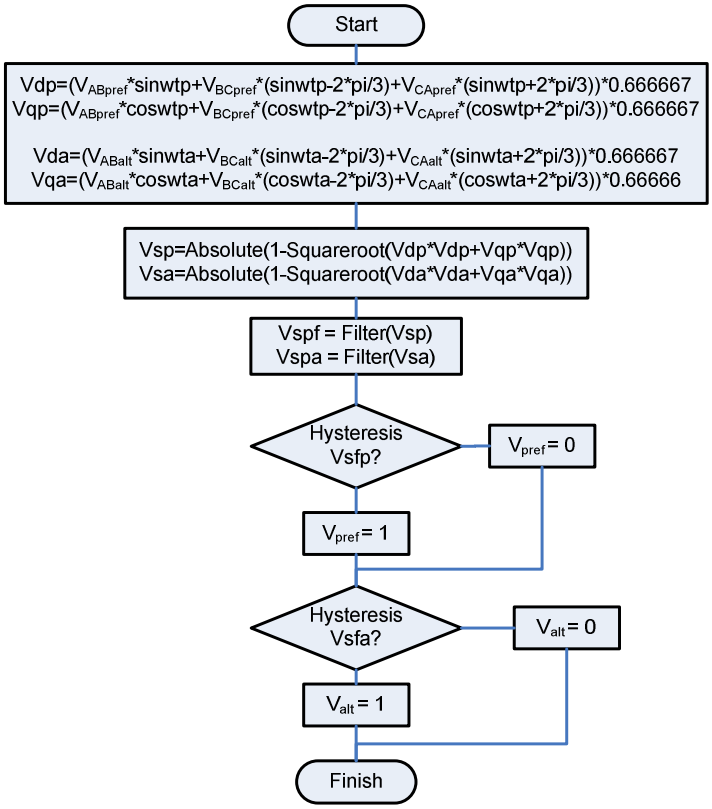

Figure 5.7. Flowchart of dq transformation based sag-swell detection function

In the function, the phase-to-phase voltages are transformed into dq reference frame. Equation (4.5) and (4.6) is used for this purpose. By the use of hysteresis function, "V_{pref}" and "V_{alt}" values are determined.

The control algorithms for both PLL based sag detection and dq transformation based sag detection is the same after the detection functions. Henceforth, they will be examined together.

After the sag detection in preferred and alternate feeders, the transfer logic explained earlier is applied. STS transfers the loads to preferred feeder or alternate feeder when needed.

• "V_{prf}" = 0 and "V_{alt}" = 1

This situation appears when a sag or swell occurs on preferred feeder. The load is transferred to alternate feeder as it is healthy.

• "V_{prf}" = 1 and "V_{alt}" = 0

This time, a sag or swell occurred on alternate feeder and preferred feeder is healthy. If the load was supplied from alternate feeder before this situation happened, it will be transferred to preferred feeder. No action will occur if it is supplied from preferred feeder anyway.

• "V_{prf}" = 1 and "V_{alt}" = 1

This shows that both feeders are healthy. For this reason, if the alternate feeder was supplying the load before this situation occurred, the load will be transferred back to preferred feeder. No transfer is made if the preferred feeder was supplying the load anyway.

• "V_{prf}" = 0 and "V_{alt}" = 0

If there are problems on both feeders and alternate feeder was supplying the load before the situation occurred, the load is transferred to preferred feeder. No transfer is made if the preferred feeder was supplying the load anyway.

The flowchart given on the left hand side of Figure 5.8 shows the algorithm used to transfer the load alternate feeder while the flowchart on the right hand side of Figure 5.8 shows the algorithm used to transfer load back to preferred feeder.

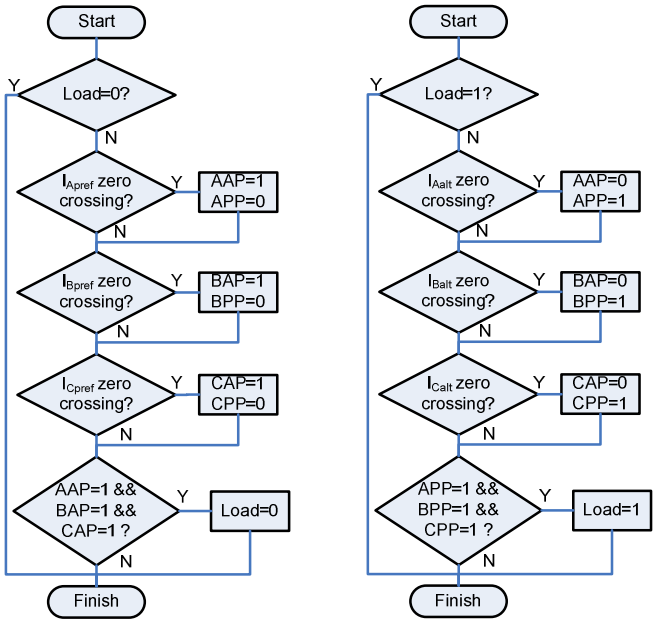

Figure 5.8. Load transfer function flowcharts

In the load transfer function that is used to transfer the load from preferred feeder to alternate feeder, it is seen that the variable "Load" is used to determine which feeder is supplying the load. A value of "0" in the "Load" variable means that the alternate feeder is supplying the load. It is seen that if the alternate feeder is already supplying the load, the function will return with no transfer actions. But a value of "1" in the "Load" variable means that the preferred feeder is supplying the load and the load must be transferred to alternate feeder. While transferring the load from preferred feeder to alternate feeder, current zero crossings of preferred feeder are waited. On each zero crossing of each phase current of preferred feeder, that phase is transferred to alternate feeder. This continues until all phases are transferred to alternate feeder. The function determines the complete transfer from the states of variables "AAP", "BAP" and "CAP". If the values of these variables are both "1", the transfer is completed.

The same way is followed for the transfer from alternate feeder to preferred feeder. This time, current zero crossings of alternate feeder phases are waited to make the transfer. Variables "APP", "BPP" and "CPP" are used instead.

5.1.2. Hardware Design of DSP based Static Transfer Switch

The experimental setup of STS is composed of six back to back connected thyristor pairs used as static AC switches. The experimental setup for the STS is presented in Figure 5.9.

There are two voltage sources named preferred and alternate. The load is supplied from the preferred source in normal operation. When a disturbance occurs, the load is transferred to alternate source. After the disturbance, the load is transferred to the preferred source again. R and L elements in the Figure 5.9 are the sum of line and source impedances of two sources. There are 6 current and 6 voltage transducers in the experimental setup. The outputs of these transducers are applied to the signal conditioning board to adjust the voltage levels to the ADC inputs of the controller. F2812 ezDSP kit is used as the DSP controller. The output buffer and isolation circuit isolates and drives the thyristor modules

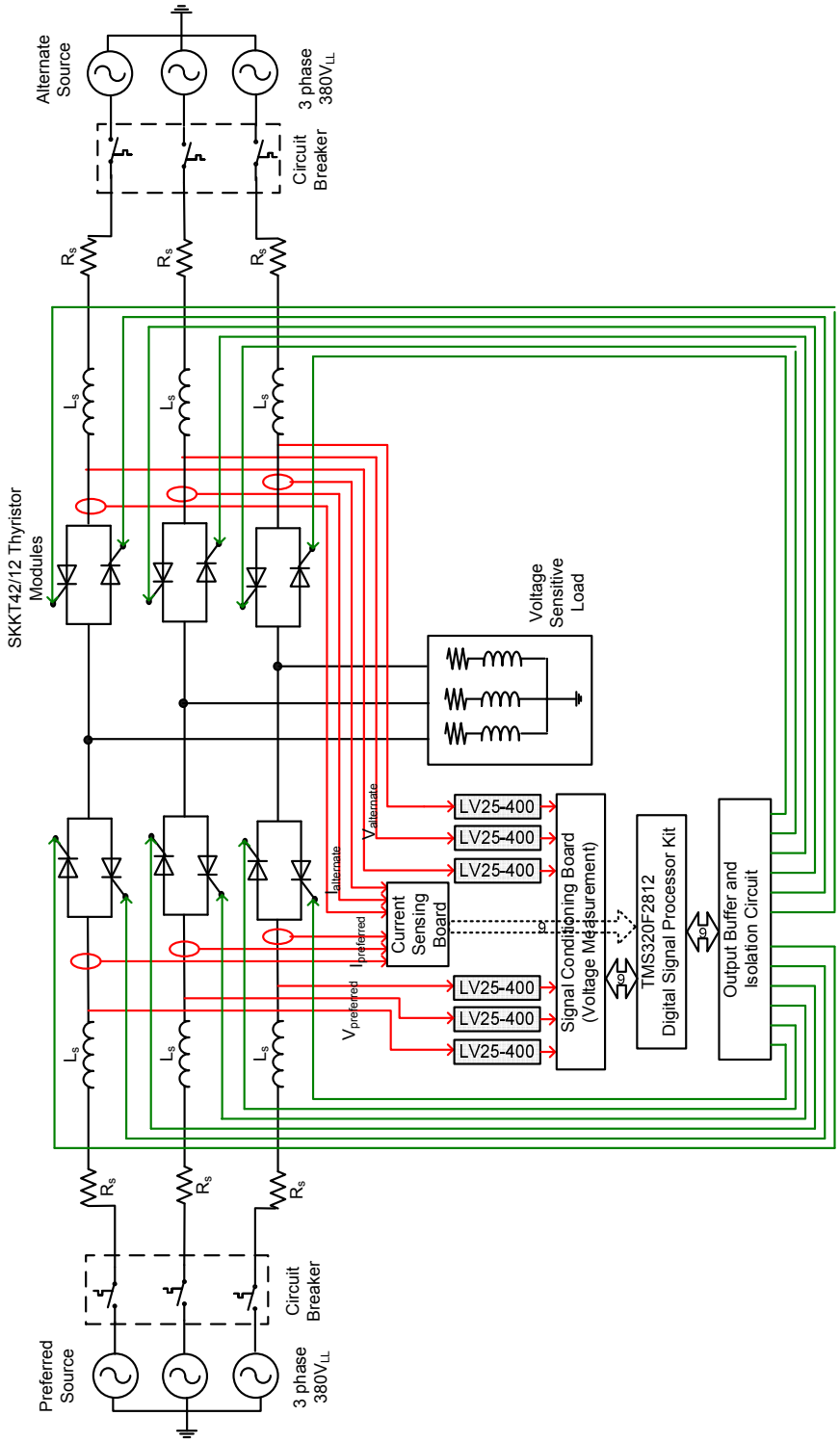

Figure 5.9. Experimental block diagram of STS

F2812 DSP controller, LEM LV25-400 voltage transducers are the same as in DVR case. So no further detailed descriptions given for these equipments. To measure the preferred and alternate feeder currents, LA25-P hall effect current sensors are used. To drive the gates of SKKT42/12 thyristor modules, a circuit formed by using MOC3023 integrated circuits is used. Each of the elements used in STS will be explained in detail later in following sections.

The parameters of proposed STS are given in Table 5.1.

Table 5.1. Parameters of proposed STS

Description	Value / profile
Preferred source and feeder	0-380V variable source, 18.75 kVA
Alternate source and feeder	0-380V variable source, 18.75 kVA
Thyristors	SKKT 42/12 SCRs with RC snubbers
Load impedances / per phase	Resistive, Z1: 144 Ω, Z2: 144 Ω, Z3: 48 Ω
Sample time	25 μs

5.1.2.1. Voltage Transducers and Signal Conditioning Board

The preferred and alternate source voltages are measured from the experimental setup by using the signal conditioning board and voltage transducer cards shown in Figure 5.10. The three LEM LV25-400 voltage transducer cards on the left of the figure are used to measure the preferred feeder voltages while the other three LEM LV25-400 voltage transducer cards on the right of the figure are used to measure the alternate feeder voltages. The line-to-line voltages of the feeders are used in the computations. The circuit diagram of signal conditioning board is the same as in DVR case for any of the phases. Only difference is that there are six channels instead of three.

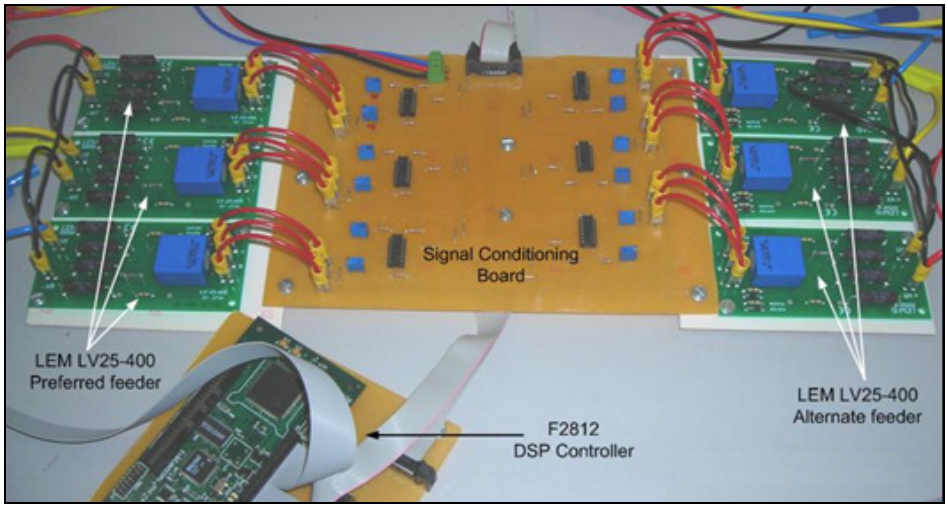

Figure 5.10. Voltage transducer cards and signal conditioning card

5.1.2.2. Current Sensing Board

To measure the currents of both preferred feeders and alternate feeders, a card is designed. The picture of current measurement card is given in Figure 5.11. It has the same electronic components as is the signal conditioning board of voltages. The main difference is that the transducers are LEM LA 25P hall effect current sensors.

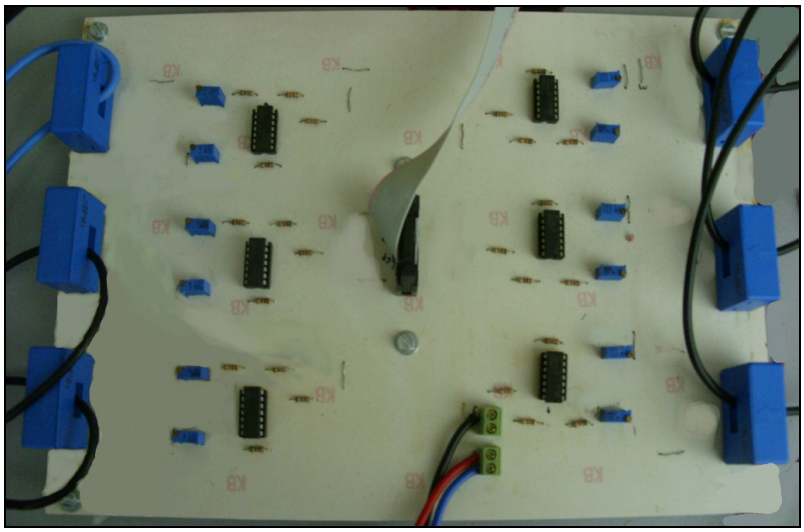

Figure 5.11. Current measurement card of STS

As the transducers are based on current transformers, the measurement signals are isolated from the line voltages as it is expected.

5.1.2.3. Output Buffer and Isolation Card

To drive the thyristor modules safely, an interface card is needed. By using 74LS241 octal buffer integrated circuits (IC) and MOC3023 non-zero crossing triac driver ICs, a circuit is designed to overcome the safety and buffering needs.

Each digital output of DSP can supply 2 mA current to the load that it is connected. The MOC3023 triac driver IC consumes 10 mA to fully turn on the thyristors. A buffer is needed to interface the MOC3023 with F2812 DSP controller. 74LS241 octal buffer ICs are used as an interface. The input currents to these ICs are approximately 0.1 mA and can supply 20 mA output current for each of its outputs. In other words, DSP triggers the 74LS241 and 74LS241 triggers the MOC3023. Later, MOC3023 drives the thyristor modules. A simplified block diagram of the output buffer and isolation card for one thyristor is given in Figure 5.12. The output buffer and isolation circuit as well as thyristor switches are shown in Figure 5.13.

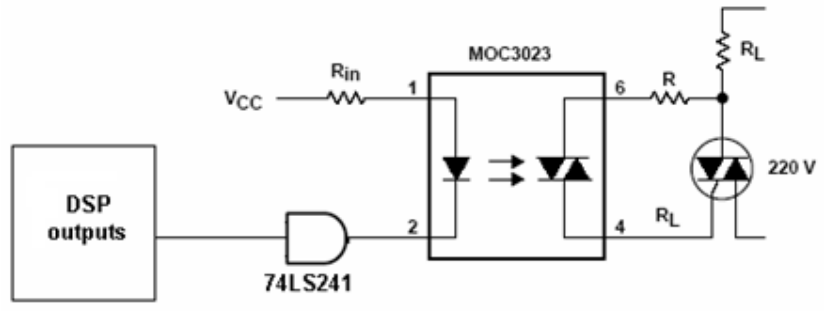

Figure 5.12. Simplified block diagram of output buffer and isolation card

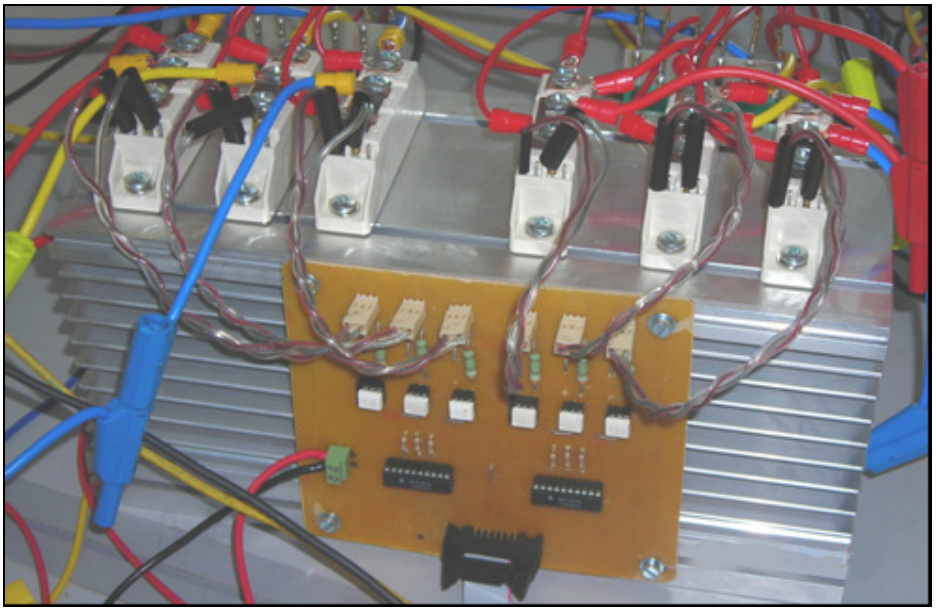

Figure 5.13. Output buffer and isolation card of STS and thyristor modules

5.1.2.4. Thyristor Modules

Semikron SKKT 42/12 thyristor modules are used as static transfer switches. Each module has two thyristors in it. A thyristor module and its equivalent circuit diagram are given in Figure 5.14.

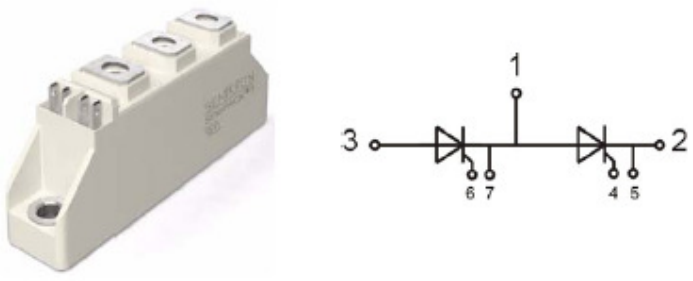

Figure 5.14. Semikron SKKT 42/12 thyristor module and circuit diagram

Each thyristor in the module is rated at 44A. It withstands 1000A short circuit current for 10 ms. It has a blocking voltage of 1200V. It typically needs 100 mA current to turn on.

5.2. Simulation of Static Transfer Switch

The simulation model of STS is shown in Figure 5.15. The model consists of sag/swell generators to generate voltage sags and swells on both preferred and alternate feeders. Six pairs of back-to-back connected thyristor switches form the STS. Two voltage sensitive loads are supplied via STS.

Preferred and alternate source voltages and currents are measured to control the transfer. All the measurements are applied to the controller given in right bottom of the Figure 5.15. This controller is responsible of sag, swell and interrupt detection. When a sag or swell detected on the preferred source, the supply of the loads are transferred to the alternate source if it is available to feed the loads in the zero crossings of the load currents.

Several case studies are formed to test the performance of the STS. This section presents the results taken from simulation runs.

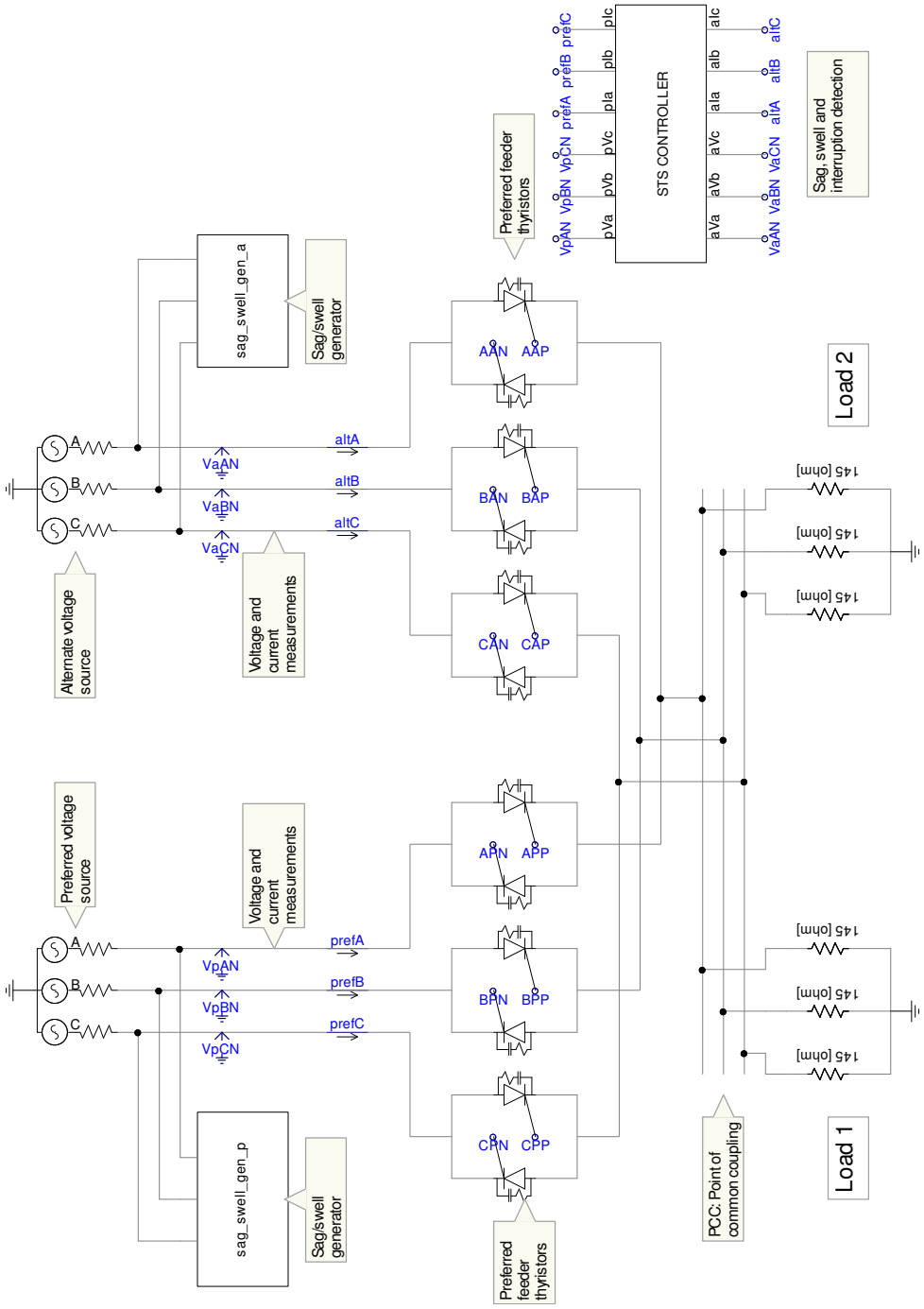

Figure 5.15. Simulation model of STS

5.2.1. Simulation Results of Static Transfer Switch

The simulation results taken are discussed in this section. Several case studies are realized. The results taken from control algorithm using PLL based sag detection and dq transform based sag detection are given. These case studies include three phase 40% voltage sag on preferred feeder for both PLL based and dq transformation based methods, three phase 20% sag and single phase 15% sag on preferred feeder for dq transformation based method and lastly, three phase 30% voltage sag on both feeders.

5.2.1.1. Case 1: Three Phase 40% Sag, PLL Detection

The three phase voltage sag starts at 0.25 seconds and ends at 0.4 seconds. The rms values of preferred feeder voltage and load voltage are given in Figure 5.16. The preferred feeder voltage is given on the upper part of the figure and the load bus voltage is the lower part of the figure. It is seen that three phase sag are occurred on the preferred feeder, the load is then transferred to alternate feeder and load is not affected from the sag.

The currents for the case are shown in Figure 5.17. The upper part shows the current of preferred feeder and lower part shows the current of load bus. It is seen that before the sag, the load is supplied from the preferred feeder. After the sag occurred, the load is transferred to the alternate feeder.

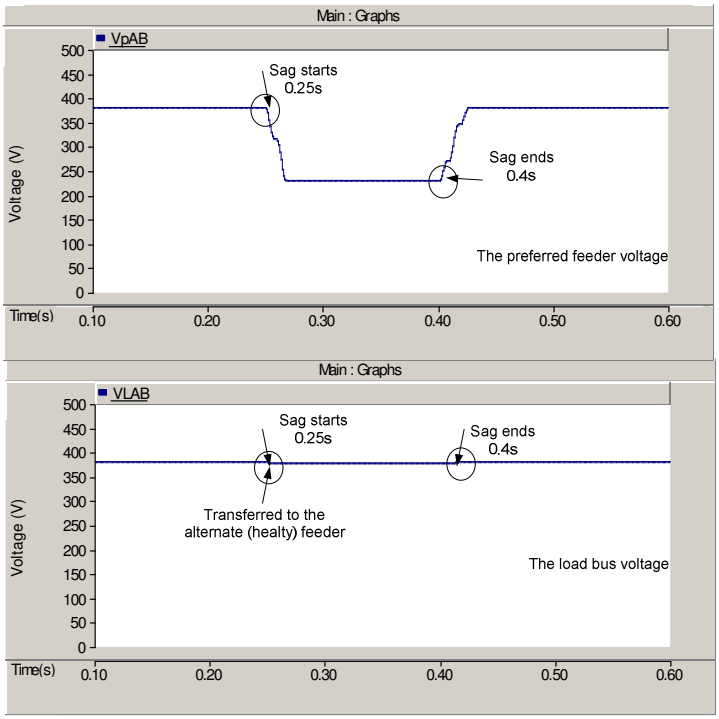

Figure 5.16. Rms voltages for preferred feeder and load bus for Case 1

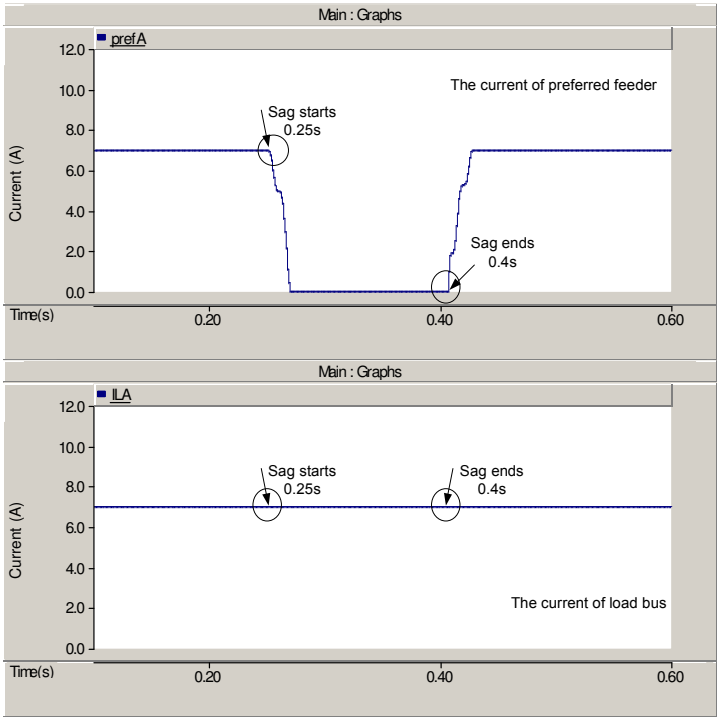

Figure 5.17. Rms current trends for preferred feeder and load bus for Case 1

Figures 5.18 and 5.19 below show the waveforms for the transfer process of preferred to alternate feeder and back. The waveform of load voltage remains unchanged and in phase with the alternate feeder voltage.

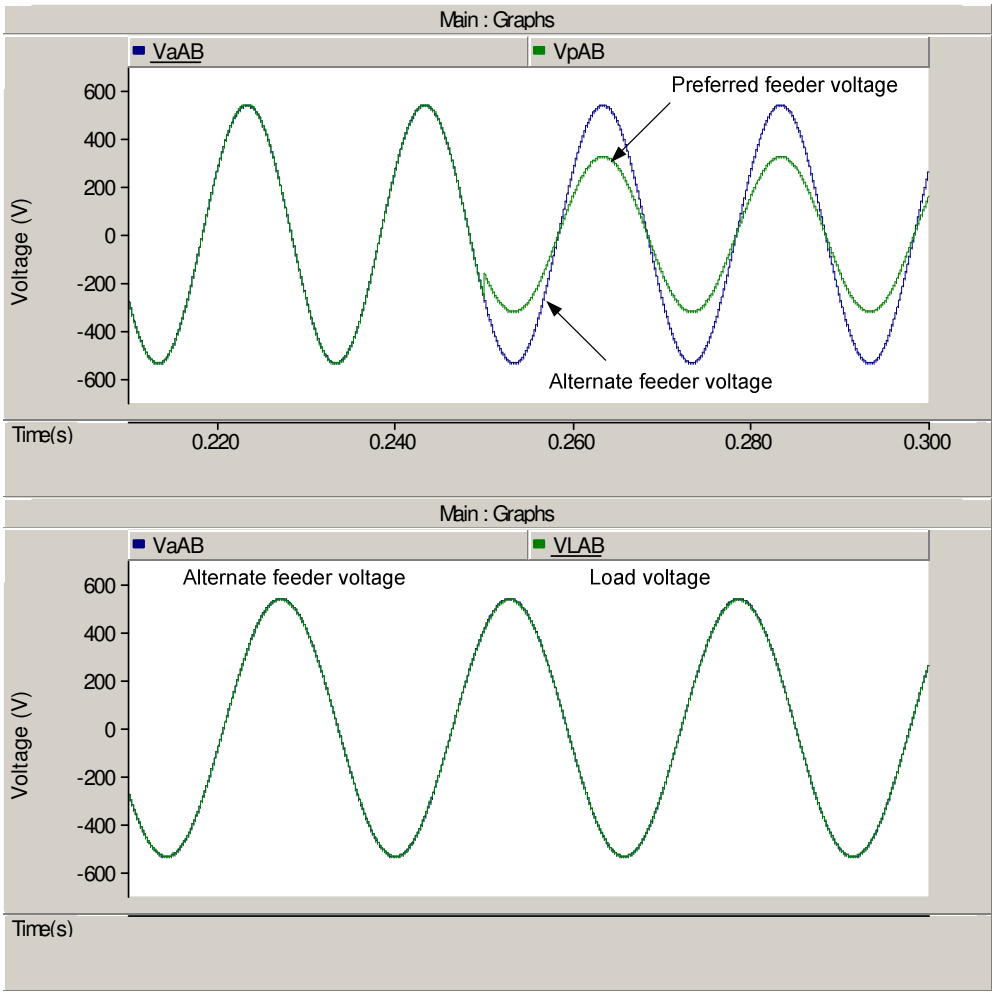

Figure 5.18. Waveforms for preferred to alternate feeder transfer for Case 1

If Figure 5.18 is investigated, it is seen that the load is transferred to the alternate feeder very fast when the sag is detected on the zero crossing of preferred feeder current. But in Figure 5.19, it is seen that the current transferred back to preferred feeder after a period of voltage on the zero crossing of alternate feeder. However, the return is not a problem anyway.

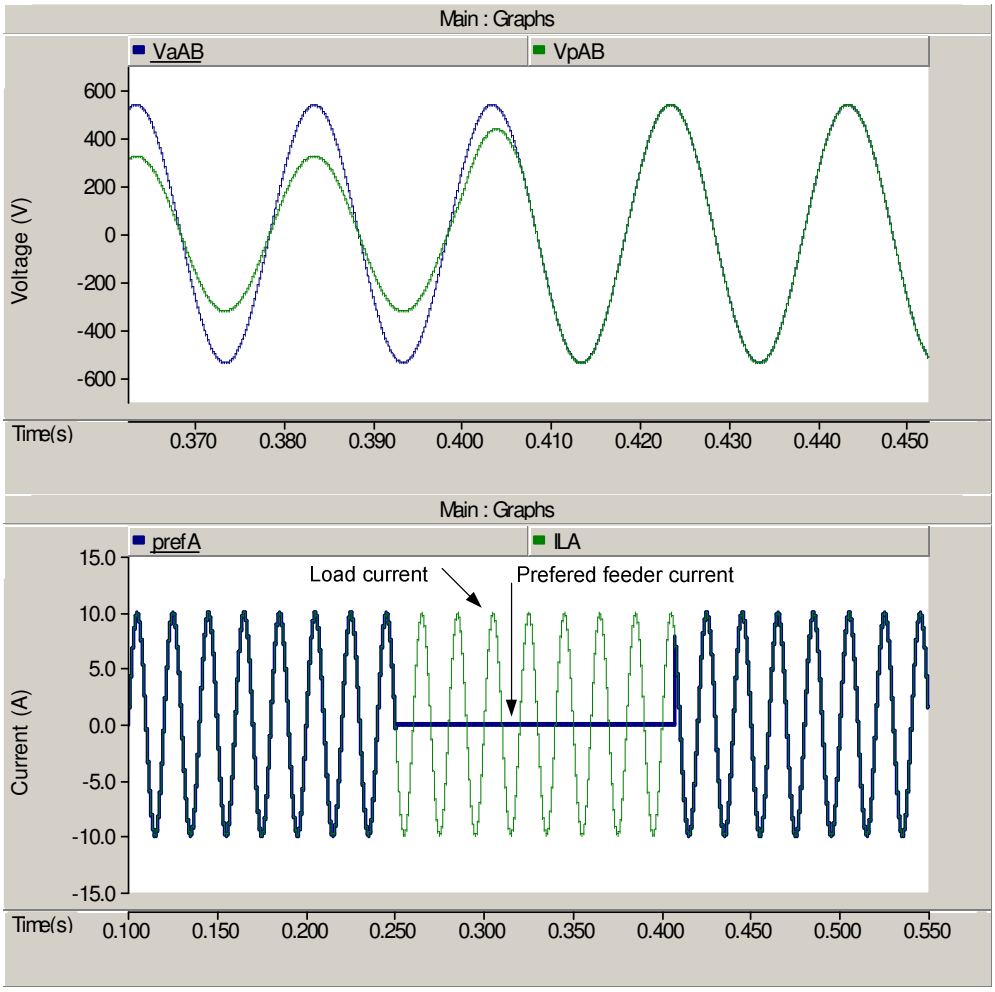

Figure 5.19. Waveforms for alternate to preferred feeder for Case 1

5.2.1.2. Case 2: Three Phase 40% Sag, dq Detection

Three phase fault occurs between (0.2-0.26 seconds) and (0.32-0.42 seconds). The rms values of preferred and load voltages are shown in Figure 5.20. The preferred feeder voltage is given on the upper part of the figure and the load bus voltage is the lower part of the figure. It is seen that three phase sags are occurred on the preferred feeder twice, the load is then transferred to alternate feeder and load is not affected from any of the sags.

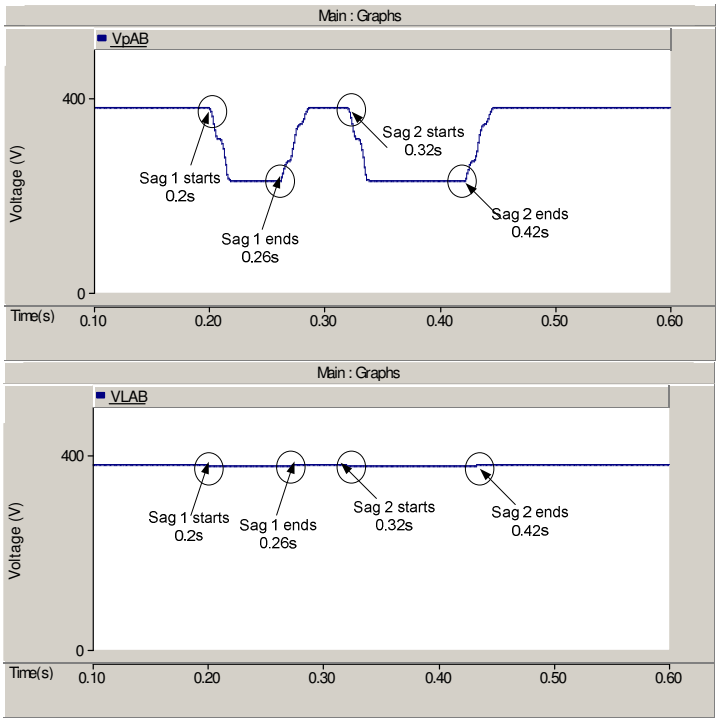

Figure 5.20. Rms voltages for preferred feeder and load bus for Case 2

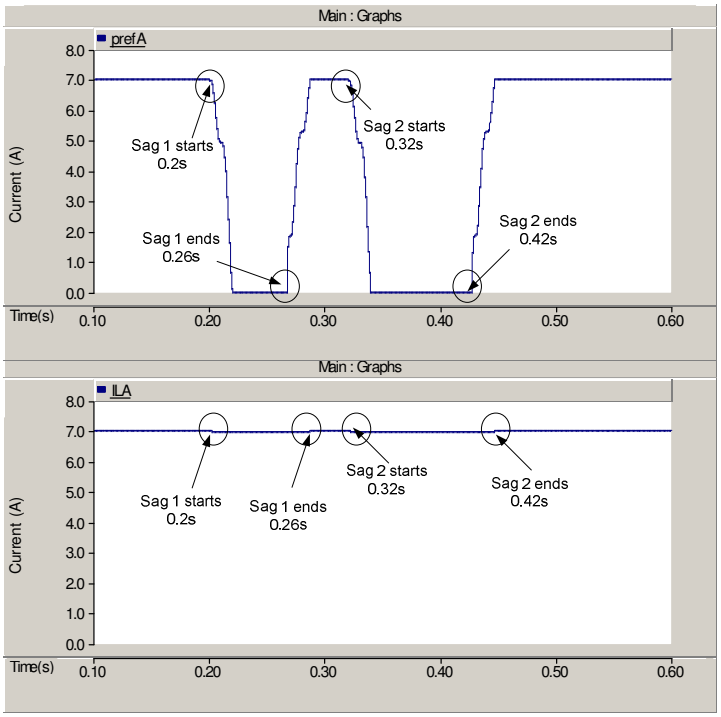

Figure 5.21. Rms current trends for preferred feeder and load bus for Case 2

Figure 5.21 shows that the load current is not affected from the sags occurred on the preferred feeder. Figures 5.22 and 5.23 below the waveforms for the transfer process of preferred to alternate feeder and back. The waveform of load voltage remains unchanged and in phase with the alternate feeder voltage. It seen from Figure 5.22 that the load is transferred to the alternate feeder after the sag is detected.

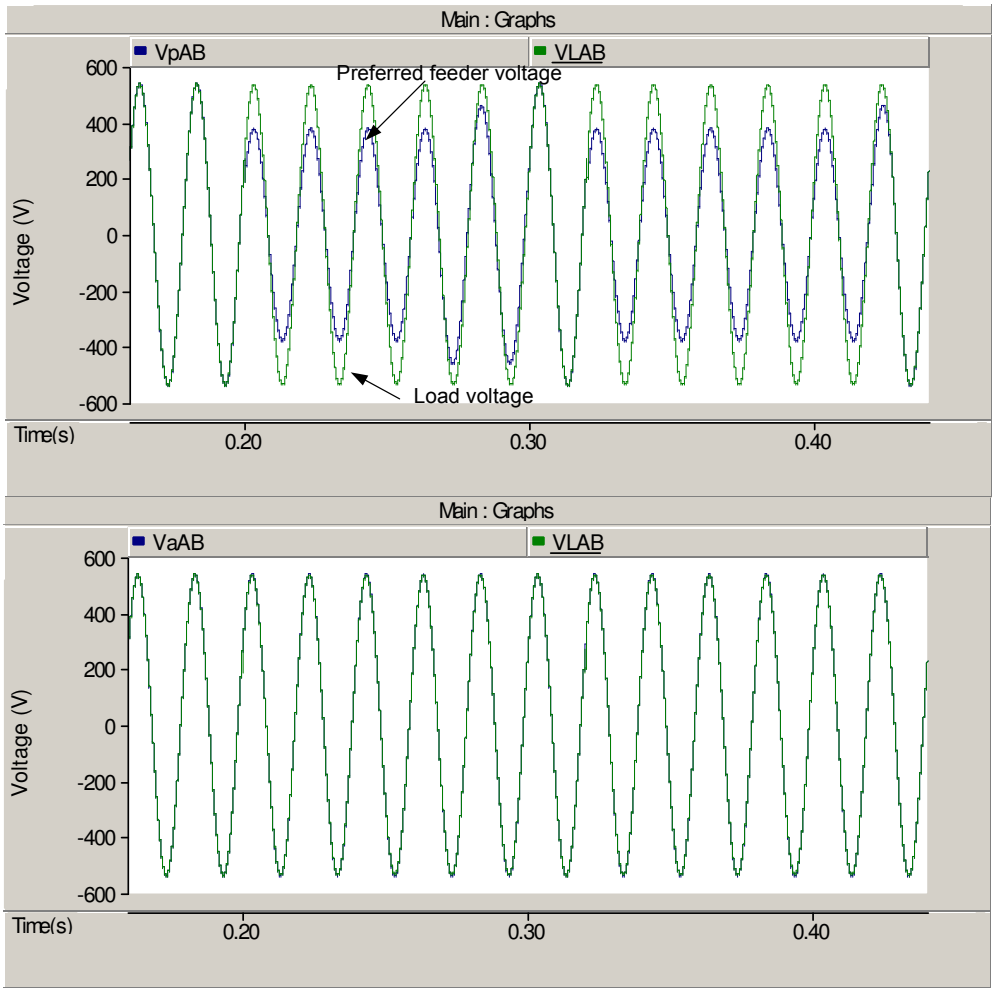

Figure 5.22. Waveforms for preferred to alternate feeder transfer for Case 2

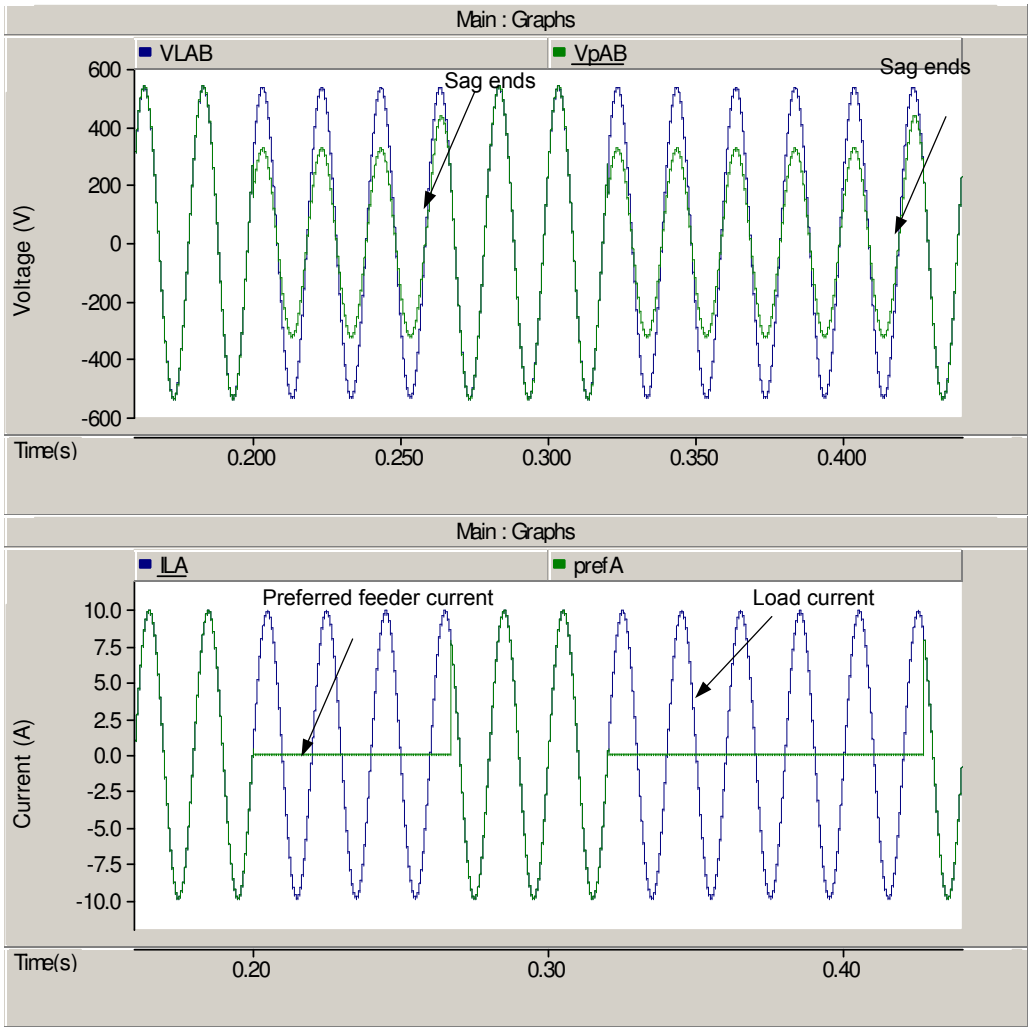

Figure 5.23. Waveforms for alternate to preferred feeder transfer for Case 2

5.2.1.3. Case 3: Three Phase 20% Sag, dq Detection

Single phase fault occurs between (0.2-0.26 seconds). Figure 5.24 shows the rms values of preferred and load voltages. The preferred feeder voltage is given on the upper part of the figure and the load bus voltage is the lower part of the figure. The load is then transferred to the alternate feeder and load is not affected from any of the sags. In Figure 5.25, rms trend for currents are given.

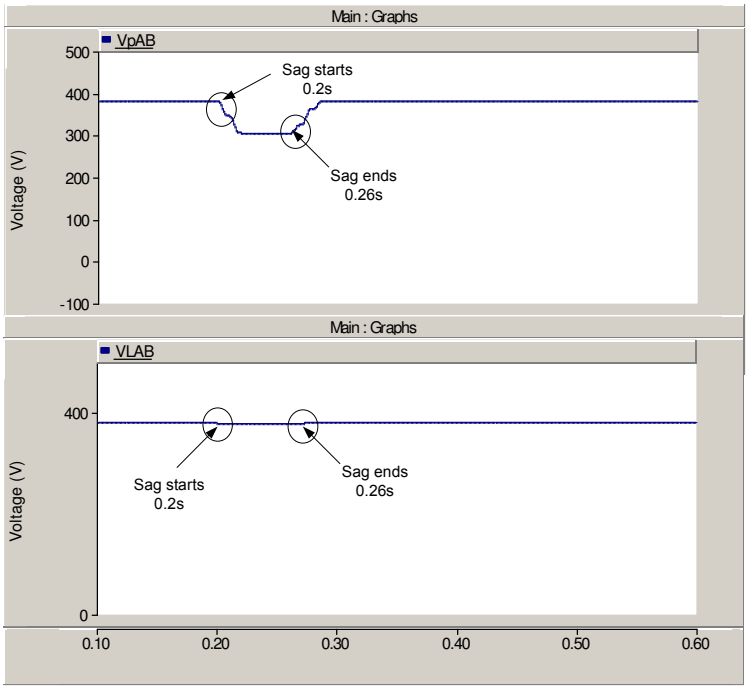

Figure 5.24. Rms voltages for preferred feeder and load bus for Case 3

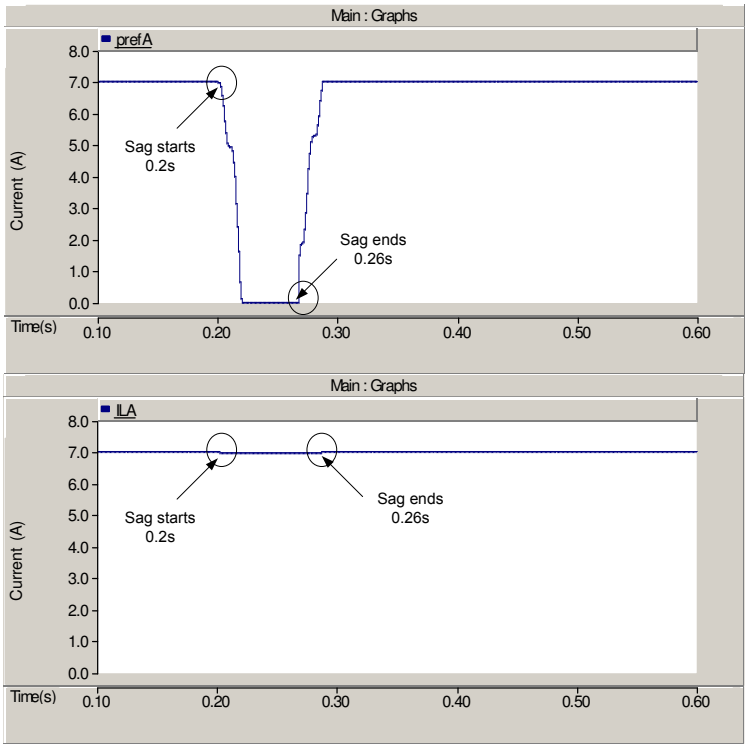

Figure 5.25. Rms current trends for preferred feeder and load bus for Case 3

Figures 5.26 and 5.27 below show the waveforms for the transfer process of preferred to alternate feeder and back. The waveform of load voltage remains unchanged and in phase with the alternate feeder voltage.

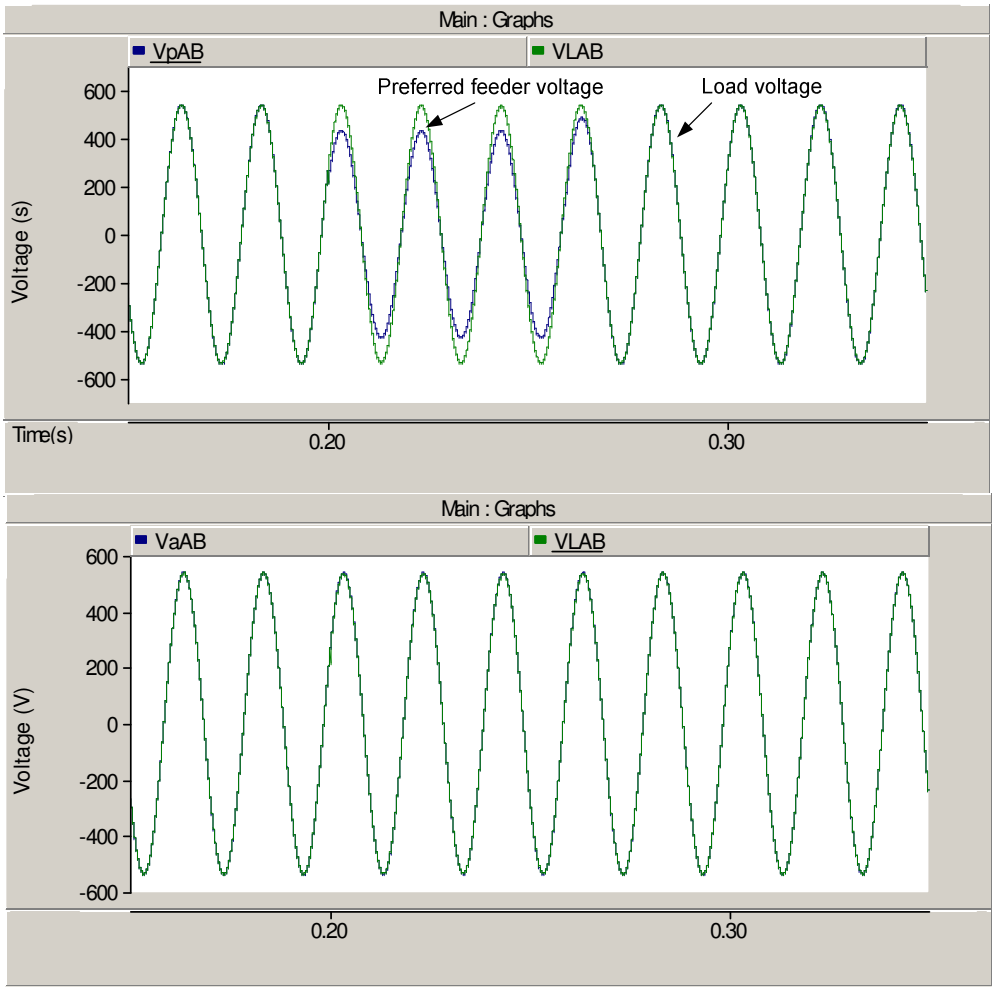

Figure 5.26. Waveforms for preferred to alternate feeder transfer for Case 3

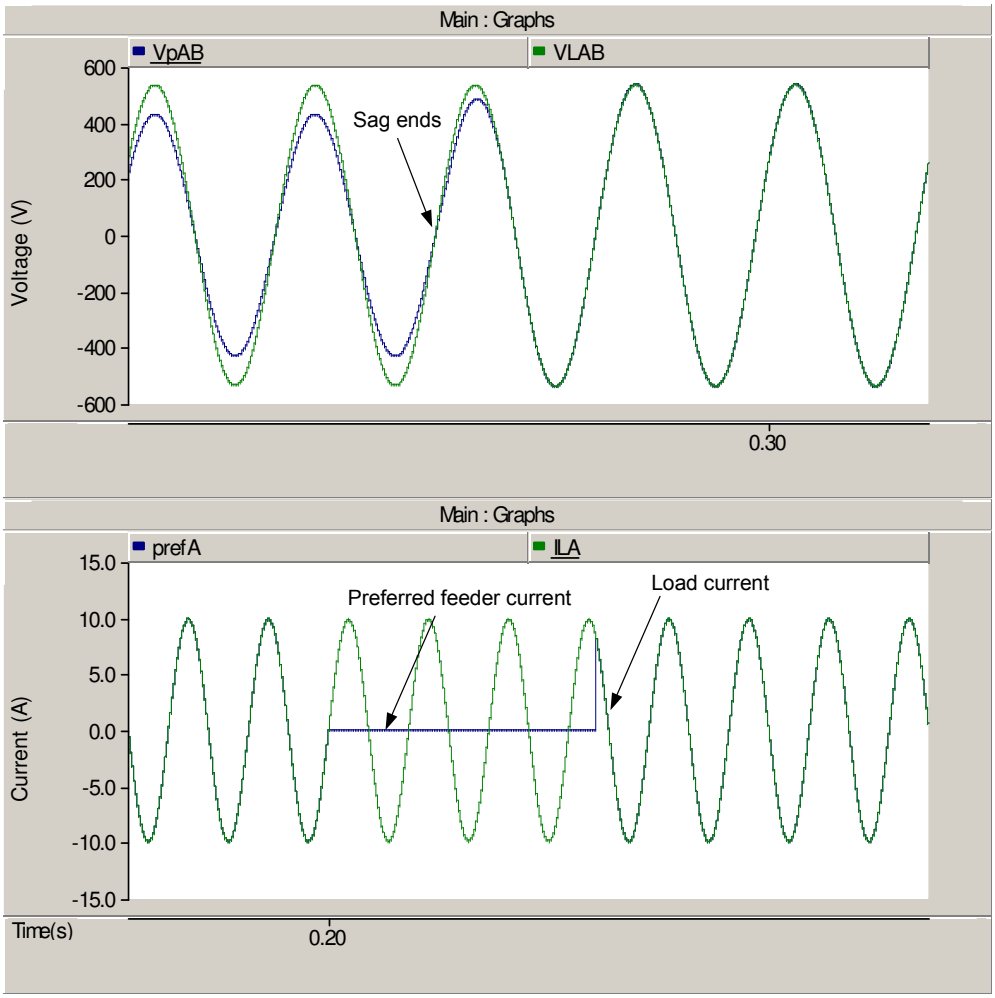

Figure 5.27. Waveforms for alternate to preferred feeder transfer for Case 3

5.2.1.4. Case 4: Single Phase 15% Sag, dq Detection

The main disadvantage of dq transformation based sag detection is that if there is a single phase sag on the line, it may not be detected by the method. Because the method uses the average of three phases to calculate the sag depth. So a single phase sag with small depth will not be able to produce a sag detection signal. The voltage trends for a single phase 15% sag on preferred feeder are presented in Figure 5.28. As it can be seen from the figure, a sag started and continued. However, the

sag detection algorithm is unable to detect the sag when the sag level is 10% (0.1 pu). So, the load is affected from the voltage sag. No transfer is made.

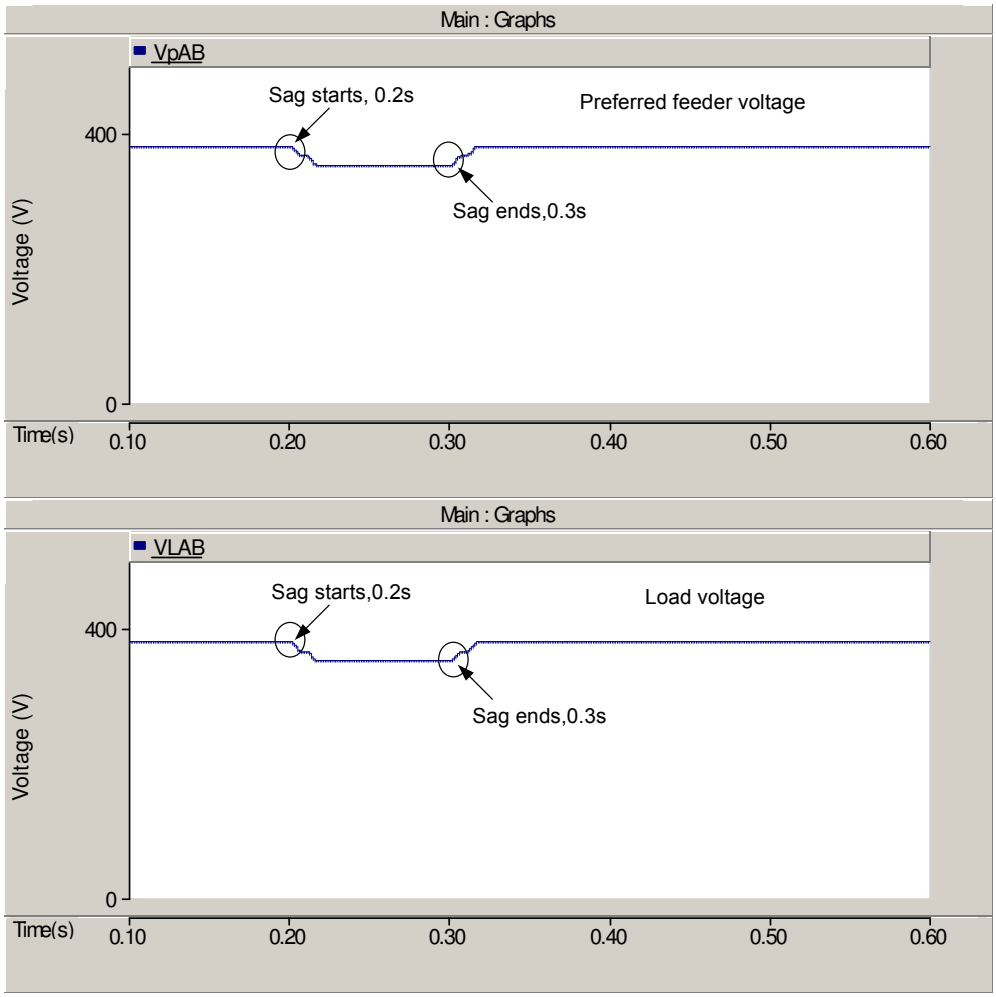

Figure 5.28. Rms voltage trend for single phase 15% sag for Case 4

Figure 5.29 is given to show the no transfer event is triggered on a single phase 15% sag. As it can be seen, the load faces the voltage sag.

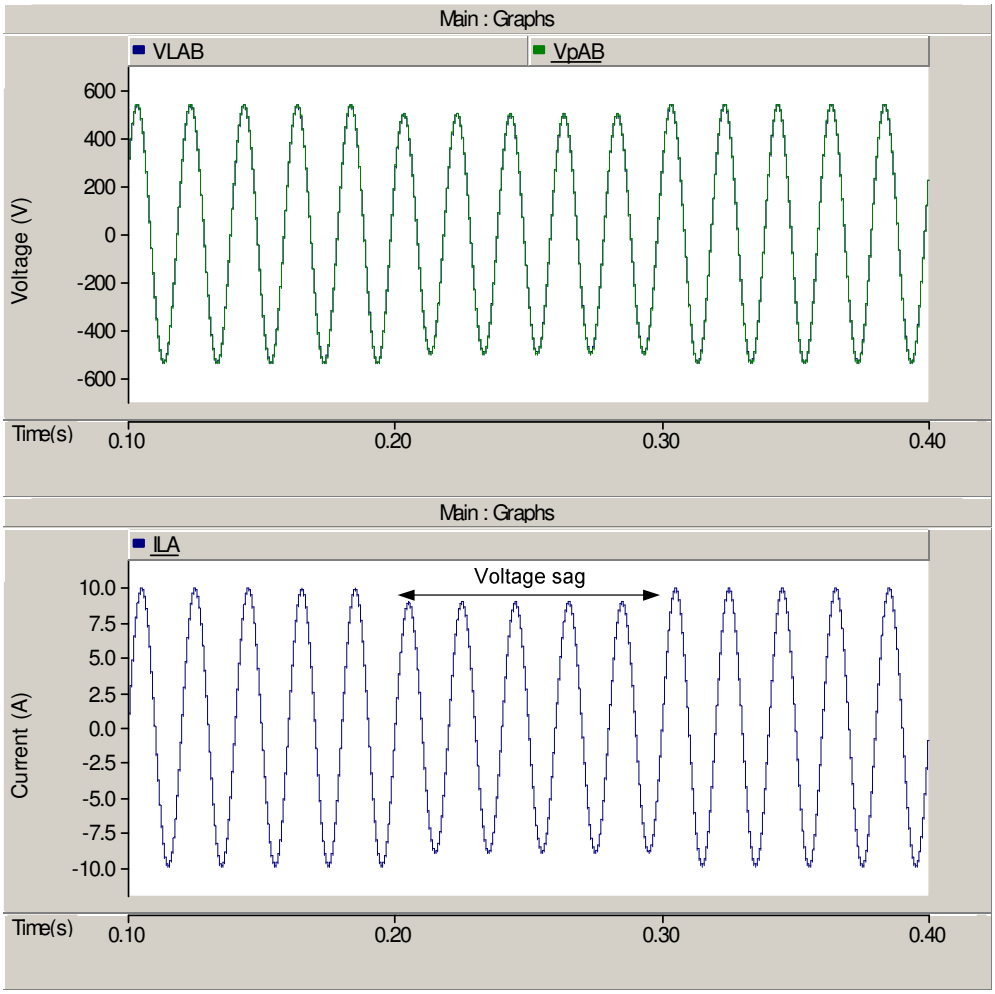

Figure 5.29. Waveform for single phase 15% sag with dq based method

5.2.1.5. Case 5: Three Phase 30% Sag on Both Feeders

In this case, there are 30% sags on both preferred and alternate feeders. Figure 5.30 is used to show the voltage trends for this case.

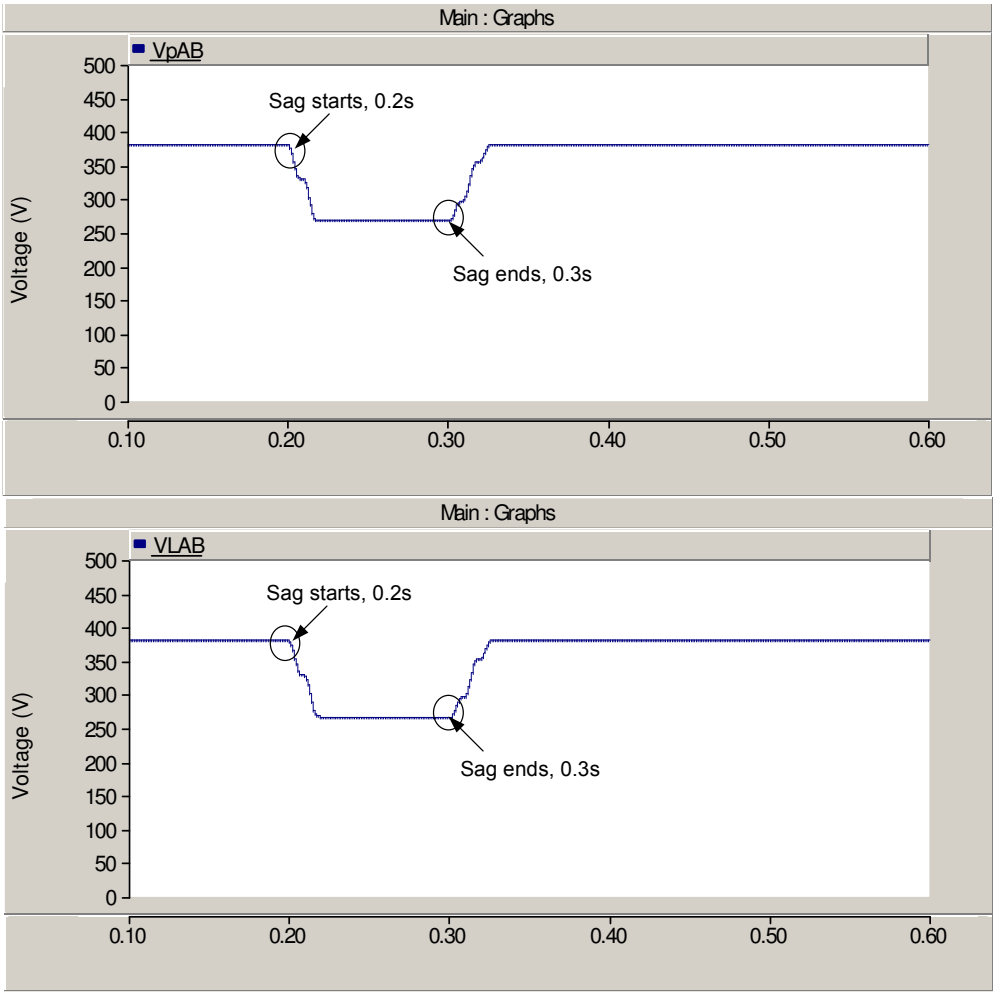

Figure 5.30. Rms voltage trends for preferred feeder and load bus for Case 5

The same magnitude of sags is applied to preferred and alternate feeders. So, the "V_{alt}" and "V_{pref}" signals are "0" at the same time. Recalling from the transfer logic, the load should not be transferred to alternate feeder in this case. Figure 5.31 shows that no transfer occurred in this case. The load is continued to supplied from the preferred feeder although there is a sag on the line.

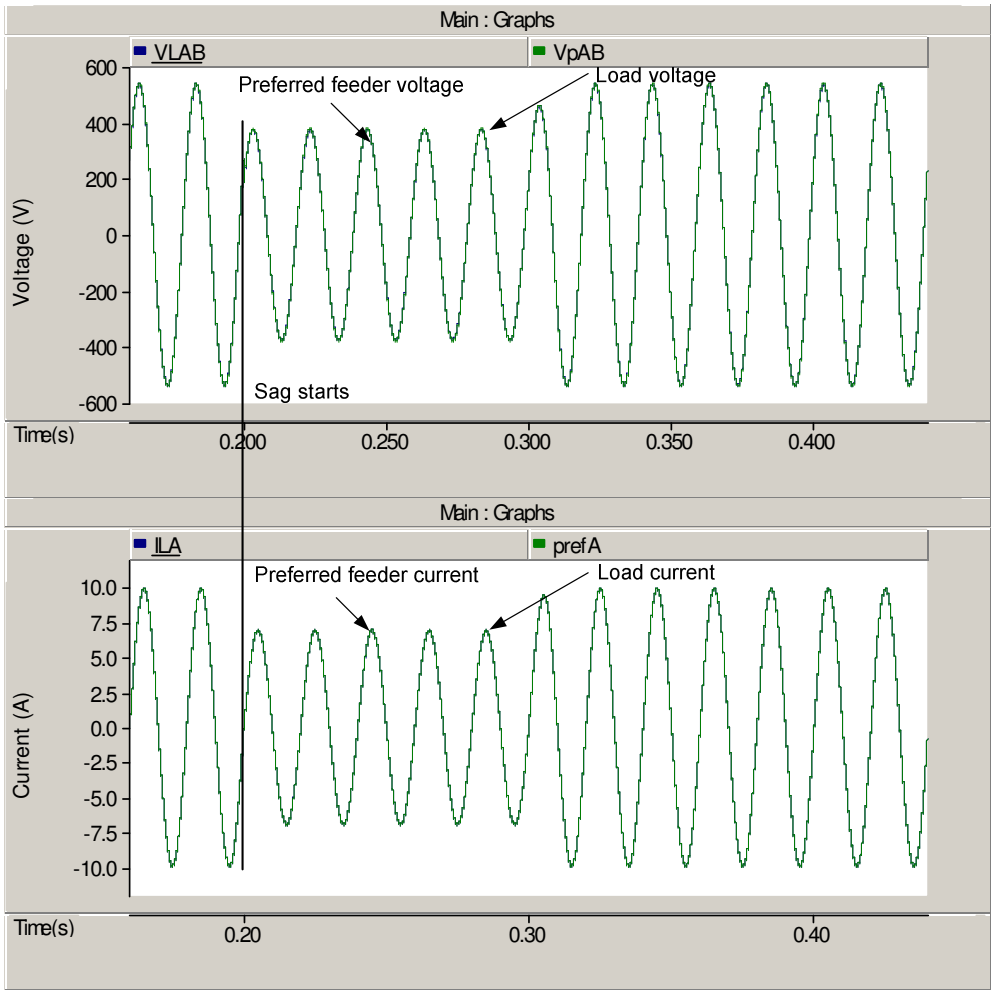

Figure 5.31. Waveforms for three phase 30% sags on both feeders for Case 5

5.3. Experimental Results of Static Transfer Switch

The experimental results taken are discussed in this section. Several case studies are realized. The results taken from control algorithm using PLL based sag detection and dq transform based sag detection are given. PLL based method needs some improvements so far.

These case studies include three phase 40% voltage sag on preferred feeder for both PLL based and dq transformation based methods. Three phase 20% sag and single phase 15% sag on preferred feeder for dq transformation based method.

Lastly, three phase 30% voltage sag on both feeders. The experimental results are taken from the project "Modeling and Implementation of Custom Power Park" which is supported by Scientific and Technological Research Council of Turkey with project number of 106E188. HIOKI 3196 Power Quality Anaylzer is used to record the current and voltage waveforms in the case studies.

5.3.1. Case 1: Three Phase 40% Sag, PLL Detection

The rms values of preferred and load voltages are given in Figure 5.22. The preferred feeder voltage is given on the upper part of the figure and the load bus voltage is the lower part of the figure. It is seen that three phase sags are occurred twice on the preferred feeder, the load is then transferred to alternate feeder and load is not affected from any of the sags.

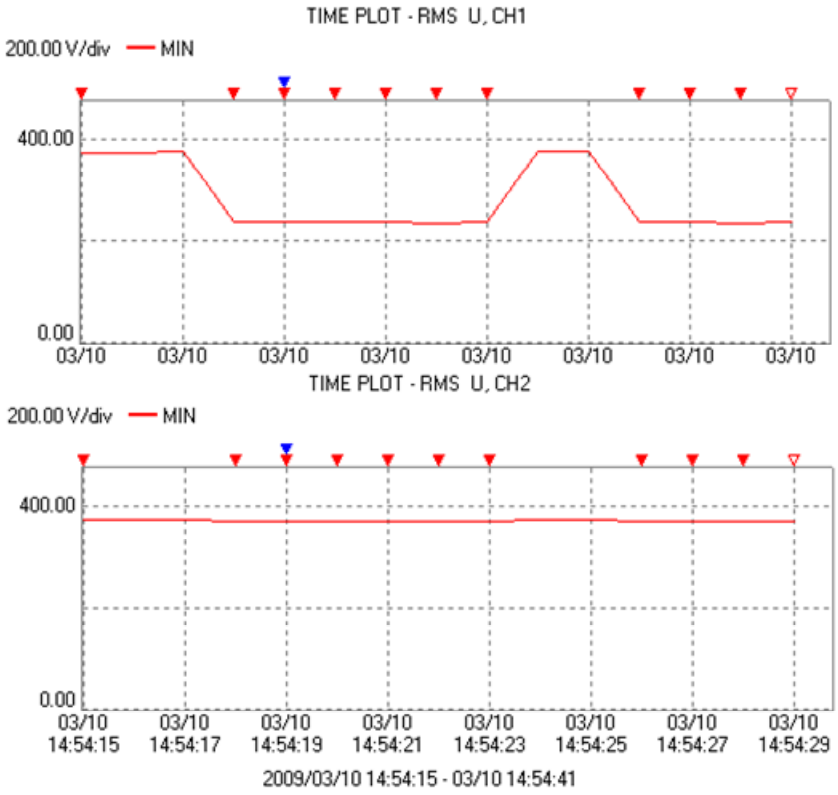

Figure 5.32. Rms voltages for preferred feeder and load bus for Case 1

Figure 5.33 shows the currents for the case. The upper part shows the current of preferred feeder and lower part shows the current of load bus. It is seen that before the sag, the load is supplied from the preferred feeder. After the sag occurred, the load is transferred to the alternate feeder.

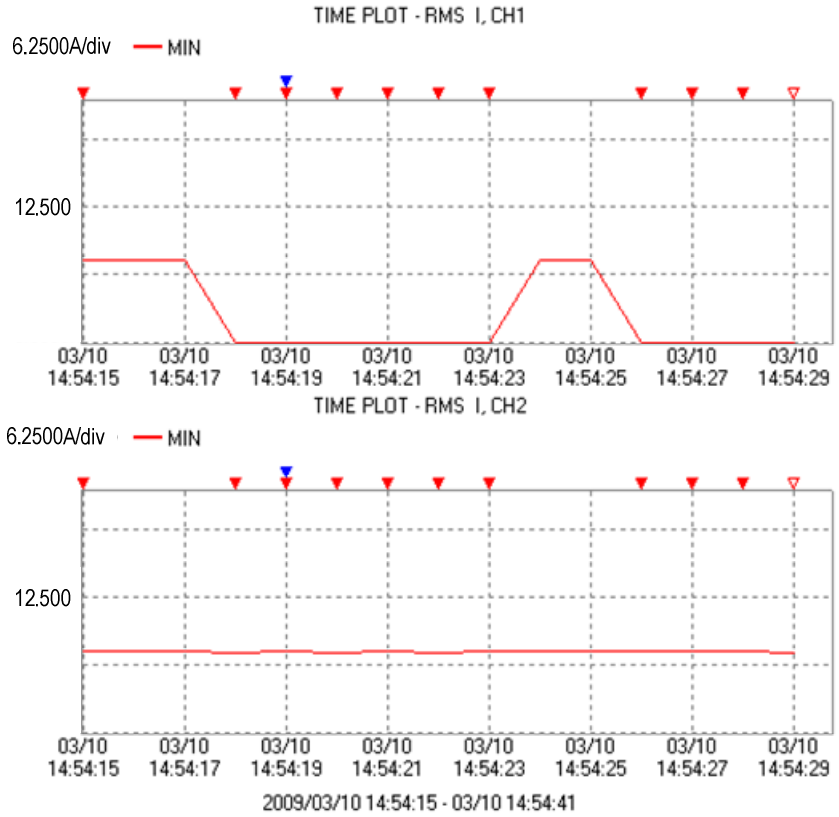

Figure 5.33. Rms current trends for preferred feeder and load bus for Case 1

Figures 5.34 and 5.35 below show the waveforms for the transfer process of preferred to alternate feeder and back. For voltages, red denotes preferred feeder, blue denotes alternate feeder and green denotes load bus. For currents, red denotes preferred feeder, blue denotes alternate feeder and green denotes load bus.

If Figure 5.34 is investigated, it is seen that the load is transferred to the alternate feeder very fast when the sag is detected on the zero crossing of preferred feeder current. But in Figure 5.35, it is seen that the current transferred back to

preferred feeder after a complete cycle of voltage on the zero crossing of alternate feeder. However, the return is not a problem anyway.

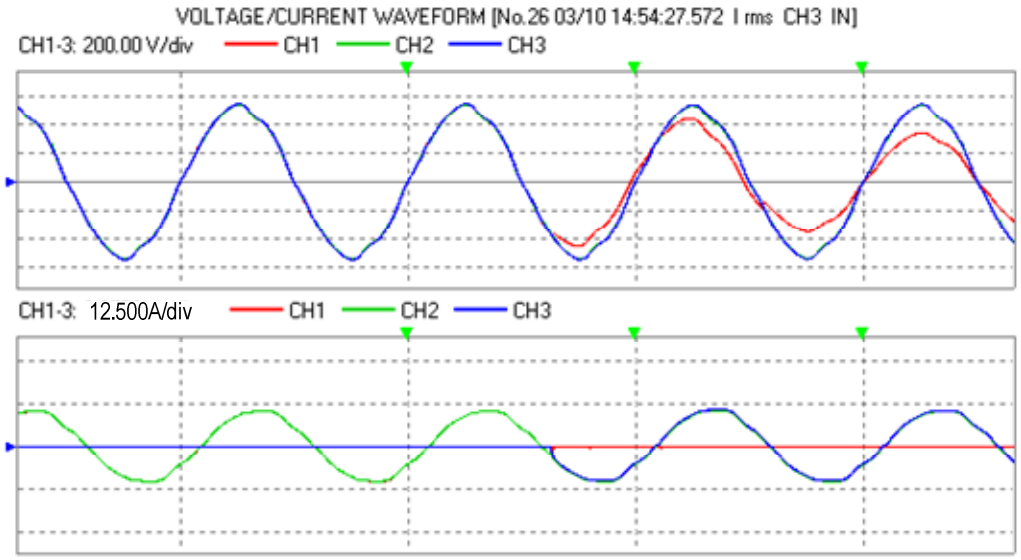

Figure 5.34. Waveforms for preferred to alternate feeder transfer for Case 1

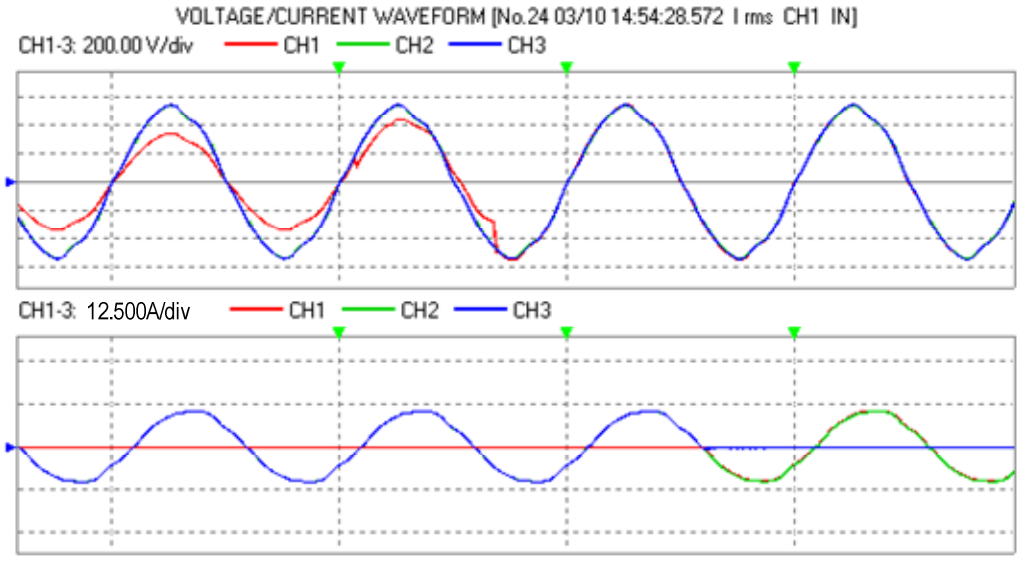

Figure 5.35. Waveforms for alternate to preferred feeder transfer for Case 1

5.3.2. Case 2: Three Phase 40% Sag, dq Detection

The rms values of preferred and load voltages are shown in Figure 5.36. The preferred feeder voltage is given on the upper part of the figure and the load bus voltage is the lower part of the figure. It is seen that several three phase sags are occurred on the preferred feeder, the load is then transferred to alternate feeder and load is not affected from any of the sags.

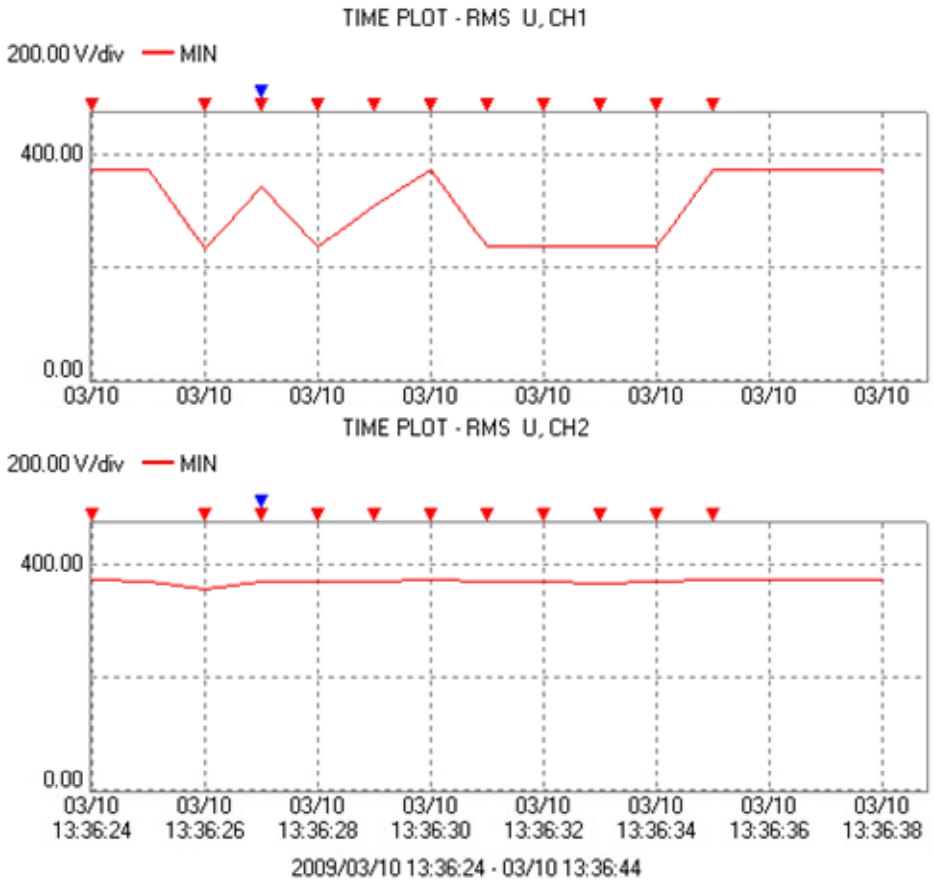

Figure 5.36. Rms voltages for preferred feeder and load bus for Case 2

Figure 5.37 shows that the load current is not affected from the sags occurred on the preferred feeder. Figures 5.38 and 5.39 below the waveforms for the transfer process of preferred to alternate feeder and back.

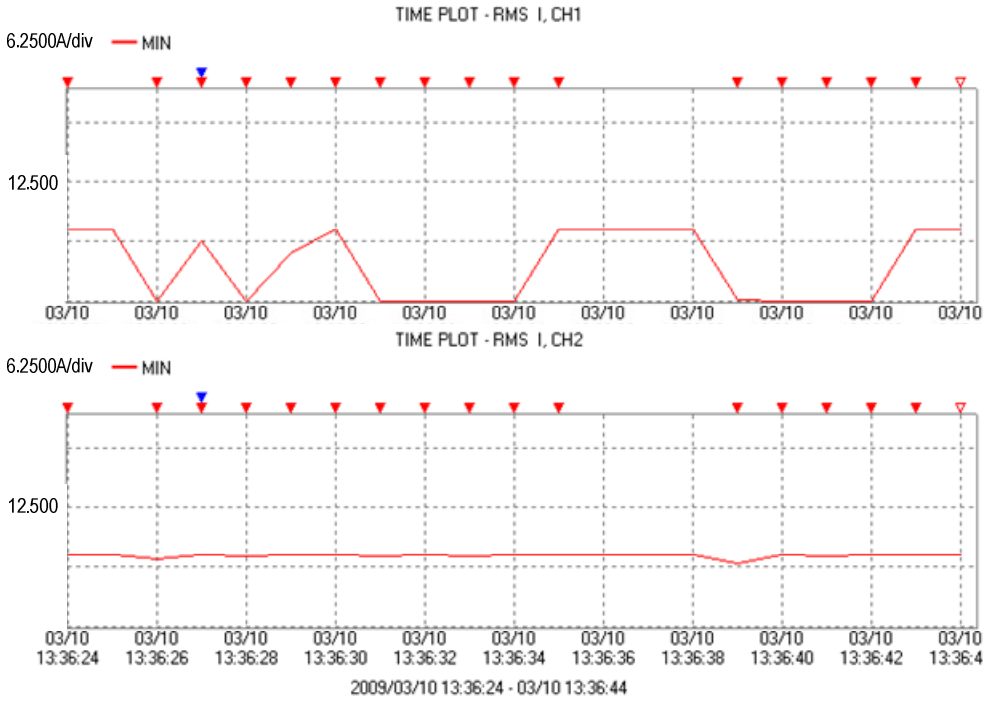

Figure 5.37. Rms current trends for preferred feeder and load bus for Case 2

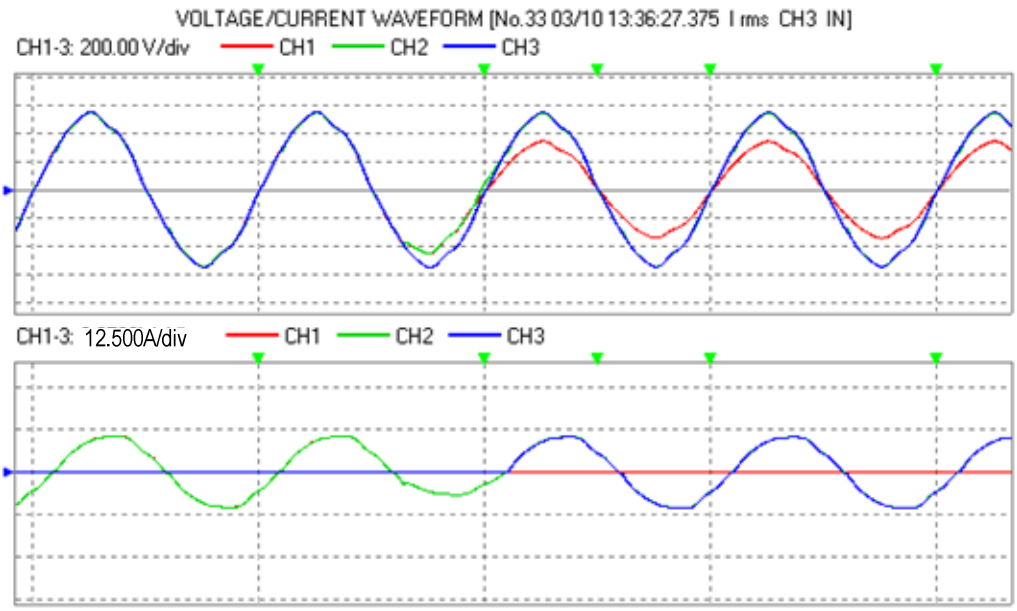

Figure 5.38. Waveforms for preferred to alternate feeder transfer for Case 2

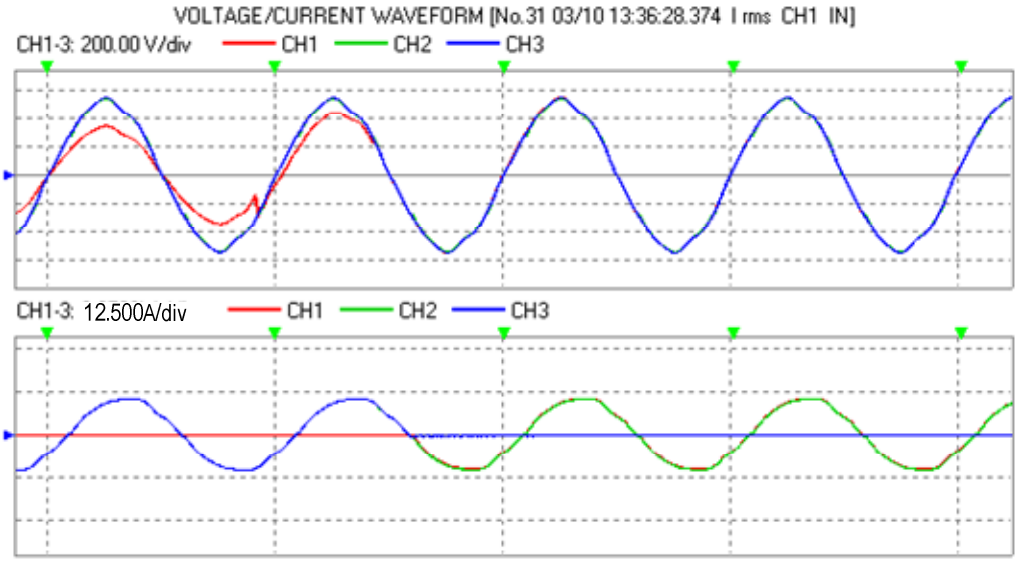

Figure 5.39. Waveforms for alternate to preferred feeder transfer for Case 2

For voltages, red denotes preferred feeder, blue denotes alternate feeder and green denotes load bus. For currents, red denotes preferred feeder, blue denotes alternate feeder and green denotes load bus. It seen from Figure 5.38 that the load is transferred to the alternate feeder after the sag is detected. However, an acceptable voltage drop occurs on the load line. In response to this, the transfer back is made faster than the PLL based method.

5.3.3. Case 3: Three Phase 20% Sag, dq Detection

The rms values of preferred and load voltages are given in Figure 5.40. The preferred feeder voltage is given on the upper part of the figure and the load bus voltage is the lower part of the figure. It is seen that several three phase sags are occurred on the preferred feeder, the load is then transferred to alternate feeder and load is not affected from any of the sags. In Figure 5.41, rms trend for the currents are given.

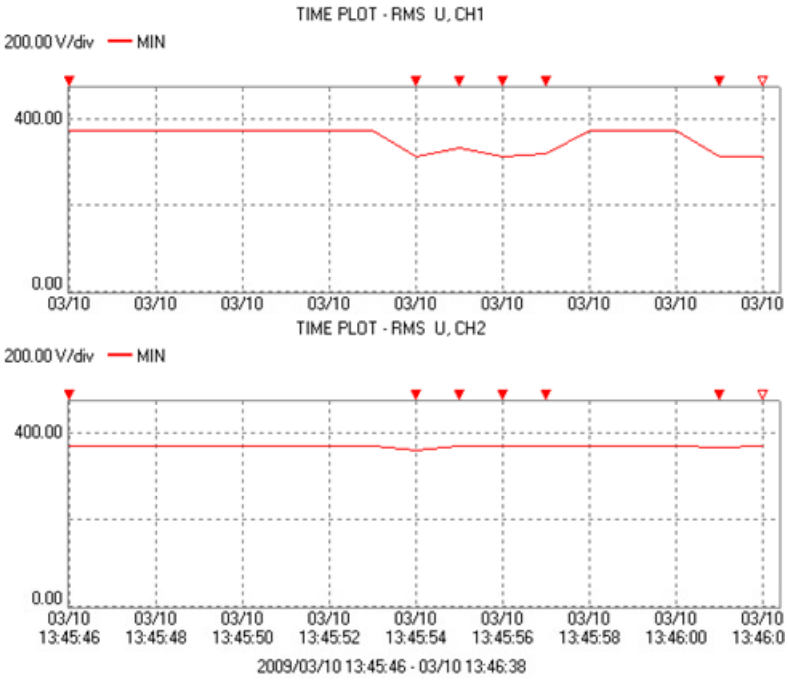

Figure 5.40. Rms voltages for preferred feeder and load bus for Case 3

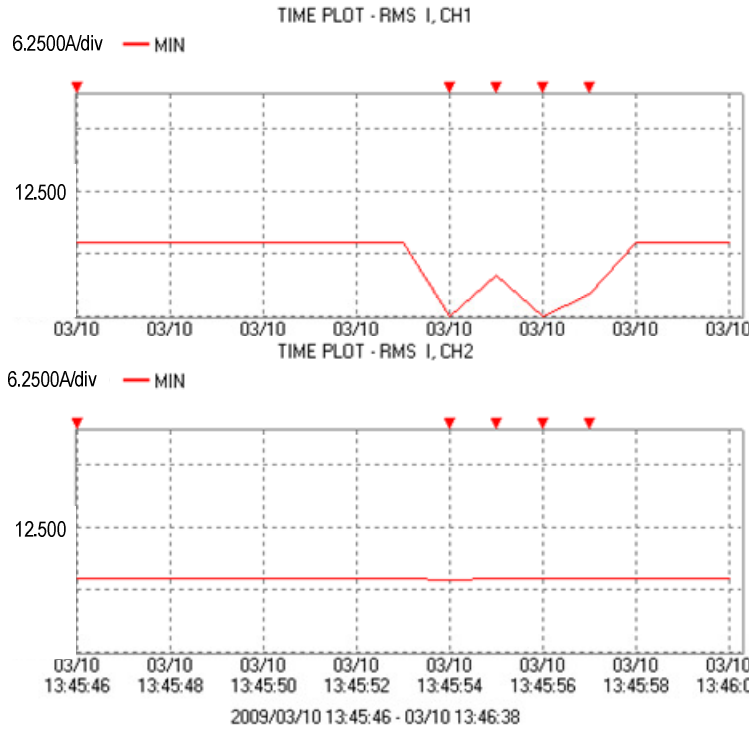

Figure 5.41. Rms current trends for preferred feeder and load bus for Case 3

Figures 5.42 and 5.43 below show the waveforms for the transfer process of preferred to alternate feeder and back. For voltages, red denotes preferred feeder, blue denotes alternate feeder and green denotes load bus. For currents, red denotes preferred feeder, blue denotes alternate feeder and green denotes load bus.

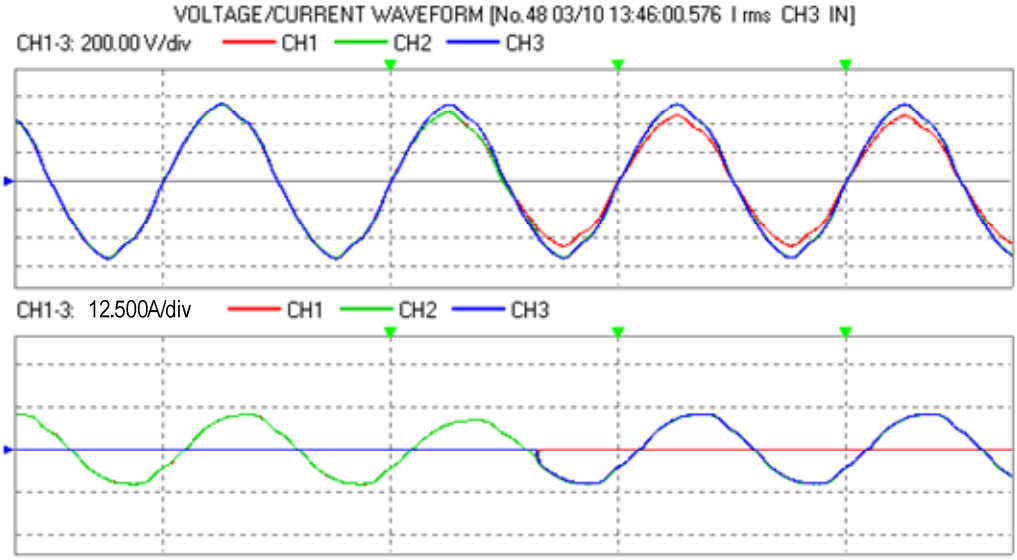

Figure 5.42. Waveforms for preferred to alternate feeder transfer for Case 3

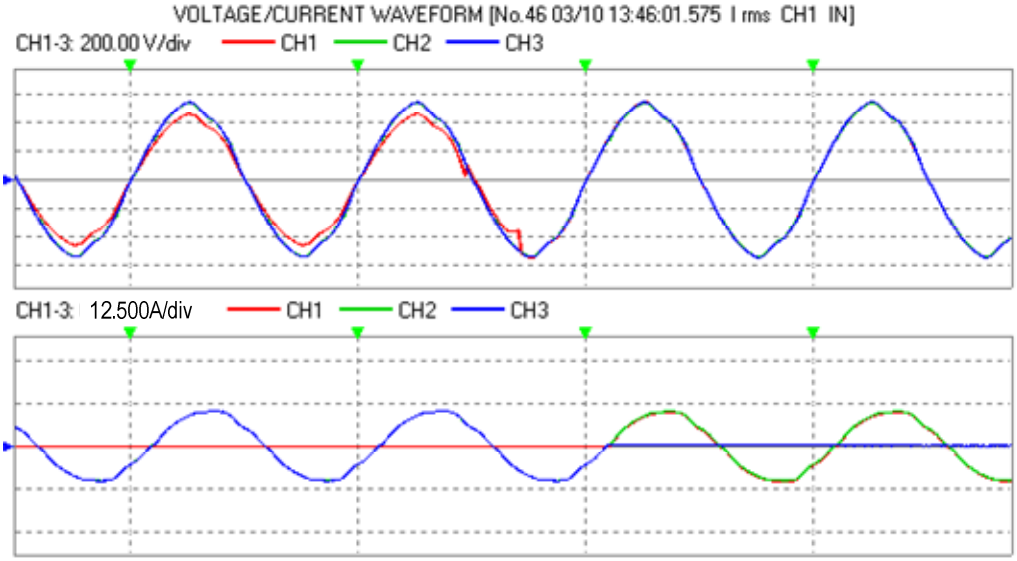

Figure 5.43. Waveforms for alternate to preferred feeder transfer for Case 3

5.3.4. Case 4: Single Phase 15% Sag, dq Detection

The main disadvantage of dq transformation based sag detection is that if there is a single phase sag on the line, it may not be detected by the method. Because the method uses the average of three phases to calculate the sag depth. So a single phase sag with small depth will not be able to produce a sag detection signal. Figure 5.44 shows the voltage trends for a single phase 15% sag on preferred feeder. As it can be seen from the figure, a sag started and continued. However, the sag detection algorithm is unable to detect the sag when the sag level is adjusted as 10% (0.1 pu) of nominal. So, the load is affected from the voltage sag. No transfer is made.

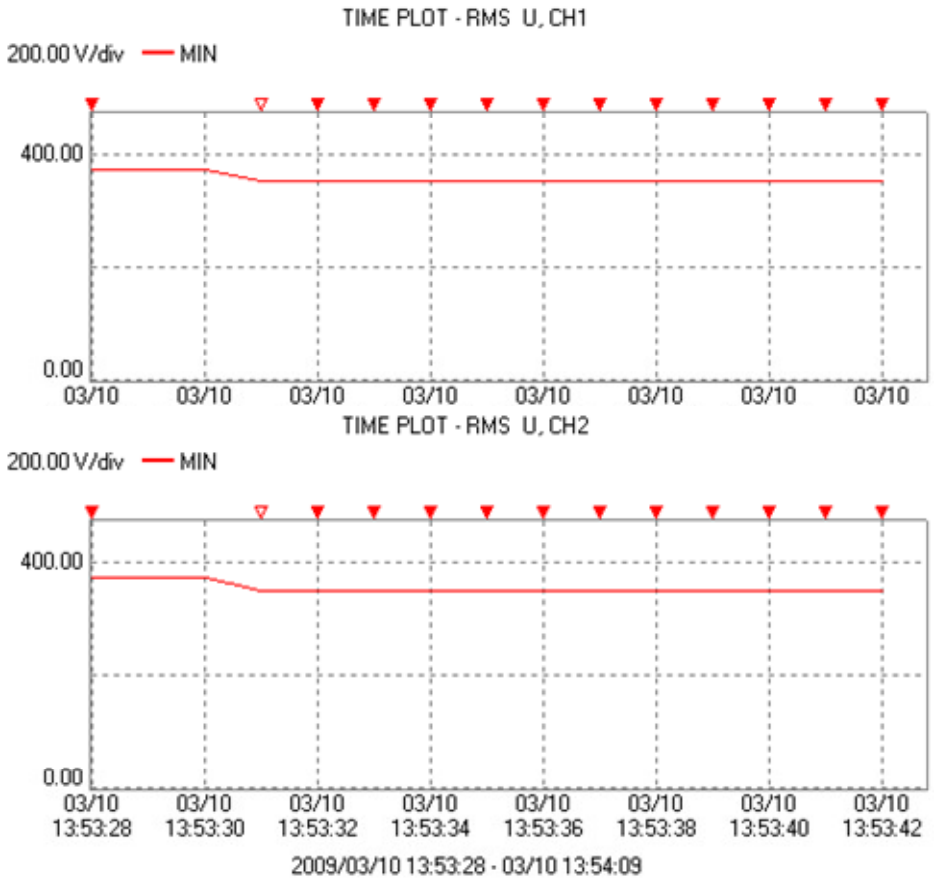

Figure 5.44. Rms voltage trend for single phase 15% sag for Case 4

Figure 5.45 is given to show the no transfer event is triggered on a single phase 15% sag. As it can be seen, the load faces the voltage sag.

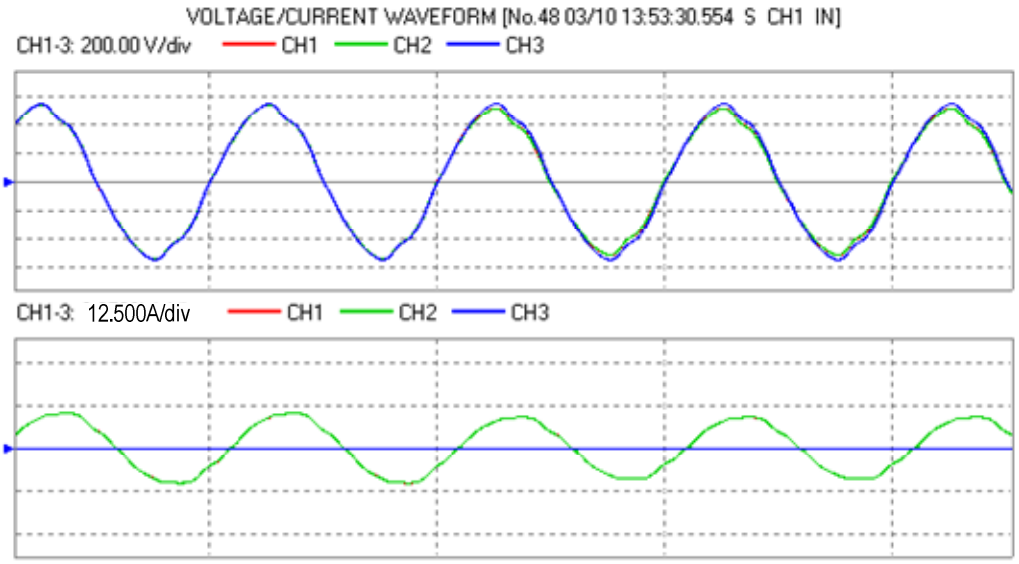

Figure 5.45. Waveform for single phase 15% sag with dq transformation based method for Case 4

5.3.5. Case 5: Three Phase 30% Sag on Both Feeders

In this case, there are 30% sags on both preferred and alternate feeders. Figure 5.46 is used to show the voltage trends for this case. The same magnitude of sags is applied to preferred and alternate feeders. So, the V_{alt} and V_{pref} signals are 0 at the same time. Recalling from the transfer logic, the load should not be transferred to alternate feeder in this case. Figure 5.47 shows that no transfer occurred in this case. The load is continued to supplied from the preferred feeder although there is a sag on the line.

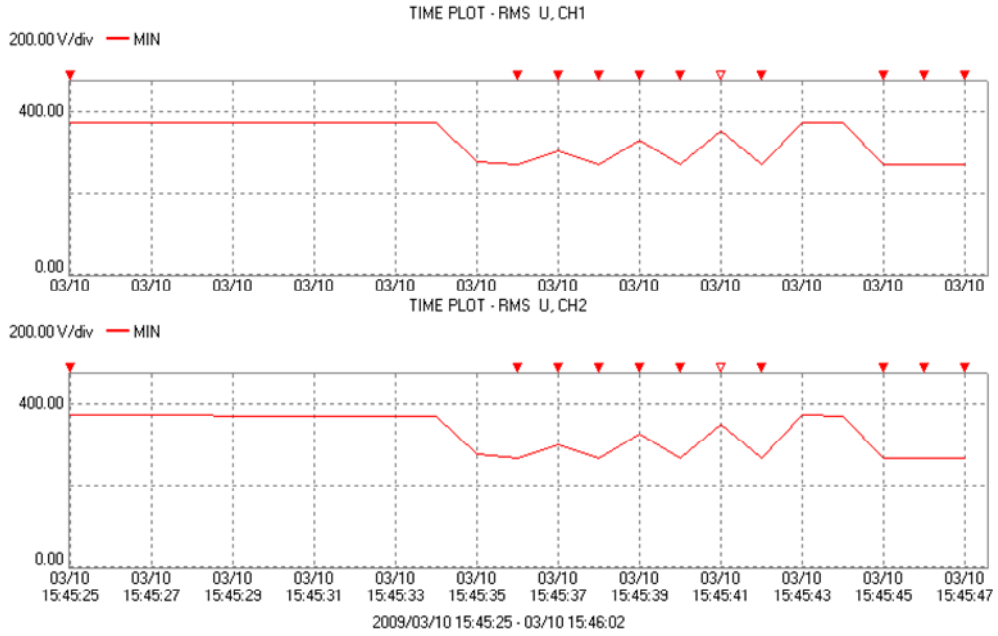

Figure 5.46. Rms voltage trends for preferred feeder and load bus for Case 5

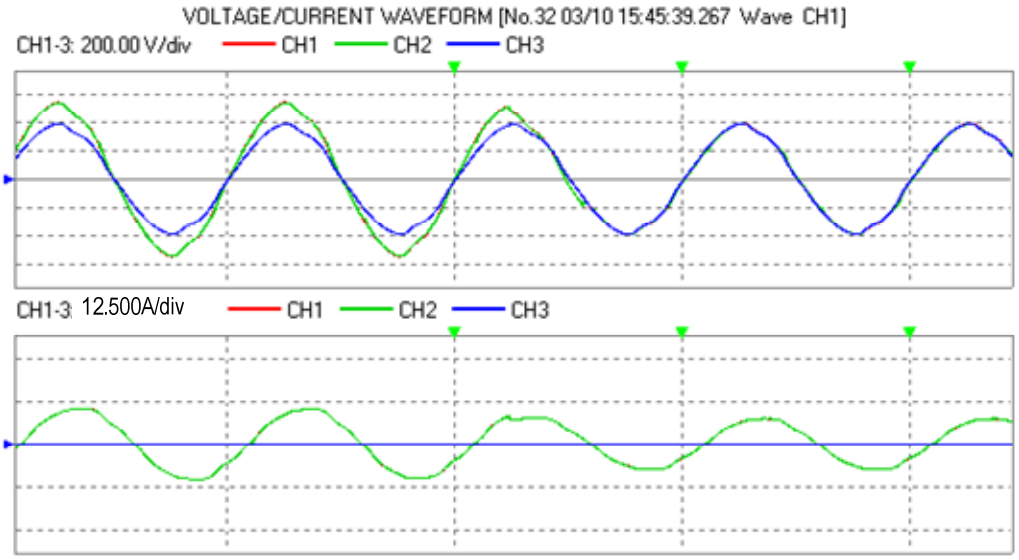

Figure 5.47. Waveforms for three phase 30% sags on both feeders for Case 5

6. IMPLEMENTATION OF DSP BASED SHUNT ACTIVE POWER FILTER

The simulation model of SAPF is developed by the use PSCAD/EMTDC program. The parameters are updated after the experimental study as ideal parameters does not give adequate results that a real system can give. Following sections presents both software and hardware design of SAPF and results of the study.

6.1. Design of Shunt Active Power Filter

This section covers the design of control algorithms and power circuit of SAPF. In the control of SAPF, instantaneous reactive power theory is used to calculate the compensating current signals. Hysteresis current control is used to generate the required switching signals.

6.1.1. Controller Design of Shunt Active Power Filter

The control system of the proposed SAPF is shown in Figure 6.1. V_{AB} source voltage and load currents and actual filter currents are the input for the control system. The output of the control system is reference I_{aRef}, I_{bRef} and I_{cRef} currents. The filter currents are subtracted from reference currents to obtain error signals used. The error signals are applied to hysteresis controller to get to firing pulses of the IGBTs.

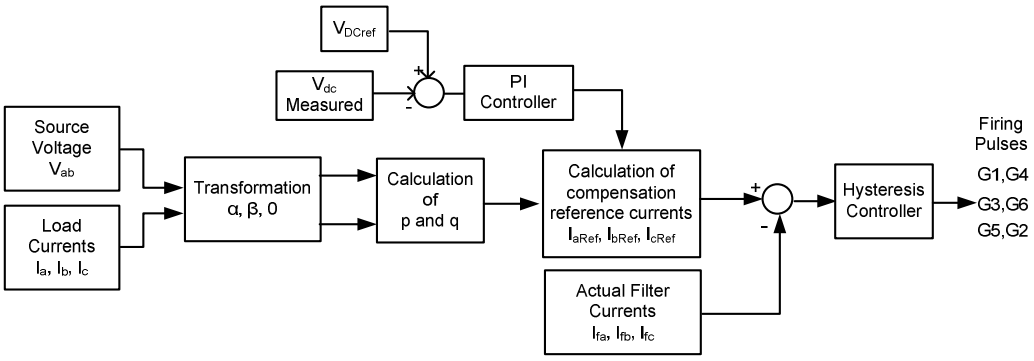

Figure 6.1. Control block diagram of SAPF

6.1.1.1. Instantaneous Reactive Power Theory

Instantaneous Reactive Power Theory (p-q theory) is based on set of instantaneous powers defined in the time domain and uses the Park Transform. No restrictions are imposed on the voltage or current waveforms and it can be applied to three phase systems with or without a neutral wire for three phase generic voltage and current waveforms. Thus, it is valid not only in the steady state but also in the transient state. This theory is very efficient and flexible in designing controllers for power conditioners based on power electronics devices (Akagi et al., 2007).

In three-phase circuits, instantaneous currents and voltages are converted to instantaneous space vectors. In instantaneous power theory, the instantaneous three-phase currents and voltages are calculated as following equations. These space vectors are easily converted into the alpha-beta orthogonal coordinates (Kale and Ozdemir, 2005), (Akagi et al., 1986).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{6.1}$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{6.2}$$

Considering only the three-phase three-wire system, the three-phase currents can be expressed in terms of harmonic positive, negative and zero sequence currents. In Equations (6.1) and (6.2), α and β are orthogonal coordinates. V_α and I_α are on α axis, V_β and I_β are on β axis. In three-phase conventional instantaneous power is calculated as follows:

$$p = V_\alpha I_\alpha + V_\beta I_\beta \tag{6.3}$$

In fact, instantaneous real power (p) is equal to following equation:

$$p = V_a I_a + V_b I_b + V_c I_c \tag{6.4}$$

Instantaneous real and imaginary powers are calculated as;

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \tag{6.5}$$

In Equation (6.5), $V_\alpha I_\alpha$ and $V_\beta I_\beta$ are instantaneous real "p" and imaginary "q" powers. Since these equations are products of instantaneous currents and voltages in the same axis, in three-phase circuits, instantaneous real power is "p" and its unit is watt. In contrast $V_\alpha I_\beta$ and $V_\beta I_\alpha$ are not instantaneous powers. Since these are products of instantaneous current and voltages in two orthogonal axes, "q" is not conventional electric unit like watt or VAr. The value "q" is instantaneous imaginary power and its unit is imaginer volt ampere (IVA) (Kale and Ozdemir, 2005). These power quantities given above for an electrical system represented in a–b–c coordinates and have the following physical meaning (Kale and Ozdemir, 2005).

$\bar{p}$, is the mean value of the instantaneous real power, corresponds to the energy per time unity which is transferred from the power supply to the load, through a–b–c coordinates, in a balanced way.

$\tilde{p}$, is the alternated value of the instantaneous real power, it is the energy per time unity that is exchanged between the power supply and the load through a–b–c coordinates.

$\bar{q}$, instantaneous imaginary power, corresponds to the power that is exchanged between the phases of the load. This component does not imply any exchange of energy between the power supply and the load, but is responsible for the existence of undesirable currents, which circulate between the system phases.

$\tilde{q}$, is the mean value of the instantaneous imaginary power that is equal to the conventional reactive power.

The instantaneous active and reactive power includes AC and DC values and can be expressed as follows:

$$p = \bar{p} + \tilde{p} \qquad q = \bar{q} + \tilde{q} \tag{6.6}$$

DC values of the "p" and "q" are created from positive-sequence component of the load current. AC values of the "p" and "q" are produced from harmonic components of the load current (Kale and Ozdemir, 2005). Equation (6.5) can be written as Equation (6.7):

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p \\ q \end{bmatrix} \tag{6.7}$$

From Equation (6.7), in order to compensate harmonics and reactive power instantaneous compensating currents $i_{c\alpha}$ and $i_{c\beta}$ on α and β coordinates are calculated by using $-\tilde{p}$ and $-q$ as given below:

$$\begin{bmatrix} I_{CP\alpha} \\ I_{CP\beta} \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix}^{-1} \begin{bmatrix} -\tilde{p} \\ -q \end{bmatrix} \tag{6.8}$$

The feedback method used to control self-supporting DC bus is very important. The procedure consists of controlling the capacitor voltage to a reference value. To achieve it, a PI control may be chosen for the error between the reference value and the capacitor voltage value at the end of each period. The result is the value of the compensator lost power. This value modifies the power terms, which appear in the compensation current expressions. This term is multiplied with a constant and added as an error to the filtered value of the instantaneous real power (Herrera et al., 2008).

In order to obtain the reference compensation currents in the a–b–c coordinates the inverse of the transformation given in Equation (6.9) is applied (Kale and Ozdemir, 2005):

$$\begin{bmatrix} I^{*}_{CPa} \\ I^{*}_{CPb} \\ I^{*}_{CPc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{CP\alpha} \\ I_{CP\beta} \end{bmatrix} \tag{6.9}$$

6.1.1.2. Hysteresis Current Control

The basic of the hysteresis current control is based on an error signal between an injection current "I_{inj}" and a reference current of SAPF "I_{ref}" which produces proper control signals. The hysteresis band current controller decides the switching pattern of SAPF (Ezoji, 2009). The conventional hysteresis band current control scheme is used for the control of SAPF. There are bands above and under the reference current and when the error reaches to the upper (lower) limit; the current is forced to decrease (increase) as shown in Figure 6.2.

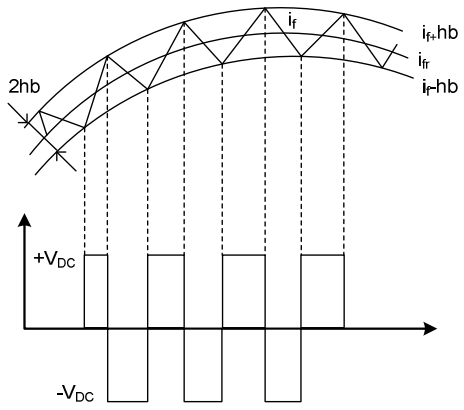

Figure 6.2 Voltage and current waveforms of hysteresis band control

6.1.1.3. DSP Software Flowcharts of Shunt Active Power Filter

The flowchart of the SAPF controller is presented in Figure 6.3. Appendix B, Listing B.3. is the C implementation of SAPF controller. Processor starts with C_int0 interrupt and calls the main routine shown in the left hand side of the Figure 6.3. In this routine, global variables are defined that will be used program wide firstly. Thereafter, object oriented software modules are initialized. CPU timer is configured to determine the sampling time. The sampling time is adjusted to be 25 μs. Six of the output pins of the DSP are adjusted to generate firing pulses. In the last step, analog-to-digital converter module is initialized. There are two 8 channels analog input multiplexer on F28335. ADC module is adjusted to use simultaneous sampling method that is each channel pair of multiplexers is sampled at the same time. The main function gets in an endless loop and waits for the timer interrupt, INT1, to occur.

Every occurrence of INT1 interrupt is accepted to be a sampling interval. The source voltages and currents, filter currents and DC link capacitor voltage are measured first.

DC link voltage control is important as it affects the THD level. Digitization is not an ideal process because of quantization errors. To stabilize the measured DC link voltage, although it is filtered in signal conditioning board, a digital low pass filter with a cut off frequency of 15 Hz is also applied.

A variable named “start” is used to control the states of the DSP controller. If the value of “start” variable is “0”, an averaging operation on measurement channels is made. The average of any of the channels gives the mean offset error for that channel. These calculated average offset errors are subtracted from the measured values to find the exact values of measurement if the value of “start” is great equal to “1”. The value of “2” in “start” variable means SAPF is in compensation state. From Figure 6.3, it can be seen that the ADC offset correction is made if the value of “start” is “1”.

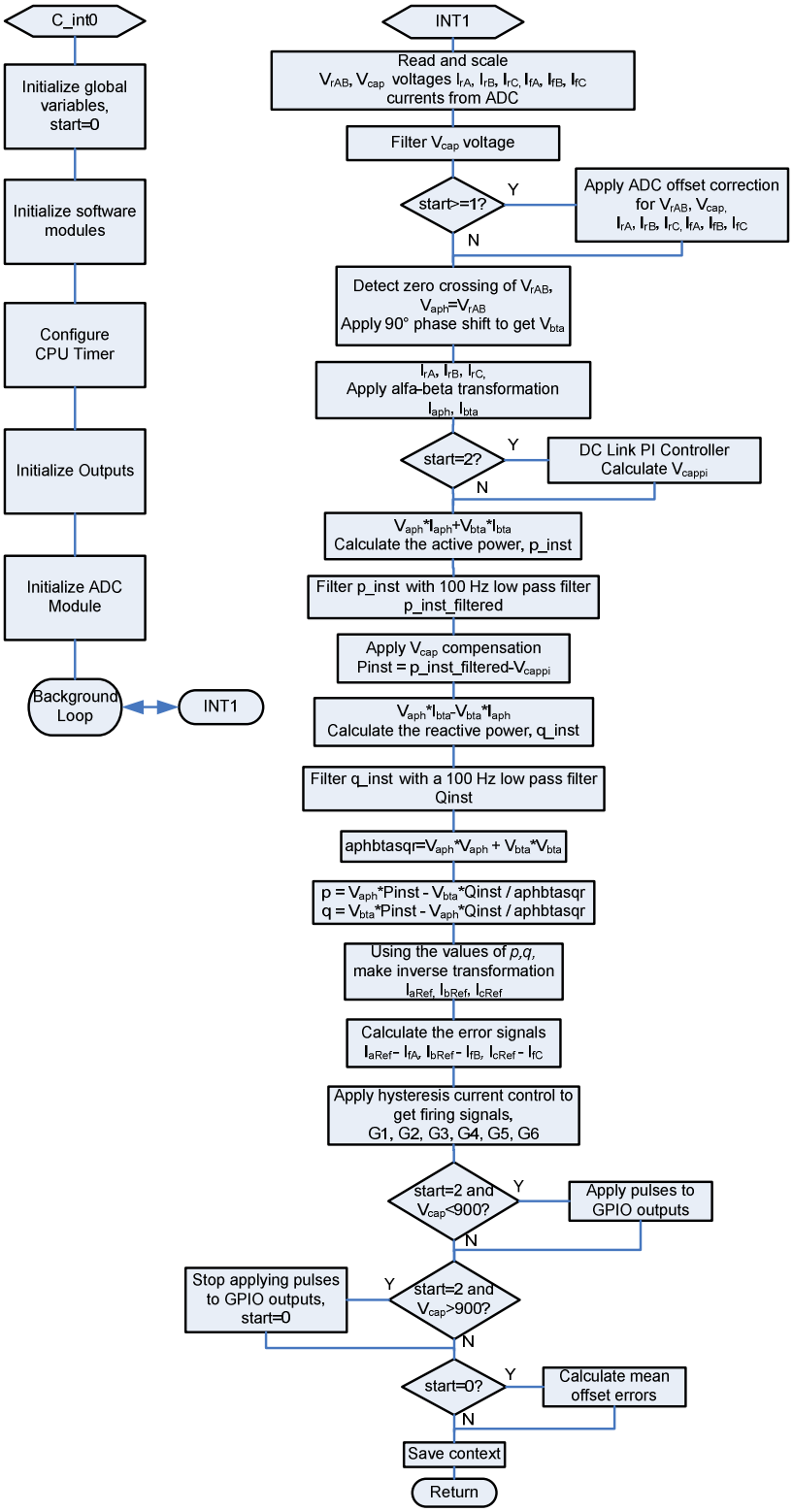

Figure 6.3. DSP control flowchart of SAPF

During the experimental studies, it is seen that any unbalance and harmonics in source voltages result in increased THD content. To overcome this problem, only one voltage measurement is used and with the use the measured value, 90 degree phase shifted virtual voltage is generated. The generation of this virtual voltage depends on the detection of zero crossing of phase-to-phases voltage of A and B phases. With the zero crossing detection, frequency compensation is made on virtual voltage. By this method, the unbalances between measured source voltages are eliminated.

With the alpha-beta transformation, voltages and currents are transformed into alpha-beta components. A PI controller is used to compensate the DC link capacitor voltage if the SAPF is in compensation state. The instantaneous active power is calculated by the using the transformed values and they are applied to a 100 Hz digital low pass filter. The filtered active power value is summed by the output of the voltage controller to be used in reverse transformation. With a similar way, the reactive power value is calculated and a reverse transformation is made by using the active and reactive power values.

The reverse transformation gives the reference current signal that must be injected to the line to compensate the current harmonics. The controller uses a hysteresis function to generate the firing pulses to the IGBT drivers. If the value of "start" is "2" and the DC link voltage is less than 900 V_{DC} which is the maximum permissible DC link voltage, than firing pulses are applied to DSP outputs. If "start" is set to "2" but the DC link voltage is gets greater than 900 V_{DC}, the all of the DSP outputs going to SAPF are set to zero resulting in protection state. If such a case occurs, the value of "start" variable is set to "0" automatically.

6.1.2. Hardware Design of DSP Based Shunt Active Power Filter

The experimental setup used in SAPF studies is presented in Figure 6.4. The three phase diode rectifier module (Semikron SKD62/16) is used to generate current harmonics. This module is supplied via choke reactors which prevent current overlapping. 45 ohm resistive load is fed from the output of diode rectifier

Three phase three leg IGBT inverter is used as the voltage source converter. This inverter is fed from a DC link capacitor bank. This bank is formed by two series and two parallel connections of four 450V, 2200μF DC capacitors. By this way, DC voltage rating of the filter is adjusted to $900V_{DC}$ while maintaining 2200 μF of capacitor value.

The output of the VSI is connected to the line via interface reactors. These reactors are used to convert the voltage output of inverter to current. Without interface reactors, active power filter could not inject the necessary currents to the line.

CTF-5A current transformers are used to step down the filter and load currents. A signal conditioning board is designed to measure source voltages and DC link capacitor voltage by the use LV25-P voltage transducers and the stepped down filter and load currents. The detailed description of this board is given in the following sections.

TMS320F28335 DSP kit is used as the controller of SAPF. This DSP offers floating point unit which increases the performance of the control algorithms. TMS320F28335 DSP kit is directly connected on the signal conditioning board.

The outputs of the TMS320F28335 DSP are applied to a protection and firing board. This board is responsible to protect the overall system by closing the firing pulses going to IGBT drivers. The board senses the voltage and current levels on the system and makes analog protection by the use of logic. The firing section is used as a buffer between the outputs of DSP kit and IGBT drivers.

Three Semikron SKHI 22B H4 IGBT drivers are used to drive three Semikron SKM75GB123D dual IGBT modules.

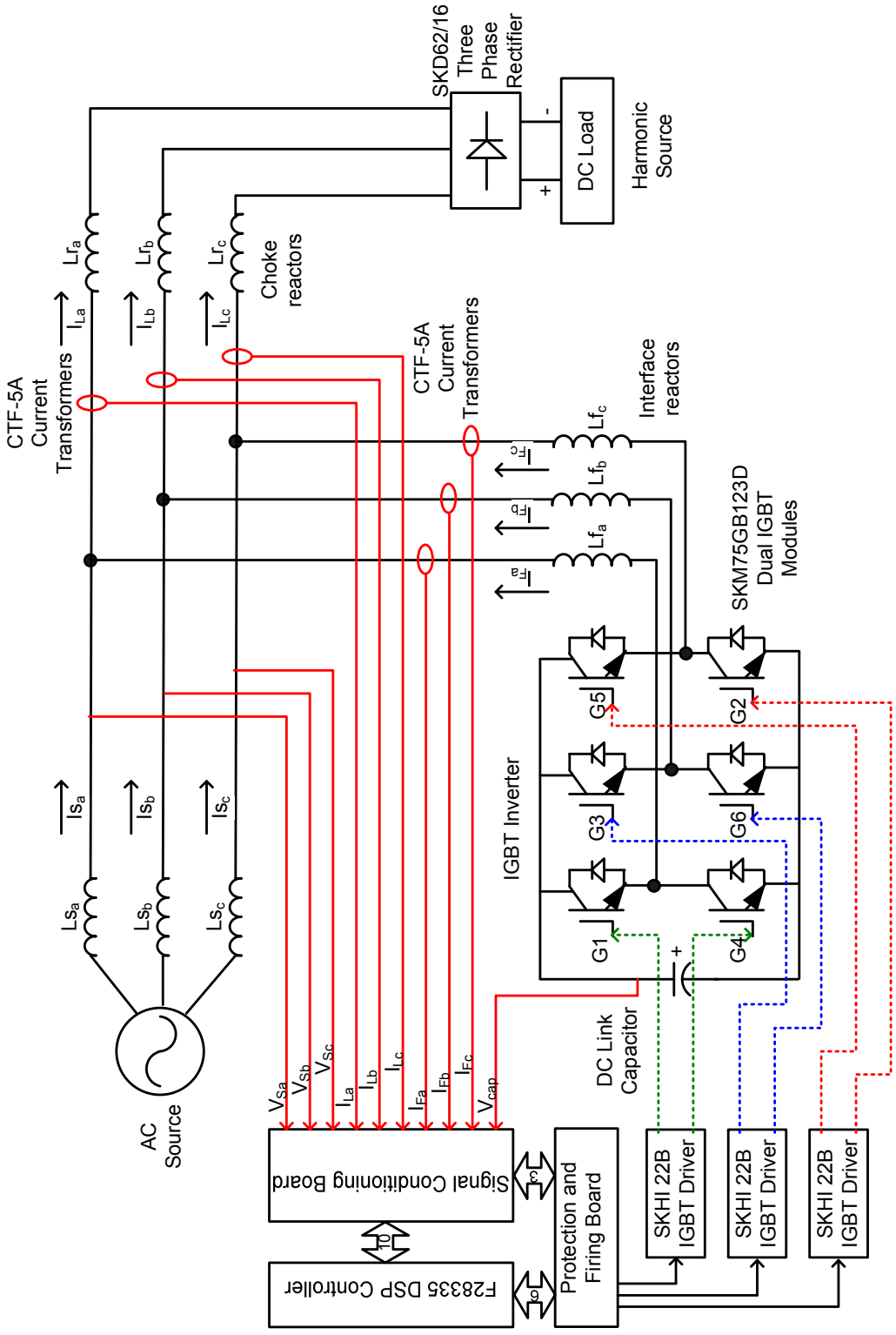

Figure 6.4. Experimental block diagram of SAPF

The parameters of experimental SAPF are given in Table 6.1. These parameters are also used in simulation model.

Table 6.1. SAPF system parameters

System voltages	Phase A: 233 Vrms, 2.5% THD Phase B: 232 Vrms, 2.4% THD Phase C: 228 Vrms, 2.4% THD
Smoothing reactor	Phase A: 19.41 mH Phase B: 20.04 mH Phase C: 19.49 mH
Choke reactor	Phase A: 6.14 mH Phase B: 6.07 mH Phase C: 6.21 mH
Sampling time	25 μs
DC link capacitor and voltage	2200 μF, 650 Vdc

6.1.2.1. Signal Conditioning Board

To accurately measure the source voltages, DC link voltage, load and filter currents, a signal conditioning board is designed. The design is based on the signal processing boards used in (Ucak, 2009). The circuit diagrams of signal conditioning board are given in Appendix C. Figure 6.5 is the picture of the signal conditioning board.

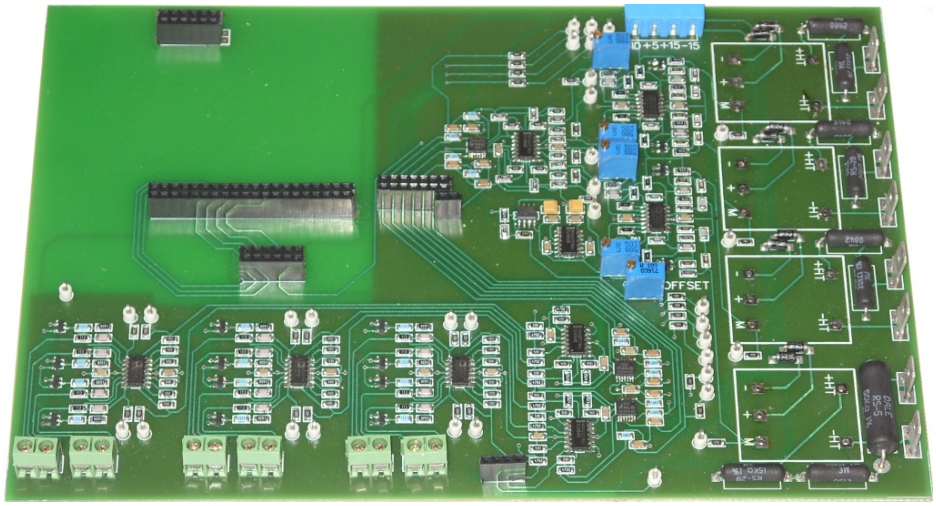

Figure 6.5. Picture of signal conditioning board of SAPF

The secondary sides of CTF-5A current transformers are connected to six connectors on the left bottom of the signal conditioning board. CTF-5A current transducers output a current in -1.5 degrees phase lead. The three sub circuits on the above of the connectors are difference amplifiers. These difference amplifiers have two duties; one is to amplify the difference of the applied voltage to their input and second is to introduce 1.5 degrees phase delay to their output. By this way, the leading current measurements are compensated. Figure 6.6 is the circuit diagram for a difference amplifier. Equation (6.10) gives the relationship between inputs and output of the difference amplifier.

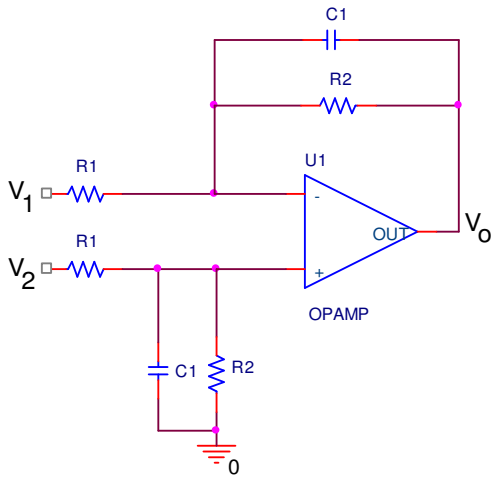

Figure 6.6. Difference amplifier circuit diagram

$$V_o = (V_2 - V_1)\frac{R_2}{R_1} \tag{6.10}$$

The right side of Figure 6.5 shows the connection points of voltages. Three source voltages and DC link voltage are connected to these connectors. LEM LV25-P voltage transducers are placed on the bottom side of the signal conditioning board. The outputs of this transducer must be filtered before applying to the ADC inputs as any voltage harmonic results in increased THD content in the inverter output. The sallen-key low pass filters with a cut off frequency of 50 Hz are used to filter the

voltage measurements. The Sallen–Key topology is an electronic filter topology used to implement second-order active filters that is particularly valued for its simplicity. The circuit diagram for a sallen-key low pass filter is given in Figure 6.7. These filters introduce phase delays. Equation (6.11) gives the relation between the input and output of the sallen key filters. The cut off frequency of the filter is determined using Equation (6.13).

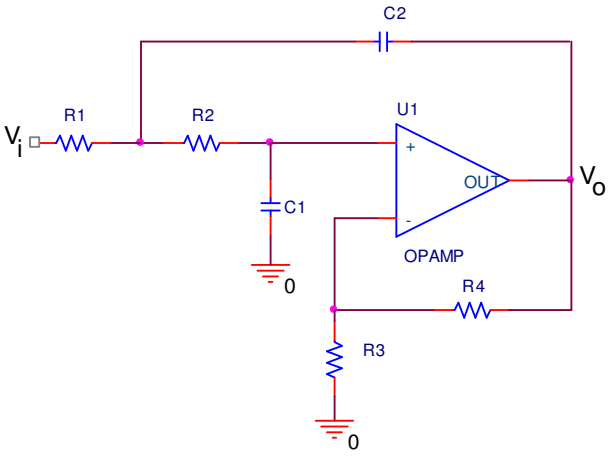

Figure 6.7. Sallen-key low pass filter circuit diagram

$$\frac{V_o}{V_i} = \frac{K}{s^2(R_1R_2C_1C_2) + s(R_1C_1 + R_2C_1 + R_1C_2(1-K)) + 1} \tag{6.11}$$

$$K = 1 + \frac{R_4}{R_3} \tag{6.12}$$

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \tag{6.13}$$

To compensate phase delays introduced by low pass filters, the outputs of the sallen-key low pass filters are applied to all pass filters. Figure 6.8 shows an all pass filter. All pass filters introduce a phase shift that goes from -180° to 0° and 0° at high frequencies. The phase shift will be -90° at frequency determined by Equation (6.14).

$$\omega = \frac{1}{RC} \tag{6.14}$$

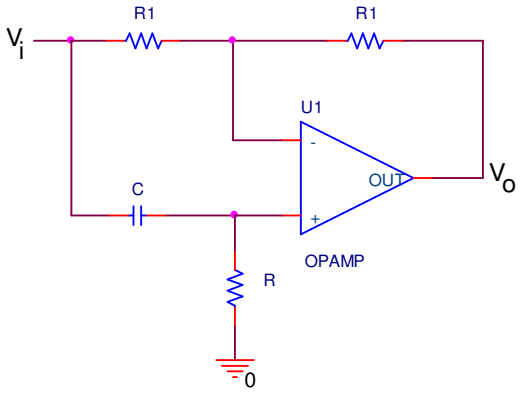

Figure 6.8. All pass filter circuit diagram

The outputs of both voltage and current measurement circuits are bipolar. As the ADC inputs of DSP accept only unipolar signals, +1.5V offset must be added for all the measurements. To achieve this goal, non-inverting summing amplifiers are used in signal conditioning board. A non-inverting amplifier circuit diagram is given in Figure 6.9. The relation between the summing inputs V_1, V_2 and output V_o is given in Equation (6.15).

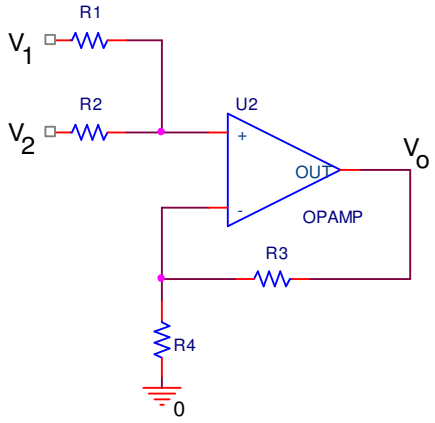

Figure 6.9. Non-inverting summing amplifier circuit diagram

$$V_o = (R_1 V_2 + R_2 V_1)\frac{R_3 + R_4}{(R_1 + R_2)R_4} \tag{6.15}$$

6.1.2.2. Protection and Firing Board

This board is responsible to drive the IGBT drivers while making protection functions at the same time. The outputs of signal conditioning board are limited to 3V DC as the ADC inputs of DSP are 3V compatible. A voltage level greater than 3V means the measured signal gets out of limits. An adjustable voltage compare level is used to control the SAPF voltage and currents. Any voltage above the compare level stops the firing signals going to the drivers. This is achieved by comparing the compare voltage level with measurement outputs. The comparator output is connected to a monostable multivibrator that changes it's output state to "0" for 10 seconds. The output of multivibrator and firing pulses from DSP are applied to an AND logic gate. As a result, if the multivibrator output is logic "0" output of AND gate is "0" for all firing pulses. The simplified circuit diagram for protection and firing board is given in Figure 6.10. Figure 6.11 is the picture of this board. The design of protection and firing board is based on (Ucak, 2009).

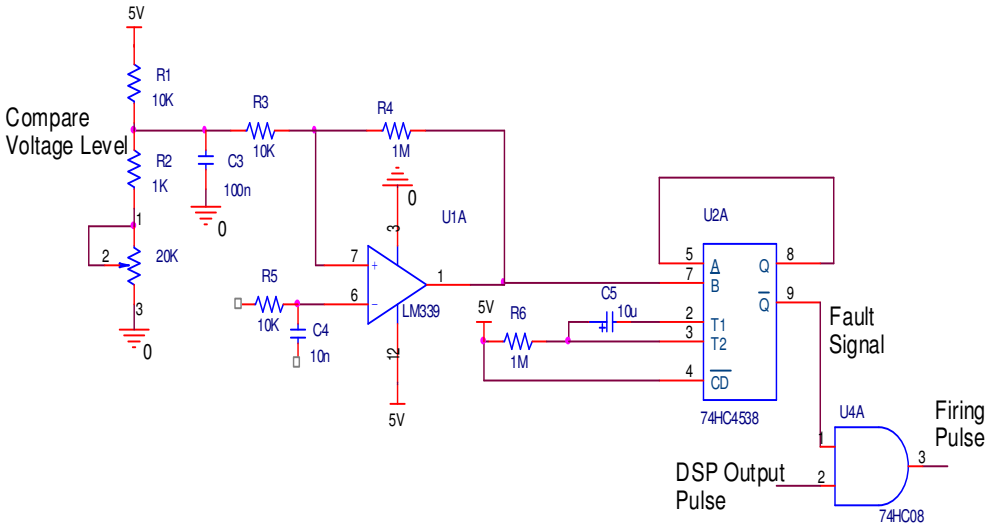

Figure 6.10. Protection and firing board circuit diagram

In fact, TMS320F28335, signal conditioning board, protection and firing board forms the complete control board as shown in Figure 6.12. Signal conditioning board becomes the main board and located at the bottom of the other two boards. TMS320F28335 DSP kit is in the right bottom of the picture where protection and firing board is on the right top.

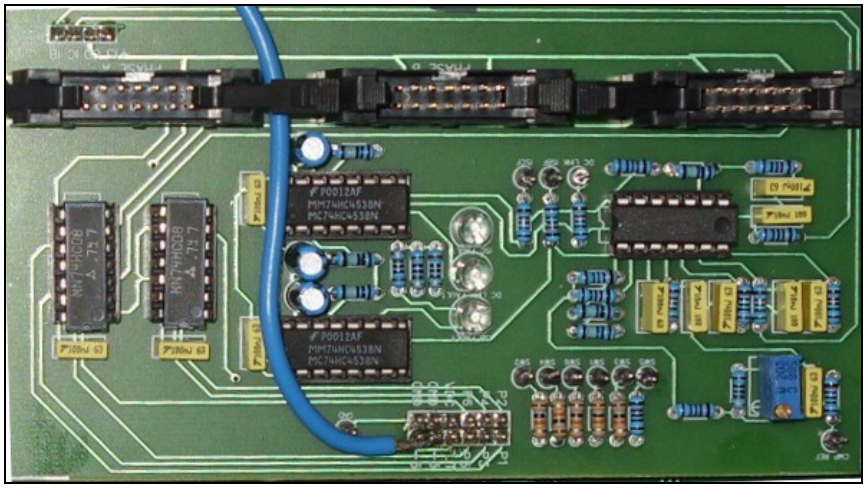

Figure 6.11. Picture of protection and firing board

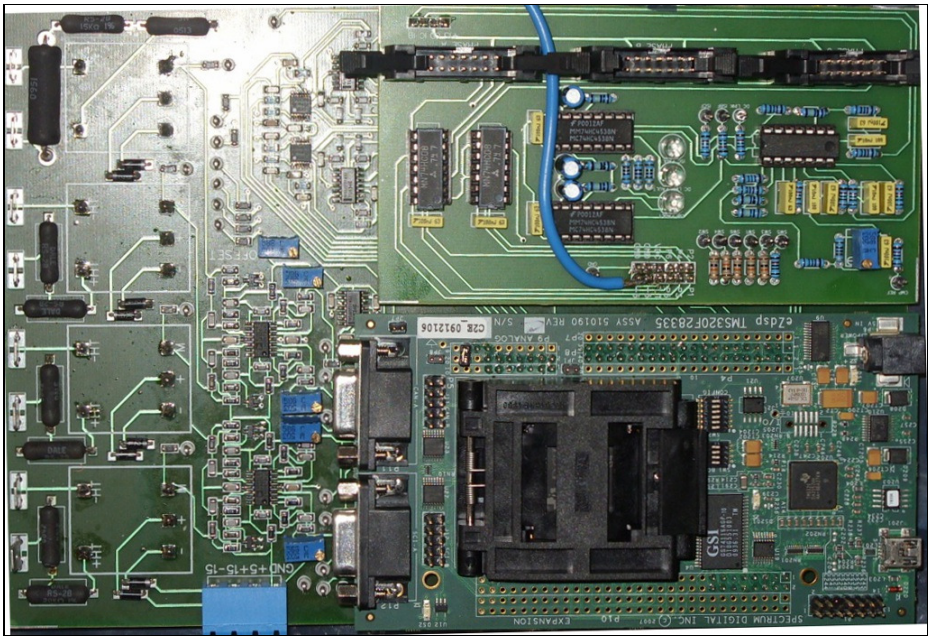

Figure 6.12. SAPF control board

6.1.2.3. Three Phase IGBT Inverter and DC Link Capacitors

Three Semikron SKM75GB123D IGBT modules are used to construct the three wire IGBT inverter as shown in Figure 6.13. The DC link capacitors are in two series and two parallel configuration. The DC link capacitors are connected to the IGBT inverter via busbars. Four $1600V_{DC}$ 0.22 µF snubber capacitors are also added to the inverter to suppress overshoots. IGBT drivers are also seen in the figure.

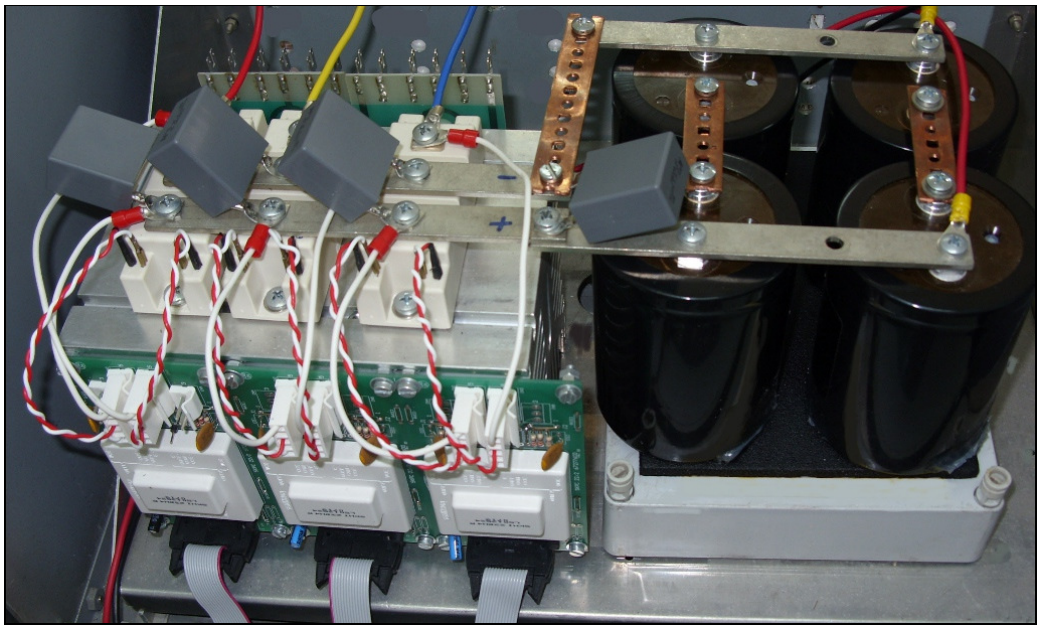

Figure 6.13. SAPF inverter with DC link capacitors

6.1.2.4. Interface and Choke Reactors

To filter out the high frequency components caused by the triggering of IGBT modules, an output inductor is connected between the line and inverter output. A method to solve the inductor value problem has been given as (Moran et al., 1992):

$$\lambda = 4\xi f \tag{6.16}$$

$$L_f = \frac{V_{an} + V_{dc}/2}{4\xi f} \tag{6.17}$$

L_f is the value of the output reactor,

ξ is the amplitude of the triangle wave,

f is the switching frequency,

V_{an} is the phase-neutral source voltage,

V_{dc} is the capacitor voltage

To overcome the problems seen in the diode bridge applications, choke inductors are used in the study. In paper (Guru et al., 1998), a formula is developed for the calculation of the value of the shock inductors is given. The interface and choke inductors are shown in Figure 6.14.

$$L_{ch} = Z_L * (1 - 3\%) \tag{6.18}$$

L_{ch} is the choke inductor,

Z_L is the load impedance

Figure 6.14. Choke reactors (on the top) and interface reactors (on the bottom)

6.2. Simulation of Shunt Active Power Filter

The simulation model of shunt active power filter is given in Figure 6.15. There phase IGBT inverter is used as VSC. The DC link capacitor supplies the inverter. The AC source is modeled to include voltage harmonics and unbalances as present in real AC source in the laboratory. By this way, simulation results obtained become much more realistic and fit with experimental results. As an instance, the values of choke and interface reactors are different.

A three phase uncontrolled diode bridge rectifier is used to generate load harmonics. This rectifier is supplied via choke reactors to prevent current overlaps in diodes. The output of this rectifier is a DC voltage and applied to a 45 ohm load.

Three phase IGBT inverter is formed by using three leg three phase configuration. The output of this inverter is voltage pulses and to change these voltage pulses into current, interface reactors are used.

SAPF controller measures source voltages, load and filter currents and DC link voltage to generate the compensation signals. IRPT is used to calculate the current references.

Two phase to phase voltage levels are used to match the simulation and experimental results. While commissioning the SAPF, initially phase to phase voltage level of 220V is used. After getting good results, the phase to phase voltage level is increased to 380V. As a result of this, two cases are investigated.

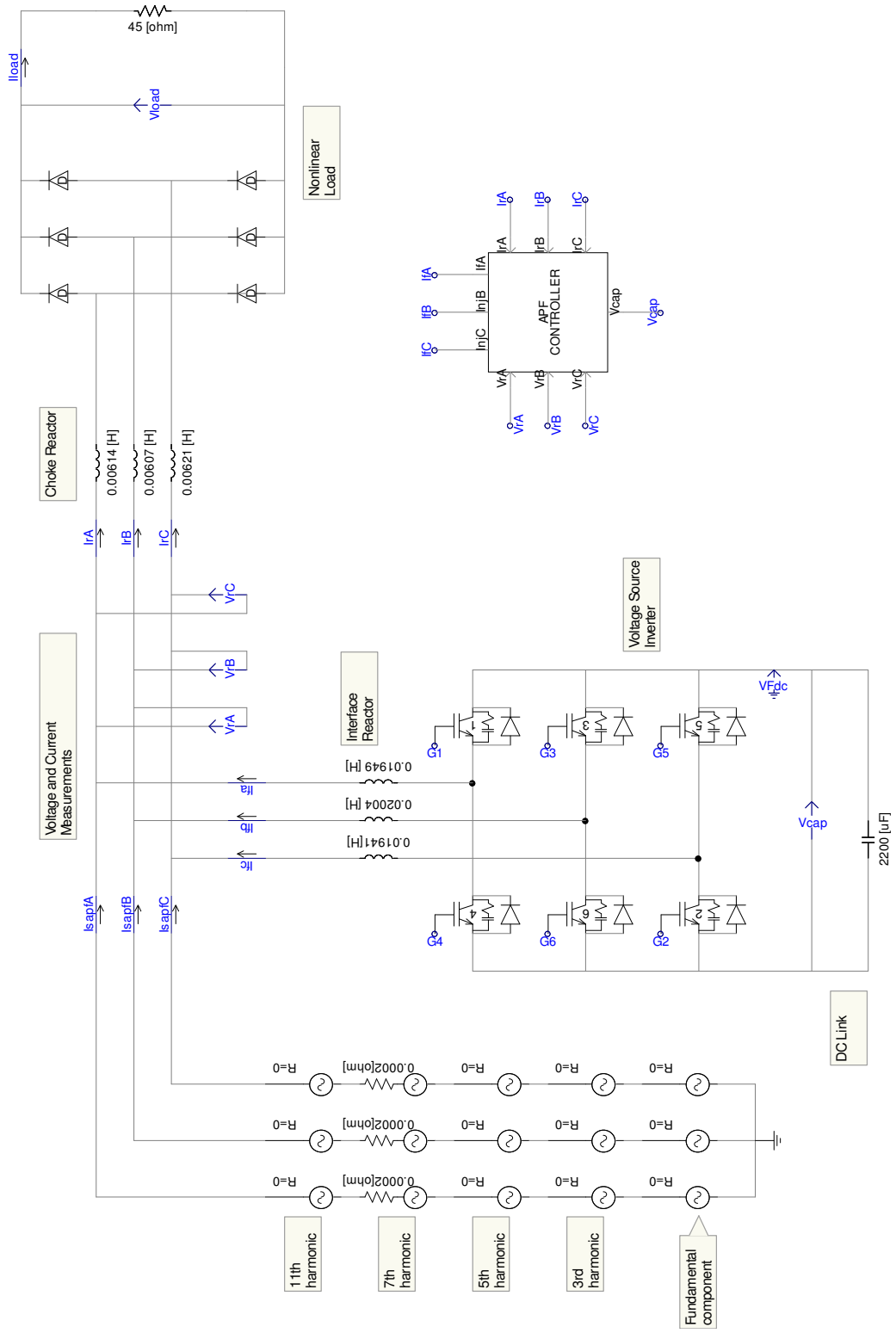

Figure 6.15. Simulation model of SAPF

6.2.1. Case 1: 220V (Line to line) Source Voltage and 45Ω Load

In order to coincide simulation results with the experimental results, the simulation parameters are selected by considering the real values.

The performance of the system is tested for 45Ω resistive load feeding from a 6-pulse diode rectifier. The current waveform of the harmonic polluting load (23.5% THD) is given in Figure 6.16.

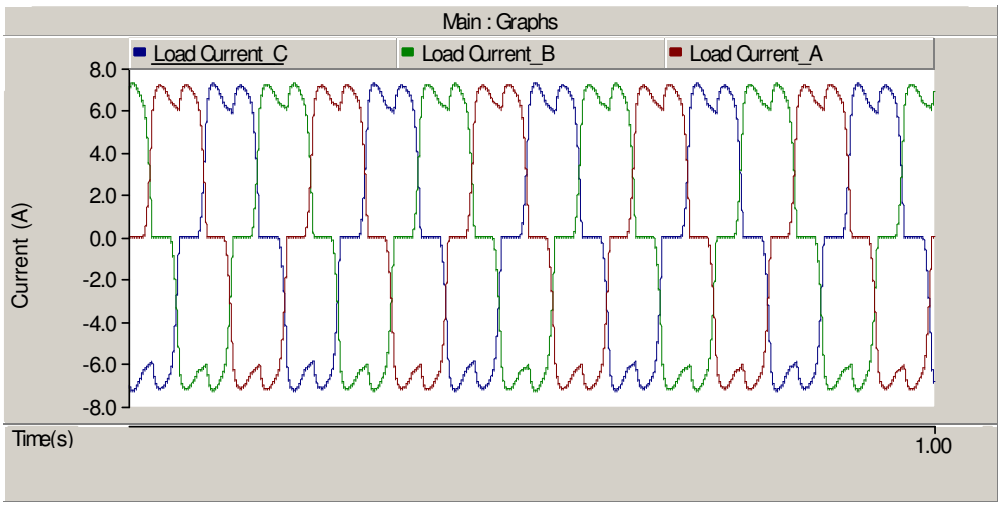

Figure 6.16. The load currents with 23.5% current harmonics for Case 1

The waveforms of load current, injected current and source currents are given in Figure 6.17 after SAPF starts compensation. The load current with 23.5% THD is decreased to 3.9% THD at the source side.

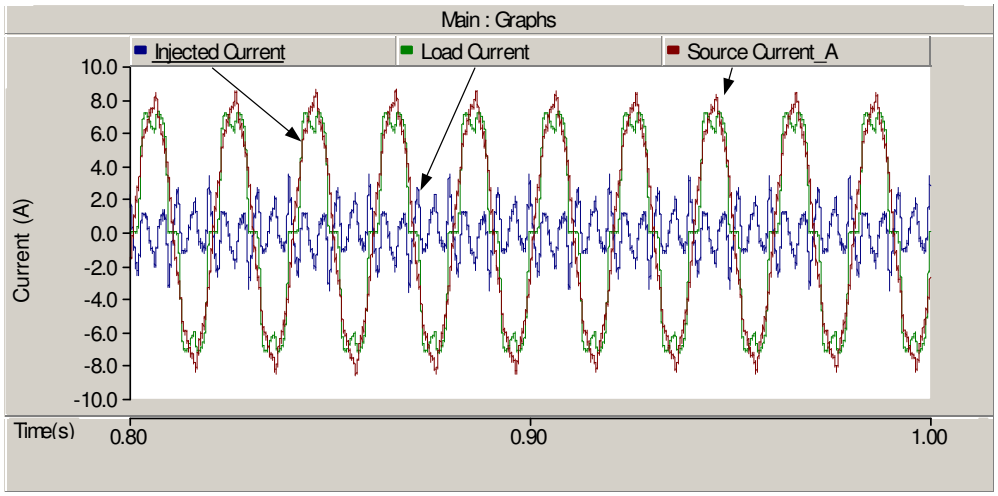

Figure 6.17. Injected, source and load currents Case 1

From Figure 6.17, it can be seen that the harmonics of the load current are eliminated. The new THD of the source current is approximately 3.9%. Figure 6.18 shows the source currents for three phases. Figure 6.19 shows the injected currents.

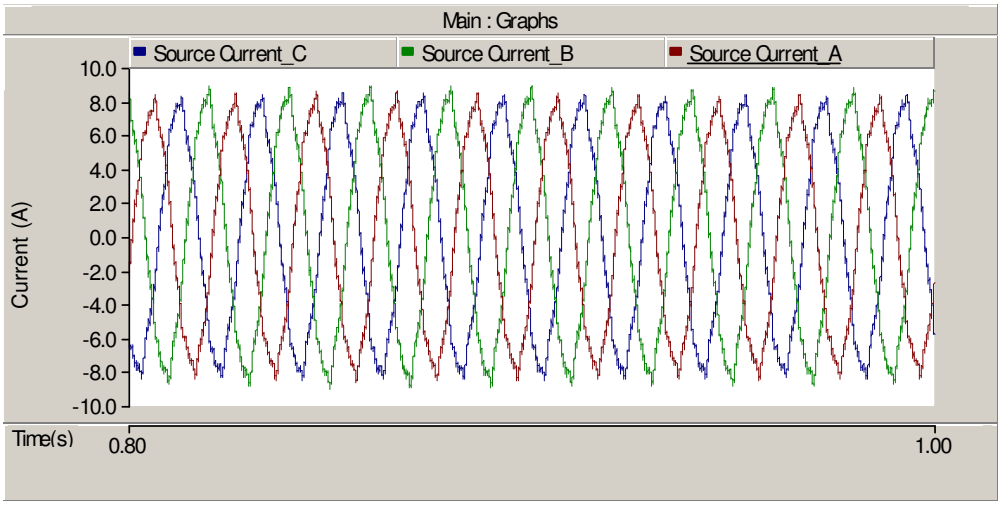

Figure 6.18. Source currents filtered by SAPF for Case 1

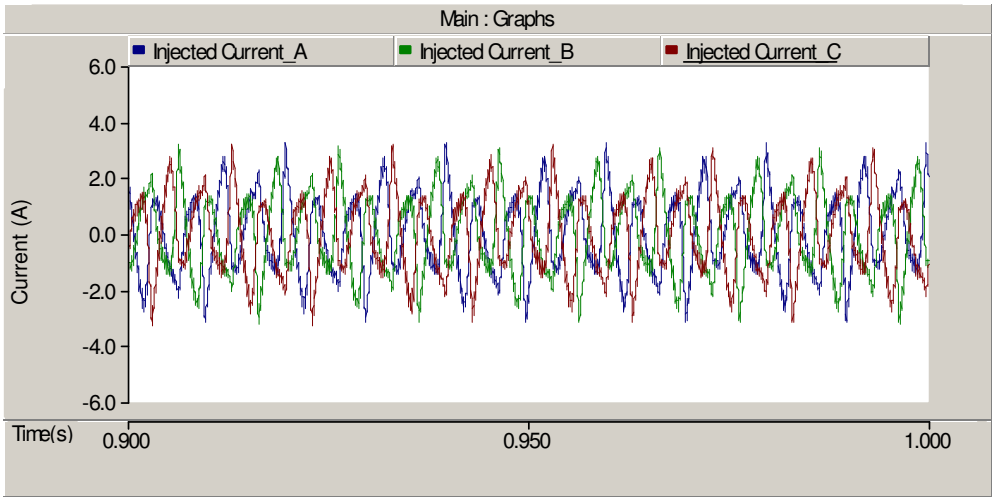

Figure 6.19. Injected filter currents by SAPF for Case 1

6.2.2. Case 2: 380V (Line to line) Source Voltage and 45Ω Load

After the performance test of SAPF at $220V_{rms}$ (line to line), the system voltage is set to 380 V_{rms} (line to line). The current waveform of the harmonic polluting load (23.5% THD) is given in Figure 6.20.

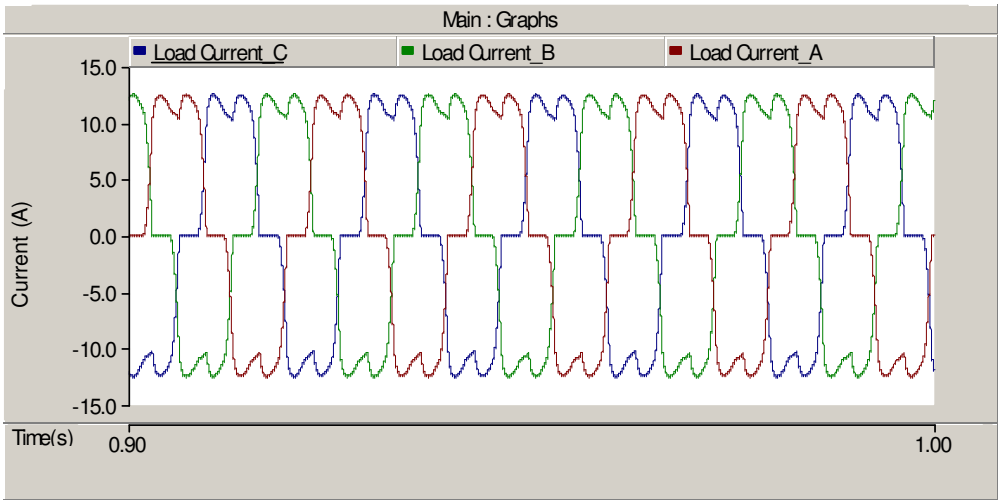

Figure 6.20. The load currents with 23.5% current harmonics for Case 2

The waveforms of load current, injected current and source currents for $380V_{rms}$ (line to line) are given in Figure 6.21. The load current with 23.5% THD is decreased to 4.62% THD at the source side.

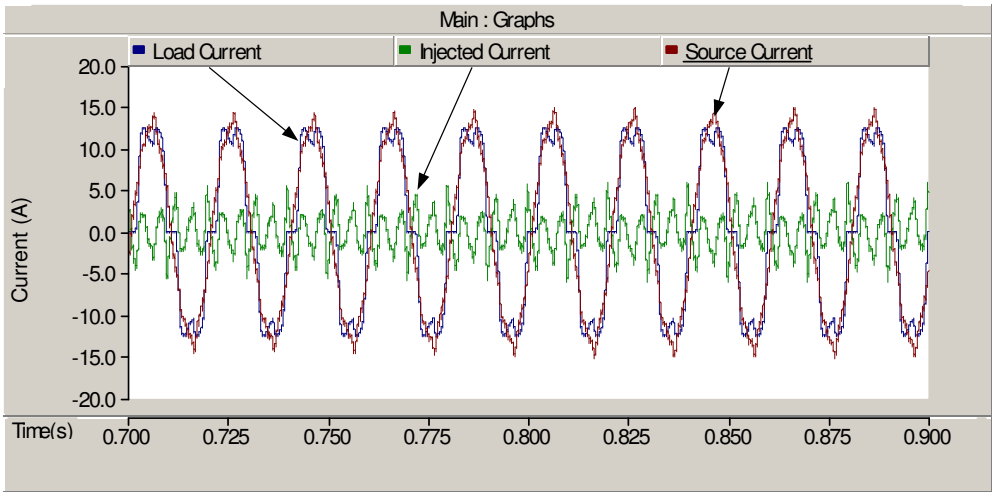

Figure 6.21. Injected, source and load currents for Case 2

Figure 6.22 shows the three phase filtered source currents and Figure 6.23 shows the injected currents.

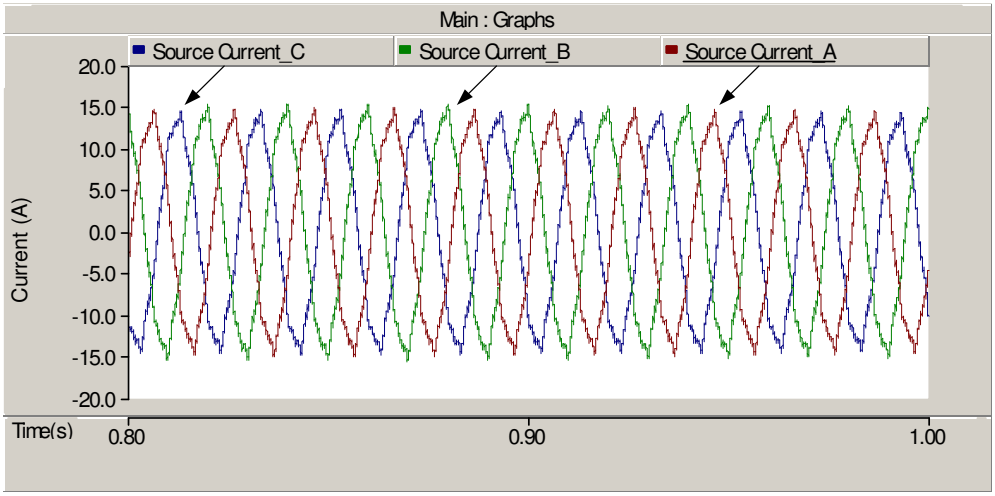

Figure 6.22. Source currents filtered by SAPF for Case 2

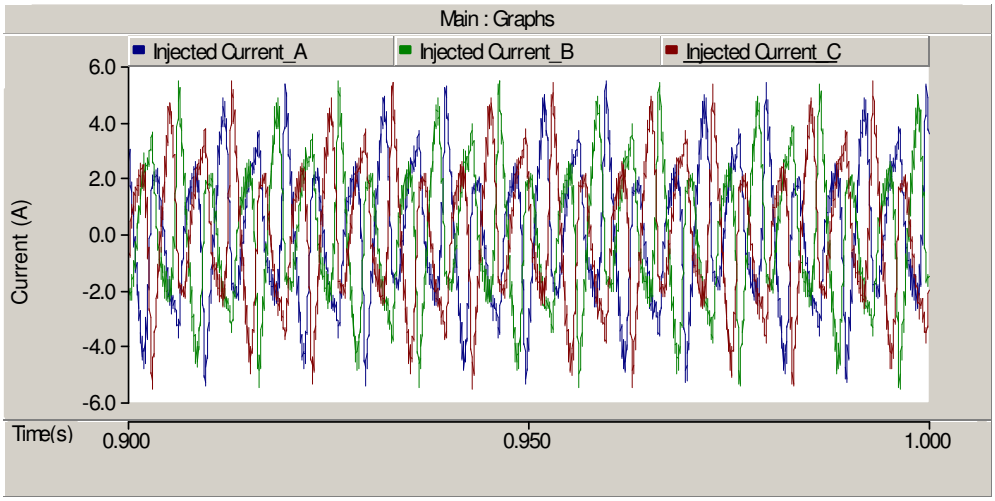

Figure 6.23. Injected filter currents by SAPF for Case 2

6.3. Experimental Results of Shunt Active Power Filter

This section shows the experiment results taken from the setup of SAPF. But initially, measured source and load current for phase A, alpha beta components of voltage and reference currents calculated for A and B phases in DSP controller are given. The source voltage and load current of phase A are shown in Figure 6.24.

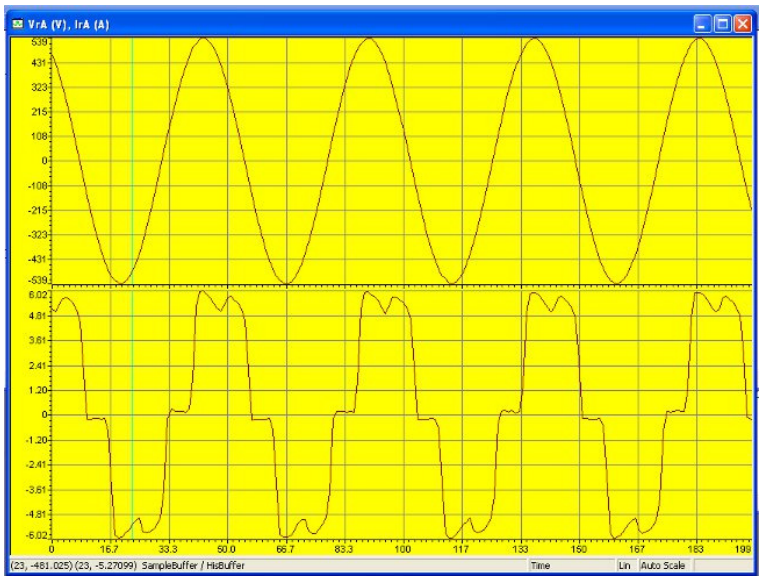

Figure 6.24. Source voltage (top) and load current (bottom) for phase A

Figure 6.25 is the alpha and beta components of source voltage. The beta component is virtually generated in the DSP controller. The calculated reference currents for phases A and B shown in Figure 6.26. These reference current values are used to generate the firing pulses as said before.

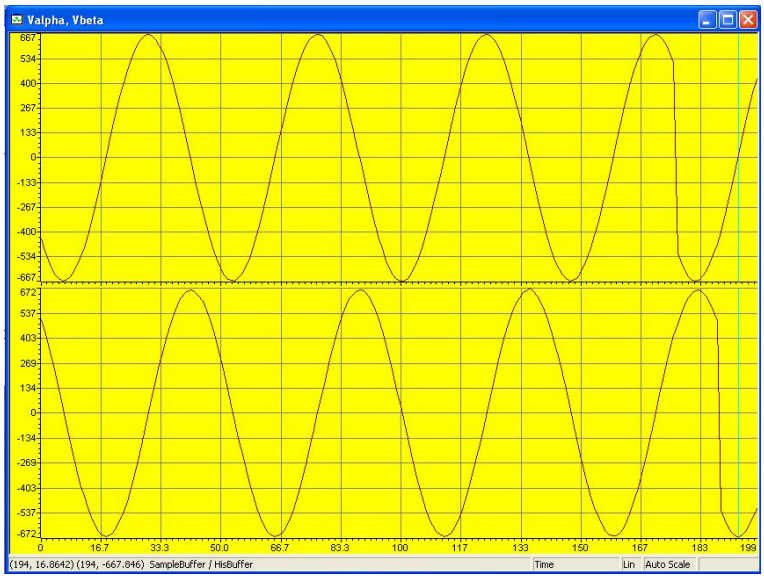

Figure 6.25. Alpha and beta components of source voltage

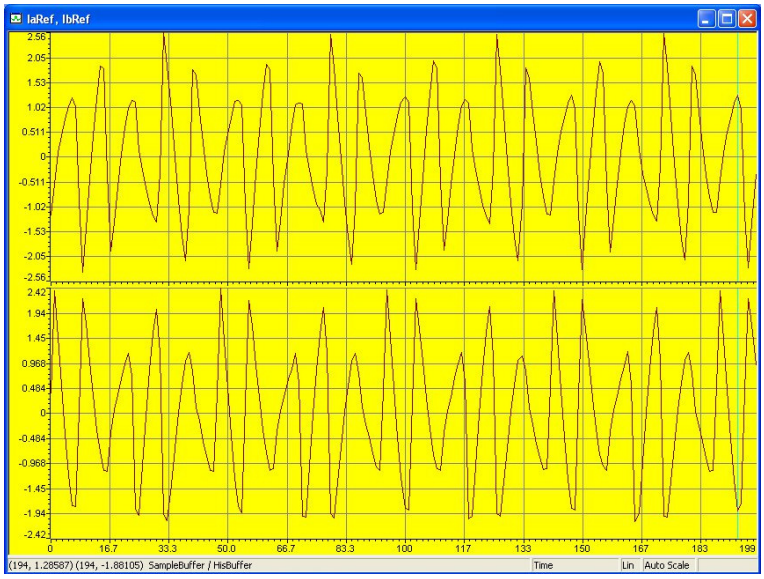

Figure 6.26. Reference currents for phases A and B

6.3.1. Case 1: 220V (Line to line) Source Voltage and 45Ω Load

The experimental performance of the system is tested for 45Ω resistive load feeding from a 6-pulse diode rectifier (23.9% THD). The current waveform of the harmonic polluting load is given in Figure 6.27.

The system voltage is $220V_{rms}$ (line to line). The waveforms of load current, injected current and source currents are given in Figure 6.28. The load current with 23.9% THD is decreased to 4.00% THD at the source side.

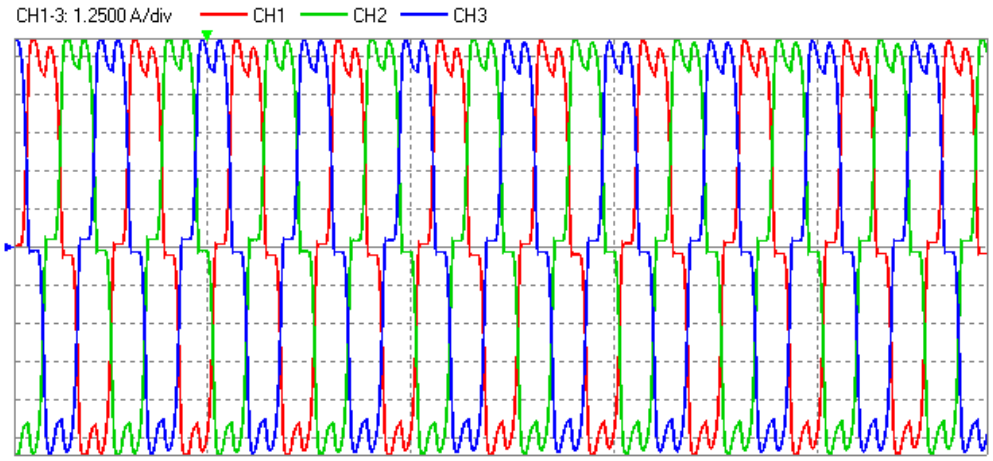

Figure 6.27. The load currents with 23.9% current harmonics for Case 1

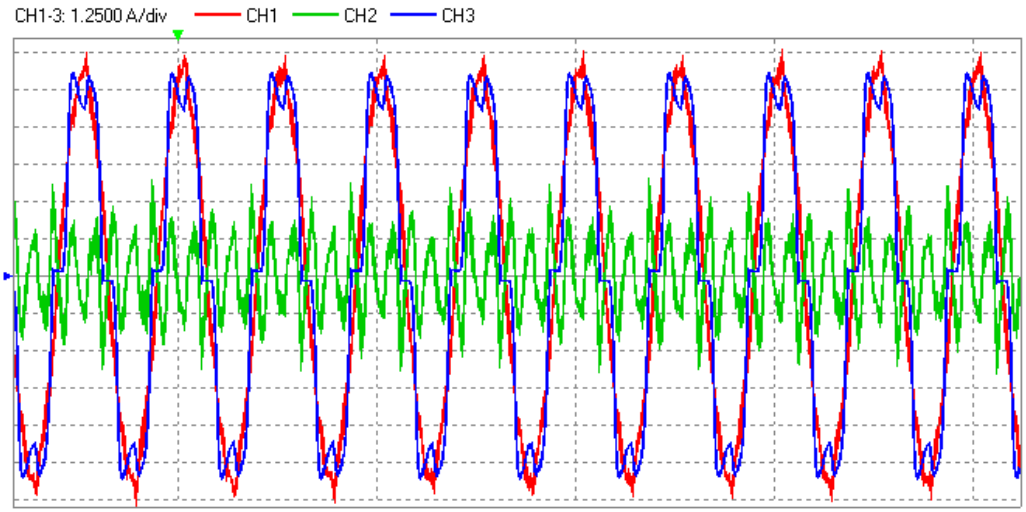

Figure 6.28. Injected, source and load currents for Case 1

Figure 6.29 shows the filtered source currents by SAPF, while Figure 6.30 shows the filter currents. The harmonic content up to 31th harmonic of the filtered current are given in Table 6.2.

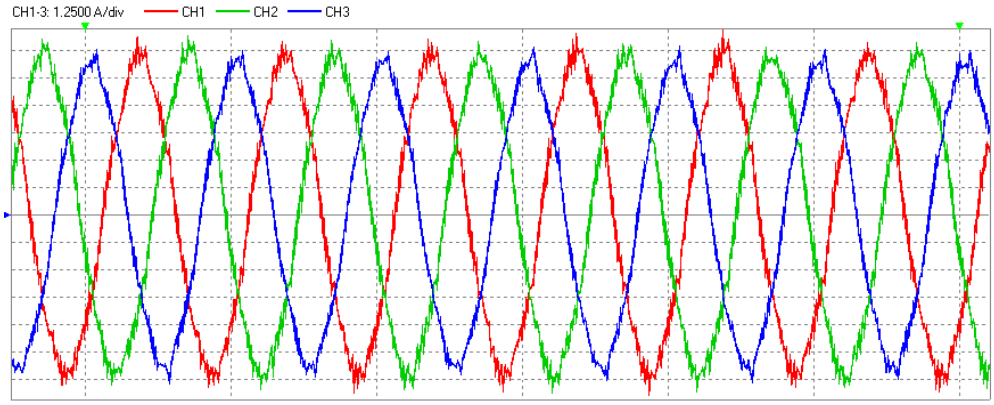

Figure 6.29. Source currents filtered by SAPF for Case 1

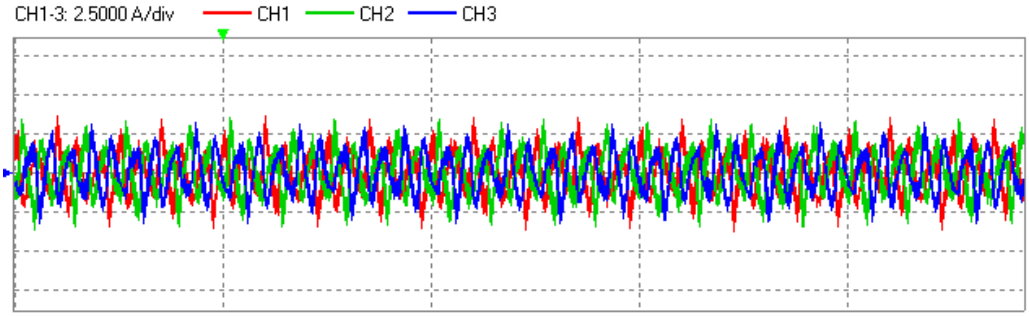

Figure 6.30. Injected filter currents by SAPF for Case 1

Table 6.2 THD content of filtered source currents for Case 1

Order	***(%)***	***Order***	***(%)***	***Order***	***(%)***	***Order***	***(%)***
1	100.00	9	0.14	17	0.91	25	0.52
2	0.32	10	0.21	18	0.24	26	0.19
3	0.41	11	1.41	19	0.73	27	0.35
4	0.22	12	0.18	20	0.14	28	0.27
5	2.62	13	1.13	21	0.25	29	0.22
6	0.23	14	0.18	22	0.21	30	0.24
7	1.62	15	0.15	23	0.39	31	0.56
8	0.26	16	0.12	24	0.23	THD=4.00%	

6.3.2. Case 2: 380V (Line to line) Source Voltage and 45Ω Load

The line-to-line voltages are increased to 380V for this case. The experimental performance of the system is tested for 45Ω resistive load feeding from a 6-pulse diode rectifier (23.9% THD). The current waveform of the harmonic polluting load is given in Figure 6.31.

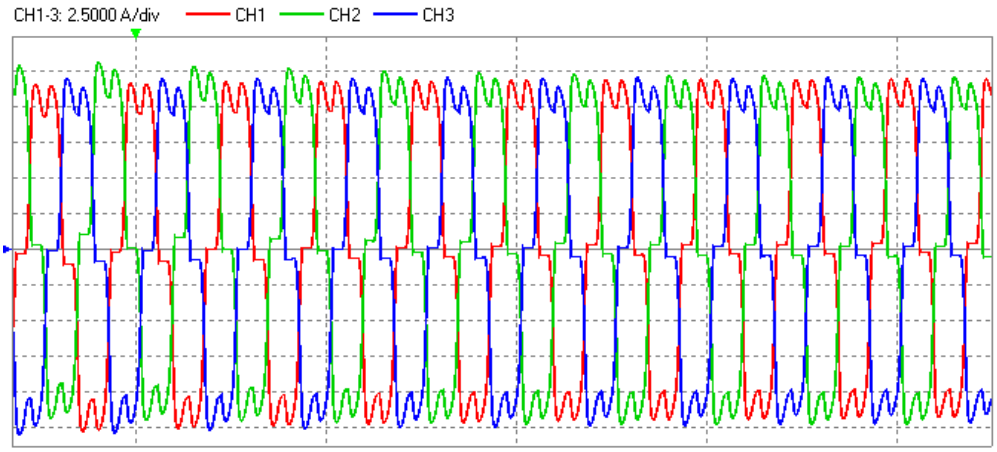

Figure 6.31. The load currents with 23.9% current harmonics for Case 2

The waveforms of load current, injected current and source currents for $380V_{rms}$ (line to line) are given in Figure 6.32. The load current with 23.9% THD is decreased to 4.77% THD at the source side.

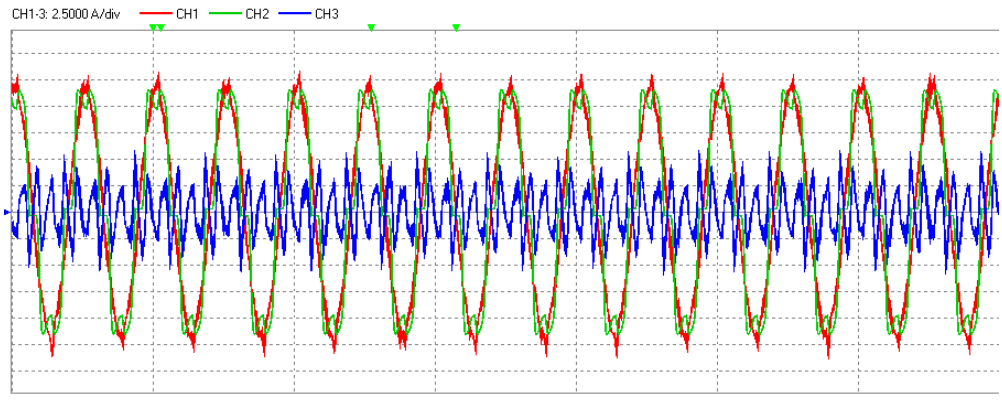

Figure 6.32. Injected, source and load currents for Case 2

Figure 6.33 shows the filtered source currents by SAPF, while Figure 6.34 shows the filter currents. The harmonic content up to 31th harmonic of the filtered current for case 2 are given in Table 6.3.

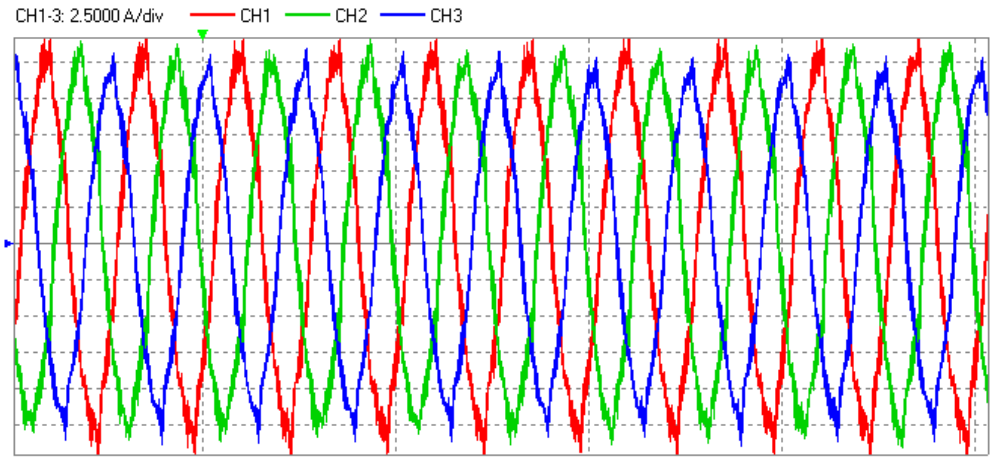

Figure 6.33. Source currents filtered by SAPF for Case 2

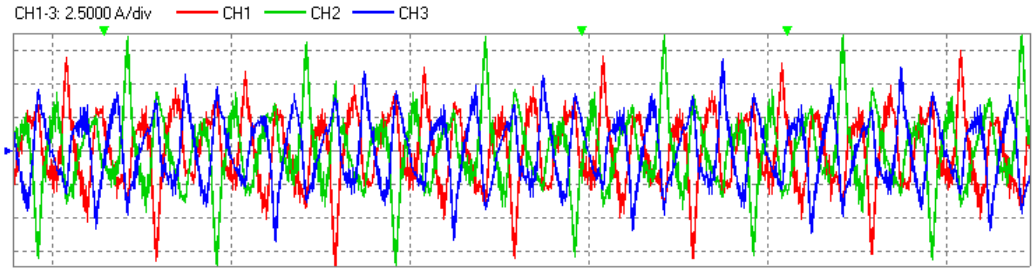

Figure 6.34. Injected filter currents by SAPF for Case 2

Table 6.3 THD content of filtered source currents for Case 2

Order	***(%)***	***Order***	***(%)***	***Order***	***(%)***	***Order***	***(%)***
1	100.00	9	0.70	17	1.05	25	0.40
2	0.44	10	0.39	18	0.14	26	0.36
3	0.44	11	1.84	19	0.71	27	0.20
4	0.51	12	0.25	20	0.28	28	0.27
5	3.19	13	0.75	21	0.50	29	0.60
6	0.33	14	0.24	22	0.33	30	0.28
7	1.62	15	0.56	23	0.85	31	0.35
8	0.42	16	0.24	24	0.23	THD = 4.77%	

The experimental results are taken from the project “Modeling and Implementation of Custom Power Park” which is supported by Scientific and Technological Research Council of Turkey with project number of 106E188. HIOKI 3196 Power Quality Analyzer is used to record the current and voltage waveforms in the case studies.

7. CONCLUSIONS

Mitigation of power quality problems such as voltage sag, interruption and current harmonics has gained significant importance in recent years. The concept of custom power devices that mitigate these power quality problems is introduced recently. Custom power devices are based on power electronics switches to control voltage and current. Most common known types of these devices are Dynamic Voltage Restorer, Static Transfer Switch and Shunt Active Power Filter that are generally controlled by DSPs.

In this thesis, a three phase 3 kVA TMS320F2812 based laboratory prototype DVR is designed and implemented. Three H bridge IGBT inverters are used. DVR quickly senses the voltage sag on the feeder and injects the missing voltage to system thus protects the loads from voltage sag. The algorithms are developed to control DVR in the study. New voltage sag detection and voltage compensation methods based on enhanced phase locked loop are proposed. The power losses are minimized in by controlling the each phase independently. Sinusoidal pulse width modulation techniques are used to generate the switching signals. Case studies which include the single phase 20%, three phase 20% and single phase 40% and three phase 40% voltage sag are performed. The experimental results of rms voltage trends for source and load voltages are given. Four voltage sags are shown in detail for four cases. The results show that the designed DVR quickly responses to the voltage sags and restores the load voltage to the presag value.

TMS320F2812 based STS laboratory prototype of back-to-back connected thyristor pairs rated at 10 kVA quickly senses the voltage sag and/or interruption on the feeder and transfers the load to the healthy feeder. The control flowcharts developed for STS are explained. Make-before-break switching strategy is analytically evaluated. The results taken from experimental setup of STS are given and discussions are made on the results. Enhanced phase locked loop based sag detection is also proposed in the present study which is easy to implement. To show the effectiveness of the proposed method, conventional dq transformation based sag detection is compared with the new method. It is seen that both dq transformation

based sag detection method and PLL based sag detection method have advantages over each other. PLL based method gives more accurate results over conventional model for single phase voltage sags. The results show that the designed STS quickly responses to the voltage sags and interruptions thus it protects the load voltage disturbances.

TMS320F28335 based 5 kVA laboratory prototype of SAPF is developed using three leg three phase IGBT inverter. SAPF extracts the load current harmonics exactly and injects the required compensation current to the system by keeping the THD level of source current at the predefined values determined by IEEE standards. In the implementation of SAPF, it is seen that voltage unbalance and voltage harmonics results in very high harmonic distortion. The compensating signals are extracted using instantaneous reactive power theory and the switching signals of SAPF are generated with hysteresis current control. The voltage harmonics and unbalance affect the performance of the SAPF. To overcome this voltage harmonics and unbalance problems, a low pass filter with a cut off frequency of 50 Hz is used in the voltage measurement for harmonic filtering and a virtual beta component with the same amplitude with alpha component is generated in the DSP for compensation of voltage unbalance. This method eliminates the disadvantages of instantaneous reactive power theory under distorted and unbalanced source voltage conditions.

The experimental design procedure, control flow charts and related C codes to implement the custom power devices are presented in detail and given in the appendix. As these C implementations are easy to understand and could be used in any control applications. These can help the researchers on their custom power based projects. Further research could be carried out in the following areas:

• Implementation of unified power quality conditioner (combination of DVR and SAPF) with different circuit topologies.

• Large scale application of custom power devices.

• Realization of minimum power dissipation methods for DVR, STS and SAPF.

• Performance comparison of available power quality detection and reference signal generation methods experimentally.

• Implementation of custom power devices using FPGA and performance comparison of FPGA versus DSP.

• The investigation of interactions of these devices on the same supply.

• Custom Power Park is a concept that combines DVR, STS and SAPF in a single solution. With the improvements that could be made on these devices, a Custom Power Park may be formed.

REFERENCES

AKAGI, H., NABAE, A., ATOH, S., 1986. Control Strategy of Active Power Filters using Multiple Voltage Source PWM Converters. IEEE Transactions on Industrial Applications, 1A(22):460 - 465.

AKAGI, H., WATANABE, E.H., AREDES, M., 2007. Instantaneous Power Theory and Application to Power Conditioning. John Wiley & Sons, 379p.

AREDES,M., AKAGI,H., WATANABE, E.H., SALGADO, V.E., ENCARNACAO, L.F., 2009. Comparisons Between the p-q and p-q-r Theories in Three Phase Four Wire Systems. IEEE Transactions on Power Electronics, 24(4):924 - 933.

BAGGINI, A., 2008. Handbook of Power Quality. Wiley-IEEE Press, 642p.

BANAEI, M.R., HOSSEINI, S.H., KHAJEE, M.D., 2006. Mitigation of Voltage Sag using Adaptive Neural Network with Dynamic Voltage Restorer. International Power Electronics and Motion Control Conference, 2:1 - 5.

BARROS, J., SILVA, F., 2010. Multilevel Optimal Predictive Dynamic Voltage Restorer. IEEE Transactions on Industrial Electronics, 57(8):2747 - 2760.

BENACHAIBA, C., FERDI, B., 2008. Voltage Quality Improvement using DVR. Electrical Power Quality and Utilisation Journal, 14(1):39 - 46.

BORMANN, F., 2007. Texas Instruments TMS320F2812 Tutorial. Texas Instruments, 474p.

BURKE, J., GRIFFITH, D., WARD D., 1990. Power Quality-Two Different Perspectives. IEEE Transactions on Power Delivery, 5:1501 - 1513.

CHANG, G.W., YEH, C.M., CHEN, W.C., 2006. Meeting IEEE-519 Current Harmonics and Power Factor Constraints with a Three-Phase Three-Wire Active Power Filter under Distorted Source Voltages. IEEE Transactions on Power Delivery, 21(3):1648 - 1654.

CHAPMAN, D., 2001. Power Quality Application Guide, "Harmonics: Causes and Effects". Copper Development Association, 15p.

CHEN, Z., XU, D., 2004. Control and Design Issues of a DSP-Based Shunt Active Power Filter for Utility Interface of Diode Rectifiers. Applied Power Electronics Conference and Exposition, 1:197 - 203.

CHIANG, H.K., LIN, B.R., WU, K.W., 2005. Study of Dynamic Voltage Restorer under the Abnormal Voltage Conditions. International Conference on Power Electronics and Drives Systems, 308 - 312.

CHUNG, Y.H., KIM, H.J., KWON, G.H., PARK, T.B., KIM, S.H., KIM, K.S., CHOE, J.W., 2007. Dynamic Voltage Restorer with Neural Network Controlled Voltage Disturbance Detector and Real-time Digital Voltage Control. IEEE Power Engineering Society General Meeting, 1 - 7.

CIRRINCIONE, M., PUCCI, M., VITALE, G., MIRAOUI, A., 2009. Current Harmonic Compensation by a Single-Phase Shunt Active Power Filter Controlled by Adaptive Neural Filtering. IEEE Transactions on Industrial Electronics, 56(8):3128 - 3143.

COSTA-CASTELLO, R., GRINO, R., CARDONER, R., FOSSAS, E., 2007. High Performance Control of a Single-Phase Shunt Active Filter. IEEE International Symposium on Industrial Electronics, 3350- 3355.

DAHONO, P.A., PURWADI, A., QUAMARUZZAMAN, Q. 1995. An LC Filter Design Method for Single-Phase PWM Inverters. IEEE International Conference on Power Electronics and Drive Systems, 2:571 - 576.

DAI, N.Y., WONG, M.C., FAN, N.G., HAN, Y.D., 2008. A FPGA Based Generalized Pulse Width Modulator for Three Leg Center Split and Four Leg Voltage Source Inverters. IEEE Transactions on Power Electronics, 23(3):1472 - 1484.

DENG, H., ORUGANTI, R., SRINIVASAN, D., 2004. Adaptive Digital Control for UPS Inverter Applications with Compensation of Time Delay. Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 1:450 - 455.

DEVARAJU, T., VEERA V.C., REDDY, M., KUMAR, V., 2010. Modeling and Simulation of Custom Power Devices to Mitigate Power Quality

Problems. International Journal of Engineering Science and Technology, 2(6):1880 - 1885.

DORR, D., PERRY, C., 2003. Custom Power Choices Abound. Transmission and Distribution World.

DUGAN R.C., MCGRANAGHAN, M.F., SANTOSO, S., BEATY, H.W., 2002. Electrical Power Systems Quality. McGraw-Hill Press, 528p.

EL-HABROUK, M., DARWISH, M.K., MEHTA, P., 2000. Active Power Filters: A Review. IEE Electric Power Applications, 147(5):403 - 413.

ERRABELLI, R.R., KOLHATKAR, Y.Y., DAS, S.P., 2006. Experimental Investigation of DVR with Sliding Mode Control. IEEE Power India Conference, 1 - 5.

EZOJI, H., FAZLALI M., GHATRESAMANI A., NOPOUR, M., 2009. A Novel Adaptive Hysteresis Band Voltage Controller for Dynamic Voltage Restorer. European Journal of Scientific Research, 37(2):240 - 253.

FANG, Z., SHING, C.S., KENNETH, S.E.K., TONGXUN, W., ZHAOAN, W., 2004. Study on the Dynamic Voltage Restorer Use in an Isolated Power Supply System. The 4th International Power Electronics and Motion Control Conference, 3:1207 - 1212.

FERNANDES, D.A., NAIDU, S.R., LIMA, A.M.N., 2009. Dynamic Voltage Restorer based on a Four-Leg Voltage Source Converter. IET Generation, Transmission Distribution, 3(5):437 - 447.

FRANTZ, G., 2008. Digital Signal Processor Trends. IEEE Micro, 20(6):52 - 59.

FRATTA, A., GRIFFERO, G., NIEDDU, S., 2004. Comparative Analysis among DSP and FPGA based Control Capabilities in PWM Power Converters. Proceedings of the 30th Annual Conference of the IEEE Industrial Society, 257 - 262.

GODBOLE, R.P., 2008. Design of a Flexible DSP Based Controller Hardware System for Power Electronics Applications. MSc Thesis, North Carolina State University, 86p.

GONZALEZ, M., CARDENAS, V., ALVAREZ, R., 2006. Detection of Sags Swells and Interruptions Using the Digital RMS Method and Kalman Filter with

Fast Response. 32nd Annual Conference on IEEE Industrial Electronics, 2249 - 2254.

GREGORY, D., FITZER, C., BARNES, M., 2002. The Static Transfer Switch Operational Considerations. International Conference on Power Electronics, Machines and Drives, 620 - 625.

GURU, A.K., BALDA, J.C., CARR, K., XIANG, Y.Q., 1998. Design of a Switching Ripple Filter for a Shunt Connected Active Power Filter. Motors & Drives, Fort Smith, 2:1364 - 1368.

HAN, B.M., BAE, B.Y., OVASKA, S.J., 2005. Reference Signal Generator for Active Power Filters using Improved Adaptive Predictive Filter. IEEE Transactions on Industrial Electronics, 52(2):576 - 584.

HENNING, P.H., FUCHS, H.D., LEROUX, A.D., MOUTON, H. 2008. A 1.5-MW Seven-Cell Series-Stacked Converter as an Active Power Filter and Regeneration Converter for a DC Traction Substation. IEEE Transactions on Power Electronics, 23(5):2230 - 2236.

HERRERA, R.S., SALMERON, P., KIM, H., 2008. Instantaneous Reactive Power Theory Applied to Active Power Filter Compensation: Different Approaches, Assessment, and Experimental Results. IEEE Transactions on Industrial Electronics, 55(1):184 - 196.

HEUSTESS, L., 2007. C28x FPU Primer. Texas Instruments, 24p.

HO, C.N., CHUNG, H.S.H., AU, K.T.K., 2008. Design and Implementation of a Fast Dynamic Control Scheme for Capacitor-Supported Dynamic Voltage Restorers. IEEE Transactions on Power Electronics, 23(1):237 - 251.

JIMICHI, T., FUJITA, H., AKAGI, H., 2008. An Approach to Eliminating DC Magnetic Flux from the Series Transformer of a Dynamic Voltage Restorer. IEEE Transactions on Industry Applications, 44(3):809 - 816.

KALE, M., OZDEMIR, E., 2005. Harmonic and Reactive Power Compensation with Shunt Active Power Filter under Non-Ideal Mains Voltage. Electric Power Systems Research, 74(3):363 - 370.

KARIMI, G.M., IRAVANI, M.R., 2002. A Nonlinear Adaptive Filter for Online Signal Analysis in Power Systems. IEEE Transactions on Power Delivery, 17(2):617 - 622.

KHADKIKAR, V., CHANDRA, A., SINGH, B.N., 2009. Generalised Single-Phase P-Q Theory for Active Power Filtering: Simulation and DSP-Based Experimental Investigation. IET Power Electronics, 2(1):67 - 78.

KIM, H., LEE, S.J., SUL, S.K., 2004. A Calculation for the Compensation Voltages in Dynamic Voltage Restorers by Use of PQR Power Theory. Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 1:573 - 579.

KOMATSU, W., GIARETTA, A.R., OLIVEIRA, M.A., MONTEIRO, T.C., GALASSI, M., AHN, S.U., MATAKAS, L., BORMIO, E., CAMARGO, J., JARDINI, J.A., 2008. Micro-DVR - A Development Platform for DVR and FACDS. Transmission and Distribution Conference and Exposition, 1 - 7.

KUMAR S.J., AGARWAL, P., 2003. Design Simulation and Experimental Investigations, on a Shunt Active Power Filter for Harmonics, and Reactive Power Compensation. Electric Power Components and Systems, 31(7):671 - 692.

LI, H., ZHUO, F., WANG, Z., LEI, W., WU, L., 2005. A novel time-domain current-detection algorithm for shunt active power filters. IEEE Transactions on Power Systems, 20(2):644 - 651.

LI, Y.W., BLAABJERG, F., VILATHGAMUWA, D.M., LOH, P.C., 2007. Design and Comparison of High Performance Stationary-Frame Controllers for DVR Implementation. IEEE Transactions on Power Electronics, 22(2):602 - 612.

LI, Y.W., VILATHGAMUWA, D.M., BLAABJERG, F., LOH, P.C., 2007. A Robust Control Scheme for Medium Voltage Level DVR Implementation. IEEE Transactions on Industrial Electronics, 54(4):2249 - 2261.

LIN, T., DOMIJAN, A., 2006. Real Time Measurement of Power Disturbances Part 1. Survey and a Novel Complex Filter Approach. Electric Power Systems Research, 76:1027 - 1032.

MAHMOOD, T., CHOUDHRY, M.A., 2006a. Reconfiguration of Feeders Using Static Transfer Switch. International Conference on Emerging Technologies, 385 - 390.

MAHMOOD, T., CHOUDHRY, M.A., 2006b. Application of Static Transfer Switch for Feeder Reconfiguration to Improve Voltage at Critical Locations. Transmission and Distribution Conference and Exposition, 1 - 6.

MAREI, M.I., 2004. Novel Control Algorithms for Inverter based Custom Power Conditioners. PhD Thesis, University of Waterloo, 185p.

MCGRANAGHAN, M.F., ROETTGER, W.C., 2003. The Economics of Custom Power. IEEE PES Transmission and Distribution Conference and Exposition, 3: 944 - 948.

MOKHTARI, H., DEWAN, S.B., IRAVANI, M.R., 2001. Effect of Regenerative Load on a Static Transfer Switch Performance. IEEE Transactions on Power Delivery, 16(4):619 - 624.

MOKHTARI, H., DEWAN, S.B., IRAVANI, M.R., 2002. Analysis of a Static Transfer Switch with Respect to Transfer Time. IEEE Transactions on Power Delivery, 17(1):190 - 199.

MOKHTARI, H., DEWAN, S.B., IRAVANI, M.R., 2000. Performance Evaluation of Thyristor based Static Transfer Switch. IEEE Transactions on Power Delivery, 15(3):960 - 966.

MOKHTARI, H., IRAVANI, M.R., 2007. Effect of Source Phase Difference on Static Transfer Switch Performance. IEEE Transactions on Power Delivery, 22(2):1125 - 1131.

MORAN, L., DIAZ, M., HIGUERA, V., WALLACE, R., DIXON, J., 1992. A Three Phase Active Power Filter Operating with Fixed Switching Frequency for Reactive Power and Current Harmonic Compensation. International Conference on Power Electronics and Motion Control, 1:362 - 367.

MOSCHAKIS, M.N., HATZIARGYRIOU, N.D., 2003. A Detailed Model for a Thyristor based Static Transfer Switch. IEEE Transactions on Power Delivery, 18(4):1442 - 1449.

PETIT, J.F., ROBLES, G., AMARIS, H., 2007. Current Reference Control for Shunt Active Power Filters under Nonsinusoidal Voltage Conditions. IEEE Transactions on Power Delivery, 22(4):2254 - 2261.

POPOOLA, O., JIMOH, A., NICOLAE, D., 2007. On-Line Remote and Automatic Switching of Consumers Connection for Optimal Performance of a Distribution Feeder. AFRICON, 1 - 6.

RADZI, M.A.M., RAHIM, N.A., 2009. Neural Network and Bandless Hysteresis Approach to Control Switched Capacitor Active Power Filter for Reduction of Harmonics. IEEE Transactions on Industrial Electronics, 56(5):1477 - 1485.

RAHIMI, K., PAKDEL, M., YOUSEFI, M.R., 2009. Neuron Adaptive Control of a Shunt Active Power Filter and Its Realization of Analog Circuit. IEEE EUROCON, 272 - 277.

RAHMANI, S., HAMADI, A., MENDALEK, N., AL-HADDAD, K., 2009. A New Control Technique for Three-Phase Shunt Hybrid Power Filter. IEEE Transactions on Industrial Electronics, 8:2904 - 2915.

RAMASAMY, A.K., KRISHNAN IYER, R., RAMACHANDARAMUTHY, V.K., MUKERJEE, R.N., 2005. Dynamic Voltage Restorer for Voltage Sag Compensation. International Conference on Power Electronics and Drives Systems, 1289 - 1294.

RAMOS-CARRANZA, H.A., MEDINA, A., CHANG, G.W., 2008. Real-Time Shunt Active Power Filter Compensation. IEEE Transactions on Power Delivery, 23(4):2623 - 2625.

ROUTIMO, M., SALO, M., TUUSA, H., 2007. Comparison of Voltage-Source and Current-Source Shunt Active Power Filters. IEEE Transactions on Power Electronics, 22(2):636 - 643.

SABIN, D.D., SANNINO, A., 2003. A Summary of the Draft IEEE P1409 Custom Power Application Guide. IEEE PES Transmission and Distribution Conference and Exposition, 3: 931 - 936.

SANKARAN, C., 2002. Power Quality. CRC Press, 202p.

SANNINO, A., 2001. Static Transfer Switch: Analysis of Switching Conditions and Actual Transfer Time. IEEE Power Engineering Society Winter Meeting, 1:120 - 125.

SCHWARTZENBERG, J.W., DE DONCKER, R.W., 1995. 15 kV Medium Voltage Static Transfer Switch. Industrial Applications Conference,3:2515 - 2520.

SEMIKRON CORPORATION, 2008. SKHI 21A, SKHI 22A/B Datasheet. 12p.

SHI, W., TANG, G., 2008. Study of Double Feedforward Controller for Dynamic Voltage Restorer. Third International Conference on Electric Utility Deregulation and Restructuring and Power Technologies, 1906 – 1910.

SPECTRUM DIGITAL, 2003. ezDSP F2812 Technical Reference. 46p.

TAYLOR, G.A., 1995. Power Quality Hardware Solutions for Distribution Systems: Custom Power. IEE North Eastern Centre Power Section Symposium on Security and Power Quality of Distribution Systems, 11:1-9.

TEXAS INSTRUMENTS, 2008. Digital Signal Processing Selection Guide. Texas Instruments, 101p.

_____, 2010a. TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 Digital Signal Processors, Data Manual. Texas Instruments, 170p.

_____, 2009a. TMS320C28 MCU Workshop, Workshop Guide and Lab Manual. Texas Instruments, 400p.

_____, 2010b. TMS320F28335, TMS320F28334, TMS320F28332, TMS320-F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers, Data Manual. Texas Instruments, 197p.

_____, 2009b. TMS320x2833x, 2823x Enhanced Pulse Width Modulator (ePWM) Module, Reference Manual. Texas Instruments,122p.

THIRUMOORTHI, P., SURENDAR, V., YADAIAH, N., 2009. Digital Control of Active Power Line Conditioner based on Instantaneous Reactive Power

Theory. International Conference on Control, Automation, Communication and Energy Conservation, 1 - 6.

UCAK, O., 2009. Design and Implementation of Voltage Source Converter based Hybrid Active Power Filter. MSc Thesis, Middle East Technical University, 158p.

UYYURU, K.R., MISHRA, M.K., GHOSH, A., 2009. An Optimization-Based Algorithm for Shunt Active Filter under Distorted Supply Voltages. IEEE Transactions on Power Electronics, 24(5):1223 - 1232.

WANG, B., VENKATARAMANAN, G., 2005. Operation and Control of a Dynamic Voltage Restorer Realized Using Cascaded H-Bridge Converters. IEEE Power Electronics Specialists Conference, 2222 - 2229.

WEI, P., CHEN, H., ZHAN, Z., 2009. Three-Phrase Active Power Filter Based on DSP for Power Distribution Systems. Power and Energy Engineering Conference, 1 - 5.

WEI, X., ZHAO, K., SHUANG, K., 2009. Current Control Strategy Research for Active Power Filter. IEEE EUROCON, 1513 - 1520.

ZHAN, C., FITZER, C., RAMACHANDARAMURTHY, V.K., ARULAMPALAM, A., BARNES, M., JENKINS, N., 2001. Software Phase-Locked Loop Applied to Dynamic Voltage Restorer (DVR). IEEE Power Engineering Society Winter Meeting, 3:1033 - 1038.

ZHANG, D., 2006. A Stochastic Approach to Digital Control Design and Implementation in Power Electronics. PhD Thesis, The Florida State University, College of Engineering, 142p.

ZHAO, Y., 2008. Design and Implementation of Inverter in Dynamic Voltage Restorer based on Selective Harmonic Elimination PWM. Third International Conference on Electric Utility Deregulation and Restructuring and Power Technologies, 2239 - 2244.

ZHOU, H., ZHOU, J., QI, Z.P., 2008. Fast Voltage Detection for a Single-Phase Dynamic Voltage Restorer (DVR) using Morphological Low-Pass Filters. Third International Conference on Electric Utility Deregulation and Restructuring and Power Technologies, 2042 - 2046.

CIRRICULUM VITAE

Mehmet Uğraş CUMA was born in 1982. He received his BSc and MSc degrees in Electrical and Electronics Engineering from Çukurova University in 2004 and 2006, respectively. His research interests are power quality, power quality devices and microcontroller applications. He is a member of Turkish Chamber of Electrical Engineers. He has worked in several research projects supported by Scientific and Technological Council of Turkey. He is married and has a one child.

Table A.1 Basic features of TMS320F2812 (Texas Instruments, 2010a)

Feature	Value
Generation	28x fixed point series
Central Processing Unit	C28x core
Floating Point Unit	None
Operating Frequency	150 MHz
Random Access Memory	36 KB
On Time Programmable Read Only Memory	2 KB
Flash Memory	256 KB
External Memory Interface	16 bit single interface
Number of Pulse Width Modulation Channels	16 channels
Number of Capture Channels	6 channels
Number of Quadrature Encoder Pulse Channels	2 channels
Analog to Digital Converter	16 channel,12 bits
Analog to Digital Conversion Time	80 nano seconds
Number of Multi Channel Buffered Serial Ports	1
Number of Universal Asynchronous Receiver/Transmitters	2
Number of Serial Peripheral Interface	1
Number of Controller Area Network Peripheral	1
Timers	3x 32 bit, 1 Watchdog
Number of General Purpose Input Outputs	56

Table A.2 Basic features of TMS320F28335 (Texas Instruments, 2010b)

Feature	Value
Generation	28x fixed point series
Central Processing Unit	C28x core
Floating Point Unit	Yes
Operating Frequency	150 MHz
Random Access Memory	68 KB
On Time Programmable Read Only Memory	2 KB
Flash Memory	512 KB
External Memory Interface	32/16 bit interface
Number of Pulse Width Modulation Channels	18 channels
Number of Capture Channels	6 channels
Number of Quadrature Encoder Pulse Channels	2 channels
Analog to Digital Converter	16 channel,12 bits
Analog to Digital Conversion Time	80 nano seconds
Number of Multi Channel Buffered Serial Ports	2
Number of Universal Asynchronous Receiver/Transmitters	3
Number of Serial Peripheral Interface	1
Number of Controller Area Network Peripheral	2
Timers	3x 32 bit, 1 Watchdog
Number of General Purpose Input Outputs	88

Listing B.1. C Implementation of Dynamic Voltage Restorer

```
#include "DSP281x_Device.h"
#include "IQmathLib.h"
#include "fuzzy.h"
#include "dlog4ch.h"
#include "f281xadc04b.h"

interrupt void CpuTimerIsr(void);

//MODEL FUNCTION PROTOTYPES (Beginning)

void ThetaSph(_iq);
void Theta(_iq,_iq,_iq);
void Theta2(_iq);
void Theta3(_iq);

void SagDetection();
_iq Detect();
_iq PqrDetect();
_iq SecOrderFilter(_iq);
_iq HysteresisA(_iq);
_iq HysteresisB(_iq);
_iq HysteresisC(_iq);

void Filtering(_iq,_iq,_iq);
int Not(int);
int Or(int,int,int);

//MODEL FUNCTION PROTOTYPES (End)

// AUXILIARY VARIABLES (Beginning)

long int_count = 0;
int flag = 0;
int sn = 0,sp = 0;

_iq sag = _IQ(0), sagA =_IQ(0), sagB =_IQ(0), sagC =_IQ(0);
_iq dx,tmpx =_IQ(0), filtered = _IQ(0);

int16 DlogCh1=0, DlogCh2=0, DlogCh3=0, DlogCh4=0;

int flgA1 = 0, flgA2 = 0, flgA3 = 0;
int xA1 = 0, xA2 = 0, xA3 = 0;

int flgB1 = 0, flgB2 = 0, flgB3 = 0;
int xB1 = 0, xB2 = 0, xB3 = 0;
int flgC1 = 0, int flgC2 = 0, int flgC3 = 0;
int xC1 = 0, int xC2 = 0, int xC3 = 0;

// AUXILIARY VARIABLES (End)

//PLL VARIABLES (Beginning)

_iq y1 = _IQ(0), y2 = _IQ(0), y3 = _IQ(0);
_iq A1 = _IQ(0), A2 = _IQ(0), A3 = _IQ(0);
```

```
_iq Ts    = _IQ(0.00002);
_iq K     = _IQ(340);
_iq Kp    = _IQ(20);
_iq Kv    = _IQ(25);

_iq intg1 = _IQ(0),intg2 = _IQ(0), intg3 = _IQ(0);
_iq phi1 = _IQ(0), phi2 = _IQ(0), phi3  = _IQ(0);

_iq swt901 = _IQ(0), swt902 = _IQ(0), swt903 = _IQ(0);
_iq swt   = _IQ(0), swte  = _IQ(0), swta  = _IQ(0);
_iq cwt   = _IQ(0), cwte  = _IQ(0), cwta  = _IQ(0);
_iq w0    = _IQ(W);

//PLL VARIABLES (End)

//GLOBAL VARIABLES (Beginning)

_iq Va = _IQ(0), Vb = _IQ(0), Vc = _IQ(0);
_iq Vs = _IQ(0), Vsf = _IQ(0);

_iq Vd = _IQ(0), Vq = _IQ(0), Vq_ = _IQ(0);
_iq dVq   = _IQ(0), Vqis  = _IQ(0);

_iq Valp = _IQ(0), Vbta = _IQ(0), V0 = _IQ(0);
_iq VAerr = _IQ(0), VBerr = _IQ(0), VCerr = _IQ(0);

//GLOBAL VARIABLES (End)

//FILTER VARIABLES (Beginning)

_iq x[2]={_IQ(0),_IQ(0)};
_iq xn[2]={_IQ(0),_IQ(0)};

_iq xVa[2]={_IQ(0),_IQ(0)};
_iq xnVa[2]={_IQ(0),_IQ(0)};

_iq xVb[2]={_IQ(0),_IQ(0)};
_iq xnVb[2]={_IQ(0),_IQ(0)};

_iq xVc[2]={_IQ(0),_IQ(0)};
_iq xnVc[2]={_IQ(0),_IQ(0)};

//FILTER VARIABLES (End)

PWMGEN pwm1 = PWMGEN_DEFAULTS;
DLOG_4CH dlog = DLOG_4CH_DEFAULTS;
ADCVALSB adc1 = ADCVALSB_DEFAULTS;

void main(void)
{

      InitSysCtrl();
      DINT;
      IER = 0x0000;
      IFR = 0x0000;
```

```
	InitPieCtrl();

	InitPieVectTable();

	EvaRegs.GPTCONA.all=0;
	EvbRegs.GPTCONB.all=0;

	EvaRegs.EVAIMRA.bit.T1UFINT=1;
	EvaRegs.EVAIFRA.bit.T1UFINT=1;

	EvbRegs.EVBIMRA.bit.T3UFINT=1;
	EvbRegs.EVBIFRA.bit.T3UFINT=1;

	EALLOW;
	PieVectTable.TINT0 = &CpuTimerIsr;
	EDIS;

	InitCpuTimers();

	ConfigCpuTimer(&CpuTimer0, 150, 20);

	PieCtrlRegs.PIEIER1.bit.INTx7=1;
	IER = M_INT1;

	EINT;
	ERTM;

	pwm1.PeriodMax=3750;
	pwm1.init(&pwm1);

	dlog.iptr1=&DlogCh1;
	dlog.iptr2=&DlogCh2;
	dlog.iptr3=&DlogCh3;
	dlog.iptr4=&DlogCh4;

	dlog.trig_value=0x0;
	dlog.size=0x400;
	dlog.prescalar=12;
	dlog.init(&dlog);

	adc1.ChSelect=0x3210;
	adc1.init(&adc1);
	CpuTimer0Regs.TCR.bit.TSS = 0;

	while(1)
		{
		//ENDLESS LOOP
		}
}


interrupt void CpuTimerIsr(void)
{

	int_count++;
```

```
      adc1.read(&adc1);

      Va = _IQ15toIQ(_IQmpy(_IQ(1.25),adc1.Ch3Out));
      Vb = _IQ15toIQ(_IQmpy(_IQ(1.25),adc1.Ch2Out));
      Vc = _IQ15toIQ(_IQmpy(_IQ(1.25),adc1.Ch1Out));

      Theta(Va,Vb,Vc);
      Filtering(Va,Vb,Vc);

/* //PQR DETECTION

sag = PqrDetect();

if(sag){

VAerr = swt - _IQmpy(y1,_IQ(0.9));
VBerr = swte - _IQmpy(y2,_IQ(0.9));
VCerr = swta - _IQmpy(y3,_IQ(0.9));

pwm1.MfuncC1 = _IQsat(_IQmpy(VAerr,_IQ(2)),_IQ(1),_IQ(-1));
pwm1.MfuncC2 = _IQsat(_IQmpy(VBerr,_IQ(2)),_IQ(1),_IQ(-1));
pwm1.MfuncC3 = _IQsat(_IQmpy(VCerr,_IQ(2)),_IQ(1),_IQ(-1)); }
else  {
      VAerr = _IQ(0); VBerr = _IQ(0); VCerr = _IQ(0);
      pwm1.MfuncC1 = _IQ(-10);}

pwm1.update(&pwm1);

// PQR DETECTION (End) */

//PLL DETECTION (Beginning)

SagDetection();

if (sagA){
VAerr = swt - _IQmpy(y1,_IQ(0.91));
pwm1.MfuncC1 = _IQsat(_IQmpy(VAerr,_IQ(2)),_IQ(1),_IQ(-1));}
else { VAerr = _IQ(0);
pwm1.MfuncC1 = _IQ(-5);}

if (sagB) {
VBerr = swte - _IQmpy(y2,_IQ(0.91));
pwm1.MfuncC2 = _IQsat(_IQmpy(VBerr,_IQ(2)),_IQ(1),_IQ(-1));}
else  { VBerr = _IQ(0);
pwm1.MfuncC2 = _IQ(-5);}

if (sagC) {
VCerr = swta - _IQmpy(y3,_IQ(0.91));
pwm1.MfuncC3 = _IQsat(_IQmpy(VCerr,_IQ(2)),_IQ(1),_IQ(-1));}
else  { VCerr = _IQ(0);
pwm1.MfuncC3 = _IQ(-5);}

pwm1.update(&pwm1);

// PLL DETECTION (End)
```

```
      //MEASUREMENT CODE SEGMENT (Beginning)

      DlogCh1 =(int16)(long)adc1.Ch1Out;
      DlogCh2 =(int16)_IQtoIQ15(_IQmpy(_IQ(0.5),VCerr));
      DlogCh3 =(int16)_IQtoIQ15(_IQmpy(_IQ(0.5),Vc));
      DlogCh4 =(int16)_IQtoIQ15(_IQmpy(_IQ(0.5),VCerr));
      dlog.update(&dlog);

      //MEASUREMENT CODE SEGMENT (End)

      EvaRegs.EVAIMRA.bit.T1UFINT = 1;
      EvaRegs.EVAIFRA.all = BIT9;
      EvbRegs.EVBIMRA.bit.T3UFINT=1;
      EvbRegs.EVBIFRA.all = BIT9;

      PieCtrlRegs.PIEACK.all |= PIEACK_GROUP1;

}

void Filtering(_iq fVa,_iq fVb,_iq fVc) {

      xnVa[0] = _IQmpy(xVa[0],_IQ(0.712962789476025))
            +_IQmpy(xVa[1],_IQ(-828.406989209829))
            +_IQmpy(fVa,_IQ(0.856481394738012));

      xnVa[1] = _IQmpy(xVa[0],_IQ(0.000042824069736))
            +_IQmpy(xVa[1],_IQ(0.979289825269754))
            +_IQmpy(fVa,_IQ(0.000021412034868));

      xVa[0]  = xnVa[0];
      xVa[1]  = xnVa[1];

      Va     = _IQmpy(xVa[0],_IQ(0.0207101747302457))
            +_IQmpy(xVa[1],_IQ(957.205570955174))
            +_IQmpy(fVa,_IQ(0.0103550873651229));


      xnVb[0] = _IQmpy(xVb[0],_IQ(0.712962789476025))
            +_IQmpy(xVb[1],_IQ(-828.406989209829))
            +_IQmpy(fVb,_IQ(0.856481394738012));

      xnVb[1] = _IQmpy(xVb[0],_IQ(0.000042824069736))
            +_IQmpy(xVb[1],_IQ(0.979289825269754))
            +_IQmpy(fVb,_IQ(0.000021412034868));

      xVb[0]  = xnVb[0];
      xVb[1]  = xnVb[1];

      Vb     = _IQmpy(xVb[0],_IQ(0.0207101747302457))
            +_IQmpy(xVb[1],_IQ(957.205570955174))
            +_IQmpy(fVb,_IQ(0.0103550873651229));

      xnVc[0] = _IQmpy(xVc[0],_IQ(0.712962789476025))
            +_IQmpy(xVc[1],_IQ(-828.406989209829))
            +_IQmpy(fVc,_IQ(0.856481394738012));
```

```
      xnVc[1] = _IQmpy(xVc[0],_IQ(0.000042824069736))
            +_IQmpy(xVc[1],_IQ(0.979289825269754))
            +_IQmpy(fVc,_IQ(0.000021412034868));

      xVc[0]  = xnVc[0];
      xVc[1]  = xnVc[1];

      Vc     = _IQmpy(xVc[0],_IQ(0.0207101747302457))
            +_IQmpy(xVc[1],_IQ(957.205570955174))
            +_IQmpy(fVc,_IQ(0.0103550873651229));
}

_iq PqrDetect() {

      Vd  = _IQmpy(_IQmpy(Va,swt)+_IQmpy(Vb,swte)
            +_IQmpy(Vc,swta),_IQ(0.666667));
      Vq  = _IQmpy(_IQmpy(Va,cwt)+_IQmpy(Vb,cwte)
            +_IQmpy(Vc,cwta),_IQ(0.666667));
      Vs  = _IQ(1)-_IQsqrt(_IQmpy(Vd,Vd)+_IQmpy(Vq,Vq));

      Vs = _IQabs(Vs);
      Vsf = SecOrderFilter(Vs);

      return HysteresisA(Vsf);

}

_iq SecOrderFilter(_iq u) {
      _iq y;

      xn[0] = _IQmpy(x[0],_IQ(0.993092695057976))
            +_IQmpy(x[1],_IQ(-1.96710364349232))
            +_IQmpy(u,_IQ(0.996546347528988));
      xn[1] = _IQmpy(x[0],_IQ(0.000019930926950))
            +_IQmpy(x[1],_IQ(0.999980328963565))
            +_IQmpy(u,_IQ(0.000009965463475));

      x[0]  = xn[0];
      x[1]  = xn[1];

      y     = _IQmpy(x[0],_IQ(0.0000196710364349))
            +_IQmpy(x[1],_IQ(1.97390146568309))
            +_IQmpy(u,_IQ(0.000009835518217));
      return y;
}

_iq HysteresisA(_iq Vx) {

      if (Vx>_IQ(0.1)) flgA1=1;
            else
                  flgA1=0;
      if(Vx>_IQ(0.04) && Vx<_IQ(0.1)) flgA2=1;
            else
                  flgA2=0;
      if (Vx>_IQ(0.04)) flgA3=1;
            else
```

```
                  flgA3=0;

      xA3 = Or(flgA1,xA1,xA2);
      xA1 = Not(flgA2)*flgA3;
      xA2 = flgA2*xA3;

      if (xA3==1)
            return _IQ(1);
      else
            return _IQ(0);
}

_iq HysteresisB(_iq Vx) {

      if (Vx>_IQ(0.1)) flgB1=1;
            else
                  flgB1=0;
      if(Vx>_IQ(0.04) && Vx<_IQ(0.1)) flgB2=1;
            else
                  flgB2=0;
      if (Vx>_IQ(0.04)) flgB3=1;
            else
                  flgB3=0;

      xB3 = Or(flgB1,xB1,xB2);
      xB1 = Not(flgB2)*flgB3;
      xB2 = flgB2*xB3;

      if (xB3==1)
            return _IQ(1);
      else
            return _IQ(0);
}

_iq HysteresisC(_iq Vx) {

      if (Vx>_IQ(0.1)) flgC1=1;
            else
                  flgC1=0;
      if(Vx>_IQ(0.04) && Vx<_IQ(0.1)) flgC2=1;
            else
                  flgC2=0;
      if (Vx>_IQ(0.04)) flgC3=1;
            else
                  flgC3=0;

      xC3 = Or(flgC1,xC1,xC2);
      xC1 = Not(flgC2)*flgC3;
      xC2 = flgC2*xC3;

      if (xC3==1)
            return _IQ(1);
      else
            return _IQ(0);
}
```

```
int Not(int x) {
      if (x==1) return 0;
      else  return 1; }

int Or(int x, int y, int z) {
      if ((x+y+z)>0) return 1;
      else  return 0;}

void SagDetection() {

      if (HysteresisA(_IQabs(_IQ(1)-A1)))
            sagA = _IQ(1);
      else
            sagA = _IQ(0);

      if (HysteresisB(_IQabs(_IQ(1)-A2)))
            sagB = _IQ(1);
      else
            sagB = _IQ(0);
      if (HysteresisC(_IQabs(_IQ(1)-A3)))
            sagC = _IQ(1);
      else
            sagC = _IQ(0);
}

void Theta(_iq u,_iq v,_iq w) {

      _iq aux11,aux12,aux13,
            aux21,aux22,aux23,
            aux31,aux32,aux33,
            aux41,aux42,aux43=_IQ(0);
      _iq e_pll1,e_pll2,e_pll3 = _IQ(0);

      e_pll1 = u - y1;

      swt901 = _IQsin(phi1);
      swt   = _IQsin(phi1+_IQ(-PI/2)-_IQ(1/180*PI));
      cwt   = _IQcos(phi1+_IQ(-PI/2)-_IQ(1/180*PI));

      aux11 = _IQmpy(Ts,K);
      A1 = A1 + _IQmpy(_IQmpy(e_pll1,swt),aux11);
      y1 = _IQmpy(A1,swt);

      aux21 = _IQmpy(e_pll1,swt901);
      aux31 = _IQmpy(Kp,Kv);
      aux41 = _IQmpy(aux21,aux31);
      intg1 = aux41 + w0;

      phi1 = phi1 + _IQmpy(intg1,Ts);

      if (phi1>=_IQ(2*PI)) phi1=_IQ(0);

      e_pll2 = v - y2;

      swt902 = _IQsin(phi2);
```

```
        swte   = _IQsin(phi2+_IQ(-PI/2)-_IQ(1/180*PI));
        cwte   = _IQcos(phi2+_IQ(-PI/2)-_IQ(1/180*PI));

        aux12 = _IQmpy(Ts,K);
        A2 = A2 + _IQmpy(_IQmpy(e_pll2,swte),aux12);
        y2 = _IQmpy(A2,swte);

        aux22 = _IQmpy(e_pll2,swt902);
        aux32 = _IQmpy(Kp,Kv);
        aux42 = _IQmpy(aux22,aux32);
        intg2 = aux42 + w0;

        phi2 = phi2 + _IQmpy(intg2,Ts);

        if (phi2>=_IQ(2*PI)) phi2=_IQ(0);

        e_pll3 = w - y3;

        swt903 = _IQsin(phi3);
        swta   = _IQsin(phi3+_IQ(-PI/2)-_IQ(1/180*PI));
        cwta   = _IQcos(phi3+_IQ(-PI/2)-_IQ(1/180*PI));

        aux13 = _IQmpy(Ts,K);
        A3 = A3 + _IQmpy(_IQmpy(e_pll3,swta),aux13);
        y3 = _IQmpy(A3,swta);

        aux23 = _IQmpy(e_pll3,swt903);
        aux33 = _IQmpy(Kp,Kv);
        aux43 = _IQmpy(aux23,aux33);
        intg3 = aux43 + w0;

        phi3 = phi3 + _IQmpy(intg3,Ts);

        if (phi3>=_IQ(2*PI)) phi3=_IQ(0);
}
```

Listing B.2. C Implementation of Static Transfer Switch

```
#include "DSP281x_Device.h"
#include "IQmathLib.h"
#include "dlog4ch.h"
#include "adc_conversion.h"
#include "sts.h"

interrupt void CpuTimerIsr(void);

//MODEL FUNCTION PROTOTYPES (Beginning)
void ThetaP(_iq,_iq,_iq);
void ThetaA(_iq,_iq,_iq);

void SagDetection();
_iq Hysteresis(_iq);
_iq SecOrderFilterP(_iq);
_iq SecOrderFilterA(_iq);
void Filtering(_iq,_iq,_iq,_iq,_iq,_iq);
void Gpio_Select(void);
void Transfer();
void TransferToAlternate();
void TransferToPreffered();
void Control();
void InitOutput();
void DqDetect();
void ZeroCross();
int RangeComparator(_iq,_iq,_iq);

//MODEL FUNCTION PROTOTYPES (End)

//AUX. VARIABLES (Beginning)
long int_count = 0;
int flag = 0;
int sn = 0;
int sp = 0;
int a=0;
int load = 0;
int transfer = 0;

int zcntaA=0,zcntpA =0,zcntaB=0,zcntpB=0,zcntaC=0,zcntpC=0;
int APP=0,APN=0,AAP=0,AAN=0,BPP=0,BPN=0;
int BAP=0,BAN=0,CPP=0,CPN=0,CAP=0,CAN=0;
_iq tmpzcpA=_IQ(0),tmpzcpB=_IQ(0),tmpzcpC=_IQ(0);
_iq tmpzcaA=_IQ(0),tmpzcaB=_IQ(0),tmpzcaC=_IQ(0);

_iq sag=_IQ(0);
_iq dx;
_iq tmpx =_IQ(0);
_iq filtered = _IQ(0);
_iq t = _IQ(0);

int16 DlogCh1=0, DlogCh2=0, DlogCh3=0, DlogCh4=0;
int flg1 = 0, flg2 = 0;

//AUX. VARIABLES (End)
```

```
// PLL VARIABLES (Beginning)

_iq Ts = _IQ(0.000025);
_iq K  = _IQ(150);
_iq Kp = _IQ(25);
_iq Kv = _IQ(25);
_iq w0 = _IQ(W);

// PLL VARIABLES (End)


//PREFERRED PLL VARIABLES (Beginning)
_iq py1 = _IQ(0), py2 = _IQ(0), py3 = _IQ(0);
_iq pA1 = _IQ(0), pA2 = _IQ(0), pA3 = _IQ(0);

_iq pintg1 = _IQ(0), pintg2 = _IQ(0), pintg3  = _IQ(0);
_iq pphi1 = _IQ(0), pphi2 = _IQ(0), pphi3 = _IQ(0);
_iq pswt901 = _IQ(0), pswt902 = _IQ(0), pswt903 = _IQ(0);

_iq pswt = _IQ(0),_iq pswte = _IQ(0),_iq pswta = _IQ(0);
_iq pcwt = _IQ(0), pcwte = _IQ(0), pcwta = _IQ(0);

//PREFERRED PLL VARIABLES (End)

//ALTERNATE PLL VARIABLES (Beginning)
_iq ay1 = _IQ(0), ay2 = _IQ(0), ay3 = _IQ(0);
_iq aA1 = _IQ(0), aA2 = _IQ(0), aA3 = _IQ(0);

_iq aintg1 = _IQ(0), aintg2  = _IQ(0), aintg3  = _IQ(0);
_iq aphi1 = _IQ(0), aphi2 = _IQ(0), aphi3 = _IQ(0);

_iq aswt901 = _IQ(0), aswt902 = _IQ(0), aswt903 = _IQ(0);
_iq aswt = _IQ(0), aswte = _IQ(0), aswta = _IQ(0);
_iq acwt = _IQ(0), acwte = _IQ(0), acwta = _IQ(0);

// ALTERNATE PLL VARIABLES (End)


//GLOBAL VARIABLES (Beginning)

_iq VpAB = _IQ(0), VpBC = _IQ(0), VpCA = _IQ(0);
_iq VaAB = _IQ(0), VaBC = _IQ(0), VaCA = _IQ(0);

_iq prefA = _IQ(0), prefB = _IQ(0), prefC = _IQ(0);
_iq altA  = _IQ(0), altB  = _IQ(0), altC  = _IQ(0);

_iq VsP   = _IQ(0), VsA   = _IQ(0), VsfP  = _IQ(0), VsfA  = _IQ(0);

int Vprf = 0, Valt = 0;

//GLOBAL VARIABLES (End)

//FILTER VARIABLES (Beginning)

_iq xpA[2]={_IQ(0),_IQ(0)};_iq xnpA[2]={_IQ(0),_IQ(0)};
_iq xpB[2]={_IQ(0),_IQ(0)};_iq xnpB[2]={_IQ(0),_IQ(0)};
```

```
_iq xpC[2]={_IQ(0),_IQ(0)};_iq xnpC[2]={_IQ(0),_IQ(0)};
_iq xaA[2]={_IQ(0),_IQ(0)};_iq xnaA[2]={_IQ(0),_IQ(0)};
_iq xaB[2]={_IQ(0),_IQ(0)};_iq xnaB[2]={_IQ(0),_IQ(0)};
_iq xaC[2]={_IQ(0),_IQ(0)};_iq xnaC[2]={_IQ(0),_IQ(0)};
_iq xA[2]={_IQ(0),_IQ(0)};_iq xnA[2]={_IQ(0),_IQ(0)};
_iq xP[2]={_IQ(0),_IQ(0)};_iq xnP[2]={_IQ(0),_IQ(0)};

//FILTER VARIABLES (End)

DLOG_4CH dlog = DLOG_4CH_DEFAULTS;
ADCVALS adc = ADCVALS_DEFAULTS;

void main(void)
{

      InitSysCtrl();

      DINT;
      IER = 0x0000;
      IFR = 0x0000;

      InitPieCtrl();

      InitPieVectTable();

      Gpio_Select();

      EvaRegs.GPTCONA.all=0;

      EvaRegs.EVAIMRA.bit.T1UFINT=1;
      EvaRegs.EVAIFRA.bit.T1UFINT=1;

      EALLOW;
      PieVectTable.TINT0 = &CpuTimerIsr;
      EDIS;

      InitCpuTimers();

      ConfigCpuTimer(&CpuTimer0, 150, 25);

      PieCtrlRegs.PIEIER1.bit.INTx7=1;
      IER = M_INT1;

      EINT;
      ERTM;

      InitOutput();

      dlog.iptr1=&DlogCh1;
      dlog.iptr2=&DlogCh2;
      dlog.iptr3=&DlogCh3;
      dlog.iptr4=&DlogCh4;

      dlog.trig_value=0x0;
      dlog.size=0x400;
      dlog.prescalar=8;
```

```
      dlog.init(&dlog);

      adc.ChSelect1 = 0x3210;
      adc.ChSelect2 = 0x7654;
      adc.ChSelect3 = 0xBA98;
      adc.ChSelect4 = 0xFEDC;
      adc.init(&adc);

      GpioDataRegs.GPADAT.all = 0;

      CpuTimer0Regs.TCR.bit.TSS = 0;

    while(1)
      {
            //ENDLESS LOOP
      }
}

interrupt void CpuTimerIsr(void)
{
      int_count++;

      t+=_IQ(0.000025);

      adc.read(&adc);

      VpAB = _IQ15toIQ(_IQmpy(_IQ(1.2),adc.Ch1Out));
      VpBC = _IQ15toIQ(_IQmpy(_IQ(1.2),adc.Ch2Out));
      VpCA = _IQ15toIQ(_IQmpy(_IQ(1.2),adc.Ch3Out));

      VaAB = _IQ15toIQ(_IQmpy(_IQ(1.2),adc.Ch4Out));
      VaBC = _IQ15toIQ(_IQmpy(_IQ(1.2),adc.Ch5Out));
      VaCA = _IQ15toIQ(_IQmpy(_IQ(1.2),adc.Ch6Out));

      prefA = _IQ15toIQ(adc.Ch9Out);
      prefB = _IQ15toIQ(adc.Ch10Out);
      prefC = _IQ15toIQ(adc.Ch11Out);

      altA  = _IQ15toIQ(adc.Ch12Out);
      altB  = _IQ15toIQ(adc.Ch13Out);
      altC  = _IQ15toIQ(adc.Ch14Out);

      ThetaP(VpAB,VpBC,VpCA);
      ThetaA(VaAB,VaBC,VaCA);

      Filtering(prefA,prefB,prefC,altA,altB,altC);

//    SagDetection();
      DqDetect();
//    ZeroCross();

      zcntpA = RangeComparator(_IQ(-0.01),_IQ(0.01),prefA);
      zcntpB = RangeComparator(_IQ(-0.01),_IQ(0.01),prefB);
      zcntpC = RangeComparator(_IQ(-0.01),_IQ(0.01),prefC);
```

```
zcntaA = RangeComparator(_IQ(-0.01),_IQ(0.01),altA);
zcntaB = RangeComparator(_IQ(-0.01),_IQ(0.01),altB);
zcntaC = RangeComparator(_IQ(-0.01),_IQ(0.01),altC);


if (transfer == 0) {

      if (Vprf==0 && Valt==1)
            {
            if (load !=1)
                  {
                  TransferToAlternate();
                  transfer=1;
                  }
            }
      else if (Vprf==1 && Valt==0)
            {
            if (load != 0)
                  {
                  TransferToPreffered();
                  transfer=2;
                  }
            }
      else if (Vprf==1 && Valt==1)
            {
            if (load != 0)
                  {
                  TransferToPreffered();
                  transfer=2;
                  }
            }
      else if (Vprf==0 && Valt==0)
            {
            if (load != 0)
                  {
                  TransferToPreffered();
                  transfer=2;
                  }
            }
}
else if (transfer==1) TransferToAlternate();
else if (transfer==2) TransferToPreffered();

//MEASUREMENT CODE SEGMENT (Beginning)

DlogCh1 = (int16)(long)adc.Ch1Out;
DlogCh2 = (int16)_IQtoIQ15(_IQmpy(_IQ(0.5),VpAB));
DlogCh3 = (int16)_IQtoIQ15(_IQmpy(_IQ(0.5),VpBC));
DlogCh4 = (int16)_IQtoIQ15(_IQmpy(_IQ(0.5),VpCA));
dlog.update(&dlog);

//MEASUREMENT CODE SEGMENT (End)

EvaRegs.EVAIMRA.bit.T1UFINT = 1;
EvaRegs.EVAIFRA.all = BIT9;
PieCtrlRegs.PIEACK.all |= PIEACK_GROUP1;}
```

```
void TransferToAlternate() {

      if (zcntpA) {
                  AAP=1; APP=0;
                  GpioDataRegs.GPADAT.bit.GPIOA1 = AAP;
                  GpioDataRegs.GPADAT.bit.GPIOA4 = APP;
                  }
      if (zcntpB) {
                  BAP=1; BPP=0;
                  GpioDataRegs.GPADAT.bit.GPIOA3 = BAP;
                  GpioDataRegs.GPADAT.bit.GPIOA2 = BPP;
                  }
      if (zcntpC) {
                  CAP=1; CPP=0;
                  GpioDataRegs.GPADAT.bit.GPIOA5 = CAP;
                  GpioDataRegs.GPADAT.bit.GPIOA0 = CPP;
                  }

      if (AAP==1 && BAP==1 && CAP==1) {load=1;transfer=0;}
}

void TransferToPreffered() {


      if (zcntaA) {
                  AAP=0; APP=1;
                  GpioDataRegs.GPADAT.bit.GPIOA1 = AAP;
                  GpioDataRegs.GPADAT.bit.GPIOA4 = APP;
                  }
      if (zcntaB) {
                  BAP=0; BPP=1;
                  GpioDataRegs.GPADAT.bit.GPIOA3 = BAP;
                  GpioDataRegs.GPADAT.bit.GPIOA2 = BPP;
                  }
      if (zcntaC) {
                  CAP=0; CPP=1;
                  GpioDataRegs.GPADAT.bit.GPIOA5 = CAP;
                  GpioDataRegs.GPADAT.bit.GPIOA0 = CPP;
                  }

      if (APP==1 && BPP==1 && CPP==1) {load=0;transfer=0;}

}


void Filtering(_iq pA,_iq pB,_iq pC,_iq aA,_iq aB,_iq aC) {

      xnpA[0] = _IQmpy(xpA[0],A1)+_IQmpy(xpA[1],A2)+_IQmpy(pA,B1);
      xnpA[1] = _IQmpy(xpA[0],A3)+_IQmpy(xpA[1],A4)+_IQmpy(pA,B2);
      xpA[0]  = xnpA[0];
      xpA[1]  = xnpA[1];

      prefA   = _IQmpy(xpA[0],C1)+_IQmpy(xpA[1],C2)+_IQmpy(pA,D);

      xnpB[0] = _IQmpy(xpB[0],A1)+_IQmpy(xpB[1],A2)+_IQmpy(pB,B1);
      xnpB[1] = _IQmpy(xpB[0],A3)+_IQmpy(xpB[1],A4)+_IQmpy(pB,B2);
```

```
      xpB[0]  = xnpB[0];
      xpB[1]  = xnpB[1];

      prefB   = _IQmpy(xpB[0],C1)+_IQmpy(xpB[1],C2)+_IQmpy(pB,D);

      xnpC[0] = _IQmpy(xpC[0],A1)+_IQmpy(xpC[1],A2)+_IQmpy(pC,B1);
      xnpC[1] = _IQmpy(xpC[0],A3)+_IQmpy(xpC[1],A4)+_IQmpy(pC,B2);
      xpC[0]  = xnpC[0];
      xpC[1]  = xnpC[1];

      prefC   = _IQmpy(xpC[0],C1)+_IQmpy(xpC[1],C2)+_IQmpy(pC,D);

      xnaA[0] = _IQmpy(xaA[0],A1)+_IQmpy(xaA[1],A2)+_IQmpy(aA,B1);
      xnaA[1] = _IQmpy(xaA[0],A3)+_IQmpy(xaA[1],A4)+_IQmpy(aA,B2);
      xaA[0]  = xnaA[0];
      xaA[1]  = xnaA[1];

      altA    = _IQmpy(xaA[0],C1)+_IQmpy(xaA[1],C2)+_IQmpy(aA,D);

      xnaB[0] = _IQmpy(xaB[0],A1)+_IQmpy(xaB[1],A2)+_IQmpy(aB,B1);
      xnaB[1] = _IQmpy(xaB[0],A3)+_IQmpy(xaB[1],A4)+_IQmpy(aB,B2);
      xaB[0]  = xnaB[0];
      xaB[1]  = xnaB[1];

      altB    = _IQmpy(xaB[0],C1)+_IQmpy(xaB[1],C2)+_IQmpy(aB,D);

      xnaC[0] = _IQmpy(xaC[0],A1)+_IQmpy(xaC[1],A2)+_IQmpy(aC,B1);
      xnaC[1] = _IQmpy(xaC[0],A3)+_IQmpy(xaC[1],A4)+_IQmpy(aC,B2);
      xaC[0]  = xnaC[0];
      xaC[1]  = xnaC[1];

      altC    = _IQmpy(xaC[0],C1)+_IQmpy(xaC[1],C2)+_IQmpy(aC,D);

}

void ThetaP(_iq u,_iq v,_iq w) {

      _iq aux11,aux12,aux13,
            aux21,aux22,aux23,
            aux31,aux32,aux33,
            aux41,aux42,aux43=_IQ(0);
      _iq e_pll1,e_pll2,e_pll3 = _IQ(0);

      e_pll1 = u - py1;

      pswt901 = _IQsin(pphi1);
      pswt   = _IQsin(pphi1+_IQ(-PI/2)-_IQ(1/180*PI));
      pcwt   = _IQcos(pphi1+_IQ(-PI/2)-_IQ(1/180*PI));

      aux11 = _IQmpy(Ts,K);
      pA1 = pA1 + _IQmpy(_IQmpy(e_pll1,pswt),aux11);
      py1 = _IQmpy(pA1,pswt);

      aux21 = _IQmpy(e_pll1,pswt901);
      aux31 = _IQmpy(Kp,Kv);
      aux41 = _IQmpy(aux21,aux31);
```

```
      pintg1 = aux41 + w0;

      pphi1 = pphi1 + _IQmpy(pintg1,Ts);
      if (pphi1>=_IQ(2*PI)) pphi1=_IQ(0);

      e_pll2 = v - py2;

      pswt902 = _IQsin(pphi2);
      pswte   = _IQsin(pphi2+_IQ(-PI/2)-_IQ(1/180*PI));
      pcwte   = _IQcos(pphi2+_IQ(-PI/2)-_IQ(1/180*PI));

      aux12 = _IQmpy(Ts,K);
      pA2 = pA2 + _IQmpy(_IQmpy(e_pll2,pswte),aux12);
      py2 = _IQmpy(pA2,pswte);

      aux22 = _IQmpy(e_pll2,pswt902);
      aux32 = _IQmpy(Kp,Kv);
      aux42 = _IQmpy(aux22,aux32);
      pintg2 = aux42 + w0;

      pphi2 = pphi2 + _IQmpy(pintg2,Ts);
      if (pphi2>=_IQ(2*PI)) pphi2=_IQ(0);

      e_pll3 = w - py3;

      pswt903 = _IQsin(pphi3);
      pswta   = _IQsin(pphi3+_IQ(-PI/2)-_IQ(1/180*PI));
      pcwta   = _IQcos(pphi3+_IQ(-PI/2)-_IQ(1/180*PI));

      aux13 = _IQmpy(Ts,K);
      pA3 = pA3 + _IQmpy(_IQmpy(e_pll3,pswta),aux13);
      py3 = _IQmpy(pA3,pswta);

      aux23 = _IQmpy(e_pll3,pswt903);
      aux33 = _IQmpy(Kp,Kv);
      aux43 = _IQmpy(aux23,aux33);
      pintg3 = aux43 + w0;

      pphi3 = pphi3 + _IQmpy(pintg3,Ts);
      if (pphi3>=_IQ(2*PI)) pphi3=_IQ(0);
}

void ThetaA(_iq u,_iq v,_iq w) {

      _iq aux11,aux12,aux13,
            aux21,aux22,aux23,
            aux31,aux32,aux33,
            aux41,aux42,aux43=_IQ(0);
      _iq e_pll1,e_pll2,e_pll3 = _IQ(0);

      e_pll1 = u - ay1;

      aswt901 = _IQsin(aphi1);
      aswt = _IQsin(aphi1+_IQ(-PI/2)-_IQ(1/180*PI));
      acwt = _IQcos(aphi1+_IQ(-PI/2)-_IQ(1/180*PI));
      aux11 = _IQmpy(Ts,K);
```

```
      aA1 = aA1 + _IQmpy(_IQmpy(e_pll1,aswt),aux11);
      ay1 = _IQmpy(aA1,aswt);

      aux21 = _IQmpy(e_pll1,aswt901);
      aux31 = _IQmpy(Kp,Kv);
      aux41 = _IQmpy(aux21,aux31);
      aintg1 = aux41 + w0;

      aphi1 = aphi1 + _IQmpy(aintg1,Ts);
      if (aphi1>=_IQ(2*PI)) aphi1=_IQ(0);

      e_pll2 = v - ay2;

      aswt902 = _IQsin(aphi2);
      aswte   = _IQsin(aphi2+_IQ(-PI/2)-_IQ(1/180*PI));
      acwte   = _IQcos(aphi2+_IQ(-PI/2)-_IQ(1/180*PI));

      aux12 = _IQmpy(Ts,K);
      aA2 = aA2 + _IQmpy(_IQmpy(e_pll2,aswte),aux12);
      ay2 = _IQmpy(aA2,aswte);

      aux22 = _IQmpy(e_pll2,aswt902);
      aux32 = _IQmpy(Kp,Kv);
      aux42 = _IQmpy(aux22,aux32);
      aintg2 = aux42 + w0;

      aphi2 = aphi2 + _IQmpy(aintg2,Ts);
      if (aphi2>=_IQ(2*PI)) aphi2=_IQ(0);

      e_pll3 = w - ay3;

      aswt903 = _IQsin(aphi3);
      aswta   = _IQsin(aphi3+_IQ(-PI/2)-_IQ(1/180*PI));
      acwta   = _IQcos(aphi3+_IQ(-PI/2)-_IQ(1/180*PI));

      aux13 = _IQmpy(Ts,K);
      aA3 = aA3 + _IQmpy(_IQmpy(e_pll3,aswta),aux13);
      ay3 = _IQmpy(aA3,aswta);

      aux23 = _IQmpy(e_pll3,aswt903);
      aux33 = _IQmpy(Kp,Kv);
      aux43 = _IQmpy(aux23,aux33);
      aintg3 = aux43 + w0;

      aphi3 = aphi3 + _IQmpy(aintg3,Ts);
      if (aphi3>=_IQ(2*PI)) aphi3=_IQ(0);
}

void DqDetect() {

      _iq Vd,Vq;
      int flgP=0,flgA=0;

      Vd   = _IQmpy(_IQmpy(VpAB,aswt)+_IQmpy(VpBC,aswte)
            +_IQmpy(VpCA,aswta),_IQ(0.666667));
      Vq   = _IQmpy(_IQmpy(VpAB,acwt)+_IQmpy(VpBC,acwte)
```

```
            +_IQmpy(VpCA,acwta),_IQ(0.666667));

      VsP  = _IQsqrt(_IQmpy(Vd,Vd)+_IQmpy(Vq,Vq));
      VsP  = _IQabs(VsP);
      VsfP = SecOrderFilterP(VsP);

      Vd   = _IQmpy(_IQmpy(VaAB,aswt)+_IQmpy(VaBC,aswte)
           +_IQmpy(VaCA,aswta),_IQ(0.666667));
      Vq   = _IQmpy(_IQmpy(VaAB,acwt)+_IQmpy(VaBC,acwte)
           +_IQmpy(VaCA,acwta),_IQ(0.666667));

      VsA  = _IQsqrt(_IQmpy(Vd,Vd)+_IQmpy(Vq,Vq));
      VsA  = _IQabs(VsA);
      VsfA = SecOrderFilterA(VsA);

      if (Hysteresis(_IQabs(_IQ(1)-VsfP))) flgP=0; else flgP=1;
      if (Hysteresis(_IQabs(_IQ(1)-VsfA))) flgA=0; else flgA=1;

      Vprf = flgP;
      Valt = flgA;}

_iq SecOrderFilterP(_iq u) {
      _iq y;

      xnP[0] = _IQmpy(xP[0],_IQ(0.9889252934))
      +_IQmpy(xP[1],_IQ(-2.453738228)) +_IQmpy(u,_IQ(0.9944626467));
      xnP[1] = _IQmpy(xP[0],_IQ(0.0000248615))
      +_IQmpy(xP[1],_IQ(0.9999693282))+_IQmpy(u,_IQ(0.0000124307));

      xP[0]  = xnP[0];
      xP[1]  = xnP[1];

      y = _IQmpy(xP[0],_IQ(0.0000306717))
      +_IQmpy(xP[1],_IQ(2.4673632605))+_IQmpy(u,_IQ(0.0000153358));
      return y;
}

_iq SecOrderFilterA(_iq u) {
      _iq y;

      xnA[0] = _IQmpy(xA[0],_IQ(0.9889252934))
      +_IQmpy(xA[1],_IQ(-2.453738228))+_IQmpy(u,_IQ(0.9944626467));

      xnA[1] = _IQmpy(xA[0],_IQ(0.0000248615))
      +_IQmpy(xA[1],_IQ(0.9999693282))+_IQmpy(u,_IQ(0.0000124307));

      xA[0]  = xnA[0];
      xA[1]  = xnA[1];

      y = _IQmpy(xA[0],_IQ(0.0000306717))
      +_IQmpy(xA[1],_IQ(2.4673632605))+_IQmpy(u,_IQ(0.0000153358));

      return y;
}

void SagDetection() {
```

```
      int flgpA=0,flgpB=0,flgpC=0;
      int flgaA=0,flgaB=0,flgaC=0;

      if (Hysteresis(_IQabs(_IQ(1)-pA1))) flgpA=0; else flgpA=1;
      if (Hysteresis(_IQabs(_IQ(1)-pA2))) flgpB=0; else flgpB=1;
      if (Hysteresis(_IQabs(_IQ(1)-pA3))) flgpC=0; else flgpC=1;

      if (Hysteresis(_IQabs(_IQ(1)-aA1))) flgaA=0; else flgaA=1;
      if (Hysteresis(_IQabs(_IQ(1)-aA2))) flgaB=0; else flgaB=1;
      if (Hysteresis(_IQabs(_IQ(1)-aA3))) flgaC=0; else flgaC=1;

      Vprf = flgpA*flgpB*flgpC;
      Valt = flgaA*flgaB*flgaC;}

      _iq Hysteresis(_iq Vx) {

      int flgA1=0, flgA2=0, flgA3 = 0;
      int xA1  =0, xA2  =0, xA3   = 0;

      if (Vx>_IQ(0.1)) flgA1=1;
            else  flgA1=0;
      if(Vx>_IQ(0.04) && Vx<_IQ(0.1)) flgA2=1;
            else  flgA2=0;
      if (Vx>_IQ(0.04)) flgA3=1;
            else  flgA3=0;

      xA3 = Or(flgA1,xA1,xA2);
      xA1 = Not(flgA2)*flgA3;
      xA2 = flgA2*xA3;

      if (xA3==1) return _IQ(1); else return _IQ(0);
}

int Not(int x) {
      if (x==1) return 0;
      else return 1;
}

int Or(int x, int y, int z) {
      if ((x+y+z)>0)return 1;
      else return 0;
}

int RangeComparator(_iq xl,_iq xh,_iq in) {
      int ret=0;
      if (in<xl)ret=0;
            else if (in>=xl && in<=xh)ret=1;
            else if (in>xh)ret=0;
      return ret;
}

void ZeroCross(){

      if (_IQmpy(tmpzcpA,prefA)<=_IQ(0))
            zcntpA = 1; else  zcntpA = 0;
```

```
      if (_IQmpy(tmpzcpB,prefB)<=_IQ(0))
            zcntpB = 1; else  zcntpB = 0;

      if (_IQmpy(tmpzcpC,prefC)<=_IQ(0))
            zcntpC = 1; else  zcntpC = 0;

      if (_IQmpy(tmpzcaA,altA)<=_IQ(0))
            zcntaA = 1; else  zcntaA = 0;

      if (_IQmpy(tmpzcaB,altB)<=_IQ(0))
            zcntaB = 1; else  zcntaB = 0;

      if (_IQmpy(tmpzcaC,altC)<=_IQ(0))
            zcntaC = 1; else  zcntaC = 0;

      tmpzcaA = altA; tmpzcaB = altB; tmpzcaC = altC;
      tmpzcpA = prefA; tmpzcpB = prefB; tmpzcpC = prefC;
}

void Gpio_Select(void)
{
    EALLOW;
    GpioMuxRegs.GPAMUX.all = 0x0;
    GpioMuxRegs.GPBMUX.all = 0x0;
    GpioMuxRegs.GPDMUX.all = 0x0;
    GpioMuxRegs.GPFMUX.all = 0x0;
    GpioMuxRegs.GPEMUX.all = 0x0;
    GpioMuxRegs.GPGMUX.all = 0x0;

    GpioMuxRegs.GPADIR.all = 0x00FF;
    GpioMuxRegs.GPBDIR.all = 0x0;
    GpioMuxRegs.GPDDIR.all = 0x0;
    GpioMuxRegs.GPEDIR.all = 0x0;
    GpioMuxRegs.GPFDIR.all = 0x0;
    GpioMuxRegs.GPGDIR.all = 0x0;

    GpioMuxRegs.GPAQUAL.all = 0x0;
    GpioMuxRegs.GPBQUAL.all = 0x0;
    GpioMuxRegs.GPDQUAL.all = 0x0;
    GpioMuxRegs.GPEQUAL.all = 0x0;
    EDIS;}

void InitOutput() {
       EvaRegs.T1PR = 3750;
       EvaRegs.T1CON.all = PWM_INIT_STATE;
       EvaRegs.COMCONA.all= 2000;

       APP=1;BPP=1;CPP=1;
       GpioDataRegs.GPADAT.bit.GPIOA0 = 1;
       GpioDataRegs.GPADAT.bit.GPIOA2 = 1;
       GpioDataRegs.GPADAT.bit.GPIOA4 = 1;
}
```

Listing B.3. C Implementation Of Shunt Active Power Filter

```
#include "DSP28x_Project.h"
#include "adc_conversion.h"
#include "math.h"

interrupt void cpu_timer0_isr(void);

#define PosK 0.01
#define NegK -0.01
#define PLIMIT 600.0
#define ILIMIT 600.0

// Hysteresis Controller Variables (Start)

long intcount=0;
int outa=0,outb=0,outc=0;
float t=0.0;

// Hysteresis Controller Variables (End)

// Function Prototypes (Beginning)

float filterP(float);
float filterQ(float);
float DcFilter(float);
int Hysteresis(float,float,float,int);
int Not(int);
void ChargeCap();
void GpioSelect(void);

// Function Prototypes (End)

// Offset Compensation Variables (Beginning)

unsigned int time_cnst = 200;
float total_cnt = 800.0;

float mt1=0.0,mt2=0.0;
float VrASum=0.0,       VrBSum=0.0,       VrCSum=0.0;
float VrAMean=0.0,      VrBMean=0.0,      VrCMean=0.0;
float IrASum=0.0,       IrBSum=0.0,       IrCSum=0.0;
float IrAMean=0.0,      IrBMean=0.0,      IrCMean=0.0;
float IfASum=0.0,       IfBSum=0.0,       IfCSum=0.0;
float IfAMean=0.0,      IfBMean=0.0,      IfCMean=0.0;

// Offset Compensation Variables (End)

// Measurement Variables (Beginning)

float VrA=0.0,VrB=0.0,VrC=0.0;
float IrA=0.0,IrB=0.0,IrC=0.0;
float IfA=0.0,IfB=0.0,IfC=0.0;
float Vcap=0.0;

// Measurement Variables (End)
```

```
// DC Link PI Compensator Variables (Beginning)

float Vcaperr=0.0,Vcappi=0.0;
float Ts=0.000025;
float Kp = 1.5;
float Ki = 4.0;
float m_int = -50.0;
float m_p=0.0;
float VCapSet=650.0;

// DC Link PI Compensator Variables (End)

// Auxilary Variables (Beginning)

float Iaph=0.0,Ibta=0.0;
float Vaph=0.0,Vbta=0.0;
float Vaph1=0.0,Vbta1=0.0;

float p_inst=0.0,p_inst_f=0.0,Pinst=0.0;

float q_inst=0.0,Qinst=0.0,Qinstdc=0.0;
float a2pb2=0.0,p=0.0,q=0.0;

float IaRef=0.0,IbRef=0.0,IcRef=0.0;
float errA=0.0,errB=0.0,errC=0.0;

int G1=0,G2=0,G3=0,G4=0,G5=0,G6=0;
int flgCap = 0;

int start=0,stcap=0;
int trg=0;

// Auxilary Variables (End)

// Filter Variables (Beginning)

float xP[2]={0.0,0.0};
float xnP[2]={0.0,0.0};

float xQ[2]={0.0,0.0};
float xnQ[2]={0.0,0.0};

float dcP[2]={0.0,0.0};
float dcnP[2]={0.0,0.0};

// Filter Variables (End)

// Va Phase Shift Varibles (Beginning)

float VaBuf[210];
unsigned int ZCFlag=0;
int n; clarke_buf=200;
int PLL_buf=0;
float Va_Filt[3],Va_old, Va_Temp,Va;

// Va Phase Shift Variables (End)
```

```
ADCVALS adc = ADCVALS_DEFAULTS;

void main(void)
{
   int i;

   InitSysCtrl();

   DINT;
   IER = 0x0000;
   IFR = 0x0000;

   InitPieCtrl();

   InitPieVectTable();

   GpioSelect();

   EALLOW;
   PieVectTable.TINT0 = &cpu_timer0_isr;
   EDIS;

   InitCpuTimers();

   ConfigCpuTimer(&CpuTimer0, 150, 25);

   PieCtrlRegs.PIEIER1.bit.INTx7 = 1;
   IER |= M_INT1;

   EINT;
   ERTM;

   mt1 = time_cnst*total_cnt;

   adc.init();

   for(i=0;i<210;i++) VaBuf[i]=0.0;

   CpuTimer0Regs.TCR.bit.TSS = 0;

   for(;;);
}


interrupt void cpu_timer0_isr(void)
{
      t +=0.000025;
      intcount++;

      adc.read(&adc);

      VrA = adc.Ch9Out*468.0;
      VrB = adc.Ch10Out*468.0;
      VrC = adc.Ch11Out*468.0;
```

```
IrA = adc.Ch4Out*8.8617;
IrB = adc.Ch5Out*8.8617;
IrC = adc.Ch6Out*8.8617;

IfA = adc.Ch1Out*3.178813;
IfB = adc.Ch2Out*3.178813;
IfC = adc.Ch3Out*3.178813;

Vcap = DcFilter(adc.Ch12Out);
Vcap *= 633.52826510;
Vcap -= 2.5;

if (start>=1) {
      VrA = VrA - VrAMean;
      VrB = VrB - VrBMean;
      VrC = VrC - VrCMean;

      IrA = IrA - IrAMean;
      IrB = IrB - IrBMean;
      IrC = IrC - IrCMean;

      IfA = IfA - IfAMean;
      IfB = IfB - IfBMean;
      IfC = IfC - IfCMean;

      mt2 = 0.0;
}

n++;
if (VrA>0.0 && ZCFlag==6) {
      clarke_buf = n*0.25;
      if (clarke_buf < 190) clarke_buf=190;
      else if (clarke_buf > 210) clarke_buf=210;
      n=1;
      ZCFlag=0;
}
else if (VrA < 0.0 && ZCFlag==0) ZCFlag=1;
else if (VrA < 0.0 && ZCFlag==1) ZCFlag=2;
else if (VrA < 0.0 && ZCFlag==2) ZCFlag=3;
else if (VrA < 0.0 && ZCFlag==3) ZCFlag=4;
else if (VrA < 0.0 && ZCFlag==4) ZCFlag=5;
else if (VrA < 0.0 && ZCFlag==5) ZCFlag=6;

PLL_buf++;
if (PLL_buf>=clarke_buf)
      PLL_buf = 0;

Vaph = VrA;
Vbta = VaBuf[PLL_buf];
VaBuf[PLL_buf] = VrA;

Vaph = Vaph*1.2247448713;
Vbta = Vbta*1.2247448713;

Iaph = IrA*0.8165 + IrB*(-0.4082) + IrC*(-0.4082);
Ibta = IrB*0.7071 + IrC*(-0.7071);
```

```
if (start==2) {

// DC LINK COMPENSATION (Beginning)

      Vcaperr = VCapSet - Vcap;
      m_p = Vcaperr*Kp;
      m_int += Ts*Ki*Vcaperr;

      if (m_p > PLIMIT)       m_p = PLIMIT;
      if (m_p < -PLIMIT)      m_p = -PLIMIT;
      if (m_int > ILIMIT)     m_int = ILIMIT;
      if (m_int < -ILIMIT)    m_int = -ILIMIT;

      Vcappi = m_p + m_int;

// DC LINK COMPENSATION (End)
}

//INSTANTENOUS P-Q VALUES (Beginning)

p_inst = Vaph*Iaph + Vbta*Ibta;
p_inst_f= filterP(p_inst);
Pinst = p_inst_f - Vcappi;

q_inst = Vaph*Ibta - Vbta*Iaph;
Qinst = filterQ(q_inst);

//INSTANTENOUS P-Q VALUES (End)

//CALCULATION OF P-Q REFS(Beginning)

a2pb2 = Vaph*Vaph + Vbta*Vbta;
p = (Vaph*Pinst - Vbta*Qinst - Vbta*0.0)/a2pb2;
q = (Vbta*Pinst + Vaph*Qinst + Vaph*0.0)/a2pb2;

//CALCULATION OF P-Q REFS(End)

//CURRENT REFERENCES (Beginning)

IaRef = p*0.8165 + q*0.0;
IbRef = p*(-0.4082) + q*0.7071;
IcRef = p*(-0.4082) + q*(-0.7071);

//CURRENT REFERENCES (End)

//ERROR CALCULATION (Beginning)
errA = IaRef - IfA;
errB = IbRef - IfB;
errC = IcRef - IfC;
//ERROR CALCULATION (End)

//PULSE GENERATION (Beginning)

G1 = Hysteresis(errA,(float)PosK,(float)NegK,1);
G4 = Not(G1);
G3 = Hysteresis(errB,(float)PosK,(float)NegK,2);
```

```
G6 = Not(G3);
G5 = Hysteresis(errC,(float)PosK,(float)NegK,3);
G2 = Not(G5);

if (start ==2 && Vcap < 900.0) {
      if (G1)
            GpioDataRegs.GPASET.bit.GPIO0=1;
      else
            GpioDataRegs.GPACLEAR.bit.GPIO0=1;
      if (G4)
            GpioDataRegs.GPASET.bit.GPIO1=1;
      else
            GpioDataRegs.GPACLEAR.bit.GPIO1=1;
      if (G3)
            GpioDataRegs.GPASET.bit.GPIO2=1;
      else
            GpioDataRegs.GPACLEAR.bit.GPIO2=1;
      if (G6)
            GpioDataRegs.GPASET.bit.GPIO3=1;
      else
            GpioDataRegs.GPACLEAR.bit.GPIO3=1;
      if (G5)
            GpioDataRegs.GPASET.bit.GPIO4=1;
      else
            GpioDataRegs.GPACLEAR.bit.GPIO4=1;
      if (G2)
            GpioDataRegs.GPASET.bit.GPIO5=1;
      else
            GpioDataRegs.GPACLEAR.bit.GPIO5=1;
      flgCap = 0;
}
// PULSE GENERATION (End)

// PROTECTION (Beginning)

if (start==2 && Vcap > 900.0) {
      ChargeCap();start=1;}

// PROTECTION (End)


if (start==0)
{
      ChargeCap();
      m_int = 0.0;
      Vcappi = 0.0;

      VrASum = VrASum + VrA;
      VrBSum = VrBSum + VrB;
      VrCSum = VrCSum + VrC;

      IrASum += IrA;
      IrBSum += IrB;
      IrCSum += IrC;
```

```
            IfASum += IfA;
            IfBSum += IfB;
            IfCSum += IfC;

            mt2++;

            if (mt2>mt1) {
                  VrAMean = VrASum/mt1;
                  VrBMean = VrBSum/mt1;
                  VrCMean = VrCSum/mt1;

                  IrAMean = IrASum/mt1;
                  IrBMean = IrBSum/mt1;
                  IrCMean = IrCSum/mt1;

                  IfAMean = IfASum/mt1;
                  IfBMean = IfBSum/mt1;
                  IfCMean = IfCSum/mt1;

                  VrASum = 0.0;
                  VrBSum = 0.0;
                  VrCSum = 0.0;

                  IrASum = 0.0;
                  IrBSum = 0.0;
                  IrCSum = 0.0;

                  IfASum = 0.0;
                  IfBSum = 0.0;
                  IfCSum = 0.0;

                  mt2 = 0.0;
            }
      }

   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}

float filterP(float u) {
      float y;

      xnP[0] = u*0.99680695054296375;
      xnP[0] = xnP[0] + xP[0]*0.99361390108592751
      + xP[1]*(-9.8380902661152980);

      xnP[1] = u*0.000012460086881787046;
      xnP[1] = xnP[1] + xP[0]*0.000024920173763574091
      + xP[1]*0.99987702387167354;

      xP[0]  = xnP[0];
      xP[1]  = xnP[1];

      y = u*0.99680695054296375 + xP[0]*(-0.0063860989140724798)
      + xP[1]*(-9.8380902661152980);

return y; }
```

```
float filterQ(float u) {
      float y;

      xnQ[0] = u*0.99680695054296375;
      xnQ[0] = xnQ[0] + xQ[0]*0.99361390108592751
      + xQ[1]*(-9.8380902661152980);

      xnQ[1] = u*0.000012460086881787046;
      xnQ[1] = xnQ[1] + xQ[0]*0.00002492017376357409l
      + xQ[1]*0.99987702387167354;

      xQ[0]  = xnQ[0];
      xQ[1]  = xnQ[1];

      y = u*0.99680695054296375 + xQ[0]*(-0.0063860989140724798)
      + xQ[1]*(-9.8380902661152980);

return y; }

float DcFilter(float u) {
      float y;

      dcnP[0] = dcP[0]*0.997643808776148 +
      dcP[1]*(-0.221804483927692) + u*0.998821904388074;

      dcnP[1] = dcP[0]*0.0000249705476097019 +
      dcP[1]*0.999997227443951 + u*0.0000124852738048509;

      dcP[0]  = dcnP[0];
      dcP[1]  = dcnP[1];

      y = dcP[0]*0.00000277255604909615 + dcP[1]*0.222065791179157
      + u*0.00000138627802454808;
      return y;
}


int Not(int x) {
      if (x==1)
            return 0;
      else
            return 1;
}

void ChargeCap(void)
{
      if (flgCap == 0) {
       GpioDataRegs.GPACLEAR.bit.GPIO0 = 1;
       GpioDataRegs.GPACLEAR.bit.GPIO1 = 1;
       GpioDataRegs.GPACLEAR.bit.GPIO2 = 1;
       GpioDataRegs.GPACLEAR.bit.GPIO3 = 1;
       GpioDataRegs.GPACLEAR.bit.GPIO4 = 1;
       GpioDataRegs.GPACLEAR.bit.GPIO5 = 1;
       flgCap = 1;
      }
}
```

```
void GpioSelect(void) {

   EALLOW;
   GpioCtrlRegs.GPAPUD.bit.GPIO0 = 0;
   GpioCtrlRegs.GPAPUD.bit.GPIO1 = 0;
   GpioCtrlRegs.GPAPUD.bit.GPIO2 = 0;
   GpioCtrlRegs.GPAPUD.bit.GPIO3 = 0;
   GpioCtrlRegs.GPAPUD.bit.GPIO4 = 0;
   GpioCtrlRegs.GPAPUD.bit.GPIO5 = 0;

   GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 0;
   GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 0;
   GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 0;
   GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 0;
   GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 0;
   GpioCtrlRegs.GPAMUX1.bit.GPIO5 = 0;

   GpioCtrlRegs.GPADIR.bit.GPIO0 = 1;
   GpioCtrlRegs.GPADIR.bit.GPIO1 = 1;
   GpioCtrlRegs.GPADIR.bit.GPIO2 = 1;
   GpioCtrlRegs.GPADIR.bit.GPIO3 = 1;
   GpioCtrlRegs.GPADIR.bit.GPIO4 = 1;
   GpioCtrlRegs.GPADIR.bit.GPIO5 = 1;
   EDIS;
}

int Hysteresis(float Vx,float ul,float al,int ch) {
      if (ch==1) {
            if (Vx >= ul) outa=1;
            else if (Vx < ul && Vx > al && outa == 1) outa=1;
            else if (Vx < ul && Vx > al && outa == 0) outa=0;
            else if (Vx <= al) outa=0;
            return outa;
      }

      if (ch==2) {
            if (Vx >= ul) outb=1;
            else if (Vx < ul && Vx > al && outb == 1) outb=1;
            else if (Vx < ul && Vx > al && outb == 0) outb=0;
            else if (Vx <= al) outb=0;
            return outb;
      }

      if (ch==3) {
            if (Vx >= ul) outc=1;
            else if (Vx < ul && Vx > al && outc == 1) outc=1;
            else if (Vx < ul && Vx > al && outc == 0) outc=0;
            else if (Vx <= al) outc=0;
            return outc;
      }
}
```

APPENDIX C: Circuit Diagrams of Signal Conditioning Board of SAPF

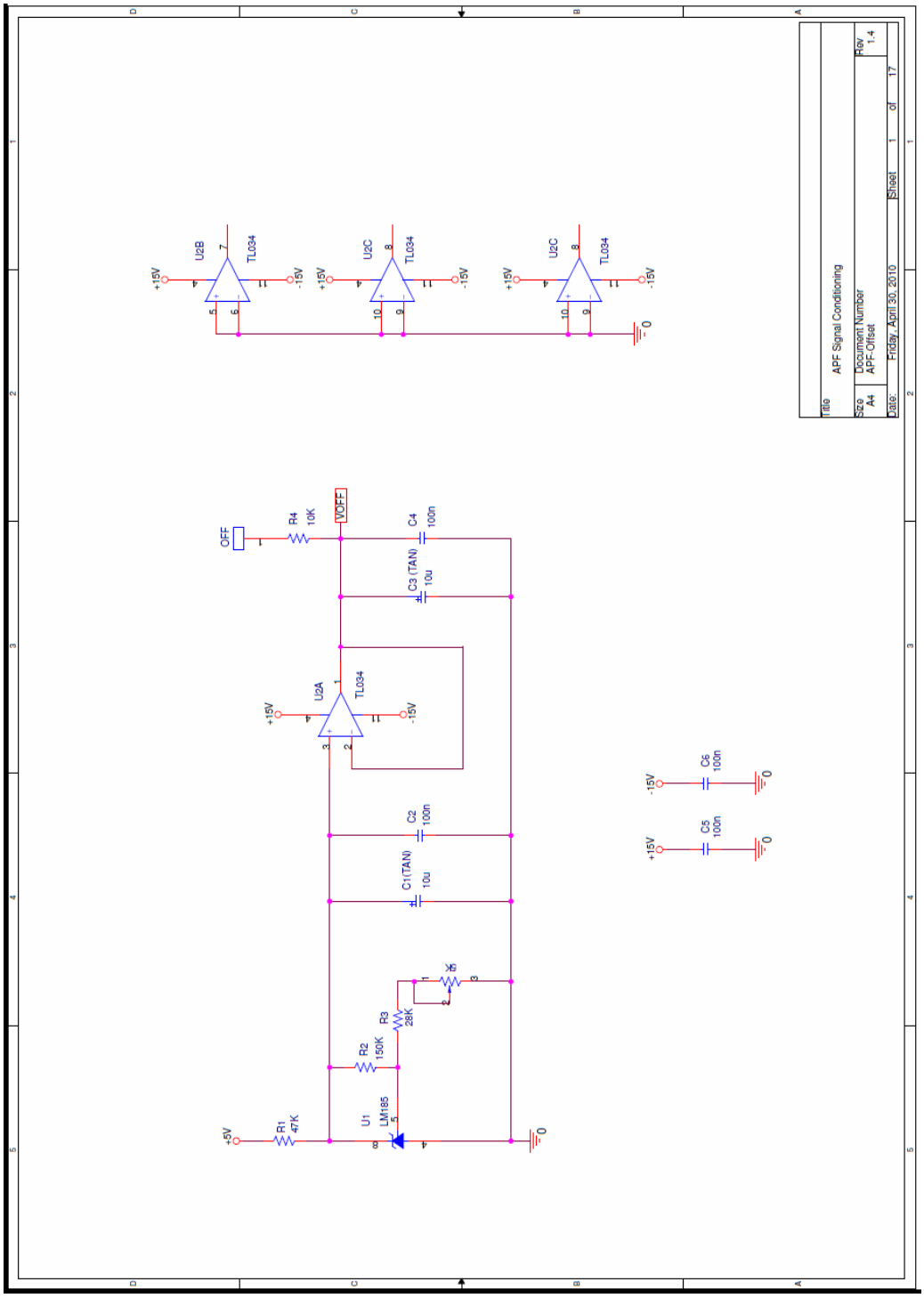

Figure C.1. Offset generation sub circuit

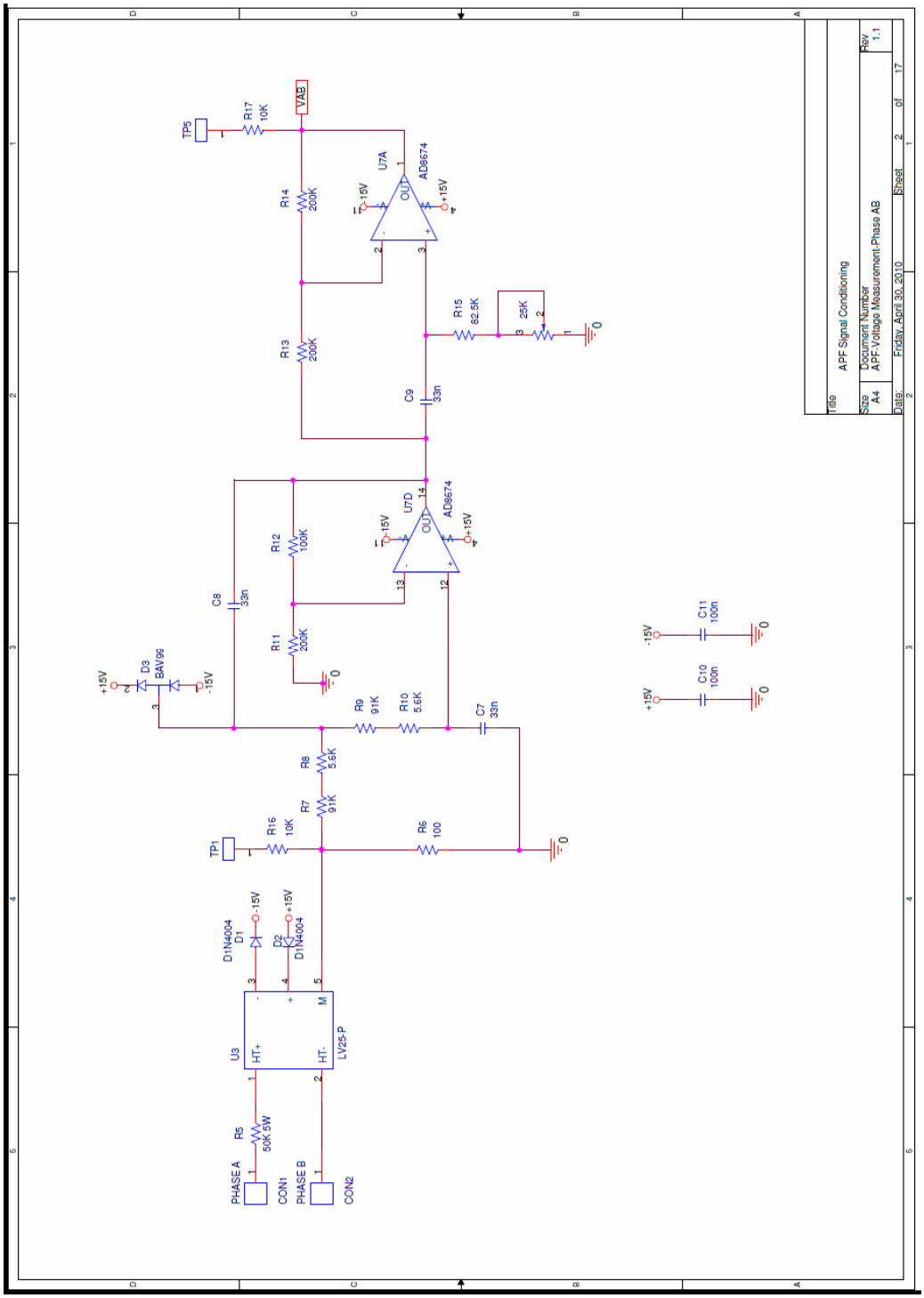

Figure C.2. Voltage measurement sub circuit of voltages of phases AB

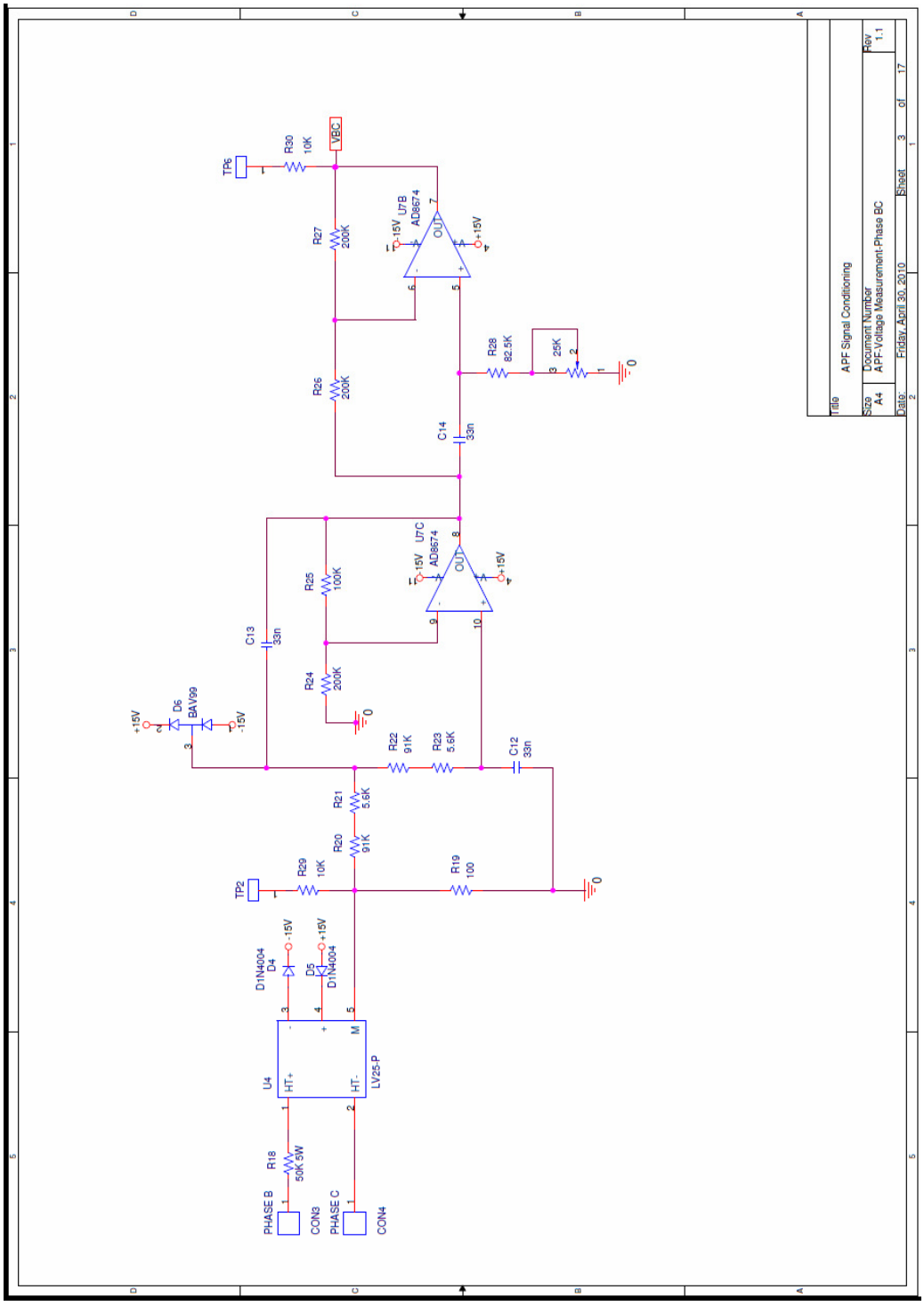

Figure C.3. Voltage measurement sub circuit of voltages of phases BC

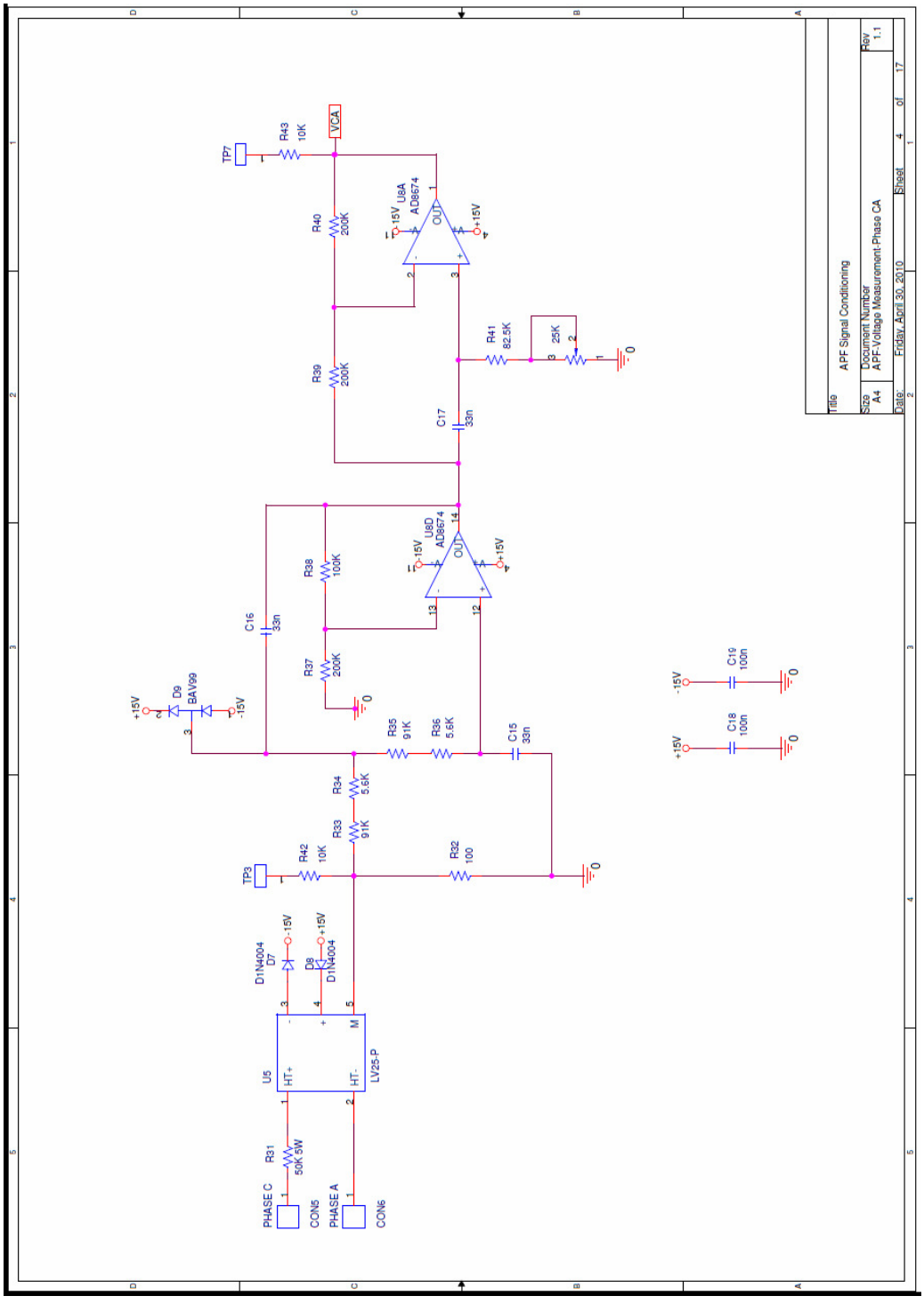

Figure C.4. Voltage measurement sub circuit of voltages of phases CA

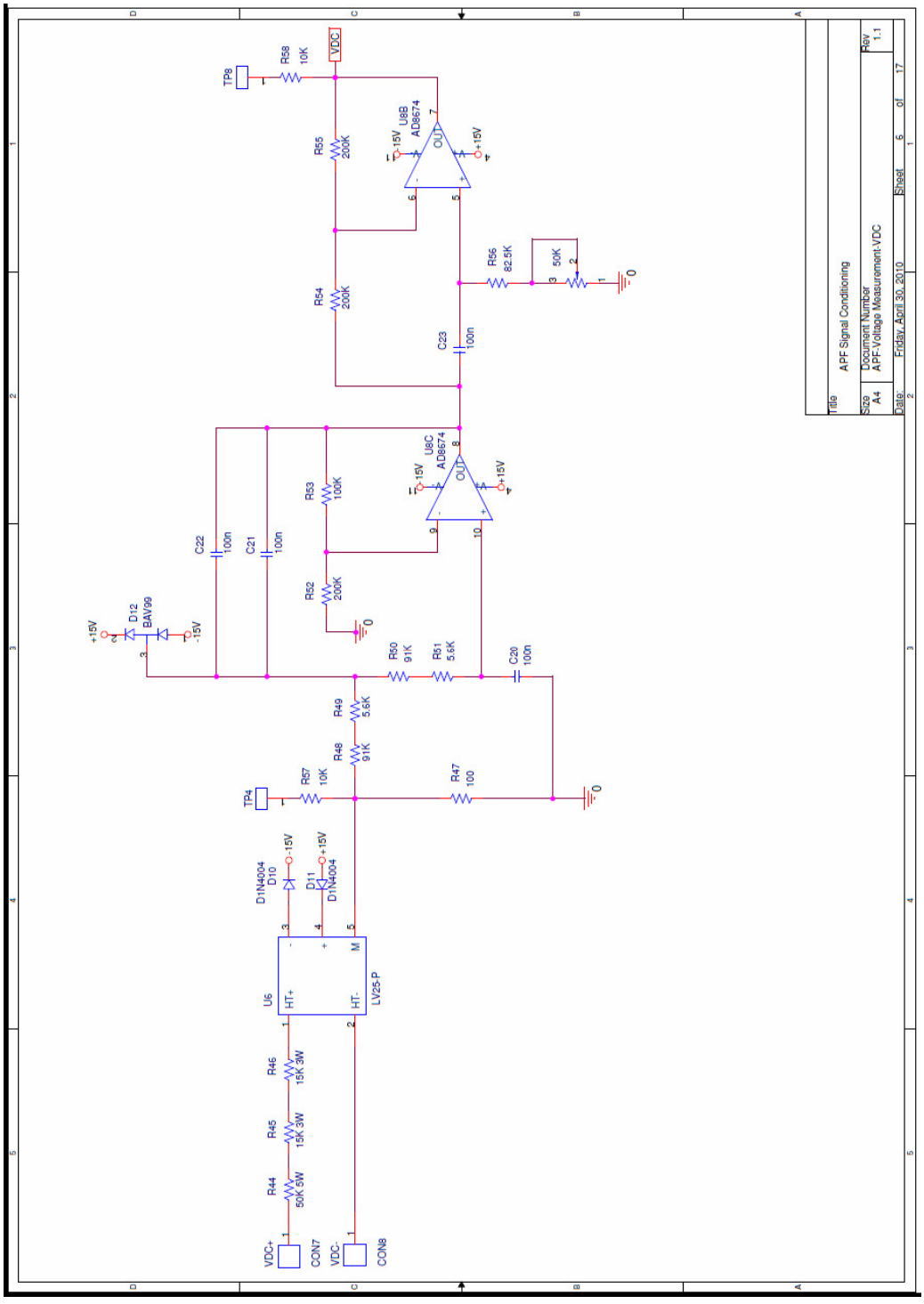

Figure C.5. Voltage measurement sub circuit of DC link voltage

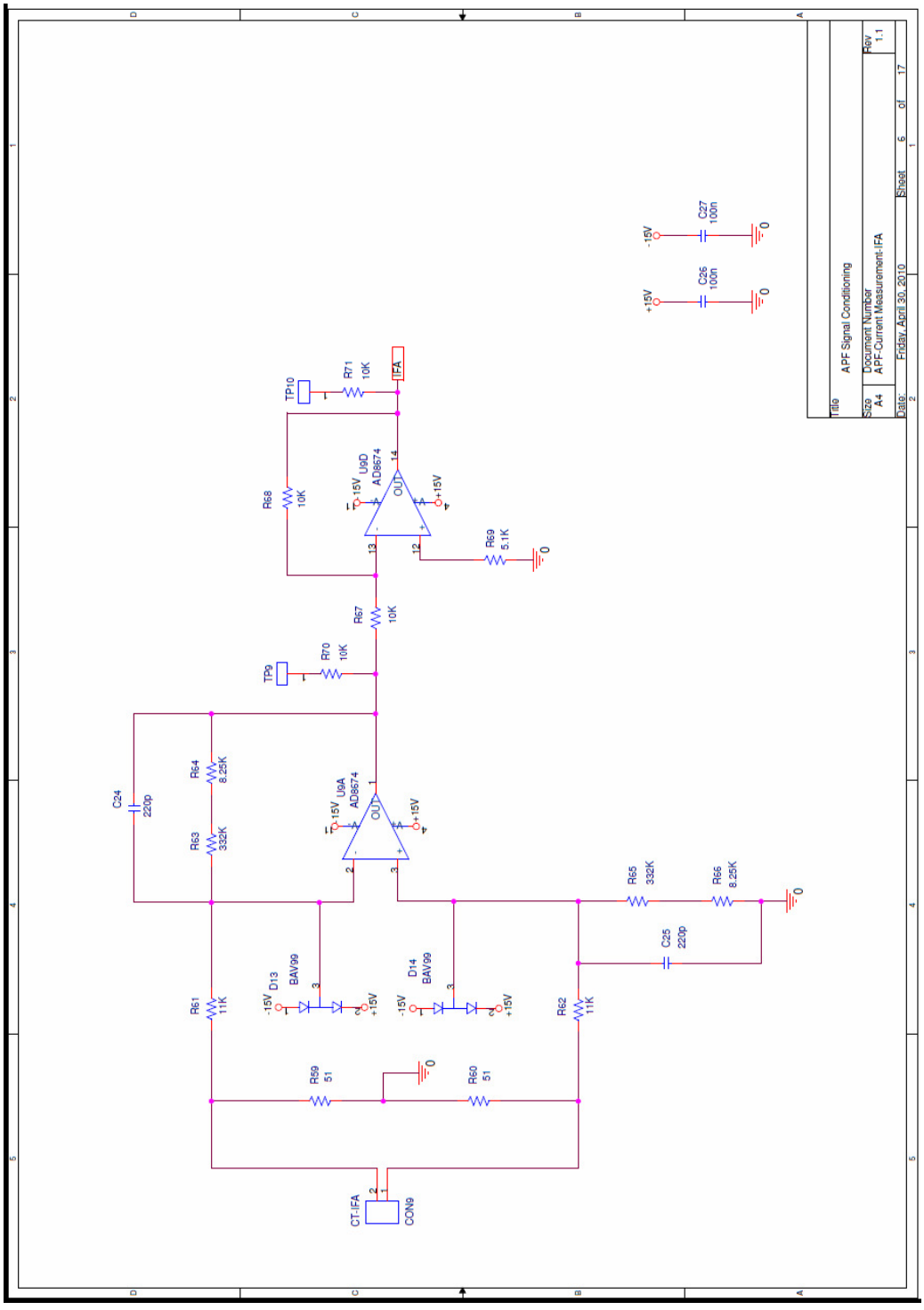

Figure C.6. Filter current measurement sub circuit for phase A

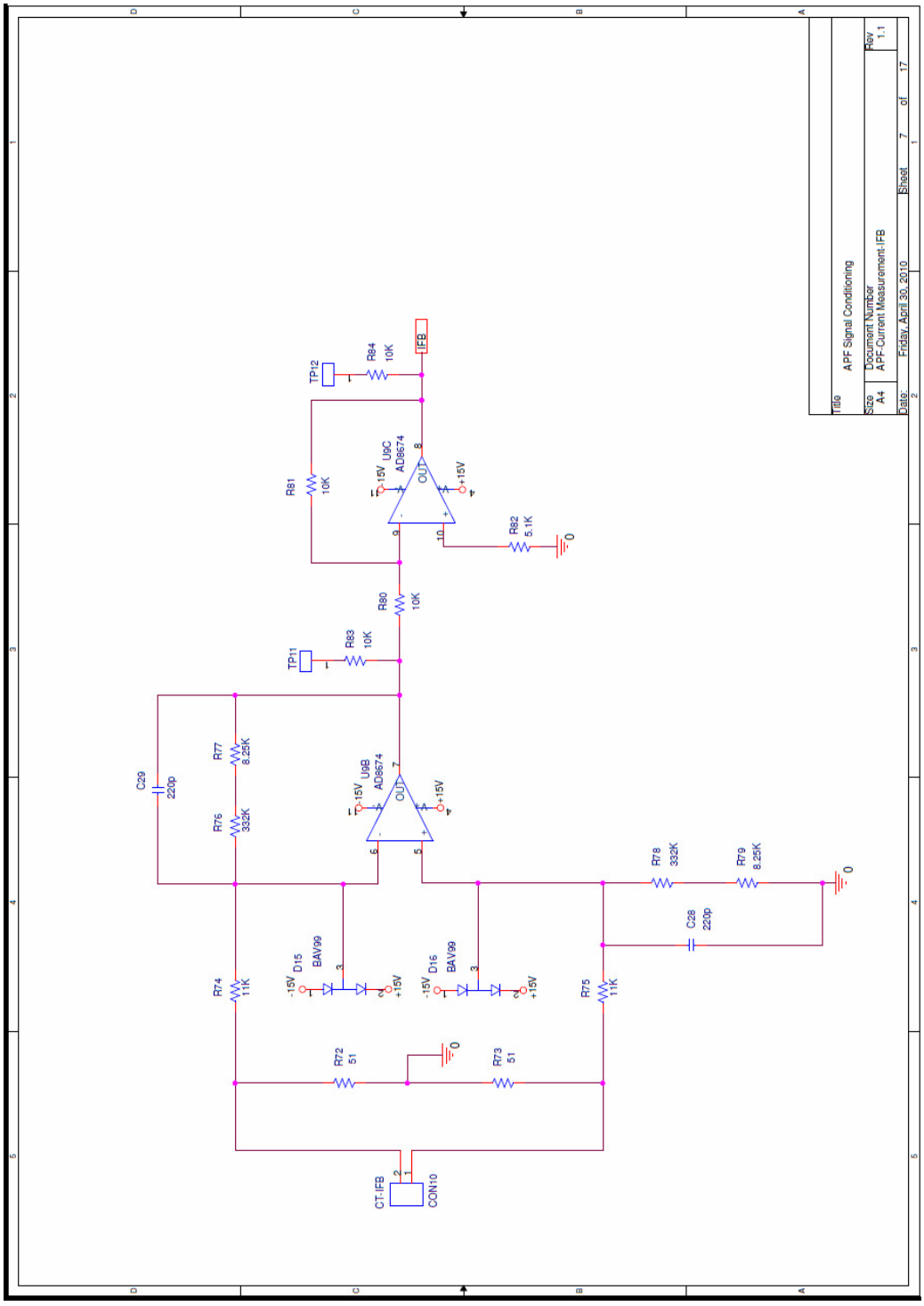

Figure C.7. Filter current measurement sub circuit for phase B

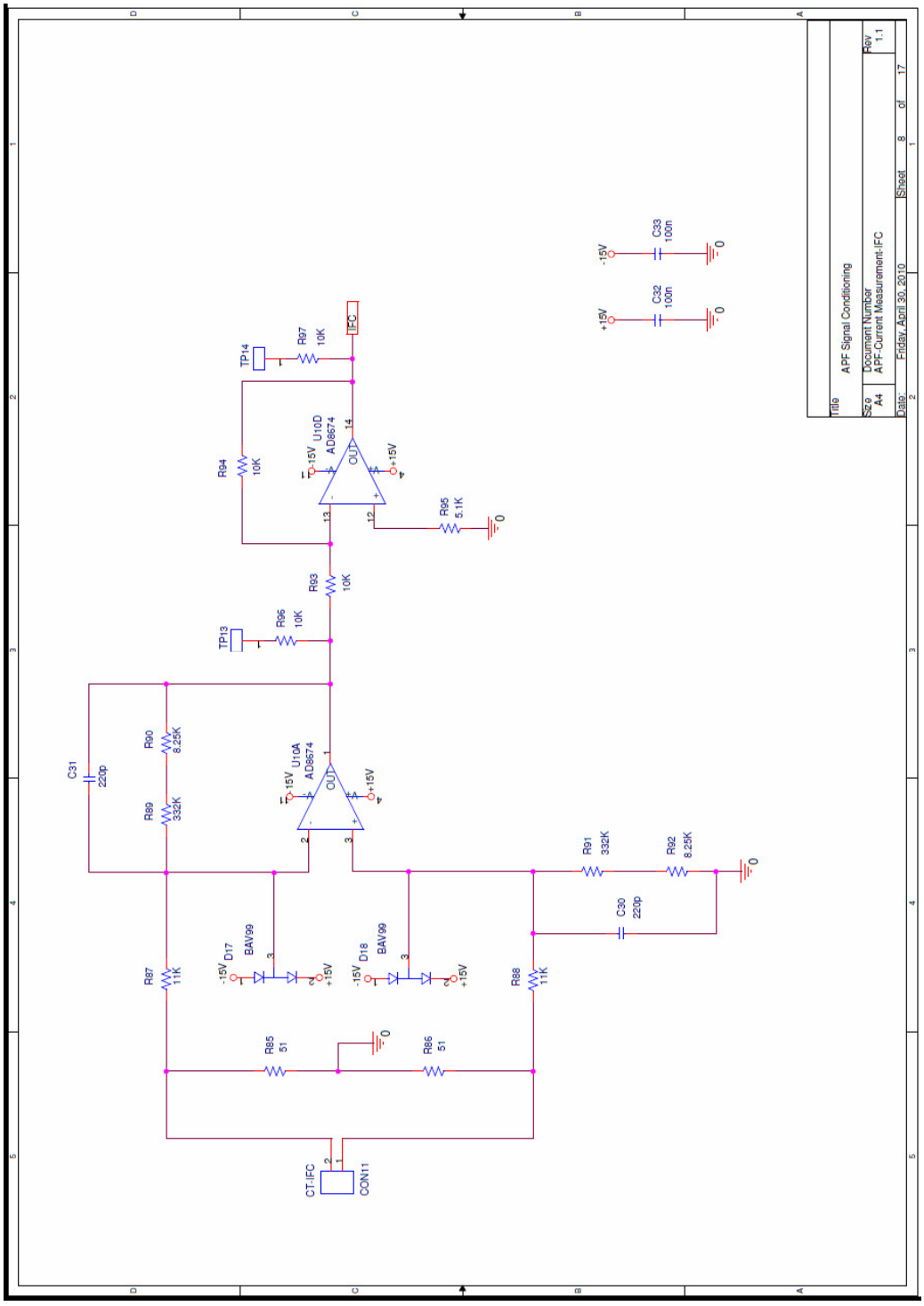

Figure C.8. Filter current measurement sub circuit for phase C

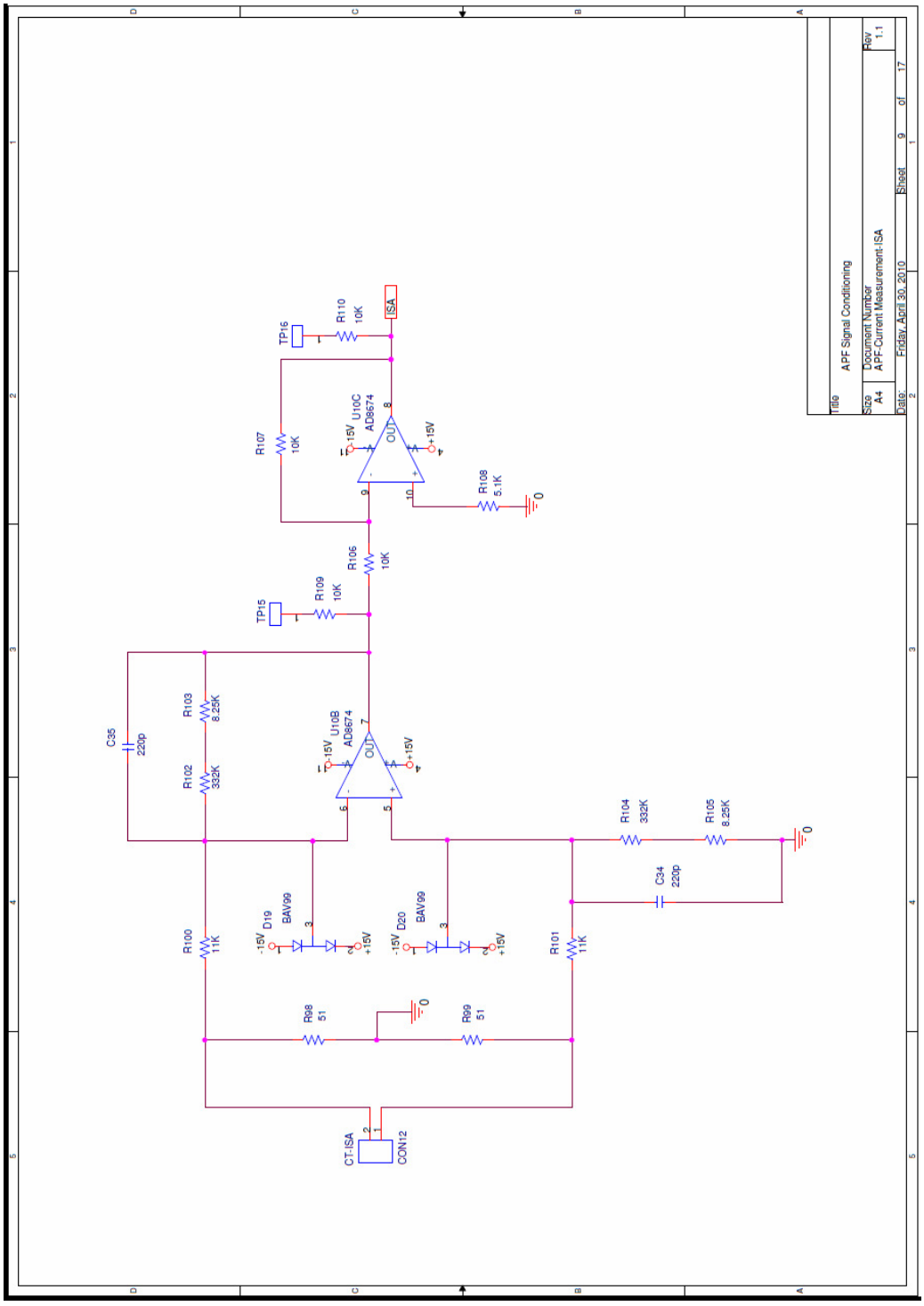

Figure C.9. Source current measurement sub circuit for phase A

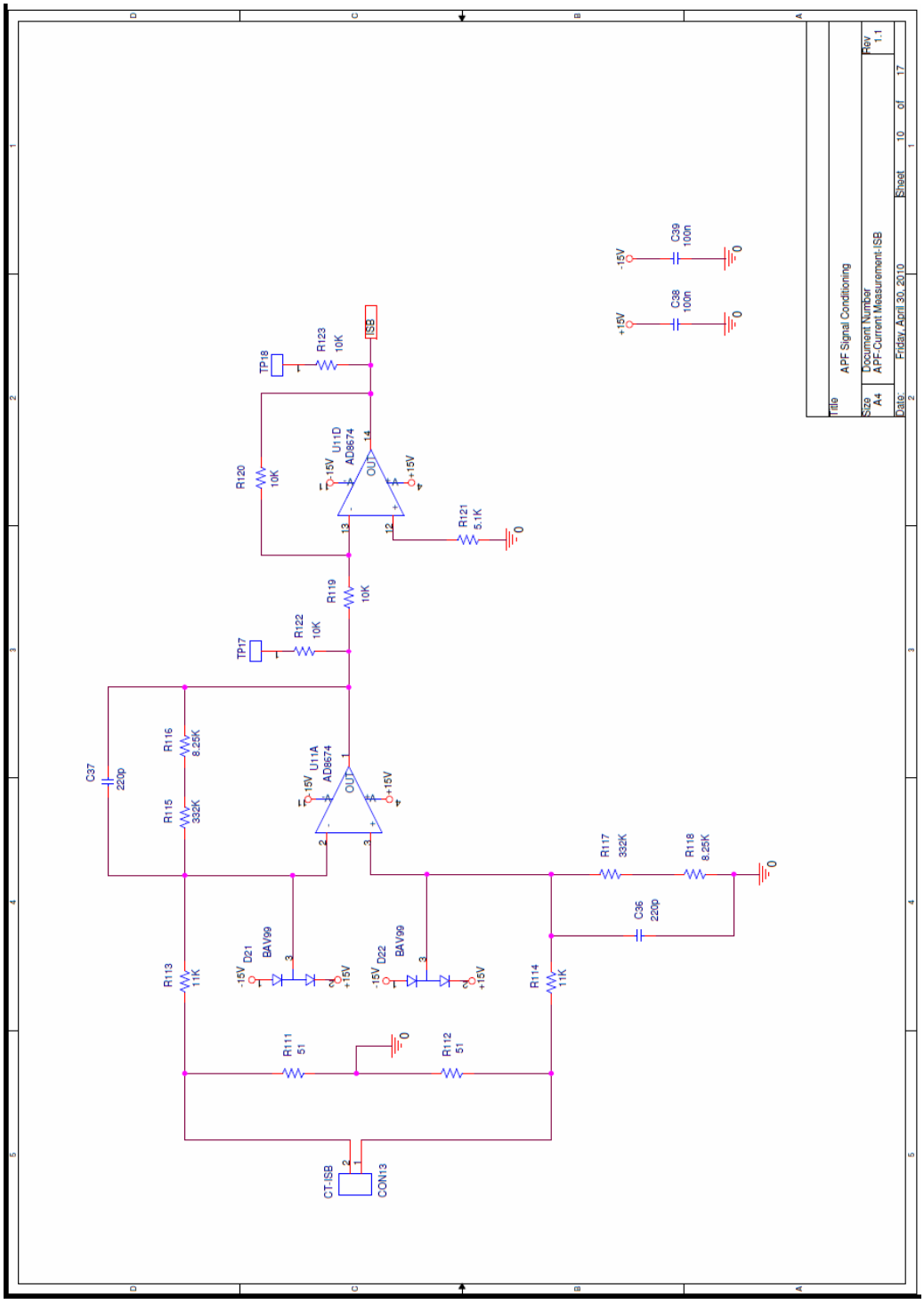

Figure C.10. Source current measurement sub circuit for phase B

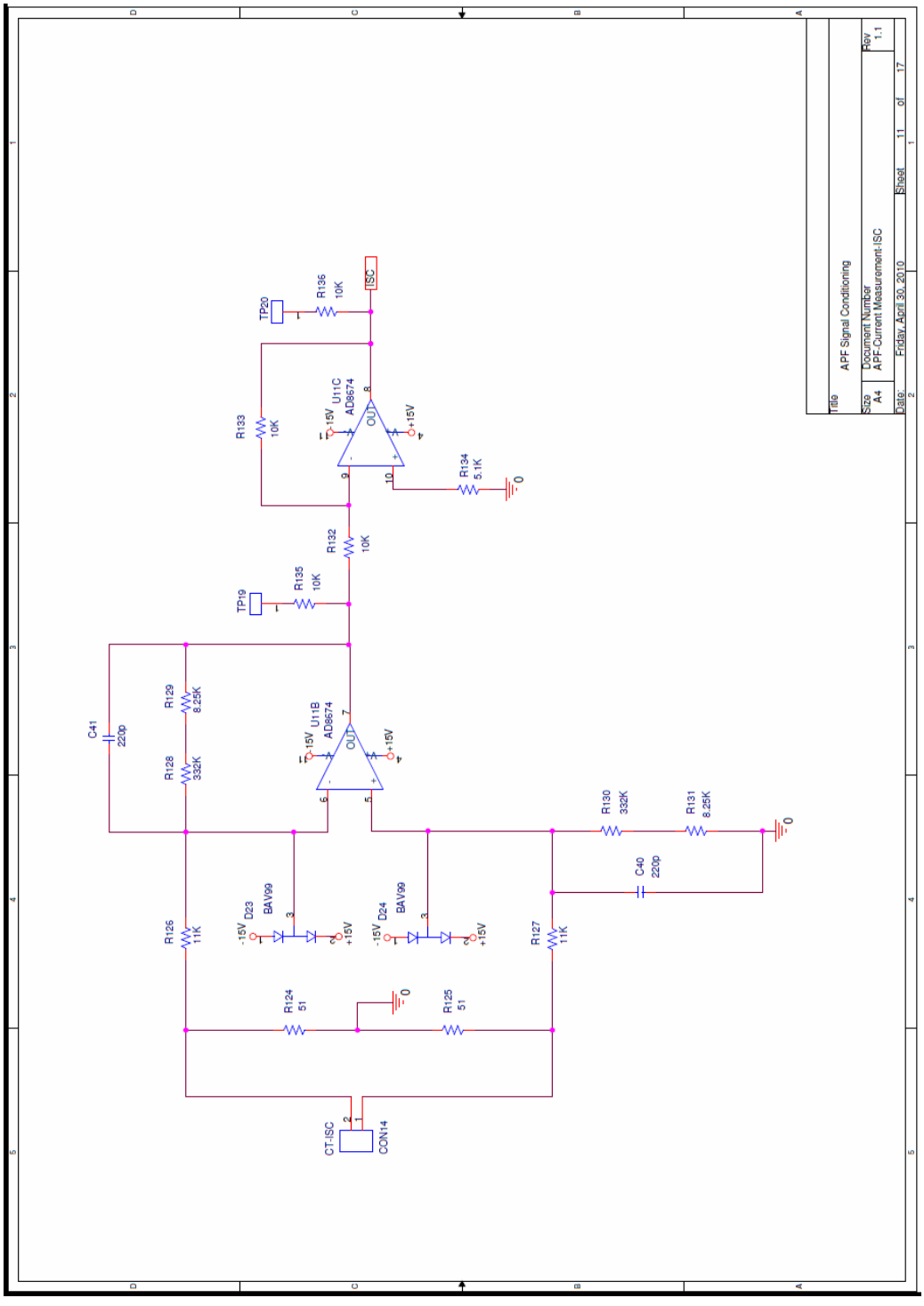

Figure C.11. Source current measurement sub circuit for phase C

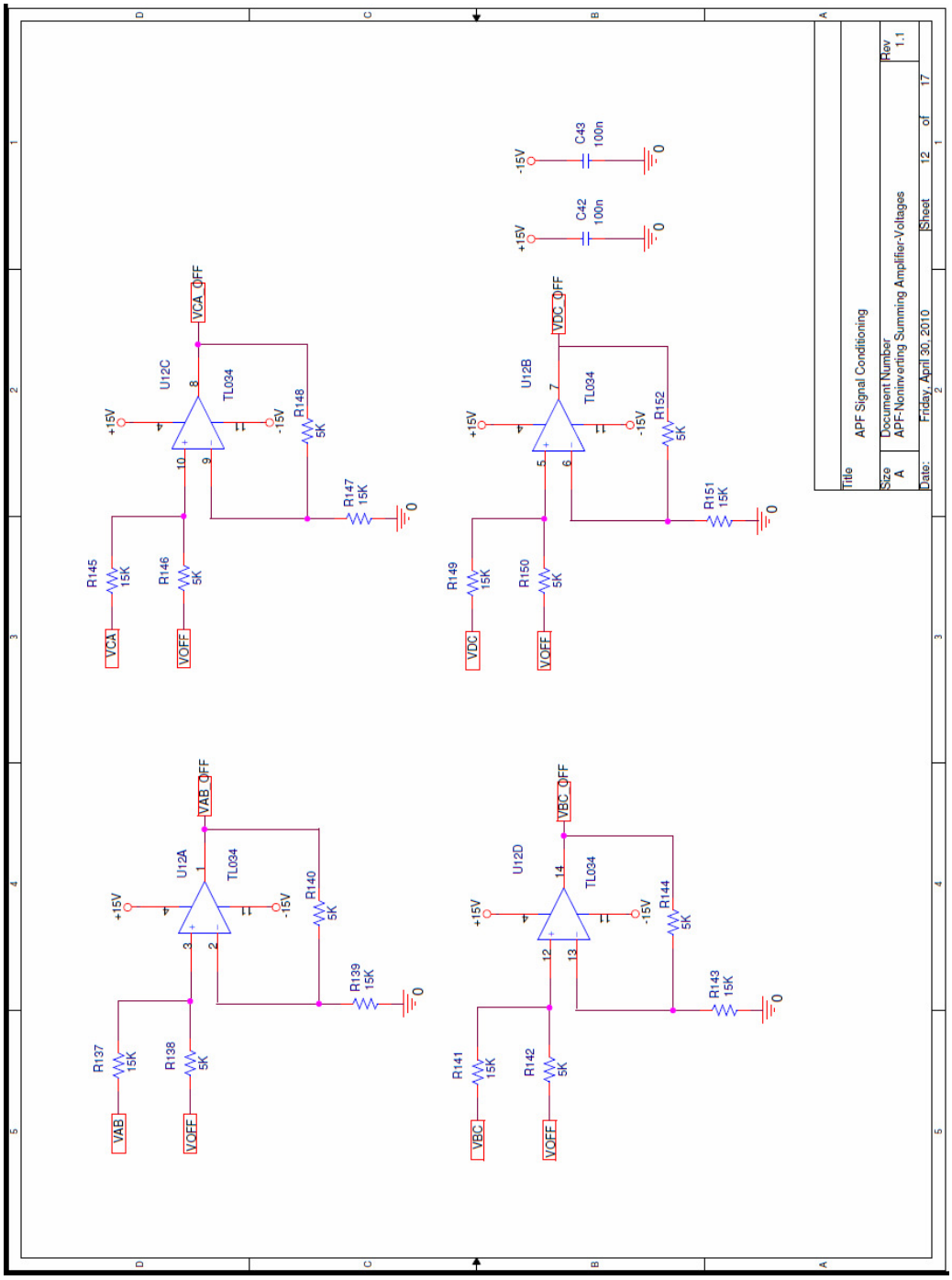

Figure C.12. Non-inverting summing amplifiers for voltage measurements

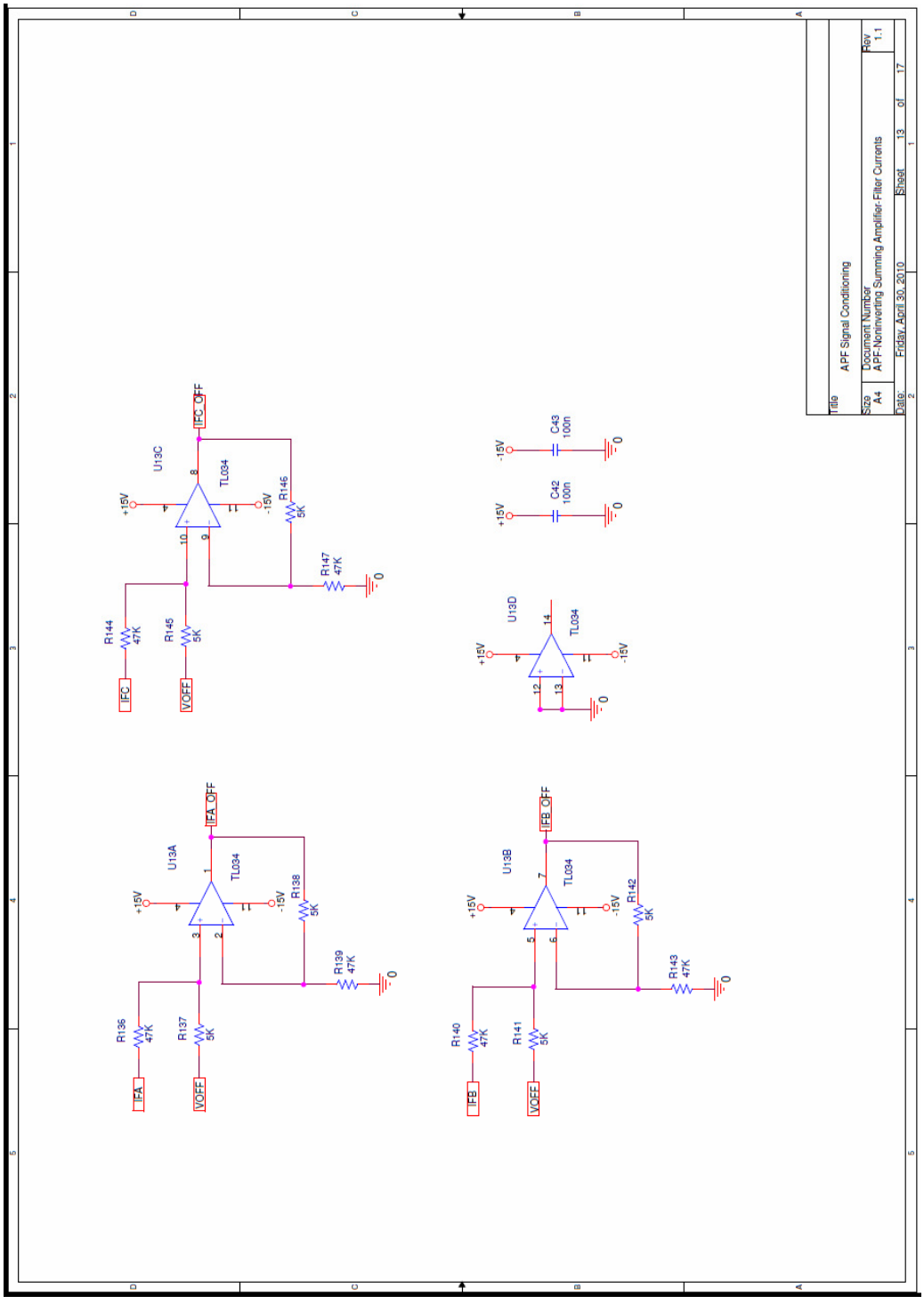

Figure C.13. Non-inverting summing amplifiers of filter current measurements

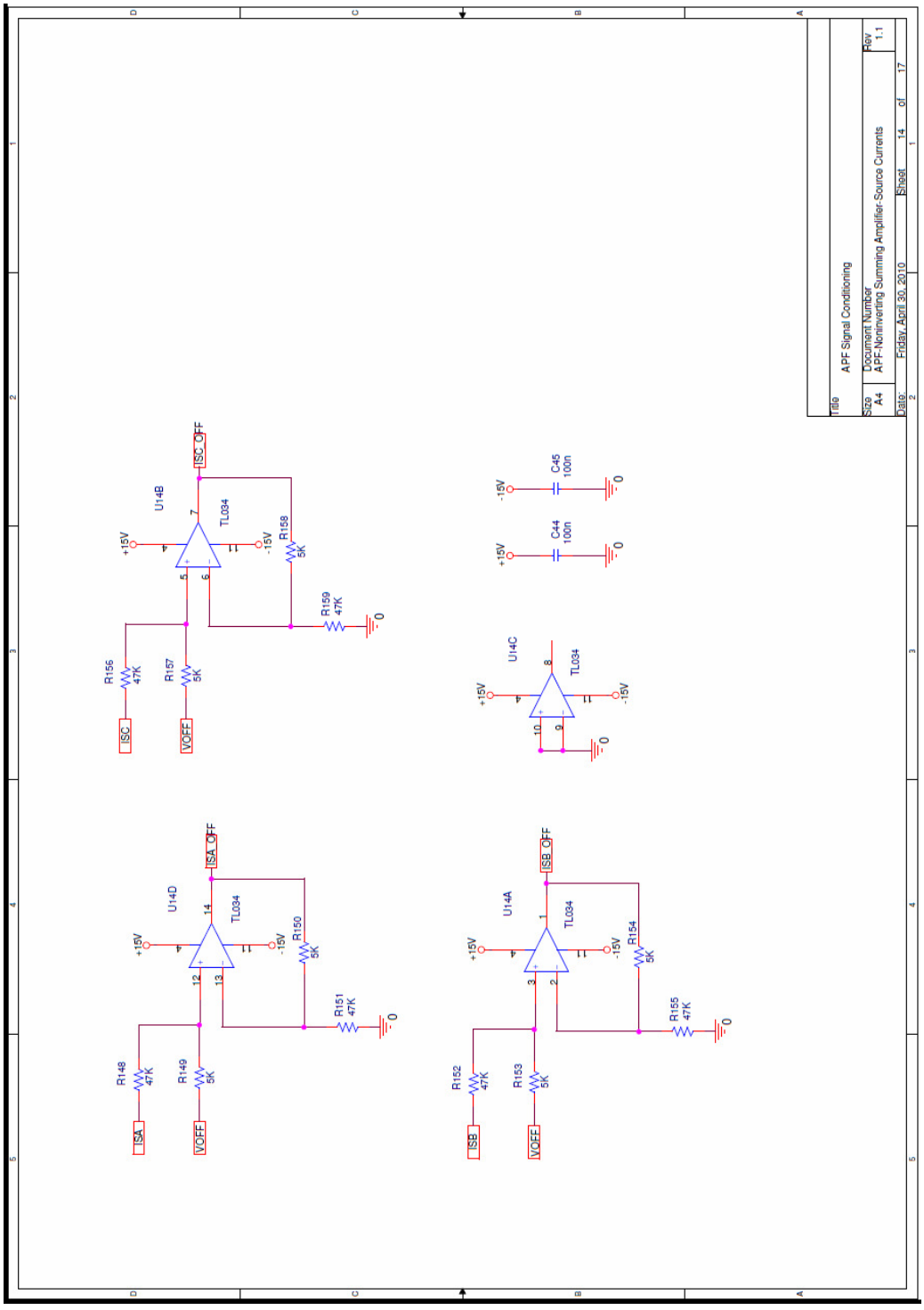

Figure C.14. Non-inverting summing amplifiers of source current measurements

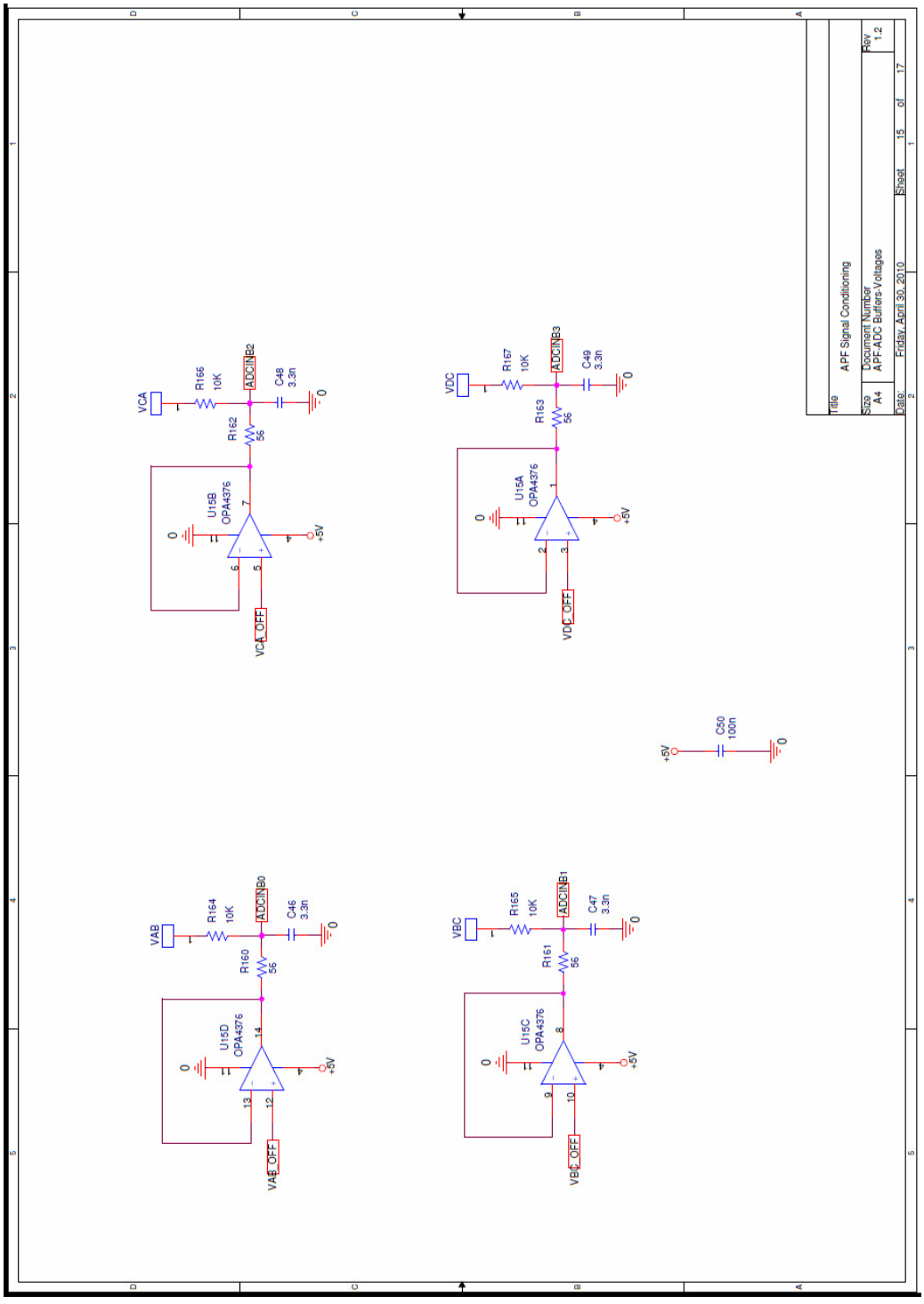

Figure C.15. ADC input buffers for voltage measurements

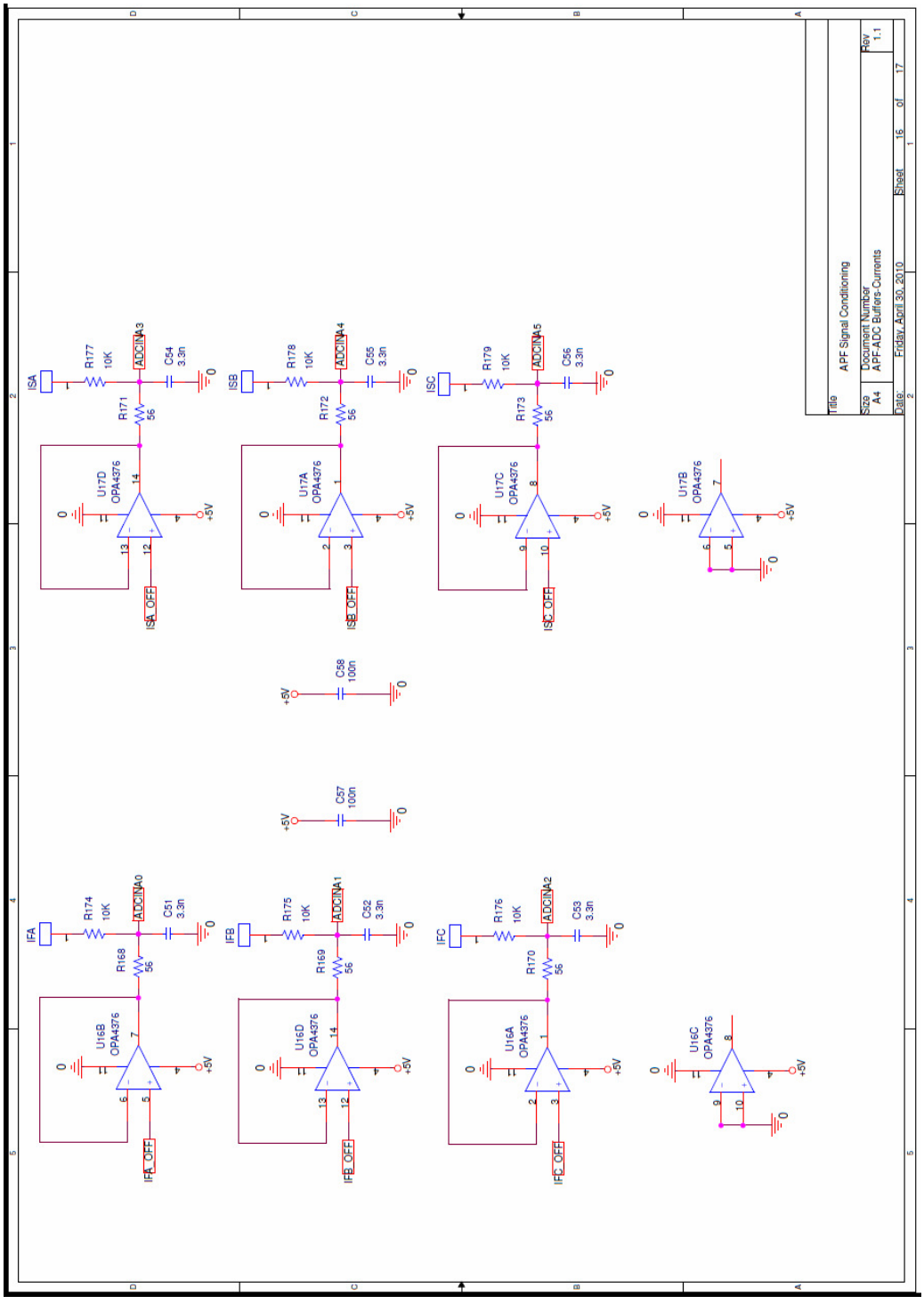

Figure C.16. ADC input buffers for current measurements

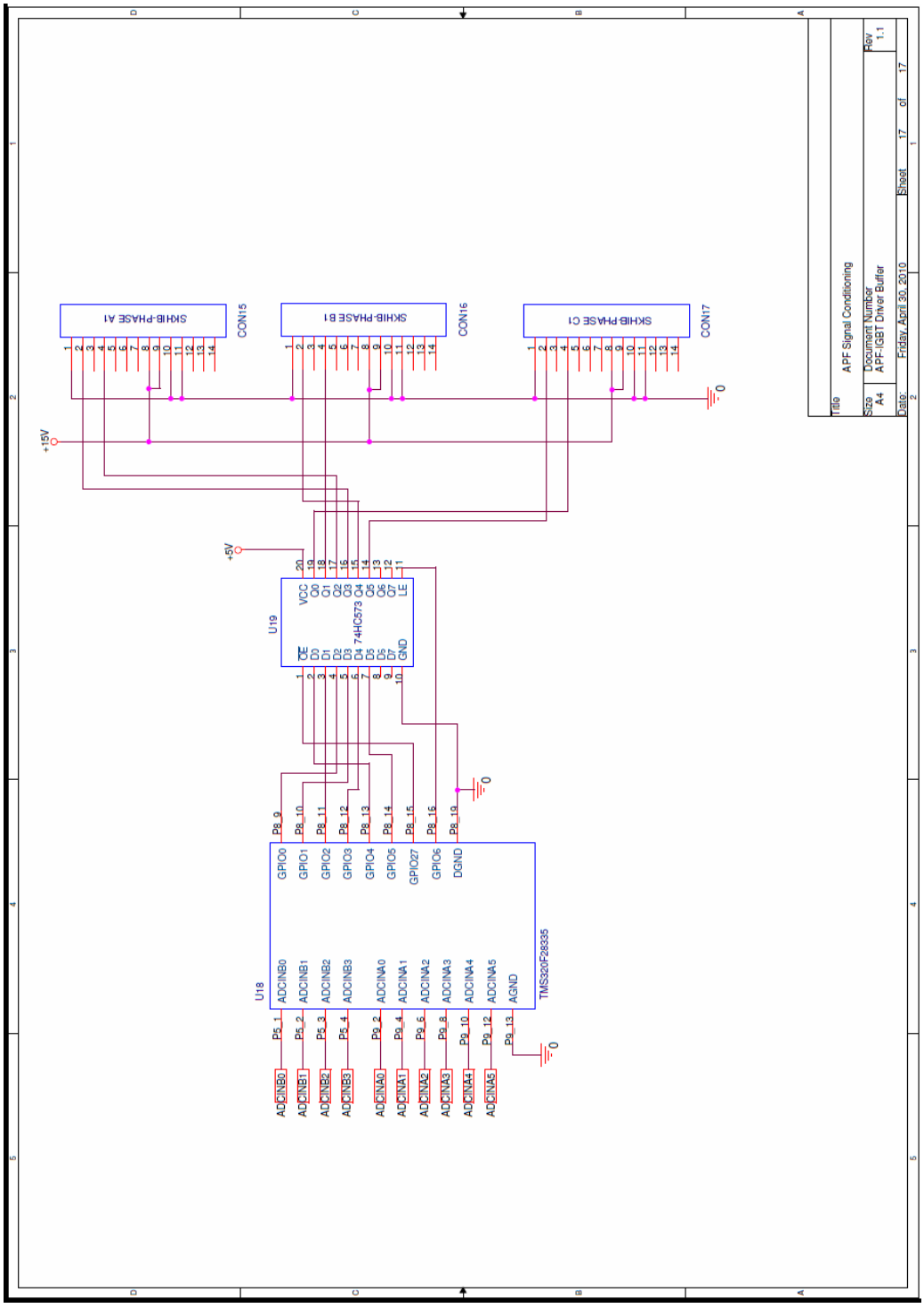

Figure C.17. DSP controller connections, output buffer sub circuit and IGBT driver connections