THE UNIVERSITY OF TURKISH AERONAUTICAL ASSOCIATION
INSTITUE OF SCIENCE AND TECHNOLOGY

IMPROVING THE BOOST CAPABILITY FOR ELECTRIC POWER CONVERSION BY A COMBINATION OF SWITCHED INDUCTORS AND IMPEDANCE-SOURCE NETWORK

MASTER THESIS

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ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT

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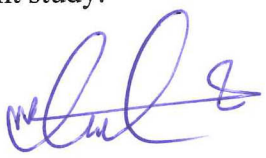
I hereby declare that all the information in this study I presented as my Master's Thesis, called: "Improving The Boost Capability For Electric Power Conversion By a Combination of Switched Inductors and Impedance-Source Network" has been presented in accordance with the academic rules and ethical conduct. I also declare and certify with my honor that I have fully cited and referenced all the sources I made use of in this present study.



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LIST OF ABBREVIATION

Ac	**:**	Alternating Current
B	**:**	Boost factor
B_B	**:**	Buck-Boost factor
C	**:**	Capacitor
CSI	**:**	Current-Source Inverter
D	**:**	Duty cycle
Dc	**:**	Direct Current
GaN	**:**	Gallium nitride
I-Source	**:**	Current source
I_L	**:**	Inductor current
L	**:**	Inductor
M	**:**	Modulation index
PWM	**:**	Pulse width modulation
PV	**:**	Photovoltaic
R	**:**	Resistance
Sic	**:**	Silicon carbide
SL&ZSI	**:**	Switched inductor combined with ZSI
SL	**:**	Switched inductor
T	**:**	Full switching cycle
T_1	**:**	The interval of active state
T_2	**:**	The interval of shoot through
V-Source	**:**	Voltage source
V_C	**:**	Capacitor voltage
VSI	**:**	Voltage Source Inverter
V_{in}	**:**	Input voltage
V_{i1}	**:**	Input voltage into ZSI
V_{i2}	**:**	dc-link voltage
(X shape SL&SZI)	**:**	X shape of switched inductor (SL) combined with ZSI
ZSI	**:**	Z-source inverter

ABSTRACT

IMPROVING THE BOOST CAPABILITY FOR ELECTRIC POWER CONVERSION BY A COMBINATION OF SWITCHED INDUCTORS AND IMPEDANCE-SOURCE NETWORK

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In the last decade, the impedance source network has been vastly used in electric power conversion with huge efficiency improvements such as in distribution systems, electric vehicles, industrial machines, and avionics. In this study, two new impedance source network topologies have been designed and modeled for inverter applications. The first is the one cell the switched inductor (SL), the second is the two cell switched inductor (X-shape SL) combined with the traditional Z-source inverter (ZSI). This combination allows the switched inductor to store the unused source energy during the shoot-through zero state which is the interval where the source separates from the ZSI network. The design is enhanced by adding multi branches in series of multiple inductors and diodes which improve the circuit performance. All simulations and calculations of the new topologies are implemented by MATLAB and National Instrument (Multisim) programs. The proposed topologies, I-SL&ZSI and X-SL&ZSI, are designed according to specific values of inductance and capacitance. These topologies prove the major improvement in boost factor (B) and elimination of start-up inrush current that are compared to the

traditional ZSI scheme. Meanwhile, the capacitor stress is also significantly reduced in both topologies.

Key Words: Switched inductor (SL), Z-source inverter (ZSI), duty cycle (D), boost factor (B), boost converter, inverter.

ÖZET

ELEKTRİKSEL GÜÇ DÖNÜŞÜMÜNDEKİ YÜKSELTME YETENEĞİNİN ANAHTARLAMALI ENDÜKTÖR VE EMPEDANS KAYNAĞI AĞI BİRLEŞİMİ KULLANIMIYLA İYİLEŞTİRİLMESİ

AL-DARRAJI, Othman Khalid Hasan
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği
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Son on yılda, empedans kaynağı ağı, elektrik enerjisinin dönüşümünde büyük oranda yüksek verimlilik iyileştirmeleri ile dağıtım sistemleri, elektrikli araçlar, endüstriyel makineler ve havacılık elektroniğinde olduğu gibi, kullanılmaktadır. Bu çalışmada, Evirgeç uygulamaları için iki yeni empedans kaynak ağ topolojisi tasarlanmış ve modellenmiştir. Birincisi anahtarlamalı evirgecin tek hücresi (SL), ikincisi anahtarlamalı evirgecin iki hücresi (X-shape [şeklinde] SL) olup, geleneksel Z-kaynaklı evirgeç (ZSI) ile birleştirilmişlerdir. Bu kombinasyon, sıfırdan geçiş (shoot-through zero) sürecinde kaynak ZSI ağından ayrıldığı esnada aralıktaki kullanılmayan kaynak enerjisinin anahtarlamalı indüktör tarafından depolanmasına imkan sağlar. Bu çalışmadaki tasarım, devrenin performansını arttıran çoklu endüktörler ve diyot serilerine çoklu dallar ekleyerek genelleştirilmiştir. Tüm benzetimlerde ve yeni topolojilerin hesaplanmasında MATLAB ve National Instrument (Multisim) programları kullanılmıştır. önerilen I-SL & ZSI ve X-SL & ZSI topolojileri spesifik endüktans ve kapasitans değerlerine göre, tasarlanmıştır.Her iki topolojide de geleneksel ZSI şemasına kıyasla Yükseltme (Boost) Faktöründe (B) büyük artış ve başlangıç ani akımının ortadan kaldırıldığıgözlemlenmiştir. Bununla birlikte, kondansatör gerilmesi (capacitor stress) her iki topolojide de önemli ölçüde azalmıştır.

Anahtar Kelimeler: Anahtarlamalı Evirgeç (SL), Z-Kaynaklı Evirgeç (ZSI), Görev Çarpanı (D), Yükseltme (Boost) Faktörü (B), Yükseltme (Boost) Dönüştürücüsü, Evirgeç.

CHAPTER ONE

INTRODUCTION

1.1 Presentation of the Study

This study presents new improvements of impedance source networks topology. Impedance source networks supply is an effective means of power conversion between source and load in an extensive range of electric power convention applications [1], [2]. The first type of this topology was called Z-source inverter (ZSI). In this study, two new proposed topologies are used which will be considered a new contribution in boost converter system. The proposed study combines between two impedance networks. The first topology combined Z-source inverter (ZSI) with one cell of switched inductor (SL), called “one cell SL&ZSI”. While the second proposed topology has two SL cells called “X-shape SL&ZSI”. These new proposed topologies will lead to a significant increase in the boost factor, elimination of the start-up inrush current and reduce the capacitor stress. The boost factor is the main reason for increasing the gain voltage in the circuit.

1.2 The Motivation for the Study

In this study, one or two cell switched inductors were combined to the ZSI to take advantage of the interval shoot-through zero state when the diode of the ZSI is reverse biased by storing the unused source energy and releasing it during the active state. So this new topology is proposed to fix the conventional ZSI problems of discontinuous input current, higher voltage stress on the capacitor and lower boost factor. The proposed one and two cell SL&ZSI give the following solutions:

1. Continuous input power.
2. A wide range of gain voltage.

3. Raised boost factor.
4. Decreased stress on the capacitor.
5. Decreased size of the capacitor.
6. Decreased duty cycle.
7. Decreased thermal losses inside the switching.

1.3 The Status of Impedance Network Topologies

Since the first proposed topology of the impedance Z-source inverter in 2002; the related research with Z-source has grown rapidly, so the modifications numbers and new proposals of Z-source topologies have expanded significantly. A recent survey conducted in September 2013 showed that the number of journal and conference papers published on impedance source networks reached a total of 1113 papers [3] as shown in Figure 1.1. Classification and synopsis of the Z-source network topologies will explain in chapter two.

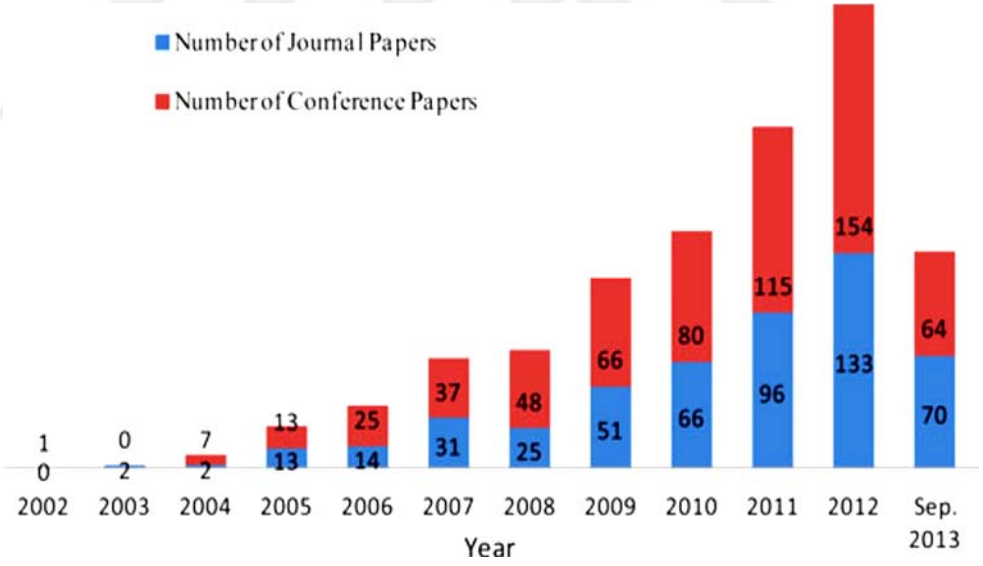


Figure 1.1: Published work related to impedance source network in the period between 2002 to Sep. 2013.

Different topologies and various control methods have been employed in the literature of impedance-source networks, e.g., for uninterruptible power supply (UPS) [4], [5], adjustable-speed drives [6],[7], battery or supercapacitor energy storage [8], [9], distributed generation [10]–[14], electric vehicles [15][16], flywheel energy storage systems [17], avionics [18], distributed dc power systems [10], electronic loads [19], dc circuit breaker [20].According to the classification of power

conversion functionality, the conversion has been classified into four major groups: dc-dc converters, ac-ac converters, ac-dc rectifiers, and dc-ac inverters. The standpoint of the impedance-source networks; the fed may be current-fed or voltage-fed. Moreover, the classification of impedance network depend on the magnetics used in this topology so, it has divided into transformer based or coupled inductor [54]–[69] and nontransformer based [33]–[53].

A novel research field in power electronics has been opening because of the Z-source concept. A lot of improvements and modifications have been introduced on the former Z-source topologies. Unique properties and applications have found in every topology in order to be more appropriate in terms of use. The new Z-source topology is expected to continue forward to meet and enhance the work of the converter in various applications. The future applications of Z-source converters to generate the power will be with renewable energy because Z-source converters have a unique feature of voltage buck–boost efficiency, least element count, and probably low cost. Also, the performance of Z-source converters will be absolutely improved with new devices of power electronic, as gallium nitride (GaN) and silicon carbide (SiC) devices [21], [22]. Actually, Z-source networks have been still advancing in applications and topologies.

1.4 The General Aspect of Impedance-Source Network

The general design of an impedance-source network for electric power convention can be represented in Figure 1.2, with various switching cells depending on design requirements.

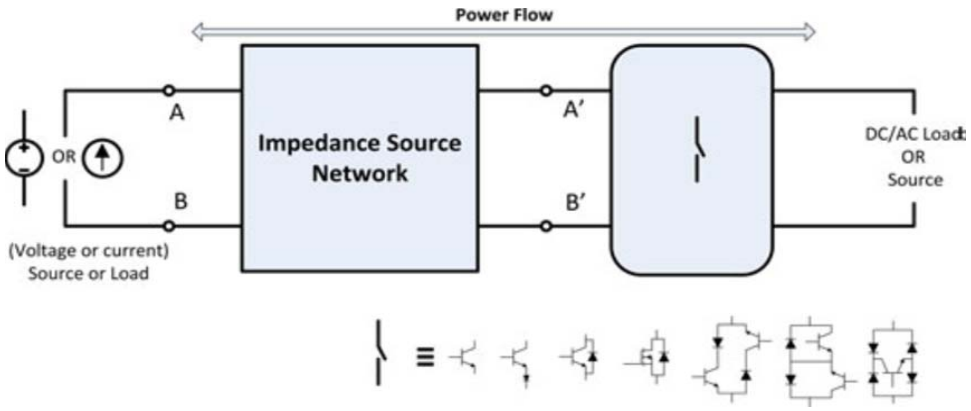


Figure 1.2: The general design of impedance-source network for electric power convention.

The basic design of impedance source network is formed mainly from two main elements combined to store energy linearly, i.e., C and L (generally, element (R) is neglected). Even though the improved performance of the impedance-source network can be done with various configurations of the circuit by inserting different nonlinear components to the network, e.g., switches, diodes, and/or both of them.

Originally, the main reason to create the impedance-source network was to bypass certain weaknesses in the current-source inverter(CSI) and voltage-source inverter (VSI) that are usually applied to electric power conversion [1][2],[4]-[7]. In the voltage-source inverter (VSI), the output voltage (ac) is limited lower than the input voltage, i.e., the topology of the VSI is a type of buck inverter that does not provide the demand for distributed generation. Therefore, to get a desired ac output voltage, it needs to add dc-dc boost converter that makes the system more cost and the efficiency will be lower. In addition, electromagnetic interference may be at risk of getting in the switching devices and the switching devices may be destroyed at the short circuit across the inverter bridge.

Furthermore, the output voltage in the CSI is more than the voltage at the input. In the applications to get the desired output voltage, it needs an additional dc-dc buck converter. In addition, the lower and upper switches of the inverter must be gated on at any time. On the other hand, the devices may be destroyed when the dc inductor will be open circuit.

To benefit the features of the impedance source network, various switching design has been adopting and modulating with different types of control methods and pulse width modulation (PWM) to correspond with the needs of the different application. The range technique of pulse width modulation (PWM) and start from simple-single switch topologies to matrix configurations [23]–[32].

The aforementioned of the concepts and theoretical limitations of the classic CSI and VSI have been fixed when the impedance-source converter has invented. The impedance-source converter gives a new principle in power conversion. This topology has the best feature which operates such as I-source or V-source according to the needs and the applications, and the output range of the voltage will be from 0 to ∞.

Since the first invention of the impedance-source network in the year 2002, titled a “Z-source network” [1], a lot of modification and improvement in the

topologies and modulation methods have been invented and published to enhance the implementation of different applications [2]–[25].

The general design of Z-source network as shown in Figure 1.3 consists of two capacitors C_1 and C_2 and two inductors L_1 and L_2 linked between two legs as X shape that present as a buffer among source and load (current or voltage source).

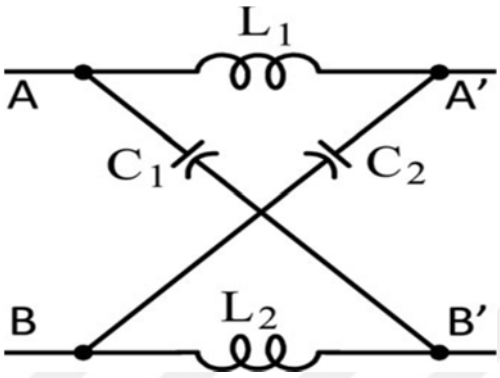
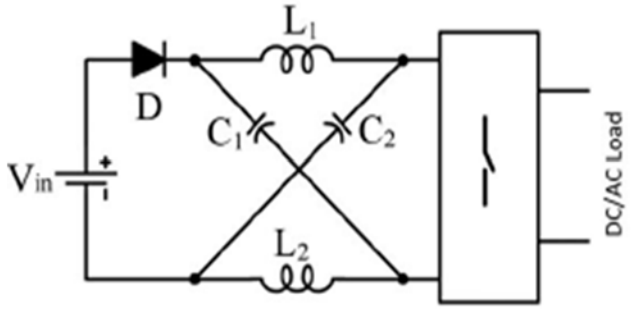


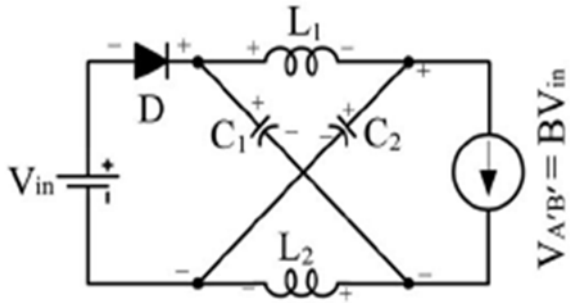
Figure 1.3: The general design of Z-source impedance network.

1.5 The General Principle of Operating Impedance-Source Converter

All power conversions ac-to-ac, ac-to-dc, dc-to-ac, and dc-to-dc can be achieved by the new topology of the impedance-source network. The dc source and/or load can be either a current or voltage source and/or a load. A Z-source impedance network can be taken as a sample to briefly explain the principle of operating and control technique of the impedance-source network. Figure 1.4 shows the general diagram circuit of the Z-source converter and the equivalent circuit at an active state and the equivalent circuit at shoot-through state.



(a)



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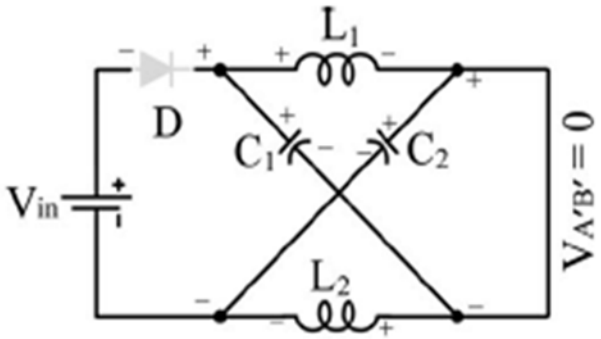

(c)

Figure 1.4: Voltage-fed of the (a) general diagram circuit of the Z-source converter at (b) active (c) shoot-through states.

The terminals of output A' and B' for the impedance network during the period of shoot-through will be short-circuited by upper and lower switch or a combination of switches which will make the diode in the network working reverse-bias. At this period of the shoot-through state, the energy storage in the capacitor and inductor will transfer to the load through the following stage of the active state, and at this time the diode returns to conduction.

The switching circuit considered from the dc side at the period of the active state is similar to a current source as shown in Figure 1.4 (b). From these two switching states, the averaging is resulting in a term to calculate the peak dc-link

voltage$V_{A',B'}$, on the terminals A' and B', in the expression of its input voltage V_{in} as:

$$V_{A',B'} = \left(\frac{1}{1-2D}\right) V_{in} = BV_{in} \tag{1.1}$$

where (D) is the partial shoot-through time in a switching period, called duty cycle (D).The allowable range of D is ($0 \le D < 0.5$).

The period of the shoot-through state is prevented in the conventional VSI because of the possibility of the short circuit at the terminal of the dc link which leads to destroying the converter. Power conversion systems have been gained a unique feature of buck–boost topology from the network of Z-source inverter and the period of shoot-through zero state and the improvement in the modulation index. Theoretically, the ac output from the inverter (as shown in Figure 1.4 a) is [2]:

$$V_{ac} = MB\frac{V_{in}}{2} = M\left[\frac{1}{1-2D}\right]\frac{V_{in}}{2} \tag{1.2}$$

Therefore it can provide any value from 0 to ∞. All the schemes of the conventional PWM are valid to control the impedance source network and the relationships of theoretical output-input still true. Also, a novel state has been added to all the traditional modulation techniques, named a “shoot-through state”, which is and included with the modulation strategy of power conversion systems without infringement of the volt-sec balance in the principle of operating. Because of this unique property of the shoot-through states, many modifications of new PWM techniques have been developed as sine PWMs and space vector modulation [23]–[32] to control the output voltage.

1.6 Brief Explanation of the Main Aspects of the Proposed Typology and its Importance

The general aspects and operating principles that mentioned above are a preface to study the proposed topology which will be detailed later. İn this work will combine two impedance networks, the conventional ZSI, and the SL. The reason for this combination is to overcome the problems found in the conventional ZSI and invention new type of impedance source networks. In general, the circuit of SL consists of inductors and diodes as shown in Figure1.5. In this work, there will be two proposed circuits. The first circuit will contain one cell of SL combined with the

conventional ZSI by one switch. An SL can be a series of extended cells that will increase the circuit's advantages as needed. The second proposed circuit will contain two cells of the SL combined with the conventional ZSI by two switches. Each cell of SL consists of two inductors and three diodes. Therefore, the total number of the circuit SL will be four inductors and six diodes. The circuit shape of the SL is similar to X-shape and called “X-shape SL”. A switched inductor X-shape SL can be a series of extended cells that will increase the circuit's advantages as needed.

The problems of discontinuous input current, higher voltage stress on the capacitor and lower boost factor that faced the conventional ZSI will solve by combining the two networks. The origin of the idea is to exploit the period of the shoot through state. This is done when the conventional ZSI separates from the source during the period of the shoot through (as explained above); therefore the cells of SL or X-shape SL will work to store the energy. The switches devices work only at shoot through state. During the shoot through period, the inductors are linked in parallel with the source, thus each inductor will take the same voltage source value. However, during the active state, the inductors are linked in series with the source and conventional ZSI and will add stored energy from the previous period to the circuit. The stored energy that will be paid to the circuit will be more than double the source value. Therefore, there will be an improvement in:

1. Continuous input power.
2. A wide range of gain voltage.
3. Raised boost factor.
4. Decreased stress on the capacitor.
5. Decreased size of the capacitor.
6. Decreased duty cycle.
7. Decreased thermal losses inside the switching.

In addition, the design of the capacitors and inductors will be accurately not randomly in accordance with derivative equations.

This new type of impedance source network will be of the nontransformer type and dc-ac inverter. All mentioned above are detailed in subsequent chapters.

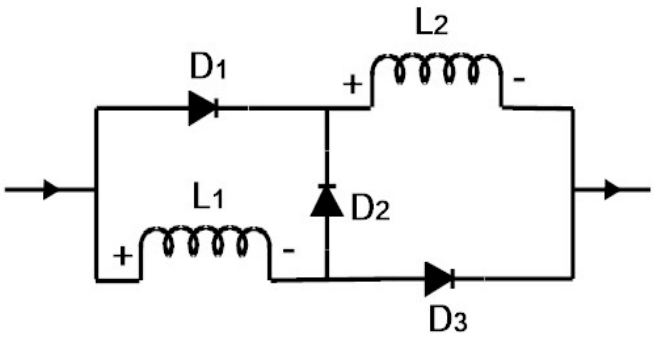

Figure 1.5: One cell of switched inductor (SL).

1.7 The Organization of the Next Chapters

a) The second chapter will include the literature survey of all types of impedance–source network and include the main classifications of the impedance network. Chapter two will explain the theory of each topology in terms of composition, work technique, and its pros and cons. And gives a summary for all topologies.

b) The third chapter will explain the appropriate design of the capacitors and inductors for the proposed circuits SL&ZSL and X- shape SL&ZSI according to the derived equations.

c) The fourth chapter consists of three parts:

1- Analysis the proposed circuit of SL&ZSL theoretically.

2- Design the proposed circuit of SL&ZSL according to the equations in chapter two.

3- Implement simulation for the proposed circuit.

After each part, the results will be discussed and compared with each other.

d) The fifth chapter also consists of three parts:

1- Analysis the proposed circuit of X-shape SL&ZSI theoretically.

2- Design the proposed circuit of X-shape SL&ZSI according to the equations in chapter two.

3- Implement simulation for the proposed circuit.

After each part, the results will be discussed and compared with each other.

e) The sixth chapter will include the conclusions.

CHAPTER TWO

IMPEDANCE-SOURCE NETWORK TOPOLOGIES

2.1 Introduction

All varieties of power converter topologies with impedance source networks have been fundamentally extracted from the topology of Z-source network via amendment of the fundamental impedance network or via rearrangement of the links of capacitors and inductors [33]–[69]. Every Z-source network topology has given unique properties for various or special Application requirements. The Development in topologies Z-source has been continued, at most because four reasons:

1) Decreasing the component rating and count of the Z-source network.

2) Increasing the gain range of voltage.

3) Obtaining higher power.

4) Improvement of optimization application.

Moreover, by combining conventional switched-capacitor, switched-inductor, tapped inductor, capacitor-assisted extension, and diode-assisted with the Z-source or quasi-Z-source network, the voltage in the network impedance will be increasing; however, the circuit needs more elements.

In general, the classification of impedance network (as shown in Figure 2.1) based on the magnetics used divided into [3]:

1) Nontransformer based

2) Coupled or transformer based

Every topology has special properties and will be explained shortly in the following sections.

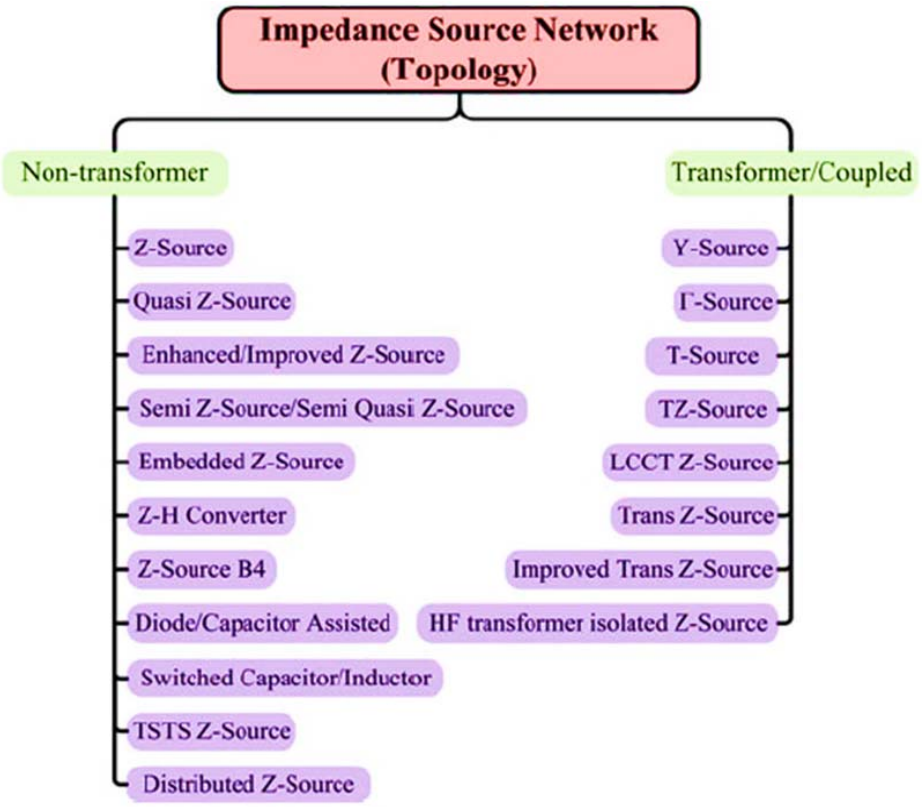

Figure 2.1: General classification of impedance network based on the magnetics (as of Sept. 2013).

2.2 Non-transformer Based

1. Z-source and Quasi-Z-source:

In general, Z-source converters have been divided two categories: current-fed and voltage-fed. However, in contrast the conventional voltage-fed /current- fed inverter, the impedance source network acts as a buffer among the dc-link inverter and the source and helps the process of an open and a short circuit of impedance network at any time according to the operation technique. The problems in conventional Z-source networks are the suffering from discontinuous input current when the diode is in the state of reverse bias. Different current- and voltage -fed topologies extracted from ZSI and qZSI with enhanced the execution have proposed in [33]–[36] to fix the suffering of ZSIs [35], [36]. It should be referred that all three currents-fed of ZSIs be able of the buck–boost mode and bidirectional power flow, though the switches devices must be reverse-blocking. These new advantages from this topology have been used in applications of motor drives and renewable energy generation [33], [34], [1]–[25].

2. Enhanced/Improved Z-source:

In this amazing race to raise the efficiency of impedance source networks, different alterations have been made on the Z-source and quasi-Z-source networks. At the same pace, to improve the boost of ZSI has been proposed in [37] and [38] with alternate tapped-inductor and cascaded switched cells using some less rated elements.

Likewise, an enhanced Z-source [39], [40] and an enhanced trans-Z-source [65] has been proposed, sequentially, to decrease the voltage stress on the capacitor. To fix some of the suffering facing the conventional ZSI and qZSI, effective topologies have been invented. However, the circuit has required adding more components for implementation. Therefore, the circuit will be expensive and the power density of the converter will reduce.

3. Semi-Z-source /Semi-Quasi-Z-source:

"Semi-ZSIs" have invented to reduce cost and to achieve an increase in efficiency of applications as single phase grid-tie PV power systems. A Semi-ZSI achieves a voltage boost duty with only two active switches and the ground feature is double (both ac output and PV panel are grounded) [41], [42]. A period of the shoot through state is not used to a Semi-ZSI, on the contrary, the traditional ZSI/qZSI.

The improved PWM method has been used to obtain the required duty cycle D that gives sinusoidal output voltages. Using a few switches devices the "Semi-Z-source and Semi-qZSIs" [43] can be operated if compared to a conventional ZSI and qZSI so this is an advantage of this topology, however the increase of the voltage stress on the switching devices is the drawback of this circuit.

4. Embedded Z-source:

In order to achieve continuity of input current, reduce the rate of capacitor voltage and feature multisource which mostly appropriate for PV power generation, the "embedded Z-source" topology was invented [44][45].

5. Z-H Converter:

A novel topology of power converter system was invented by [46], with similar in impedance source networks to the Z-source network but, the connections are different. In this topology, the diode of the input side and the period of the shoot-through have been removed from this proposed topology. This proposed topology and traditional Z-source network are similar in the gain; however, Z− H topology has

two operation technique, i.e., positive output voltage when boost mode in duty cycle D= [0, 0.5] and negative output voltage when boost mode in duty cycle D= [0.5, 1]. This topology can be used to ac-ac, ac-dc, dc-ac, and dc-dc in power conversion.

6. Z-source B4 Converter:

This topology has been deduced from the conventional B4 VSI. A “Z-source B4 Converter” has invented in [47] to improve the reliability and getting of lower cost with making a few active components.

7. Switched Inductor/Capacitor:

The main purpose of this topology is increasing the boost capability in the circuit of impedance network by adding extra capacitors and inductors to Z-source impedance network and quasi-Z-source impedance network. A lot of proposed topologies have been invented and mentioned in the literature to decrease the passive components stress and to remove the inrush current in the start-up. Thus, the topology of switched inductor or capacitor ZSI/qZSI has been invented for continuity of input current and reduces the stress of capacitor voltage [48]–[51]. Embedding switched inductor with Z-source inverter will produce many benefits, e.g., decrease the stress of capacitor voltage, getting a high ratio of boosting, and input ripple current will be low [52]. However, in this topology the number of the components will increase therefore the cost will be rising and size of the converter will be large.

8. Capacitor/Diode Assisted:

Extension of the circuit impedance source network is by adding the diodes and capacitors called “Capacitor/Diode Assisted”. This topology has been proposed in order to approach from the applications desiring of very high voltage boost [53], [54]. The rising voltage gain and decreasing the stress on the capacitor are the advantages of this topology, but the disadvantage of this topology is the increasing cost because of extra elements.

9. Three-Switch Three-State (TSTS) Z-source:

This topology called “Three-Switch Three-State (TSTS) Z-source” because it has three switches to operate three states in the same circuit. This topology has been invented recently by [55] and distributed into two categories: “buck-boost-TSTS-ZSI” and “boost-TSTS-ZSI”. Moreover, if this topology of “three-switch three-state (TSTS) Z-source” is compared with conventional impedance-source topologies, the numbers of switches devices used in this circuit will be less, and the advantage of

this topology is a higher level of power density and the minimum stress voltage. This circuit used duple grounds that make the PV power generation more reliable.

10. Distributed Z-Source:

Designs such as hybrid LC elements and transmission lines are models of impedance source network called “Distributed Z-Source” in [56], [57]. The implementation of distributed Z-source networks topology may be difficult; however, in this topology of the distributed ZSI, no extra switches or diodes have been found which can obtain the duty of voltage boost.

2.3 With Transformer or Magnetic Coupling

Impedance source networks have found a niche for a new feature of transformers and magnetically coupled inductors to enhance the capability of voltage boost and modulation index. In addition, this feature of the transformers or magnetically coupled inductors topology has reduced the elements that the circuit does not need; also this technology has resulted in enhanced power and reduced cost. The description of the impedance transformer or coupled inductor network topologies will be in the following sections.

1. Y-Source:

By using three windings (N_1, N_2 and N_3) and coupled inductors have been obtained a unique feature of impedance network titled “Y-source network” and presented in [58]. In this topology of Y-Source, there is no match in the profit with currently networks that run at the same duty ratio. The more degree of freedom (duty cycle and three windings) have been found in this proposed topologies of Y-Source to get the desired voltage boost if compared with conventional impedance network. In theory, by setting the turn's ratio and the period of shoot-through, the topology of Y-Source is got the desired magnitude of the voltage.

2. Γ-Z-Source:

Γ-Z-Source is an unparalleled topology. Γ-Z-Source topology has shape consisting of two coupled winding transformer [59], [60] to extend the modulation ratio M and the gain together, whilst the elements number will decrease. The other topologies of the basic impedance networks transformers are on the contrary of this proposed technology of Γ-Z-Source. The former topologies e.g., “Trans-Z-source, T-source, TZ-source or inductor–capacitor–capacitor–transformer Z-source inverters

(LCCT Z-source)" will increase the rate of gain at the expense of increasing the turns ratio, whereas the new topology (Γ-Z-Source) on the contrary, it will increase the rate of gain while reducing the turns ratio.

3. T-Source:

The T-source topology has form also consisting of one capacitor and two coupled inductor winding [61], [62]. By adjusting the turn's ratio of transformer T-Source on greater than 1, the earning T-Source will be higher than the conventional ZSI and qZSI.

4. Trans-Z-Source:

In theory, most of the above-mentioned impedances networks generate a wide range of the voltage earning. In practice, when the earning is high (2 or 3) there will be high stress on the switches. The innovative topology of Trans-Z-Source has been invented to get high earning with lower stress on the switches and decrease the coupled inductor to one [63]–[65].

5. TZ-Source:

Also in this topology of TZ-Source, by adjusting the turn's ratio of transformer T-Source on greater than 1, earning voltage will be high [66]. Because it needs four coupled inductors, this topology will be not valid to decrease the elements and size.

6. LCCT Z-Source:

The integration between the winding of transformer and inductor has founded a novel topology called "LCCT Z-Source". This topology produces bigger modulation index and gain [67], [68].

7. HF Transformer-Isolated Z-Source/Quasi-Z-Source/Trans-Z-Source:

Applications that need the insulation for safety has been used HF isolation topology with all the families of impedance-source [69]. All previous inheritance has the advantages of high boost and little stress on the devices which had been discovered in HF Transformer Isolated topology. But the disadvantages of this topology are the use of more elements. Of the terms of this topology is the correct design to minimize the leakage.

Table 2.1: Synopsis of impedance network topology.

Impedance Network Topology	Boost Factor	Voltage Stress on the Switching Device	No. of Semiconductors	No. of Capacitors	No. of Inductors	Features
Z-Source[1]	$B = [1-2D]^{-1}$ Where, $0 \le D \le 0.5, V_0 > 0$	$\frac{1}{1-2D} V_{In}$	1diode	2	2	- Elementary circuit to overcome the conceptual and theoretical barrier of VSI and CSI that leads to many useful derived topologies - Discontinuous input current and higher voltage stress on capacitors. -The inductors of current-fed ZSI must sustain high current.
Quasi Z-Source [36]	$B = [1-2D]^{-1}$ Where, $0 \le D \le 0.5, V_0 > 0$	$\frac{1}{1-2D} V_{In}$	1diode	2	2	-First modification of Z-Source network - Continuous input current. - Reduced passive component ratings. -Reduced component count.
Improved Z-Source [41]	$B = [1-2D]^{-1}$ Where, $0 \le D \le 0.5, V_0 > 0$	$\frac{1}{1-2D} V_{In}$	1diode	2	2	-Reduced capacitor voltage stress. -Limit inrush current at startup.
Semi Z-Source[41], [42]Semi Quasi Z-Source [43]	$B = [1-2D]/[1-D]$ Where, $V_o > 0, For\ 0 \le D \le 0.5, Buck\ and\ V_o < 0,$ $\begin{cases} 0.5 < D < 2/3, Buck \\ 2/3 < D \le 1, Boost \end{cases}$	$\frac{1}{1-D} V_{In}$	2 Switches	2	2	-Reduced active components count. -Lower cost - Higher voltage stress across switches compared to ZSI/qZSI. -Eliminate leakage currents and suitable for grid-connected PV system.
Embedded Z-Source [44],[45]	$B = [1-2D]^{-1}$ Where, $0 \le D \le 0.5, V_0 > 0$	$\frac{1}{1-2D} V_{In}$	1diode	2	2	-Draws smooth current from the source without adding additional components or passive filter.

Table 2.1 (Continue): Synopsis of impedance network topology.

Impedance Network Topology	Boost Factor	Voltage Stress on the Switching Device	No. of Semiconductors	No. of Capacitors	No. of Inductors	Features
Enhanced Z-Source [37]	SL Cell:$B = \frac{1+(y_{SL}-1)D}{1-(Ny_{SL}-1)D}$ Where, $0 \le D \le \frac{1}{Ny_{SL}+1'}$ $V_o > 0$	$\frac{1+(y_{SL}-1)D}{1-(Ny_{SL}+1)D}V_{In}$	$N + 3(y_{SL} - 1)$ Where, N is no. of cascaded n/w	2N	$y_{SL}(N+1)$	-Higher voltage conversion compared to ZSI/qZSI at small shoot-through duration -Increases the number of components (low power rated).
	TL Cell $B = \frac{1+y_{TL}D}{1-[1+N(y_{TL}+1)]D}$ Where, $0 \le D \le \frac{1}{1+N(y_{TL}+1)'}$ $V_o > 0$	$\frac{1 + y_{TL}D}{1 - [1 + N(y_{TL} + 1)]d_{ST}}V_{In}$	$N + 2(y_{SL} - 1)$ Where, N is no. of cascaded n/w	2N	(N+1), each with turns rate γ_{TL}	
Z-H Converter [46]	$B = [1 - 2D]^{-1}$ Where$0 \le D \le 0.5\ For V_0 > 0$ And $0.5 \le D \le 1\ For V_0 < 0$	$\frac{1}{1-2D}V_{In}$	4 Switches	2	2	- Front-end diode is eliminated. - No shoot-through state for voltage boosting.
Z-Source B4 [47]	$B = [1 - 2D]^{-1}$ Where, $0 \le D \le 0.5, V_0 > 0$	$\frac{1}{1-2D}V_{In}$	1 diode	2	2	-Reduce the number of active semiconductors. - Simplify the control and gating circuitries.
Y-Source [58]	$B(k, D) = [1 - kD]^{-1}$ Where $k \ge 2\ and\ 0 \le D \le \frac{1}{k'}V_0$	$\frac{k-1}{1-kD}V_{in}$	1 diode	1	Integrated three windings	- Versatile. - More degree of freedom to choose the gain of the converter - Very high gain can be achieved with small shoot-through duty cycle. - Higher voltage boost and higher modulation index can be achieved simultaneously. - Reduce THD of the inverter
Γ-Source [59]-[60]	$B = [1 - (1 + [n-1]^{-1})D]^{-1}$ Where,$0 \le D \le [1 + [n + 1]^{-1}]^{-1}\ and\ 1 < n < 2(decreasing), V_0 > 0$	$\frac{1}{n-1\left\|1-\left(1+\frac{1}{n-1}\right)D\right\|}V_{In}$	1 diode	2	One inductor and one 2-winding coupled inductor	- Higher gain can be achieved by lowering the turns ratio of coupled inductor - Better spectral performance at the inverter output.

Table 2.1 (Continue): Synopsis of impedance network topology.

Impedance Network Topology	Boost Factor	Voltage Stress on the Switching Device	No. of Semiconductors	No. of Capacitors	No. of Inductors	Features
T-Source [61],[62] Trans Z-Source [63]-[65]	$B = [1-(n+1)D]^{-1}$ Where, $0 \le D \le [n+1]^{-1}, V_0 > 0$	$\frac{n}{1-(1+n)D}V_{In}$	1 diode	1	Integrated two winding	-Increases voltage gain compared to ZSI and qZSI. - Fewer reactive components compared to ZSI and qZSI. - Common ground with the load. - Reduced component stress.
TZ-Source[66]	$B = [1-(n+1)D]^{-1}$ Where, $0 \le D \le [n+1]^{-1}, V_0 > 0$	$\frac{n}{1-(1+n)D}V_{In}$	1 diode	2	Two integrated 2- windings	-Produce higher voltage boost with N.
LCCT Z-Source [67],[68]	$B = [1-(n+1)D]^{-1}$ Where, $0 \le D \le [n+1]^{-1}, V_0 > 0$	$\frac{n}{1-(1+n)D}V_{In}$	1diode	2	One inductor and one 2-winding coupled inductor	- Continuous input current even during light load - Filters out high-frequency ripple from the input current.
HF Transformer Isolated [69]	$B = [1-2D]^{-1}$ Where, $0 \le D \le 0.5, V_0 > 0$	$\frac{1}{1-2D}V_{in}$	1 diode 2 diode	4	Two integrated 2- windings	- Input-output isolation - Lower device stress
Diode/ Capacitor assisted Z-Source, QZS[53], [54]	Diode Assisted: $B = [(1-D)(1-2D)]^{-1}$ Where, $0 \le D \le 0.5, V_0 > 0$	$\frac{1}{1-D}V_{in}$	3 diode	3	3	- Higher voltage boost and lower voltage stress across the capacitor compared to ZSI/qZSI - Number of passive and active components increases with number of stages
	Capacitor Assisted: $B = [1-3D]^{-1}$ Where, $0 \le D \le 0.33, V_0 > 0$	$\frac{1}{1-3D}V_{in}$	2 diode	4	3	
Switched Inductor [48]-[52]	$B = (1+D)/[1-3D]^{-1}$ Where, $0 \le D \le 0.33, V_0 > 0$	$\frac{1+D}{1-3D}V_{in}$	7 diode	2	4	-Higher voltage boost and lower voltage stress across the capacitor compared to ZSI/qZSI. -Number of components increases with corresponding size and cost.
TSTS Z-Source [55]	Boost $B = \frac{2D_2-1}{1-D_1}$	$(2+K)V_{In}$	3 Switches	2	3	-Reduce the number of active semiconductors. - Buck-boost capability. - Common ground - Lower device stress. - Higher power density
	Buck-Boost $B = 1 + \frac{1-2D_2}{1-D_1}$	$(1+K)V_{In}$	3 Switches	2	3	

CHAPTER THREE

DESIGNING THE SIZE OF CAPACITOR AND INDUCTOR FOR SWITCHED INDUCTOR (SL) AND Z-SOURCE INVERTER (ZSI)

3.1 Introduction

The goal of most published work in the area of impedance source network is to maximize the ratio of boost voltage while reducing the stress of its components. However, the subjects of designing the impedance source network of the ZSI and the operation modes in steady state are published in limited numbers.

The five possible operational states have been identified by Shen and Peng [32] when the inductance will be low. However, to get a large capacitance must be still assumed, and to calculate the critical values of capacitance and inductance below which would appear undesirable operating modes, there is no procedure proposed. Therefore the inductor and capacitor are assumed to differ over a wide range, and the nonlinear waveforms are considered in [70]. So, there are six possible operating states showed in systematically. However, a guideline to find the size of capacitor and inductor has not presented until 2010 by Sumedha Rajakaruna and Laksumana Jayawickrama, so that ZSI will not operate in the unwanted operating states. Sumedha Rajakaruna and Laksumana Jayawickrama have been founded designing guideline [71], after describing the steady state operation of the impedance source network in a clear analysis. They also put equations to how to calculate the critical values of capacitance and inductance. Also Ting Wang, Yu Tang and Yaohua He have been put a guideline to how to calculate the network of SL [72].

This study will derive from these research papers a guideline to design our proposed topology for SL and ZSI as the following section.

3.2 Designing the Z-Source Network in the Proposed Circuit

Figure 3.1 represents the general design for new proposed topology and all the parameters of ZSI network are mentioned in this figure.

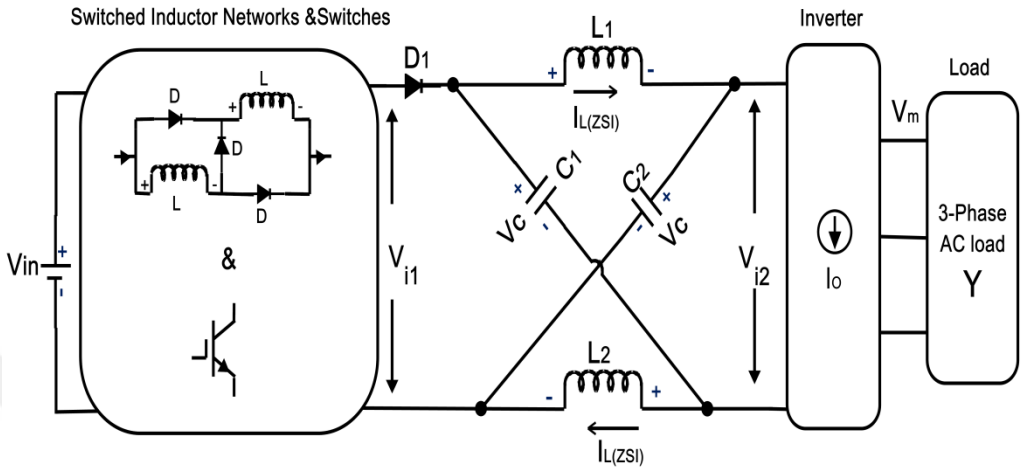

Figure 3.1: General design for new proposed topology.

3.2.1 Simple-Boost Control Techniques

The relationship between modulation index M and duty cycle D for simple-boost control [2], is

$$M = 1 - D \tag{3.1}$$

$$V_m = \sqrt{2}\, V_{L\text{-}L} \big/ \sqrt{3} \tag{3.2}$$

V_m is the output value of peak phase voltage (peak value of line to neutral)

$$I_m = \frac{V_m}{R_{load}} \tag{3.3}$$

I_m is the output value of peak phase current (peak value of line to neutral)

The constant current source on the input terminals of the VSI is I_0.

$$I_0 = (3/4)\, I_m \cos\phi. \tag{3.4}$$

$$\overline{V}_{i2} = 2\, V_m / M \tag{3.5}$$

($\overline{V}_{i2}$) is the average value of dc-link voltage.

$$D = \frac{(2V_m - V_{il})}{(4V_m - V_{il})} \tag{3.6}$$

$$\overline{V}_c = 2V_m \tag{3.7}$$

($\overline{V}_c$) is the average value of capacitor voltage.

$$\bar{I}_{IZSI} = (2V_m I_0 / V_{i1}) \tag{3.8}$$

($\bar{I}_{IZSI}$) is the average value of inductor current.

$$\Rightarrow C = \frac{3T_S I_m \cos\phi (2V_m - V_{i1})}{8K_V V_{i1}(4V_m - V_{i1})} \tag{3.9}$$

$$\Rightarrow L = \frac{2V_{i1}T_S(2V_m - V_{i1})}{3K_i I_m \cos\phi (4V_m - V_{i1})} \tag{3.10}$$

Therefore, the size of inductance and capacitance can be easily done with (3.9), (3.10) for simple-boost control.

3.2.2 Constant-Boost Control Techniques

The relationship between modulation index M and duty cycle D [2] for constant-boost control techniques, is

$$M = 2(1-D)/\sqrt{3}. \tag{3.11}$$

$$I_0 = (\sqrt{3}/2) I_m \cos\phi \tag{3.12}$$

$$D = \frac{(\sqrt{3}V_m - V_{i1})}{(2\sqrt{3}V_m - V_{i1})} \tag{3.13}$$

$$\overline{V}c = \sqrt{3}V_m \tag{3.14}$$

$$\bar{I}_{IZSI} = (\sqrt{3}V_m I_0 / V_{i1}) \tag{3.15}$$

$$\Rightarrow C = \frac{\sqrt{3}T_S I_m \cos\phi (\sqrt{3}V_m - V_{i1})}{4K_V V_{i1}(2\sqrt{3}V_m - V_{i1})} \tag{3.16}$$

$$\Rightarrow L = \frac{V_{i1}T_S(\sqrt{3}V_m - V_{i1})}{\sqrt{3}K_i I_m \cos\phi (2\sqrt{3}V_m - V_{i1})} \tag{3.17}$$

Therefore, the size of inductance and capacitance can be easily done with (3.16), (3.17) for constant-boost control techniques

3.3 Designing Switched Inductor Network in the Proposed Circuit [72]

3.3.1 One Cell of Switched Inductor

Figure 3.2 focuses on the ON and OFF state modes for boost converter SL and how is connected with ZSI in general design to give new proposed topology. All the parameters of SL are mentioned in this figure.

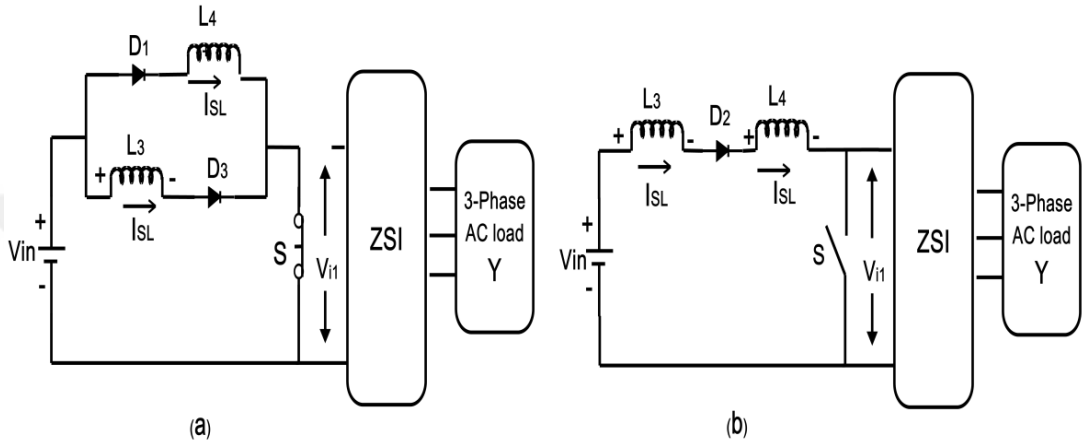

Figure 3.6:(a) ON state mode (b) OFF state mode of SL.

When the switch S is turned on and off, the equation will be:

$$L_{SL}\frac{\Delta i_{SL}}{DT_S} = V_{in} \tag{3.18}$$

The inductor current ripple Assume $\Delta i_{SL} = K_i I_{SL}$

$$L_{SL} = \frac{DV_{in}}{K_i I_{SL} f_s} \tag{3.19}$$

$$\Longrightarrow L_{SL} = L_3 = L_4 \geq \frac{D(1-D)RL}{K_i(1+D)f_S} \tag{3.20}$$

Therefore, the size of inductance for one cell of SL can be easily done with (3.20)

3.3.2 Two Cell of Switched Inductor

$$\Longrightarrow \quad L_{SL} = L_3 = L_4 = L_5 = L_6 \geq \frac{D(1-D)RL}{K_i(1+3D)f_S} \tag{3.21}$$

The size of inductance for two cell of X-shape of SL can be easily done with (3.21).

CHAPTER FOUR

THE PROPOSED TOPOLOGY FOR THE FIRST CIRCUIT: ONE CELL OF SWITCHED INDUCTOR (SL) COMBINED WITH ZSI

4.1 Introduction

This chapter will discuss the first circuit idea by combining one cell of SL with traditional ZSI and includes the following divisions: The first part is an analysis of the circuit and knowing the behavior of the passive and active components at the moment of the active state and shoot-through state. During the shoot- through state, the input energy will store in the SL and the stored energy in the capacitors of ZSI will be transferred into inductors. These processes occur after the reverse bias for some diodes. These behaviors will improve the proposed theory. The second part of this chapter contains the exact size design of each element in the circuit according to the mathematical equations mentioned in the third chapter. The third part is simulation the circuit by the multizim program. The last part of this chapter is the improvement that will occur in the circuit if expanded by adding extra cells of SL. After each part, there will be a discussion and comparison of the results.

4.2 The Analysis of Proposed Circuit Topology

The Z-source network composed of two inductors (L_1=L_2) and two capacitors (C_1=C_2) in addition to one diode D_1. While the switched inductor network composed of two inductors (L_3=L_4) and three diodes (D_2, D_3, D_4) which represents one cell of SL, as shown in Figure 4.1.

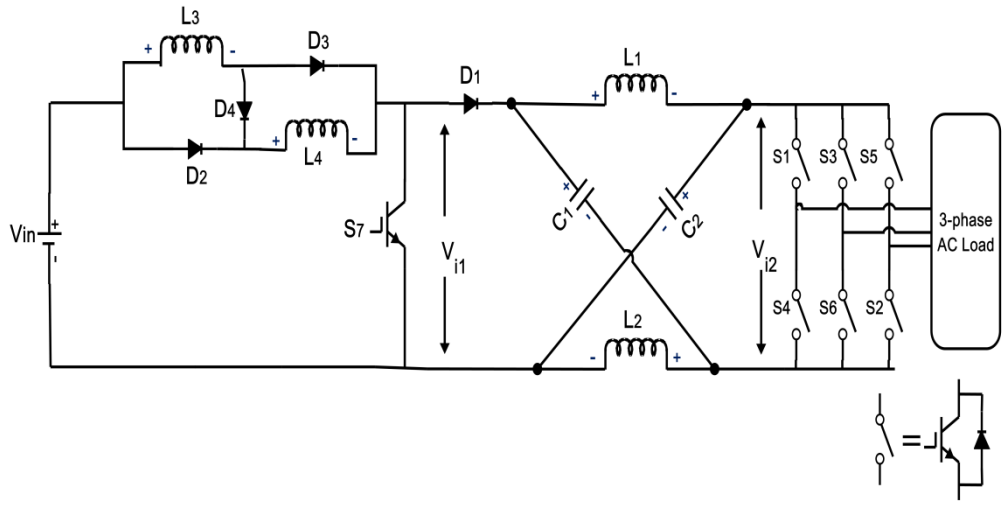

Figure 4.1: Switch inductor (SL) combined with traditional ZSI.

The operating principles of the proposed topology are also similar to those of the classical ZSI. For the purpose of analysis, the operating states are simplified into shoot-through and nonshoot-through states. Figure 4.2 shows the equivalent circuits of SL with the traditional Z-source inverter at nonshoot-through states.

In the nonshoot-through state, the behavior of switched inductor network will be as follows: D_4 is on, while D_2 and D_3 are off, L_3 and L_4 (L_3=L_4) are connected in series. L_3 and L_4 are transferring the energy from the dc voltage source to the Z-source network.

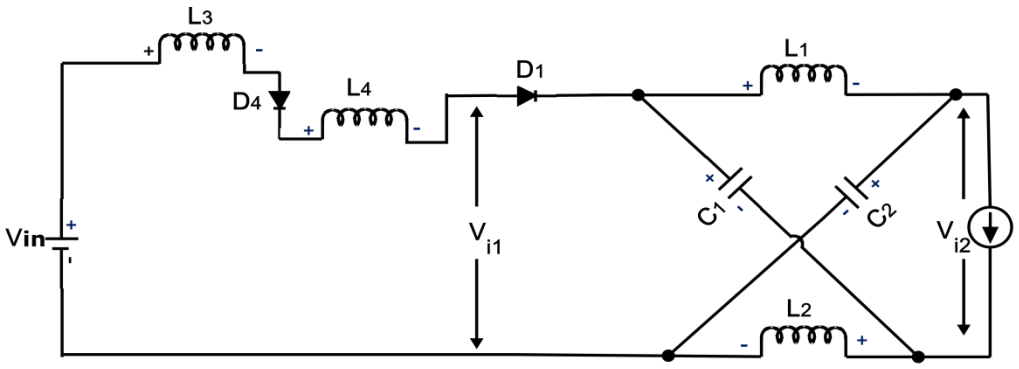

Figure 4.2 The switch (S_7) of one cell SL is OFF state.

The corresponding voltages across L_3 and L_4 in this state are V_{L3} and V_{L4}, respectively, will be:

$$V_{L3} + V_{L4} + V_{i1} = V_{in} \tag{4.1}$$

$$V_{L3} = V_{L4} \tag{4.2}$$

From 4.1, 4.2, the equation will be:

$$V_{L3} = \frac{1}{2} V_{in} - \frac{1}{2} V_{i1} = V_{L4} \tag{4.3}$$

For the Z-source network, D_1 is on, (L_1=L_2) and (C_1=C_2), so the Z-source network becomes symmetrical. From the symmetry and the equivalent circuit:

$$V_{C1} = V_{C2} = V_C, V_{L1} = V_{L2} = V_L \tag{4.4}$$

$$V_L = V_{i1} - V_C \tag{4.5}$$

$$\Longrightarrow \quad V_{i2} = V_C - V_L \qquad V_{i2} = V_C - (V_{i1} - V_C)$$

$$V_{i2} = 2V_C - V_{i1} \tag{4.6}$$

In the shoot-through state, the behavior of switched inductor network will be as following (as shown in Figure 4.3): D_4 is off, D_2 and D_3 are on and L_3, L_4 are connected in parallel.

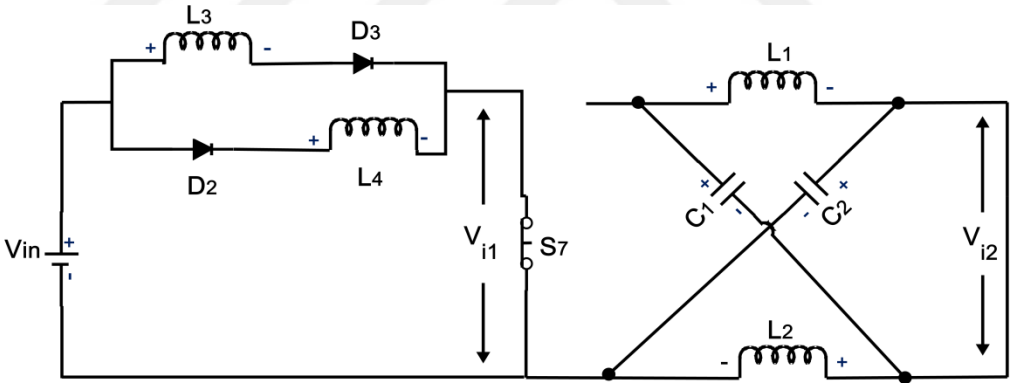

Figure 4.3: The switch (S_7) of one cell SL is ON state.

The equivalent circuit is:

$$V_{L3} = V_{L4} = V_{in}, V_{i1} = 0 \tag{4.7}$$

For Z-source network, D_1 is off, L_1 and C_1 are connected in parallel, L_2 and C_2 are connected in parallel. From the equivalent circuit:

$$V_L = V_C, V_{i2} = 0 \tag{4.8}$$

Where V_{in} is the input voltage for the SL network, V_{i1} is the input voltage for the Z-source network; T is the full switching cycle, T_1 is the non-shoot through

interval, T_0 is the shoot through interval, ($T=T_1+T_0$) and D is the shoot through duty cycle where ($D = \frac{T_o}{T}$).

Based on the volt-second balance principle, the voltage across the inductor L_3 and L_4 can be getting it in the two periods which were represented in (4.1, 4.2, 4.3 and 4.7). By setting the interval of the shoot-through state: DT, non-shoot through state: (l-D) T, subsequently:

$$(DT * V_{in}) + (1-D)T * \left(\frac{1}{2}V_{in} - \frac{1}{2}V_{i1}\right) = 0$$

$$DT * V_{in} = (D-1)T * \left(\frac{1}{2}V_{in} - \frac{1}{2}V_{i1}\right) \quad (4.9)$$

$$V_{i1} = \frac{1+D}{1-D}V_{in} = B_1 * V_{in} \quad (4.10)$$

$$B_1 = \frac{1+D}{1-D} \quad (4.11)$$

Where B_1 is the boost factor of the switched inductor network.

The average voltage of the inductors (L_1 and L_2) over one switching period (T) should be zero in steady state, from (4.5, 4.6, and 4.8):

$$\overline{V_L} = \frac{T_o V_C + T_1 (V_{i1} - V_C)}{T} = 0 \quad (4.12)$$

$$\frac{V_C}{V_{i1}} = \frac{T_1}{T_1 - T_o} \quad (4.13)$$

Similarly, the average dc-link voltage across the output of the inverter bridge can be:

$$V_{i2} = \frac{T_o * (0) + T_1 (2V_C - V_{i1})}{T} = \frac{T_1}{T_1 - T_o}V_{i1} = V_C \quad (4.14)$$

The peak dc-link voltage across the inverter bridge obtained as:

$$V_{i2} = 2V_C - V_{i1} = \frac{T}{T_1 - T_o}V_{i1} = B_2 * V_{i1} \quad (4.15)$$

Where:

$$B_2 = \frac{T}{T_1 - T_o} = \frac{1}{1-2D} \quad (4.16)$$

Where B_2 is the boost factor of the Z-source network.

By substituting 4.10 in 4.15:

$$\overline{V_{i2}} = \frac{1}{1-2D} * \frac{1+D}{1-D} V_{in} = \frac{1+D}{1-3D+2D^2} V_{in} \quad (4.17)$$

Where:

$$B = \frac{1+D}{1-3D+2D^2} \; ; \; D \leq 0.5 \quad (4.18)$$

The boost factor is resulting from the shoot through zero-state. The average dc-link voltage V_{i2} is the equivalent dc-link voltage of the inverter. On the other side the output peak phase voltage from the inverter can be expressed as:

$$V_{ac} = M \frac{V_{i2}}{2} \quad (4.19)$$

Where M is the modulation index. By using (4.17, 4.19) the peak phase voltage will be as follows:

$$V_{ac} = M * B \frac{V_{in}}{2} \quad (4.20)$$

$$V_{ac} = B_B \frac{V_{in}}{2} \quad (4.21)$$

$$B_B = M * B = (0 \sim \infty) \quad (4.22)$$

The buck-boost factor is (B_B).

(V_{ac}) is the output value of peak phase voltage (peak value of line to neutral) [2].

From (4.4, 4.13, and 4.16) the capacitor voltage can be expressed as:

$$V_C = \frac{1-D}{1-2D} V_{i1}$$

$$V_C = \frac{1+D}{1-2D} V_{in} \quad (4.23)$$

The boost factor B and modulation index adjust the factor of the buck-boost B_B. The boost factor as expressed in 4.18 can be determined by the duty cycle (i.e., interval ratio).

Figure 4.4 represented the improvement of the boost capability and comparing the proposed circuit of SL&ZSI with the traditional ZSI. The boost factor increased by combining one cell of SL with ZSI at a small value of duty cycle (D) comparing with a traditional Z-source inverter. The boost factor will increase by increasing the duty cycle. For example, in figure 4.4, the boost factor at D=0.25 was equal B=2 for the traditional ZSI. However, the boost factor at same duty cycle is 3.333 for the proposed topology. This means that the increase rate is 66.65%. In addition, the boost factor at D=0.4 is equal to 5 for the traditional ZSI while the boost factor at same duty cycle is 11.666 for SL&ZSI network. This means that the increasing rate is 133.32%.Therefore, the improvement for the boost factor clearly shows in Figure 4.4 for one cell of SL&ZSI.

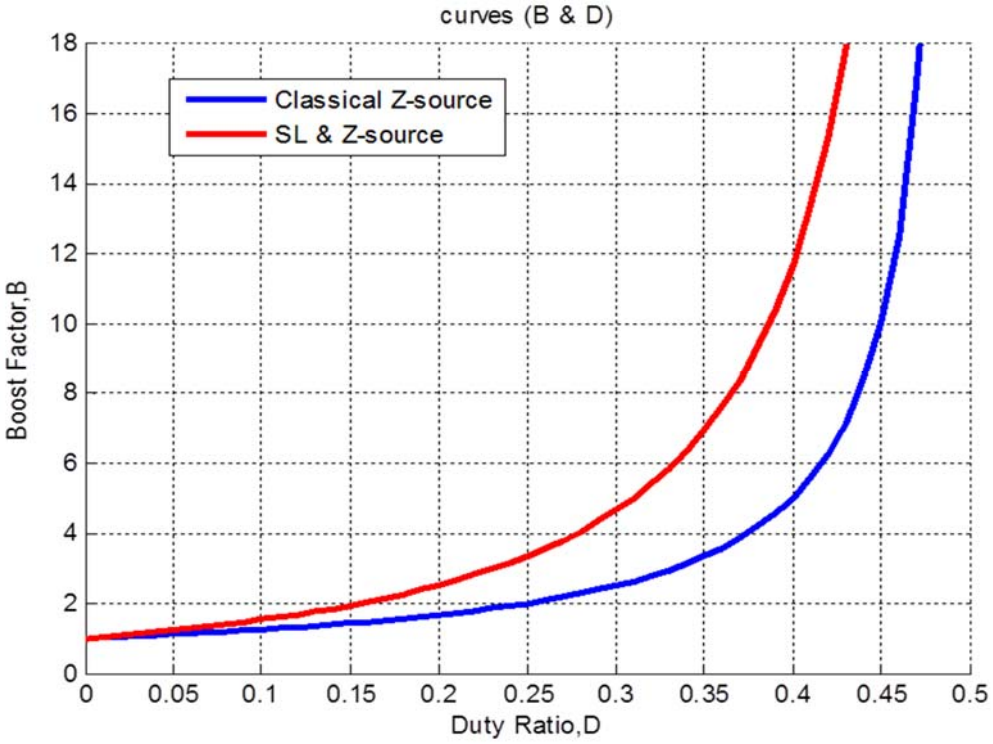

Figure 4.4: The comparison of boost factor for one cell SL&ZSI with traditional ZSI.

Moreover, the rate of the capacitor voltage stress will decrease for one cell of SL&ZSI comparing with the traditional ZSI (The rate of capacitor voltage stress will be explained in more details in section (4.3).

4.3 The Calculation of Proposed Circuit Topology Elements' Values

The input values for designing the proposed circuits are: V_{in} = 80 V, T_S = 10^{-4} sec (fz=10 kHz), $V_{L\text{-}L(RMS)} = 380\,V$, $Rl_{Load} = 10\Omega$.

1- Designing the traditional ZSI:

$$V_m = \sqrt{2}V_{L-L}/\sqrt{3}$$

$$\Rightarrow V_m = 310.27\,V$$

$$\overline{V}_{i1} = V_{in}$$

$$D = \frac{2V_m - \overline{V}_{i1}}{4V_m - \overline{V}_{i1}}$$

$$\Rightarrow D = 0.4655$$

$$M = 1 - D$$

$$\Rightarrow M = 0.5344$$

$$\overline{V}_{i2} = \overline{V}_{iA} = 2V_m/M$$

$$\Rightarrow \overline{V}_{i2} = 1161.2$$

$$\overline{V}_C = 2V_m$$

Or

$$\overline{V}_C = \frac{(1-D)}{(1-2D)}V_O$$

$$\Rightarrow \overline{V}_C = 619.6\,V$$

$$C = \frac{3T_S I_m \cos\phi\left(2V_m - \overline{V}_{i1}\right)}{8K_V V_{i1}\left(4V_m - \overline{V}_{i1}\right)}$$

$$K_V = 5\%$$

$$\Rightarrow C = 1.354 * 10^{-4}\,\mu F$$

$$L = \frac{2 V_{i1} T_S \left(2 V_m - \overline{V}_{i1}\right)}{3 K_i I_m \cos\phi \left(4 V_m - \overline{V}_{i1}\right)}$$

$K_i = 5\%$

$\Rightarrow L = 2.0672 * 10^{-3} mH$

$$B = \frac{1}{1-2D}$$

$\Rightarrow B = 14.4927$

$$V_{ac} = M * B \frac{V_O}{2}$$

$\Rightarrow V_{ac} = 309.8 V$

$\frac{\overline{V}_C}{V_{in}} = 7.745$ Stress ratio on the capacitor

2- Designing One cell of SL& ZSI:

$V_m = \sqrt{2} V_{L-L} / \sqrt{3}$

$\Rightarrow V_m = 310.27 V$

$$I_m = \frac{V_m}{R_{load}}$$

$\Rightarrow I_m = 31.027 A$

$$D = \frac{2 V_m - \overline{V}_{i1}}{4 V_m - \overline{V}_{i1}}$$

By subtracting equation 4.10 from this equation

$\Rightarrow D = 0.4091$

And substitute (D) in 4.10

➡ $\overline{V}_{i1} = 190.8 V$

$M = 1 - D$

$\Rightarrow M = 0.5909$

$$\overline{V}_{i2} = 2V_m/M$$

Or

$$\overline{V}_{i2} = \frac{1+D}{1-3D+2D^2} V_{in}$$

$$\Rightarrow \overline{V}_{i2} = 1050.1V$$

$$C = \frac{3T_S I_m \cos\phi\left(2V_m - \overline{V}_{i1}\right)}{8K_V V_{i1}\left(4V_m - \overline{V}_{i1}\right)}$$

$$K_V = 5\%$$

$$\Rightarrow C = 5*10^{-5}\,\mu F$$

$$L = \frac{2V_{i1}T_S\left(2V_m - \overline{V}_{i1}\right)}{3K_i I_m \cos\phi\left(4V_m - \overline{V}_{i1}\right)}$$

$$K_i = 5\%$$

$$\Rightarrow L = 3.35*10^{-3}\,mH$$

$$\overline{V}_C = 2V_m$$

Or

$$\overline{V}_C = \frac{1+D}{1-2D} V_O$$

$$\Rightarrow \overline{V}_C = 620.06V$$

$$B = \frac{1+D}{1-3D+2D^2}$$

$$\Rightarrow B = 13.116$$

$$V_{ac} = M*B\frac{V_O}{2}$$

$$\Rightarrow V_{ac} = 310.01V$$

(V_{ac}), (V_m) is the output value of peak phase voltage (peak value of line to neutral) [2][71].

$\frac{\overline{V}_C}{V_{i1}} = 3.249$ Stress ratio on the capacitor

$$\bar{I}_{lZSI} = \frac{2 V_m I_0}{V_{i1}}$$

$$\bar{I}_{lZSI} = 76\ A$$

$$L_{SL} = L_3 = L_4 \geq \frac{D(1-D)^2 RL}{K_i (1+D) f_S}$$

$$f_S = 10KH$$

$$\Rightarrow L_{SL} = 2*10^{-3}\ mH$$

From the design of the two circuits ZSI and one cell of SL&ZSI and theoretical results values that appeared, the proposed topology of one cell of SL&ZSI can be applied, because the values that have obtained were almost true, which proves the theory. For example, in equation 4.20 the peak phase voltage V_{ac} is 310.01V, and it is almost equal to V_m value, therefore the percentage of error between V_{ac} and V_m is very small and equal to 0.04%. So, the V_{RMS} value of phase voltage equals 219.21V and V_{RMS} value of line to line voltage equals 379.68V.

In addition, the design of traditional ZSI showed that the capacitor value was equal to $1.354*10^{-4}\ \mu F$ at D=0.4655 however, the proposed topology of one cell of SL&ZSI showed that the capacitor value decreased and became $5*10^{-5}\ \mu F$ at D=0.4091, whereas, the decrease rate is 63%. One of the aims of this research is to reduce the value of the capacitor. Figure 4.5 shows the difference between them.

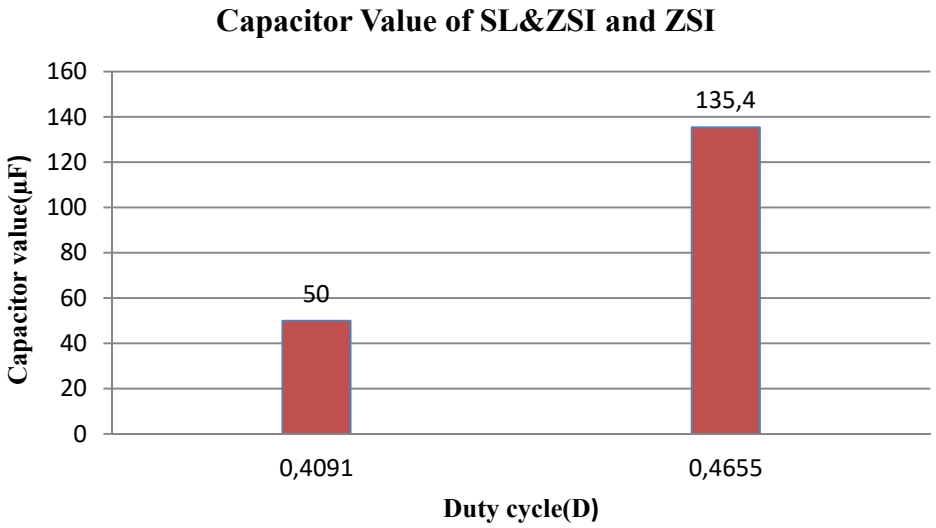

Figure 4.5: Comparing between capacitor value of SL&ZSI and ZSI.

The input voltage V_{in} into a traditional ZSI is 80v (V_{in}=V_{i1}) but, the input average voltage V_{i1} into ZSI in one cell of SL) as shown in Figure 4.1)was increased (according to equation (10)) to 190.8V at D=0.4091, which will give great support to the circuit. Thus, the increase rate is 138.5%. Figure 4.6 illustrates this increase.

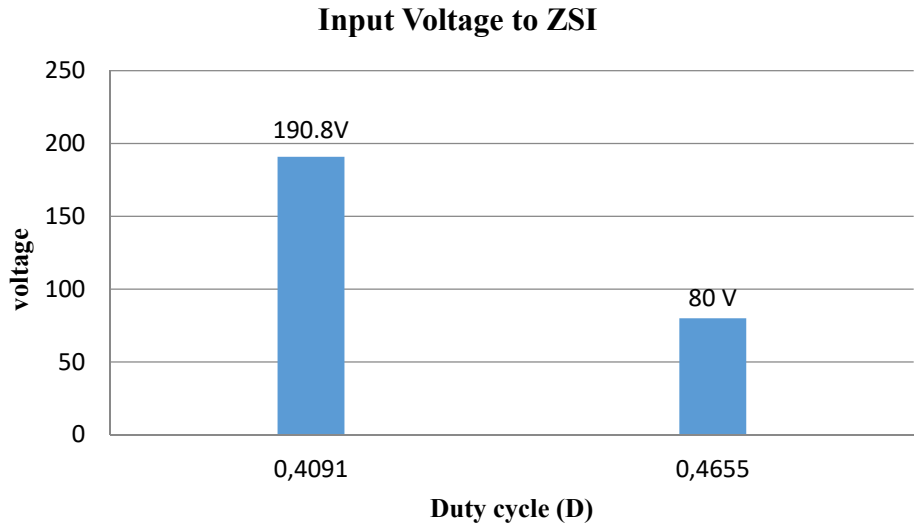

Figure 4.6: Input voltage to Z-source inverter for (1cell SL&ZSI) and traditional ZSI.

When the circuit of the ZSI and the circuit of one cell SL&ZSI designed, the output voltage V_{RMS} line to line was 380V and the input voltage was 80V for both circuits. From the derived equations, the duty cycle of the traditional ZSI equals 0.4655, whereas, the duty cycle of one cell SL&ZSI equals 0.4091. Therefore, the duty cycle of one cell SL&ZSI has been reduced at a rate of 12.12% on the traditional ZSI, which means that the thermal losses in the switches will decrease because of the decreasing in closing and opening processes. (This is one of the objectives of this research).

Figure 4.7 shows that those curves are identical and both of them are starting from zero, the curve related to the SL&ZSI over the curve of the traditional ZSI. However, the curve related to the SL&ZSI shows the stress ratio on the capacitor reaches a maximum value and stops at D=0.4091 according to the required design values. While the curve of the traditional ZSI continues to rise up to the maximum value of the stress ratio on the capacitor and stops at D=0.4655. Therefore, the stress ratio decreases when the duty cycle decreases by increasing the input voltages to ZSI. Additionally, the average voltage value V_{1i}, which boosted into ZSI, is equal

190.8v at D=0.4091, according to equation 4.10 and 3.6, so the stress ratio $\frac{Vc}{Vi1}$ equal 3.249. While, in traditional ZSI, the average voltage value V_{1i} is the same as the main voltage ($V_{in} = V_{1i}$) and equals 80V at D=0.4655, therefore, the stress ratio $\frac{Vc}{Vin}$ equals 7.745. (The stress ratio was reduced to 58.1%), which is one of the objectives of this research. Figure 4.8 shows the difference between them.

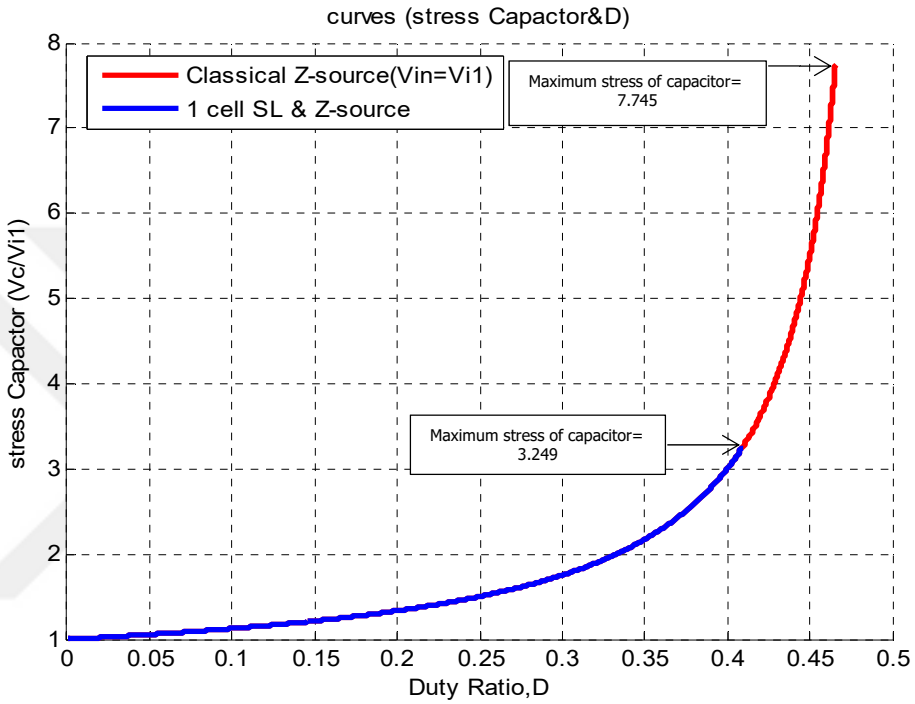

Figure 4.7: The rate of voltage stress on the capacitor.

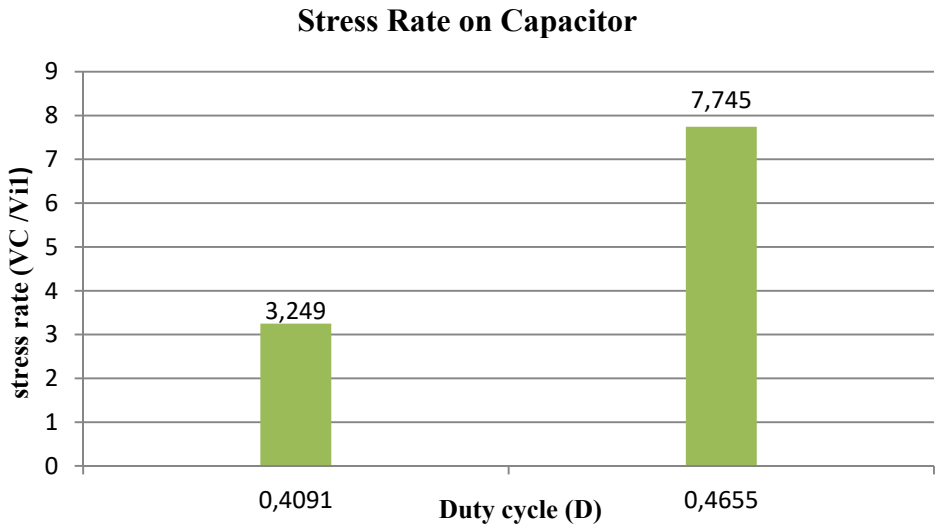

Figure 4.8: Difference between Stress rate on the capacitor.

4.4 Simulation Results

The results schemes for one cell of SL & ZSI depend on Figure 4.1 and an input value that referred to the previous design. A simulation has been done by using National Instrument (Multisim) with the simple boost control method. And three – phase output filter: L_f=1mH, C_f =22 µF.

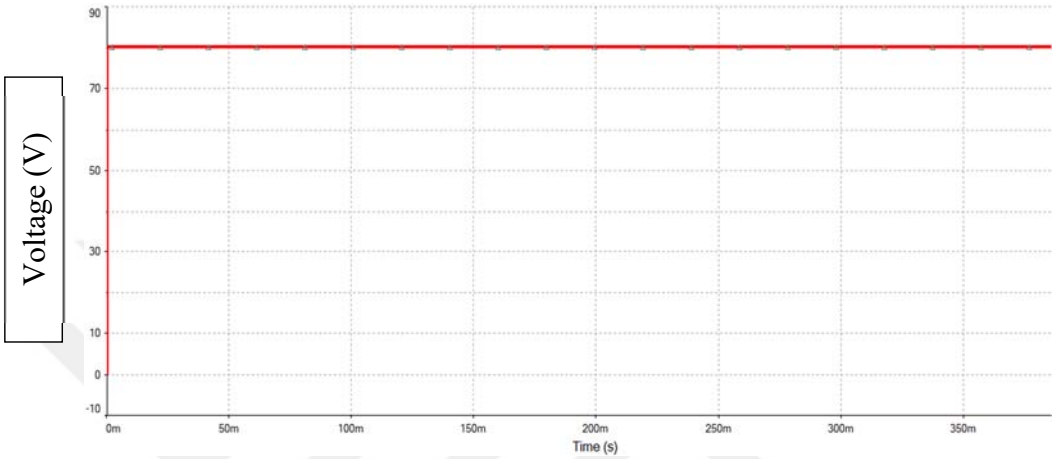

Figure 4.9: Input voltage (V_{in}).

In Figure 4.9, the value of the source energy is 80V (DC), and this source can be batteries, solar cells or other sources of renewable energy.

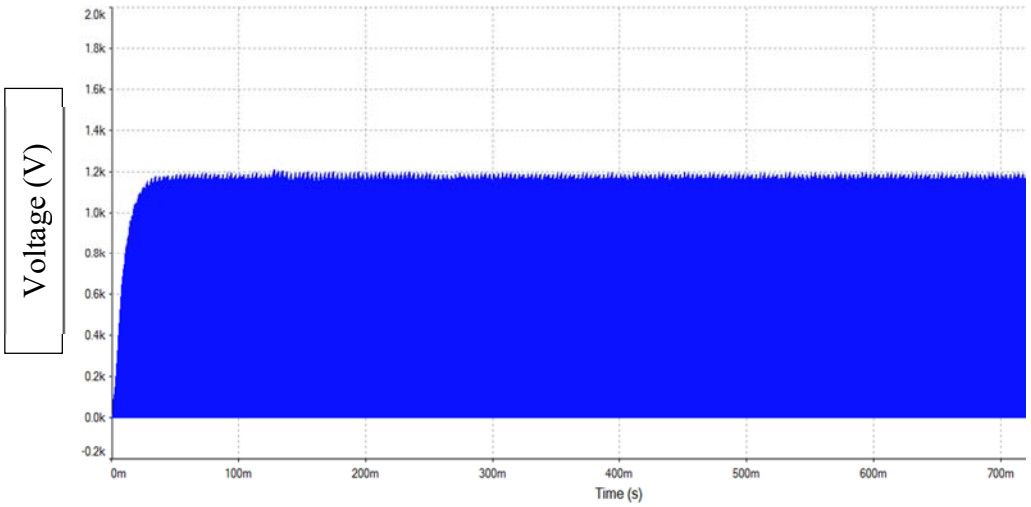

Figure 4.10: dc-link voltage (V_{i2}).

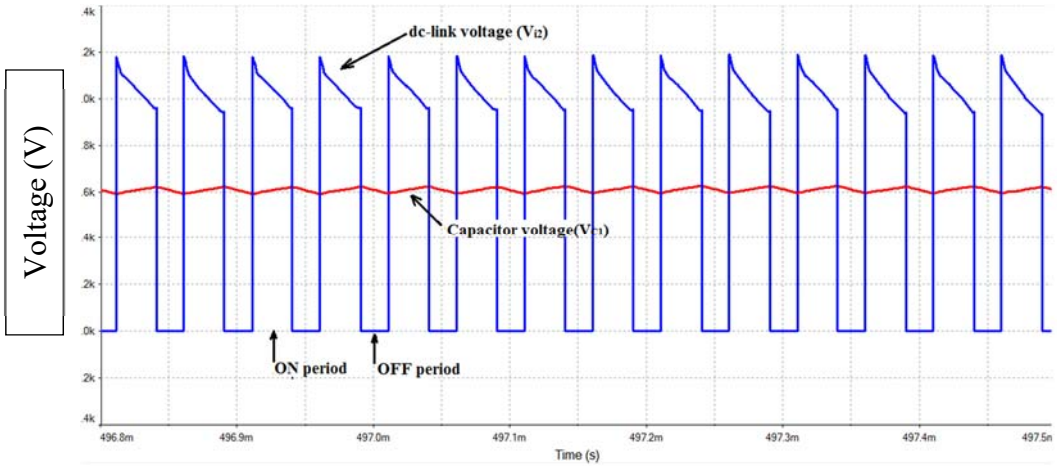

Figure 4.11: dc-link voltage (V_{i2}) & charge –discharge for the capacitor (V_{C1}) voltage.

Figure 4.10, 4.11 showed the average value of dc-link voltage $\overline{V}_{i2}$ and equal almost to 1035V, but theoretical result equal to 1050.1V, therefore the error rate is 1.4%.

The charging and discharging process of the capacitor is linearly (not sinusoidal). This is an important point to reduce the ripple in the circuit and reduce the harmonic content [71]. Figure 4.11 shows this relationship between the charge and discharge of the capacitor voltage with average dc-link voltage $\overline{V}_{i2}$. During the Active state period, the figure indicates the process of charging the capacitor voltage at the ON period of average dc-link voltage, and during the shoot-Through state, the capacitor will discharge the energy into the inductors at OF period of average dc-link voltage $\overline{V}_{i2}$. Also, Figure 4.12 shows the linear behavior of the capacitor.

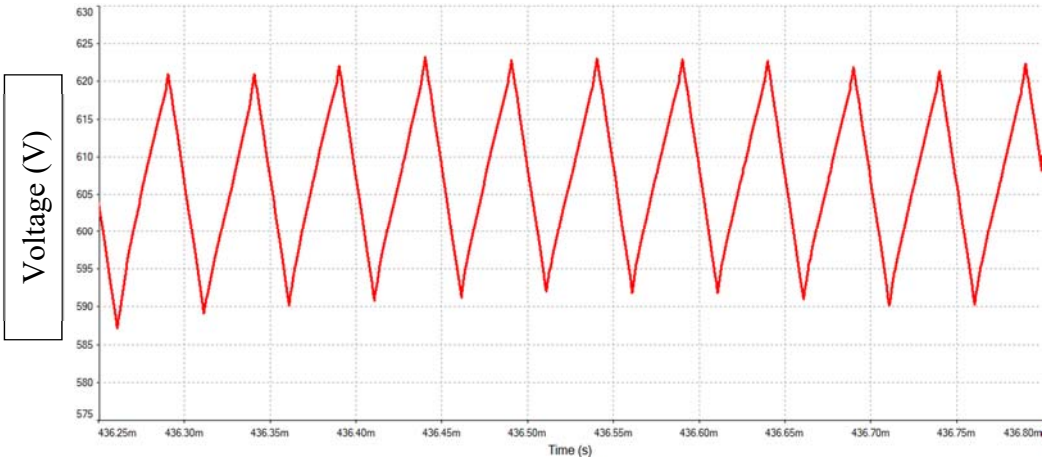

Figure 4.12: Charge & discharge for capacitor voltage (V_{C1}= V_{C2}).

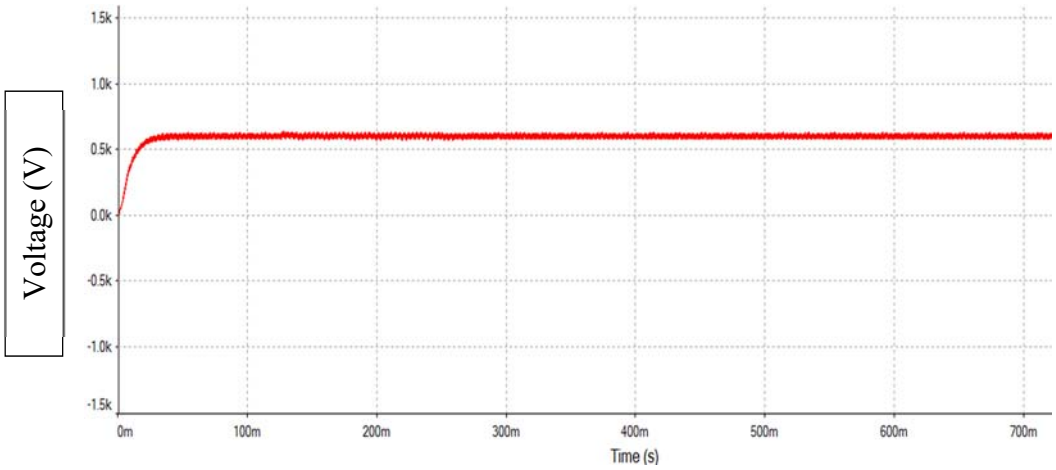

Figure 4.13: Capacitor voltage (V_{C1}= V_{C2})

The average value of the capacitor voltage in the simulation reached to 607V as shown in Figure 4.12, 4.13 while, theoretically reached to 620.06 V. The error rate is 2%.

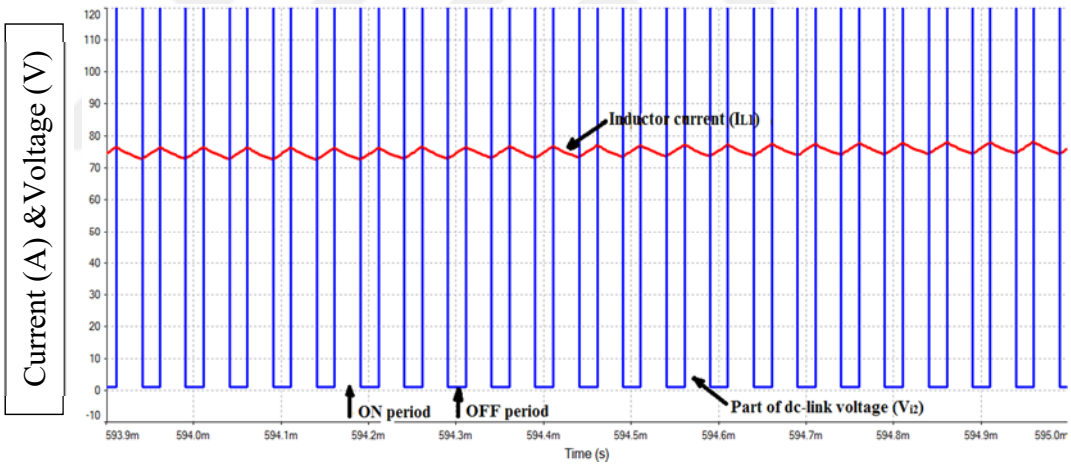

Figure 4.14: Part of dc-link Voltage (V_{i2}) & charge –discharge for the inductor current (I_{L1}).

The period of charging and discharging for the inductor current is contrary to the capacitor behavior, so in Figure 4.14, the Active state period shows the discharge energy of the inductor to the load at ON period of the average dc-link voltage $\overline{V}_{i2}$, however, during the Shoot-Through states, the inductor will charge from the transferred energy from the capacitor discharge at OFF period of average dc-link voltage $\overline{V}_{i2}$. The charging and discharging process of the inductor must be almost linearly (not sinusoidal) to reduce the ripple in the circuit, therefore, reduce the harmonic content [71] as in Figure 4.15.

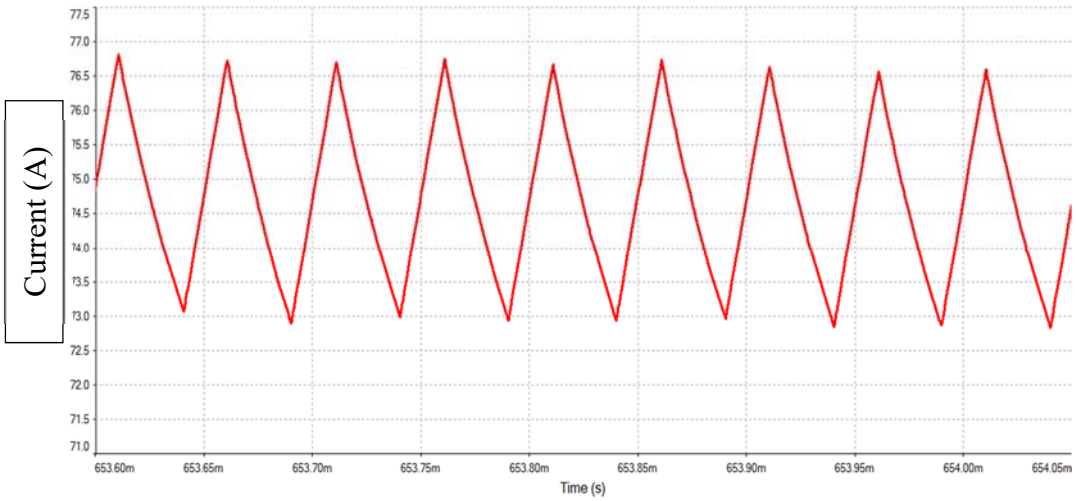

Figure 4.15: Charge & discharge for the inductor current (I_{L1}=I_{L2}).

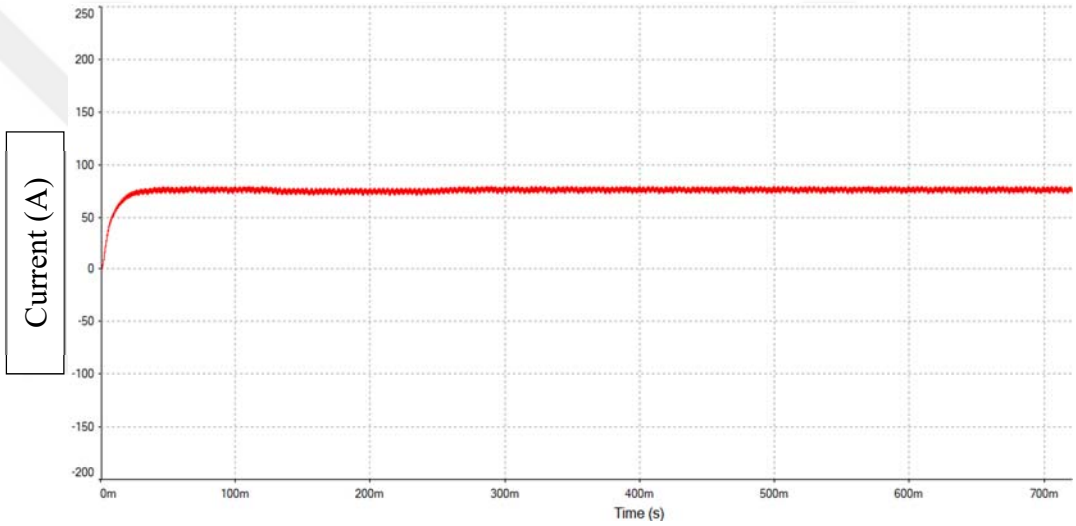

Figure 4.16: Inductor current (I_{L1}=I_{L2}).

The average value of inductor current (as in Figure 4.15, 4.16) reached in the simulation 75A; however, theoretical value is 76A, so the error rate is 1.3%.

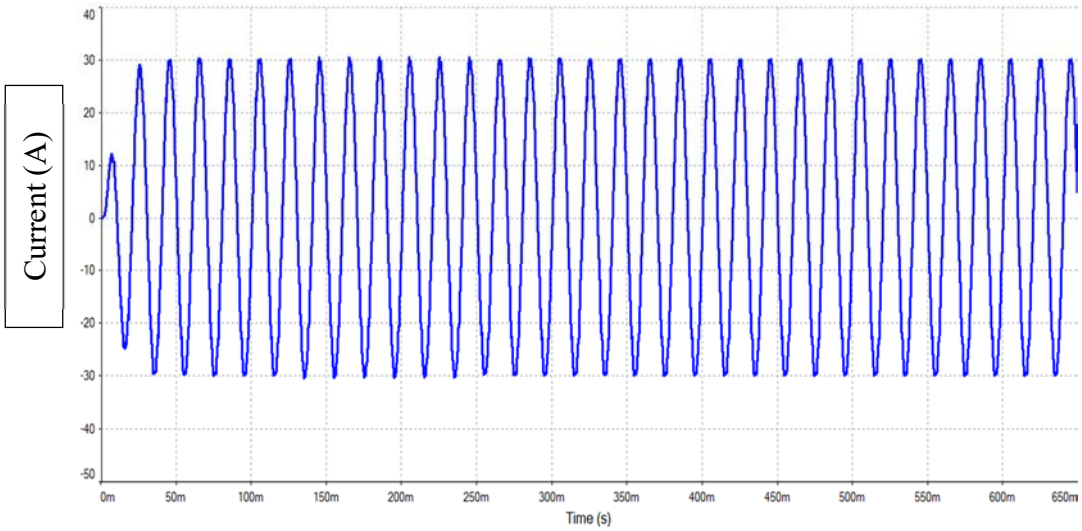

Figure 4.17: Peak current of phase (R).

The peak value of phase current I_m in the simulation is equal 30.5A (as in Figure 4.17), while, the peak phase current value in theoretical equals 31.027A, so the rate error is 1.7%.

$$I_{RMS} = \frac{\text{peak phase current}}{\sqrt{2}} = \frac{31.027}{\sqrt{2}} = 21.1\,A$$

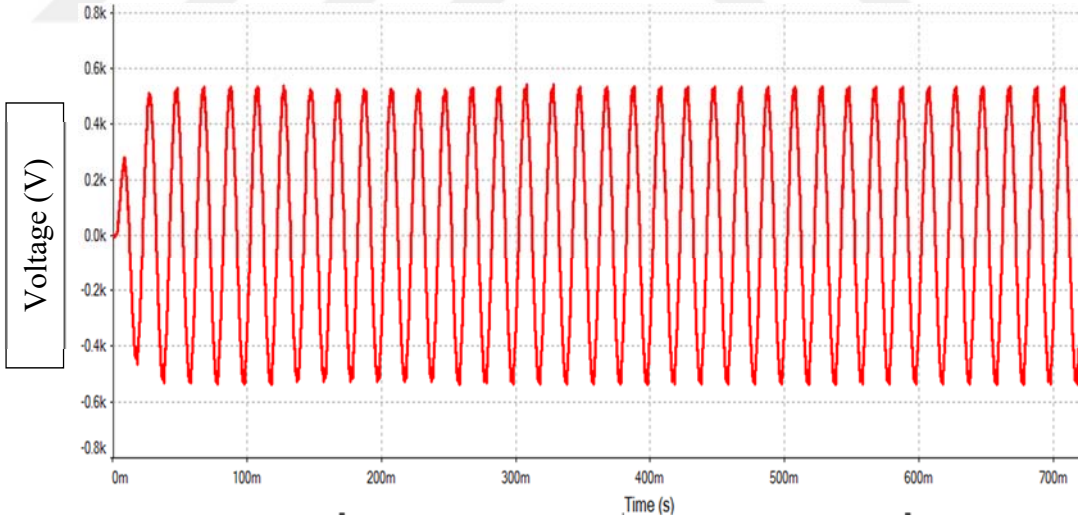

Figure 4.18: Peak to peak of (R-S) line voltage.

The peak value of line to line voltage $V_{peak\ line\text{-}line}$ is equal 530V (as in Figure 4.18).

$$V_{line\text{-}line(RMS)} = \frac{V_{peak\ line\text{-}line}}{\sqrt{2}} = \frac{535.5}{\sqrt{2}} = 374.8\,V$$

However, the given value and the desired output is 380V_{RMS}, therefore the error rate is 1.3%.

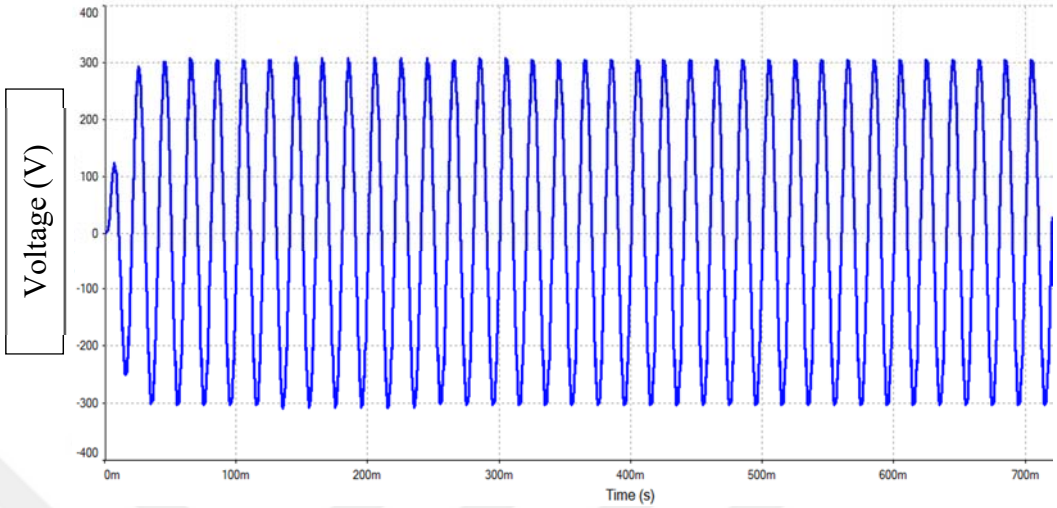

Figure 4.19: Peak voltage of phase (S).

V_m and V_{ac} are the peak values of phase voltage [2] [71] that mentioned in the previous equations, are equal to 305V (as in Figure 4.19) the given value and desired to get the output is V_m=310.27V, therefore, the error rate is 1.7%. Comparing the simulation value 305V and the value from equation (20) V_{ac}=310.01, the error rate will be 1.6 %, and both error rates are very small.

$$V_{phase(RMS)} = \frac{\text{peak phase voltage}(V_{ac})}{\sqrt{2}} = \frac{305}{\sqrt{2}} = 215.7\,V$$

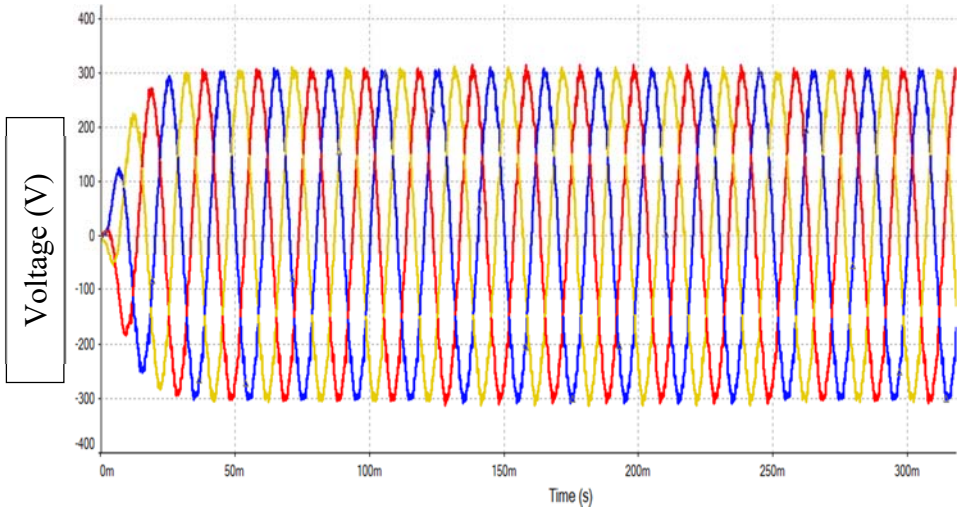

Figure 4.20: Peaks phase voltages of 3-phase (R, S, T).

Three phase peak voltage that represented in Figure 4.20 has the frequency of (50Hz).

4.5 Extension in One Cell of Switched Inductor (SL)

From recent analysis (section 4.4), it can be known that switched-inductor cell can improve the voltage gain. Based on this feature, the output voltage can be boosted by adding multiple switched inductor cells as shown in Figure 4.21. The operating concept is analyzed as follows.

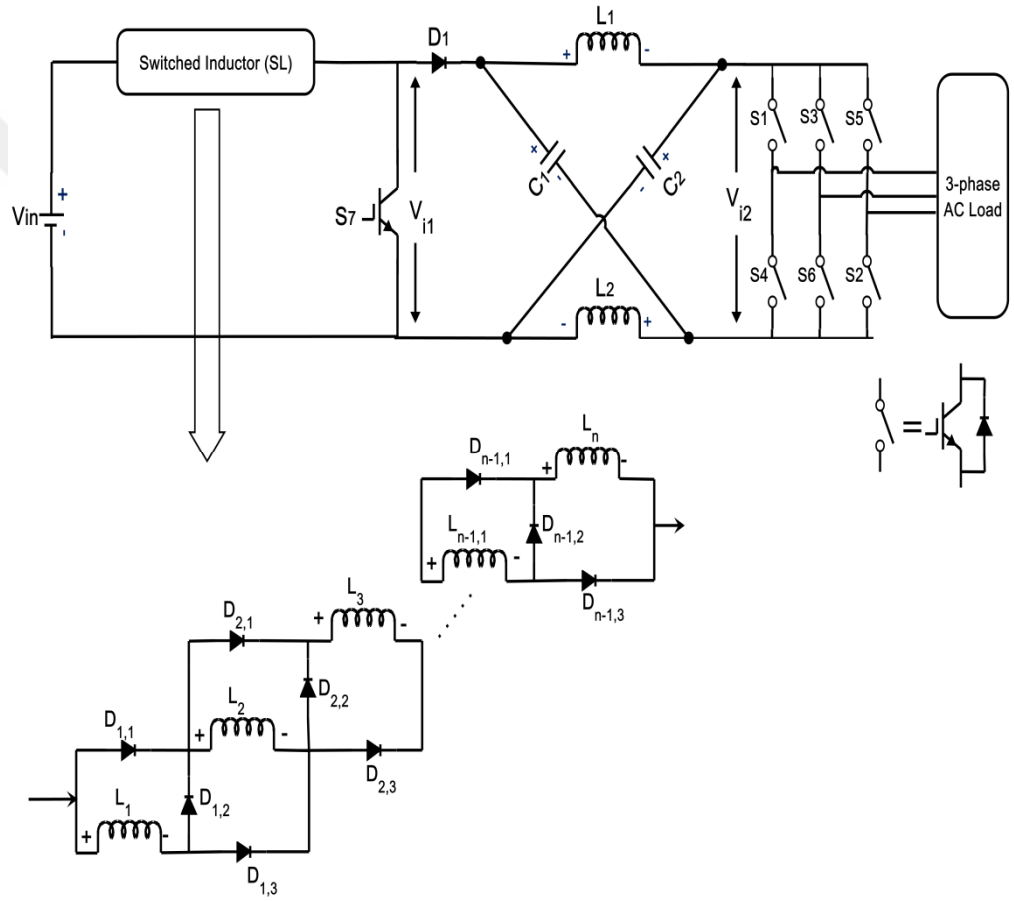

Figure 4.21: Extended SL with n number of inductors.

In nonshoot-through state L_1, L_2, L_3…..L_{n-1} and Ln will be connected in series ($L_1=L_2=L_3=\ldots.=L_{n-1}=L_n$). Thereby:

$$V_{L1} + V_{L2} + V_{L_{n-1}} + V_{L_n} + V_{i1} = V_{in} \quad (4.24)$$

$$V_{L1} = V_{L2} = V_{L_{n-1}} = V_{L_n} \quad (4.25)$$

From (4.24, 4.25):

$$V_{L1} = \frac{1}{n} V_{in} - \frac{1}{n} V_{i1} = V_{L2} = V_{L_{n-1}} = V_{L_n} \tag{4.26}$$

While in shoot through state L_1, L_2, L_3, ….L_{n-1} and L_n will be connected in parallel.

$$V_{L1} = V_{L2} = V_{L3} = V_{L_{n-1}} = V_{L_n} = V_{in} \tag{4.27}$$

By applying the volt-second balance principle to each inductor:

$$V_{i1} = \frac{1+(n-1)D}{1-D} V_{in} = B_1 * V_{in}$$

$$B_1 = \frac{1+(n-1)D}{1-D} \tag{4.28}$$

Now the dc-link voltage of SL&ZSI for n number of SL will be:

$$V_{i2} = \frac{1}{(1-2D)} * \frac{(1+(n-1)D)}{(1-D)} * V_{in} = \frac{(1+(n-1)D)}{(1-3D+2D^2)} V_{in} \tag{4.29}$$

The boost factor for n number of inductors will be:

$$B = \frac{1+(n-1)D}{1-3D+2D^2} \qquad \text{When } n \geq 2 \tag{4.30}$$

$$V_{ac} = M * B \frac{V_{in}}{2} \tag{4.31}$$

V_{ac} is the output value of peak phase voltage (peak value of line to neutral) [2]. Figure 4.22 shows the improvement in the boost factor value at a lower duty cycle by increasing the number of the inductors in one cell of switched inductor (as shown in Figure 4.21). From the equation 4.30, n represents the number of the inductors. By increasing the number of inductors, the boost factor will increase. For example, in Figure 4.22 at n=2 (the number of inductors is two) there is a good increasing ratio of the boost factor compared with traditional ZSI, and when n=3 the ratio of the boost factor became better than n=2, while at n=4 the boost factor became better compared with n=2 and n=3. So the designers can increase the number of inductors and get to L_n of inductors, according to the design requirements, therefore the switched inductor will be a series of inductors cells SL. Whereof, by increasing one inductor, a number of diodes need to be added.

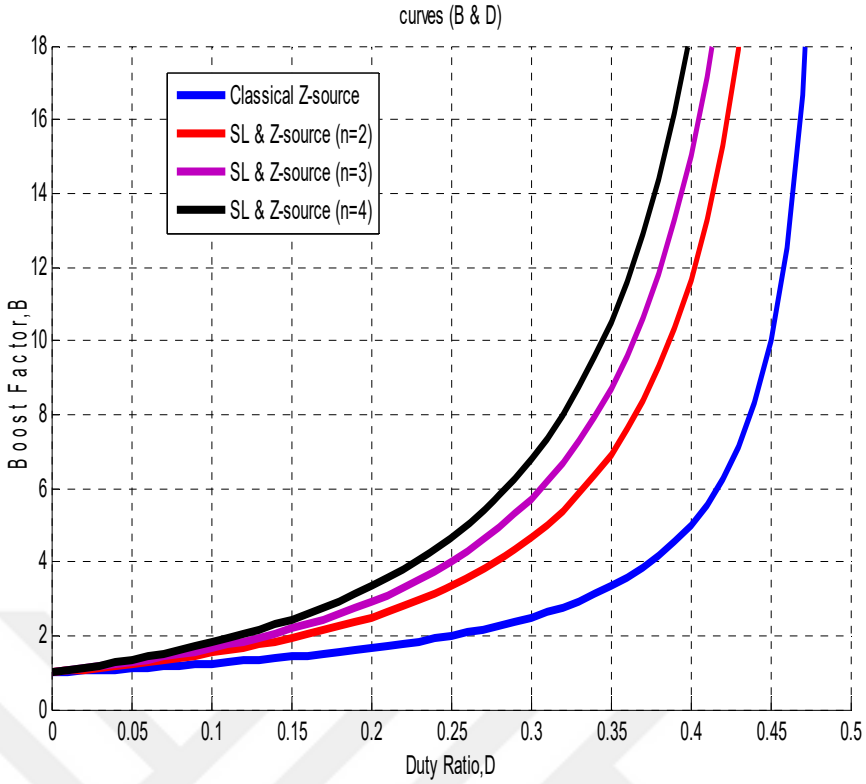

Figure 4.22: Improving the boost factor of extension in one cell of switched inductor (SL).

Table 4.1: Comparison between various types of Z-source

	SL-ZSI	Classical ZSI	One cell SL&ZSI (Proposed Topology)
B	$\frac{1+D}{1-3D}$	$\frac{1}{1-2D}$	$\frac{1+(n-1)D}{1-3D+2D^2}$
Vc	$\frac{(1+D)Vin}{(1-3D)}$	$\frac{(1-D)Vin}{(1-2D)}$	$\frac{(1+(n-1)D)Vin}{(1-2D)}$

The above table compares the proposed topology one cell of SL&ZSI with two different topologies, and the comparison is in terms of the boost factor and voltage capacitor.

CHAPTER FIVE

THE PROPOSED TOPOLOGY FOR THE SECOND CIRCUIT: TWO CELL OF SWITCHED INDUCTOR (X-SHAPE SL) COMBINED WITH ZSI

5.1 Introduction

This chapter will discuss the second circuit idea by combining two cells of SL with traditional ZSI. The shape of SL is similar of X-shape, so called "X-shape SL". The contents of this chapter will be similar to the contents of Chapter 4 in terms of division. Also after each part, there will be a discussion and comparison of the results.

5.2 The Analysis of Proposed Circuit Topology

The Z-source network composed of two inductors (L_1=L_2) and two capacitors (C_1=C_2) in addition to one diode D_1. While the first cell of switched inductor network composed of two inductors (L_3=L_4) and three diodes (D_2, D_3, and D_4). The second cell of switched inductor network consists two inductors (L_5=L_6) and three diodes (D_5, D_6, and D_7), as shown in Figure 5.1.

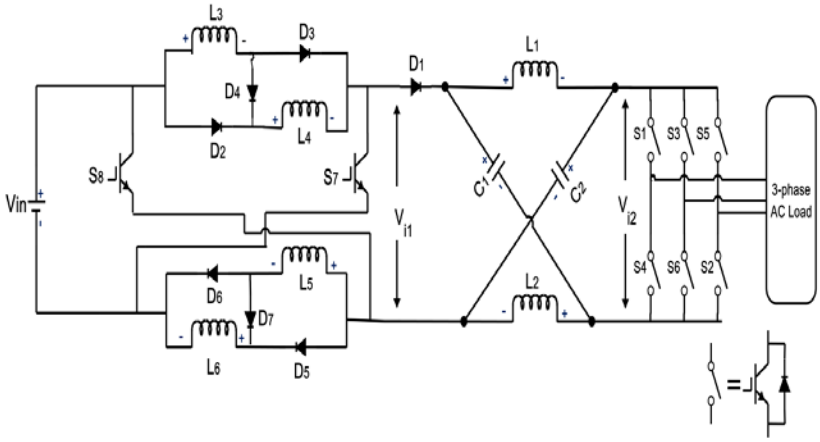

Figure 5.1: X-shape SL combined with traditional ZSI.

The operating principles of the proposed topology are also similar to those of the classical ZSI and SL&ZSI. For the purpose analysis, the operating states are simplified into shoot-through and nonshoot-through states. Figure 5.2 shows the equivalent circuits of X-shape SL with the traditional ZSI at nonshoot-through states.

In the nonshoot-through state, the behavior of X-shape switched inductor network will be as following: D_4, D_7 are on, while D_2, D_3, D_5, and D_6 are off. L_3 and L_4 are connected in series. L_5 and L_6 are also connected in series (L_3= L_4=L_5= L_6). L_3, L_4, L_5 and L_6 transfer the energy from the dc voltage source to the Z-source network.

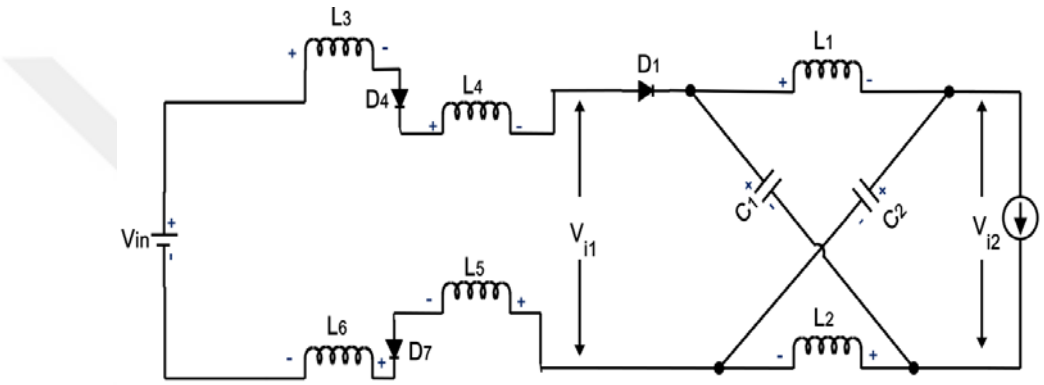

Figure 5.2: The switch (S_7), (S_8) of X-shape SL is OFF state.

The corresponding voltages across L_3, L_4, L_5 and L_6 which in this state are V_{L3}, V_{L4} V_{L5}, and V_{L6}, respectively, will be:

$$L_3 = L_4 = L_5 = L_6$$

$$V_{L3} + V_{L4} + V_{L5} + V_{L6} + V_{i1} = V_{in} \tag{5.1}$$

$$V_{L3} = V_{L4} = V_{L5} = V_{L6} \tag{5.2}$$

From 5.1, 5.2, the equation will be:

$$4\,V_{L3} = V_{in} - V_{i1}$$

$$V_{L3} = \frac{V_{in} - V_{i1}}{4} \tag{5.3}$$

For the Z-source network, D_1 is on, (L_1=L_2), (C_1=C_2), so the Z-source network becomes symmetrical. From the symmetry and the equivalent circuit:

$$V_{C1} = V_{C2} = V_C, V_{L1} = V_{L2} = V_L \tag{5.4}$$

$$V_L = V_{i1} - V_C$$

$$V_{i2} = V_C - V_L \longrightarrow V_{i2} = V_C - (V_{i1} - V_C) \quad (5.5)$$

$$V_{i2} = 2V_C - V_{i1} \quad (5.6)$$

In the shoot through state, the behavior of X- shape SL will be (as shown in Figure 5.3): D_4 and D_7 are off. D_2, D_3, D_5, and D_6 are on. L_3, L_4, L_5, and L_6 are connected in parallel.

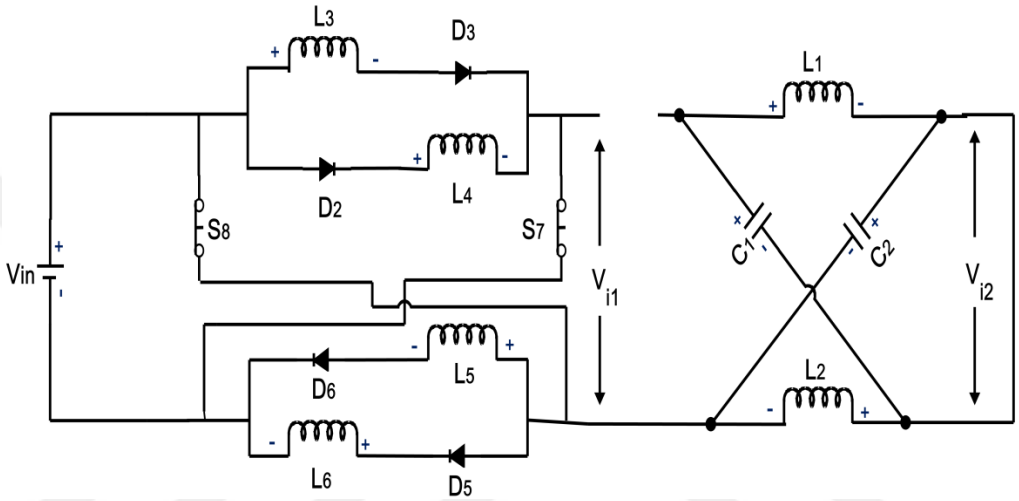

Figure 5.3: The switch (S_7), (S_8) of X-shape SL is ON state.

The equivalent circuit is:

$$V_{L3} = V_{L4} = V_{L5} = V_{L6} = V_{in}, V_{i1} = 0 \quad (5.7)$$

For Z-source network, D_1 is off, L_1 and C_1 are connected in parallel, L_2 and C_2 are connected in parallel. From the equivalent circuit:

$$V_L = V_C, V_{i2} = 0 \quad (5.8)$$

Where V_{in} is the input voltage for the X-shape SL network, V_{i1} is the input voltage for the ZSI network.

Based on the volt-second balance principle, the voltage across the inductor L_3, L_4, L_5, and L_6 can be getting it in the two periods which were represented in (5.1, 5.2, 5.3 and 5.7). By setting the interval of the shoot-through state: DT, while non-shoot through state: (l-D) T, subsequently:

$$DT * V_{in} = (D-1)T * \frac{V_{in} - V_{i1}}{4} \quad (5.9)$$

$$V_{i1} = \frac{1+3D}{1-D} V_{in} = B_1 * V_{in} \tag{5.10}$$

$$B_1 = \frac{1+3D}{1-D} \tag{5.11}$$

Where B_1 is the boost factor of the switched inductor network.

The average voltage of inductors (L_1 and L_2) over one switching period (T) should be zero in steady state, from (5.5, 5.6, and 5.8) it obtains:

$$\overline{V_L} = \frac{T_o V_C + T_1 (V_{i1} - V_C)}{T} = 0 \tag{5.12}$$

$$\frac{V_C}{V_{i1}} = \frac{T_1}{T_1 - T_o} \tag{5.13}$$

Similarly, the average dc-link voltage across the output of the inverter bridge can be:

$$V_{i2} = \frac{T_o * (0) + T_1 (2V_C - V_{i1})}{T} = \frac{T_1}{T_1 - T_o} V_{i1} = V_C \tag{5.14}$$

The peak dc-link voltage across the inverter bridge is obtained as:

$$V_{i2} = 2V_C - V_{i1} = \frac{T}{T_1 - T_o} V_{i1} = B_2 * V_{i1} \tag{5.15}$$

Where:

$$B_2 = \frac{T}{T_1 - T_o} = \frac{1}{1-2D} \tag{5.16}$$

Where B_2 is the boost factor of the Z-source network.

By substituting 5.10 in 5.15:

$$V_{i2} = \frac{1}{1-2D} * \frac{1+3D}{1-D} V_{in} = \frac{1+3D}{1-3D+2D^2} V_{in} \tag{5.17}$$

Where:

$$B = \frac{1+3D}{1-3D+2D^2} \quad ; \quad D \leq 0.5 \tag{5.18}$$

The boost factor is resulting from the shoot through zero-state. The average dc-link voltage V_{i2} is the equivalent dc-link voltage of the inverter. On the other side, the output peak phase voltage from the inverter can be expressed as:

$$V_{ac} = M \frac{V_{i2}}{2} \tag{5.19}$$

Where M is the modulation index. By using (5.17, 5.19) the peak phase voltage will be as follows:

$$V_{ac} = M * B \frac{V_{in}}{2} \tag{5.20}$$

$$V_{ac} = B_B \frac{V_{in}}{2} \tag{5.21}$$

$$B_B = M * B = (0 \sim \infty) \tag{5.22}$$

The buck-boost factor is (B_B).

From (5.4, 5.13, and 5.16) the capacitor voltage can be expressed as:

$$V_C = \frac{1 - D}{1 - 2D} V_{i1}$$

$$V_C = \frac{1 + 3D}{1 - 2D} V_{in} \tag{5.23}$$

The boost factor and modulation index adjust the factor of the buck-boost B_B. The boost factor as expressed in 5.18 can be determined by duty cycle (i.e., interval ratio).

Figure 5.4 represents the improvement of the boost capability and comparing the proposed circuit of X-shape SL&ZSI with a network of SL&ZSI and the traditional ZSI. The boost factor increased by combining X-shape SL with ZSI at a small value of duty cycle compared with a traditional ZSI. The boost factor will increase by increasing the duty cycle. For example in Figure 5.4, the boost factor at D=0.25 was equal 2 for the traditional ZSI and equal 3.333 for SL&ZSI. However, the boost factor at same duty cycle is 4.666 for X-shape SL&ZSI. The increase rate between X-shape SL&ZSI and SL&ZSI is 40% and between X-shape SL&ZSI and ZSI is 133.3%. In addition, the boost factor at D=0.4 is equal to 5 for the traditional ZSI and equal 11.666 for SL&ZSI network while, the boost factor at same duty cycle

is 18.333 for X-shape SL&ZSI network**.** The increase rate between X-shape SL&ZSI and SL&ZSI is 57.2% and between X-shape SL&ZSI and ZSI is 266.7% at D=0.4.

Therefore, the improvement for the boost factor clearly shows in Figure 5.4 for X-shape SL&ZSI.

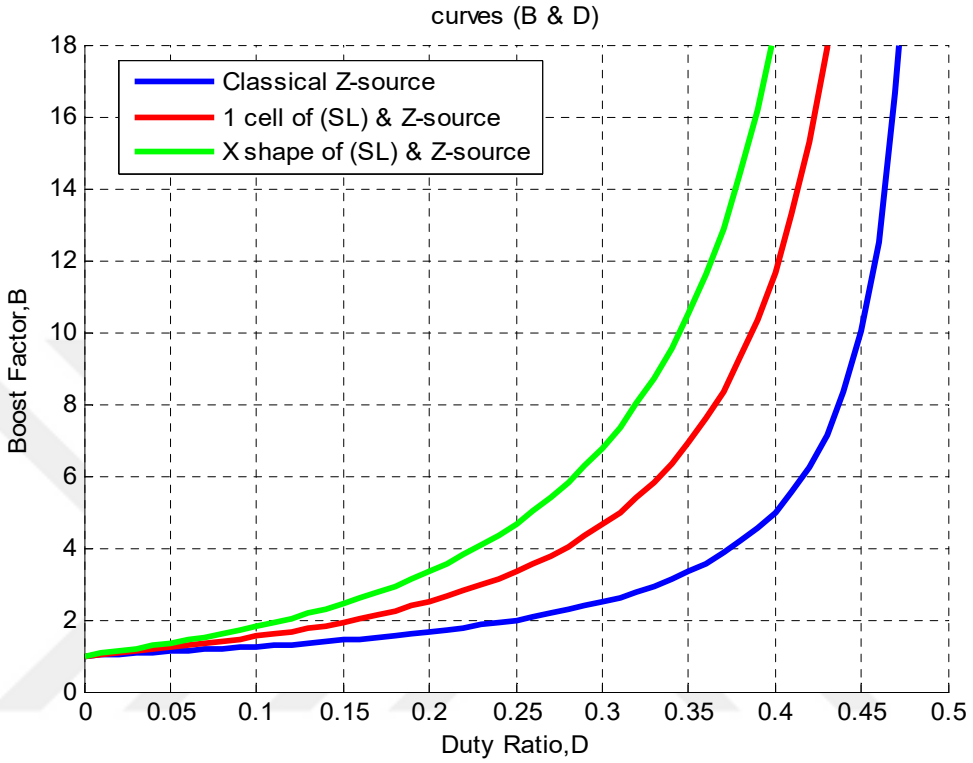

Figure 5.4: The comparison of boost factor with other types.

Moreover, the rate of the capacitor voltage stress will decrease for X-shape SL&ZSI comparing with SL&ZSI and the traditional ZSI (The rate of capacitor voltage stress will be explained in more details in section (5.3).

5.3 The Calculation of Proposed Circuit Topology Elements' Values

Design X-shape SL &ZSI will take the same steps of design traditional ZSI and design one cell of SL&ZSI and also will take the same input data:

$V_{in} = 80v$, $V_{L-L} = 380v$, $T_S = 10^{-4}\,\text{sec}$, $Rl_{Load} = 10\Omega$.

$V_m = \sqrt{2} * V_{L-L} / \sqrt{3}$

$\Rightarrow \mathrm{V_m} = 310.27\,\mathrm{V}$

$$I_m = \frac{V_m}{R_{load}}$$

$$\Rightarrow I_m = 31.027\,A$$

$$D = \frac{2\,V_m - \overline{V}_{i1}}{4\,V_m - \overline{V}_{i1}}$$

By subtracting equation 5.10 from this equation

$\Rightarrow D = 0.3649$ And substitute (D) in 5.10

$$\overline{V}_{i1} = 264\,V$$

$$M = 1 - D$$

$$\Rightarrow M = 0.6351$$

$$\overline{V}_{i2} = 2\,V_m / M$$

Or

$$\overline{V}_{i2} = \frac{1+3D}{1-3D+2D^2} V_{in}$$

$$\Rightarrow \overline{V}_{i2} = 977.07\,V$$

$$C = \frac{3\,T_S I_m \cos\phi\left(2\,V_m - V_{i1}\right)}{8\,K_V V_{i1}\left(4\,V_m - V_{i1}\right)}$$

$$K_V = 5\%$$

$$\Rightarrow C = 3.216 * 10^{-5}\,\mu F$$

$$L = \frac{2\,V_{i1} T_S \left(2\,V_m - V_{i1}\right)}{3\,K_i I_m \cos\phi\left(4\,V_m - V_{i1}\right)}$$

$$K_i = 5\%$$

$$\Rightarrow L = 4.14 * 10^{-3}\,mH$$

$$\overline{V}_C = 2\,V_m$$

Or

$$\overline{V}_C = \frac{1+3D}{1-2D} V_{in}$$

$$\Rightarrow \overline{V}_C = 620.19\,V$$

$$B = \frac{1+3D}{1-3D+2D^2}$$

$$\Rightarrow B = 12.206$$

$$V_{ac} = M * B\frac{V_{in}}{2}$$

$$\Rightarrow V_{a.c} = 310.1V$$

$$\frac{V_C}{V_{i1}} = 2.349 \quad \text{Stress ratio on the capacitor}$$

$$\bar{I}_{1ZSI} = 2\,V_m I_0 / V_{i1}$$

$$\bar{I}_{1ZSI} = 54.7\ A$$

$$L_{SL} = L_3 = L_4 = L_5 = L_6 \geq \frac{D(1-D)^2\,RL}{K_i(1+3D)f_S}$$

$$f_S = 10\,KH$$

$$\Rightarrow L_{SL} = 1.4*10^{-3} mH \approx 1.5*10^{-3}$$

From the design the circuits of X-shape SL&ZSI (as shown in Figure 5.1) and theoretical results values that appeared, the proposed topology of the X-shape SL&ZSI can be applied, because the values that have been obtained almost true, which proves the theory. For example, in equation 5.20 the peak phase voltage V_{ac} is 310.1V, and it is almost equal to V_m value, therefore the percentage of error between V_{ac} and V_m is very small and equal to 0.05%. So, the V_{RMS} value of phase voltage equals 219.27 and V_{RMS} value of line to line voltage equals 379.8.

In addition, the design of traditional ZSI showed that the capacitor value was equal to $1.354*10^{-4}\,\mu F$ at D =0.4655 and equals $5*10^{-5}\,\mu F$ for one cell of SL&ZSI at D=0.4091 however, the proposed topology of the X-shape SL&ZSI showed that the capacitor value decreased and became $3.216*10^{-5}\,\mu F$ at D = 0.3649, whereas, the decrease rate between X-shape SL&ZSI and SL&ZSI is 35.7% and between X-shape SL&ZSI and traditional ZSI is 76.24%.Where one of the aims of this research is to reduce the value of the capacitor. Figure 5.5 shows the difference between them.

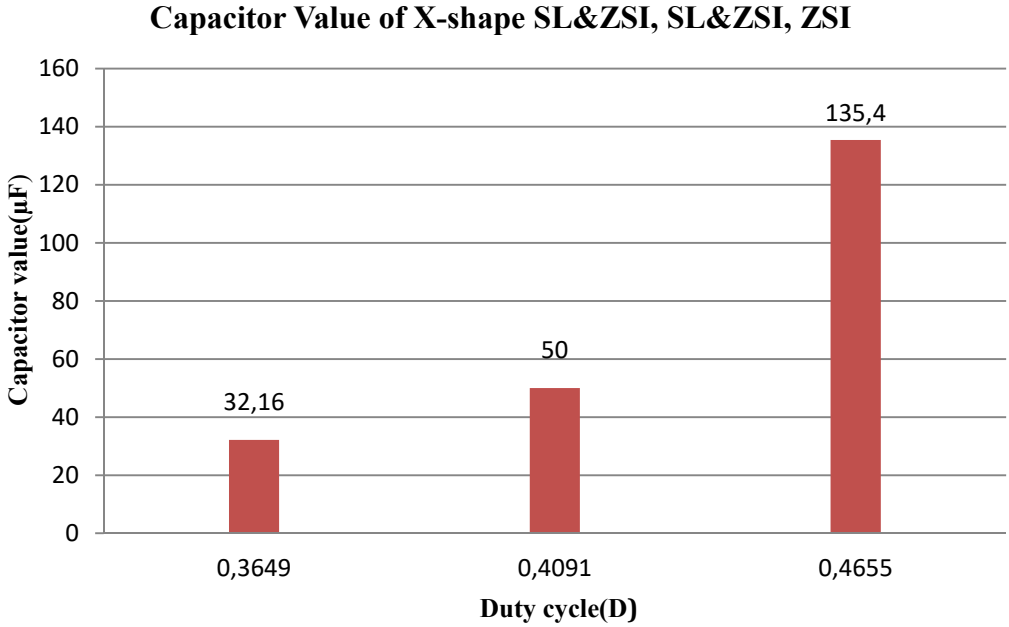

Figure 5.5: Comparing between capacitor value of X-shape SL&ZSI, SL&ZSI, and traditional ZSI.

The input voltage V_{in} into a traditional ZSI is 80v ($V_{in}=V_{i1}$) but, the input average voltage V_{i1} into ZSI in one cell of SL)as shown in Figure 4.1)was increased (according to equation 4.10) to 190.8v at D=0.4091, however the input voltage V_{i1} into ZSI in X-shape SL)as shown in Figure 5.1)was increased (according to equation 5.10) and became equal 264 at D=0.3649, which will give great support to the circuit. Therefore, the decrease rate between X-shape SL&ZSI and SL&ZSI is 38.36% and between X-shape SL&ZSI and traditional ZSI is 230%. Figure 5.6 illustrates this increase.

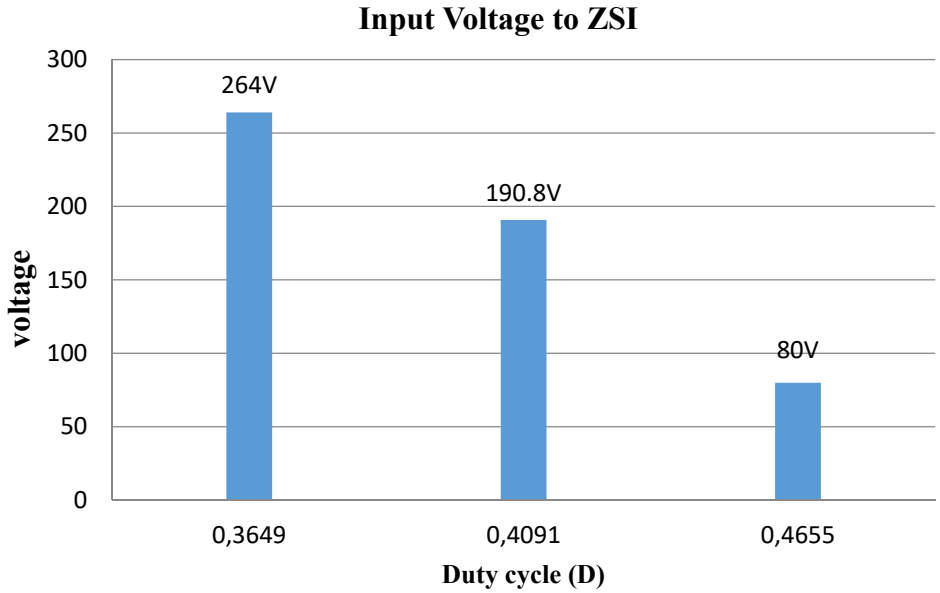

Figure 5.6: Input voltage to Z-source inverter for X-shape SL&ZSI, one cell SL&ZSI and traditional ZSI.

When the circuit of the traditional ZSI, one cell SL&ZSI and X-shape SL&ZSI designed, the output voltage V_{RMS} line to line was 380V and the input voltage was 80V for all circuits. From the derived equations, the duty cycle of the traditional ZSI equals 0.4655 and the duty cycle of one cell SL& ZSI equals 0.4091.Whereas, the duty cycle of X-shape SL&ZSI is equal 0.3649. Therefore, the duty cycle of X-shape SL&ZSI has reduced the rate of 10.8% on the one cell of SL&ZSI and reduced in the rate of 21.6% on the traditional ZSI, which means that the thermal losses in the switches will decrease because of the decreasing in closing and opening processes. (This is one of the objectives of this research).

Figure 5.7shows, these curves are identical and all of them starting from zero, the curve related to one cell of SL&ZSI over curve traditional ZSI and the curve related to X-shape SL&ZSI over curve one cell of SL&ZSI. However, the curve of X-shape SL&ZSI shows the stress ratio on the capacitor reaches to maximum and stops at D=0.3649 according to the required design values. The curve of one SL&ZSI shows the stress ratio on the capacitor reaches to maximum and stops at D=0.4091. While the curve of the traditional ZSI continues to rise up to the maximum value of the stress ratio on the capacitor and stops at a duty cycle 0.4655. Therefore, the stress ratio decreases when the duty cycle decreases by increasing the input voltages to ZSI. In addition, the voltage value V_{i1}, which boosted into ZSI, is equal 264V at

D=0.3694, according to equation 5.10 and 3.6, so the stress ratio $\frac{Vc}{Vi1}$ equal 2.349 . The stress ratio was reduced to 69.7% from the conventional Z-source inverter, which is one of the objectives of this research. Figure 5.8 shows the difference between them.

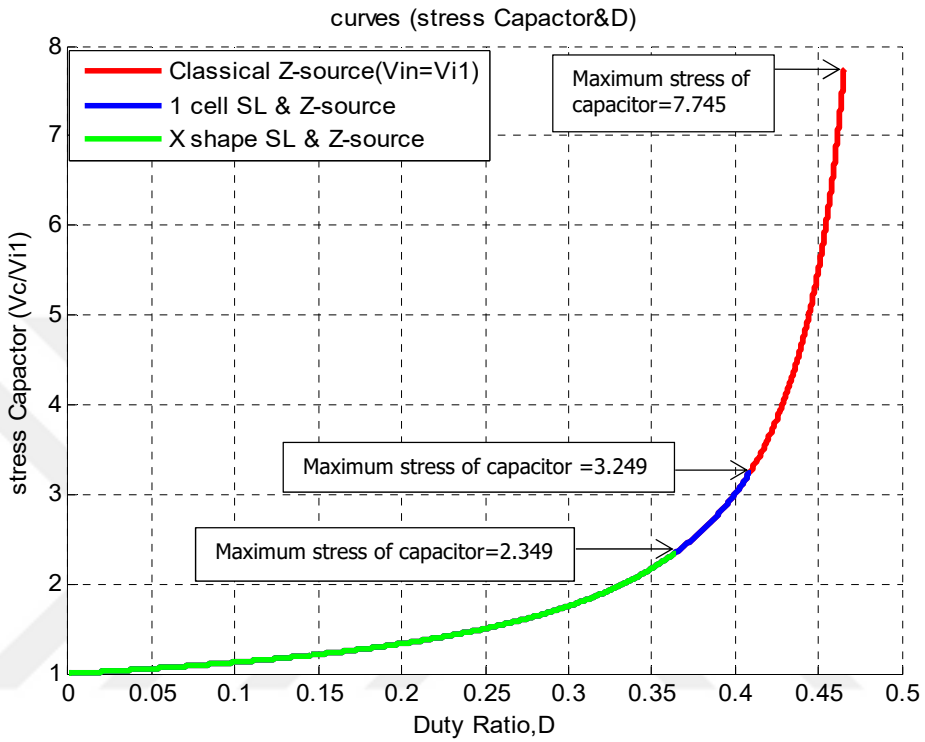

Figure 5.7: The rate of voltage stress on the capacitor.

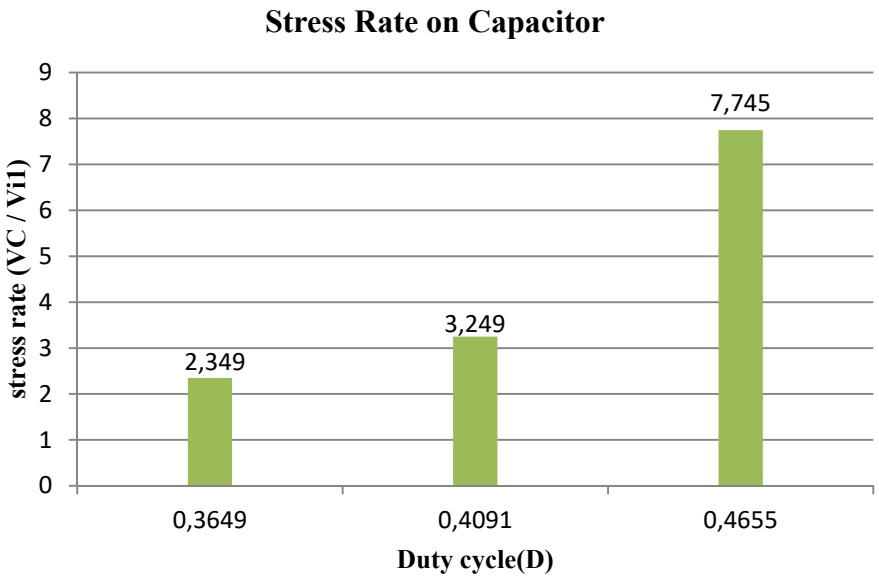

Figure 5.8: Difference between Rate stress on the capacitor.

5.4 Simulation Results

The results schemes for X-shape SL&ZSI depended on Figure 5.1 and an input value that referred to the previous design. A simulation has been done by using National Instrument (Multisim) with simple boost control method. And three –phase output filter: L_f=1mH, C_f =22 µF.

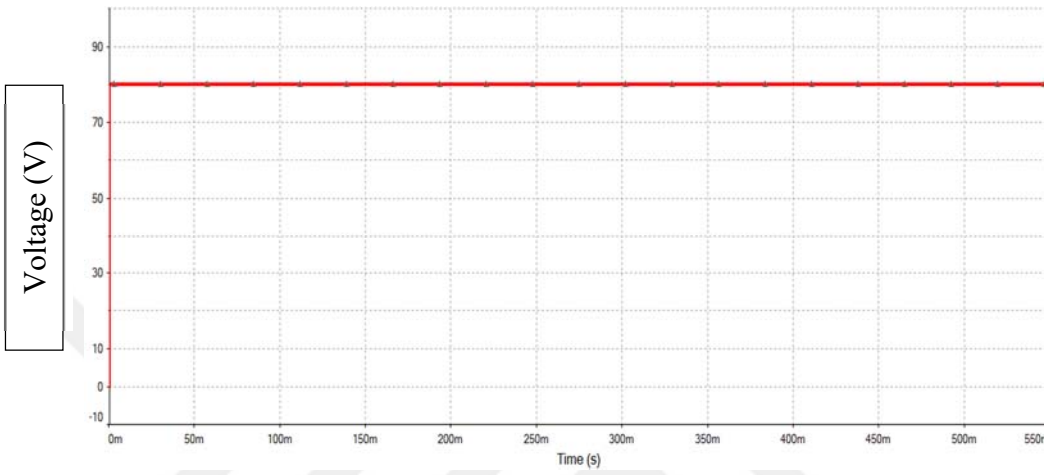

Figure 5.9: Input voltage (V_{in}).

In Figure 5.9, the value of the source energy is 80V (DC), and this source can be batteries or solar cells or other sources of renewable energy.

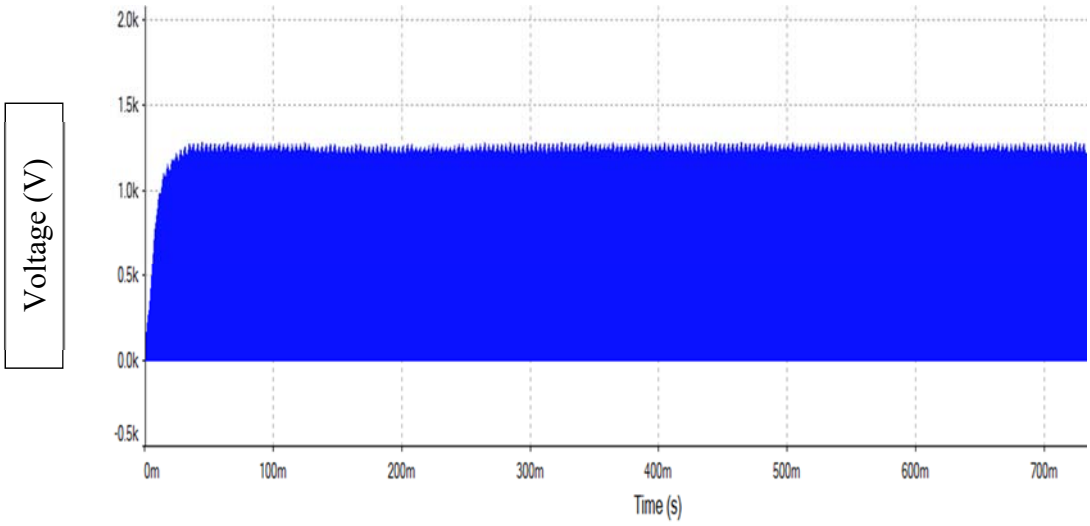

Figure 5.10: dc-link voltage (V_{i2}).

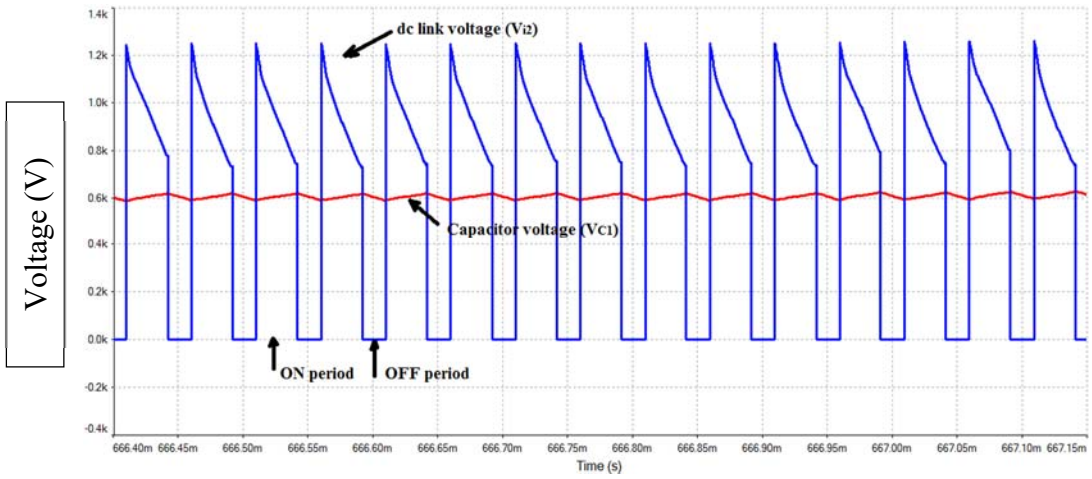

Figure 5.11: dc-link voltage (V_{i2}) & charge –discharge for the capacitor voltage (V_{C1}).

Figure 5.10,511 showed the average value of dc-link voltage $\overline{V}_{i2}$ equal to 967V which is almost identical to the theoretical 977.07V; therefore the error rate is 1%.

The charging and discharging process of the capacitor is linearly (not sinusoidal). This is an important point to reduce the ripple in the circuit and therefore reduce the harmonic content [71]. Figure 5.11 showed this relationship between the charge and discharge of the capacitor voltage with average dc-link voltage $\overline{V}_{i2}$. During the Active state period, the figure indicates the process the charging capacitor voltage at the ON period of average dc-link voltage, and during the Shoot-Through states, the capacitor will discharge the energy into the inductors at OF period of average dc-link voltage $\overline{V}_{i2}$. Also, figure 5.12 shows the linear behavior of the capacitor.

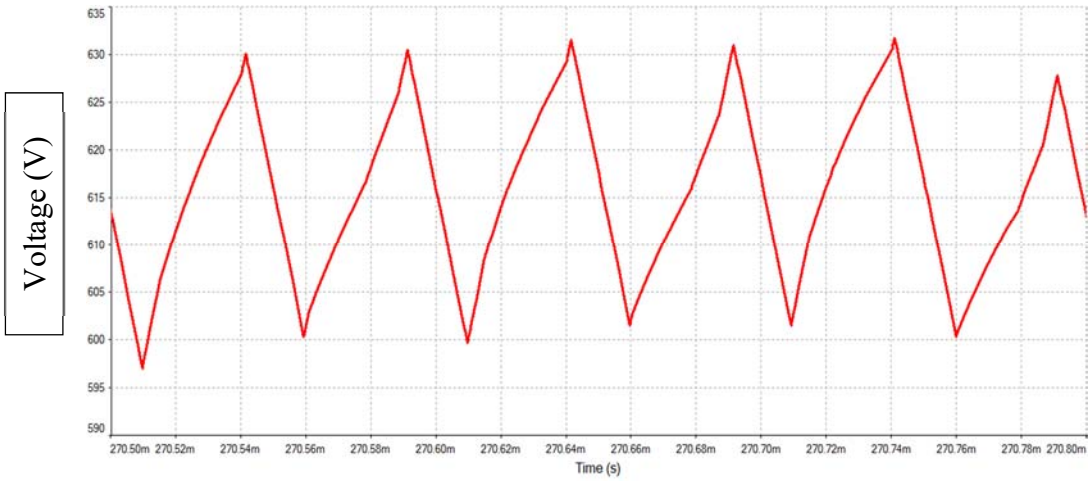

Figure 5.12: Charge & discharg for capastor voltage (V_{C1}= V_{C2}).

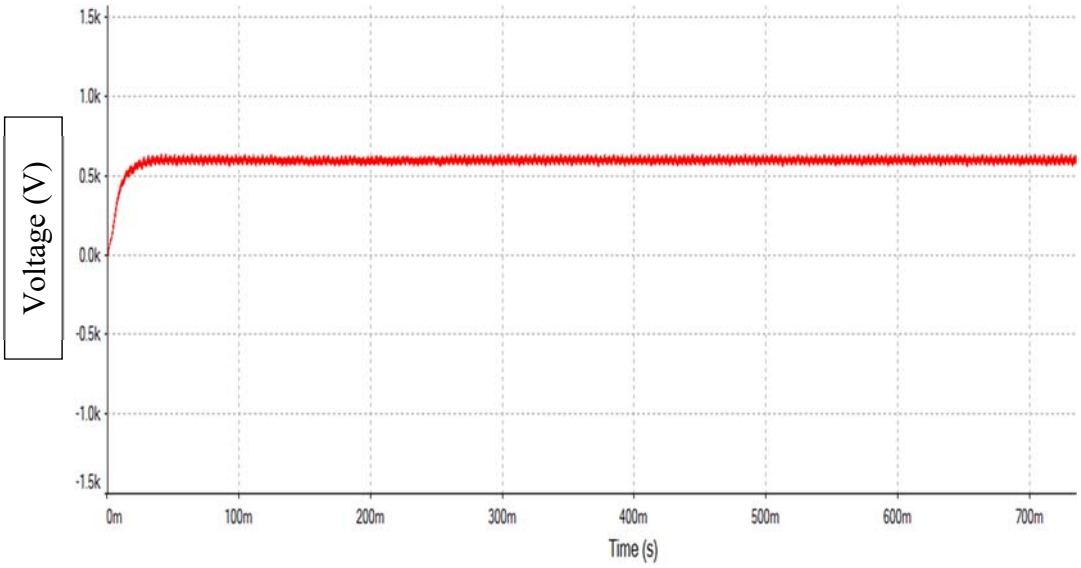

Figure 5.13: Capacitor voltage (V_{C1}= V_{C2}).

The average value of the capacitor voltage in the simulation reached 615V as shown in Figure 5.12, 5.13. While theoretically, the average value reached 620.19 V. The error rate is 0.8%.

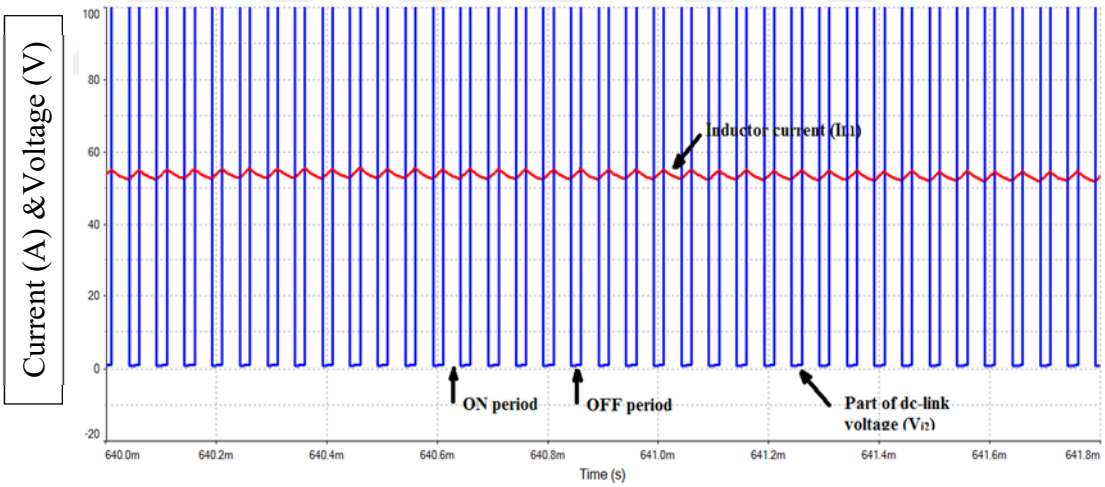

Figure 5.14: Part of dc-link voltage (V_{i2}) & charge –discharge for the inductor current (I_{L1}).

The period of charging and discharging of the inductor current is contrary to the capacitor behavior, so in Figure 5.14, the Active state period shows the discharge energy of the inductor to the load at ON period of the average dc-link voltage $\overline{V}_{i2}$, however, during the Shoot-Through states, the inductor will charge from the transferred energy from the capacitor discharge at OFF period of average dc-link voltage $\overline{V}_{i2}$. The charging and discharging process of the inductor must be almost

linearly (not sinusoidal) to reduce the ripple in the circuit and therefore reduce the harmonic content [71] as in Figure 5.15.

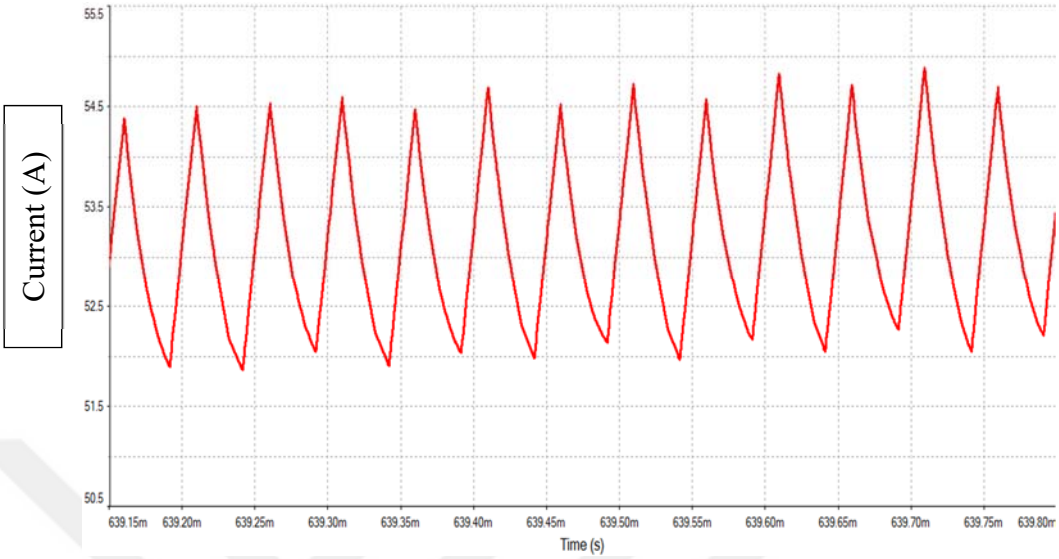

Figure 5.15: Charge & discharge for the current inductor (I_{L1}=I_{L2}).

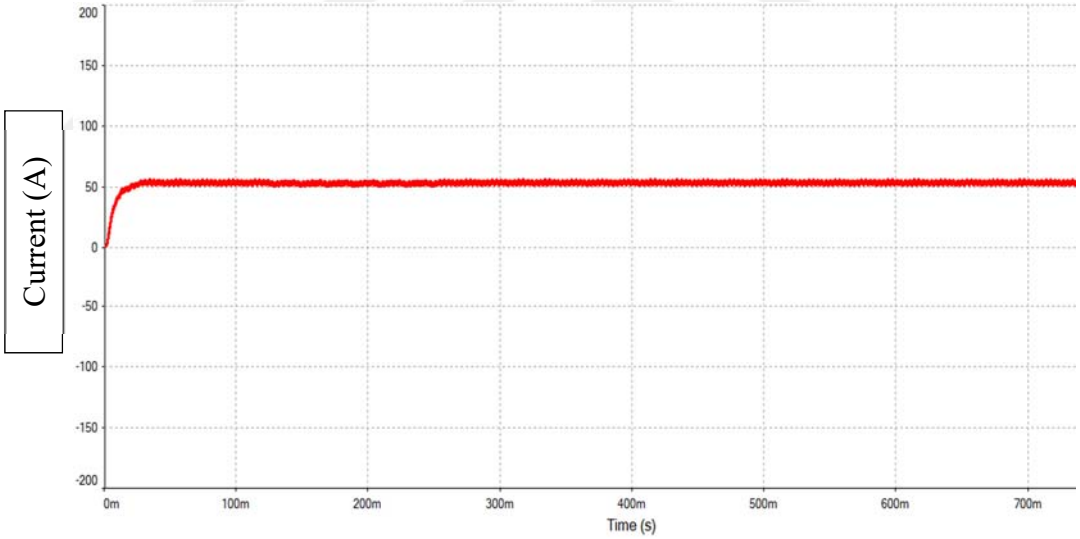

Figure 5.16: Inductor current (I_{L1}=I_{L2}).

The average value of inductor current (as in Figure 5.15, 516) reached in the simulation 53.6A; however, the average theoretical value is 54.7A, so the error rate is 2 %.

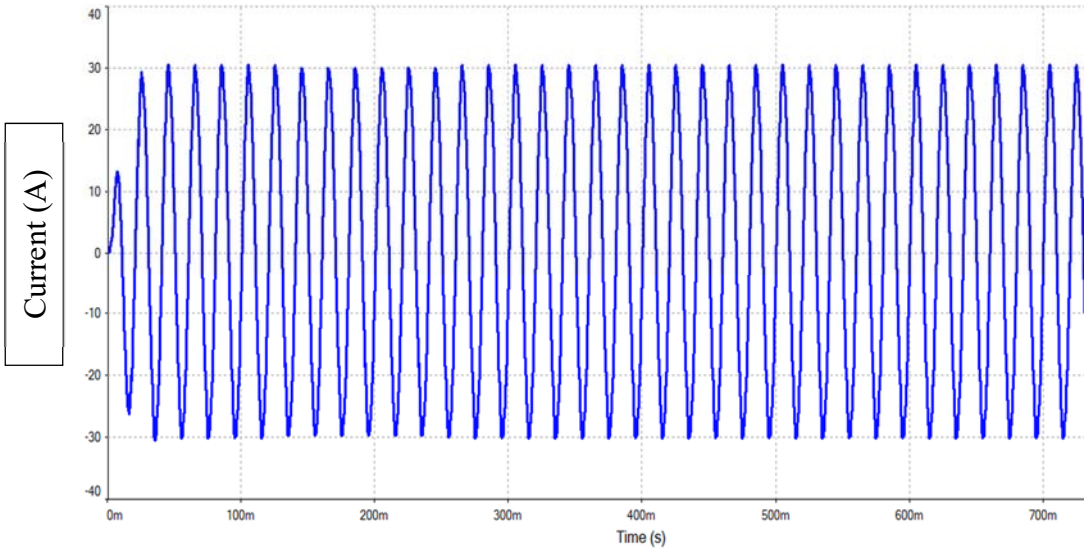

Figure 5.17: Peak current of phase (R).

The value of peak phase current I_m in the simulation is equal 30.5A (as in Figure 5.17), while, the peak phase current value in theoretical equal 31.027A, so the rate error is 1.7 %.

$$I_{RMS} = \frac{\text{peak phase current}}{\sqrt{2}} = \frac{30.5}{\sqrt{2}} = 21.57\,A$$

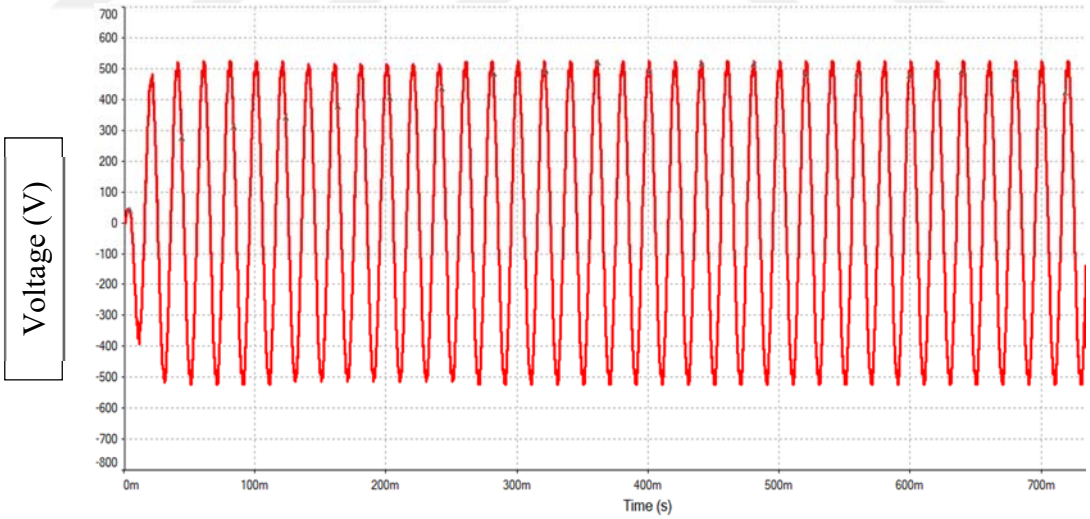

Figure 5.18: Peak to peak of (R-S) line voltage (phase S).

The peak value of line to line voltage $V_{peak\ line\text{-}line}$ equals 532V (as in Figure 5.18).

$$V_{line\text{-}line(RMS)} = \frac{V_{peak\ line\text{-}line}}{\sqrt{2}} = \frac{532}{\sqrt{2}} = 376.2V$$

However, the given value and desired to get the output is 380V_{RMS}, therefore the error rate is 1%.

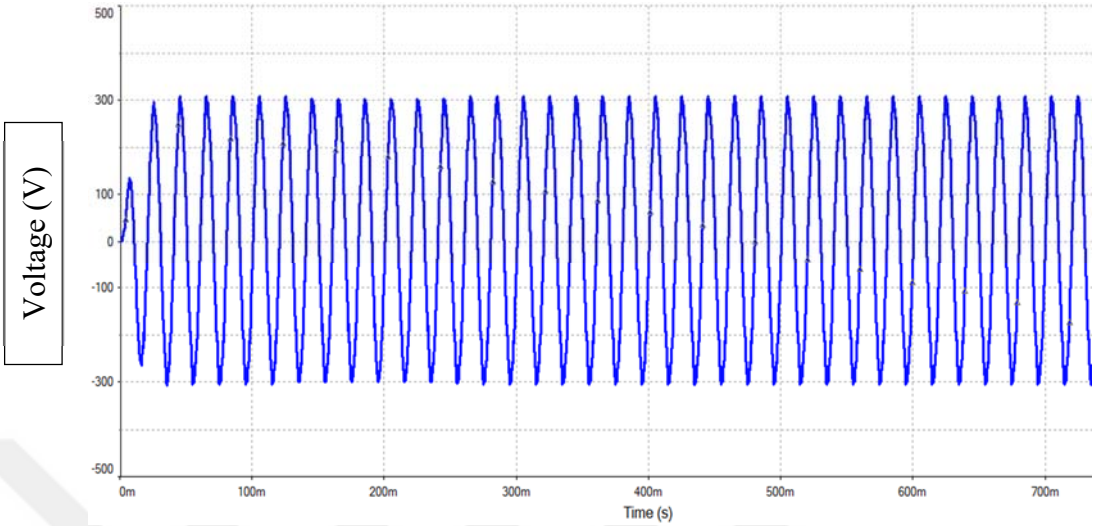

Figure 5.19: Peak voltage of phase (S).

V_m and V_{ac} the peak values of phase voltage [2], [71] that mentioned in previous equations, are equal to 307V (as in Figure 5.19) the given value and desired to get the output is V_m=310.27V, therefore the error rate is 1%. Comparing the simulation value 307V and the value from equation (20) V_{ac} = 310.1, the error rate will be 1%, and both of error rates are very small.

$$V_{phase(RMS)} = \frac{\text{peak phase voltage}(V_{ac})}{\sqrt{2}} = \frac{307}{\sqrt{2}} = 217.1V$$

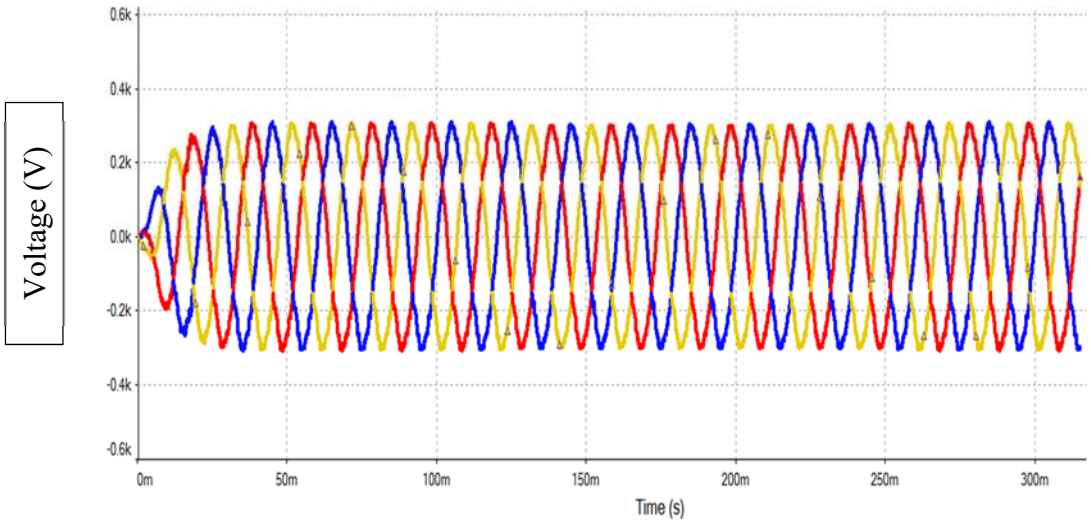

Figure 5.20: Peaks phase voltages of 3-phase(R, S, T).

Three phase peak voltage that represented in Figure 5.20 has the frequency of 50Hz.

5.5 Extension in X-shape of Switched Inductor (SL)

From the recent analysis, it can be known that X-shape of switched-inductor cells can improve the voltage gain. Based on this feature, the output voltage can be boosted by adding multiple switched inductors in every cell as shown in Figure 5.21. The operating concept is analyzed as follows.

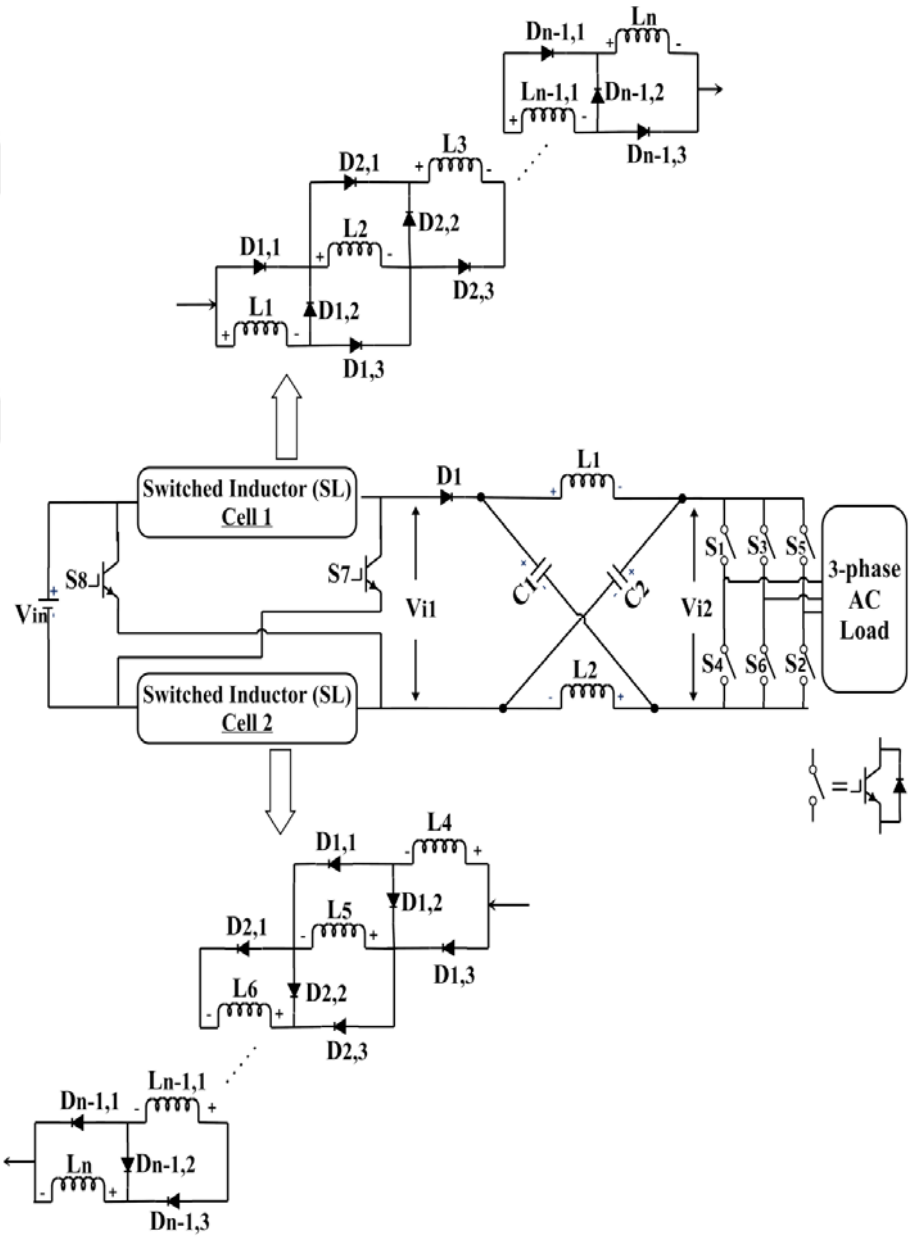

Figure 5.21: Extended X-shape SL with number (n) of inductors.

In nonshoot-thorough state L_1, L_2, L_3, L_4, L_5, L_6…..L_{n-1} and L_n will be connected in series ($L_1=L_2=L_3=L_4=L_5=L_6\ldots.=L_{n-1}=L_n$). Thereby:

$$V_{L1}+V_{L2}+V_{L3}+V_{L4}+V_{L_{n-1}}+V_{L_n}+V_{i1}=V_{in} \tag{5.24}$$

$$V_{L1}=V_{L2}=V_{L3}=V_{L4}=V_{L_{n-1}}=V_{L_n} \tag{5.25}$$

From (5.24, 5.25):

$$V_{L1}=\frac{1}{n}V_{in}-\frac{1}{n}V_{i1}=V_{L2}=V_{L_{n-1}}=V_{L_n} \tag{5.26}$$

While in shoot through state L_1, L_2, L_3, L_4, L_5, L_6..……L_{n-1} and Ln will be connected in parallel. The boost factor for n number of inductors will be:

$$V_{L1}=V_{L2}=V_{L3}=V_{L4}=V_{L_{n-1}}=V_{L_n}=V_{in} \tag{5.27}$$

By applying the volt-second balanced principle to each inductor:

$$B=\frac{1+(n-1)D}{1-D} \quad \text{When } n \geq 4 \tag{5.28}$$

Now the dc-link voltage of X-shape SL&ZSI for n number of SL will be:

$$V_{i2}=\frac{1}{1-2D}*\frac{1+(n-1)D}{1-D}*V_{in}=\frac{1+(n-1)D}{1-3D+2D^2}V_{in} \tag{5.29}$$

$$B=\frac{1+(n-1)D}{1-3D+2D^2} \qquad \text{When } n \geq 4 \tag{5.30}$$

$$V_{ac}=M*B\frac{V_{in}}{2} \tag{5.31}$$

Figure 5.22 shows the improvement in the factor boost value at a lower duty cycle by increasing the number of the inductor in every cell of X-shape of switched inductor (as shown in Figure 5.21).

From the equation 5.30, n represents the number of the inductor. By increasing the number of inductors, the boost factor will increase (condition: $n \geq 4$). For example, in Figure 5.22 at n=4 (the number of inductors is four) there is a good increasing ratio of the boost factor compared with one cell of SL&ZSI and traditional ZSI, while at n=6 the ratio of the boost factor became better than n=4, however at n= 8 the boost factor B became better compared with n=4 and n=6. So the designers can increase the number of inductors and get to L_n of inductors in every cell of X-shape of switched inductor, according to the design requirement, therefore the switched

inductor will be a series of inductors cells SL. Whoever, by increasing one inductor, a number of diodes need to be added.

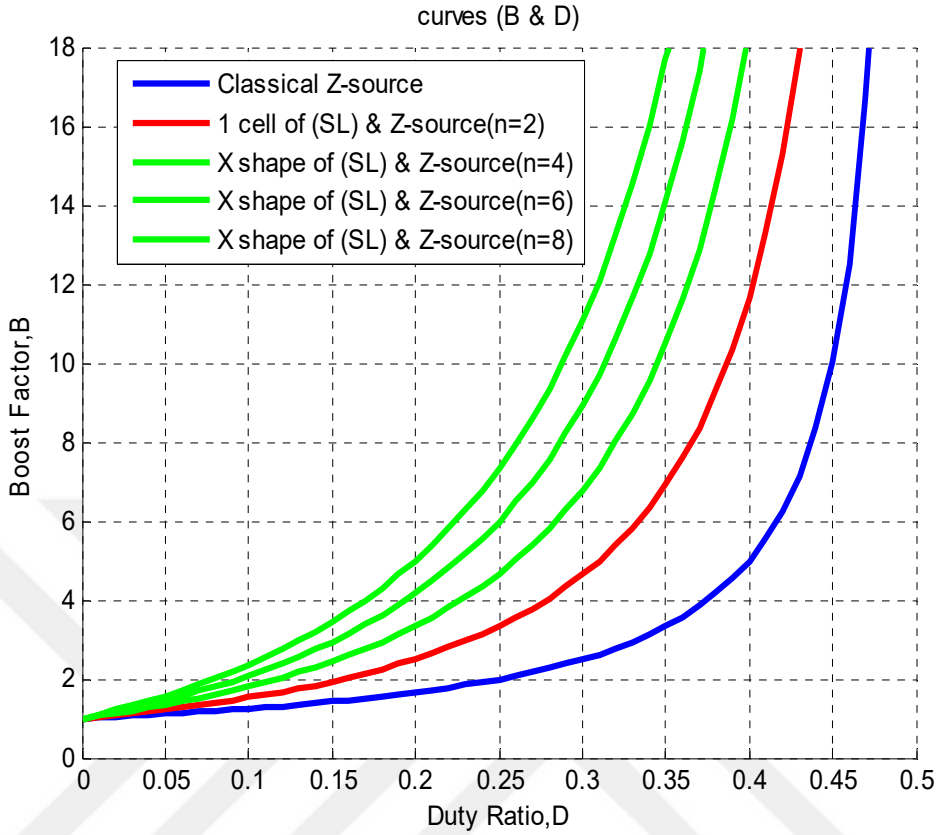

Figure 5.22: Improving the boost factor of extension in X-shape SL.

Table 5.1: Comparison between various types of Z-source.

	SL-ZSI	Classical ZSI	One Cell SL-ZSI	X Shape of SL-ZSI
B	$\frac{1+D}{1-3D}$	$\frac{1}{1-2D}$	$\frac{1+(n-1)D}{1-3D+2D^2}$ When n ≥ 2	$\frac{1+(n-1)D}{1-3D+2D^2}$ When n ≥ 4
V_C	$\frac{(1+D)Vi}{(1-3D)}$	$\frac{(1-D)Vin}{(1-2D)}$	$\frac{(1+(n-1)D)Vin}{(1-2D)}$ When n ≥ 2	$\frac{(1+(n-1)D)Vin}{(1-2D)}$ When n ≥ 4

This table compares the X-shape SL&ZSI and the one cell SL&ZSI with two different topologies and the comparison is in terms of the boost factor and voltage capacitor (V_C).

CHAPTER SIX

CONCLUSION

From the continuous improvement in the impedance-source networks topologies, the idea of this research was started to treat the weaknesses in the traditional ZSI. So In this study, the two novel proposed topologies, one cell SL&ZSI and X-SL&ZSI, are combined one or two cell switched inductor with ZSI respectively. The simulation results are obtained using MATLAB and National Instrument (Multisim) programs that are applied on both topologies. The major advantages of the two topologies are the following:

1- The boost factor is increased for I-SL&ZSI and X-SL&ZSI topologies of 133% and 266% at duty cycle, 0.4.
2- The stress voltage ratio of the capacitors is decreased up to 58% and 70%.
3- Decreased size of capacitors of 63% and 76.24%.
4- Reduced duty cycle of 12.12% and 21.6% which leads to decreased of thermal losses during the switching process.

In addition, the continuity input power is obtained; the start-up inrush current is also eliminated by the proposed topologies and wide range of gain voltage as well.

The results that are obtained from the simulation and theoretical are matched about 2%. The only disadvantage is increasing cost and size of converter. The proposed design can be further enhanced by addition of multi branches in series of inductors and diodes and can be also applied to other types of impedance source networks, especially for discontinuous input power topologies.

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