UNIVERSITY OF TURKISH AERONAUTICAL ASSOCIATION
INSTITUTE OF SCIENCES AND TECHNOLOGY

DIGITAL POWER ESTIMATION USING SUBSAMPLING ANALOG-to-DIGITAL CONVERTERS FOR COMMUNICATION RECEIVERS

MASTER THESIS

AYMEN MOHAMMED KHLEEL
1403630043

Department of Electrical and Electronics Engineering

JUNE 2017

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Aymen Mohammed Khaleel, having student number 1403630043 and enrolled in the Master Program at the Institute of Science and Technology at the University of Turkish Aeronautical Association, after meeting all of the required conditions contained in the related regulations, has successfully accomplished, in front of the jury, the presentation of the thesis prepared with the title of: "DIGITAL POWER ESTIMATION USING SUBSAMPLING ANALOG-to-DIGITAL CONVERTERS FOR COMMUNICATION RECEIVERS"

Thesis Supervisor: Asst. Prof. Dr. Ertan ZENCIR

University of Turkish Aeronautical Association

Jury Members: Asst. Prof. Dr. Hassan SHARABATY

University of Turkish Aeronautical Association

Asst. Prof. Dr. Enver ÇAVUŞ

Yıldırım Beyazıt University

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UNIVERSITY OF TURKISH AERONAUTICAL ASSOCIATION
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I hereby declare that all information in this study I presented as my Master's Thesis, called: digital power estimation using subsampling analog-to -digital converters for communication receivers, has been presented in accordance with the academic rules and ethical conduct. I also declare and certify with my honor that I have fully cited and referenced all the sources I made use of in this present study.

06.06.2017

Aymen Mohammed KHALEEL

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JUNE, 2017 Aymen Mohammed KHALEEL

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ABBREVIATIONS

ADC : Analog-to-Digital Convertor [xii].

LNA : Low Noise Amplifire [xii].

AGC : Automatic Gain Control [xii].

PVT : Process Voltage and Temperature variation [xii].

SNDR : Signal to Noise and Distortion Ratio [56].

ENOB : Effective Number of Bits [2].

RF : Bandpass signal (any modulated signal) [xii].

VSWR : Voltage Standing Wave Ratio [8].

QAM : Quadrature Amplitude Modulation [xii].

QPSK : Quadrature Phase Shift Keying [xii].

LTE : Long Term Evolution [5].

GSM : Global System for Mobile communications [8].

VGA : Variable Gain Amplifire [37].

DSP : Digital Signal Processing [73].

ABSTRACT

DIGITAL POWER ESTIMATION USING SUBSAMPLING ANALOG-to-DIGITALCONVERTERS FOR COMMUNICATION RECEIVERS

KHALEEL, Aymen Mohammed

Master Thesis, Department of Electrical and Electronics Engineering

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Assist. Prof. Dr. Ertan ZENCIR

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Abstract— The estimation of received signal power in wireline and wireless communication receiver chains is an important task since the total gain of the receiver chain is decided based on the power estimates. The setting of the receiver gain affects the noise figure of the receiver and the amount of distortion at the output of the receiver (Analog-to-Digital converter input). Adjusting the gain of several RF (Radio Frequency) and IF (Intermediate Frequency) blocks to set the overall receiver gain is carried out with Automatic Gain Control (AGC) loops, which are usually implemented as analog blocks employing analog power detection and estimation techniques. On-chip analog power estimation circuits used in RF frequencies are based on techniques such as envelope detection, and logarithmic amplification. These techniques suffer from accuracy issues such as process, voltage, temperature (PVT) spreads (primarily due to transconductance variation of core transistors), which prevents the realization of power-optimum designs. This work proposes an alternative method of measuring the power of an RF or IF signal with a subsampling analog-to-digital converter (ADC). This method presented in this thesis, which is called subsampling power estimation, being mainly digital, has a very tightly controlled power estimation characteristic unlike analog-only methods. The subsampling approach has a very low PVT spread due mainly to the sample and hold amplifier at the input stage of the ADC. Power estimation errors due to temperature variations may be compensated through self-calibration by generating a dynamically changing look-up table that would contain the power estimate vs. the digital code at the ADC output. In order to verify the validity of the

subsampling method, an MATLAB code was developed to find the power of a voice signal with amplitude modulation (AM) and quadrature amplitude modulation (QAM). The error between the Nyquist sampling and subsampling approaches is defined as the main parameter to verify the validity of the subsampling method. In simulations, it was found that the error was within approximately +0.1 dB for the power estimation of AM modulated signal, and -0.148 dB for the QAM modulated signal. Results confirm that the estimation of power of RF signals could be achieved at much lower sampling rates rather than Nyquist rate. This would reduce the complexity of power estimation circuits which results in lower design cost.

Key words: Digital power estimation, subsampling ADC, communication receivers, RSSI.

ÖZET

Kablolu ve kablosuz haberleşme alıcı zincirlerinde sinyal gücünün hesaplanması, alıcının toplam kazancının güç tahminlerine dayalı olarak karar verilmesinden dolayı önemli bir fonksiyondur. Alıcı kazancının ayarlanması, alıcının gürültü faktörünü ve alıcının çıkışındaki bozulma miktarını etkiler (Analog-Dijital çevirici girişi). Alıcının tamamının kazancını belirlemek için birçok RF (Radio Frequency) ve IF (Intermediate Frequency) blokların kazancının ayarlanması otomatik kazanç kontrol döngüleri sayesinde gerçekleştirilir. Kazanç control döngüleri analog güç bulma ve tahmin etme teknikleri kullanan analog bloklar kullanılarak icra edilir. RF frekanslarında kullanılan yonga-üstü analog güç hesaplama devreleri zarf bulma ve logaritmik yükseltme gibi teknikler temel alınarak tasarlanmaktadır. Bu teknikler proses, voltaj, sıcaklık (PVT) serpilmelerine (özellikle ana transistor transkondaktans değişimlerinden kaynaklı hassasiyet problemlerine) maruz kalmaktadır. Bu durum güç-optimize tasarımların gerçekleşmesine engel teşkil etmektedir. Bu tezde sunulan **alt-örnekleme güç tahmini metodu** sadece-analog usüllerin aksine çok sıkı control edilebilen güç tahmini karakteristiklerine sahiptir. Alt-örnekleme yaklaşımı çok düşük PVT serpilmesine sahiptir. Bu serpilmenin kaynağı da temelde analog bir blok olan ve Analog-Dijital Çeviricinin girişinde yer alan örnekle-ve-tut yükseltecidir. Sıcaklık değişimlerinden kaynaklı güç hesaplama hataları kendi-kendine kalibrasyon kullanılmasıyla telafi edilebilir. Bu kalibrasyon Analog-Dijital Çevirici çıkışındaki "güç tahminine" karşılık "dijital kod" tablosunu dinamik olarak değiştiren bir "look-up" tablosu sayesinde sağlanabilir. Alt-örnekleme metodunun geçerliliğini doğrulamak maksadıyla, genlik modulasyonlu (AM) ve kuadratik genlik modülasyonlu (QAM) bir ses sinyalinin gücünün hesaplanması için bir MATLAB kodu geliştirildi. Nyquist örnekleme ve alt-örnekleme güç tahmini değerleri arasındaki hata alt-örnekleme metodunun geçerliliğini ölçmek için temel parametre olarak tanımlandı. Simülasyonlarda genlik modülasyonlu sinyalin güç tahmini için yaklaşık +0.1 dB'lik ve kuadratik genlik modülasyonlu sinyal için ise -0.148 dB'lik hatalar elde edildi. Elde edilen

sonuçlar, RF taşıyıcı frekanslarda modulasyona tabi tutulmuş sinyallerin güç tahminlerinin Nyquist örnekleme hızlarından çok daha aşağı hızlarda başarılabileceğini doğrulamaktadır. Bu doğrulama sayesinde, güç tahmini devrelerinin karmaşıklıklarının azaltılabileceği ve bunun da daha düşük maliyetli tasarımlara kapı aralayacağı söylenebilir.

CHAPTER 1:

1. INTRODUCTION

1.1. Background

Maintaining a constant level of signal power at the output of an analog front end (the input of the ADC) regardless of the input signal level is an important design requirement which mandates strict control of each block's gain. Hence, several automatic gain control (AGC) loops are required to perform the task of adjusting the gain of their attached loop. *AGC*s are feedback amplifiers with closed-loop low-pass gain characteristics; they are responsible for providing a relatively constant output amplitude so that a circuit controlled by the loop can function with acceptably low distortion [1]. The power detector block is an important component of the *AGC* loop, which usually taps the output of the corresponding amplifier whose output power needs to be adjusted. Power detector circuits used in classical analog integrated designs are based on envelope detection where a differential amplifier is used such that the virtual ground is the full-wave rectified version of the input signal [2]. The spread in the gain of the differential amplifier and the following RC filter over process, voltage, and temperature significantly affects the accuracy of the voltage count, and thus the power estimates, which then affects the precise gain setting. Therefore, maintaining a good signal-to-noise ratio (SNR) with minimal distortion at the output of the related gain block is achieved with poor accuracy. This affects the performance of the receiver chain significantly. The negative gain errors for low input signal levels might lower the output SNR of the gain block, which in turn reduces the SNR of the entire receiver chain in terms of linearity. The positive gain errors for high input signal levels may drive the amplifier into a nonlinear region, thereby resulting in distortion. Moreover, setting the gain to levels higher than the required optimum level may significantly increase the power dissipation of the block(s). Another power estimation popularly used by analog designers is logarithmic amplification, which also suffers from the

aforementioned problems of PVT spread. Logarithmic amplifiers need to employ multiple linear amplifiers to achieve the required dynamic range, which makes them a power hungry choice for power detection [3]. Another factor that makes logarithmic amplifiers less attractive is the high temperature variation. CMOS logarithmic amplifiers are so far unable to provide a stable performance of *RF* power detection over a wide dynamic range without using sophisticated temperature compensation techniques [4], [5]. The generic analog power detection technique is shown in Fig. 1. This article suggests an alternative digital method of measuring the power of an *RF* or *IF* signal. The method is mainly based on the idea that less analog processing would mean less spread over PVT. For this purpose, the signals are directly sampled by using a low power low energy over bit (*ENOB*) simple *ADC* whose clock frequency needs to be at least double the bandwidth of its input signal.

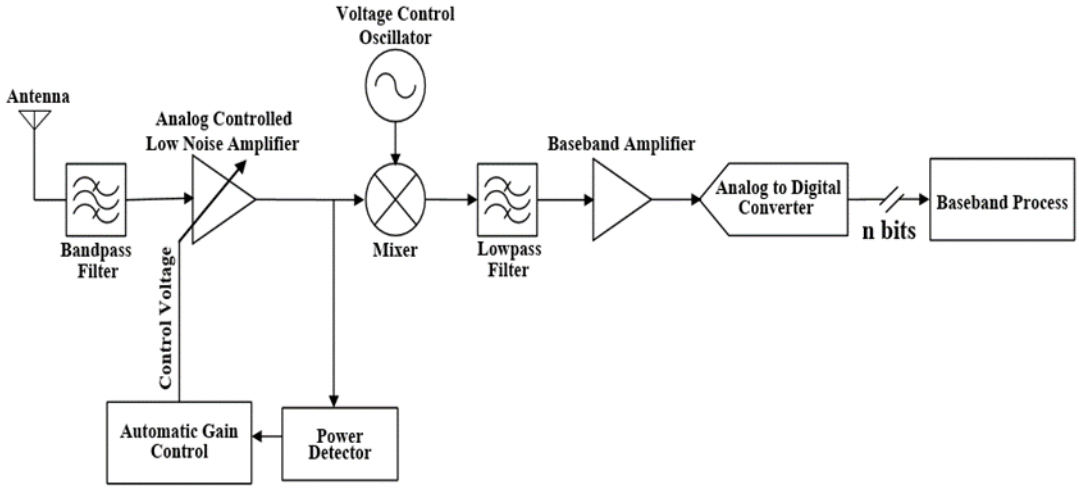

Figure 1: Analog-only automatic gain control loop including an analog power detector in a generic receiver chain.

According to Nyquist sampling criteria, the sampling rate of an analog-to-digital convertor (*ADC*) should be at least twice the highest frequency of its input signal. This necessitates very high sampling rates, especially for *RF* frequencies, which makes the *ADC* design more challenging with high power consumption, since the power dissipation is directly proportional to the sampling frequency [6]. In addition, *ADC*

clock signal jitter requirements will also be more challenging when the sampling frequency increases [7]. The Nyquist-Shannon sampling Theorem, which is the modified version of the Nyquist Theorem, states that sampling the signal at a rate double its bandwidth will be sufficient to recover the original signal from the sampled version instead of considering the doubling of the highest frequency component [8]. For example, a signal with bandwidth B with a carrier frequency fc will require a minimum sampling frequency of *2B* instead of $2(f_c + B)$ because the narrow-band signals do not change significantly during the time taken by a carrier to make one cycle. In this work, sampling of the analog signal is performed at the sub-Nyquist (or subsampling) rate directly at *RF* or *IF* frequencies. The sampled signal data is then squared and low-pass filtered (averaging) to estimate the power. The digital code representing the power estimate at the output of each block can then be used to adjust the gain of each block digitally through automatic gain control (*AGC*) loops, as shown in Fig. 2.

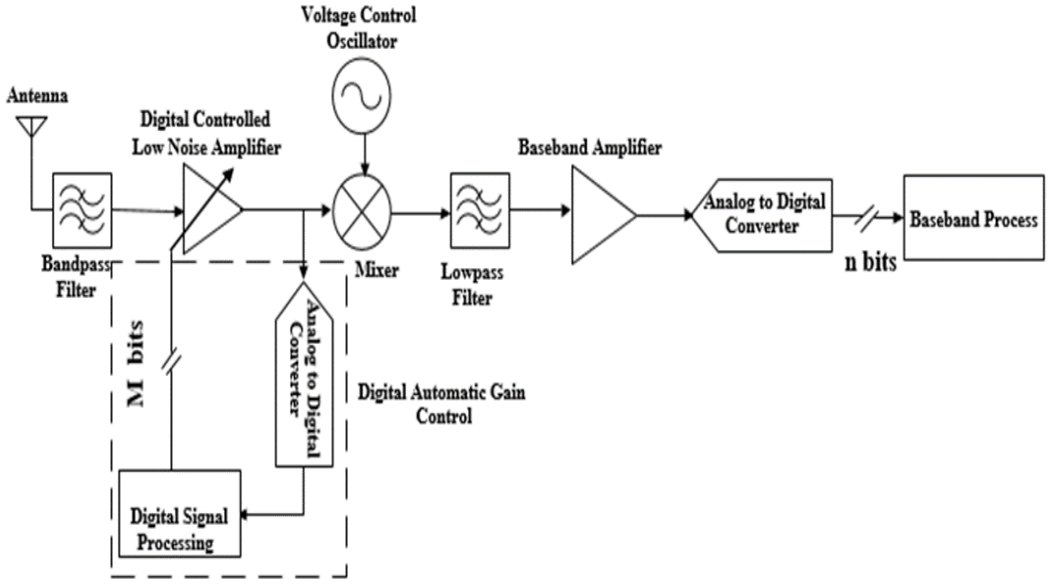

Figure 2: Digital automatic gain control loop in a generic receiver chain.

The subsampling process creates replicas of the spectrum. These replicas are spread on the frequency axis from the base band to the *RF* frequencies [9]. This process also generates extra thermal noise produced by the sampler circuit; this noise will affect the low power side of the large range for the power estimate. By looking at the sampler circuit depicted in Fig. 3, and in order to have negligible attenuation due to the thermal noise, , this circuit must have a bandwidth equal to the input frequency, f_{in} at least. Resistor R_{on} will have an integrated noise power of kT/C. The noise power added by the sampling circuit will be multiplied by a factor of $2m$ if subsampling is performed by a factor of m. Subsampling can also make the effect of noise in the sampling clock to deteriorate. It can be proven that the clock phase noise power is also amplified by m^2 [10], [11], [12]. Increasing the sampling frequency to decrease the thermal noise is not practical due to the previous introduction; otherwise, the subsampling technique will be meaningless. Instead of increasing the sampling frequency, two consecutive subsampling stages can be used to reduce subsampling thermal noise, where a relatively high sampling frequency can be set at the first subsampling stage. This leads to a lower contribution of the first sampler circuit to the folded thermal noise [13], [14]. Furthermore, the MT/C thermal noise limit can be reduced with other techniques (which will not be discussed here) [15].

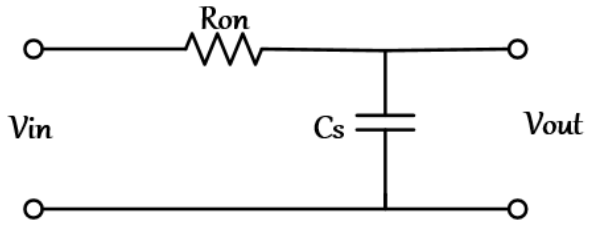

Figure 3: Equivalent circuit of sampler.

1.2. Literature Review

Diode detectors (used in envelop detection) have a better operation bandwidth and less plan area in implementation, which results in the cost advantage if it is compared to the FET counterparts. The Schottky diode is widely used for frequency mixing and RF power detection [16], [17], and the GaAs Schottky diode is used for terahertz (THz) spectroscopy in order to increase the operating bandwidth [18]. However, diode detectors have a significant uncertainty in determining accurately the dynamic diode turn-on characteristics when it deals with low-level signals in a precision operation. In high frequency cases, power dissipation increases in order achieve the required signal level by providing sufficient high-frequency gain. Moreover, dynamic range improvement will be a trade-off with sensitivity and power dissipation according to the method that is used for the improvement, which are either increasing the diode's video resistance or increasing the bias current [19]. Temperature is another effective parameter which needs compensation techniques such as enhancing the matching input network and using a supplemental DC bias current. Using each one of these solutions is related to the presence of low or high temperature conditions [20]. Unlike diodes detectors, FET transistors used for envelop detection increase the accuracy when used in precision applications at very high frequency due to the closed-form expressions that describe the transfer characteristics of the FET circuit [21]. These envelop detectors can function well with low dynamic range modulation schemes, while using it with high peak-to-average modulation schemes will lead to inaccurate measurements. In modern communication systems such as 4G, 5G and LTE, signals may have a high peak-to-RMS ratio (crest factor) that reaches 10 to 15 dB. For such operating conditions, RMS power detectors offer accurate measurements within ±0.2 dB, with a high linearity of ±1 dB over a 40-decibel range and GHz operating area. RMS power detectors can be implemented based on different power detection methods, including thermal detection, diode detection, and translinear detection methods [22], [23], [24], [25]. The log detector provides a very high dynamic range compared with the other power detectors, typically (60 dB-120 dB) and this is the

main feature for this detector over the others. It is used widely in radar application systems for its high dynamic range and the constant false alarm rate properties that it has [26], [27]. Similar to the other power detectors, temperature is one of the main limitations that need to be compensated for in a log detector [28]. Moreover, these detectors are power-hungry detectors since they are implemented with a progressive compression technique over a cascaded amplifier chain [29]. However, all the previous power detectors are suffering from the PVT issue since they are based on analog topologies. This fact is the core reason to suggest the digital power estimation method in this study, where less analog processing would mean less spread over PVT.

1.3. Scope of Research

In this study, based on the subsampling approach, a digital power estimation method is introduced. This method is proposed to be the alternative for the analog power detection techniques. Therefore, we defined first the main concept for this method, which is the subsampling technique. This technique provides us with the discrete-time version (samples) of the given continuous-time signal, then, by using these samples, the signal power is being calculated and used to adjust the gain of a VGA. For the design purposes, a practical model for this method have been introduce, which is consist of multiple units that include filters, ADC with relatively low clock rate and code calculation block. In order to verify the validity of the proposed subsampling method, an MATLAB code was developed to find the power of different amplitude-modulated signals. The error between the Nyquist sampling and subsampling approaches is defined as the main parameter to verify the validity of this subsampling method. Finally, we have discussed the optimal sampling frequency selection method and illustrated the minimum sampling frequency that could be considered besides the effects of increasing it above the minimum value.

1.4. Thesis Overview

Chapter 2 contains the theory part that presents the different power detection techniques in detail, including the features and drawbacks for each technique. At

the end of the chapter, there will be a quick review of AGC circuit configuration and the principle of the work. Chapter 3 is a review of sampling theory. Additionally, the formulas and relationships for time and the frequency domain of sampling and reconstructing the signal are derived. The subsampling (bandpass sampling) concept is introduced in detail. Chapter 4 illustrates the proposed method for power estimation, including circuit configuration, work principles, mathematical formulas for computing the power value of a given signal, and finally the simulation results using the MATLAB software. In Chapter5, the conclusion and a brief discussion of future work are presented.

CHAPTER 2:

2. RF POWER DETECTION

A power detector is an electronic circuit that converts input RF power into a new form of DC voltage which is directly proportional to the input power via the RMS or logarithmic relationship. Moreover, a power detector can represent the oscillating signal in an envelope form by detecting the peak values of the input signal. These detectors are mainly used to measure and control the power in wireless systems for regularities, proof-of-design, safety, power amplifier linearization, and many other applications. This occurs when the detector is included within the AGC circuit. RSSI in mobile systems, for example, is used to control the incoming power and keep it at a desired level for the ADC and demodulator circuits. VSWR is another fundamental measurement that can be achieved with the use of a power detector circuit for high-power RF amplifiers to avoid the signal reflections from an antenna. These reflections are caused by the impedance mismatch, which causes severe damage to the amplifier. In the receiver chain, power detectors are used along with the LNA in order to guarantee that the signal level is not very high to be cut due to the op-amp saturation, and not very low to be within the noise level.

2.1. Envelop Detection

The envelop of a signal is the smooth curve that connects all the positive peaks of an oscillating signal. From the signal processing perspective, it is the low-frequency or DC-version of the oscillating signal (see Figure 4).

The envelop detector is an electronic circuit that rectifies an input oscillating signal and produces its envelop by detecting only the positive peaks of the oscillating signal. This can be done by using either a diode or a transistor. These types of detectors perform well when a constant envelop or low crest factor modulated signals are considered, such as GSM. However, it cannot produce the same good performance for a high peak-to- RMS ratio for modulated signals found in WCMDA and LTE.

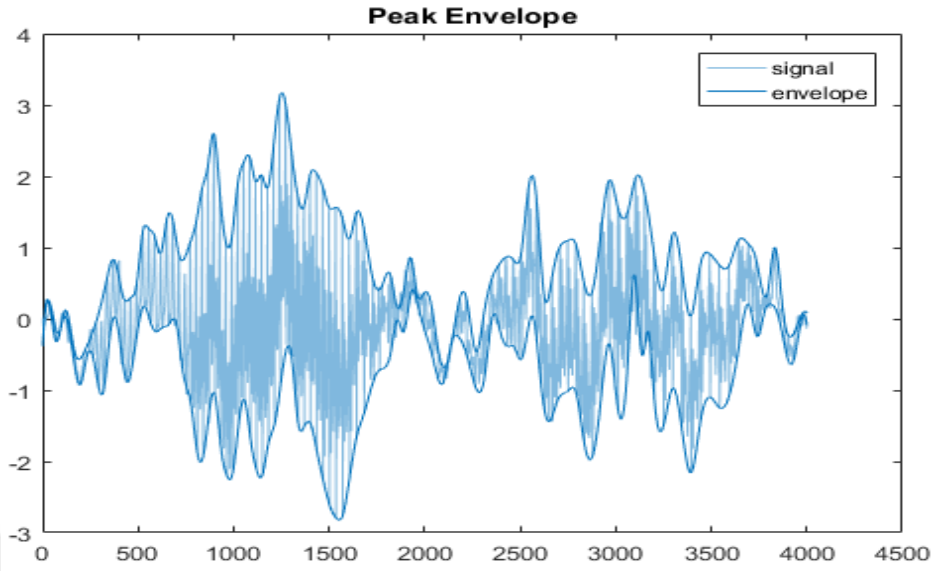

Figure 4: Envelop of an oscillating signal.

2.1.1. Diode Envelop Detector

In Figure 5, the RF input signal is detected by the diode to be a DC voltage signal. This is done according to the diode operating concept, where the diode acts as a nonlinear element that passes the current in one direction and prohibits it in the reverse direction. Hence, the diode will connect all the positive peaks of the oscillating signal to form the envelop of the input signal, and prohibit the flow of negative peaks. This process called signal *rectifying*. A capacitor will smooth the rectified signal and filter it from the RF combined signals. The capacitance value will be according to the input signal bandwidth such that the signal will not filtered out due to the low cut off frequency. The direction of the diode will matter only when the rectified signal feeds back to the AGC circuit; otherwise, the positive or negative envelop signal could both be used, for example, for audio detection.

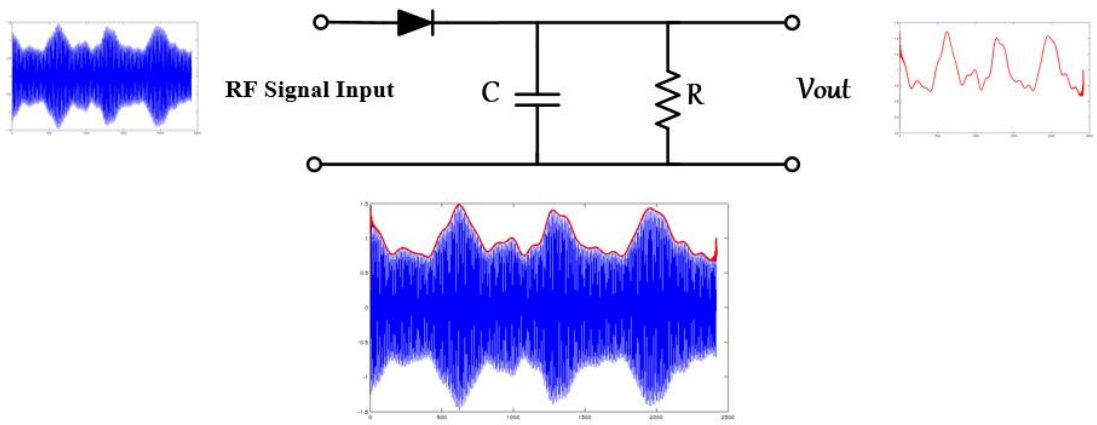

Figure 5: Basic diode detector circuit.

In order to detect the positive and negative carrier cycles, two diodes are often used. At the other hand, this makes the circuit relatively insensitive to even harmonic distortion (see Figure 6). The DC voltage signal at the output is proportional to the input signal power at low levels and it is proportional to the peak RF voltage when a high-level signal is present. Mega-ohm load resistor are used when high sensitivity is required.

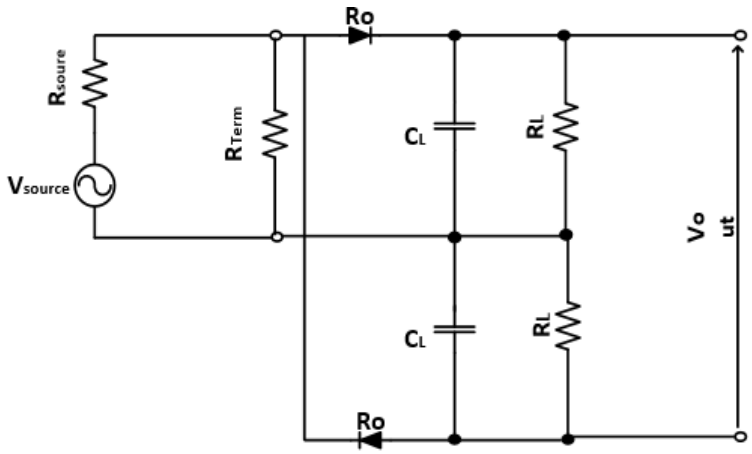

Figure 6: Dual diode power detector.

When the RF input is insufficient to make diodes the pass saturation current in the forward direction (less than -20 dBm, 30mV peak carrier voltage), diodes act as nonlinear resistors (see Figure 7) [30]. In this case the output signal is proportional to the squared RF input signal voltage and this is called the “square-

law" region of the diode detector. If the input signal peak power is within this region, then the RF average power may be measured by considering the average of the output DC voltage, and this is also true for a modulated signal.

For a signal level greater than 0 dB (300-millivolt peak input voltage), the detector circuit acts as a peak detector, and the diodes will be able to pass the saturation current in the forward direction for the positive cycles of the input oscillating signal. The output DC voltage is equal to the peak RF input voltage minus the voltage drops at each diode (see Figure 7).

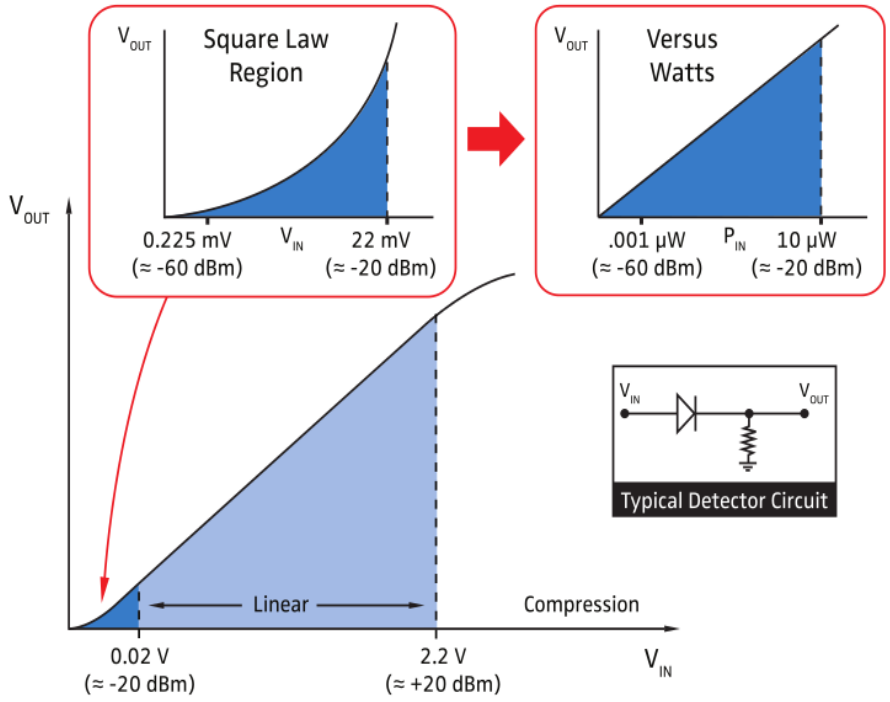

Figure 7: Square-law, linear and compression operating regions of the diode detector [30].

Diode detectors have a large dynamic range; however, since there are two regions of operation, the detector response will not be linear across the entire dynamic range. Moreover, diode detectors are very sensitive, and with the use of digital techniques, they can be linearized easily. However, when a modulated signal has a peak with an amplitude exceeding the limits of the square region, diode detectors will be challenged wherever these peaks enter the peak detection region.

In this case, the detector output voltage tracks the peaks of the signal, and while the capacitor is discharging, the output voltage will not be able to track the peaks within this time. Therefore, the average power of the RF signal cannot be measured within the peak region of the diode detector.

To solve this problem, the resistor value may be chosen such that the output voltage signal decay time decreases and the output voltage signal will be sufficiently fast to follow the envelop fluctuations of the input modulated signal. This may be done through the decrease of the load resistance and capacitance (R_L, C_L) after the diodes in Figure 6. It is possible to linearize the output signal in real time and perform filtering when the detector is sufficiently fast to track the signal envelop without any lagging (see Figure 8). For such a fast diode detector, the instantaneous and average power of a given modulated signal may be measured so long as the power is within the dynamic range of the detector [30].

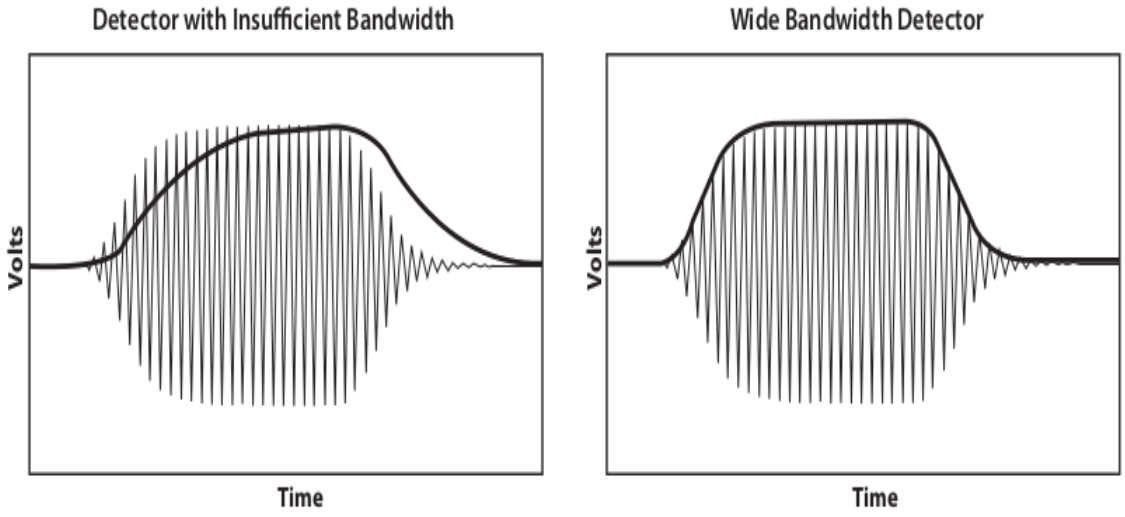

Figure 8: Using a wide bandwidth detector to track the signal envelop correctly [30].

2.1.1.1. Schottky Diode Detector Circuit

In Figure 9, a half-wave rectifier represents the fundamental Schottky detector circuit. The incident RF oscillating signal alternatively causes the Schottky diode

to be forward and reverse biased. In the case of forward bias, the filter capacitor charges until the voltage across it equals the input voltage value.

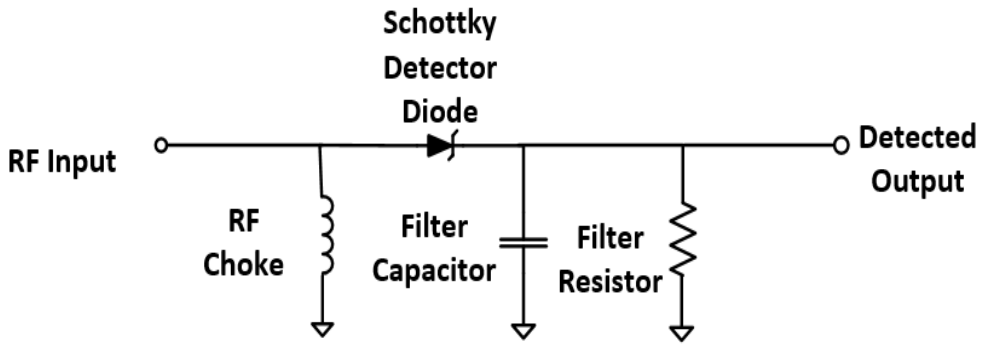

Figure 9: Schottky Diode Detector Circuit.

There are multiple detector circuit configurations, most of which contain more than one Schottky diode. This improves the detected output voltage. One of the basic Schottky detector circuit configurations is the voltage doubler detector circuit (see Figure 10).

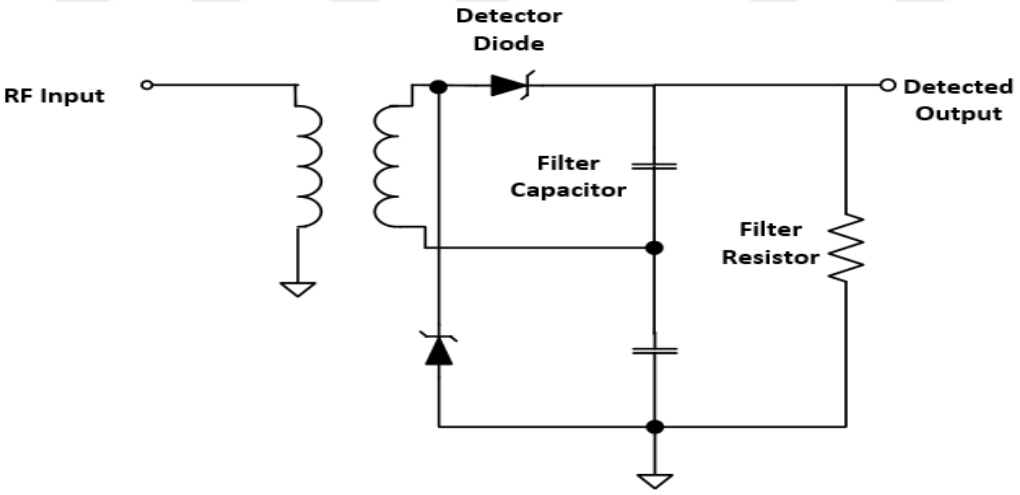

Figure 10: Schottky Diode, Voltage Doubler Detector Circuit.

The Schottky diode junction operates with a majority of carriers without minority ones, unlike the p-n diode. This advantage slows the recovery time of the Schottky diode when the applied signal changes its polarities causing forward and reverse biasing of the Schottky diode. Moreover, due to the change of input signal polarity,

the impedance changes virtually instantaneously enabling the Schottky diode to have a wide frequency operating area. The significantly low forward voltage of the Schottky diode with respect to the p-n junction diode adds another advantage to these diodes such that they are more sensitive than the p-n junction diodes. Figure 11 shows a comparison of sensitivity and operating bandwidth for different Skyworks' Schottky detector diodes **[**31].

Minimum Detectable Signal (dBm)	Barrier Height	Input Signal Frequency Range	Maximum Capacitance (pF)	Configuration	Base Part Number
-52	ZBD	Up to 30 GHz	0.25	Chip, ceramic packaged	CDC7630
-56	ZBD	Ku band	0.15	Chip, ceramic packaged	CDC7631
-60	ZBD	Up to 10 GHz	0.3	Single junction, reverse series pair, series pair, and unconnected pair, plastic packages	SMS7630
-60	ZBD	Up to 100 GHz	0.3	Single junction flip chip	SMS7630
-50	Low	Ku band	0.15	Chip, ceramic packaged	CDB7620
-53	Low	Ku band	0.1	Chip, ceramic packaged	CDF7621
-53	Low	X band	0.3	Chip, ceramic packaged	CDF7623
-53	Low	Up to 10 GHz	0.25	Single junction, common cathode pair, reverse series pair, series pair, and unconnected pair, plastic packages	SMS7621
-53	Low	Up to 100 GHz	0.18	Single junction flip chip	SMS7621
-52	ZBD	Ku band		Beam lead, ceramic packaged	DDC2353
-56	ZBD	Ku band		Beam lead, ceramic packaged	DDC2354
-50	Medium	X band	0.15	Beam lead, ceramic packaged	DDB2503
-50	GaAs	Up to 150 GHz	0.04–0.07	GaAs single junction flip chip	DMK2790
-48	Medium	Ku band	0.1	Beam lead, ceramic packaged	DDB2504
-47	Medium	S band	0.30–0.50	Beam lead, ceramic packaged	DME2127
-45	Medium	K band	0.1	Chip, ceramic packaged	CDE7618
-45	Medium	Ku band	0.15	Chip, ceramic packaged	CME7660
-45	Medium	K band	0.1	Beam lead, ceramic packaged	DME2458
-45	Medium	Ku band	0.05–0.15	Beam lead, ceramic packaged	DME2333
-45	Medium	S band	0.3–0.5	Series pair, beam lead, ceramic packaged	DME2050
-40	High	X band	0.15	Chip, ceramic packaged	CDP7624
-40	High	K band	0.1	Beam lead, ceramic packaged	DDB2265

Figure 11: Schottky Detector Diodes [31].

2.1.1.2. Features and Drawbacks

The Schottky diode is used as a detector and mixer as well as for power levelling for wireless LAN detectors, cellular phones, 24GHz radar systems, video detectors, etc. The RF performance (bandwidth) of diodes and the smaller plan area makes them often preferred and superior to that of FET circuits. The Zero Bias Schottky diode detector is widely used in RF and other applications. GaAs Schottky diodes are used to increase the operating bandwidth in terahertz (THz) spectroscopy [18]. The Schottky junction is widely used in frequency mixing and RF power detection circuits, due nearly to the ideal performance of Schottky diodes [17]. Furthermore, peak detectors utilizing nonlinear diode characteristics have long been used in electronic systems. They have the advantage of simplicity and high frequency capability. However, in order to use these detectors for precision operation, it generally requires high signal levels in order to overcome the uncertainties in determining accurately the dynamic diode turn-on characteristics. Moreover, when using diode detectors, the power dissipation will significantly increase at high frequencies in order to provide sufficient high-frequency gain to achieve the required signal level [21].

- Dynamic range: The square law dynamic range of Schottky diode detectors is defined as the difference between the power input for a 1-dB deviation from the ideal square law response (compression point) and the power input corresponding to the tangential signal sensitivity (TSS). In order to increase the dynamic range, the spacing between the TSS and the compression point should be increased (see Figure 12) [19].

The compression level can be raised by reducing R_L, the load resistance; however, this will degrade the sensitivity by

$$R_L/(R_L + R_V) \qquad \text{Eq. 3}$$

R_L : Diode video resistance.

This degradation in the TSS exceeds the improvement in compression; therefore, there is no improvement in the square law dynamic range. Increasing the bias current raises

the compression level, but it also degrades the sensitivity. Nevertheless, the improvement in compression exceeds this degradation in sensitivity; hence, the square law dynamic range is increased. However, increasing the bias current will cause the power consumption to increase, too [19].

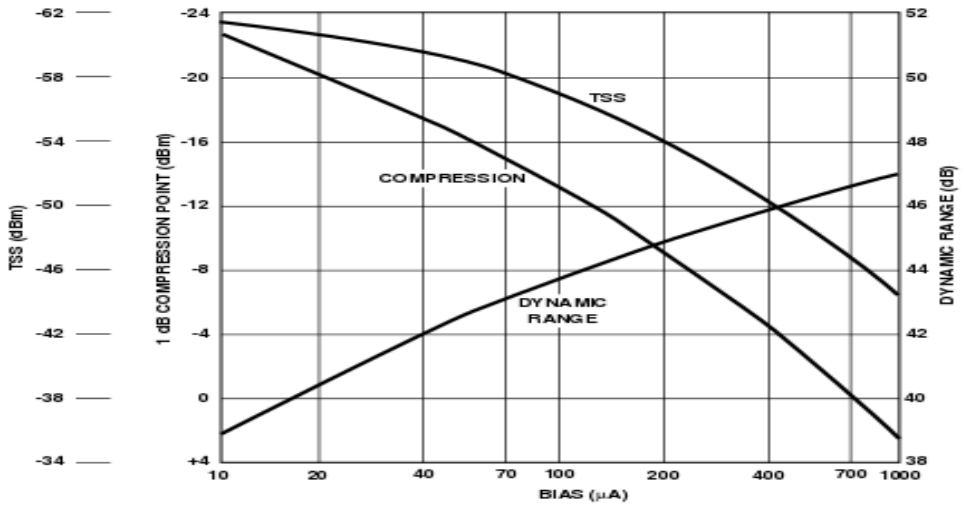

Figure 12: Dynamic range improvement with bias, [20].

- Sensitivity: This can be increased by decreasing the saturation current I_S.This happens when the video resistance R_L increases. However, there is a limit to improving the sensitivity such that when the resistance is so large such that it cannot be matched. An optimum diode is designed to have the proper saturation current. The choice of decreasing the saturation current involves a compromise between sensitivity due to high resistance and the losses due to matching. The disadvantages of using a resistor and DC biasing are the increase of power consumption and the 1/f generated noise.
- Temperature effect: At a relatively low temperature compensation, the use of a supplemental DC bias current is a possible solution to poor video bandwidth and low sensitivity. High temperature compensation can be performed by

providing a perfect matching at the input network as the impedance mismatch is the major cause of poor voltage sensitivity at 85° C [20].

2.1.2. Envelop Detector Using Transistors

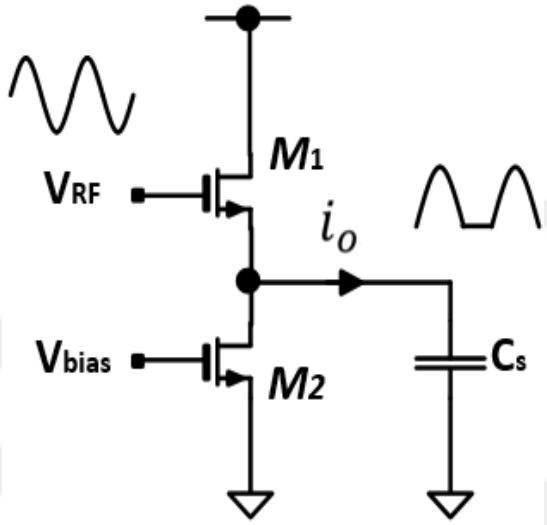

Figure 13: CMOS envelop detector scheme.

Figure 13 shows a basic schematic of an envelope detector, which is the CMOS version transferred from the bipolar one [21], [32]. M1 is biased in a subthreshold, where it provides a maximum nonlinear transfer function. M2 is a constant bias current source; this keeps the M1 gate bias voltage V_{gs0} constant. At capacitor C_s, the detector output is shown. The capacitor is charged by the output current i_0 and it provides the grounding path to the RF signal. M1 performs the nonlinear transfer function from voltage to current to detect the RF signal, and depending on how abrupt the nonlinear transfer function is, the detector efficiency will be affected directly. MOS transistors show an exponential nonlinearity at room temperature in the subthreshold region of operation.

2.1.2.1. Detection Mechanism

If an NMOS transistor is used in subthreshold region for power detection, then the $I_d - V_{gs}$ characteristic is:

$$I_d = I_{d0}\, e^{V_{gs}/V_0} \qquad \text{Eq.1}$$

where $V_0 = nkT/q$, 1<n<2 and V_{gs} can be given by

$$V_{gs}=V_g + V_{gs0} \qquad \text{Eq.2}$$

V_{gs} : Gate-source voltage.

where $V_g$is the same V_{RF} represented in Figure 13, the low signal voltage. For small deviations from V_{gs0} (small amplitudes of V_g), and by assuming any DC bias being included in I_{d0}, Eq.1 can be expanded to :

$$I_d=I_{d0} + \frac{d\, I_d}{d\, V_g} V_g + \frac{d^2 I_d}{d\, {V_g}^2} \frac{{V_g}^2}{2} \qquad \text{Eq. 3}$$

then, the second derivative will be

$$\frac{d\, I_d}{d\, V_g} = \frac{I_{d0}}{{V_0}^2} \qquad \text{Eq.4}$$

For an applied unmodulated RF signal, $V_g = V_s \cos(wt)$, and the quadratic term above can be expanded to be $\cos^2(wt) = (1 + \cos 2wt)/2$. Thus, to calculate the wanted incremental component in the output signal current i_0, which is dependent on the amplitude V_s, then:

$$i_s = I_{d0} \frac{{V_s}^2}{4{V_s}^2} \qquad \text{Eq.5}$$

Different components of noise are added to the output current. These noise components originate from the transistor channel, a baseband noise which is transferred without frequency conversion, and the noise from the RF that is down converted to the baseband. The transistor channel noise is related to the bias current; therefore, it does not change with the change of the input signal level, and consequently, it will be kept constant in this circuit. By connecting the input to the

ground at the baseband frequency, the baseband noise may be kept to low levels. The noise component originating from the RF frequency is down converted to the baseband when it is combined with the carrier or the in band blocker. Large blocking signals have a significant effect on the bias conditions of the transistor, and this will increase the detector sensitivity, while also risking the transistor to be pulled out of the subthreshold region. By keeping the bias current (DC current) generator constant in the circuit, the transistor channel noise and the sensitivity can be expected to be unaffected by the blocker power [32].

2.1.2.2. NMOS Envelop Detector: Features and Drawbacks

Closed-form expressions for the transistor-base envelop detector transfer function characteristic allow its use in precision applications at a very high frequency, unlike the diode-base envelop detectors, which require fairly large signal levels for precisions operation [21]. However, this envelop detector suffers from the PVT issue, where it is very sensitive to temperature and bias variations. In [33], a dummy envelop detector is used to feed the other input of the differential amplifier with an equal DC voltage while it is under the PVT variations, and the differential amplifier will amplify the difference signal.

2.2. Root Mean Square (RMS) Power Detectors

Envelop power detectors are designed for constant envelop modulated signals, such as the Global System for Mobile communications (GSM) signals. Therefore, these detectors cannot be used for accurate measurements of a high peak-to-average ratio modulated signals. RMS power detectors, which are based on the average power measurement, are particularly suited to accurate power measurements of RF modulated signals that exhibit high peak-to-average ratio or noise-like property. RMS power detectors are usually realized by using methods of thermal detection, diode detection, and translinear detection [22], [23] [24] [25]. RMS power detectors produce a DC voltage signal proportional to the log of the input signal RMS value

in a linear relationship. Within a 40 dB range, it may provide a linearity of better than ∓1 dB. In addition, it can function well within the GHz range. Accurate measurements of ∓0.2 dB may be achieved for even high crest factor RF signals that are found in CDMA/WCDMA, WimAX, OFDM and higher level QAM modulation systems. These systems can produce a 10 to 15 dB crest factor in 3G, 4G, 5G and LTE wireless devices implemented in smartphones and cellular base stations.

2.2.1. Thermal Detection Method

The most basic design of thermal sensors was in the "light bulb" power detector by Ernst Lecher toward the end of the 1800s. These thermal-sensors absorb the input RF energy and generate an increase of heat in a terminating load. The increase in temperature in the terminating load is measured and calculated using a direct or indirect method, followed by computation of the conforming input power.

For RF power measurement equipment, the thermal detection method is widely used. It compares the heat value generated by an unknowing AC signal with a known heat value generated by a calibrated reference DC voltage (Figure 14). The advantages of this method are the wide bandwidth and the low measurement errors produced [22], [23]. However, the realization of thermal detection is complex and expensive, and it is not suitable for integration with the low-cost CMOS process.

A thermistor (Bolometer, see Figure 15) acts as an RF load from one side, and as the temperature measurement device from the other side, as illustrated in Figure 14. The thermistor's resistance varies according to the temperature; thus, by detecting the in-circuit resistance, it is easy to measure its temperature.

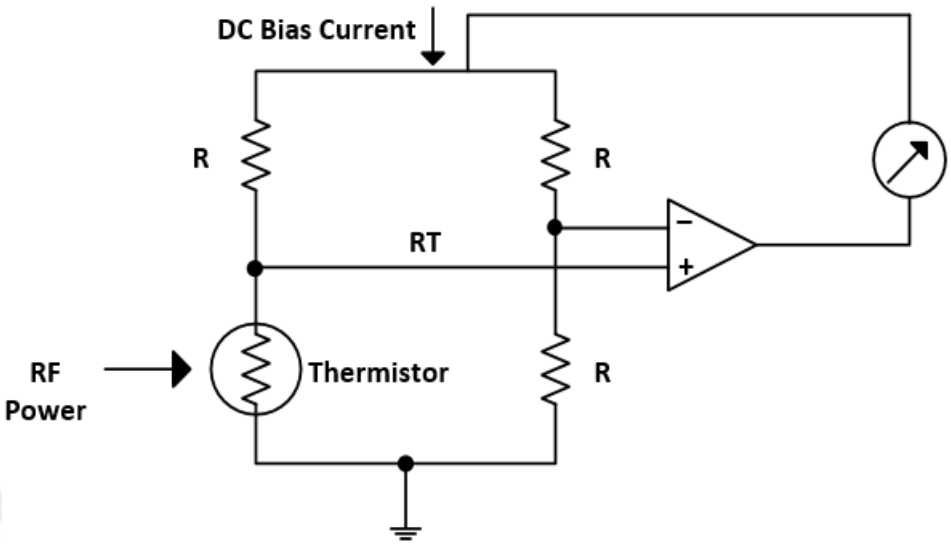

Figure 14: Thermistor Sensor Diagram.

Putting the thermistor element in one corner of a wheat-stone bridge is one of the common and basic practices. Thermistor resistance should be at the same value as the other resistors in the bridge to ensure balance. A (DC) substitution circuit is used for the purpose of balance, where a DC bias current is used to heat the thermistor and increase the temperature; thus, the thermal resistance will be sufficiently increased to be equal to the other resistors in the bridge. The thermistor resistance should be at the correct value in order to properly terminate the input RF signal, typically $50\ \Omega$ or $100\ \Omega$.

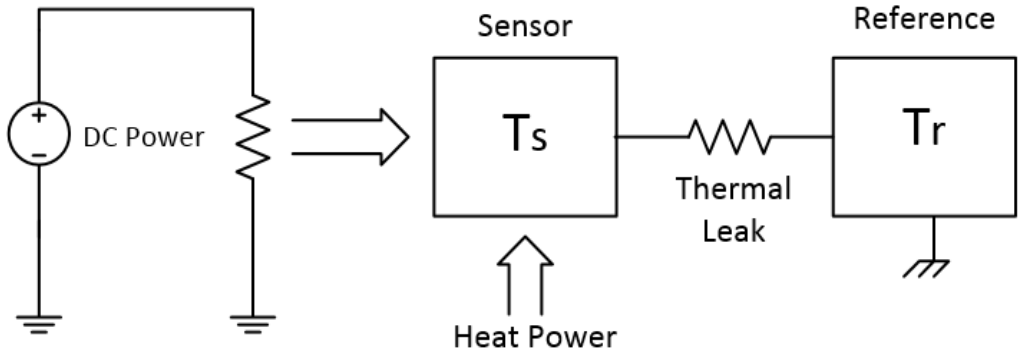

Figure 15: Bolometer diagram.

The input RF signal power plus the power from the DC bias current is equal to the total power dissipated by the thermistor. The power consumption in relation to the RF signal heat can be calculated easily (since the bridge is in balance) by subtracting the DC reference power that is equal to 1/4(V_{bridge}*I_{bridge}) from the total dissipated power. The remaining three resistors are designed to have a negligible temperature coefficient due to resistance.

Practically, another thermistor bridge is used (the first thermal bridge is exposed to the RF signal) to cancel the temperature changes of the environment. The RF signal power will be dissipated in the terminated load of a thermocouple sensor; accordingly, the increase in the temperature is calculated. The temperature increases because of the thermocouple concept.

The output-generated voltage from the thermocouple-sensor is linear with the input power, and due to heat flow delays, it has a relatively long time constant. This means that the obtained readings are proportional to the average power of the input RF signal. Therefore, these sensors are widely used for modulated signal average-power measurements. However, the sensitivity is a major disadvantage for the thermal detection method in the RF measurement usage (for signals lower than microwatts level).

2.2.2. Diode Detection Method

Diode detector circuits need to function with constant envelop signals. However, calibration ensures that the detector will perform well at a fixed peak-to-average ratio. In this case, for instance, QPSK is the only modulation scheme used by a communication system; then accurate power measurements can be made through the use of diode circuits. However, in systems with varying crest factors, such as CDMA or WCDMA, true RMS measurements become difficult to realise. Theoretically, different look-up tables may be used to solve this problem. This is based on the call loading at the base station (to notify with the crest factor for a specific channel). However, the calibration of a base station for every call loading is unpractical. In multi-carrier systems, it becomes impossible with this virtual

solution, where the crest factor of multiple carriers is changing for each carrier independently [34].

2.2.3. Translinear Detection Method

The translinear concept is a simple and smart method to realize complex mathematical functions by implementing a small number of transistors. All the input and output signals are current signals and the voltage changes need to be ignored while analysing translinear circuit behaviour. Static and dynamic translinear principles for nonlinear analog circuits are discussed in [35], [36], with systematic analyses and practical applications.

Depending on the translinear principle, an RMS detector has two essential units: a squarer-driver and low-pass filter circuits. These two parts can be performed within a single translinear loop. In Figure 16 [37], the relationship between I_{in} and I_{out} for ideal transistors (infinite β), is represented by

$$I_{in}{}^2 = I_o I_{out} + C V_T I_{out} \qquad \text{Eq. 1}$$

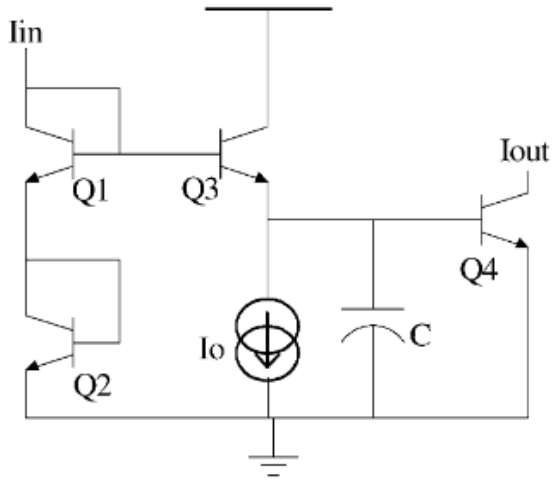

Figure 16: Basic translinear loop that used in RMS detector

I_o : the bias current, solving for I_{out} yields

$$I_{out} = \frac{{I_{in}}^2/I_o}{1+sCV_T/I_o} = \langle\frac{{I_{in}}^2}{I_o}\rangle \quad \text{Eq.2}$$

The operator<> stands for the time-average function.

Thus, I_{out} becomes the mean square of I_{in} and by performing the square root of I_{out},gives the baseband signal RMS value. To save the implementation area, the square-root operation is performed off-chip. The input current I_{in} to the translinear loop has to be positive. For the purpose of improving the high-frequency performance, all transistors should be biased at all times, which is done by adding a DC bias current I_o to I_{in} to eliminate the need for a rectifier ($|I_{in}| < I_o$). (V_{in}/I) and (I_{out}/V) converters are provided to interface with external voltage-mode signals

2.2.3.1. Input Interface Circuit

Figure 17, shows the RMS detector wide-bandwidth voltage-to-current converter circuit, [38] [39]. I_{in} is given by:

$$I_{in} = \frac{V_{in}}{R_{in}} - \frac{V_{BE1}-V_{BE2}}{R_{in}} \quad \text{Eq.3}$$

$V_{BE1} and\ V_{BE2}$ directly affect the current; therefore, the current generated from the voltage dropping across the resistor (in the second term of the right side in Eq.3) is a nonlinear current. The additional output current from Q3–Q6 in Caprio quad minimizes this nonlinearity effect for a certain level. A 50-ohm Shunt-resistance is connected to each of the differential V/I converter inputs (see Figure 20). On-chip capacitors are used to bypass $V_{bias1} and\ V_{bias2}$ inputs. In this case, the circuit can be driven as single-ended with one input left open-circuited. Figure 18 shows the simulated frequency response of the V/I converter.

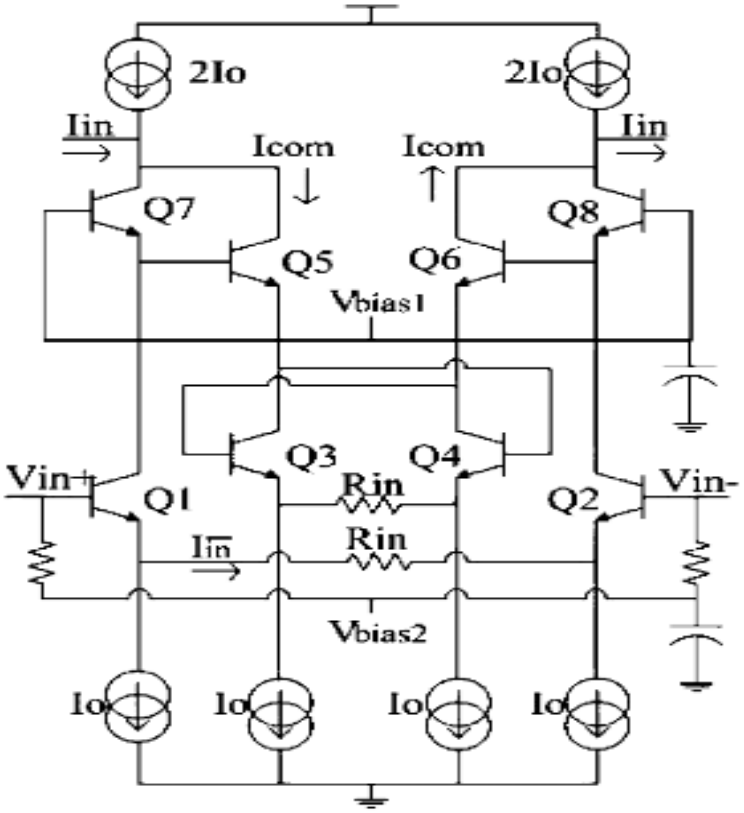

Figure 17: Caprio quad input interface circuit [37].

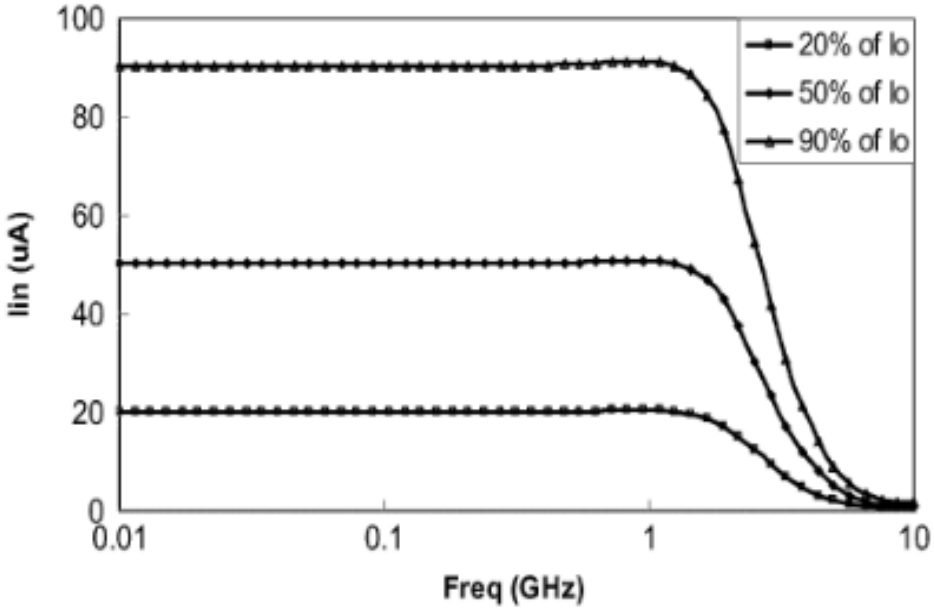

Figure 18: Frequency response at the input of the translinear loop [37].

2.2.3.2. Squarer-Divider and Low-Pass Filter

A rectifier is unnecessary for signal balancing processing purposes, where the output currents, $+I_{in}$ and $-I_{in}$ of the differential V/I convertor are added to the bias current and feed to two copies of the translinear loops, as shown in Figure 19. These output currents are given by

$$I_{out\ 1,2} = \langle \frac{(I_o \pm I_{in})^2}{I_o} \rangle \qquad \text{Eq. 4}$$

For two loops, the output current is given by

$$I_{out\ 1} + I_{out\ 2} = \langle \frac{(I_o + I_{in})^2}{I_o} \rangle + \langle \frac{(I_o - I_{in})^2}{I_o} \rangle = \frac{1}{I_o} \langle (I_o + I_{in})^2 + (I_o - I_{in})^2 \rangle$$

$$= \frac{2\langle {I_{in}}^2 \rangle}{I_o} + 2I_o \qquad \text{Eq. 5}$$

Obviously, omitting the second right part of Eq.5 (offset current) will result in the mean-square value of the input current being multiplied by $2/I_o$.

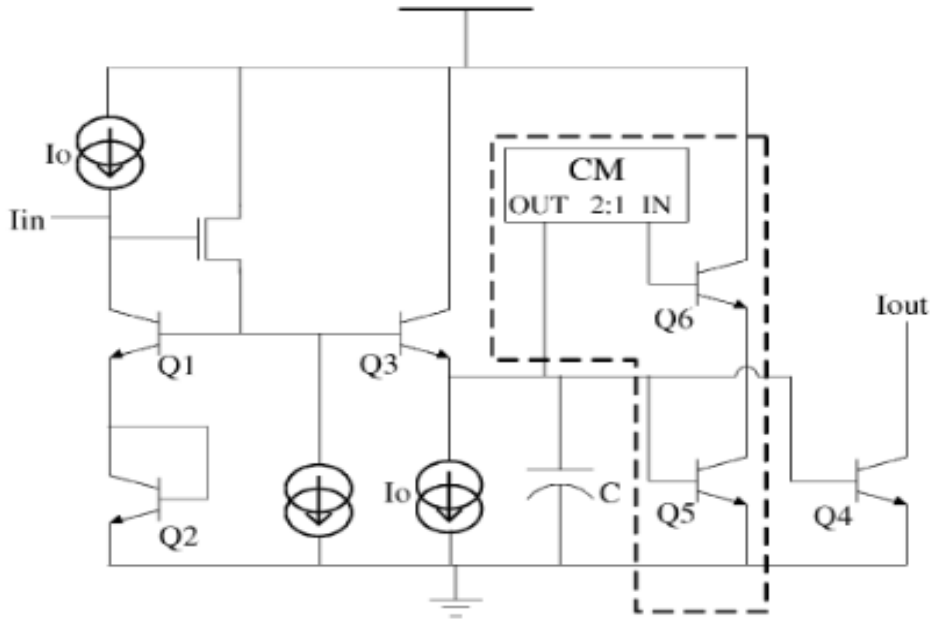

Figure 19: Translinear loop with base-current compensation shown in the dashed region (CM: current mirror) [37].

It is worth mentioning that temperature is not an effective parameter for these formulas. Instead of connecting a diode at the input of the loop, an NMOS source follower is used for the purpose of base-current error minimization (see Figure 21).

2.2.3.3. Output Interface Circuit

After the squarer-driver and low-pass filter, the current-signal should be converted back to a voltage-signal and the offset current removed, which is performed by I/V converter circuit. This circuit is realized by a transimpedance amp consisting of a CMOS op-amp with feedback resistor R_{out} (see Figure 20).

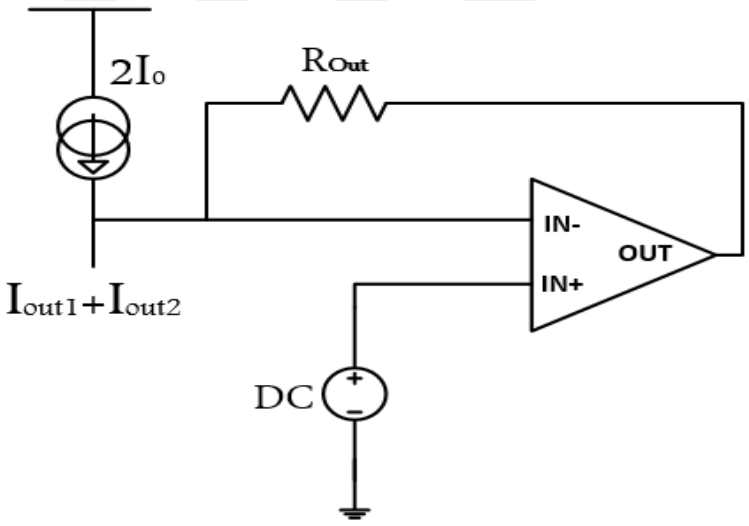

Figure 20: Output interface circuit.

The circuit design of this converter is basic and straightforward due to the signal's low frequency level at this point. The non-inverting terminal is connected to a DC value equalling the collector voltages of the output transistors in the translinear circuits in order to compensate for early effects. The current remaining after subtracting the offset current is converted into an output voltage. $V_{out}$is the product of the mean-square value of V_{in} and the gain k.

$$V_{out} = \frac{2R_{out}\langle {I_{in}}^2 \rangle}{I_o} = k\langle {V_{in}}^2 \rangle \qquad \text{Eq. 6}$$

Figure 21 shows the complete RMS circuit.

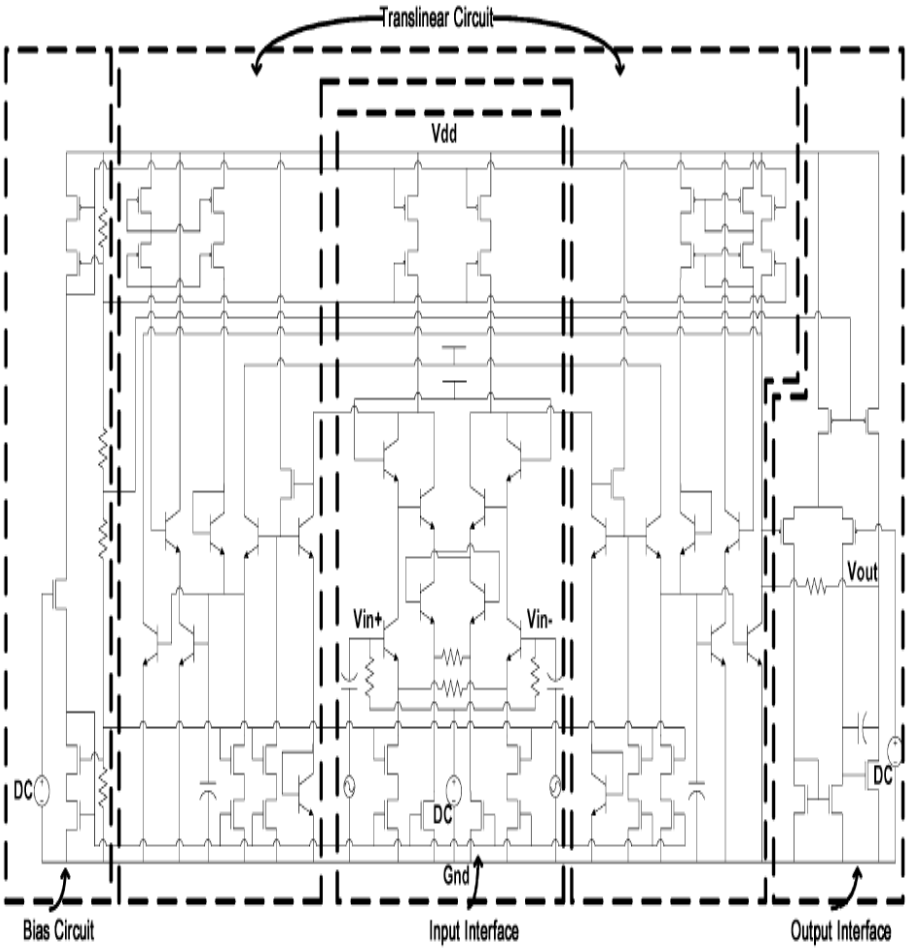

Figure 21: Complete circuit diagram of RMS detector by using the translinear principle [37],.

2.2.3.4. Error Analysis

The collector current of Q3 (see Figure 21) is not exactly equal to $I_o - I_c$ because of the finite current gain of the transistors Q4 and Q5. This causes an error in the translinear loop, which worsens when I_{cQ4} is increases. The dashed part of Figure 19 shows how base-current compensation can be used to significantly reduce the base-current error. The compensation circuit causes the base-current errors to be

decreased by $2/(1+\beta)$. For free-temperature variations, it can be experimentally proved that the total relative errors of the output are decreased to $\pm 1\%$. For temperature variations from –40 ℃ to 100℃, the output will change by ± 1.2 dB, [37].

2.2.4. Features and Drawbacks

The key advantage of using RMS detectors over other types of power detectors is the ability to deal with high peak-to-average ratio signals existing within different modulation schemes in modern communication systems, such as 4G, 5G and LTE. For instance, long calculation procedures and large calibration tables in the baseband are no longer necessary when dealing with modulated CDMA signals and unmodulated carriers because the RMS detector will produce the same value (0 dBm) for both. However, dynamic range, sensitivity, bandwidth, power dissipation, and chip-area are trade-offs between all these parameters, and it is very difficult (if not impossible) to achieve optimal RMS detector performance with respect to each of the previous parameters (see Table 1).

Parameters	[41]	[42]	[43]	[40]
Voltage	1.2 V	2.8 V	3V	3.3 V
Power	0.18 mW	70 mW	50 dB	63.36 mW
Dynamic Range	20 dB	40dB@ 8GHz 60dB@ 3.6Ghz	50dB	58dB
Min.Input Power	-35dBm @ 1Ghz	-60dBm@ 3.6 GHz	-45 dBm	-50dBm
Frequency	125MHz-5.5GHz	DC – 8GHz	450MHz	0.5-3GHz

Process	130 nm	180 nm	350 nm	130nm

Table 1: Comparison between different RMS power detectors [40].

2.3. LOG Detector

A logarithmic amplifier (a log-amp or log detector) is used as a power detector depending on its transfer function (see Figure 22). The concept is simple such that the output voltage or current is proportional to the logarithic value of the input voltage or current. This power representation is compatible with the modern communication standards that use the dBm power scale. Keeping this input/output relationship valid over a high dynamic range is a key advantage of using log detectors among the other power detectors. The word "amplifier" in the name "log amplifier" does not have the common meaning of amplification; it is in fact a linear-to-logarithmic converter.

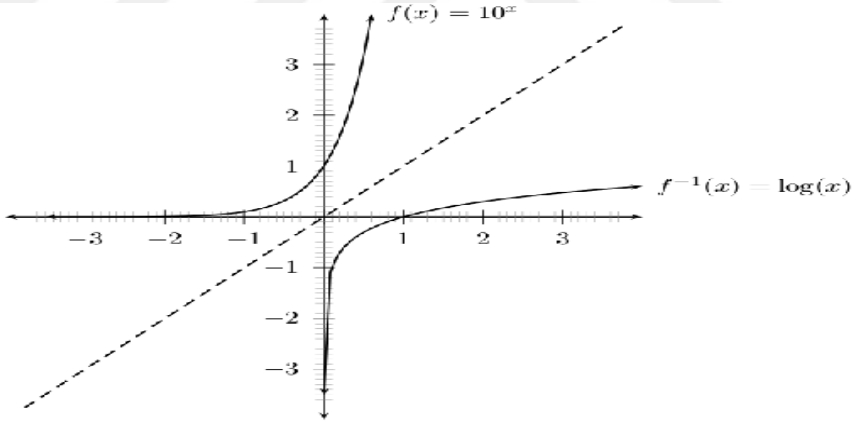

Figure 22: Logarithm function of the log detector, assuming (*x*,*y*) to be the input and output signals respectively.

2.3.1. Log-amp Applications

- Log-amps can be used for optical-circuits, power control, as well as for medical, chemical, and biological instrumentation. The DC log-amp ("DC" is

somewhat of a misnomer) is used where signals in such applications are common to be relatively slowly-changing signals, i.e., up to about 1 MHz.

- Baseband log-amp: It used in audio and video circuits, when some type of signal compression is needed, as well as within IF stages of a signal receiver chain and the signal-processing path of ultrasound circuits. It has a symmetrical output for positive and negative input signals, with an output, which is positive for positive inputs and negative for negative inputs.
- Demodulating log-amp: This both compresses and demodulates RF signals and generates at the output a logarithmic version of the rectified input signal's envelope. This detector is used in RF-transceiver applications, where the received RF-signal strength is used to control the transmitter output power. The output is based on the absolute value of the input, and it is positive regardless whether the input is positive or negative.

2.3.2. LOG Detector Principle of Work

The relationship between voltage and current within the p-n junction diode is the core function on which the log detector is based (see Figure 23(a)). This relationship is used in conjunction with an op-amp in a practical circuit (Figure 23(b)). Depending on this basic principle, many topologies and configurations have been introduced, each providing various performance attributes and priorities according to accuracy and bandwidth requirements. The internal details may not be of direct interest to the log-amp user, but they do affect the fit between the log amp and the required application. Log amps, which are called "linear in dB," provide a highly accurate transfer function – a characteristic which is needed in some and not all applications.

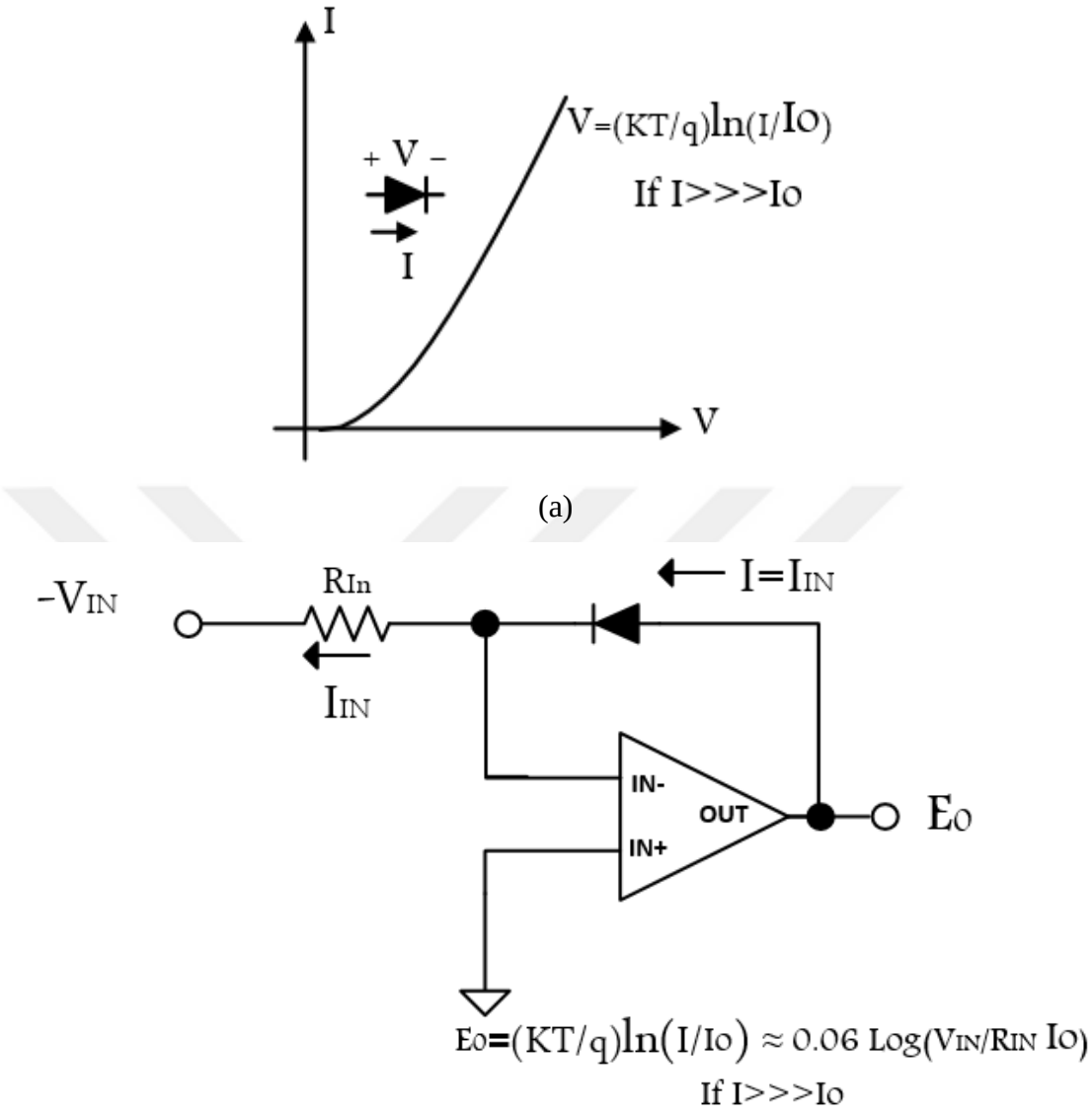

Figure 23: (a) Current vs. voltage relationship of a diode, (b) the use of this relationship within the op-amp feedback.

2.3.3. Log Detector Specifications

The log-amp detector can be implemented as an integrated circuit (IC) or as a module comprised of individual and discrete components. The IC versions are cheaper, smaller, have less power dissipation among other types, and can provide good performance. They are usually the first choice to consider. The singular

process technology of an IC, and thus a single IC, cannot adequately meet all the required parameters of the application, such as noise, bandwidth, or temperature range. Therefore, a hybrid construction is used instead of the single IC version. Many specifications of log-amps are similar to those for non-log amps, while others may be unique according to the nature of the device. Vendors also have different terms and definitions for the device parameters, which makes the datasheet for each vendor an essential reference in order to use these devices properly.

- Dynamic range: The range in most cases is from 60 dB to 120 dB; some reach 160 dB. Although this is a key advantage, wide range may not be needed in all situations, and achieving it may come at a trade-off with the degradation of other key features. This wide dynamic range and the constant false alarm rate property make the log detector a widely used application in radar systems [26], [27].
- Bandwidth: This is limited to the several GHz range; however, for today's RF applications, some advanced devices can reach tens of GHz.
- Accuracy: This is related to a perfect linear/logarithmic transfer function. Typically, it is ±0.2 dB, which makes them compatible with the needs of both RSSI and TSSI (transmit-signal-strength indicator) functions; furthermore, it may vary depending on where in the input range it is measured.
- Sensitivity: The 1 nA or 1 μV ranges are the lowest signal value which the log amp can usually process; however, it can be lower, and it is often specified in dBm, usually at 50 Ω.
- Offset: since log 0 is undefined, do not expect zero log-amp detector output for a minimum input.
- Adjustable or Fixed reference: Some allow the user to supply a reference which determines the scale factor. Scale factor can be called out with respect to dB or decades, such as 20 mV/dB or 400 mV/decade. Other log-amps will have a fixed scale factor, such as 0.25 V/decade (or 10 mA/decade).
- Bipolar vs. non-bipolar inputs and outputs: Many real-world signals are bipolar with negative values, and while the log of a negative number is undefined,

to overcome this constraint, baseband and demodulating log amps use offsets, squaring, or other techniques to allow inputs below 0 V.

2.3.4. LOG-amp Detectors Limitations and Issues

- Noise: This is one of the main challenging issues for log amps. Log amps work over many decades, and they are expected to handle signals in the μ, n, or even p range (V or A). However, if the signal levels are that low, the internal noise of the log amp may overwhelm the signal. Nevertheless, for many RF applications, fortunately, low noise is not as critical as dynamic range and bandwidth, so long as the noise spectral density is sufficiently low (usually on the order of nV/√Hz).
- Temperature: This is another main challenging issue for designers and users, where the core of a log amp is based on semiconductor junction behaviour; hence, it unavoidably changes with temperature. To cancel this effect, log-amp designers use a variety of design techniques to compensate, trim, or minimize tempco. Using a current reference circuit is one of the solutions to this issue [28]. However, it is still a factor, which is part of the trade-off in the overall performance. Like many other analog devices, log amps are available with detailed specifications used for standard commercial, extended industrial and even military temperature ranges.
- Power dissipation: they are power hungry devices, where log-amps in order to extend dynamic range and bandwidth, use the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell, [4] (see Figure 24) [29]. These detector cells provide accurate log conformance for signals of 1 MHz to 6 GHz and an operating region up to 8 GHz. Simultaneously, it will add more power dissipation for each extra cell.

2.3.5. LOG-amp Detector Circuit Diagram

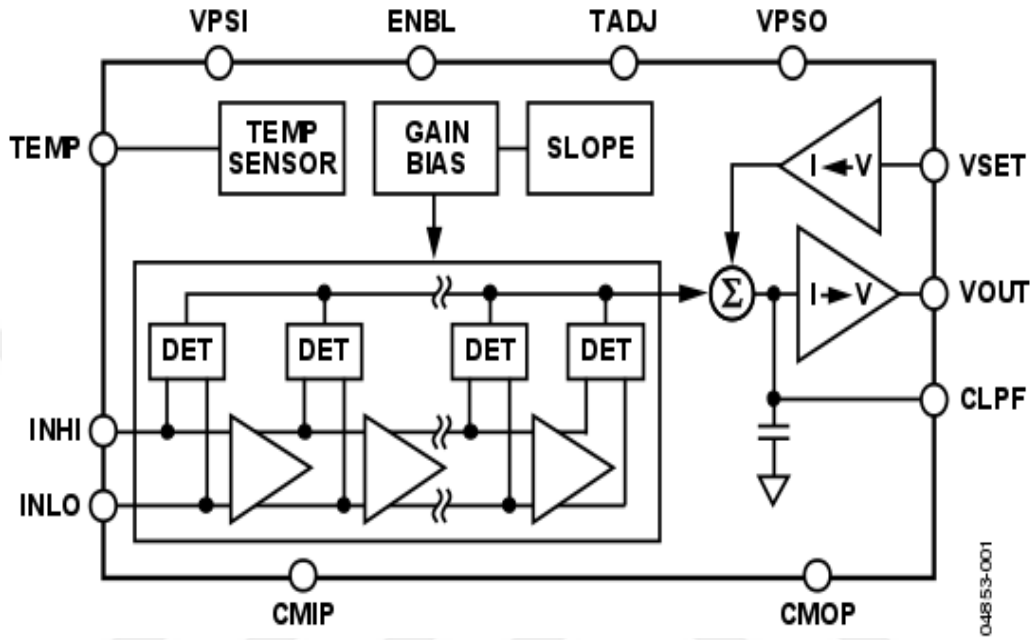

Figure 24: Functional block diagram of AD8318 logarithmic Detector/Controller

Figure 24 shows the AD8318 logarithmic Detector/Controller from Analog Devices Inc. It is a demodulating logarithmic amplifier. The input range is typically 60 dB (with a 50-ohm input impedance) with an error of less than ±1 dB (see Figure 25), at 5.8 GHz, V_{out} (nearly straight descending line) and log conformance ("wiggly" line) vs. input amplitude at 8 GHz. Figure 25 also shows the performance at +25°C (black), −40°C (blue), and +85°C (red), [30] . While stability over temperature is ±0.5 dB, the 4 mm × 4 mm, 16-lead device is specified over a –40^{0}C to +85^{0}C range and operates from a single 5–volt supply.$V_{POS} = 5$ V; $T_A = +25^\circ$ C −40°C, +85°C; C_{LPF}= 220 pF; $R_{\text{TA DJ}}$ = 500 Ω; unless otherwise, Colors: +25°C Black; −40°C Blue; +85°C Red.

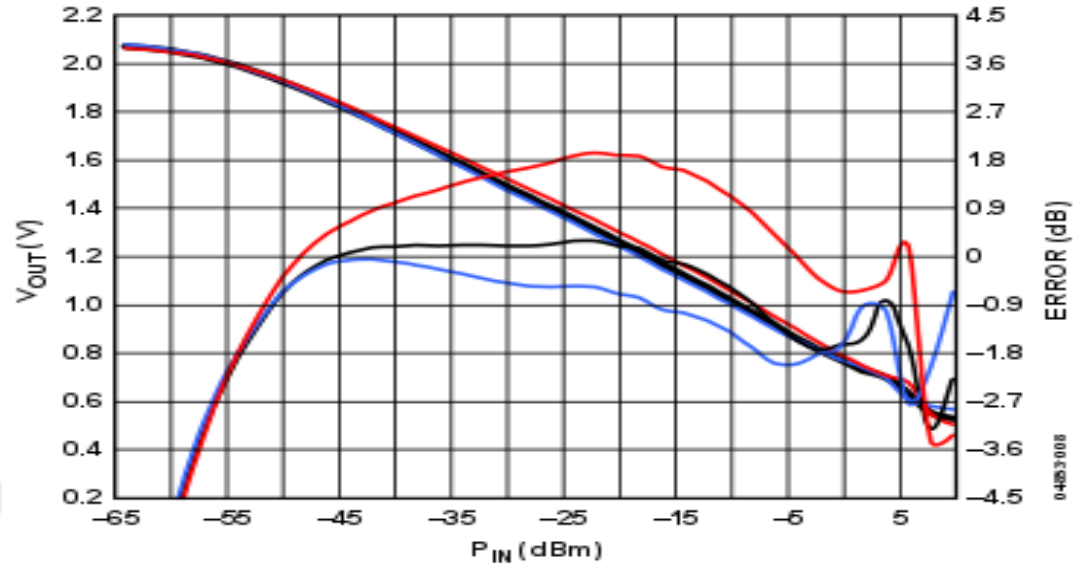

Figure 25: Typical Logarithmic Response and Error vs. Input Amplitude at different temperatures

2.4. Automatic Gain Control (AGC)

The AGC system is an essential component of any wireless communication system that requires specific maximum and minimum input signal levels. The different requirements of communication systems determine the complexity of the AGC. AGCs are feedback amplifiers with closed-loop low-pass gain characteristics; they are responsible for providing a relatively constant output amplitude so that a circuit following the AGC circuit can function with modest linearity performance [1].

A basic schematic for AGC is shown in Figure 26. The variable gain amplifier (VGA), whose gain is adjusted by the external signal V_c, will amplify the input signal; then the output from the VGA can be amplified again in a second stage to fulfil the required level of V_o. The detector senses the output signal's parameters, such as amplitude, carrier frequency, index of modulation or frequency, and any undesired component is filtered out, after which the remaining signal is compared with a reference signal. The result of the comparison is used to generate the control voltage (V_c) which in turn adjusts the gain of the VGA.

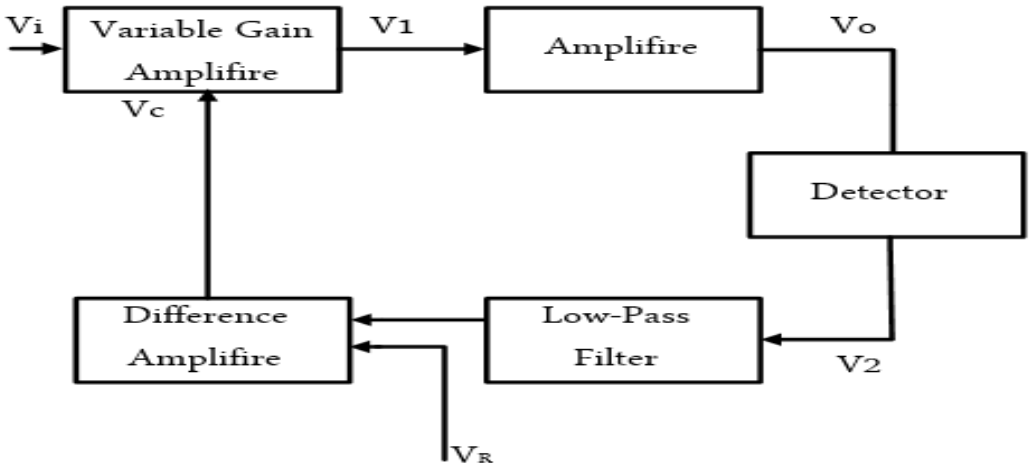

Figure 26: AGC block diagram.

The system can be described in terms of its transfer function due to the fact that an AGC is basically a negative feedback system. The idealized transfer function for an AGC system is illustrated in Figure 27. For low input signals, the output is in a linear relationship with the input, and the AGC is disabled. The function of the AGC is to keep the output signal level between the maximum and minimum values (V_1, V_2); thus, when the output reaches a threshold value (V_1), the AGC becomes operative and maintains a constant output level until it reaches a second threshold value (V_2). At this point, the AGC is disabled again; this is usually done in order to prevent stability problems at high levels of gain.

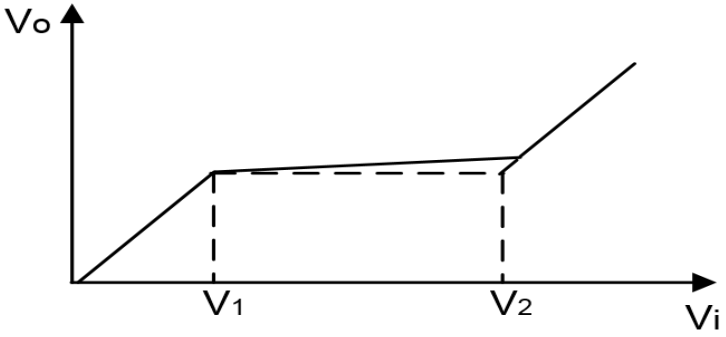

Figure 27: AGC (ideal) transfer function.

The parameters of the AGC loop (many of them) depend on the type of modulation used within the system. In the case of Amplitude Modulation (AM) for instance, the AGC should not respond to any change in amplitude; otherwise,

distortion would occur. Moreover, the information is already stored in the amplitudes of the signal. Thus, the bandwidth of the AGC must be limited to a value lower than the lowest modulating frequency. In contrast, for systems where frequency or pulse modulation is used, the system requirements are not as stringent.

2.4.1. Complete System Circuit Scheme

Figure 28 shows a practical AGC system. This circuit is included in the demo board of the OPA660 of Burr Brown (now part of Texas Instruments). OPA660 stands for Operational Transconductance Amplifier. It has a high bandwidth, high slew rate and transconductance, which can be varied by means of a resistor connected to pin 1. In this circuit, a resistive divider (at the input of the OPA660) will attenuate the input signal and convert it into a current, I_{OUT}. The second amplifier (the OPA621), will then convert the output current back into a voltage. The peak value of the output voltage is checked against the reference voltage V_{REF} with the discrete differential amplifier. The error voltage is multiplied by the gain of the discrete differential amplifier, applied to the gate of the JFET 2N5460 and filtered by the RC network ($R_{19}$and C_1). The output transconductance of the JFET adjusts the quiescent current at pin 1, thereby changing the transconductance of the OPA660 and modifying the total gain of the circuit. The process continues until the system reaches the steady state [46].

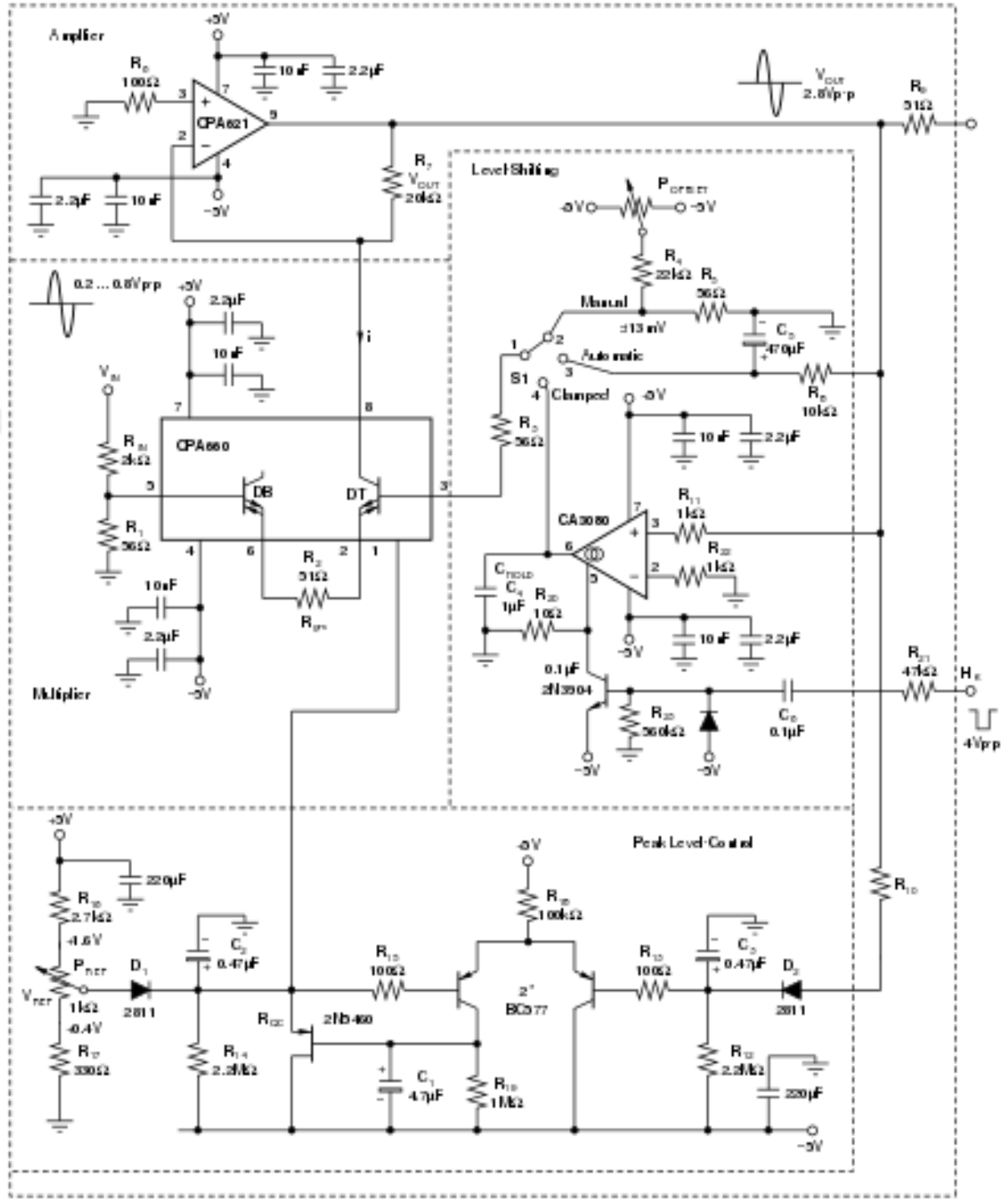

Figure 28: The complete circuit of an AGC system [44], [45].

2.5. Summary

The analog power detection techniques have been illustrated in this chapter. The simple and basic circuit for the Schottky diode and the CMOS transistor for envelop detection were presented first. Then, the RMS power detectors were presented. Multiple detection methods were discussed to achieve the function of the root-mean-square conversion for an RF input signal. The thermal detection, diode detection, and translinear detection are all different methods that perform the same function of acting as RMS power detectors. Finally, the log detector was introduced with the principle of work and circuit configuration. For all of the previous techniques, there were advantages that make some of them more suitable for a certain application than the others. On the other hand, there were also significant drawbacks, such as sensitivity, PVT spread issues, dynamic range, bandwidth limitations and power dissipation. However, it is very difficult (if not impossible) to improve the performance of all of the previous parameters simultaneously. Instead, it will be a trade-off between all of them due to the nature of the analog topologies (see Figure 11 and Table 1). Moreover, there was a general review about automatic gain control (AGC) circuit configuration and function, where a power detector element is the essential part of the AGC circuit.

CHAPTER 3:

3. SAMPLING THEORY

Sampling theory can be considered to be the transition point between analog (continuous-time-signal) and digital (discrete-time-signal) systems. It offers the ability to process and manipulate the signals to filter out combined noise, distortion, and other signal interference. After processing, it can be easy to reconstruct the same signal from its stored samples without losing any of its properties. This theorem is valid only for the type of mathematical functions where its Fourier transform outside of a finite region of frequencies is zero. The sampling rate introduced by the theory implies the critical condition to reconstruct the sampled signal correctly without losing any information from the original analog version. Nyquist–Shannon–Kotelnikov, Whittaker–Shannon–Kotelnikov, Whittaker–Nyquist–Kotelnikov–Shannon, and the Cardinal Theorem of Interpolation are names that refer to the theory and the scientists who discovered them. Some of these theorems were independently discovered by all of them and some other scientists.

3.1. Sampling and Reconstructing of RF Analog Signals

In order to process and manipulate an analog (continuous-time-signal), it has to be with finite parts that can later be converted to numbers and thus easily processed. This can be done using Sampling Theory.

Assume x_a that repeats itself (periodic) every T second to be a continuous-time-signal and x_n to be the discrete-time-signal version to be extracted from x_a; then:

$$x_n = x_a(nT)\ , \quad -\infty < n < \infty \qquad \text{Eq.3.1.1}$$

This equation shows the sampling process from the time domain perspective. x_n should be extracted from x_a with a sampling frequency $F_s = 1/T$ which is sufficiently large to avoid missing any information from the frequency content (spectrum) of the signal; otherwise, there will be aliasing. Thus, if the frequency content of the signal is recovered from x_n correctly, there will be no loss of the information of x_a. In order to analyse the relationship between the spectrum of x_a

and x_n, assume that x_a is a voltage signal with finite energy; then its spectrum is given by the Fourier transform:

$$X_a(F) = \int_{-\infty}^{\infty} x_a(t) e^{-i2\pi \mathrm{F}t} dt \qquad \text{Eq. 3.1.2}$$

Performing the inverse of Fourier transform yields the recovery of the $x_a$spectrum:

$$x_a(t) = \int_{-\infty}^{\infty} X_a(F) e^{i2\pi \mathrm{F}t} dF \qquad \text{Eq. 3.1.3}$$

If the $x_a(t)$ signal is not a band-limited signal, then, in order to recover it, all the frequency components where $-\infty < F < \infty$ have to be utilized.

After $x(n)$ is extracted from $x_a(t)$ using sampling, then, its spectrum will be:

$$X(\omega) = \sum_{n=-\infty}^{\infty} x(n) e^{-i\omega n} \qquad \text{Eq. 3.1.4}$$

or by substitution:

$$X(f) = \sum_{n=-\infty}^{\infty} x(n) e^{-i2\pi/n} \qquad \text{Eq. 3.1.5}$$

The inverse of the transform for $X(\omega)$ or $X(f)$ (the spectrum) generates the sequence (n):

$$x(n) = \frac{1}{2\pi} \int_{-\pi}^{\pi} X(\omega) e^{i\omega n} d\omega$$

$$= \int_{-1/2}^{1/2} X(f) e^{i2\pi f n} df \qquad \text{Eq. 3.1.6}$$

The t-variable refers to the spectrum (in the time domain) of x_a and the n-variable refers to the spectrum (in the frequency domain) for x_n. These variables are related as follows:

$$t = nT = \frac{n}{F_s} \qquad \text{Eq.3.1.7}$$

The corresponding relationship in the frequency domain can be derived by substituting Eq.3.1.7 into Eq3.1.3:

$$x(n) \equiv x_a(nT) = \int_{-\infty}^{\infty} X_a(F) e^{j2\pi nF/F_s} dF \qquad \text{Eq. 3.1.8}$$

By looking at Eq.3.1.6 and Eq.3.1.8, it is obvious that:

$$\int_{-1/2}^{1/2} X(f) e^{j2\pi fn} df = \int_{-\infty}^{\infty} X_a(F) e^{j2\pi nF/F_s} dF \qquad \text{Eq. 3.1.9}$$

For a periodic signal, the frequency variable of a continuous-time version f and the discrete-time version F are related to each other, where:

$$f = \frac{F}{F_s} \qquad \text{Eq. 3.1.10}$$

Substituting Eq.3.1.10 into Eq.3.1.9 yields

$$\frac{1}{F_s} \int_{-F_s/2}^{F_s/2} X(F) e^{j2\pi nF/F_s} df = \int_{-\infty}^{\infty} X_a(F) e^{j2\pi nF/F_s} dF \qquad \text{Eq. 3.1.11}$$

The infinite range at the right side of Eq.3.1.11 can be replaced as follows:

$$\int_{-\infty}^{\infty} X_a(F) e^{j2\pi nF/F_s} df = \sum_{k=-\infty}^{\infty} \int_{(k-1/2)F_s}^{(k+1/2)F_s} X_a(F) e^{j2\pi nF/F_s} dF \qquad \text{Eq. 3.1.12}$$

$X_a(F)$ from $(k-1/2)F_s$ to $(k+1/2)F_s$ and $X_a(F-kF_s)$ from $-F_s/2$ to $F_s/2$ are the same, which leads to:

$$\sum_{k=-\infty}^{\infty} \int_{(k-1/2)F_s}^{(k+1/2)F_s} X_a(F) e^{j2\pi nF/F_s} dF = \sum_{k=-\infty}^{\infty} \int_{-F_s/2}^{F_s/2} X_a(F-kF_s) e^{j2\pi nF/F_s} dF$$

$$= \int_{-F_s/2}^{F_s/2} \left[\sum_{k=-\infty}^{\infty} X_a(F-kF_s) \right] e^{j2\pi nF/F_s} dF \qquad \text{Eq. 3.1.13}$$

To obtain Eq.3.1.13 in this form, the periodicity property of the complex exponential relationship is used, where:

$$e^{i2\pi n(F+kF_s)/F_s} = e^{i2\pi nF/F_s}$$

By gathering Eq.3.1.11, Eq.3.1.12, Eq.3.1.13, one can present the relationship of the frequency content (spectrum) to $X(F)$ of $x(n)$, and the spectrum $X_a(F)$ of $x(t)$, which is:

$$X(F) = F_s \sum_{k=-\infty}^{\infty} X_a(F - kF_s) \qquad \text{Eq. 3.1.14}$$

and for $X(f)$, it will be:

$$X(f) = F_s \sum_{k=-\infty}^{\infty} X_a[(f - k)F_s] \qquad \text{Eq. 3.1.15}$$

Assume the band-limited frequency content of $x_a(t)$ is as shown in Figure 29 (a). There are spectrum $X(F)$ as long as $|F| \leq B$; otherwise, it is zero. If this signal is sampled with $F_s > 2B$, $x(n)$ (the discrete-time form) will be as shown in Figure 29 (b). Thus, where $F_s \geq 2B$, then:

$$X(F) = F_s\, X_a(F)\,, \quad |F| \leq F_s\,/2 \qquad \text{Eq.3.1.16}$$

In this case, there is no aliasing and the output spectrum from the sampling process is a set of replicas from the original sampled spectrum separated by the F_s factor along the frequency axis as long as $|F| \leq F_s/2$. However, if $F_s < 2B$, in this case, all the replicas of the spectrum along the frequency axis will overlap resulting in aliasing (see Figure 29 (c)); thus, it is impossible to recover the original signal $x_a(t)$ spectrum from the samples.

In order to reconstruct $x_a(t)$ from $x(n)$ (shown in Figure 29 (b)), which is assumed to be already sampled without aliasing, then:

$$X_a(F) = \begin{cases} \frac{1}{F_s} X(F), & |F| \leq F_s/2 \\ 0, & |F| > F_s/2 \end{cases} \qquad \text{Eq.3.1.17}$$

Using Eq.3.1.5 (Fourier transform):

$$X(F) = \sum_{n=-\infty}^{\infty} x(n) e^{-i2\pi Fn/F_s} \qquad \text{Eq. 3.1.18}$$

By taking the inverse of $X_a(F)$:

$$x_a(t) = \int_{-F_S/2}^{F_S/2} X_a(F) e^{i2\pi Ft} dF$$

E.q.3.1.19

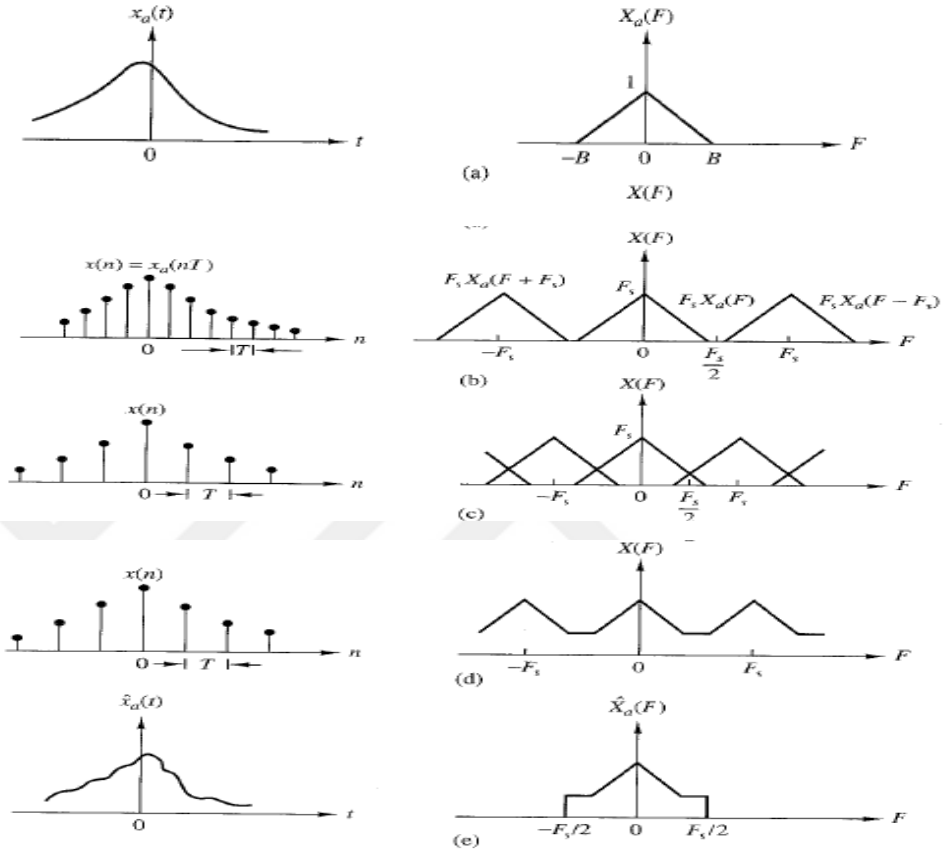

Figure 29: The sampling process for a bandlimited signal and aliasing of the spectrum replicas [9].

Supposing $F_s \geq 2B$, then substitute Eq.3.1.17 into Eq.3.1.19, which yields

$$x_a(t) = \frac{1}{F_s} \int_{-F_S/2}^{F_S/2} \left[\sum_{n=-\infty}^{\infty} x(n) e^{-i2\pi Fn/F_s} \right] e^{-i2\pi Ft} dF$$

$$= \frac{1}{F_s} \sum_{n=-\infty}^{\infty} x(n) \int_{-\frac{F_s}{2}}^{\frac{F_s}{2}} e^{i2\pi F\left(t - \frac{n}{F_s}\right)} dF \qquad \text{Eq. 3.1.20}$$

$$= \sum_{n=-\infty}^{\infty} x_a(nT) \frac{\sin\left(\frac{\pi}{T}\right)(t - nT)}{\left(\frac{\pi}{T}\right)(t - nT)}$$

Eq.3.1.20 is defined as the ideal interpolation formula which reconstructs x_a from $x(n)$, where $x(n) = x_a(nT)$ and $T = 1/F_s$ sampling interval .

The reconstruction equation that can be concluded from Eq.3.1.20 is:

$$g(t) = \frac{\sin\left(\frac{\pi}{T}\right)t}{\left(\frac{\pi}{T}\right)t} \qquad \text{Eq.3.1.21}$$

$g(t)$ In Eq.3.1.21 called interpolation function.

nT is the shifting term, and *n* is an integer number, while $x_a(nT)$ is the amplitude weight that is being multiplied by the related samples of the signal. For $t = kT$, then $g(t - nT) = 0$ if k=*n*. This means $x_a(t)$ that is estimated at $t = kT$ is obviously the sample $x_a(kT)$, while at all the times the combined shifted replicas of $g(t)$ result in the exact $x_a(t)$ (see Figure 30) [9].

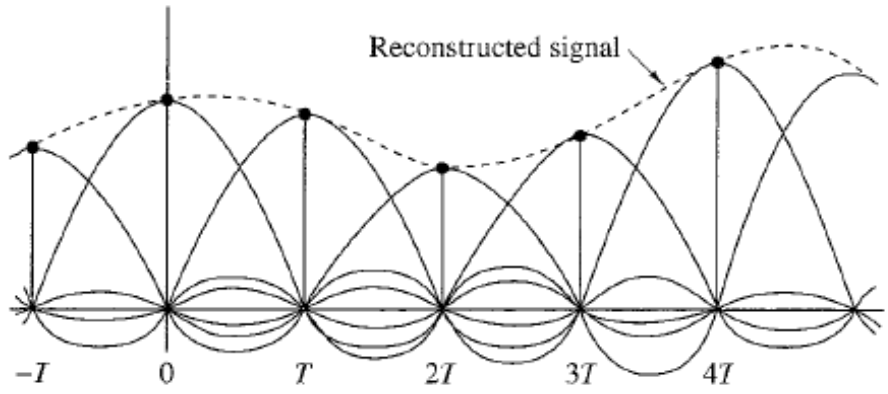

Figure 30: Reconstruction process to recover the original analog signal from its samples [9].

3.2. Aliasing

When the original spectrum of a signal cannot be recovered from the sampled version; rather than that, another different spectrum is recovered. This is called aliasing, and the resulting spectrum is called the aliased version of the original signal spectrum.

Consider the spectrum $X_a(F)$ of a continuous-time signal $x_a(t)$ with a bandwidth B that is shown in Figure 31(a). Sampling $x_a(t)$ with a sampling frequency F_s will generate multiple shifted versions of the signal spectrum $X_a(F)$ with F_s shifting period. When $F_s < 2B$, these shifted versions will be folded into each other. In Figure 31(b), the overlapping within the frequency range of $-F_s/2 \leq F \leq -F_s/2$ is illustrated. In order to reconstruct the discrete-time signal spectrum from the fundamental frequency range, all the shifted portions within $F \leq F_s/2$ should be added together to produce the spectrum that is illustrated in Figure 31(c).

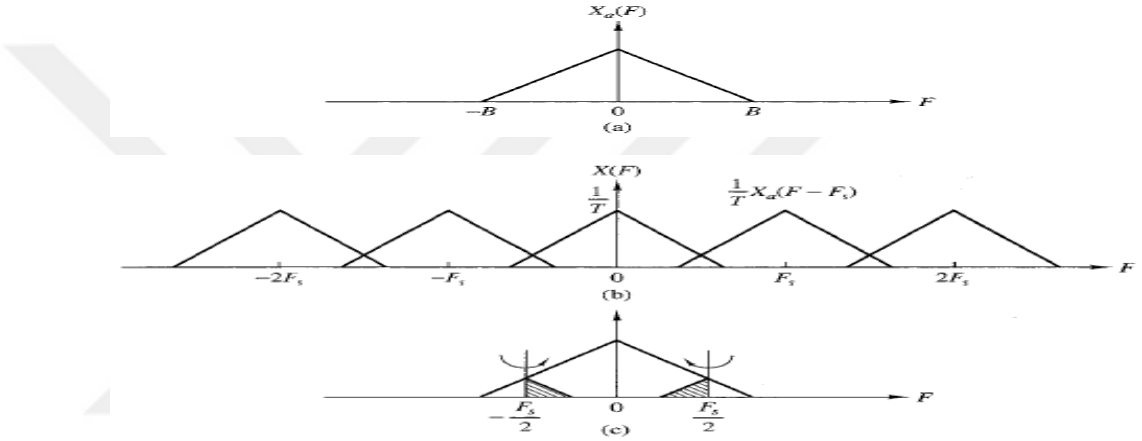

Figure 31: Aliasing of Fs < 2B [9].

For the illustration of aliasing of the sinusoidal signal, consider $x_a(t)$ a continuous-time sinusoidal signal; then:

$$x_a(t) = \cos 2\pi F_0 t = \frac{1}{2} e^{i2\pi F_0 t} + \frac{1}{2} e^{-i2\pi F_0 t}$$

It has a frequency content (spectrum) that extends from $-F_0$ to $+F_0$ (see Figure 32 (a)). Figure 32(b) shows the signal spectrum replicas that are generated when the signal is sampled with a sampling frequency F_s and $F_s/2 < F_0 < F_s$. In order to reconstruct $x_a(t)$ from the sampled spectrum, the frequency components within $|F| \leq F_s/2$ should be extracted as shown in Figure 32(c), and the recovered $x_a(t)$ will be:

$$\hat{x_a}(t) = \cos 2\pi (F_s - F_0) t$$

For the case of $F_s < F_0 < 3F_s/2$, the sampled signal spectrum and the reconstructed signal are shown in Figures 35(d) and (e) respectively. For this case, the recovered continuous-time signal is

$$x_a(t) = \cos 2\pi(F_0 - F_s)t$$

As can be seen, both cases have aliasing and the spectrum of the reconstructed signal will be aliased from the original spectrum. Figure 33 summarizes all the previous formulas to sample and reconstruct a signal [9].

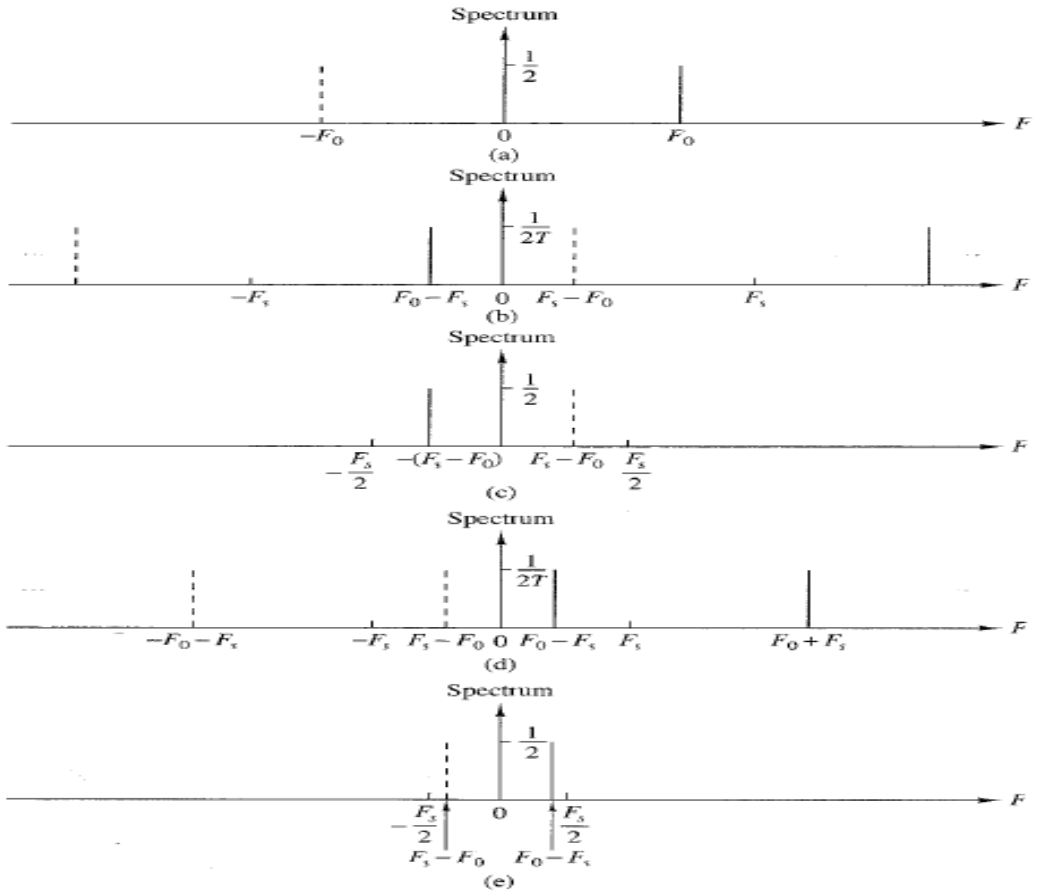

Figure 32: Aliasing in a sinusoidal signal [9].

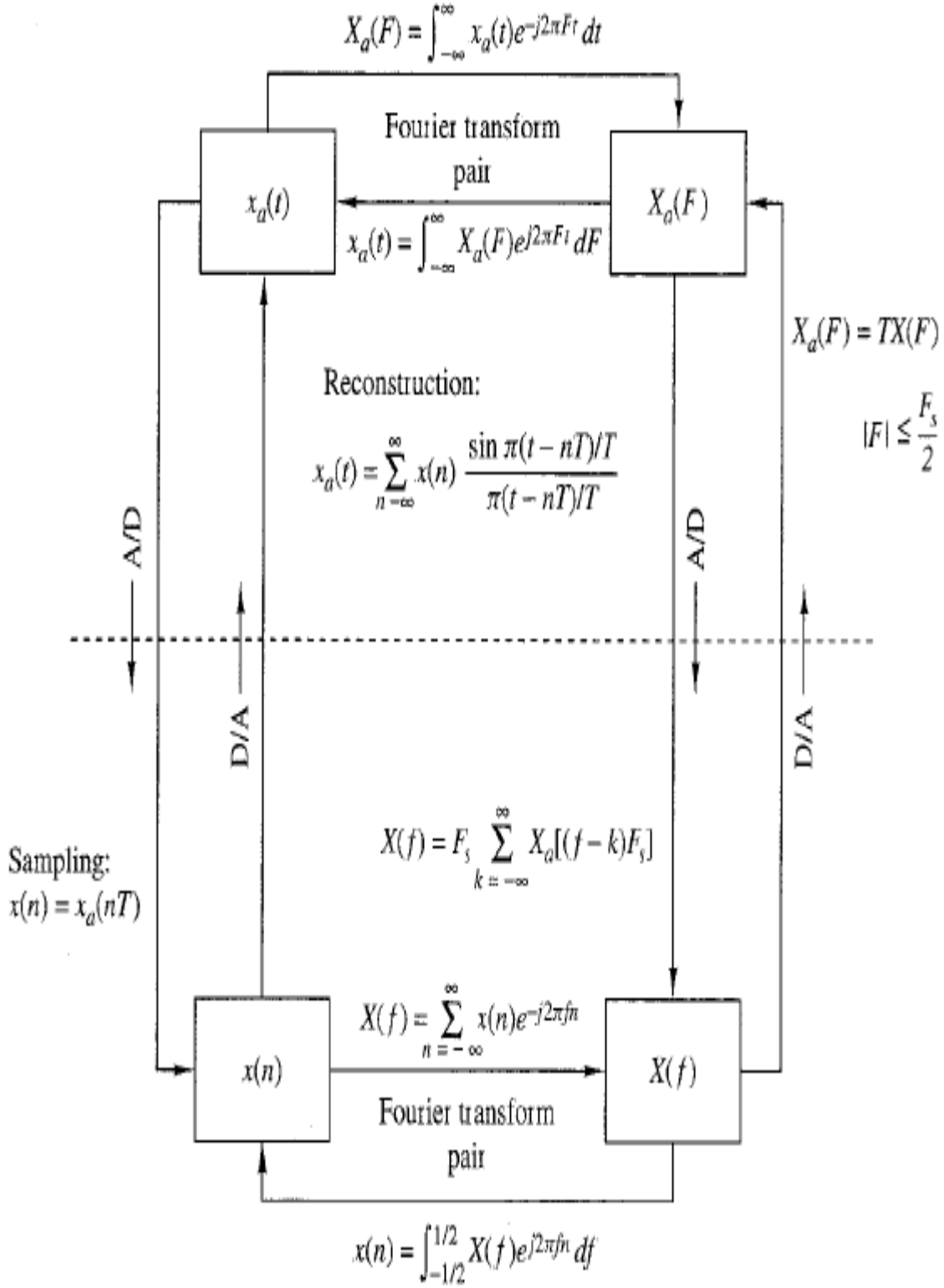

Figure 33: Sampling and reconstructing formulas for a bandlimited signals [9].

3.3. Band-pass Sampling (Subsampling)

In Figure 34(a) a band-pass analog signal (RF signal) with a bandwidth B centred at F_c, where $F_c = (F_L + F_H)/2$ and F_L, F_H are the lowest and highest frequency component of the signal spectrum respectively. A two versions of the signal spectrum exist at the regions described by $0 < F_L < |F| < F_H$. For this signal, instead of considering the sampling frequency to be $F_s \geq 2F_H$ as the basic sampling theorem suggests, a sampling frequency of $2B$ is enough to recover the original signal correctly after sampling.

3.3.1. First-order Sampling

Consider the band-pass signal shown in Figure 34(a), if it sampled by sampling frequency $F_s = 1/T$, $x(n) = x_a(nT)$ sequence will be produced, and the frequency content can be expressed as:

$$X(F) = \frac{1}{T}\sum_{k=-\infty}^{\infty} X_a(F - kF_s) \qquad \text{Eq.3.3.1}$$

F_s is the only parameter which controls the shifting position of the replicas $X(F - kF_s)$. However, it is difficult to avoid aliasing using just F_s, the reason is that the band-pass signal has double identical frequency versions of the spectrum on either side of the carrier frequency F_C.

3.3.2. Integer Spectrum Position

Integer spectrum position means that the highest side of the spectrum must be located at integer multiples of the bandwidth, $F_H = mB$. m is known as the band position, $m = F_H/B$. In Figure 34(a), the band position is even ($m = 4$), while at Figure 34(d) it is odd ($m = 3$). Figure 34(c) shows that to reconstruct the original band-pass signal, the recovering formula should be used as follows:

$$x_a(t) = \sum_{n=-\infty}^{\infty} x_a(nT)\, g_a(t - nT) \qquad \text{Eq. 3.3.2}$$

$$\text{where } g_a(t) = \frac{\sin \pi Bt}{\pi Bt} \cos 2\pi F_c t \qquad \text{Eq.3.3.3}$$

$g_a(t)$ is the inverse Fourier transform of the band-pass frequency gating function. It is illustrated in Figure 34(c) and it can be considered to be the modulated version of Eq.3.1.21. By looking to Eq.3.3.3, one can conclude that F_c is the parameter that can control the position of the two identical frequency spectra on either side of F_c; this position can be any of $F_c = \pm(kB + B/2), k = 0,1, \dots etc.$ Obviously, the baseband signal carried by the carrier signal will be at the location of $k = 0$; this is known as down conversion. At $m = 3$, the baseband spectrum has the same shape of the original band-pass spectrum, while at $m = 4$ the baseband spectrum had been inverted, and this is true as long as m is even.

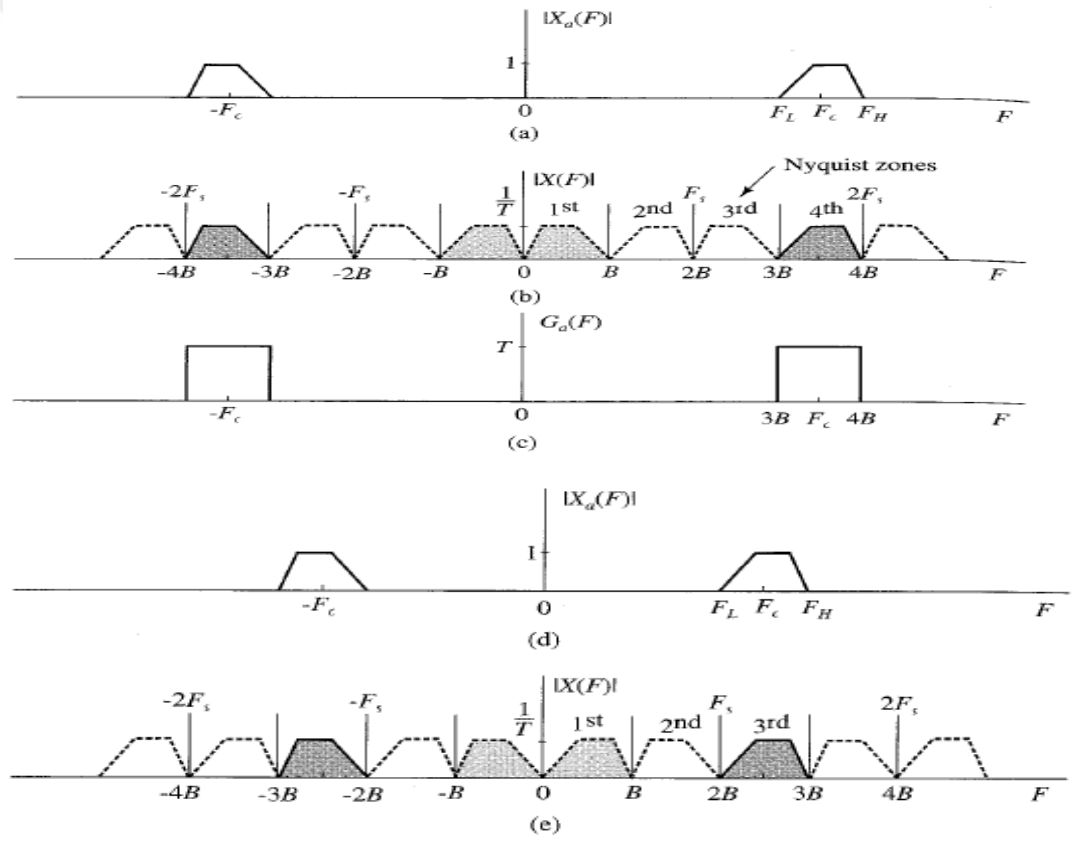

Figure 34: The band-pass position configuration: even and odd cases [9].

3.3.3. Random Band-pass Position

Figure 35 (a) shows a band-pass signal with a random position spectrum. In order to have free-aliasing sampling for a such case, F_S should be chosen in a way that $(k-1)$th and kth of the negative shifted replicas do not folded with the positive

ones. By looking to Figure 35(b), it can be seen that it is possible when k is integer and F_s to be such that:

$$2F_H \leq kF_s \quad \text{Eq.3.3.3.4}$$

$$(k-1)F_s \leq 2F_L \quad \text{Eq.3.3.3.5}$$

By looking to Eq.3.3.3.5 and Eq.3.3.3.4, obviously, the sampling frequency must be given by

$$\frac{2F_H}{k} \leq F_s \leq \frac{2F_L}{k-1} \quad \text{Eq. 3.3.3.6}$$

Eq.3.3.3.4 and Eq.3.3.3.5 can be rewritten such that:

$$\frac{1}{F_s} \leq \frac{k}{2\,F_H} \quad \text{Eq. 3.3.3.7}$$

$$(k-1) \leq 2F_H - 2B \quad \text{Eq.3.3.3.8}$$

Solving Eq.3.3.3.7 and Eq.3.3.3.8 yields

$$k_{max} \leq \frac{F_H}{B} \quad \text{Eq.3.3.3.9}$$

This is the maximum number of bands could be fitted within $0 \rightarrow F_H$, which is:

$$k_{max} \leq \left\lfloor \frac{F_H}{B} \right\rfloor \quad \text{Eq.3.3.3.10}$$

This corresponds to the minimum sampling frequency for free-aliasing, and the sampling frequency range with free-aliasing can be given by

$$\frac{2F_H}{k} \leq F_s \leq \frac{2F_L}{k-1} \quad \text{Eq.3.3.3.11}$$

In addition, the integer number k is given by

$$1 \leq k \leq \left\lfloor \frac{F_H}{B} \right\rfloor \quad \text{Eq.3.3.3.12}$$

When there are free-aliasing sampling case, Eq.3.3.2 and Eq.3.3.3 can be used to reconstruct the signal, also it is valid for integer and arbitrary band position [9].

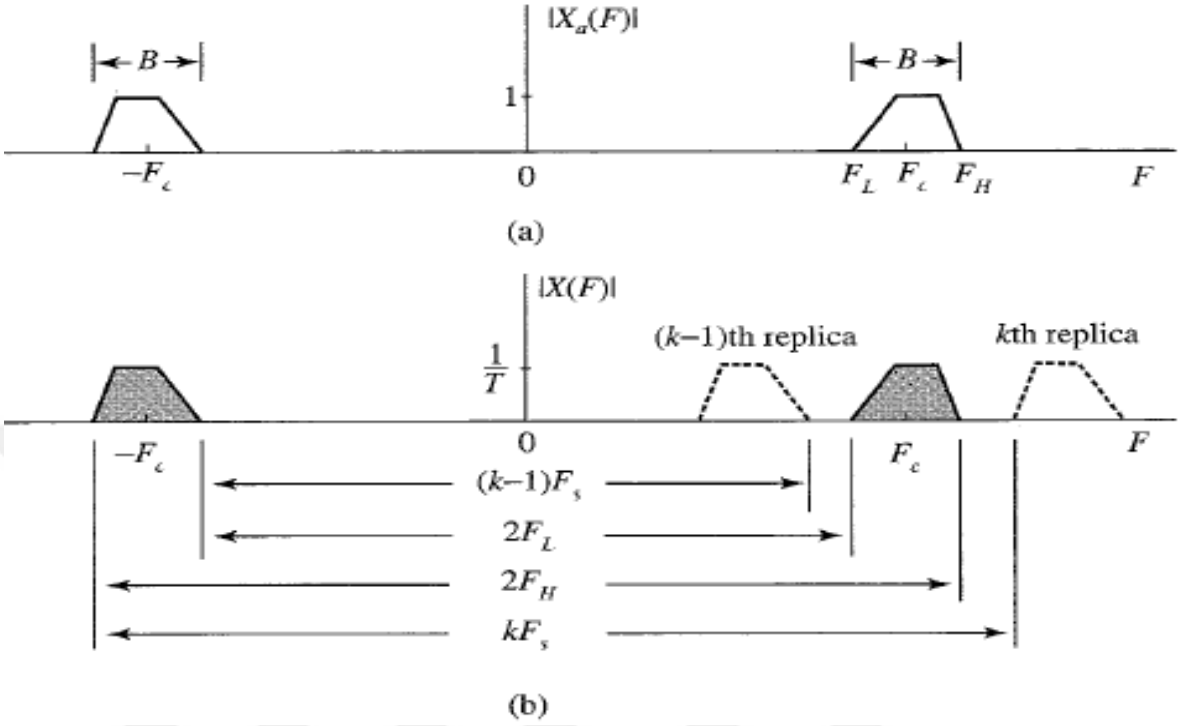

Figure 35: Arbitrary position band-pass signal sampling [9].

3.3.4. Determining the Exact Sampling Frequency

Figure 36 illustrates the strict conditions of Eq.3.3.3.11 and Eq.3.3.3.12. Eq.3.3.3.11 can be normalized with B to be given by:

$$\frac{2}{k}\frac{F_H}{B} \leq \frac{F_S}{B} \leq \frac{2}{k-1}\left(\frac{F_H}{B} - 1\right) \qquad \text{Eq.3.3.4.13}$$

According to this formula, it can achieve free-aliasing sampling with a sampling frequency far lower than Nyquist. The green-coloured areas are the aliasing sampling frequency regions, and the white ones are the free-aliasing regions. The Nyquist rate can be concluded from this formula when $k = 1$, so that $2F_H \leq F_s \leq \infty$, and the minimum sampling rate (theoretically) is $F_s = 2B$.

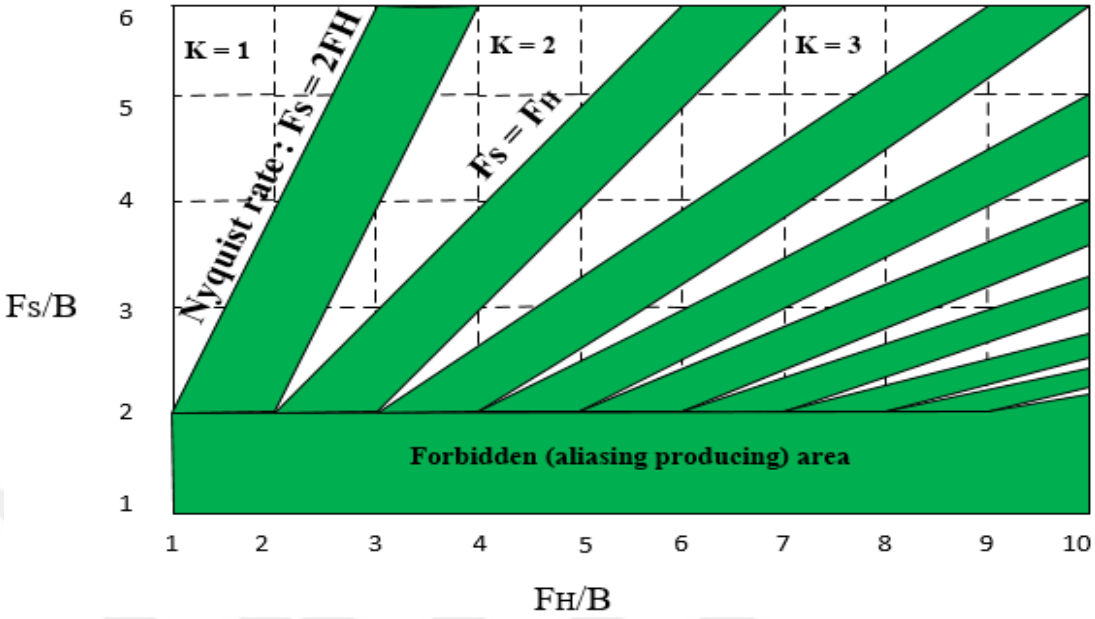

Figure 36: Allowed (white) and forbidden (green) regions of the sampling frequency.

3.4. Summary

This chapter was a quick review of the Sampling Theorem, where the basics of the sampling process were explained and formulas were derived for both of sampling the continuous time signal in addition to reconstructing it from the discrete time version. After that, the most important part, which is the subsampling or band-pass sampling concept, was introduced. The subsampling technique is the core principle on which this study is based. The Subsampling as can bee seen leads to a significant reduction in the power dissipation and the cost of the used ADC.

CHAPTER 4:

4. SUGGESTED MODULE FOR POWER ESTIMATION

This study suggests a digital module for the power estimation of an RF or IF signal instead of the used analog techniques. The module is mainly based on the idea that less analog processing would mean less spread over PVT. For this purpose, the signals are directly sampled by using a low power low ENOB (low SNDR) simple ADC whose clock frequency needs to be at least double the bandwidth of its input signal. Instead of using uniform sampling, the subsampling (band-pass sampling) technique explained in 3.3 was used. The samples are then squared and low-pass filtered (averaging) to estimate the power for a given time window to produce a digital code. The digital code that represents the power estimates can then be used to adjust the gain of the VGA digitally through an automatic gain control (AGC) loop, as shown in Figure 2. The generic analog scheme for power control is shown in Figure 1.

4.1. The Proposed Digital Power Estimation Algorithm

The first stage after receiving a signal is the low noise amplification stage, which exacerbates the signal-to-noise ratio to an acceptable level. Since there is no a priori knowledge of the signal power, the low noise amplifier (LNA) contains an AGC with a feedback loop to adjust the gain level according to the output take-over point (OTP). In the analog power detection technique, power is detected by an analog circuit that generates a DC voltage proportional to the signal power. This DC voltage is used by the *AGC* to adjust the gain of the LNA as demonstrated in Figure 1. In the digital power estimation approach, the power of the signal is estimated by directly sampling the analog signal by the analog-to-digital converter and the processed *ADC* output data is used to control a digitally programmable variable gain amplifier (VGA), as shown in Figure 2.

Figure 37 shows the digital power estimation process applied to the output of the VGA. The antialiasing filter band limits the signal and the noise present in the

vicinity of the signal bandwidth. The band limited signal is sampled with a sample and hold amplifier (SHA); then, the signal voltage is converted to a digital code at the output of the ADC. The sampling frequency, f_s, can be chosen to be far less than the Nyquist rate; with a low sampling rate, there will be replicas of the sampled signal at each integer multiple of f_s. A digital LPF (possibly an accumulator) will attenuate all the unwanted replicas except for the base band version. The ADC output code is processed within the code calculation block, which results in a new digital code to represent the input signal power. The final code represents the signal power estimate according to the look up table, which could be formed based on simulations and/or actual measured data. Then, the VGA adjusts the gain according to an algorithm based on this final code. For the case of using an analog controlled amplifier, a digital-to-analog converter (DAC) is needed to generate a DC voltage that feeds the LNA, which in turn adjusts the gain of the *LNA*.

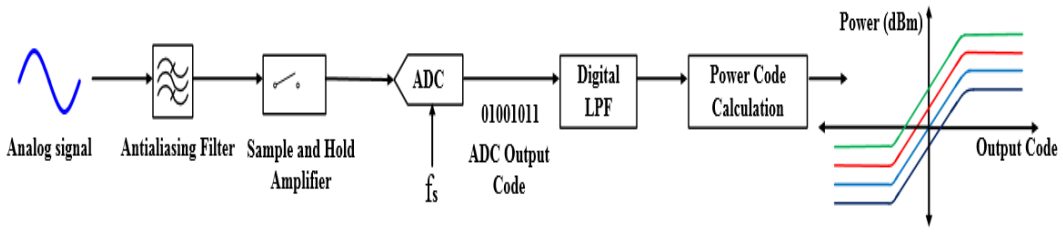

Figure 37: Digital power estimation using direct sampling.

The processing within the code calculation block is illustrated in Figure 38. *N* samples are squared, and averaged over *N* to estimate a power code according to:

$$P = \lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N} |x[n]|^2 \qquad \text{Eq. 4.1.1}$$

A time window of $N*T_s$ (T_s=1/f_s) is considered for each averaging process and the power estimate represents the signal power for that time window. The size of the time window determines the magnitude of the power estimate error, where averaging at the expense of long processing time will generate low measurement errors.

Increasing the samples within the same time window enhances the averaging process and leads to more accurate estimates, which means that the power measurement error has an inverse relationship with the sampling frequency. For a given bandwidth of the input signal and a fixed measurement interval, increasing the sampling frequency does not indefinitely improve the power estimation due to the statistical nature of the input signal. Moreover, going to a higher sampling rate means higher power dissipation. Instead of considering single sampling frequency f_s, there are mf_s (where m is an integer) sampling frequencies which may be considered according to the subsampling concept. In spite of this, the input signal bandwidth, its position on the frequency axis, and the highest frequency component should all be chosen carefully in order to avoid overlapping between adjacent replicas of the signal.

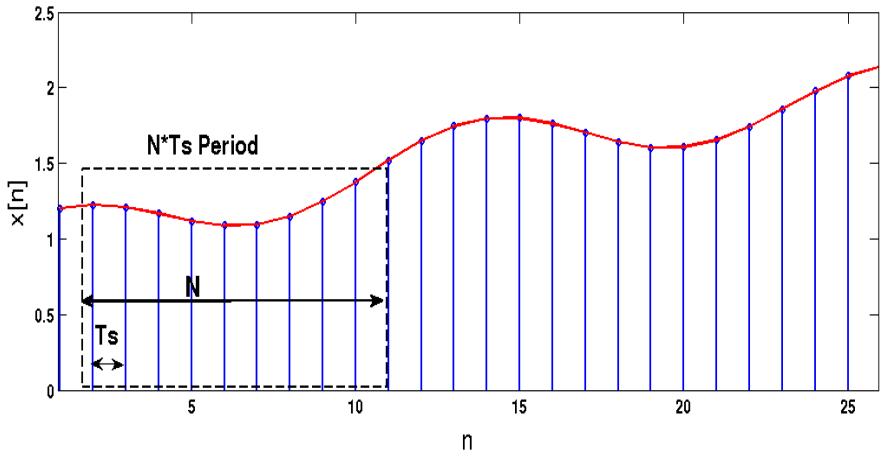

Figure 38: Sampling windows for the input signal

4.2. Sampling Frequency Selection and Application to Modulated Signals

In order to estimate the power of an input signal for a given time interval *T*, the sampling frequency should be determined first. Since the sampling frequency f_s will be below the Nyquist rate, the overlapping of the adjacent replicas is the main issue that should be considered. In Figure 36, the subsampling technique divides the frequency axis into aliasing and aliasing-free regions. These regions are discrete and adjacent areas that are formed according to the following formulas [9]:

$$2f_H/K \leq f_s \leq 2(f_H - B)/(K - 1) \quad \text{Eq.3.3.3.11}$$

$$1 \leq K \leq \lfloor f_H/B \rfloor \quad \text{Eq.3.3.3.12}$$

where K is an integer number, and f_H is the highest frequency component of the signal given by,

$$f_H = f_c + B \quad \text{Eq.3}$$

The sampling frequency should be chosen according to Eq.3.3.3.11 in order to avoid aliasing [9].

In order to clarify the sampling frequency selection method, consider the example of the *AM* modulated signal shown in Figure 39. The unmodulated signal is a *4-KHz* bandwidth baseband voice signal. The signal is sampled with a sampling frequency $f_0 = 384\ KHz$. This high sampling rate guarantees that the base band signal is close to a realistic representation of the actual continuous analog voice signal. This highly-sampled baseband signal is *AM* modulated with a carrier frequency of $f_c = 455\,KHz$ to produce the final modulated signal, as shown in Figure 39.

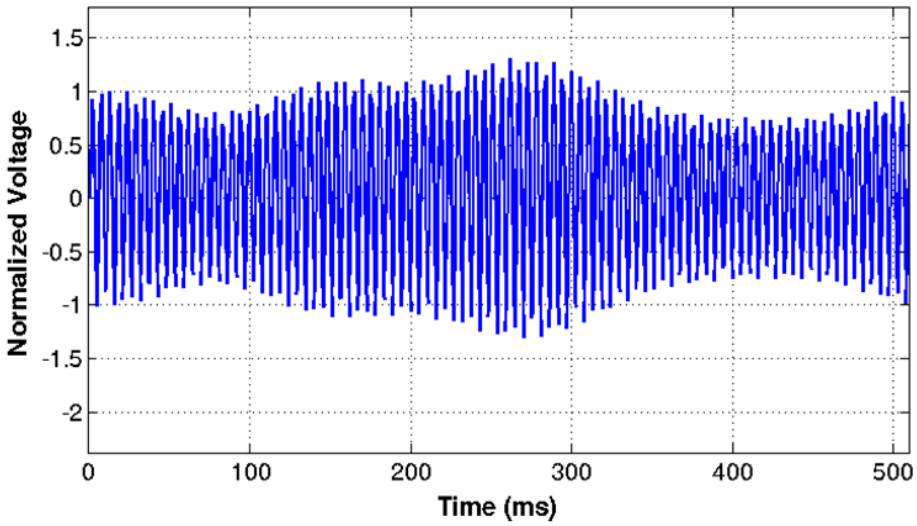

Figure 39: Example AM modulated signal.

The sampling frequency f_s that should be chosen to estimate the power of this *AM* signal with the subsampling approach from the modulated signal should be calculated according to Eq.3.3.3.11, Eq.3.3.3.12 and Eq.4.2.2 as follows:

For $f_c = 455$ KHz and B = 4 KHz, according to Eq.4.2.2,

$f_H = 455 + 4 = 459\ KHz$, then substituting f_H and B in Eq.3.3.3.12 yields

$$1 \leq K \leq \lfloor 459/4 \rfloor \rightarrow 1 \leq K \leq \lfloor 114.75 \rfloor$$

For minimum possible sampling frequency K should be maximum, which implies K_{max}= 114. Then by substitutingK_{max}, f_H and B in Eq.3.3.3.11 one gets,

$$(2 \times 459)/114 \ \leq f_s \leq 2 \times (459 - 4)/(\ 114 - 1)$$

$$8.0526 \leq f_s \leq 8.0531\ KHz$$

For this work, f_s is chosen as $8.053\ K\ Hz$ which is nearly double the signal bandwidth.

After determining the f_s that is required by the estimation method according to the input signal bandwidth, it can be assumed that the power of this *AM* modulated signal needs to be estimated for a time interval of *T*, then:

$$N_0 = T * f_0 \qquad \text{Eq.4.2.3}$$

where N_0 is the total number of samples within measurement time interval *T* that is sampled with $f_0$of *384 KHz*.

The total number of samples within the measurement time interval *T* that is sampled with f_s is given by

$$N = T * f_s \qquad \text{Eq.4.2.4}$$

where f_s is the actual sampling frequency calculated for using the subsampling method.

The exact power P_{Ex} for the time interval *T* according to 4.1.1 is

$$P_{ex} = \frac{1}{N_0} \sum_{n=1}^{N_0} |x[n]|^2 \qquad \text{Eq. 4.2.5}$$

and the estimated power P_{est} for the time interval *T* according to 4.1.1 is

$$P_{est} = \frac{1}{N} \sum_{n=1}^{N} |x[n]|^2 \qquad \text{Eq. 4.2.6}$$

For a chosen time interval, *T* of *0.375 ms*, the exact power, P_{ex}, can be calculated using the oversampled (*384 KHz*) version of the signal as follows. The number of samples that exists in this time interval can be calculated according to Eq.4.2.3 as:

$$N_0 = 0.375 * 10^{-3} * 384 * 10^3 = 144 \text{ samples.}$$

Calculating the exact power of the *AM* modulated signal in the first *0.375 ms* time interval can then be calculated as:

$$P_{ex} = \frac{1}{144} \sum_{n=1}^{144} |x[n]|^2 = 0.410 \ Watt \text{ (Normalized)}$$

To calculate the estimated power for the same time interval taking the subsampling approach, the *AM* modulated signal is subsampled with $f_s = 8.053\ KHz$. By substituting $f_s = 8.053\ KHz$ and *T=0.375 ms* into Eq.4.2.4 yields

$$N = 0.375 * 10^{-3} * 8.053 * 10^{3} = 3 \text{ samples.}$$

Calculating the estimated power of the *AM* modulated signal in 0.375 ms using the subsampling approach by utilizing Eq.4.2.6 results in:

$$P_{est} = \frac{1}{3} \sum_{n=1}^{3} |x[n]|^2 = 0.4291\ Watt \text{ (Normalized)}$$

The error produced by the estimation method can be calculated in dB (dBFS for digitally stored signals) according to the following formula:

$$err = 10 \log\left(1 + \left|\frac{P_E - P_T}{P_T}\right|\right) \qquad \text{Eq. 4.2.7}$$

By substituting P_{ex} and P_{est} values in Eq.4.2.7:

$$err = 10 \log\left(1 + \left|\frac{0.4291 - 0.410}{0.410}\right|\right) = 0.1973\ dBFS$$

Note that the decibel relative to full-scale (dBFS) unit is used instead of the absolute dB due to the sample values of the signal that are stored digitally as waveform audio file format. In this file format, the sample values are normalized to be in the 0-255 range, or –1 to 1. By taking the logarithm for the exact, the estimated power values and error will result in a unit of dBFS instead of the absolute dB.

The general procedure for estimating the signal power with subsampling can be further simplified by rewriting Eq.4.2.3, and Eq.4.2.4 as follows. Dividing Eq.4.2.4 by Eq.4.2.3:

$$\frac{N}{N_0} = \frac{T * f_s}{T * f_0} \quad \rightarrow N = \left(\frac{f_s}{f_0}\right) * N_0 \qquad \text{Eq. 4.2.8}$$

Substituting Eq.4.2.8 in Eq.4.2.6 yields

$$P_{est} = \left(\frac{f_0}{f_s N_0}\right) \sum_{n=1}^{\frac{f_s N_0}{f_0}} |x[n]|^2 \qquad \text{Eq. 4.2.9}$$

For $f_s = 8.053\ KHz$, and $f_0 = 384\ KHz$, $N = (8.053\ KHz/384KHz\ ) * N_0 \cong N_0/48$, then substituting N in Eq.4.2.9,

$$P_{est} = \left(\frac{48}{N_0}\right) * \sum_{n=1}^{\left(\frac{N_0}{48}\right)} |x[n]|^2 \qquad \text{Eq. 4.2.9}$$

The exact power of the *AM* signal is calculated according to Eq.4.2.5, whereas the estimated power can be calculated according to Eq.4.2.9. The error is then calculated according to Eq.4.2.7.

By comparing Eq.4.2.5 and Eq.4.2.9, it can be seen that the number of samples *N* used to estimate the power P_{est} is 48 times less than the number of samples N_0 used to calculate the exact power, P_{ex}. The error produced by Eq.4.2.9 with respect to Eq.4.2.5 is 0.1973 dBFS for 3 samples of subsampling. If a higher number of samples were to be taken, e.g. 50 samples instead of 3, it would be seen that the error would drop to –0.06 dBFS. Obtaining a higher number of samples is definitely not necessary since the error obtained with the subsampling approach with 3 samples already yields a significantly small error of 0.2 dBFS. In communication systems, errors of +/– 1 dB are always considered to be acceptable error levels for the system. This result by itself demonstrates the validity of the idea of using the subsampling method for estimating power, which will be further verified with simulation results for signals with different modulation schemes.

Increasing the sampling rate to more than twice the bandwidth of 2B (subsampling approach) allows the *ADC* to collect more samples in the same time window, as shown in Figure 37. This produces more accurate estimates due to better averaging. However, increasing the number of samples within the same time window does not show a significant improvement in the error of the power estimation at a higher sampling rate, as shown in Figure 40. After a certain number of samples, the increase in the sampling rate will lead to more power dissipation in the *ADC* due to the higher sampling rate although there is no significant reduction in the error.

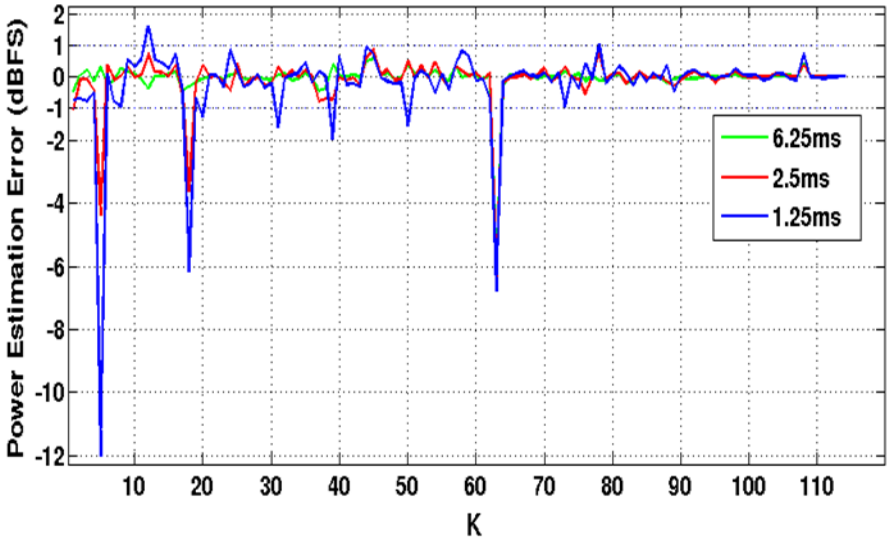

Figure 40: Power estimation error vs subsampling factor K according to Eq.3.3.3.11.

In Figure 40, an *AM* modulated signal with a *4-KHz* bandwidth is subsampled with all the possible sampling frequencies according to Eq.3.3.3.11, which extends from 2B to $2f_H$. The minimum possible sampling frequency 2B corresponds to $K_{max} = 114$, and the maximum sampling frequency corresponds to K_{min}=1. The power estimation calculation was performed for three different time intervals (6.25*ms*, 2.5*ms*, 1.25*ms*) of the *AM* modulated signal, which corresponds to 50, 20, and 10 samples that the minimum sampling frequency of *8 KHz* could provide. For the remainder of the sampling frequencies greater than 2B, the number of samples is much higher for the same time intervals. Note that *K* represents the number of signal replicas on the frequency axis, and for each different *K*, there will be a different f_s according to Eq.3.3.3.11. Most of the frequencies produce an error within 1 dBFS, while the remaining frequencies produce higher error values that are caused by the aliasing of these frequencies. As the time interval of the signal grows larger, the error produced will be lower, as shown for the three different time intervals in Figure 41, due to better averaging.

The results in Figure 40 can be discussed from a statistical point of view. When more samples are collected within the same time window, the sample values will not have a significant deviation from the mean value. In Figure 41, the blue and red

samples are the actual samples representing an analogue signal, while the red ones are the useful samples for power estimation. The average of the two red samples is close to the average of all the blue and the red samples with a very small error. From the signal perspective, the analogue information does not change significantly in amplitude within a relatively short time interval. Thus, taking many samples in a relatively short time interval will not enhance the power estimation significantly while increasing the power dissipation of the *ADC* due to a higher sampling rate. This statistical nature of the signal is also shown in Figure 42, where increasing the sampling frequency to five times greater than *2B* does not result in a significant reduction in the power estimation error, due to the statistical nature of analogue signals.

A formula cannot be developed to relate the power estimation error to the measurement time. Training the system would be a proper choice to estimate the time required by the method for a given measurement error for a signal with a certain modulation scheme. This training approach is not studied in this work.

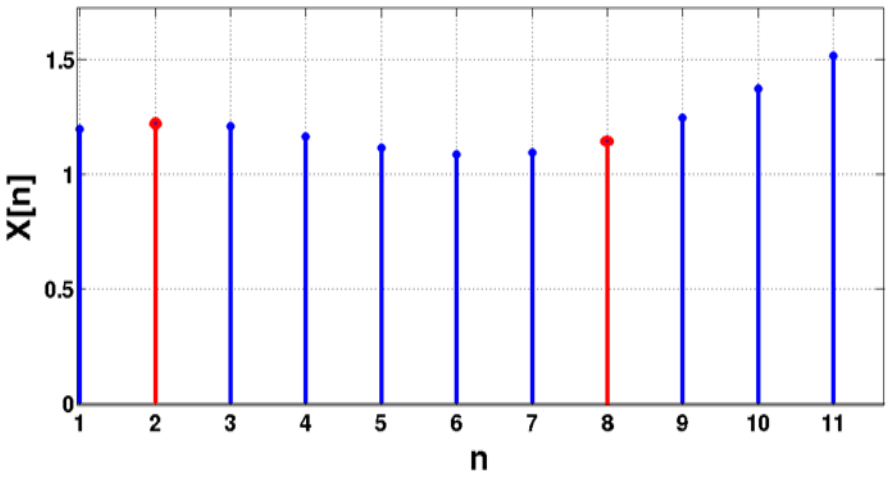

Figure 41: Example sample values of an analogue signal.

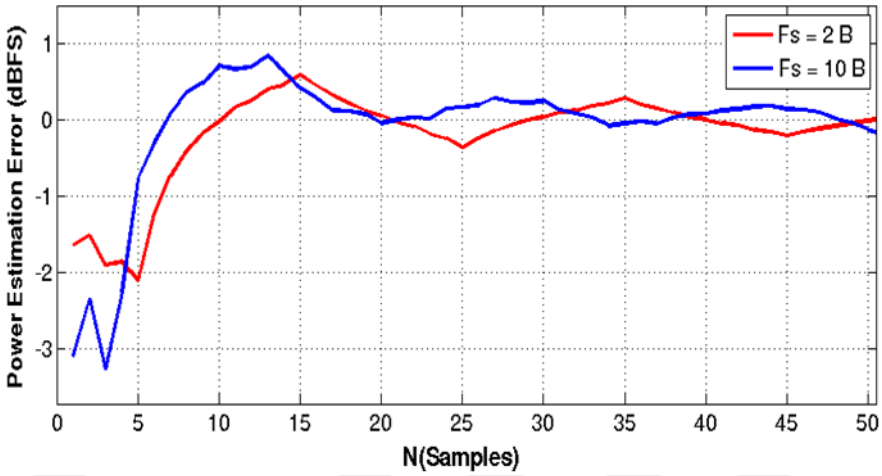

Figure 42: Error curves of two different sampling frequencies for power estimation of the AM modulated signal.

4.3. Testing Mechanism and Conditions

The method introduced in (4.1) previously is tested through simulations in the MATLAB tool. Two modulated signals are considered for the simulations. The first is a 4-*KHz* bandwidth voice signal which is *AM* modulated with a carrier frequency of 455 *KHz* for a 6.5 *ms* duration. The second signal is a 10-*KHz* bandwidth *QAM* signal with a carrier frequency of 455 *KHz* for a duration of 2.5 *ms* with different modulation levels, *M*. In simulations, to estimate the power, modulated signals are processed with the method introduced in Section II. A measurement error less than 3 dB is a generally an acceptable error level in communication systems. For the accuracy criteria for the simulations in this work, a more strict error window of a –1 to +1 dBFS range is adopted. This does not mean that the error levels higher than 1 dB are not strictly acceptable. To characterize the accuracy of subsampling method, power estimation error curves are presented for each modulated signal.

4.4. Power Estimation for AM Modulated Signals

Figure 43 shows the exact and estimated power curves for the *AM* modulated signal. The error produced by the power estimation is shown in Figure 44. According to

the subsampling method, a sampling frequency twice the signal bandwidth can produce enough number of samples for accurate results in power estimation. This means that 2 samples are needed for each cycle of the highest frequency component of the signal. This will guarantee that the power estimation will be acceptably low. This is demonstrated in Figure 44, where the error is 0.1076 dBFS for the first 2 samples. For the next 13 samples, it changes rapidly to reach 0.1689 dBFS, then it fluctuates around 0.3 dBFS until it reaches 0.01672 dBFS at sample number 50 due to the statistical nature of the signal. As can be seen from the error curve, more than 2 samples is not needed to have a very low power estimation error.

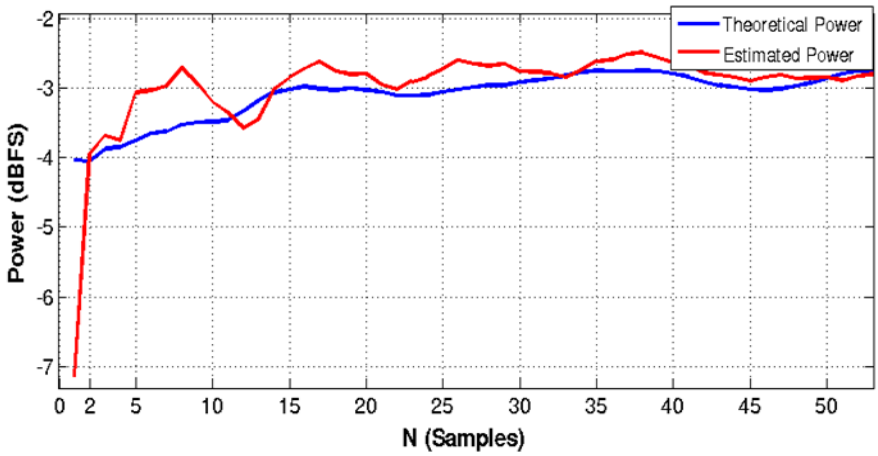

Figure 43: Theoretical and estimated power values vs. number of samples for the AM modulated signal

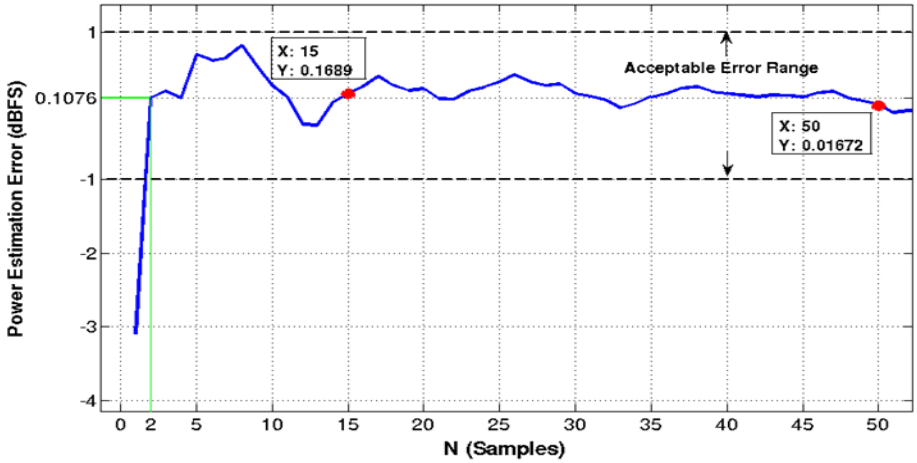

Figure 44: Power estimation error for the AM signal

4.5. Power Estimation for M-QAM Modulated signals

The subsampling method is applied to different *QAM* modulated signals with different levels, *M*. Figure 45 shows the spectrum of the M-QAM signals where the bandwidth is approximately 10-KHz. The same procedure that is used for the power estimation of the *AM* signal is used for the *QAM* signals to calculate the exact and estimated power values and to calculate the error in between. Figure 46 shows the theoretical (exact) and estimated power curves for a *4-QAM* signal. For the 4-*QAM* signal shown in Figure 47, the error is +2.803 dBFS for the first 2 samples, then for the next 14 samples, the error value is fluctuates from +1.595 dBFS to +2.495 dBFS. In the next 14 samples, it decreases gradually to reach –0.104 dBFS; then it is within the range of 0 dBFS to –1 dBFS for the remaining 20 samples to reach –0.476 dBFS at sample number 50.

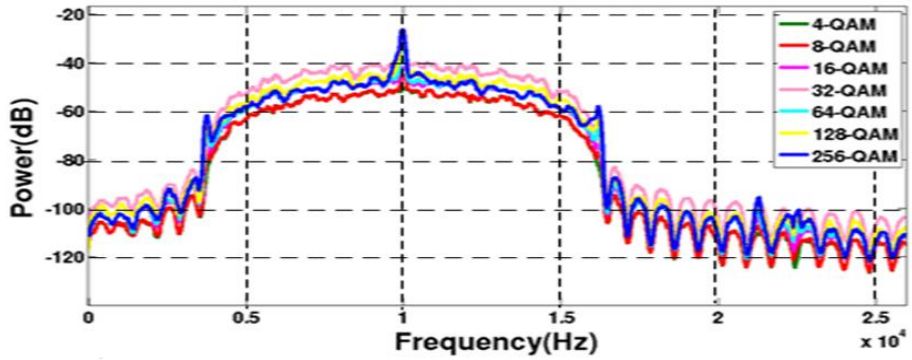

Figure 45: M-QAM signal bandwidth

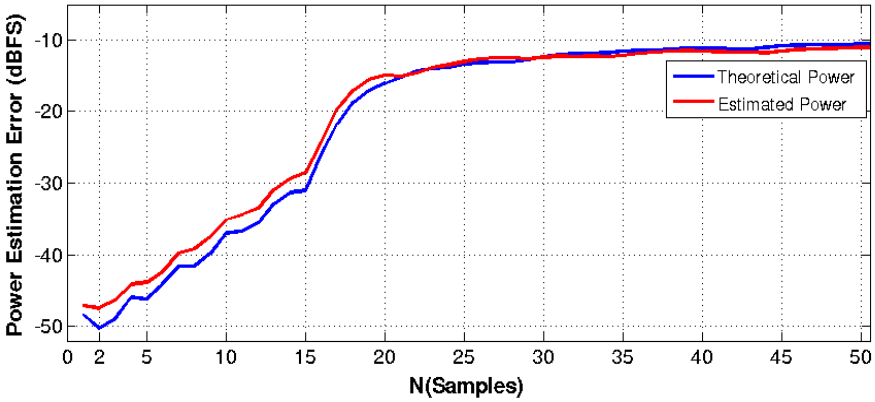

Figure 46: Theoretical and estimated power values vs. number of samples for the 4-QAM modulated signal.

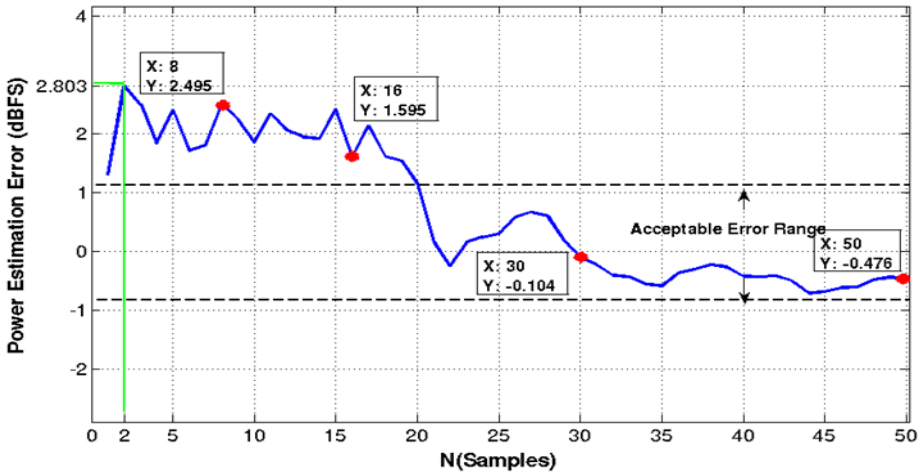

Figure 47: Power estimation error for the 4-QAM signal

For the 8-*QAM* error plot shown in Figure 48, the error is –-4.338 dBFS for the first 2 samples. After sample number 2, it rapidly changes to reach –0.8525 dBFS within the next 4 samples. For the next 31 samples, it gradually decreases from –1 dBFS to reach –0.05689 dBFS, which does not show a significant change until sample number 50.

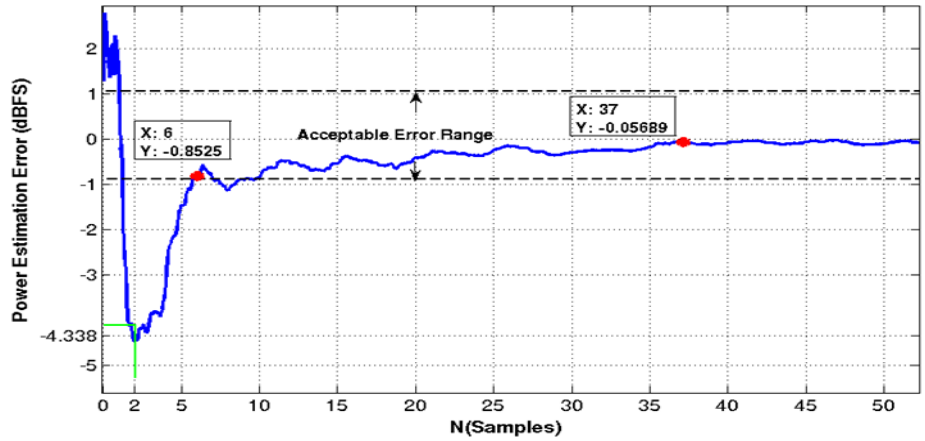

Figure 48: Power estimation error for 8-QAM signal.

The 16-*QAM* error plot, shown in Figure 49, has an error value of —0.3886 dBFS for the first 2 samples. This value is far lower than the one for the *4-QAM* case. For the next 6 samples, it increases rapidly to reach —0.6233 dBFS at sample 8, then it decreases to reach the minimum value of –0.008 dBFS at sample number 15. In the next 10 samples, the error increases to reach –0.3555 dBFS, which does not change

significantly for the next 10 samples. For the last 15 samples, the error increases slightly to reach –0.5661 dBFS at sample number 50.

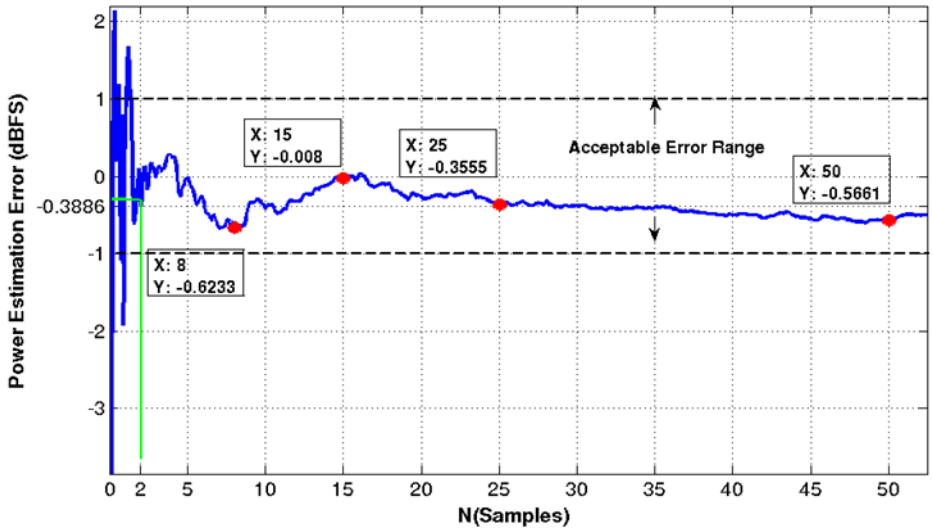

Figure 49: Power estimation error for the 16-QAM signal

For the 32-*QAM* error plot, shown in Figure 50, the error value for the first 2 samples is 0.9443. For the next 8 samples, it decreases rapidly to reach 0.1454. In the next 6 samples, the error increases rapidly to reach 0.4452 dBFS at sample number 16, then it decreases gradually for the next 14 samples to reach 0.0179 dBFS at sample number 30. For the last 20 samples, the error increases slightly, and then decreases again to reach –0.001 dBFS at sample number 50.

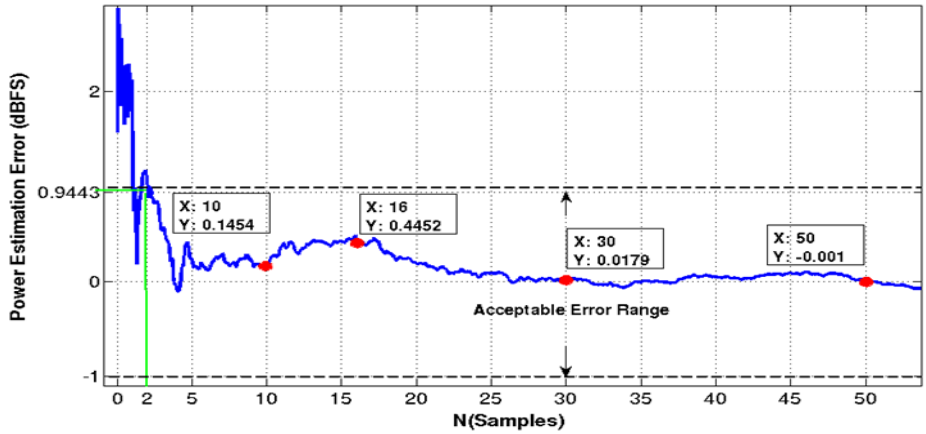

Figure 50: Power estimation error for the 32-QAM signal

For the 64-*QAM* error plot, shown in Figure 51, the error is 0.3672 dBFS for the first 2 samples. For the next 8 samples, the error changes rapidly to reach –0.5505 dBFS. For the follow 25 samples, the error decreases gradually to reach –0.0397 dBFS at sample 35. In the next 10 samples, the error increases slightly to be –0.1395 dBFS, and then it decreases again for the last 5 samples to reach –0.1137 dBFS at sample 50.

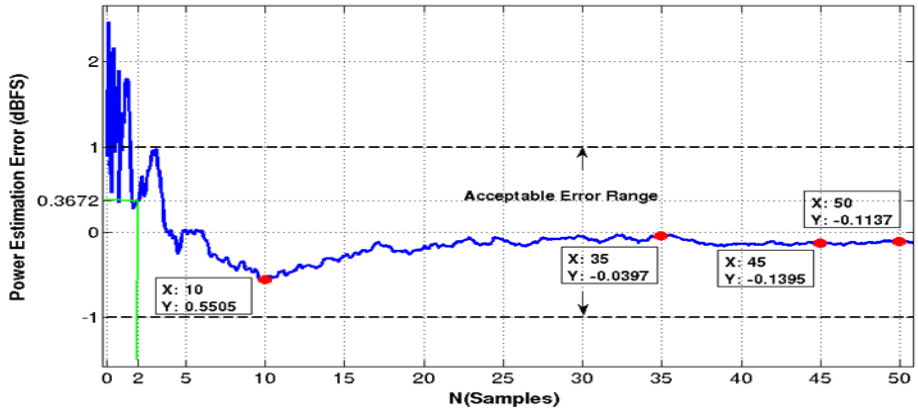

Figure 51: Power estimation error for the 64-QAM signal.

For the 128-*QAM* error plot, shown in Figure 52, the error value is 1.18 dBFS for the first 2 samples. For the next 8 samples, it rapidly decreases to reach 0.0449 dBFS, and then it gradually increases in the next 10 samples to reach –0.2061 dBFS. In the next 15 samples, it decreases again to reach –0.0375 dBFS at sample number 35, and then it increases slightly in the last 15 samples to reach –0.2025 dBFS at sample number 50.

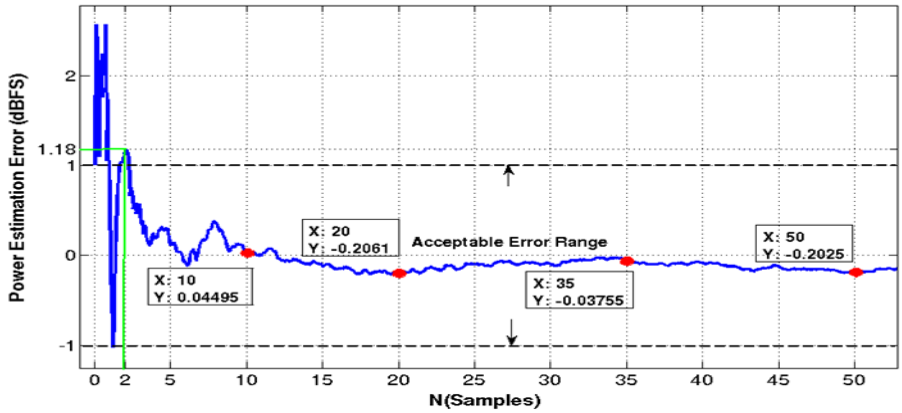

Figure 52: Power estimation error for the 128-QAM signal

For the 256-*QAM* error plot, shown in Figure 53, the error value is –2 dBFS for the first 2 samples. For the next 8 samples, it decreases rapidly to reach –0.148 dBFS. For the next 11 samples, it increases slightly, and then decreases to reach 0.0413 dBFS, which does not show significant change for the next 10 samples. For the next 19 samples, the error increases slightly to reach –0.2252 dBFS at sample number 50.

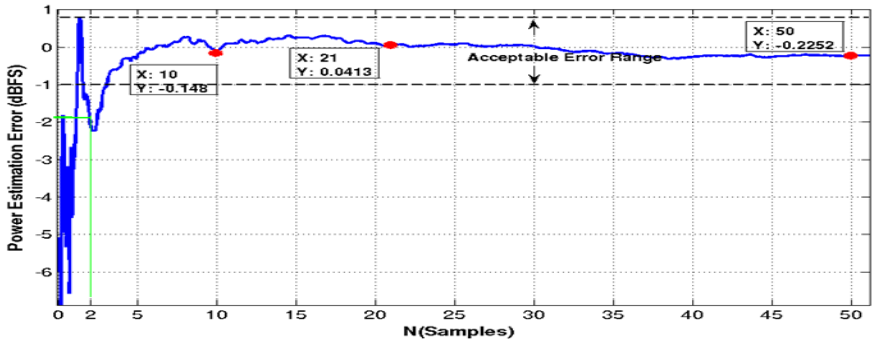

Figure 53: Power estimation error for the 256-QAM signal

For all the error plots (except for 8-*QAM*), the error value is within the conventionally acceptable range of less than 3 dB for the first 2 samples. For the case of 8-*QAM*, the error was larger than expected due to the statistical nature of the signal. Nevertheless, waiting for 3 more samples will cause the error to fall within the acceptable range, as shown in Figure 48. The previous error plots for the power estimation of the M-*QAM* modulated signals show the same behaviour. This demonstrates that even if the signal has a complex waveform and high dynamic range, this estimation method shows the same performance. As shown in Figure 45, all the *M-QAM* signals have nearly the same bandwidth. This allowed the use of same sampling frequency for all the *M-QAM* simulations. Furthermore, the error results obtained have error ranges very close to each other and within acceptable values. Therefore, it is seen that independent of the constellation of the *QAM* signals, so long as the bandwidth is same, reasonably low error values will be obtained. Another important conclusion is that the minimum number of samples yielding a reasonably low error is 2 samples, as stated by the subsampling approach. For further reduction in the error, a longer power estimation interval or a higher sampling frequency should be considered.

CHAPTER 5:

5. CONCLUSION AND FUTURE WORK

5.1. Conclusion

A digital power estimation method is presented in this study as an alternative to analog power estimation techniques where less analog processing would mean less spread over PVT. The digital processing, besides being much less sensitive to PVT variations for an application-specific integrated circuit (ASIC) implementation, makes the estimation of the signal power more flexible. Self-calibration could be performed through the use of on-chip signal feeding to the estimator input to generate a dynamically changing look-up table (power vs. the digital code). The main parameter that should be considered when using the presented subsampling method is the input signal bandwidth irrespective of the carrier frequency. The minimum number of samples that could produce an acceptably low error level is 2 samples, which corresponds to a sampling period of $T_{min} = 1/f_s$. A sampling frequency of *2B* is sufficient to produce an acceptable error of less than 3 dB for the first 2 samples ($T_{min} = 1/f_s$), and a more strict error range of –1 to +1 dB within the first 50 samples ($T = 50\ T_{min}$) depending on the type of modulation. Selecting a sampling frequency higher than *2B* does not produce a significant improvement (as shown in Section 3) while increasing the power dissipation of the ADC. The required estimation time, and the error produced accordingly, can be controlled within the power code calculation block with a trade-off between the estimation time and estimation error. The method was applied to estimate the power of the AM modulated signal, and the error was 0.1076 dBFS for the first 2 samples ($T_{min} = 125\ \mu s$) and approximately 0.2 dBFS for the first 50 samples (6.25 *ms*). It is also applied to QAM signals with different modulation levels, where the error was within the acceptable range (less than 3 dBFS) for the first 2 samples (50 μs). For other modulation schemes, the same performance of the power estimation method is expected to result in similar error performance. For the circuit implementation of

this method, a relative degradation in error characteristic should be expected due to circuit noise and ADC quantization noise.

5.2. Future Work

More simulations with different signal scenarios that include different bandwidths and more complex envelop signals should be done. This will lead to further investigation into the estimation method reliability and offer new improvements. Simulating and testing the on-chip self-calibration is another core advantage which needs to be ascertained in order to make the module compatible with more communication system receiver applications. The self-calibration should compensate for any unexpected errors that may occur due to various testing environments. Continuing one step further, using the same feedback (ADC+DSP) for the baseband loop will be a more interesting objective, where any lack of signal power adjustment in the RF loop might be compensated for in the baseband loop. Then, testing the suggested module within modern communication systems in LTE and 5G will be a significant task in the future work of this study.

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