UNIVERSITY OF TURKISH AERONAUTICAL ASSOCIATION
INSTITUTE OF SCIENCE AND TECHNOLOGY

DESIGN, MODELING AND IMPLEMENTATION OF MULTI-FUNCTION PROTECTIVE RELAY WITH DIGITAL LOGIC ALGORITHM

MASTER THESIS

Muhanned Mahmood Shakir AL-SHALAH

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

PROGRAM OF ELECTRICAL AND ELECTRONICS ENGINEERING

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Supervisor: Assist. Prof. Dr. Javad RAHEBI

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I hereby declare that all the information in this study I presented as my Master's Thesis, called: "Design, Modeling and Implementation of Multi-Function Protective Relay With Digital Logic Algorithm", has been presented in accordance with the academic rules and ethical conduct. I also declare and certify with my honor that I have fully cited and referenced all the sources I made use of in this present study.

29.11.2017

Muhanned Mahmood Shakir AL-SHALAH

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Thanks to the most compassionate, gracious and merciful. May Allah's blessings and peace be upon our prophet Mohammed who protects us from the depths of darkness and leads us forth into light, and his household.

It is a pleasure to express my special thanks to the fountain of patience, optimism and hope my dear mother, to the big heart my dear father who inspired me, to those who have demonstrated to me what is the most beautiful of life my wife and my beautiful daughters for their valuable support.

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November 2017 Muhanned Mahmood Shakir AL-SHALAH

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LIST OF ABBRIVIATION

CORDIC	**:**	Coordinate Rotation Digital Computation
DFT	**:**	Discrete Fourier Transform
FPGA	**:**	Field Programmable Gate Array
VHDL	**:**	VHSIC Hardware Description Language
PC	**:**	Personal Computer
RTL	**:**	Register-Transfer Level
LUT	**:**	Lookup table
HDL	**:**	Hardware Description Languages
EM	**:**	Electromechanical
SS	**:**	Solid-State
HMI	**:**	Human-Machine Interface
ARM	**:**	Acorn RISC Machine
OQE	**:**	overall quantization error
PSM	**:**	Plug Setting Multiplier

ABSTRACT

DESIGN, MODELING AND IMPLEMENTATION OF MULTI-FUNCTION PROTECTIVE RELAY WITH DIGITAL LOGIC ALGORITHM

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Thesis Supervisor: Assist. Prof. Dr. Javad Rahebi

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In this thesis, three phase transmission power system with three different protective schemes such as over current relay, over and under voltage relay and over and under frequency relay developed using MATLAB/Simulink toolbox. The protective relay tested for different operating conditions of the transmission power system such over load condition, over and under voltage condition, over and under frequency condition. Protective relays explained with simple flowchart. We used digital logic algorithm for implementation of protective relay. In this thesis, a digital multi-function protective relay designed and implemented on the MATLAB / Simulink. The study included exploring various present techniques ranging from the use of digital logic algorithms to system protection application. Mother power system protective relays are digital systems based on the digital signal processing of power system voltage and current waveforms.

Keywords: Multi-Function, Protective Relay, Simulink Model.

ÖZET

SAYISAL MANTIKSAL ALGORİTMA İLE ÇOKFONKSİYONLU KORUMA RÖLESİNİN TASARIMI, MODELLENMESİ VE UYGULANMASI

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Bu tez çalışmasında, aşırı akım rölesi, aşırı gerilim rölesi ve aşırı gerilim rölesi gibi üç farklı koruma şemasına sahip üç fazlı iletim sistemi, MATLAB / Simulink araç kutusu kullanılarak geliştirilmiştir. Koruyucu röle, aşırı yük koşulları, aşırı ve gerilim altında koşullar, aşırı ve düşük frekans koşulları gibi iletim güç sisteminin farklı çalışma koşulları için test edilmiştir. Koruyucu roleler basit bir akış şeması ile açıklanmıştır. Koruyucu role için dijital mantık algoritması kullandık.

Bu tezde, MATLAB / Simulink üzerinde tasarlanmış ve uygulanmış bir sayısal çok fonksiyonlu koruyucu röle. Çalışma, sayısal mantık algoritmalarının kullanımından system koruma uygulamasına kadar çeşitli mevcut teknikleri keşfetmeyi içeriyordu. Ana güç sistemi koruma röleleri, güç sistemi voltajı ve akım dalga formlarının dijital sinyal işlemesine dayanan dijital sistemlerdir.

Anahtar Kelimeler: Çok Fonksiyonlu, Koruyucu Röle, Simulink Modeli.

CHAPTER ONE

INTRODUCTION

1.1 Background

In power system, fault occur randomly irrespective to time. Due to fault or abnormal conditions, it will affect the performance of the power system i.e., damage the device connected in the power system. In order to safe card the device, relay and circuit breaker has been developed. The protective relay is used to detect the abnormal conditions of the power system and send the trip signal to circuit breaker for isolate the system from abnormal conditions. The protective relay play important role in the power system protection and protective relay can be classified into four category that are,

1. Electromechanical relay
2. Static relay
3. Digital relay
4. Numerical relay

1.1.1 Electromechanical Relay

Electromechanical relay is oldest type relay and it has been used for so many years. This type of relay could be classified into two, one is electromagnetic attraction type relay and electromagnetic induction type relay. It has some limitations,

a) Speed of operation of relay is very low.
b) Due to ageing, changes in characteristics of relay.
c) Failure in relay operation due to component damage in the relay.

d) Size of this relay is normally bulky.
e) Data relevant to fault not available in this relay.
f) Regular replacement of relay is needed for effective protection of power system.

1.1.2 Static Relay

The next generation relay is static relay. No moving parts in the static relay and it consists of transistor, capacitor, integrated circuit and small microprocessors. It has some limitations,

a) For proper operation of relay, it need auxiliary voltage.
b) This relay is sensitive to transient's voltage of the breaker.
c) Voltage spikes for small duration will affect the component of the relay.
d) The characteristics of relay changes with respect to changes in ambient temperature.
e) Data relevant to fault not available in this relay.
f) Proper isolation and filter circuits are needed for relay for electromagnetic inference protection.

1.1.3 Digital Relay

This is advanced version of static relay and this relay uses the advantages of microprocessors and microcontrollers. Analog signal is processed in the static relay but in this relay analog signal is converted into digital signal using analog to digital converters. It has some limitations,

a) Lifetime of this relay is limited due to continuous development of new technologies.
b) The devices turn into outdated rapidly.
c) Due to power system transients there will be a malfunction in relay.
d) Regular maintenance required for settings and monitoring of data.

1.1.4 Numerical Relay

The electromechanical and static relay are hard wired relay and setting is changed manually but numerical relay is programmable relay. The characteristics

and settings of the relay could be programmed. the operation of this relay same that of the digital relay but only difference, the numerical relay uses the advanced digital signal processor as a main part.

1.2 Digital Logic

The digital electronics is a defined discipline in the field of electronics , in which in principle only operate with signals in two different sizes with respect to either current or voltage (as opposed to analog electronics in which signals can assume all possible sizes within given ranges).

Digital signals are discretized in both value and time, which means that digital signals only assume a limited number of possible values, and only at defined times. You can not say anything about the digital signal outside these times. This is the main theoretical difference between digital signals and analog signals that are continuous (ie they can assume any value in any time period). A little simplified, one can say that a digital signal is either "on" or "off".

Digital circuits closely follow certain mathematical principles (symbol logic) and can, among other things, be used to perform calculations (on binary numbers). For this reason, the two different signal sizes are called "0" and "1".

1.3 Digital Logic in Practice

Most often two different voltages are used; "0" is represented by a voltage within a given range and "1" at a voltage in a different range - between the two intervals there is an area of "unused" voltages, the so-called prohibited zone.

Generally, so-called positive logic is used, where the highest voltage range represents "1" and the lowest "0" - negative logic means a low voltage such as "1" and a higher voltage such as "0". In conjunction with positive logic, the signal "1" is also referred to as high (English for "high") and "0" as low (English for "low").

"Receivers" of the digital signals are designed to be quite "tolerant"; Everything over a certain voltage limit is interpreted (by positive logic) as "1", and all under "0". This, together with the two separate, "legal" voltage ranges, means that digital circuits are highly tolerant to electrical noise.

1.4 Digital Circuits

The subcategories that digital electronics are built up can be classified in a linear hierarchy, where more complex circuits are built up by several of the simpler circuits.

1. The basic building elements

a) Gates

b) inverters

c) transmission Gates

2. Combinatorial circuits

a) Adder

b) comparator

c) Multiplexers and demultiplexers

3. Sequential circuits

a) Flip-flop

b) Shift register

c) Counting

4. Larger digital circuits

a) embedded system

b) microprocessor

c) microcontroller

1) VHDL - language appealed by IEEE to construct / program the chips with:

a) SPLD , Simple Programmable Logic Device (Manufacturer Name : PAL (Logic Circuit), GAL, PLA, PLD)

b) CPLD , Complex Programmable Logic Device (Manufacturer Names: EEPLD, EPLD, MAX , PEEL)

c) FPGA , Field Programmable Gate Array (Manufacturer Names: ACT, APEX, FGPA, FLEX, LCA, ORCA, PASIC, Virtex)

d) FPIC, Field Programmable Interconnect Chip

e) ASIC (unknown if possible)

f) FPLA (unknown eventual classification)

Larger digital systems such as sequence networks and the even more complex CPUs are (central units for computers) based on the above-mentioned sub-circuits.

1.5 Synchronous and Asynchronous Digital Circuits

Today, the vast majority of the digital circuits of the synchronous type, which means that it has a central clock generator (Eng. Clock), which allows high-speed communications via the data buses between closely related larger digital sub-circuits.

Both in low-energy and digital high-performance circuits, there may be a problem with a central tachometer in, for example, a digital hearing aid or a microcontroller. The reason is that you want the hearing aid to use as little energy as possible, and high-performance circuits lose the beat when the central ringer's frequency increases (for example, overclocking). The reason is that it takes time for the tachograph and data bus signals to get around in different parts of the chip at high frequencies - and despite the fact that the signals propagate by approximately 2/3 of the speed of light.

Redesign of digital circuits, introduction of decentralized self-rate / asynchronous, achieves less energy consumption or the possibility of higher rate of rotation. The cost is roughly a loss of service of approx. 10% at a given frequency, but with drastically reduced energy consumption eg. -30 ...- 60%. [1] [2] Which means that you can increase the decentralized tactors by 30%. [3] [4] [5] Furthermore, self-tapped circuits less noise.

1.6 Logical Systems

On the purely theoretical level, digital electronics do not "think" about how the simplest building elements, gates and invert, "carry on" in performing their tasks. The principles of the digital basic elements, gates and inverters, can and will also be realized in hydraulic, mechanical and pneumatic devices.

1.7 Objective of This Thesis

1) To design protective relay for a three phase power system such as over current relay, over voltage relay, under voltage relay, over frequency relay and under frequency relay.
2) Simulation of the above relay using MATLAB / Simulink toolbox.
3) HDL code generation and FPGA programming of above relay in the MATLAB Software.

4) Testing the Register-Transfer Level (RTL) logic of FPGA code generated from MATLAB using Xilinx ISE 9.2i Software.

1.8 Problem Definition

Protective relay is for safety an integral part of the electrical system. Compared with static relay or analogue, digital relay usually lack the computational resources but provides a wider range of settings and other digital functions. Here we use digital logic algorithm to implement the flowchart relay. The digital logic, is a simple and efficient, all the mathematical calculations and algorithms in the meter relay can be operated with a digital logic processor. Even if the relay is used to cover the multi-channel sources and different algorithms relay, processing speed must be suitable for operation in real time. As the digital model has been adapted for the characteristics of the current time is not a simple curve and not LUT (lookup table) based on extrapolation, this model provides convenience not only different characteristic curves for the relay coordination, but behavior relay very accurate due to the inherent accuracy of the algorithm digital logic algorithm.

1.9 Proposal Work

In this thesis, a digital multifunction relay will be designed and implemented on FPGA. The study will include exploring various present techniques ranging from the use of digital logic algorithms to system protection application. The contributions will be mainly in the design of an efficient FPGA architecture. Mother power system protective relays are digital systems based on the digital signal processing of power system voltage and current waveforms.

1.10 Requirements

Hardware requirements: one personal computer.
Software requirements: MATLAB/Simulink and Xilinx 9.2i

CHAPTER TWO

LITERATURE REVIEW

2.1 Literature Review

Inverse over current relay is implemented using 8 bit 8085 microprocessor [3]. Integrated type and look up table based time- current characteristics is realized using function generator program of microprocessor.

Field programmable gate array based over current relay is developed for 360 km transmission line [4]. Finite Fourier transform used for filtering to avoid false tripping in the circuit breaker. Also the status of the current is processed and communicated to central control station.

FPGA based over current relay, phase loss and locked rotor is simulated and implemented in Xilinx XC4020 FPGA [5].

The Acorn RISC Machine (ARM) processor based protective relay has been developed for transmission protection [6]. Also DSP based supervised data acquisition for setting and monitoring data is developed.

Microprocessor based protective relay has been developed for AC control power [7]. The multifunction protective scheme is designed in the microprocessor system.

Multifunction protective relay scheme has been developed for substation protection. Protective scheme uses the microprocessor based monitoring and controlling system [8].

Microprocessor based protective scheme has been developed for low voltage micro grids. And also this scheme does not required communication tool for adaptive protection. Transient time simulation was demonstrated for protective scheme using PSCAD/EMTDC software package [9].

Coordinate Rotation Digital Computer (CORDIC) algorithm based protective scheme has been developed for 75 km / 154 kV transmission line. this scheme was tested with four case such as single-line-to-ground, double-line to ground and three phase faults [10].

2.2 OSI Model

In [10] presented a new method for a hardware architecture for a digital relay. All functions can be synchronized to measure and relay coordinate rotation digital computer (CORDIC) algorithm rather than by an approximate generalization and extrapolation is calculated. Protective relays resulting in higher processing capabilities and make it more able to address the sources of parallel multi-channel / digital numerical relay is available. Care coordination can be improved by using the CORDIC algorithm. This architecture has been successfully implemented in CMOS 0.35 LM technology and after it has been approved.

In [11], they note that the overall quantisation error (OQE) above error of fact, in many cases, have led to inefficient architecture. Therefore, this article is an updated equation for OQE the forecast error more precisely. To illustrate the improved accuracy of the new OQE expression, the comparison between systems CORDIC found using both versions of the algorithm OQE and systems directly calculate the amount vector is made. This comparison is of interest as it shows that systems based on CORDIC new OQE expression of FPGA, significantly less than the original algorithm system CORDIC found using direct or equivalent schemes. Due to the widespread use of CORDIC Design FPGA, especially in DSP, this is remarkable.

In [12] in terms of the scale basis, which includes pipeline and parallel -4 new CORDIC architecture is provided. Architecture delay N / 2 clock cycles and the amount of power a valid result in N / 2 hours for the n-bit accuracy. A 16-bit architecture rooted -4 CORDIC on FPGA platform implementation is available. Delays related to architectural eight clock cycles and the potential for a valid result on each cycle of eight hours. The small architectural practice in the 56.96 MHz clock speed with a power consumption of 380 mW. The speed can be enhanced with an upgraded version of FPGA devices. Processor speed is optimized region obtained through this architecture for real-time applications.

Fingerprint recognition is one of the most popular methods used by the biometric identification system to identify personnel [13]. CORDIC algorithm fantastic solution for intensive math operations at the expense of several components such as adder, shifter, multiplexer and so provides. Intensive operations such as math required during the recovery phase of the fingerprint image to do. In [13] CORDIC-based architecture is proposed to evaluate almost all trigonometric functions. This is implemented using XILINX ISE 13.2. Performance architecture in the form of relative error was.

There are two options available operating modes. DFT processing modules, processing modules CORDIC, error detection module, and the module elements of protection: I based options DFT- relay for signal processing hardware is the phasor which consists of four modules. In this case, with regard to the error voltage and current data through I / O interface at first, fundamental amplitude and phase estimation signal DFT module. CORDIC processing and non-linear values of the sine function is to provide the mathematical calculations required. Fault detection module utilizes the DFT results of the mechanism to detect the beginning of a fault on the over-current protection, while the impedance calculation error protection element module and decides the trip logic. If a fault is detected, and the calculated impedance falls into a protected area, a trip signal is sent to the relevant circuit breakers to isolate the fault. In addition, a universal control module is designed to control all functions of the entire design. The second option relay modules are based on the instantaneous signal that can signal processing to achieve a response time much faster. In the following sections, each relay module is presented and discussed in detail the hardware design is presented.

2.3 DFT Module with DC Offset Removal

Among the existing filtering algorithms [2, 16-20] for basic extraction in digital relays, DFT is to improve safety harmonic one of the most popular methods is to obtain values. However, the DC offset transient fault signals can affect an accurate estimate of the phasor DFT. As a result, relay transmission lines tend to mal operate by area or by reaching the set value. Therefore, the DC offset component is removed. Here algorithm forward by [18] was adopted as it only requires one cycle to finish, plus two full-cycle DFT (FC DFT) calculations with DC offset removal. Additional

effects of the calculation according to the two samples can be offset with low latency FPGA hardware modules.

2.4 Briefly Survey of CORDIC Algorithms

The CORDIC Algorithm (Coordinate Rotation Digital Computer) is an efficient iterative algorithm, by means of which can be implemented many features such. As trigonometric functions, exponential and logarithms as well as the simple multiplication or division.

2.5 Motivation

In computer technology, especially in the digital signal processing, you need fast method for the calculation of, for example Trigonometric functions, Conventional series expansions. As the Taylor series often show only mediocre (ie slow, or even dependent on the arguments) convergence and poor numerical stability. A series development also mainly consists of a sum of products which are hard to calculate.

2.6 Historical Development

The CORDIC algorithm was presented in 1959 by Jack E. Volder. In the original version, it was thus possible trigonometric functions such as sine, cosine and tangent and the multiplication and division of numbers solely by the in digital circuits easily realizable additions and shift operations (eng. Shift-and-add operations) to form. Shift operations to the number base 2 are in digital circuits very easily realized by corresponding interconnection.

Volders motivation was the replacement of conventional and error-prone analog navigation computer in Convair B-58 bombers by digital computer for accurate positioning. The request was the position calculation of flying at supersonic speed bomber in real time via a simplified form as surface spherical adopted.

Mid-1960s, the CORDIC algorithm has also been used in civilian applications. Forerunner of today's calculators as the desktop computer 9100 by Hewlett-Packard in 1968 put him to calculate the trigonometric functions.

Until 1971, however, the CORDIC algorithm by JS Walther on the today usual form was expanded and therefore also possible to efficiently calculate logarithms, the exponential function and the square root in digital circuits.

2.7 Application Examples

CORDIC algorithms are used to calculate the main elementary functions in micro-computing devices such as pocket calculators. So can also be found in x87 arithmetic coprocessors Intel the CORDIC algorithm to compute mathematical operations. Further application examples are in the message transfer. For example, can be efficiently magnitude and phase of a complex signal determine.

Since multiply are extensive and thus expensive to implement, especially in digital circuits, CORDIC is often used exactly where multipliers are not efficient available. This includes especially the field of digital circuit techniques such as FPGA or ASIC.

Although CORDIC is not the fastest algorithm but its simplicity and versatility used.

Digital Schedule CORDIC is shown in figure 2.1.

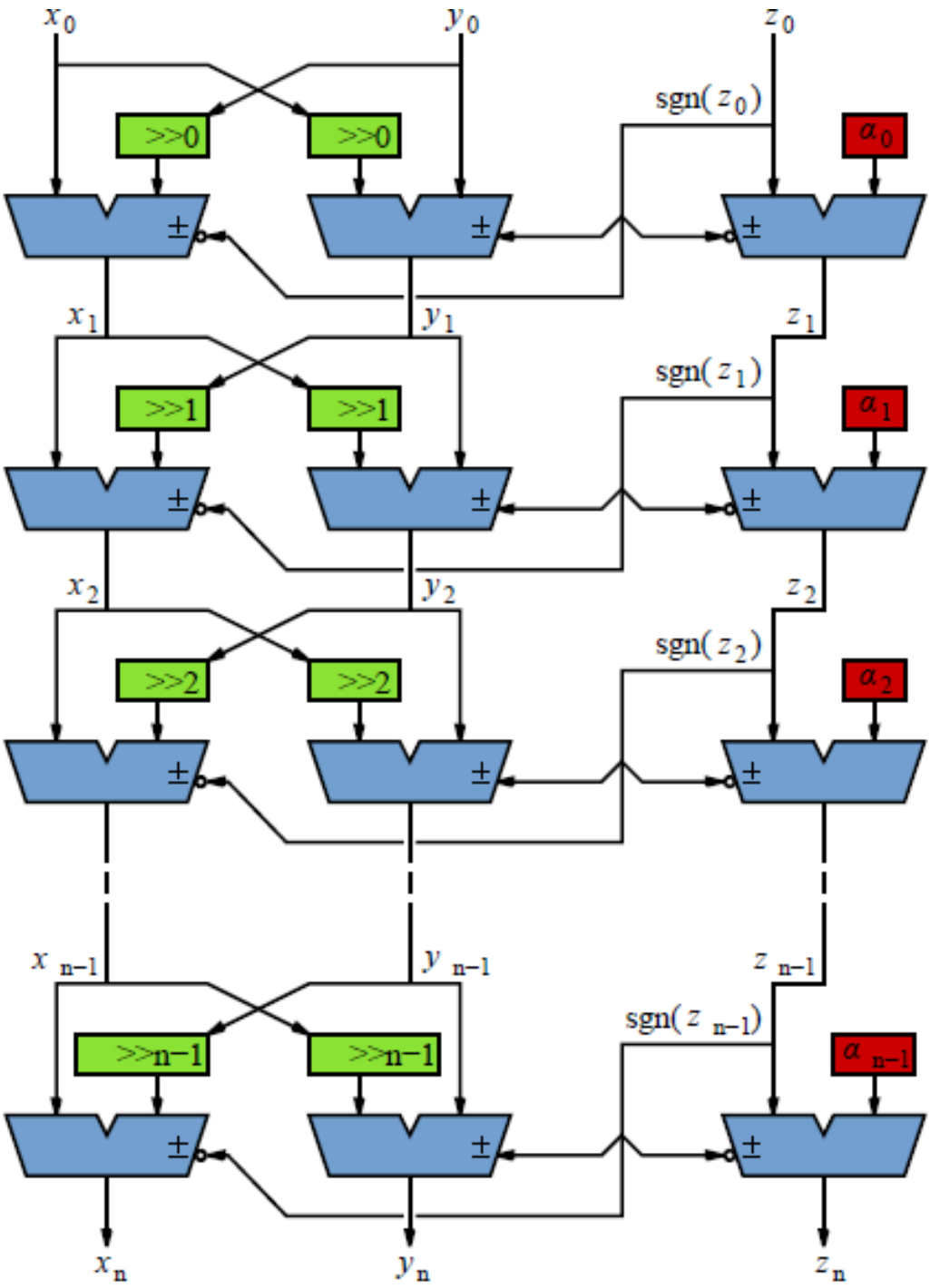


Figure 2.1: Digital schedule CORDIC.

CHAPTER THREE

METHODOLOGY OF THIS THESIS

3.1 Methodology

Figure 3.1 shows the functional block diagram of the protection scheme of three phase transmission power system.

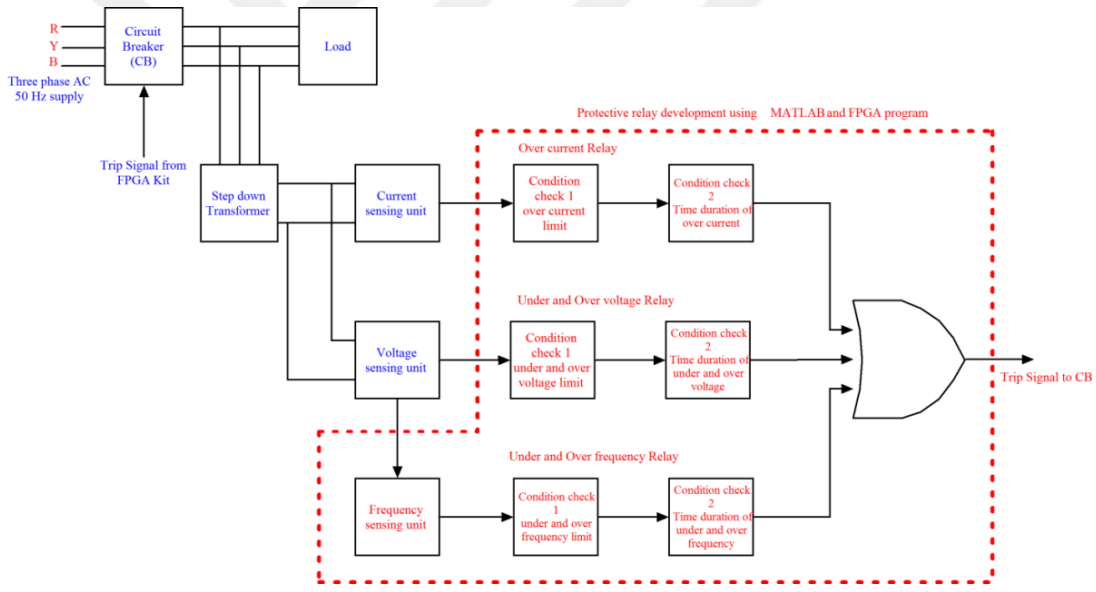


Figure 3.1: Functional block diagram of the protection scheme of three phase transmission power system.

3.2 Calculation of Rated Voltage and Rated Current

3.2.1 Sending End

Peak voltage of the single phase : $338\ V_{peak}$

RMS value of system : $\frac{338}{\sqrt{2}} = 239\ Volt$

3.2.2 Receiving End

Peak voltage of the single phase : 295 V_{peak}

RMS value of system : $\frac{295}{\sqrt{2}} = 206\ Volt$

Current of the load : 4.12 $Amps$

3.3 Settings of Maximum and Minimum Limit of Voltage, Current and Frequency of the Relay

Sending End Voltage limit:

Maximum Voltage : 105 % of the RMS value

: $\frac{105}{100} \times 239 = 250.95\ Volts$

Minimum Voltage : 95 % of the RMS value

: $\frac{95}{100} \times 239 = 227.05\ Volts$

Sending End Frequency Limit:

Maximum frequency : 106 % of the rated value

: $\frac{106}{100} \times 50 = 53\ Hz$

Minimum Frequency : 92 % of the rated value

: $\frac{92}{100} \times 50 = 46\ Hz$

Receiving End Current Limit : 5 $Amps$

Timer settings : 5 Sec

3.4 Design of Over Current Relay

Basic idea behind the over current relay is, if actual current exceed predefined value for particular time span then trip signal is given to the circuit breaker for isolation of the system. Figure 3.2 shows the flowchart for the over current relay.

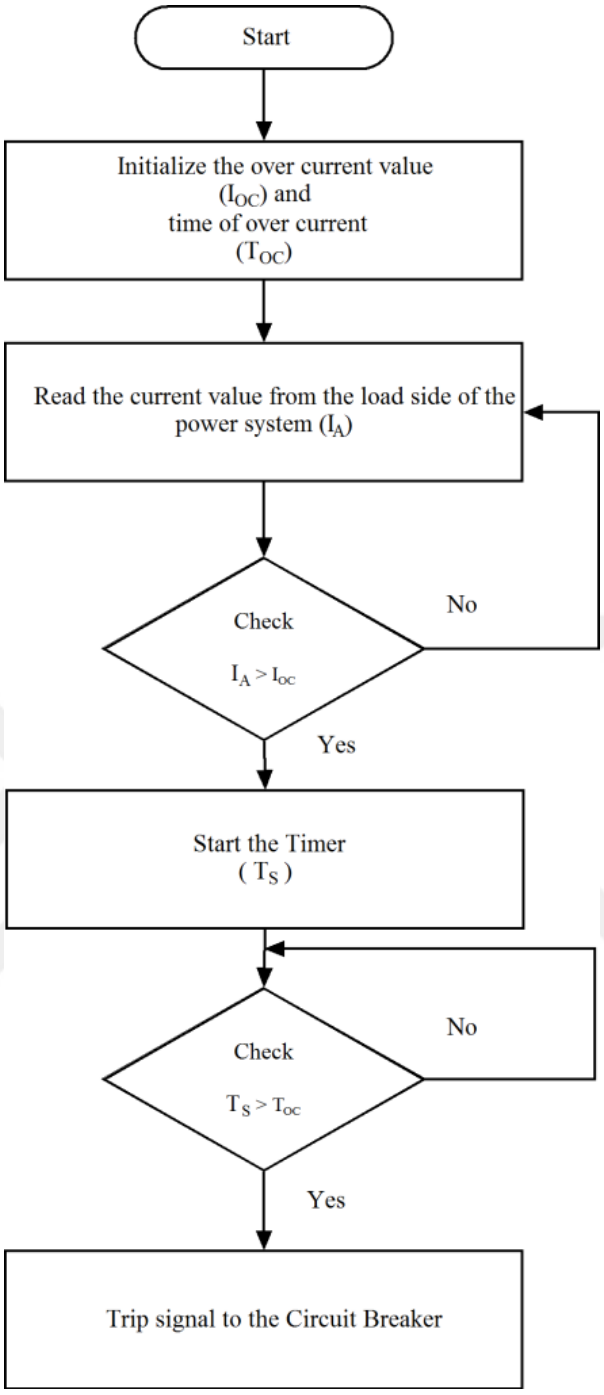


Figure 3.2: Flowchart for the over current relay.

3.4.1 Algorithm

1. Initialize the over current value (I_{OC} = 5 Amps) and time of over current (T_{OC}=5sec).
2. Read the value of actual current (I_A) from load side of the transmitted power system.

3. Check the current limit: If $I_A > I_{OC}$ go to next step otherwise go to previous step.
4. Start the timer (T_S) or counter for counting the seconds.
5. Check the Time limit: If $T_S > T_{OC}$ go to next step otherwise counting the seconds.
6. Send the trip signal to the circuit breaker for isolation of the power system.

3.4.2 Algorithm for Over Current Relay (Definite Time Over Current Relay)

a) Set the rated current of the power system and taken as a reference or threshold for over current Iref.
b) Measure the current of load I. This is equal to the rms value of the load current.
c) Find out the ratio of the absolute value for (I / Iref) or compare the rms value of load current (I) with reference current (I_{ref}).
d) This ratio absolute value of (I / Iref) is called the Plug Setting Multiplier (PSM).
e) The value of Plug Setting Multiplier indicates the rigorousness of the fault as seen by the relay.
f) Define definite time for tripping (minimum time duration of fault or over load). This algorithm follow the definite over current relay function and it always constant for all type of fault and over loading.
g) Trip the circuit breaker, if Plug Setting Multiplier is greater than threshold and time duration of fault is greater than definite time. (The PSM must be greater than 1).

This design need only following operation:

1. Reference current value setting
2. Measurement of load current
3. Comparisons of currents (I_{ref} and I)
4. Setting of definite time
5. For checking rigorousness of the fault, here just used "if then logic"

3.5 Design of Over and Under Voltage Relay

Basic idea behind the over and under voltage relay is, if actual voltage exceed predefined value (maximum and minimum voltage) for particular time span then trip signal is given to the circuit breaker for isolation of the system. Figure 3.3 shows the flowchart for the over and under voltage relay.

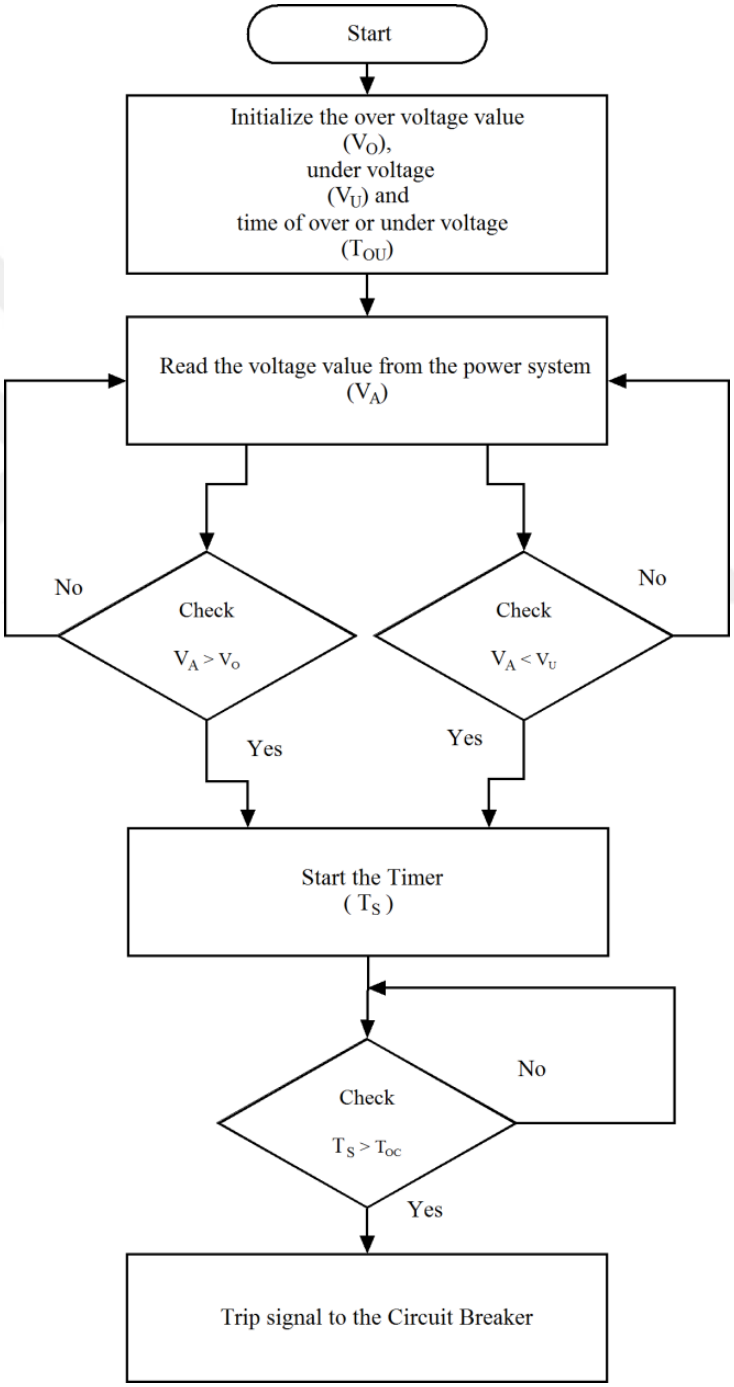


Figure 3.3: Flowchart for the over and under voltage relay.

3.5.1 Algorithm

1. Initialize the over voltage (V_O = 250.95 volts) and under voltage (V_U = 227.005 volts) value and time of over and under voltage (T_{OU}=5sec).
2. Read the value of actual voltage (V_A) from the source of the transmission power system.
3. Check the voltage limit: If $V_U > V_A > V_O$ go to next step otherwise go to previous step.
4. Start the timer (T_S) or counter for counting the seconds.
5. Check the Time limit: If $T_S > T_{OU}$ go to next step otherwise counting the seconds.

Send the trip signal to the circuit breaker for isolation of the power system.

3.6 Design of Over and Under Frequency Relay

Basic idea behind the over and under frequency relay is, if actual frequency exceed predefined value (maximum and minimum frequency) for particular time span then trip signal is given to the circuit breaker for isolation of the system. Figure 3.4 shows the flowchart for the over and under frequency relay.

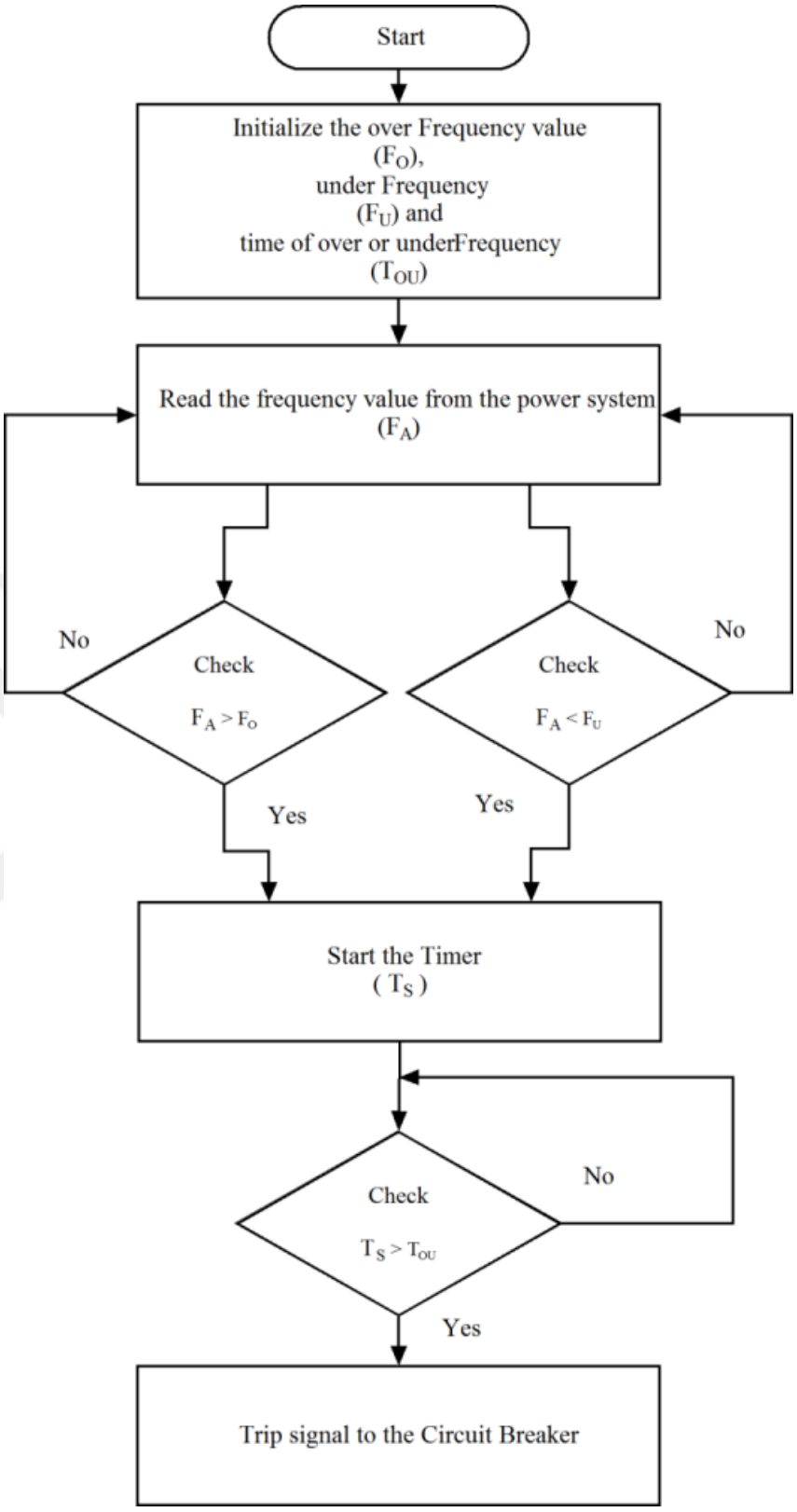


Figure 3.4: Flowchart for the over and under frequency relay.

3.6.1 Algorithm

1. Initialize the over frequency (F_O = 53 Hz) and under frequency (F_U = 46 Hz) value and time of over and under frequency (T_{OU}= 5 sec).
2. Read the value of actual frequency (F_A) from the source of the transmission power system.
3. Check the frequency limit: If $F_U > F_A > F_O$ go to next step otherwise go to previous step.
4. Start the timer (T_S) or counter for counting the seconds.
5. Check the Time limit: If $T_S > T_{OU}$ go to next step otherwise counting the seconds.

Send the trip signal to the circuit breaker for isolation of the power system.

3.6.2 Details of Power System

The parameter of the power system is shown in table 3.1.

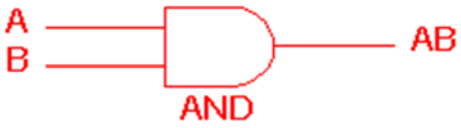
Table 3.1: Parameter of the power system.

Parameter	Value	Unit
The operating voltage	415	V
The operating frequency	50	Hz
The distance of transmission line	100	km
The resistance per unit length	0.01273	ohms/Km
The inductance per unit length	0.9337e-3	H/Km
The capacitance per unit length	12.74e-9	F/Km
Rated load	3500	W

3.7 Digital Logic

Digital systems are said to be constructed by using logic gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the aid of truth tables.

3.7.1 AND Gate



2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

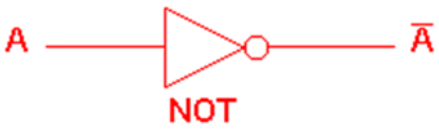
The AND gate is an electronic circuit that gives a **high** output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB

3.7.2 OR Gate

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

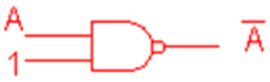
The OR gate is an electronic circuit that gives a high output (1) if **one or more** of its inputs are high. A plus (+) is used to show the OR operation.

3.7.3 NOT Gate



NOT gate	
A	$\overline{A}$
0	1
1	0

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an *inverter*. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs. The diagrams below show two ways that the NAND logic gate can be configured to produce a NOT gate. It can also be done using NOR logic gates in the same way.



3.7.4 NAND Gate

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

3.7.5 NOR Gate

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high.

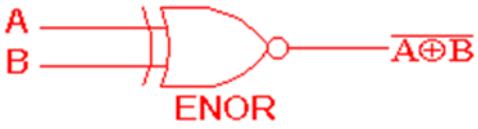
The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

3.7.6 EXOR Gate

2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

The '**Exclusive-OR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. An encircled plus sign (⊕) is used to show the EOR operation.

3.7.7 EXNOR Gate



2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

The '**Exclusive-NOR**' gate circuit does the opposite to the EOR gate. It will give a low output if **either, but not both**, of its two inputs are high. The symbol is an EXOR gate with a small circle on the output. The small circle represents inversion.

The NAND and NOR gates are called *universal functions* since with either one the AND and OR functions and NOT can be generated.

Note:

A function in *sum of products* form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates.

A function in *product of sums* form can be implemented using NOR gates by replacing all AND and OR gates by NOR gates.

Table 3.2: Logic gate symbols.

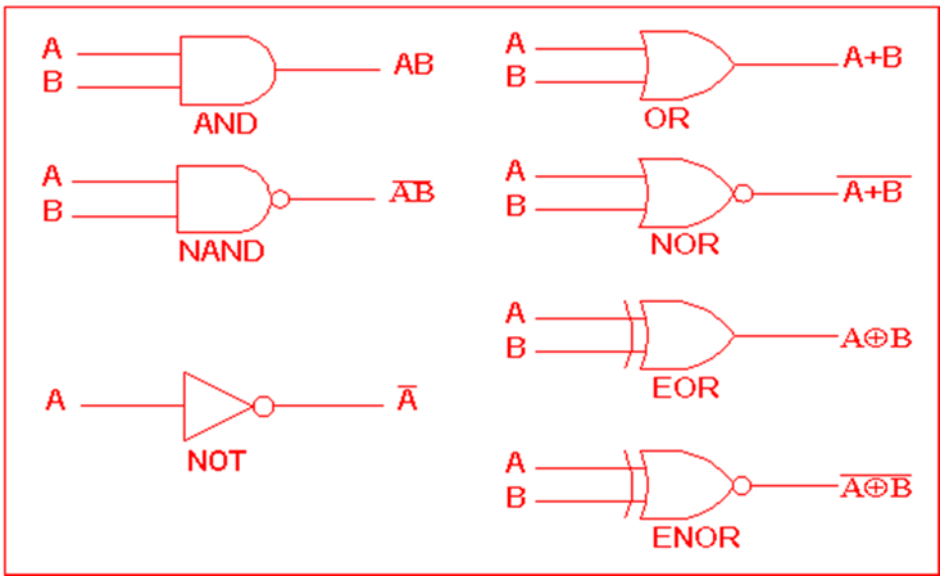


Table 2 is a summary truth table of the input/output combinations for the NOT gate together with all possible input/output combinations for the other gate functions. Also note that a truth table with 'n' inputs has 2^n rows. You can compare the outputs of different gates.

Table 3.3: Logic gates representation using the Truth table.

NOT gate	
A	$\overline{A}$
0	1
1	0

INPUTS		OUTPUTS					
A	B	AND	NAND	OR	NOR	EXOR	EXNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

CHAPTER FOUR

IMPLEMENTATION

4.1 Simulink Model of Overall Power System with Protective Relay

Figure 4.1 shows the overall simulink model of the power system with protective relay. function of the each simulink block is explined in the proceeding section.

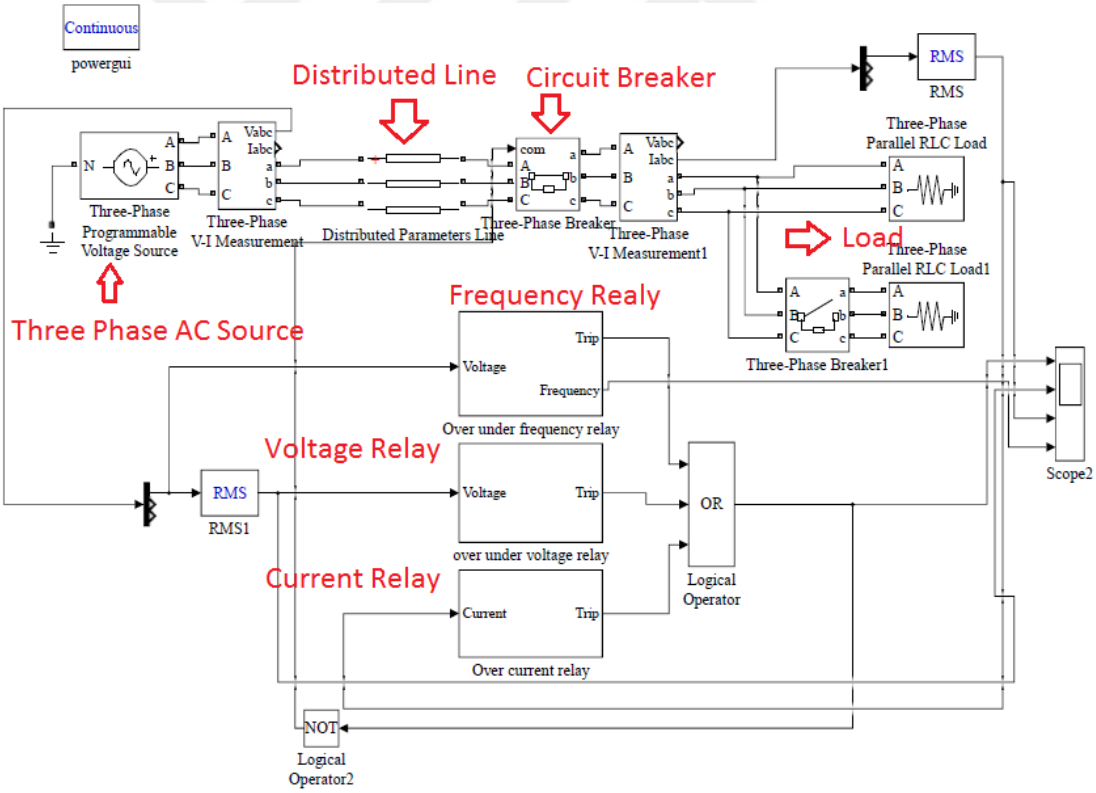
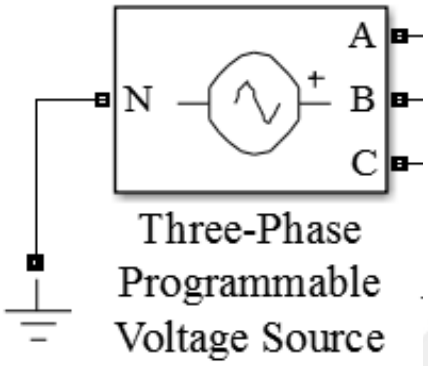


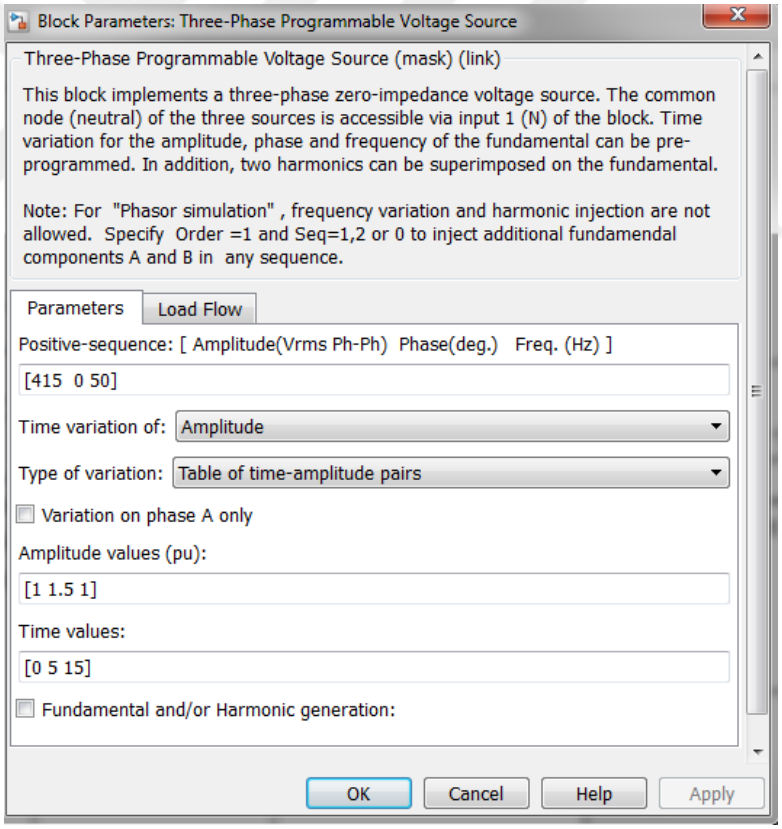
Figure 4.1: Simulink model of the overall power system with protective relay.

4.1.1 Three Phase AC Source

The Simulink Model of Three Phase AC source, Input Parameter for the Three Phase AC source and Load flow parameter for the Three Phase AC source is shown in figure 4.2.

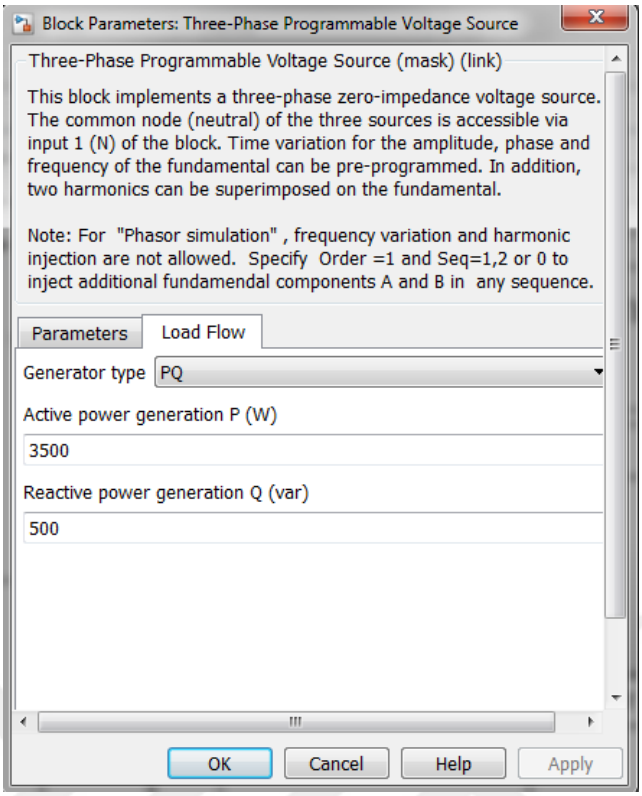


(a)

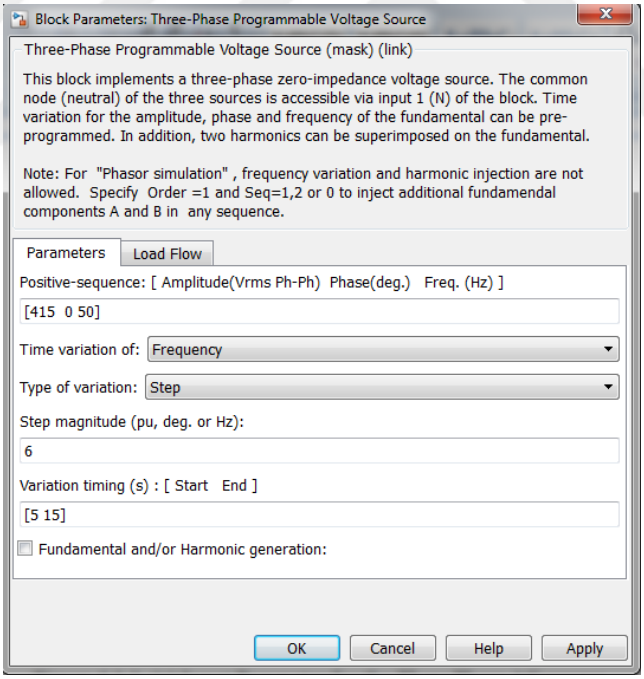


(b)

Figure 4.2: a) Simulink model of three phase AC source, b) Input parameter for the three phase AC source, c) Load flow parameter for the three phase AC source, d) Load flow parameter for the three phase AC source.



(c)



(d)

Figure 4.2 (continuation): a) Simulink model of three phase AC source, b) Input parameter for the three phase AC source, c) Load flow parameter for the three phase AC source, d) Load flow parameter for the three phase AC source.

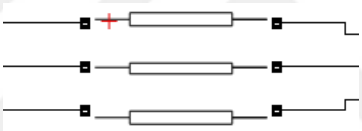
Figure 4.2 shows the simulink model and parameter of the three phase AC source. phase to phase voltage of the system is 415 Volts and frequency of the

system is 50 Hz. from the Figure 4.2 (b), the amplitude of the source is 1 pu from 0 to 5 sec. the amplitude of the source is 1.5 pu from 5 to 15 sec then it is changed to 1 pu. this function is used to create over voltage conditions in the system. the same concept could be applied for under voltage conditions in the system i.e., the amplitude of the source is 1 pu from 0 to 5 sec. the amplitude of the source is 0.5 pu from 5 to 15 sec then it is changed to 1 pu.

From the Figure 4.2 (d), frequency of the source is varied from 50 Hz to 56 Hz from 5 sec to 15 sec. this function is used for over frequency conditions in the power system. the same concept could be applied for under frequency conditions in the power system i.e., 50 Hz to 44 Hz from 5 sec to 15 sec.

4.1.2 Three Transmission Line Parameter

The Simulink Model of Transmission Line and Input Parameter for the Transmission Line is shown in figure 4.3.



(a)

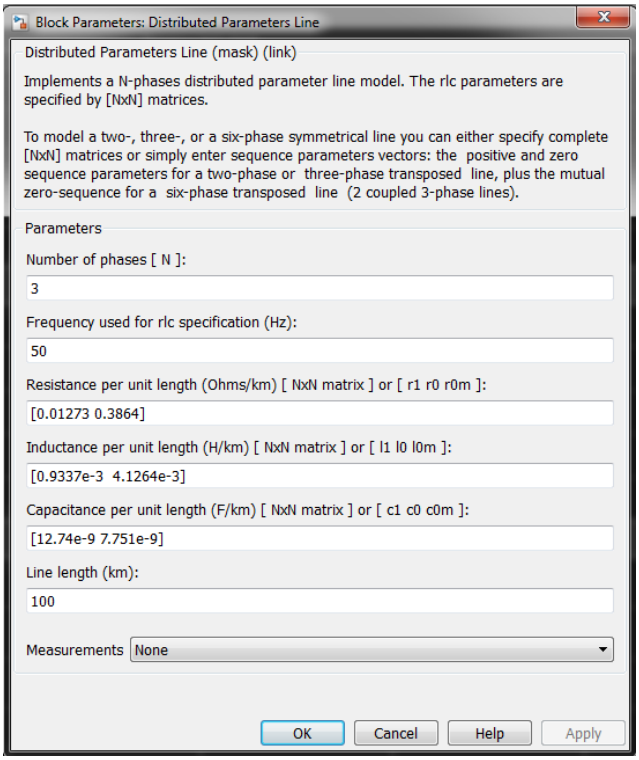
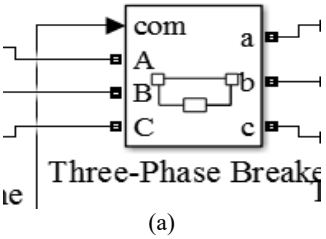


Figure 4.3: a) Simulink model of transmission line, b) Input parameter for the transmission line.

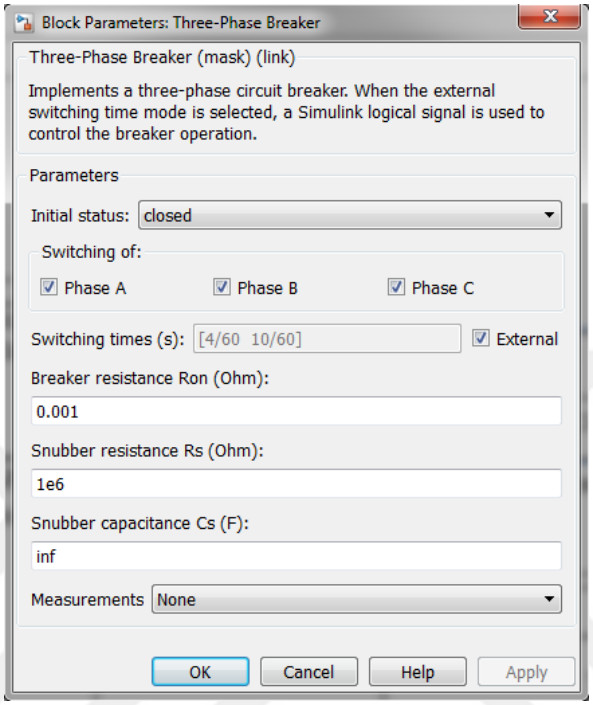
Figure 4.3 shows the simulink model and parameter of the transmission line. number of phase is equal to the three, frequency of the transmission line is 50 Hz, resistance per unit length is 0.01273 ohms/Km, inductance per unit length is 0.9337 x 10^{-3} H/Km, capacitance per unit length is 12.74 x 10^{-9} F/Km and length of the line is 100 Km.

4.1.3 Three Phase Circuit Breaker

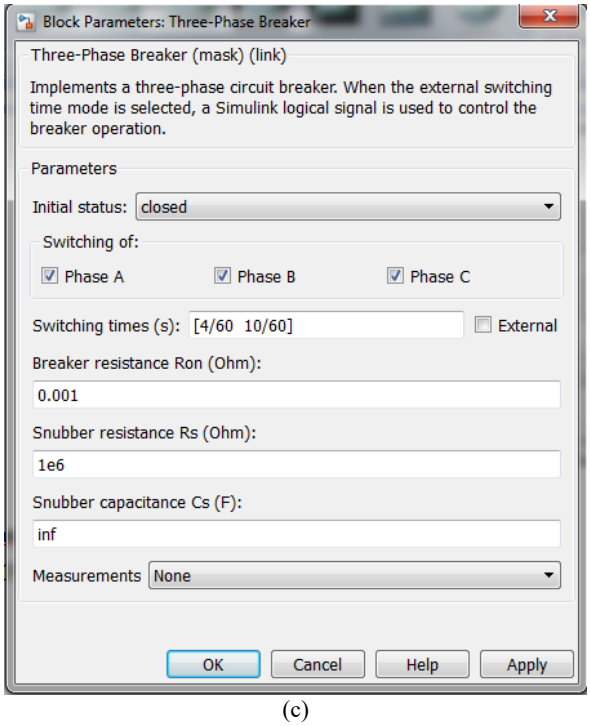
Figure 4.4 shows the simulink model of three phase circuit breaker. This circuit breaker can be configure into two operating mode, one is external controlling mode and internal controlling mode. In external controlling mode, circuit breaker can be opened or closed depending upon the external parameter variations. In internal controlling mode, circuit breaker can be opened and closed for particular time period which can be decided by the users. In our thesis, external controlling mode operation is used. Circuit breaker can be opened or closed by the trip signal comes from the protective relay.



(a)



(b)

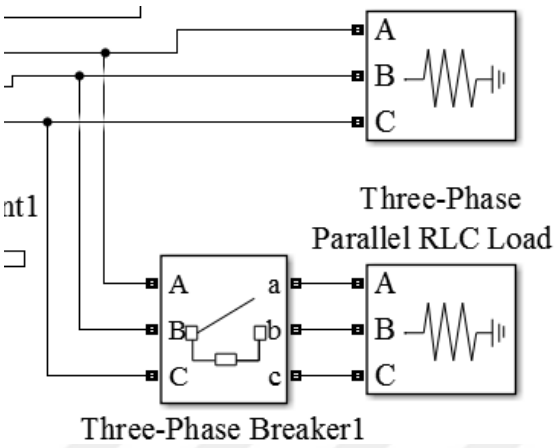


(c)

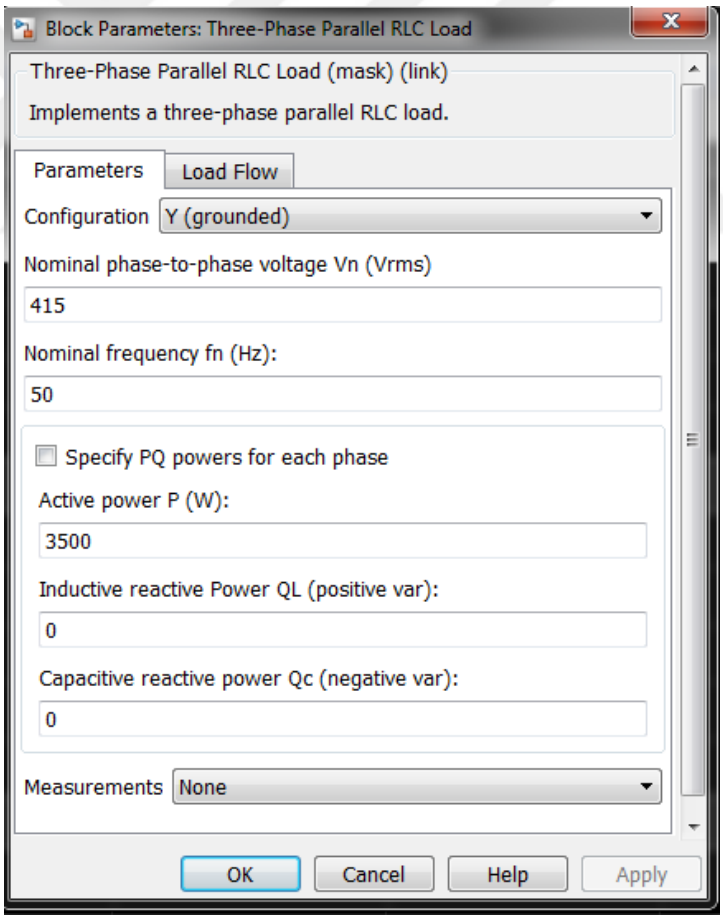
Figure 4.4: a) Simulink Model of three phase circuit breaker, (b) parameter of three phase circuit breaker in external controlling mode, (c) Parameter of three phase circuit breaker in internal controlling mode.

4.1.4 Three Phase Load Disturbance Model

The Simulink Model of three phase Load disturbance model is shown in figure 4.5.

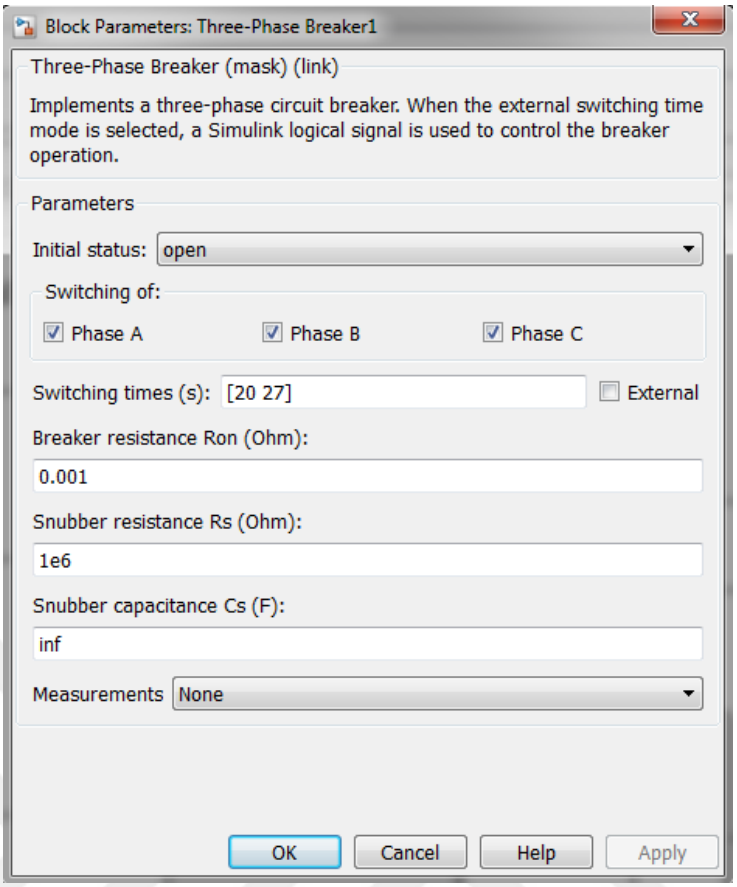


(a)



(b)

Figure 4.5: (a) Simulink Model of three phase Load disturbance model, (b) Parameter of the three phase Load, (c) Parameter of the three phase circuit breaker.



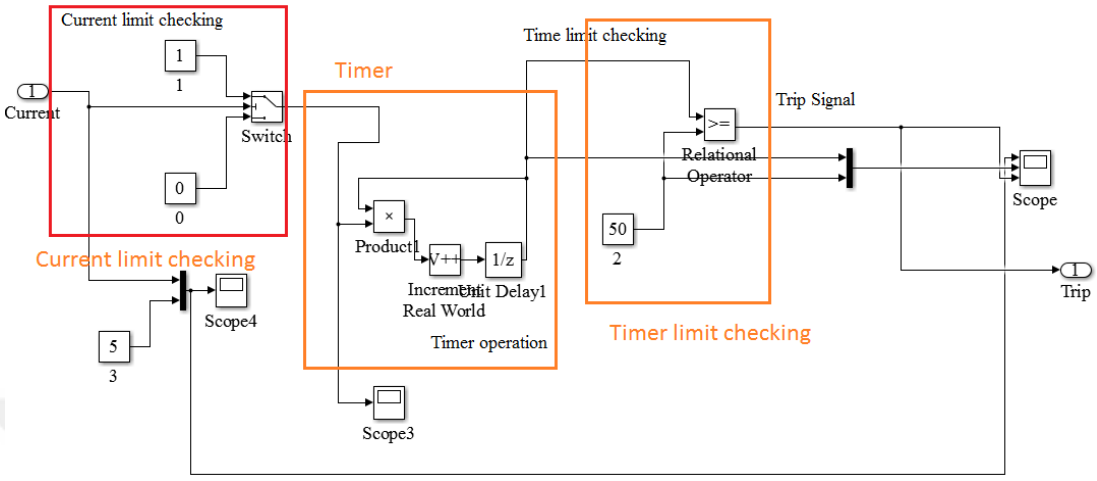
(c)

Figure 4.5 (continuation): (a) Simulink Model of three phase Load disturbance model, (b) Parameter of the three phase Load, (c) Parameter of the three phase circuit breaker.

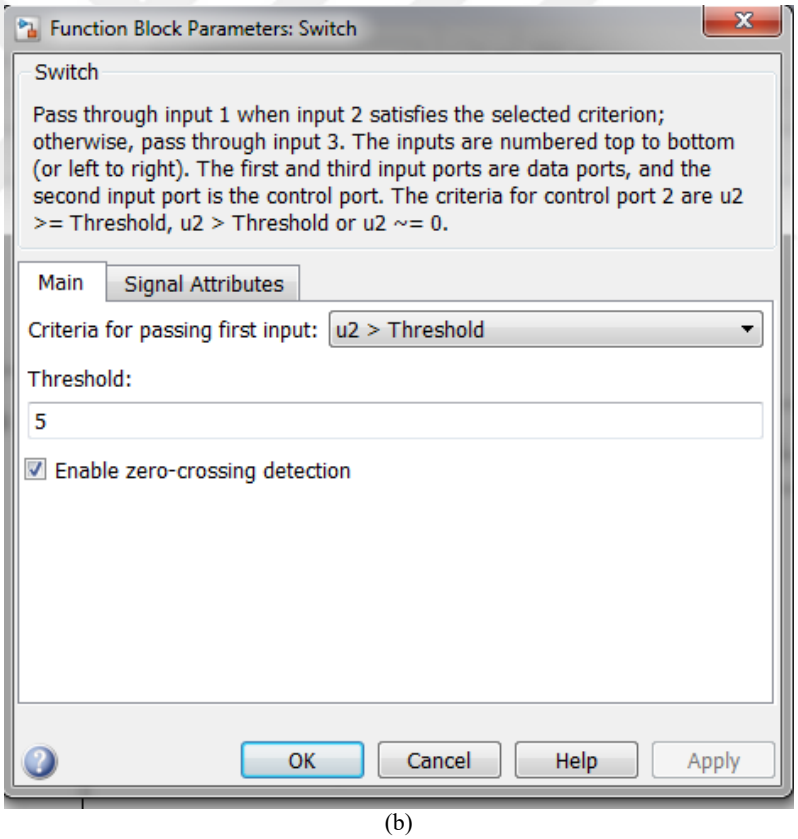
Figure 4.5 shows the simulink model and parameter of the three phase load disturbance model. Nominal RMS value of the load is 415V, frequency of the load is 50Hz and rated real power of the load is 3500 watts. Three phase circuit breaker (Figure 4.5 (c)) is used for switch the load (2000 watts) for particular time period from 20 sec to 27 sec (in this period, the total load is 5500 watts). This function is used for creation of over current conditions in the power system.

4.1.5 Over Current Relay

Figure 4.6 shows the simulink model of the over current relay.



(a)



(b)

Figure 4.6: a) Simulink model of the over current relay, b) Parameter of the Switch block in the current limit checker.

Figure 4.6 (b) shows the parameter of the switch block of the current limit checker. Switch block has three inputs, first and third inputs are used to denote the over current status of the input current. Second input is used to check the over current status. If U2 > threshold (5) then "1" is allowed to the output (over current event occurred) otherwise "0" is allowed to the output (Normal operation).

The output of the switch block is multiplied with timer output. If over current event is occurs then timer is going to start counting the seconds step by step with 0.1 sec interval otherwise the output of the timer is zero. Simultaneously, the output of the timer is compared with predefined time limit (50 means 5 sec in this case). If output reached predefined value then trip signal is send to the circuit breaker for isolation of the system.

4.1.6 Over Voltage and Under Voltage Relay

Figure 4.7 shows the simulink model of the over voltage and under voltage relay.

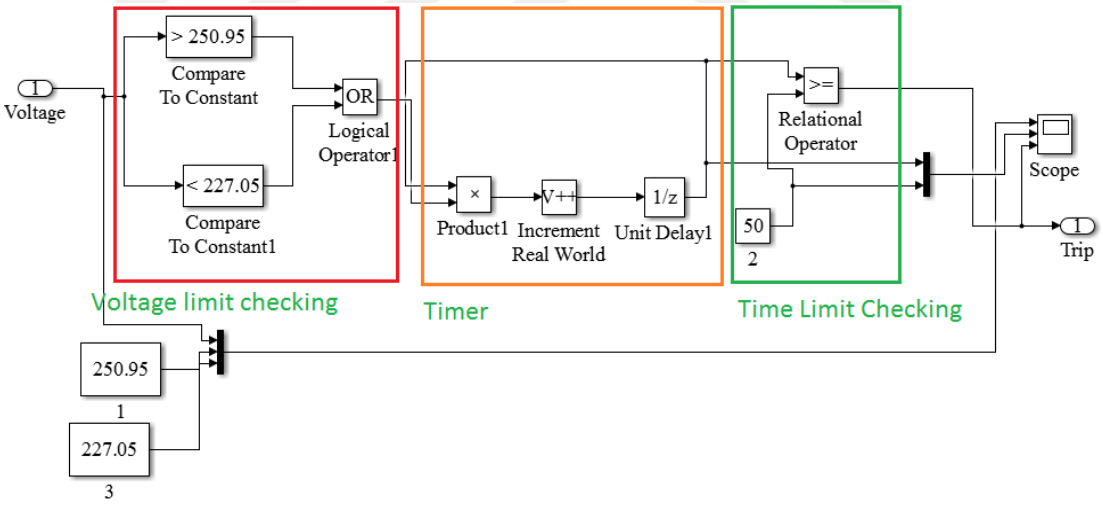


Figure 4.7: Simulink model of the over voltage and under voltage relay.

In this relay, actual voltage of the source is compared with maximum (250.95 volts) and minimum (227.05 volts) predefined value of voltage limit, and the output of the two comparator is given to OR gate. If actual voltage is greater than or less than maximum or minimum value then output of the OR gate is "1" otherwise the output is "0". The output of the OR gate is multiplied with timer then timer output is

compared with predefined time limit (50 means 5 sec). If timer value is reached predefined time value then trip signal is send to the circuit breaker for isolation of the power system.

4.1.7 Over Frequency and Under Frequency Relay

Figure 4.8 shows the simulink model of the over frequency and under frequency relay.

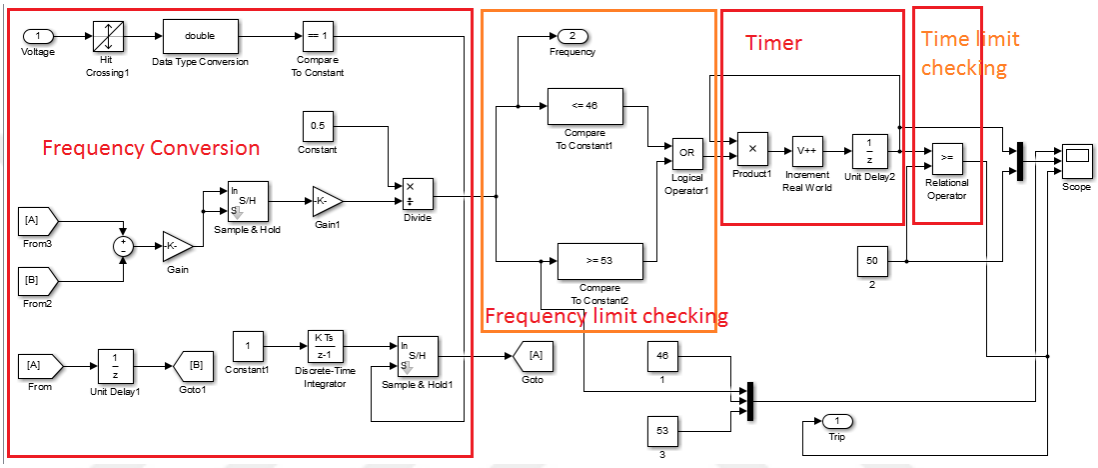


Figure 4.8: Simulink model of the over frequency and under frequency relay.

In this relay, actual frequency of the source is compared with maximum (53 Hz) and minimum (46 Hz) predefined value of frequency limit, and the output of the these two comparator is given to OR gate. If actual frequency is greater than or less than maximum or minimum value then output of the OR gate is "1" otherwise the output is "0". The output of the OR gate is multiplied with timer then timer output is compared with predefined time limit (50 means 5 sec). If timer value is reached predefined time value then trip signal is send to the circuit breaker for isolation of the power system.

4.2 Simulation Result of Over Current Relay

Figure 4.9 shows the simulation result for over current relay. Initially, load is maintained at 3500 watts and current through the load is 4 Amps. At 5 sec, 2000 watts load is added to the power system and load current is increased to 5.5 Amps. At this instant, load current exceed the predefined current value (5 Amps). At the same instant, timer is going to start the counting the seconds at 0.1 sec interval. timer output reach the time limit at 10 sec, relay give the trip signal to the circuit breaker and load is disconnected from the power system and load current goes to zero at 10 sec.

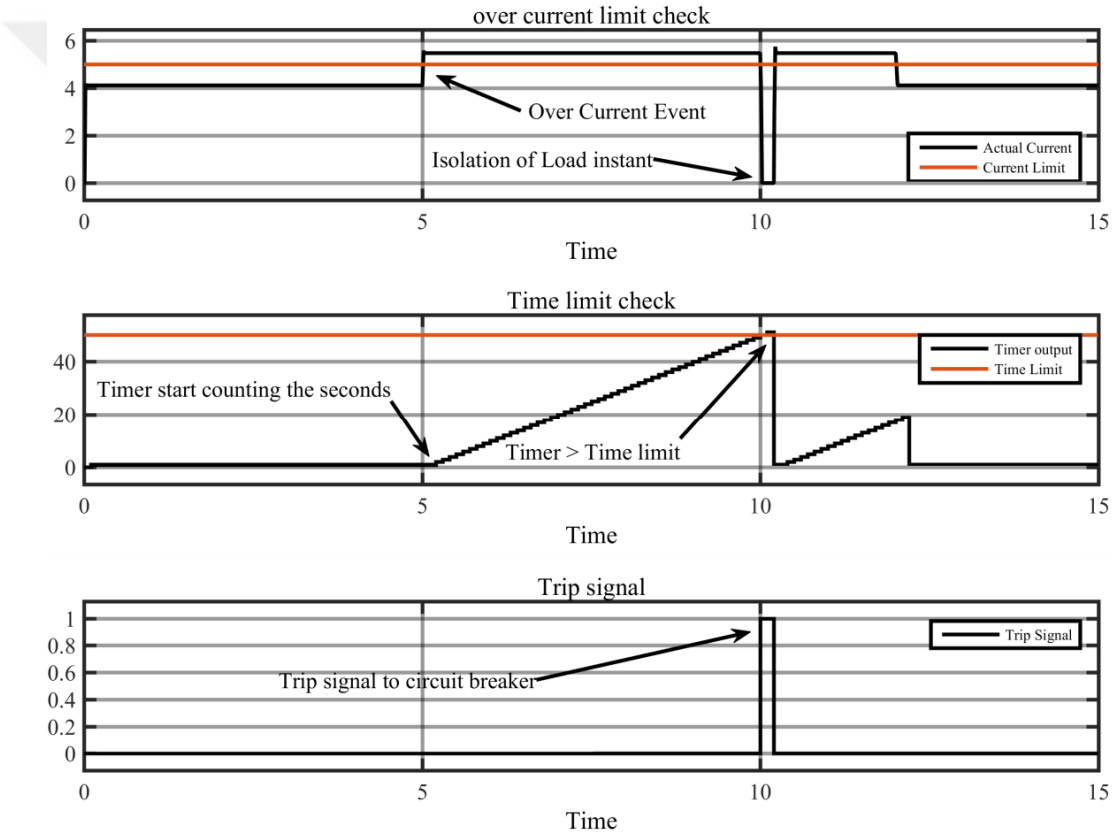


Figure 4.9: Simulation result of over current relay.

In this figure all times are in second unit.

4.3 Simulation Result of Over Voltage Relay

Figure 4.10 shows the simulation result of over voltage relay. Initially, source voltage maintained at 239 volts. At time of 5 sec, source voltage is increased to 280 volts (exceed the maximum limit- 255 volts) simultaneously timer start counting the seconds with 0.1 sec interval. At 10 sec, timer output exceed the time limit. Same time, relay give the trip signal to the circuit breaker and load is disconnected from the supply.

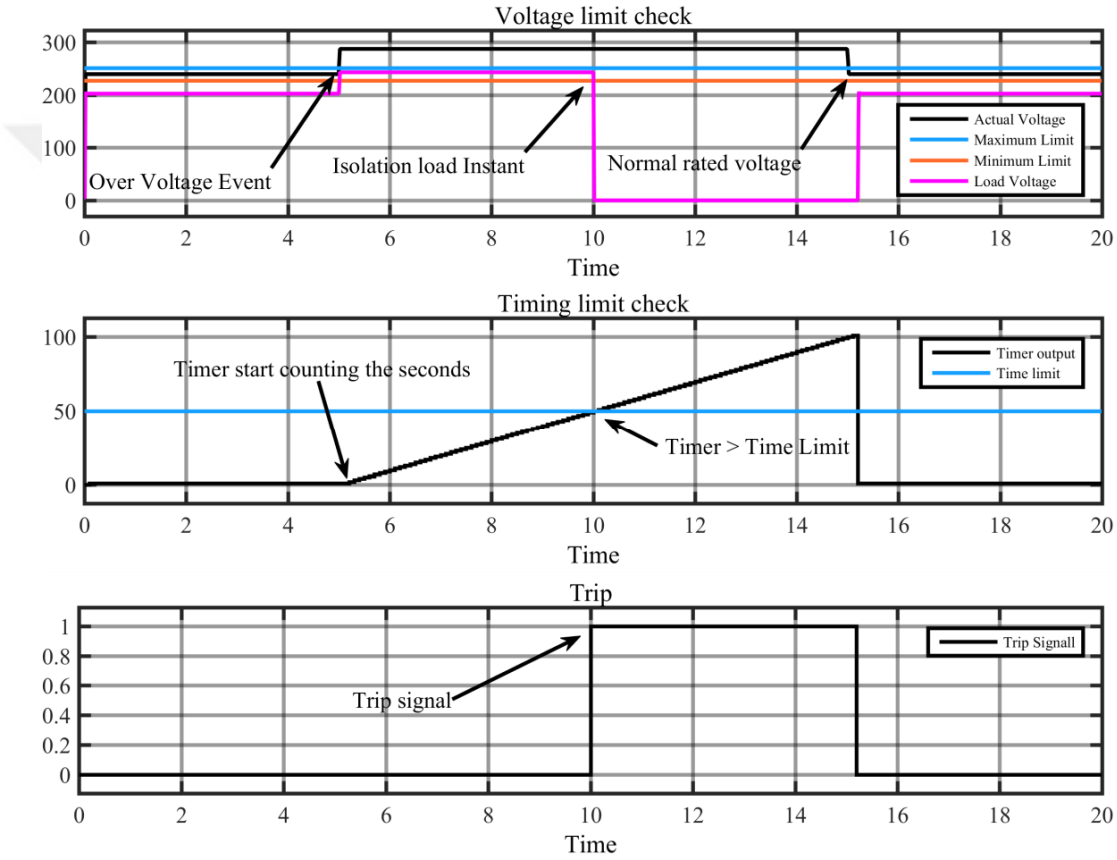


Figure 4.10: Simulation result of over voltage relay.

4.4 Simulation Result of Under Voltage Relay

Figure 4.11 shows the simulation result of under voltage relay. Initially, source voltage maintained at 239 volts. At time of 5 sec, source voltage is decreased to 200 volts (go below the minimum limit- 227 volts) simultaneously timer start counting the seconds with 0.1 sec interval. At 10 sec, timer output exceed the time limit. Same time, relay give the trip signal to the circuit breaker and load is disconnected from the supply.

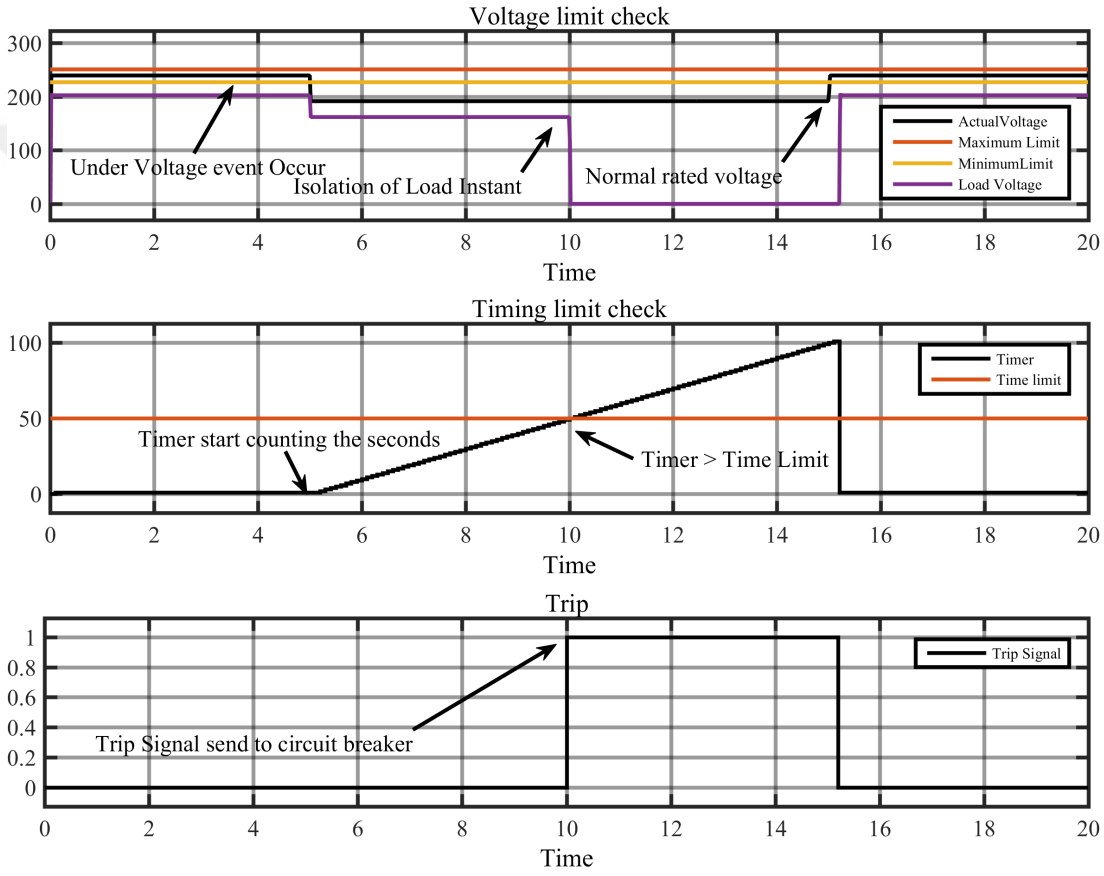


Figure 4.11: Simulation result of under voltage relay.

4.5 Simulation Result of Over Frequency Relay

Figure 4.12 shows the simulation result of over frequency relay. Initially, source frequency maintained at 50 Hz. at time of 5 sec, source frequency is increased to 56 Hz (exceed the maximum limit- 53 Hz) simultaneously timer start counting the seconds with 0.1 sec interval. At 10 sec, timer output exceed the time limit. Same time, relay give the trip signal to the circuit breaker and load is disconnected from the supply.

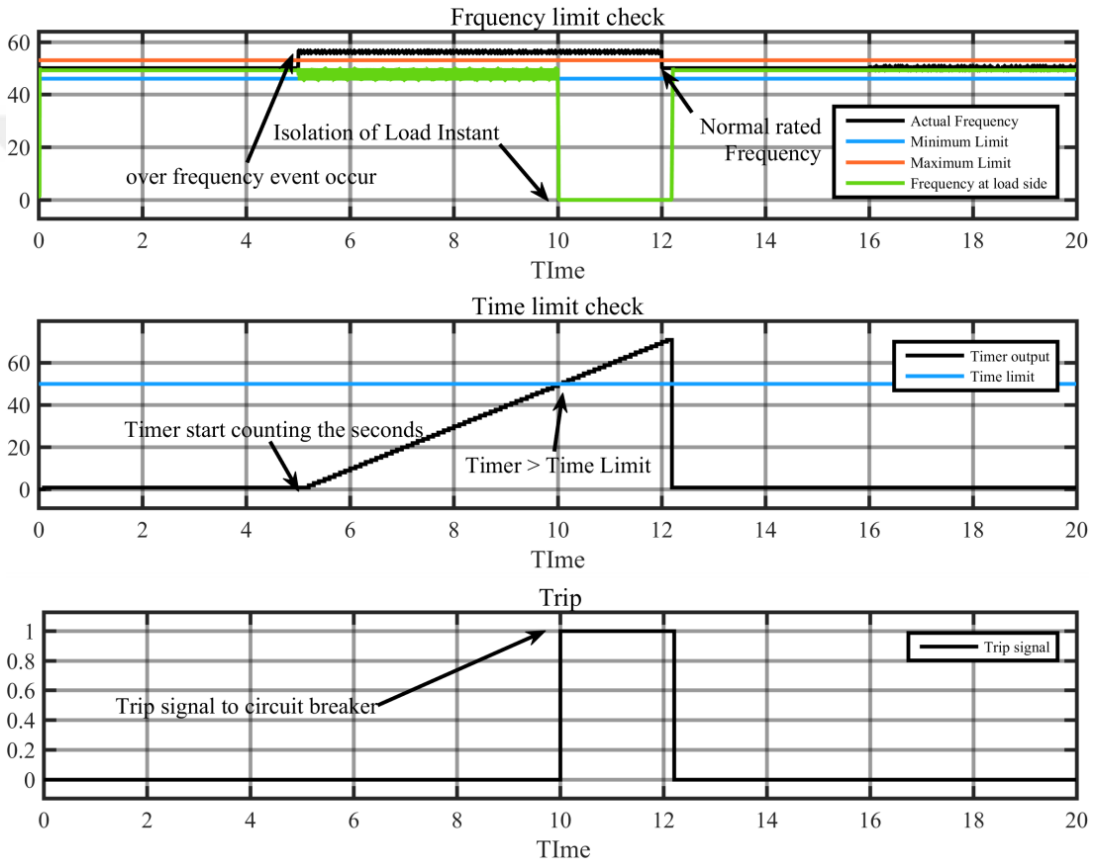


Figure 4.12: Simulation result of over frequency relay.

4.6 Simulation Result of Under Frequency Relay

Figure 4.13 shows the simulation result of under frequency relay. Initially, source frequency maintained at 50 Hz. at time of 5 sec, source frequency is decreased to 44 Hz (go below the minimum limit- 46 Hz) simultaneously timer start counting the seconds with 0.1 sec interval. At 10 sec, timer output exceed the time limit. Same time, relay give the trip signal to the circuit breaker and load is disconnected from the supply.

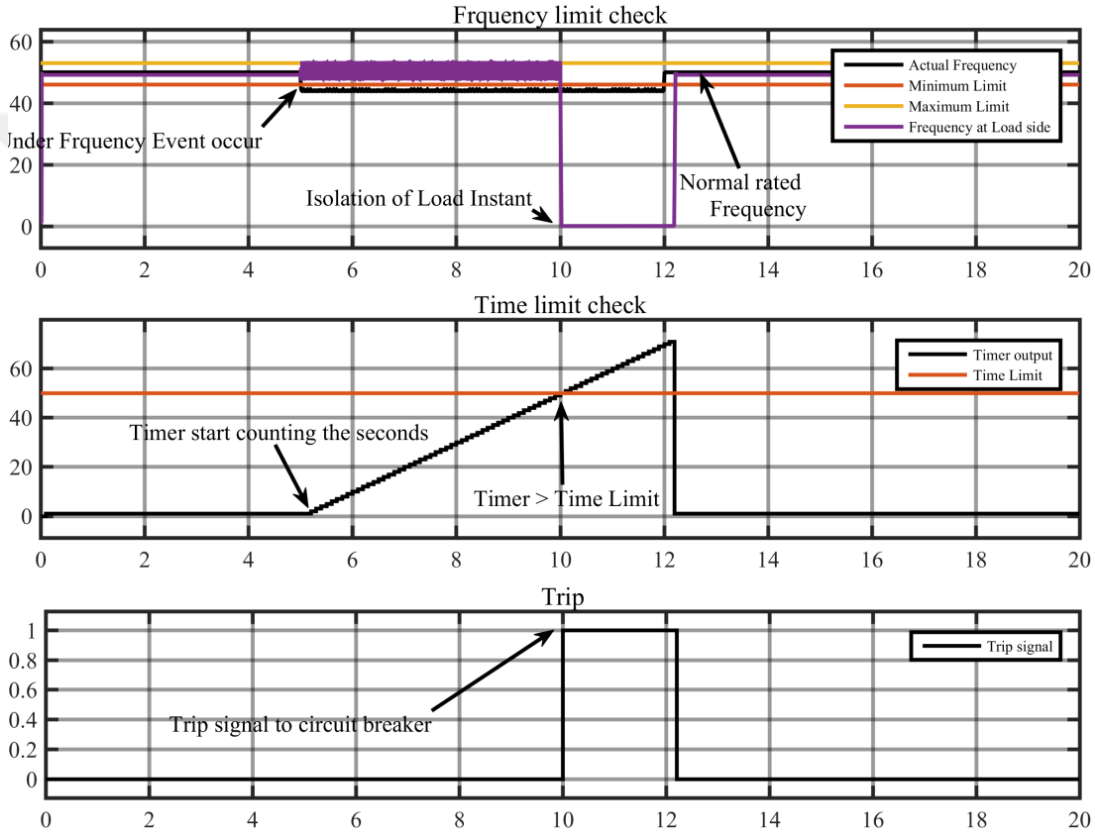


Figure 4.13: Simulation result of under frequency relay.

4.7 Objective

1) To design protective relay for three phase power system such as over current relay, over voltage relay, under voltage relay, over frequency relay and under frequency relay.
2) Simulation of the above relay using MATLAB / Simulink toolbox.
3) HDL code generation and FPGA programming of above relay in the MATLAB Software.
4) Testing and RTL logic of FPGA code generated from MATLAB using Xilinx ISE 9.2i Software.

4.7.1 RTL View of Over Current Relay

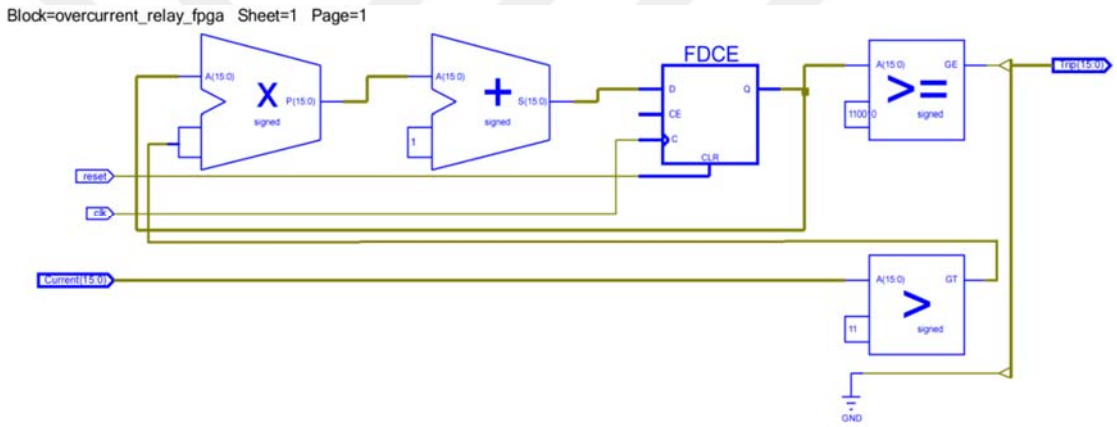


Figure 4.14: RTL View of over current relay.

CHAPTER FIVE

CONCLUSION

5.1 Background

Three phase transmission power system with three different protective schemes such as over current relay, over and under voltage relay and over and under frequency relay are developed using MATLAB / Simulink toolbox. The protective relay are tested for different operating conditions of the transmission power system such over load condition, over and under voltage condition, over and under frequency condition. Each operating, the protective relays are work effectively as seen from the simulation results. Protective relays are explained with simple flowchart. From the logic of the protective relay it can be easily deployed in the FPGA kit for real time environment. We used digital logic algorithm for implementation of protective relay.

5.2 What's New in our Research?

A. This algorithm easy and simple to implement.
B. This algorithm only need comparator and if then logic module for proper function of relay.
C. There is no complex calculation burden in this relay.
D. Response time of the relay is very quick.

5.3 What is the Difference Between Overload Current And Short Circuit?

Overload current is taking place when a device taking continuous over current from the supply source.

Short circuit current is a fault current taking place in the load by earth fault or phase fault.

1. What kind of algorithm used in the design, so why choose?

Algorithm for over current Relay (Definite time over current relay)

A. Set the rated current of the power system and taken as a reference or threshold for over current I_{ref}.
B. Measure the current of load I. This is equal to the rms value of the load current.
C. Find out the ratio of the absolute value for (I / Iref) or compare the rms value of load current (I) with reference current (I_{ref}).
D. This ratio absolute value of (I / Iref) is called the Plug Setting Multiplier (PSM).
E. The value of Plug Setting Multiplier indicates the rigorousness of the fault as seen by the relay.
F. Define definite time for tripping (minimum time duration of fault or over load). This algorithm follow the definite over current relay function and it always constant for all type of fault and over loading.
G. Trip the circuit breaker, if Plug Setting Multiplier is greater than threshold and time duration of fault is greater than definite time. (The threshold must be greater than 1).

This design need only following operation

1) Reference current value setting
2) Measurement of load current
3) Comparisons of currents (I_{ref} and I)
4) Setting of definite time
5) For checking rigorousness of the fault, here just used "if then logic"

This operation can be easily implement in any microprocessor. Digital signal processor and FPGA module.

2. We want information about the algorithm used. (General and mathematically).

Consider rated current of the source is 5 Amps then this the reference current setting for the relay.

Now relay is used for over load protection then find out current of the load and calculation as follows,

Considered rated power of the load is 3000 watts, voltage across the load is 415 volts (RMS) then load current is,

$$P_L = \sqrt{3} V I \cos\phi$$

$$I = \frac{P_L}{\sqrt{3} V \cos\phi}$$

$$I = \frac{3000}{\sqrt{3} \times 415}, \qquad \cos\phi = 1 \ (unity\ power\ factor\ load)$$

$$I = 4.17\ Amps$$

PSM is,

$$PSM = \frac{I}{I_{ref}} = \frac{4.17}{5} = 0.834$$

PSM is less than one and no problem in the power system.

If rated power of the load is increases to 6000 watts, then load current is,

$$I = \frac{6000}{\sqrt{3} \times 415}, \qquad \cos\phi = 1 \ (unity\ power\ factor\ load)$$

$$I = 8.34\ Amps$$

PSM is,

$$PSM = \frac{I}{I_{ref}} = \frac{8.34}{5} = 1.664$$

PSM is greater than one and over current flow through the source as well as load. Then time of over current is compared with definite time of relay (here consider 5 seconds) if time of over current exceed the definite time then trip signal is send to circuit breaker.

3. What's new in our research (by compared)

A. This algorithm easy and simple to implement.

B. This algorithm only need comparator and if then logic module for proper function of relay.

C. There is no complex calculation burden in this relay.

D. Response time of the relay is very quick.

4. What is the job of over current relay? (In last works (papers) about which reason they used the over current relay? And we will use for which reason?)

In the last work (paper), over current relay is used to protect the power system under different fault conditions such as single line to ground fault, double line to ground fault and three phase fault. But in our proposal, the over current relay can be used under different fault conditions as well as in over loaded conditions.

Difference between overload current and short circuit.

Overload current is taking place when a device taking continuous over current from the supply source.

Short circuit current is a fault current taking place in the load by earth fault or phase fault.

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APPENDIX

Appendix-A: FPGA Code and RTL Logic of Over Current Relay

```
-- -------------------------------------------------------------
--
-- Module: overcurrent_relay_fpga
-- Source Path: overcurrent_relay_fpga
-- Hierarchy Level: 0
--
-- -------------------------------------------------------------
LIBRARYIEEE;
USEIEEE.std_logic_1164.ALL;
USEIEEE.numeric_std.ALL;

ENTITYovercurrent_relay_fpgaIS
PORT(clk:INstd_logic;
reset:INstd_logic;
clk_enable:INstd_logic;
Current:INstd_logic_vector(15DOWNTO0);-- int16
ce_out:OUTstd_logic;
Trip:OUTstd_logic_vector(15DOWNTO0)-- int16
);
ENDovercurrent_relay_fpga;


ARCHITECTURErtlOFovercurrent_relay_fpgaIS

-- Signals
SIGNALenb:std_logic;
SIGNALCurrent_signed:signed(15DOWNTO0);-- int16
SIGNALCompare_To_Constant_cmpOut:std_logic;
SIGNALCompare_To_Constant_out1:unsigned(7DOWNTO0);-- uint8
SIGNALUnit_Delay1_out1:signed(15DOWNTO0);-- int16
SIGNALProduct1_cast:signed(8DOWNTO0);-- sfix9
SIGNALProduct1_mul_temp:signed(24DOWNTO0);-- sfix25
SIGNALProduct1_out1:signed(15DOWNTO0);-- int16
SIGNALIncrement_Real_World_out1:signed(15DOWNTO0);-- int16
SIGNALalpha2_out1:signed(15DOWNTO0);-- int16
SIGNALRelational_Operator_relop1:std_logic;
SIGNALData_Type_Conversion_out1:signed(15DOWNTO0);-- int16

BEGIN
Current_signed<=signed(Current);

-- <Root>/Compare To Constant

Compare_To_Constant_cmpOut<='1'WHENCurrent_signed>3ELSE
'0';
```

```
Compare_To_Constant_out1<='0'&'0'&'0'&'0'&'0'&'0'&'0'&Compare_To_Con
stant_cmpOut;

enb<=clk_enable;

-- <Root>/Product1
Product1_cast<=signed(resize(Compare_To_Constant_out1,9));
Product1_mul_temp<=Unit_Delay1_out1*Product1_cast;
Product1_out1<=Product1_mul_temp(15DOWNTO0);

-- <Root>/Increment Real World
Increment_Real_World_out1<=Product1_out1+1;

-- <Root>/Unit Delay1
Unit_Delay1_process:PROCESS(clk,reset)
BEGIN
IFreset='1'THEN
Unit_Delay1_out1<=to_signed(0,16);
ELSIFclk'EVENTANDclk='1'THEN
IFenb='1'THEN
Unit_Delay1_out1<=Increment_Real_World_out1;
ENDIF;
ENDIF;
ENDPROCESSUnit_Delay1_process;


-- <Root>/2
alpha2_out1<=to_signed(50,16);

-- <Root>/Relational Operator

Relational_Operator_relop1<='1'WHENUnit_Delay1_out1>=alpha2_out1ELSE
'0';

-- <Root>/Data Type Conversion
Data_Type_Conversion_out1<='0'&'0'&'0'&'0'&'0'&'0'&'0'&'0'&'0'&'0'&'
0'&'0'&'0'&'0'&'0'&Relational_Operator_relop1;

Trip<=std_logic_vector(Data_Type_Conversion_out1);

ce_out<=clk_enable;

ENDrtl;
```

CURRICULUM VITAE

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