ISTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF ENERGY

DESIGN OF FAULT-TOLERANT CASCADED H-BRIDGE MULTILEVEL INVERTER WITH OUTPUT-SIDE TRANSFORMERS USING BIDIRECTIONAL SWITCHES

M.Sc. THESIS

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Energy Science and Technology Department

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ ENERJİ ENSTİTÜSÜ

ÇİFT YÖNLÜ ANAHTARLAR KULLANARAK HATA TOLERANSLI ÇIKIŞ TRAFOLU KASKAT H-KÖPRÜ ÇOK-SEVİYELİ EVİRİCİ TASARIMI

YÜKSEK LİSANS TEZİ

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OCAK 2013

Muhammet Biberoğlu, a **M.Sc.** student of ITU **Institute of Energy** student ID **301101062**, successfully defended the **thesis** entitled "**DESIGN OF FAULT-TOLERANT CASCADED H-BRIDGE MULTILEVEL INVERTER WITH OUTPUT-SIDE TRANSFORMERS USING BIDIRECTIONAL SWITCHES**", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my parents,

FOREWORD

First, I would like to express my deepest appreciation to my advisor, Prof. Dr. Filiz KARAOSMANOĞLU, for her support, all of her help and instructions during my study and research; also, I would like to thank Assist. Prof.Dr. Kayhan INCE, for his help, guidance and suggestions throughout the research.

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December 2012

Muhammet BİBEROĞLU
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ABBREVIATIONS

MOSFET : Metal Oxide Semiconductor Field Effect Transistor
IGBT : Insulated Gate Bipolar Transistor
DC : Direct Current
AC : Alternating Current
MLI : Multilevel Inverter
BDS : Bidirectional Switch
DB : Diode-Bridge
CS : Common Source
RES : Renewable Energy Sources
SARES : Stand Alone Renewable Energy Systems
PWM : Pulse Width Modulation
PS-PWM : Phase Shifted Pulse Width Modulation
LS-PWM : Level Shifted Pulse Width Modulation
PD-PWM : Phase Disposition Pulse Width Modulation
POD-PWM : Phase Opposition Disposition Pulse Width Modulation
APOD-PWM : Alternate Phase Opposition Disposition Pulse Width Modulation
NPC : Neutral Point Clamped
FC : Flying Capacitor
CHB : Cascaded H-Bridge
MTT : Multi-winding Transformer Topology
SVM : Space Vector Modulation
SHE : Selective Harmonic Elimination
NLC : Nearest Level Control
IEA : International Energy Agency
THD : Total Harmonic Distortion
MTHD : Minimisation of Total Harmonic Distortion

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DESIGN OF FAULT-TOLERANT CASCADED H-BRIDGE MULTILEVEL INVERTER WITH OUTPUT-SIDE TRANSFORMERS USING BIDIRECTIONAL SWITCHES

SUMMARY

Local electricity production, especially from renewable energy sources, seems to be one of the ideal solutions for the areas away from electrical grid of the cities. The globally increasing energy demand, running short of fossil fuels and researches for finding environment friendly choices strengthen this solution. However, the produced energy must be conditioned for the requirements of the electrical devices so that it can be used. One of the most needed devices for this purpose is the inverter.

Inverters can convert DC voltage/current signal to the AC voltage/current with desired magnitude and frequency. After invention of multilevel inverter, which syntheses the voltage as a staircase waveform, in the early of 80's, a though competition has been started between the multilevel inverters and classic two-level inverters. Multilevel inverters can achieve very low total harmonic distortion (THD) values at low switching frequencies without using any filtering units when compared with classic two-level inverters.

Among the multilevel inverters cascaded H-Bridge inverters comes to the fore by modularity and letting to increase the level of the system easily. However, multilevel inverters use high number of semiconductor elements, which increases the probability of any fault in the circuit, which may cause the whole system stopping for a long time. This is very critical issue for the buildings that have vital importance like hospitals or the industries where faults cost large amounts of money.

In this thesis, as a candidate solution for the problem mentioned above, a fault-tolerant cascaded H-Bridge quasi-eight-level multilevel inverter with a single DC source and with output side transformers is designed and application of reconfiguration technique is shown. The proposed inverter system can continue working if a fault occurs in one of H-Bridges with a one level decrement in the output voltage in quarter period. The proposed inverter system is designed and tested in MATLAB-SIMULINK simulation environment and comparisons are made by using two types of bi-directional switches, Diode-Bridge (DB) MOSFET and Common-Source (CS) MOSFETs, up to the quality parameters, THD and efficiency, under no-fault and fault conditions with resistive and series connected resistive-inductive loads.

ÇİFT YÖNLÜ ANAHTARLAR KULLANARAK HATA TOLERANSLI ÇIKIŞ TRAFOLU KASKAT H-KÖPRÜ ÇOK-SEVİYELİ EVİRİCİ TASARIMI

ÖZET

Şehir elektrik şebekesinden uzak bölgeler için, özellikle yenilenebilir enerji kaynaklarını kullanarak yerel-yerinde elektrik üretimi ideal çözümlerden biridir. Artan enerji talebi, fosil kaynakların tükenmesi ve çevre dostu seçeneklerin aranması bu çözümü güçlü kılmaktadır. Ayrıca bu çözümün maliyeti ile bu bölgelere yeni iletim hattı kurulmasının maliyeti kıyaslandığında nu çözümün daha avantajlı olduğu söylenebilir. Ancak üretilen bu elektriksel enerjinin evlerde, işyerlerinde kullanılabilmesi için, elektrikli cihazların çalışma koşullarıyla uyumlu olması gerekmektedir. Bu gerekliliği sağlamak için en yaygın kullanılan cihazlardan biri de eviricilerdir.

Eviriciler DC gerilim/akım sinyalini istenilen büyüklük ve frekansta AC gerilim/akım sinyaline çevirebilen güç elektroniği cihazlarıdır. Eviriciler; kare dalga eviriciler, modifiye edilmiş sinüs dalga eviriciler, saf sinüs dalga eviriciler ve çok seviyeli eviriciler olarak 4 temel grup altında toplanabilir.

1980'li yılların başında gerilimi merdiven basamağı şeklinde sentezleyebilen çok seviyeli eviricilerin hayatımıza girmesi ile çok seviyeli eviriciler ve klasik eviriciler arasında amansız bir yarış başlamıştır. Çok seviyeli eviriciler diğer klasik eviriciler ile kıyaslandığında, herhangi bir filtre ünitesi kullanmadan düşük anahtarlama frekanslarında çok düşük toplam harmonik bozunma değerlerine sahip AC sinyaller üretebilirler.

Çok seviyeli eviriciler: diyot-kenetlemeli, kapasite-kenetlemeli ve kaskad H-Köprü eviriciler olarak 3 ana gruba ayrılabilirler Çok-seviyeli eviriciler içinde kaskad H-Köprü eviriciler modüler yapıları ve kolaylıkla çıkış sinyalinin seviyesini artırmaya izin vermeleri ile ön plana çıkmaktadırlar. Ayrıca kaskad H-köprü eviricilerin yenilenebilir enerji kaynakları ile kolaylıkla adapte edilebilmesi bu tip eviricilerin evirici piyasasındaki yerini her geçen gün daha da sağlamlaştırmaktadır. Buna karşın çok-seviyeli eviricilerde fazla sayıda yarı-iletken eleman bulunması bu tip eviricilerin ortak bir dezavantaj olarak karşımıza çıkmakta ve sistemde hata oluşma olasılığını artırmaktadır. Bu durumda tüm sistemin uzun sureli olarak durması sorunu gerçekleşmektedir. Böylesi durma sorunları, özellikle hastane gibi hayati öneme sahip yapılar ve sistemin uzun sureli durması ile kayda değer boyutlarda maddi zarara uğrayabilecek büyük ölçekli işletmeler için kritik ve ciddi bir probleme neden olmaktadır.

Bu tez çalışmasında, belirtilen probleme çözüm seçeneği adayı olarak, hata toleranslı, tek fazlı ve tek DC kaynaklı, çıkış tarafında ikncil sarımları çok-sarımlı trafo tipli, 15 seviyeli kaskad H-Köprü evirici tasarımı ve yeniden yapılandırma tekniğinin uygulaması sunulmaktadır. Tasarlanan çok-seviyeli evirici sistemi, H-Köprü modüllerinden herhangi birinde hata meydana gelmesi durumunda, kontrol

sisteminde uygulanan modifikasyonlar ve trafoların ikincil sarımlarında trafonun dönüşüm oranını ayarlayabilme amacıyla bulunan çift-yönlü anahtarlar sayesinde gerilim seviyesi çeyrek periyotta bir azalarak çalışmasını sürdürebilmektedir. Çift-yönlü anahtar çeşitleri olan Diyot-Köprü MOSFET ve Ortak Kaynaklı MOSFET'ler ayrı ayrı tasarlanan sistemde test edilerek çıkış gerilimi ve çıkış akımı üzerinden kalite parametrelerine göre (toplam harmonik bozunma ve verimlilik) direnç ve seri bağlı direnç-bobin yükleri altında kendi aralarında kıyaslamaları yapılmıştır. Sistem MATLAB-SIMULINK simülasyon ortamında dizayn ve test edilmiştir.

1. INTRODUCTION

According to last report of International Energy Agency (IEA), the world total electricity generation was 20055 TWh, and the world total electricity consumption was 16759 TWh in 2009. Furthermore, three scenarios are mentioned in IEA's report for the forecasting of the energy vision of the world for the period runs to 2035; The New Policies Scenario, The Current Policies Scenario, and The 450 Scenario. According to projections done in these scenarios, the world electricity demand is varies from 28321 TWh to 31722 TWh [1]. If we consider the statistics for Turkey, total net electricity consumption was 169.4 billion kWh and total net electricity generation was 211.2 billion kWh in 2010 [2]. Moreover, if Turkey's growing economy and industry is considered, the electricity demand will rise continually year after year. In order to meet that demand, new energy resources should be found or existing resources should be used in more intelligent ways. Renewable energy sources (RES) stand as a wise solution for this problem. Renewable energy continued to grow strongly in all end-use sectors, power, heating and cooling, as well as transport, and supplied an estimated 17% of global final energy consumption and has a share of 20.3%, including hydro-power, in world total electricity generation in 2011, as shown in Figure 1.1. As in previous years, about half of the new electricity capacity installed worldwide was renewable based [3].

It is estimated that 2 billion of people are living without connection to electricity grid and this amount is increasing [4]. The electricity produced from RES can be integrated to distribution grid system or as an alternative way, RES can be used as stand-alone in remote areas from integrated-grid system due to environmental and economical reasons. This is especially valid for rarely populated areas where the cost for central supply is too high due to long power transfer distances and relatively low power demand. For example, electricity supply for the houses in European Alps or for hotels in Uludağ (Turkey) can be provided by the stand alone renewable energy sources (SARES).

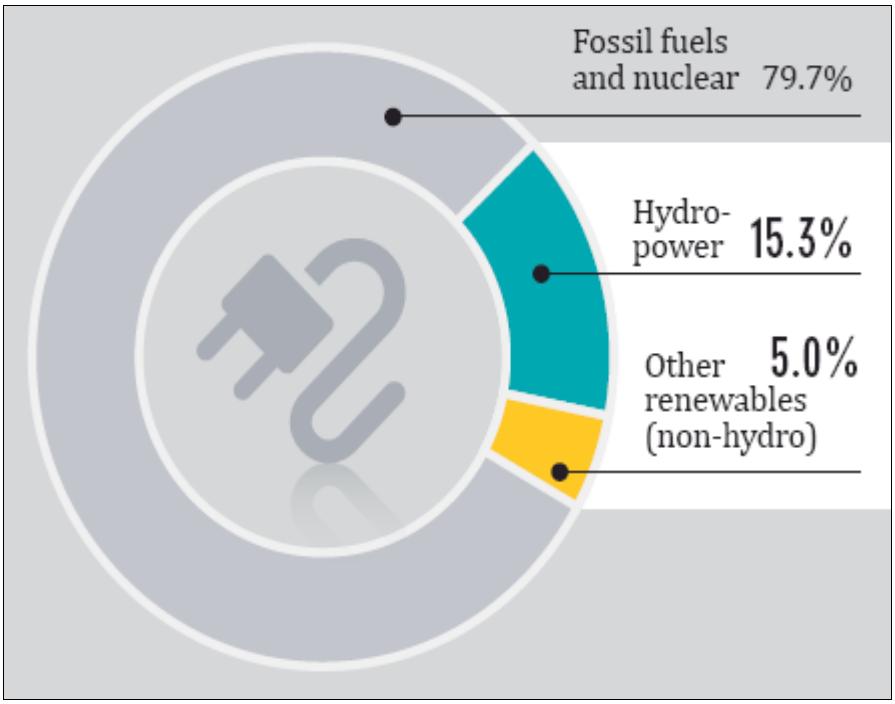


Figure 1.1 : Share of resources of the in electricity production [3].

The electricity generated from RES must be compatible with grid system or satisfy the necessities of stand-alone systems. For the particular case of SARES, it is of common sense that it should be capable of supplying alternating current (AC) electricity, thus providing compatibility with standard appliances that are cheap and widely available [5]. In Turkey, AC electricity grid needs ±10% of $230V_{rms}$ AC voltage and 50 Hz frequency. In order to satisfy these needs some power conversion systems are required.

The adoption of AC power has created a trend where most devices adapt AC power from an outlet into DC power for use by the device. However, AC power is not always available and the need for mobility and simplicity has given batteries an advantage in portable power. Thus, for portable AC power, inverters are needed. Inverters take a DC voltage from a battery or a solar panel as input, and convert it into an AC voltage output [6].

Inverters can be classified in four groups according to their output waveform; square-wave, modified square-wave (also called square wave or modified sine wave), pure sine-wave (synthesized by high frequency pulse width modulation-PWM) and multilevel (or multi-step). In Figure 1.2 waveforms for each category are shown [7].

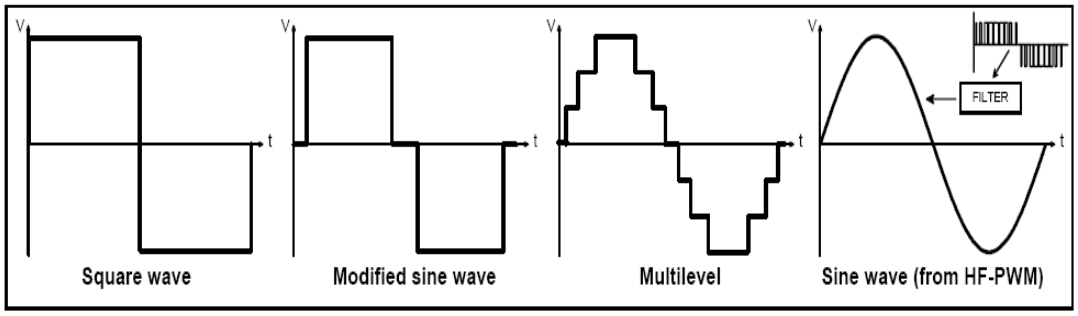


Figure 1.2 : Waveforms for different inverter types [7].

Square wave and modified sine wave inverters do not take much attention in because of their very poor quality waveforms but they are still available in market for practical applications. Multilevel and pure sine wave inverters are focused by the researches and all works are being done about them. In recent years there is a though competition between classical two level inverters and multilevel inverters. Multilevel converters show several advantages over conventional two-level converters. Some of the most attractive features of multilevel converters are briefly summarized as follows in [8] and [9]:

- **Staircase waveform quality**: Multilevel converters generate output voltages with much lower harmonic content and reduce the dv/dt stresses. Therefore, electromagnetic compatibility (EMC) problems can be reduced.
- **Common-mode (CM) Voltage**: Multilevel converters produce smaller CM voltage. The stress in the bearings of a motor connected to a multilevel motor drive, for example, can be therefore reduced. Furthermore, using advanced modulation strategies, CM voltage can be eliminated.
- **Input current**: Multilevel converters can draw input current with low distortion.
- **Switching frequency**: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. Therefore, through lower switching frequency, lower switching losses and higher efficiency can be achieved.

However, multilevel converters have some disadvantages. For these converters, great number of power semiconductors needed. This makes the overall system more complex, increases the conduction losses and probability of fault.

Reliability is a big challenge for the inverters using multilevel technology, due to used high number of semiconductor elements. The increasing number of switching elements causes the probability switching errors to rise. These switching errors may cause the whole system to shut down for a long time. Besides these errors, also short-circuit fault conditions may occur within the network system. It is wanted that the inverters simultaneously detect this error and keep the desired level of output voltage so that the energy flow continues. These issues become even more important in the buildings of vital importance (hospitals etc.) or in the institutions where these collapses cost large amounts of money. As a result, the industry leans to fault analysis and reconfiguration strategies so that the collapse time of such systems is shortened.

Conventional protection systems generally use passive devices such as fuse, over current relay and breakers, which just disconnect the system from the energy source. Fault analysis studies focus on analyzing the fault modes and providing operation methods for these modes.

The main objective of this thesis is to design and simulate a multilevel inverter which is based on the single-phase, single DC source cascaded H-Bridge multiple transformer inverter topology with bi-directional switches, and to improve the reliability of this multilevel inverter. The fault tolerant ability is resulted from the inherent redundant nature of the multi-switching-states topology and control signals modification and the performance of a reconfiguration technique that allows a cascaded H-bridge inverter to keep working even with a faulty bridge. The theory of fault-tolerant algorithm and reconfiguration is thoroughly investigated and its performance is verified by simulations in MATLAB-SIMULINK environment.

1.1 Thesis Structure

In Chapter 2, the state of the art of the multilevel inverters are presented and advantages and disadvantages of all multilevel inverter topologies are discussed briefly. Moreover, different types of bi-directional switches are shown and a short review of fault-tolerant and reconfiguration systems are done.

In Chapter 3, the proposed inverter scheme will be introduced in detail. The main working principle and control system explained briefly. Also, design parameters of

used semiconductor devices, transformers and bi-directional switches are shown. Fault management and reconfiguration techniques are explained in depth.

In Chapter 4, the simulation results are presented according to the different types of bi-directional switches and fault conditions. The designed systems performance parameters Total Harmonic Distortion (THD), efficiency, etc. Results are shown, and comments and comparisons are made. In the last chapter, a summary of works which have been done in this thesis are presented; finally, future works that can be followed as a progression of this thesis are mentioned.

2. THEORETICAL BACKGROUND OF MULTILEVEL INVERTERS

In this chapter, existing multilevel inverter (MLI) topologies in the market are explained and their differences, advantages and disadvantages are exhibited. Besides, modulation techniques of the MLIs, bidirectional swtiches' working principles and their types are presented. Finally, the fault tolerant MLI strategies are introduced.

2.1 Multilevel Inverter Topologies

Fundamentally, a multilevel converter is able to achieve higher power by using a series of power switches with several lower voltage DC sources or with single DC source to perform the power conversion by synthesizing a staircase voltage waveform. According to the inverter topology requirements, for example; power ratings and switching frequencies, appropriate power switches must be chosen. Power ranges for the power semiconductors in the market are given in Figure 2.1 [10,11].

Multilevel inverters use medium-power semiconductors as switches. While designing inverter circuitry, a choice had to be made between the two main types of switches used in power electronics. One is the power MOSFET, which is much like a standard MOSFET, but designed to handle relatively large voltages and currents. The other is the insulated gate bipolar transistor, or IGBT. Each has its advantages, and there is a high degree of overlap in the specifications of the two [12].

IGBTs tend to be used in very high voltage applications, nearly always above 200V, and generally above 600V. They do not have the high frequency switching capability of MOSFETs, and used at frequencies lower than 20 kHz. They can handle high currents, are able to output greater than 5 kW, and have very good thermal operating ability, being able to operate properly above 100 Celsius. One of the major disadvantages of IGBTs is their unavoidable current tail when they turn off. Essentially, when the IGBT turns off, the current of the gate transistor cannot dissipate immediately, which causes a loss of power each time this occurs [12].

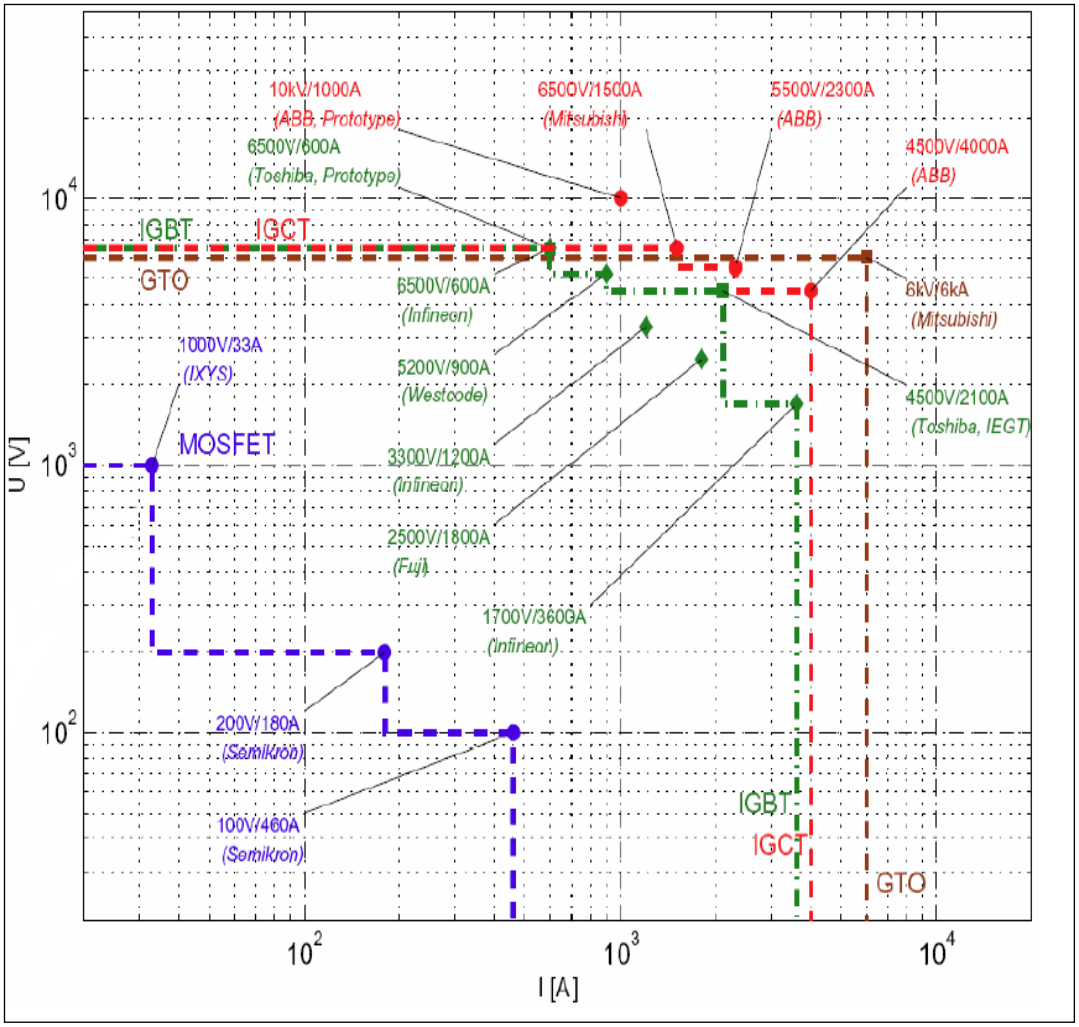


Figure 2.1: Power range of available power semiconductors [10,11].

Power MOSFETS have a much higher switching frequency capability than do IGBTs, and can be switched at frequencies higher than 200 kHz. They do not have as much capability for high voltage and high current applications, and tend to be used at voltages lower than 250V and less than 500W. MOSFETs do not have current tail power losses, which makes them more efficient than IGBTs. Both MOSFETs and IGBTs have power losses due to the ramp up and ramp down of the voltage when turning on and off (dV/dt losses). Unlike IGBTs, MOSFETs have body diode [12]. In the proposed inverter topology, MOSFETs were used as switches.

Multilevel converters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Moreover, multilevel converters present several other advantages. First of all, multilevel converters generate better output waveforms than the standard converters. Then, multilevel converter can increase the power quality due to the great number of levels of the

output voltage, by this way; the AC side filter can be reduced. Furthermore, multilevel converters can operate with a lower switching frequency sharing the whole voltage in small steps, so the electromagnetic emissions generated by them are weaker, to comply with the standards [13].

As mentioned before, multilevel inverters produces staircase voltage form. The generalized staircase waveform is shown in Figure 2.2. [7].

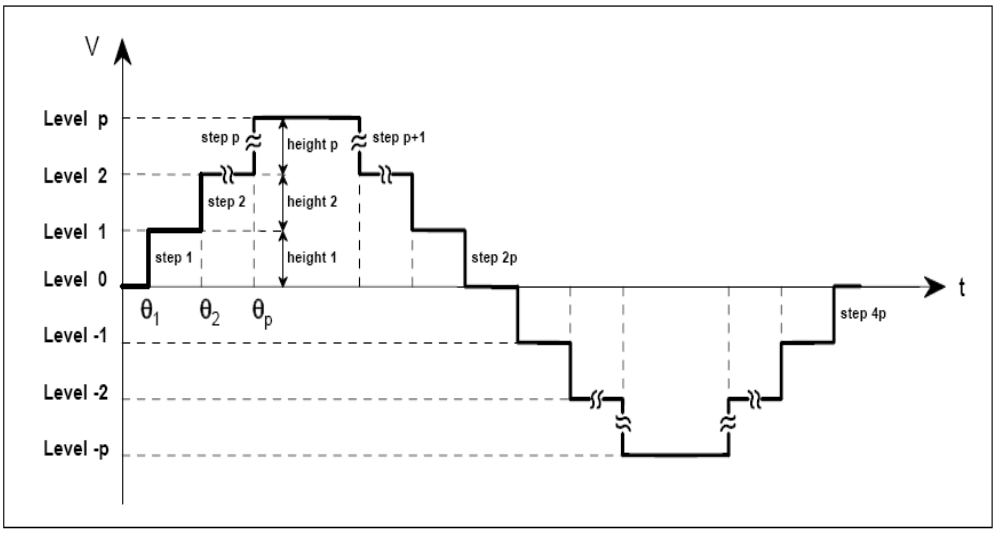


Figure 2.2: Generalized staircase waveform [7].

In this thesis following notations will be used to specify the properties of inverters;

P :The number of steps in quarter-cycle

2 × p+1 :Number of levels of an inverter

4 × p :Number of steps of an inverter

There are lots of multilevel inverter topology in the literature tested and installed. Multilevel inverters have been taking place in market about 40 years. Basicly, there are three fundamental multilevel topologies; diode clamped (NPC), flying capacitor (FC), and cascaded H-Bridge (CHB). Other topologies are the variations of these topologies. They can be classified as:

- Neutral point clamped multilevel inverter (NPC)
- Capacitor-clamped multilevel inverter (FC)
- Cascaded H-Bridge multilevel inverter (CHB)
- Multiple source topology
- Multi-winding transformer topology (MTT)

- Modular topology
- Multiple-transformer topology

2.1.1 Neutral point clamped MLI

This type of multilevel inverter topology was proposed by Nabae et al. in 1981 which is shown in Figure 2.3-a [14]. In this circuit, the DC-bus voltage is split into three levels by two series-connected bulk capacitors, C1 and C2. The middle point of the two capacitors, *n, can* be defined as the neutral point. The output voltage V_{an} has three states: *E*, 0 and -*E*. For voltage level *E*, switches S1 and S2 need to be turned on; for -*E*, switches S1' and S2' need to be turned on; and for the 0 level, S2 and S2' need to be turned on like shown in Table 2.1. [15]. It was the first widely used multilevel inverter in the market and still popular in industry applications. Number of levels can be increased by using the same concept of diode-clamped voltage levels as shown in Figure 2.3.b

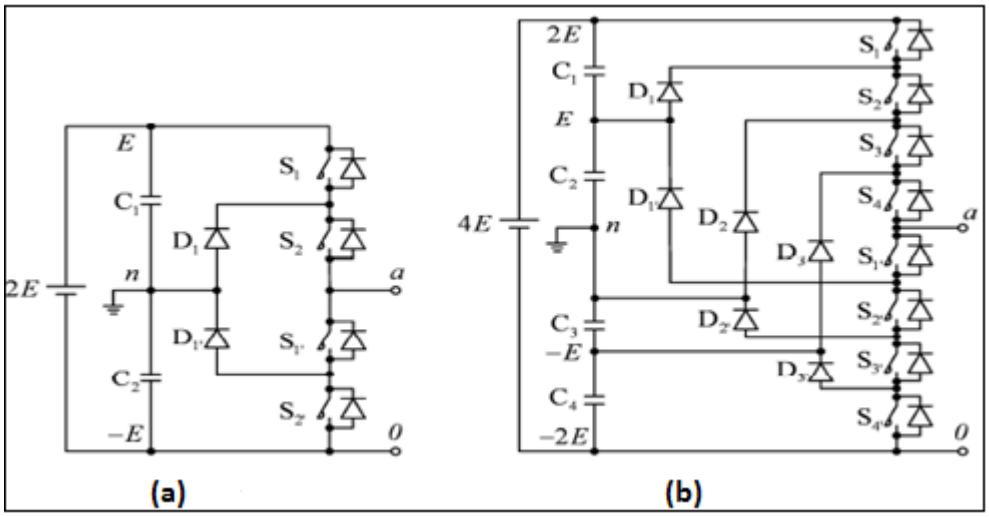


Figure 2.3 : Diode-clamped mulilevel inverter circuit topologies: (a)Three-level (b)Five-level [14].

Table 2.1 : Switches states and the output voltage for three-level NPC [15].

Output Voltage (V_{an})	**Switches' States**			
	S_1	**S_1'**	**S_2**	**S_2'**
E (V)	1	0	1	0
-E (V)	0	1	0	1
0 (V)	0	0	1	1

Advantages of NPC multilevel inverters are:

- A large number of levels yield a small harmonic distortion.
- All phases share the same DC bus.

- Reactive power flow can be controlled.
- Control is simple [16].

The disadvantages are the followings:

- Different voltage ratings for clamping diodes are required.
- Real power flow is difficult because of the capacitors' imbalance.
- Different current ratings for switches are required due to their conduction duty cycle [16].

2.1.2 Capacitor-clamped MLI

The capacitor-clamped multilevel converter or flying-capacitor (FC) converter, is similar to the diode-clamped topology, which is shown in Figure 2.4. However, the capacitor-clamped multilevel topology allows more flexibility in waveform synthesis and balancing voltage across the clamped capacitors [16]. The inverter in Figure 2.4.(a) provides a three level output across *a* and *n*, i.e. V_{an} = *E*, 0, or -*E*. For the voltage level *E*, switches S1 and S2 need to be turned on; for -*E*, switches S1' and S2' need to be turned on; and for the 0 level, either pair (S1, S1') or (S2, S2') needs to be turned on like shown in Table 2.2. Clamping capacitor C1 is charged when S1 and S1' are turned on, and is discharged when S2 and S2' are turned on. The charge of C1 can be balanced by a proper selection of the 0-level switch combinations [15]. Number of levels can be increased with the same idea as in NPC shown in Figure 2.4(b).

The advantages of the capacitor-clamped multilevel converter are:

- When the number of levels is increased that allows the capacitors extra energy during long discharge transient.
- Flexible switch redundancy for balancing different voltage levels
- A large number of levels yields a small harmonic distortion.
- Active and reactive power flow can be controlled [16].

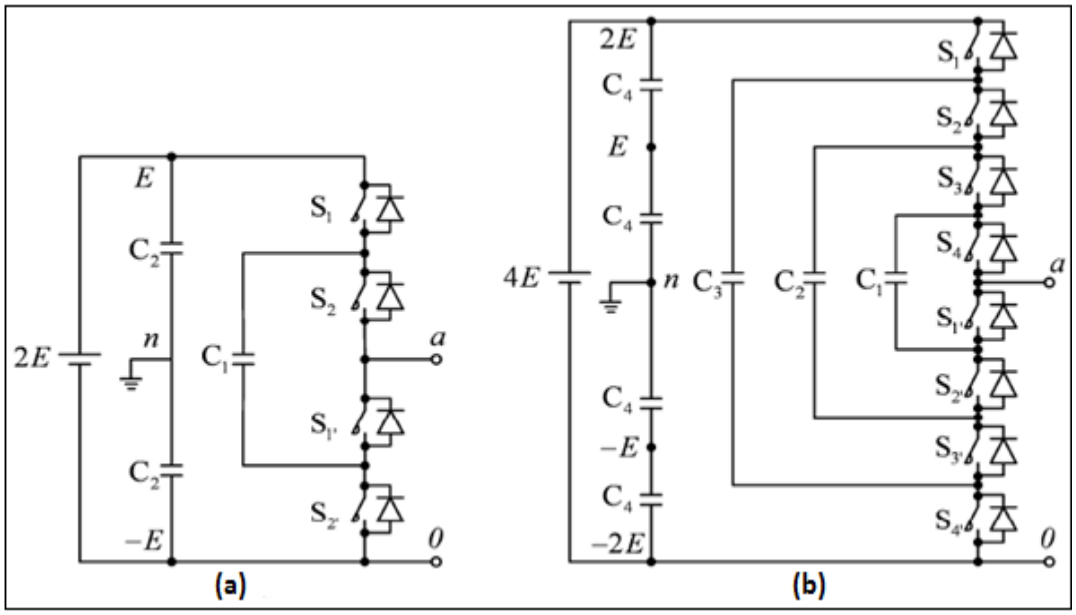


Figure 2.4 : FC multilevel inverter circuit topologies (a)Three-level (b)Five-level [16].

Table 2.2: Switches states and the output voltage for three-level FC [15].

Output Voltage (V_{an})	**Switches' States**			
	S_1	**S_1'**	**S_2**	**S_2'**
E (V)	1	0	1	0
-E (V)	0	1	0	1
0 (V)	1	1	0	0
0 (V)	0	0	1	1

The disadvantages are:

- Large number of capacitors is bulky and more expensive than the clamping diodes used in the diode-clamped multilevel converter.
- Control for maintaining the capacitors' voltage balance is complicated.
- Poor switching utilization and efficiency for real power transmission [16].

2.1.3 Cascaded H-Bridge MLI

Cascaded H-Bridge(CHB) multilevel inverter was first proposed in 1975 by Baker and Bannister [17]. The CHB inverter produces a sinusoidal voltage from different sources of direct current. The inverter is based on the fullbridge(H-Bridge) inverter (cell), that allows increase the number of levels 2m +1 where m is the number of cells that build the inverter [18]. This type of inverter avoids the use of interlocking diodes, capacitors voltage balancing float also a low THD can be obtained by controlling the gate trigger of the different voltage levels, this topology is divided into two types:

- Symmetric CHB inverter
- Asymmetric CHB inverter [19].

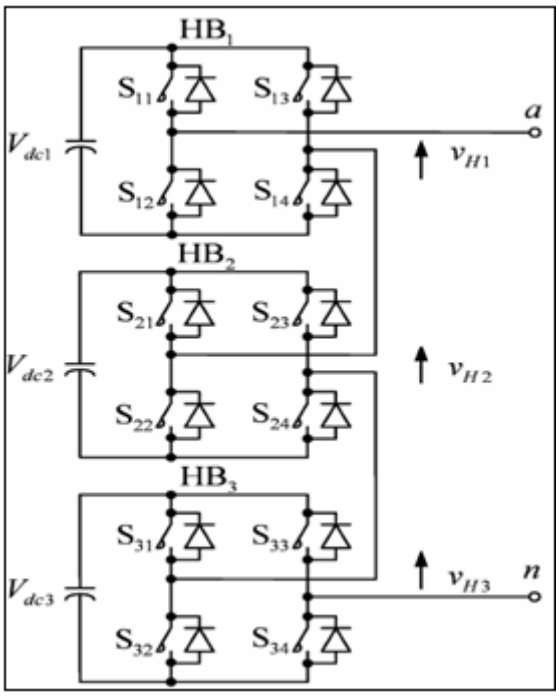


Figure 2.5 : Cascaded H-Bridge multilevel inverter with seperate DC sources [19].

In the CHB symmetric the power sources in each cell are of same value: If we consider topology in Figure 2.5, when

$$V_{DC1} = V_{DC2} = V_{DC3} = E \quad \textbf{(2.1)}$$

Each H-bridge cell can generate three output voltage: E,-E or 0 according to the switch states given in Table 2.3. In this table, switch states and output voltage values are given only for the first H-Bridge cell. Moreover, for other H-Bridge cells this idea is identical. The output voltage V_{an} is equal to the sum of the all of H-Bridges' output voltages. By the way, the output V_{an} can take values as 3E, 2E, E, 0, -E, -2E, -3E, then we have 7-level CHB symetric. The output voltage level can be increased by adding more H-bridge cells in cascade.

$$V_{an} = V_{H1} + V_{H2} + V_{H3} \quad \textbf{(2.2)}$$

Table 2.3 : Switch-Sates for the first H-Bridge cell [19].

Output Voltage (V_{an})	Switches' States			
	S_{11}	S_{12}	S_{13}	S_{14}
E (V)	1	0	1	0
-E (V)	0	1	0	1
0 (V)	1	1	0	0
0 (V)	0	0	1	1

Advantages of this topology are:

- No need for clamping diodes and clamping capacitors.
- Required a small number of components compared to diode-clamped and capacitor-clamped multilevel inverters.
- By increasing the number of levels, lower harmonic distortion can be achieved [20].

A disadvantage is that:

- The number of independent DC sources required increases with the number of desired levels [20].

The CHB asymmetric get more levels in the output voltage with the same number of cells that integrates a CHB symmetric. The difference in levels of output voltage is mainly due to use of different supply voltages in the cells of the inverter and the use of appropriate modulation technique. The advantage of using the CHB asymmetric is that it has less conduction losses favor the results of tension the inverter the output. The main disadvantage is that some levels the voltage the output is achieved by the sum of voltages of opposite signs, leading, higher switching losses [21]. Furthermore, the CHB asymmetric is divided in two classes:

- CHB asymmetric exponent 2
- CHB asymmetric exponent 3

The CHB asymmetric exponent 2 is shown in Figure 2.6, the levels of input voltage of each cell are V_{dc} and $2V_{dc}$ (exponent 2). In this configuration 2^{m+1}-1 voltage levels can be achived at the load voltage where m is the number of H-Bridge cells [22].

The CMLI asymmetric exponent 3 is shown in Figure 2.7, the levels of input voltage of each cell are Vdc and 3Vdc (exponent 3) [22] . In this topology, the voltage delivered to the output has 3^m voltage levels where m is the number of H-Bridge cells.

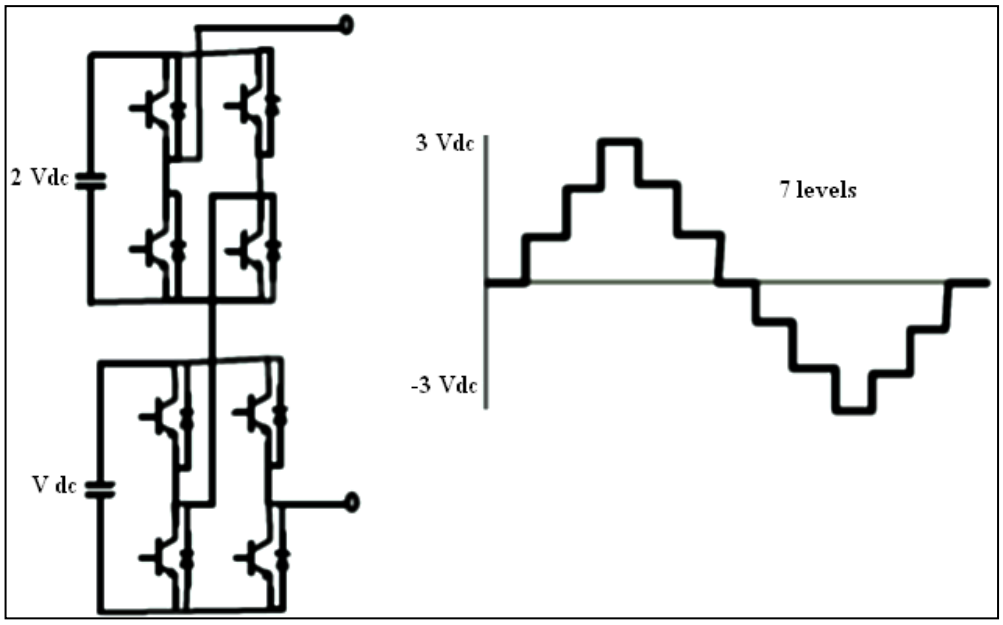


Figure 2.6 : CHB asymmetric exponent 2 [22].

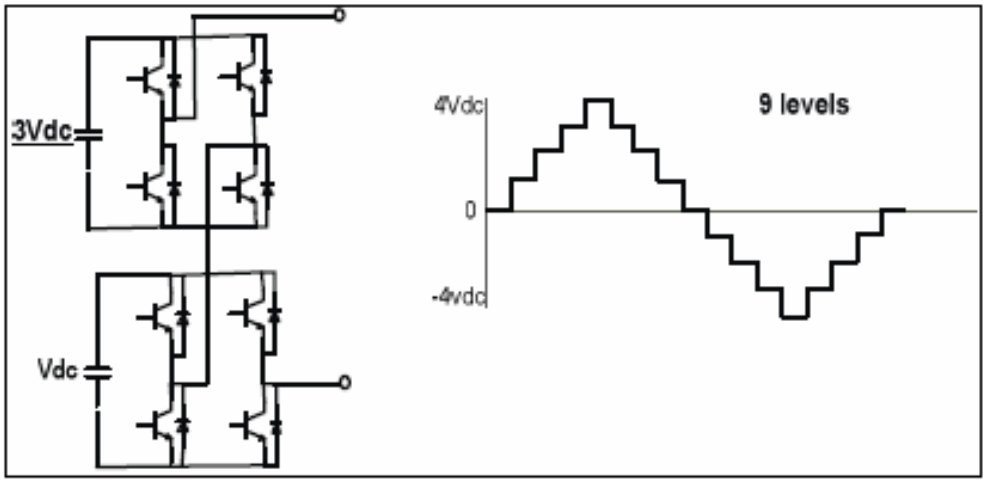


Figure 2.7 : CHB asymmetric exponent 3 [22].

In general the advantages of the CHB asymmetric are:

- It requires fewer components because the same amount of cells and more symmetric levels are achieved.
- A greater number of levels, lower harmonic distortion.
- The active and reactive power flow can be controlled [22].

A disadvantage is that:

- As the number of levels increases, the converter control becomes more complex as more levels must be achieved with less number of cells [22].

2.1.4 Multiple source topology

This topology uses isolated DC sources produce a stepped waveform by the aid of just one H-bridge inverter, shown in Figure 2.8. [23]. This topology is one of the most efficient multilevel inverter in the market. It has been tested in RES applications more than 15 years and proved that it is efficient, robust and reliable [24]. However, this configuration requires seperate DC sources and does not provide input-output isolation.

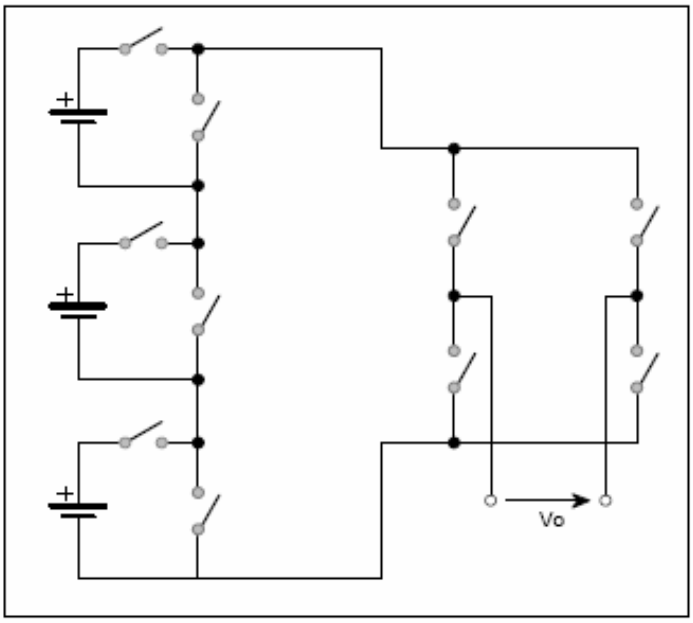


Figure 2.8 : Multiple source topology [23].

2.1.5 Multi-winding transformer topology

It is a variation of multiple source topology. An example of three-winding topology is shown in Figure 2.9.

Advantages of this topology:

- Just a single source is required
- Input-output isolation achived by the use of transformer.
- It uses just one transformer so it is efficient.

Disadvantage is:

- Lots of switches in the output side [7].

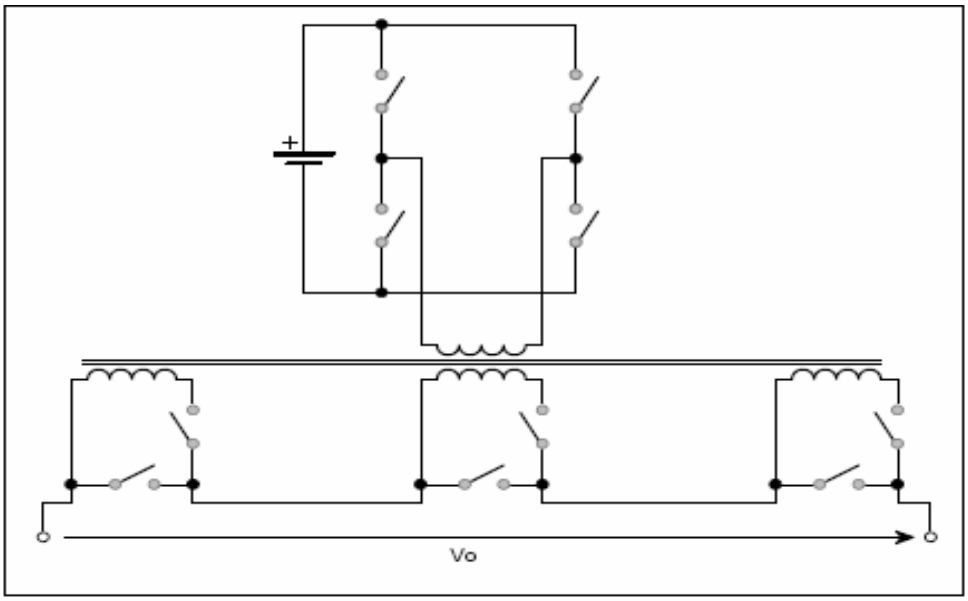


Figure 2.9 : Multi-winding transformer topology [7].

2.1.6 Modular topology

Figure 2.10 shows the eight-module modular topology. This topology is generally proposed for high power applications [25,26]. Each module, which is a two terminal device, is modelled by two switches and one local DC capacitor. The disadvantage of this topology every module's capacitor needs a voltage measurement circuit and it does not support loads with DC current component [7].

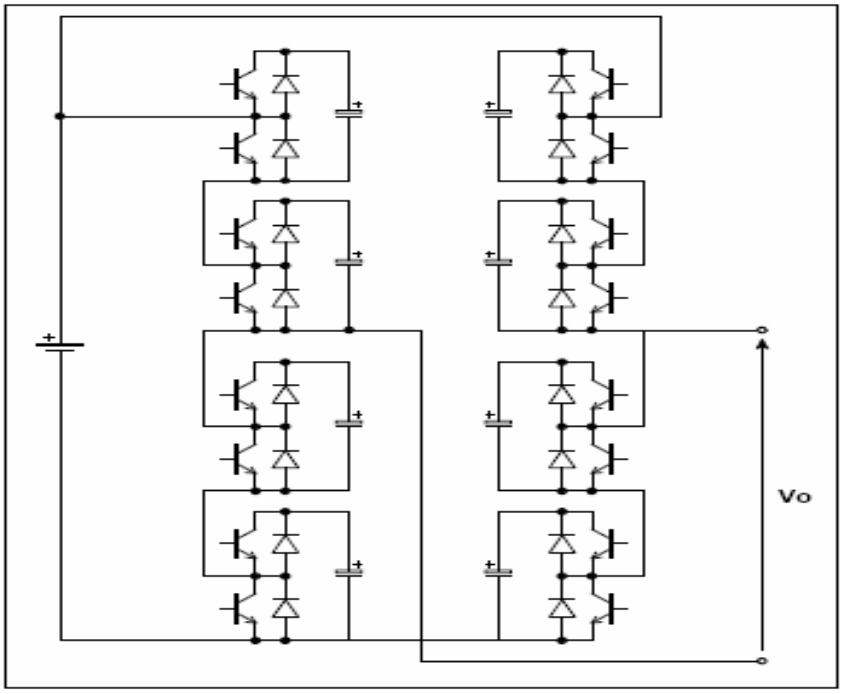


Figure 2.10 : Modular topology [25,26].

2.1.7 Multiple-transformer topology

This topology is a variation of cascaded multilevel inverter. In this configuration each H-Bridge module has a isolation transformer at the output side. Every secondary of transformer is connected in series to pile of output level up. There is some inverters in the market based on this topology [27,28].

The turn ratios of the transformers can be exponent 2 or exponent 3. According to these turn ratios of the transformers the level of the inverter is determined. When we consider the topology shown in Figure 2.11;

If we select the turns-ratios of the transformers are as exponent 2, we will have turns-ratios as followings; the first transformer's $1{:}2^0$, the second transformer's $1{:}2^1$, and for the third transformer's 2^2. As a result at the output stage will have 15-level (7 level positive,7 level negative and level'0'). The formula for determining the voltage levels in this system is 2^{n+1}-1 where n is the number of H-Bridge cells.

If we select the turn-ratios of the transformers are as exponent 3, we will have turns-ratios at first transformer is $1{:}3^0$, at second transformer $1{:}3^1$, and at third transformer 3^2. As a result, at the output stage will have 27-level (13 level positive,13 level negative and level'0'). The number of the levels in this transformer can be easily found by the formula 3^n.

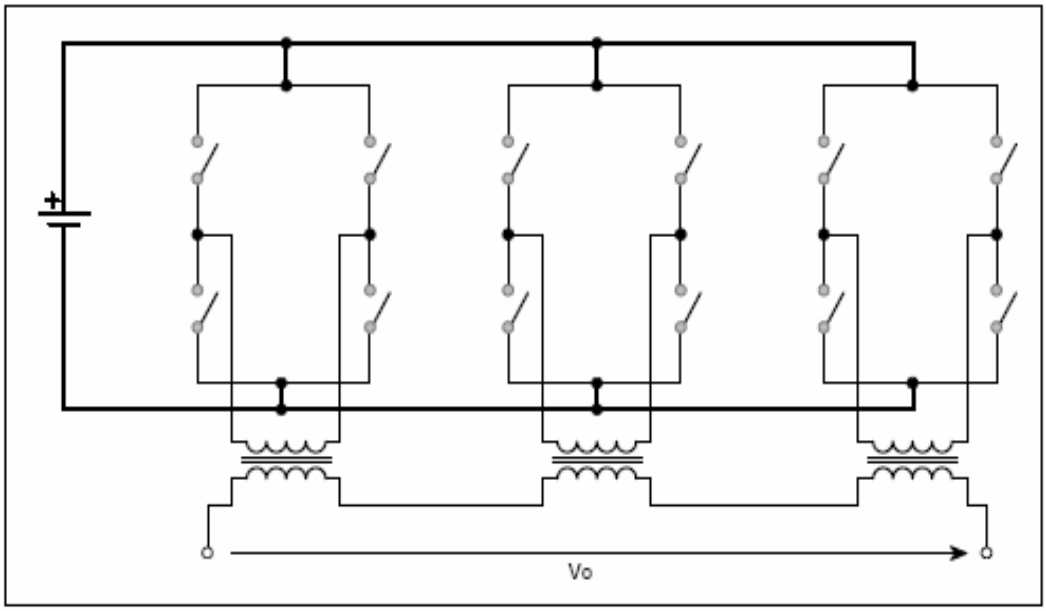


Figure 2.11 : Cascaded H-Bridges with isolation transformers [7].

Advantages of this topology:

- This topology requires only one DC source.
- It is robust and reliable.
- The leakage reactance of transformers act like series active filter, so THD is reduced.
- The transformers provide a galvanic isolation between input and output.
- It maintains the advantages of the cascade multilevel inverter:
    - Low dV/dt in the devices.
    - High definition of the output voltage and low harmonic content.
    - It uses a smaller quantity of semiconductors that the other two topologies of multilevel inverters [7].

The only disadvantage of this topology is it requires some low frequency transformers.

2.2 Modulation Techniques for MLIs

The modulation algorithm used to drive the multi-level converter give the voltage level required for each leg; the translation in the proper configuration of switches is done by other algorithms which can be hardware or software implemented. It is generally accepted that the performance of an inverter, with any switching strategies, can be related to the harmonic contents of its output voltage [29]. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms. Up-to-date, there are many techniques, which are applied to inverter topologies. A classification of the modulation methods for multilevel inverters is presented in Figure 2.12. The modulation algorithms are divided into two main groups depending on the domain in which they operate: the state-space vector domain, in which the operating principle is based on the voltage vector generation, and the time domain, in which the method is based on the voltage level generation over a time frame [30]. The aim of redundant configurations which is, to improve the switching pattern, to balance the current flowing through the switches, must be defined for the application. In general, low switching frequency methods are preferred for high-power applications due to the necessary reduction of switching

losses, while the better output power quality and higher bandwidth of high switching frequency algorithms are more suitable for high dynamics applications [31,32,33].

2.2.1 MLI PWM strategies

Classic PWM techniques have been successfully adopted to multilevel inverter topologies by using multiple carries to control each power switch of the inverter so they are known as multicarrier PWM methods.

For multicell topologies, FC and CHB, each carrier can be associated to a particular power cell to be modulated independently using sinusoidal bipolar PWM and unipolar PWM, respectively, providing an even power distribution among the cells. Therefore, this method is known as phase shifted PWM (PS-PWM). This method naturally balances the capacitor voltages for the FC and also mitigates input current harmonics for the CHB.

The carriers can also be arranged with shifts in amplitude relating each carrier with each possible output voltage level generated by the inverter. This strategy is known as level shifted PWM (LS-PWM), and depending on the disposition of the carriers, they can be in phase disposition (PD-PWM), phase opposition disposition (POD-PWM), and alternate phase opposition disposition (APOD-PWM) [34]. LS-PWM methods can be implemented for any multilevel topology; however, they are more suited for the NPC, since each carrier signal can be easily related to each power semiconductor. Particularly, LS-PWM methods are not very attractive for CHB inverters, since the vertical shifts relate each carrier and output level to a particular cell, producing an uneven power distribution among the cells. This power unbalance disables the input current harmonic mitigation that can be achieved with the multipulse input isolation transformer, reducing the power quality.

Finally, the hybrid modulation is in part a PWM-based method that is specially conceived for the CHB with unequal dc sources and for the CHB topologies with transformers [30]. Moreover, this idea gives significant results for multiple-transformer topology.The basic idea is to take advantage of the different power rates among the cells of the converters to reduce switching losses and improve the inverter efficiency. This is achieved by controlling the high-power cells at a fundamental switching frequency by turning on and off each switch of each cell only one time per

cycle, while the low-power cell is controlled using unipolar PWM. In this thesis, hybrid modulation are used and will be discussed detailly in next chapter.

2.2.2 Space vector modulation techniques

Space vector modulation (SVM) is a technique where the reference voltage is represented as a reference vector to be generated by the power converter. The SVM technique generates the voltage reference vector as a linear combination of the state vectors obtaining an averaged output voltage equal to the reference over one switching period [35].

2.2.3 Other MLI modulation algorithms

Although SVM and multicarrier PWM are widely accepted and have reached a certain maturity for multilevel applications, other algorithms have been developed to satisfy particular needs of different applications.

Selective harmonic elimination (SHE), for example, has been extended to the multilevel case for high-power applications due to the strong reduction in the switching losses [36,37,38]. However, SHE algorithms are very limited to openloop or low-bandwidth applications, since the switching angles are computed offline and stored in tables, which are then interpolated according to the operating conditions. In addition, SHE based methods become very complex to design and implement for converters with a high number of levels (above five), due to the increase of switching angles, hence equations, that need to be solved. In this case, other low switching frequency methods are more suitable. The time-domain version of SVC is the nearest level control (NLC), which in essence is the same principle but considering the closest voltage level that can be generated by the inverter instead of the closest vector [39]. As mentioned above, not all of the modulation schemes are suitable for each topology; moreover, some algorithms are not applicable to some converters. Table 2.4 summarizes the compatibility between the modulation methods and the multilevel topologies.

Selecting the best inverter topology for the application can differ according to system requirements. As a particular case for SARES, the most important performance parameters are reliabilty,surge power capacity and efficiency.Multilevel inverters are presented in recent works that they can succesfully satisfy these parameters [7].

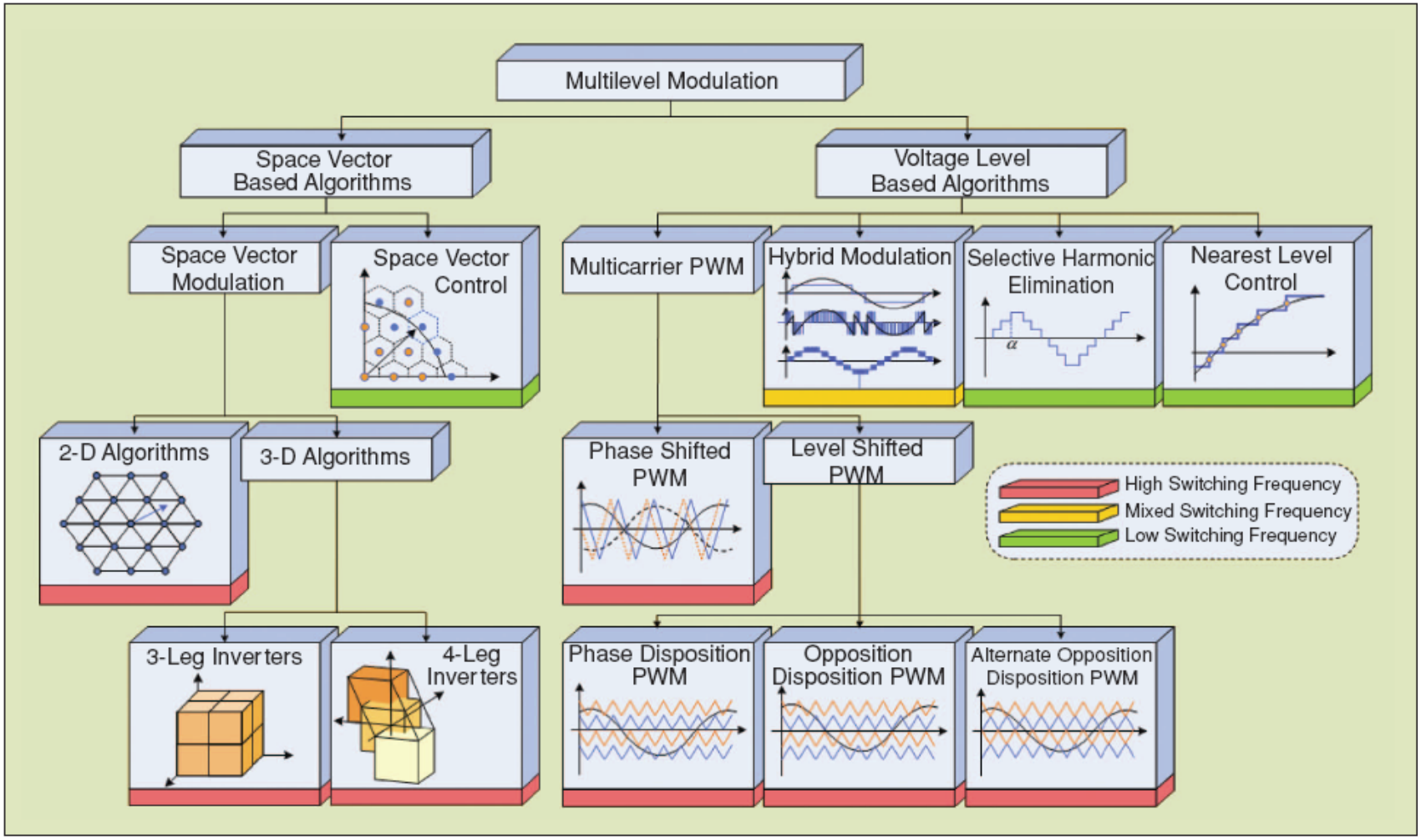


Figure 2.12 : Multilevel inverter modulation classification [30].

Depending on the application,the multilevel converter topology can be chosen according to some factors as shown in Table 2.5.

Table 2.4 : Applicability of modulation methods to multilevel topologies [30].

✓Applicable X Not Applicable −Applicable/Not Recommended

Modulation Methods	**Topologies**		
	NPC	**FC**	**CHB**
SVM	✓	✓	✓
LS-PWM	✓	✓	-
PS-PWM	X	✓	✓
Hybrid Modulation	X	X	✓
SHE	✓	✓	✓
SVC	-	✓	✓
NLC	-	✓	✓

Table 2.5 : Comparison of multilevel inverter topologies depending on implementation factors [30].

Implementation Factors	**Topologies**			
	NPC	**FC**	**CHB**	**MTT**
Specific Requirements	Clamping diodes	Additional capacitors	Isolated DC sources	Low frequency transformers
Modularity	Low	Low	High	High
Design and implementation complexity	Low	Medium	High	High
Control concerns	Voltage balancing	Voltage setup	Power sharing	Power sharing
Fault tolerance	Difficult	Easy	Easy	Easy

2.3 Bi-directional Switch Technology

By definition a Bi-Directional Switch (BDS), in literature also named bilateral switch or AC-switch or 4Q-switch (Q stands for quadrant), has to be capable of conducting

currents and blocking voltages of both polarities, depending on control actual signal as shown in Figure 2.13 [40].

Since no single device is available as a bidirectional self commutated switch, a bidirectional switch is synthesized from the combination of commonly used solid state devices. In order to build a composite BDS with the capability of conduction in both directions, it is necessary to connect two discrete devices in anti-serial association of two unidirectional voltage devices or in anti-parallel association of two unidirectional current devices [41].

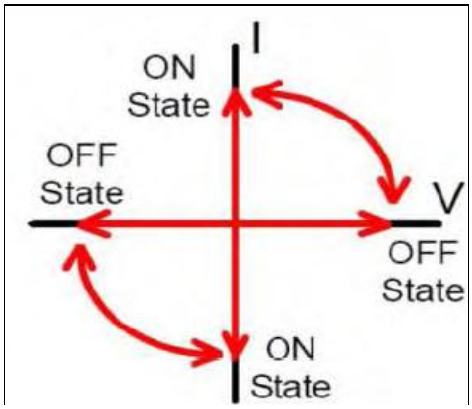


Figure 2.13 : Device working quadrants [40].

There are lots of BDS configurations in the literature using different semiconductors like IGBTs, IGTCs, BJTs and MOSFETs. However, the configurations with MOSFETs are mentioned in this work. There are different bi-directional switch configurations by MOSFETs in the market shown in Figure 2.14.

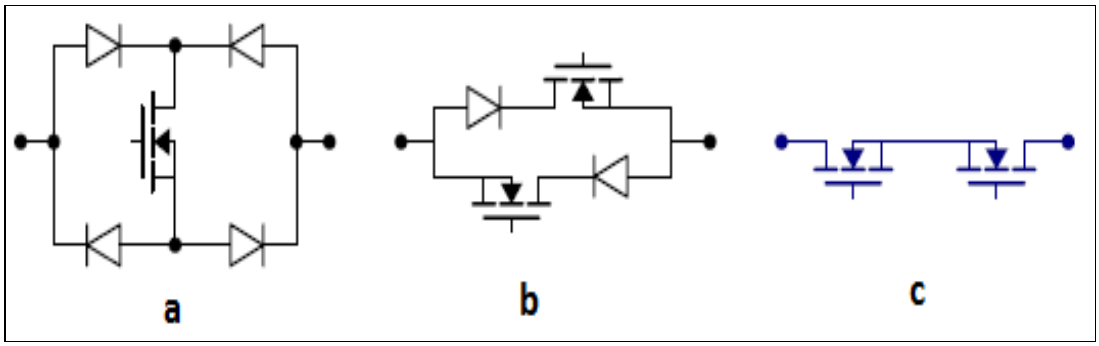


Figure 2.14 : Different bi-directional switch implementations by using MOSFETs [7].

The switch shown in Figure 2.13.a is easy to control. Only one unidirectional controllable switch (MOSFET) is used in a four-diode bridge. However, its voltage drop is high. It is equal to the sum of the voltage drops of two diodes and the

transistor. This arrangement is expensive if high voltage fast recovery diodes are to be used. The unique control makes this switch a real bidirectional switch [7].

The second proposed configuration of bi-directional switch was the anti-parallel arrangement of two active devices, MOSFETs in Fig.2.13.b, with series diode. The two diodes are used to provide the reverse voltage blocking capability. This configuration reduces the voltage drop but needs two MOSFETs. It is the most expensive configuration. Furthermore, compared to the diode bridge switch, this solution has also the advantage of lower conduction losses, since only two devices are conducting at any given time [7].

With MOS-transistors, the switch of Figure 2.13.c is the simplest one. It needs only two components because the diodes are part of the transistors. This configuration provides lower losses when compared to previously mentioned configurations because of the low on resistance of modern MOSFETs and its bi-directional channel conduction capability. When both MOSFETs are on, it can be modelled as a two times Ron resistance of a single MOSFET [7].

2.4 Fault-Tolerant MLI Strategies

Reliability is an important issue in cascaded H-bridge converters and multi-transformer topologies because they use a high number of power semiconductors. A faulty power semiconductor in any of H-bridges can potentially lead to expensive downtime and great losses on the consumer side. Also any failure of the semiconductors in H-Bridges break the balance between the positive and negative parts of the output voltage that quickly increases the harmonic distortion. It is important to maintain normal operation under fault conditions because failed operation of a inverter could cause tremendous losses for consumers, especially when the inverter is feeding critical loads. Cascaded multilevel inverters have a character that each unit can work independently. After a unit stops working because of fault, if we can make the other units continue working with the output of the system unchanged or changed in acceptable limits, the reliability of the system will be improved greatly. [42]. With the fault-tolerant control strategies and reconfiguration techniques, operation can continue with the undamaged cells; thus increasing the reliability of the system. The key issue when designing a fault-tolerant system is to improve system reliability [43].

For a fault-tolerant system, the basic goal is to continue operation in the event of a power failure. There are two types of fault-tolerant method, one is hardware redundant, and another is to cut the fault unit away [44].

The hardware redundant is to design surplus unit in the systematic design. In [43], the proposed strategy for the fault-tolerant system is redundancy. In CHB inverters, all H-Bridge cells are identical so the redundacy strategy is easily applied by adding an H-Bridge cell as a back-up to maintain operation when one of H-Bridge cells fails. When the trouble appears, replace the trouble unit with the surplus unit, in order to make the system continue working. Dependability of this method is relatively high, but it needs at least one unit unused as redundant, which causes the ratio of the systematic utilization low. When the trouble appears, replace the trouble unit with the surplus unit, in order to make the system continue working. Dependability of this method is relatively high, but it needs at least one unit unused as redundant, which causes the ratio of the systematic utilization low.

Cutting the failure unit away takes the advantage of the cascaded inverter's property that is each unit of the inverter can work independently, so after cutting the fault unit away, the rest can continue to work. If taking this method, to make the output of the three phases balance, each healthy phase should cut one unit, too. As the result, the value of output voltage is reduced and the machine system must run at a lower speed at this moment [45]. However for the single-phase systems this problem does not exist.

As an alternative method to these methodes mentioned above, B.Wang and et al. proposed a reconfiguration method with bi-directional swtiches for 3-phase systems. Once a fault is detected in any of the IGBTs of any H-bridge, the control is capable to reconfigure the hardware keeping the higher power bridges in operation. In this way, the faulty phase can continue working at the same voltage level by adjusting its gating signals. This method is based on the multiple-transformers topology. The design consists of three H-Bridge cells and with output transformers for each cell. The turn ratios of the transformers scaled in power of three. One of the transformers in the topology is multi-winding transformer with bi-directional switches which are used between different windings of the transformer. When a fault occurs, by the aid of bi-directional switches, the turn-ratio of the transformer changes and the desirable voltage level is achived [42].

2.5 Literature Review

In this subdivision, literature review of the multilevel inverter types, multilevel inverter modulation techniques, bi-directional switch types and fault tolerant designs of multilevel inverters are done.

Generally, multilevel inverter applications can be classified in three groups within the semi-conductor technologies framework; these are diode-clamped inverters, capacitor clamped inverters and multi-cascade H-bridge inverters [46,47,48,49].

There are some review studies about multilevel inverters and modulation techniques in the literature. J.Rodriguez presented the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. Their work presents relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulsewidth modulation, multilevel selective harmonic elimination, and space-vector modulation [50].

J.Rodriguez et al. presented a technology review of voltage-source-converter topologies for industrial medium-voltage drives. This paper presents the operating principle of each topology and a review of the most relevant modulation methods, focused mainly on those used by industry.They asserted that the topology and modulation-method selection are closely related to each particular application, leaving a space on the market for all the different solutions, depending on their unique features and limitations like power or voltage level, dynamic performance, reliability, costs, and other technical specifications [51]. Leopoldo G. Franquelo et al. made a review study and claimed that multilevel inverter technology has potential in current and future power applications by expailing MLI topologies,modulation techniques,fault-tolerant system designing and usage areas detailly [30]. And current survey studies about MLIs are presented in [49,52].

As a special case, S.Daher et al. presented a compilation of the most common topologies of multilevel converters is and showed which ones are best suitable to implement inverters for stand-alone applications in the range of a few kilowatts. He asserted that the most suitable topologies are the multiple transformer and the multi-winding transformer for stand-alone applications [54].

P.Palanivel analysed three carrier pulse width modulation techniques, the constant switching frequency (CSF), variable switching frequency (VSF), and phase shifted pulse width modulation (PSPWM) , which can minimise the total harmonic distortion and enhances the output voltages from five level inverter [53].

Steffen Bernet et al. was designed and compared neutral-point clamped, flying capacitor and series connected cascaded H-Bridge multilevel inverters at the same voltage level and showed that series connected cascaded H-Bridge inverts are very attractive for high frequencies [47].

In this thesis, cascaded H-Bridge inverters are used as a base for proposed inverter. Hence, literature review of cascaded H-Bridge inverter is made in detail.The CHBs generally divided into two main categories; CHB with separate DC sources and with single DC source.

A.R.Being et al. proposed a fifteen-level cascaded H-bridge configuration with equal seperate DC sources with low harmonic content using low voltage MOSFETs as switching devices [55]. H.Patangia is presented a 8-level 1kW CHB inverter prototype with seperate DC sources using sectionalized PWM technique. They achived 99% efficiency but their system has high total harmonic distortion which is about 15% [56]. O.L.Jimenez et al. focused on the comparative study of cascaded multilevel inverter with two inverter cells, symmetric (5 levels) and asymmetrical (7 and 9 levels). These inverters are implemented without changes in the power semiconductor devices, only modify the control stage and input supply voltages in the cells. Their work presented the analysis of the output voltage total harmonic distortion (THD) of CHB and ACHB [20]. N.Farokhnia et al. applied minimisation of total harmonic distortion (MTHD) switching strategy is applied to the cascaded multilevel inverter to reduce the THD. In this paper, they proposed to consider the alterable DC sources instead of constant DC sources, if it is possible. They showed that the value of THD in both cases of phase and line voltages is effectively reduced [57]. J.Pereda et al. offered a solution to the problem of Cascaded H-Bridge(CHB) and Asymetric cascaded H-bridge(ACHB) inverters that is large number of bidirectional and isolated dc supplies. This problem reduces the power quality with the voltage amplitude.They presented a solution to this problem by using high-frequency link using only one DC power source which reduces the number of active semiconductors, transformers, and reduces harmonic content [58]. Also, Cheol-soon

Kwon et al. proposed a cascaded H-bridge multilevel inverter employing trinary dc sources in order to obtain a large number of output voltage levels with minimum devices which permits to easy increase of the output voltage levels and output power owing to modularity characteristic [59].

The CHB inverters using single DC source are examined in literature in two main groups;with virtual DC sources and with transformers in literature. CHB inverters with virtual DC sources are presented as a new hybrid CHB inverter which modifies the traditional CHB inverter by using one DC source. The traditional cascade multilevel inverter requires n DC sources for 2n + 1 levels. The proposed system allows the use of a single DC source as the first DC source which would be available from PV cells, batteries or fuel cells, with the remaining DC sources being capacitors. K.M Tsang et al. designed a PWM-less 27-level inverter has been based on three cascaded H-bridges with a single energy source and two capacitors.These capacitors are used as virtual DC sources in this work [60]. There are some studies based on this topology with different modulation techniques [46,48,61 ,62,63].

CHB inverter systems with transfromers are presented as a solution to one of the major limitations of the cascade multilevel converters which is requirement of isolated dc voltage sources for each H-bridge, which increases the converter cost and reduces the reliability of the system. E.Barcenas et al , proposed a CHB topology that does not require different DC sources, using a single DC source for all the system. On the other hand, it maintains the isolation between the inverter and the system, which output transformers can be coupled for the application of series compensators.Some of the researchers are focused on adjusting the turn-ratios of transformers to achive desired voltage level with less componenet using different modulation techniques to reduce the THD,conduction losses and switching losses [64]. H.Weiss and K.Ince described design and layout of single phase system quasi-eight level PWM inverter system with the transformers' turn ratios of exponent 2 [65]. As an alternative way some of the authors offered a CHB multilevel PWM inverter system with cascaded transformers with turn ratios of exponent 3 to achive more output voltage level [66,67,68].

Also F.S. Kang proposed a system that reduces two-fold the secondary turn ratio of the transformer that is connected to the PWM inverter to reduce witching losses and THD with an efficient switching function [69]. As an alternative way, some studies

are done that subsititutes one of the full-bridge inverter by a half-bridge inverter by this difference they managed to reduce the number of switches and have a high quality output voltage [70,71]. In order to reduce the number of transformers, components size and to trim down the weight, some of the authors used three-phase transformers instead of single-phase transformers in CHB inverter systems [72,73,74,75].

If we look at the studies that employ bi-directinal switches;Yaosuo Xue and Madhav Manjrekar have used the full bridge approach with bidirectional switching method for a single phase with separated DC source, five-level-cascaded inverter [76].

Another work about bidirectional switching method is done by Won-kyun Choi and his coworkers for cascaded H-bridge inverter circuit [77]. Chawki Benboujema et al. compared various types of bidirectional switching methods. In their work they also used MOSFETs as semi-conductor elements within the bidirectional switch circuit for AC applications. The results of their work showed that MOSFETs are advantageous for applications with low voltage and high frequency requirements, whereas IGBTs are the only choice for applications with high voltage requirements [78]. In parallel with the study mentioned above, Benboujema et al. aimed to develop a bidirectional switch system for electricity networks. They compared voltage, current and gain parameters between the Bipolar Junction Transistor (BJT) and Trench Base-Shielded Bipolar Transistor (TBSBT) and determined the advantages and disadvantages of them [79].

With a fault-tolerant control strategy and reconfiguration technique, operation can continue with the undamaged cells; thus increasing the reliability of the system.

Pablo Lezana explained the fault identification methods and hardware modifications that allow for operation in faulty conditions.He asserted that that multilevel inverters can significantly increase their availability and are able to operate even with some faulty components [80].

Christophe Turpin et al. studied the probable faults of hard and soft switching techniques and emphasized that the more the switching elements are the higher the probability of a fault is [81].

Another study on this topic is done by Surin Khomfoi and Leon M. Tolbert, which investigates the feasibility of the fault correction techniques using neural networks.

They claimed that the mathematical modeling of systems having too many switching elements is difficult [82].

Another study on the topic of fault tolerance, the publication of Sergio Daher, is about the shutdowns of the excitation systems due to fault conditions and the cost of these shutdowns [7].

Pablo Barriuso et al. indicated one shortcoming of the asymmetric H-Bridge multilevel inverters scaled by power of three that is the H-Bridges are not interchangeable and under certain faulty conditions the inverter can not operate. They designed a reconfiguration system based on bidirectional electronic valves for three-phase 27-level cascaded H-bridge inverter. Once a fault is detected in any of the insulated gate bipolar transistors of any H-bridge, the control is capable to reconfigure the hardware keeping the higher power bridges in operation. In this way, the faulty phase can continue working at the same voltage level by adjusting its gating signals. The implementation of that proposed scheme may be expensive, but constitutes a very good solution for inverters that cannot be taken out of operation because a failure may mean thousands of dollars of losses or life risk in hospital applications [84].

H. Iman-Eini and his co-workers have asserted that the reliability of multi-level inverters is low because of their high number of semi-conductor elements. This is due to fact that the increasing number of switches also increases the probability of the fault conditions. In their work, an H-bridge cell was added to the CHB rectifier to achieve redundancy and fault tolerant design. The redundant H-bridge concept helps to deal with device failures and to increase system reliability [43].

Surin Khomfoi et al. researched the fault correction methods for hybrid cascaded multilevel inverter used in renewable energy systems. For this purpose, they first used simulation programs such as PSIM and MATLAB, and then they designed an experimental layout and tested the efficiency of the overall system [85].

Nasim RASHIDI et al. studied the reliability of modular inverters with Half-Bridge and Full-Bridge cells. They used Markov Chain to calculate their reliability which models a sequence of random variables. They compared the HB anf FB cells and asserted that modular inverters with HB cells will have a better reliability compared to the inverters with FB cells [83].

3. PROPOSED MULTILEVEL INVERTER SYSTEM DESIGN

In this chapter, the proposed inverter system, the fundamental working principles and main duties of each system unit are explained in detail.

H. Weiss and K. Ince, designed and experimentally tested a Quasi-eight level cascaded H-bridge inverter with output-side transformers for a single-phase off-grid system. They proved that their inverter system has very low THD when compared with the classic two level inverter and other multilevel inverter configurations. The schematic view of this system for laboratory model is shown in Figure 3.1 [65].

In Weiss and Ince's system, all H-Bridge inverters are identical and fed by a single DC source. Each H-Bridge inverter's output is connected to its own transformer module with the turns-ratios of 1:1, 1:2, 1:4, respectively. The secondary sides of the transformers connected in series to sum up all the voltages transferred to the load. Totally, the designed laboratory model includes seven transformers. Finally, this system achieves 8 level voltages (including zero voltage level) in quarter cycle at the output stage.

This study, offers a fault-tolerant system design and application of reconfiguration technique based on quasi-eight level inverter system mentioned above. The general schematic view of proposed topology is shown in Figure 3.2. In proposed system, reconfiguration technique is achieved by changing two multi-winding transformers' and one linear transformer's turns-ratios by the aid bi-directional switches and by changing the modulation techniques of the H-Bridge inverter modules at fault instants.

At normal operation mode (when no fault exists), this inverter has 15 levels; seven positive level, seven negative level and zero level as shown in Figure 3.3. At fault instants, the voltage level of the system is decreased one level in quarter period but system continues feeding the load without stopping the system. This topology is simulated and verified in MATLAB-SIMULINK simulation environment. All of the main parts of the proposed system are presented in detail.

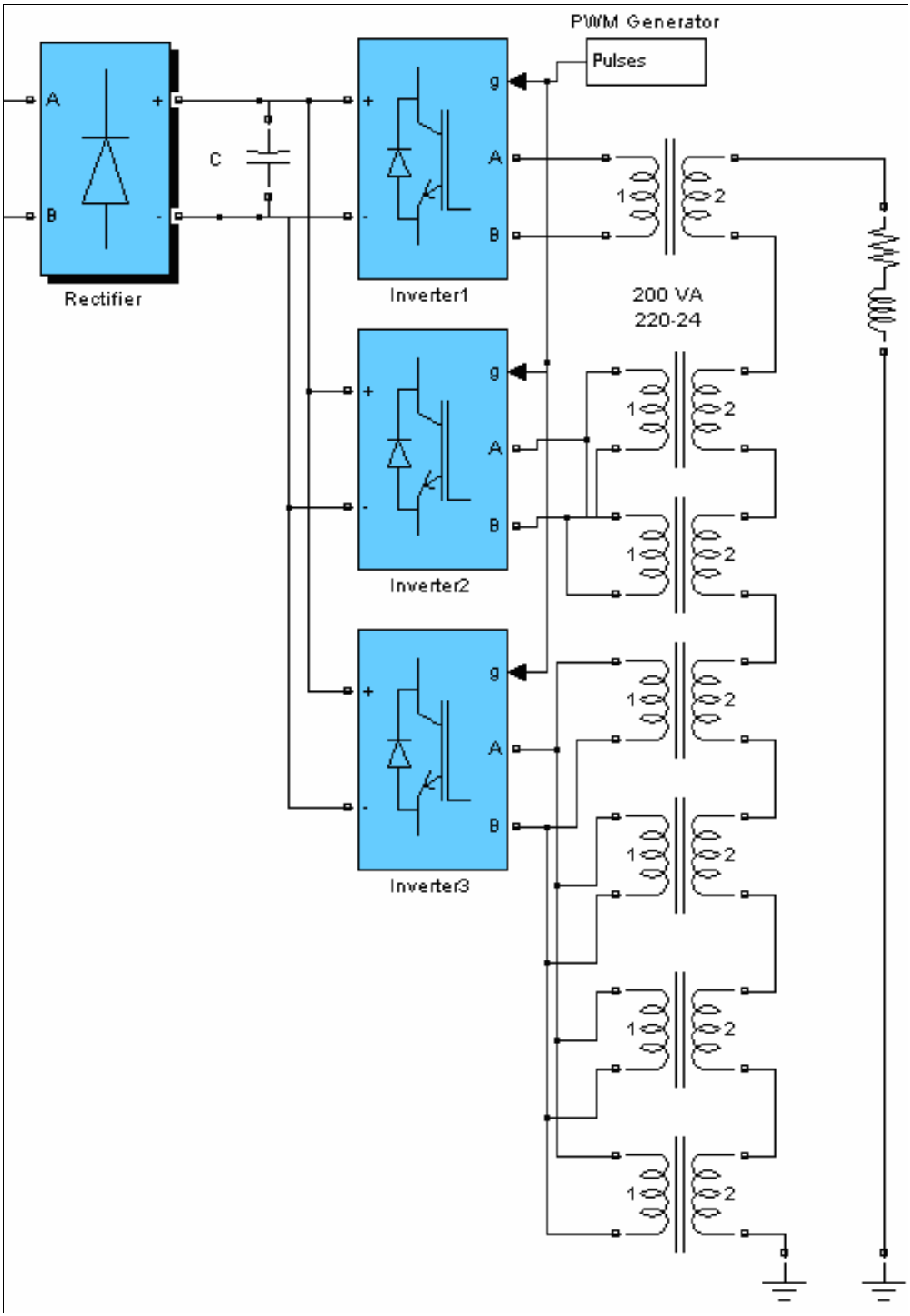


Figure 3.1 : Laboratory model of Quasi-Eight level inverter system [65].

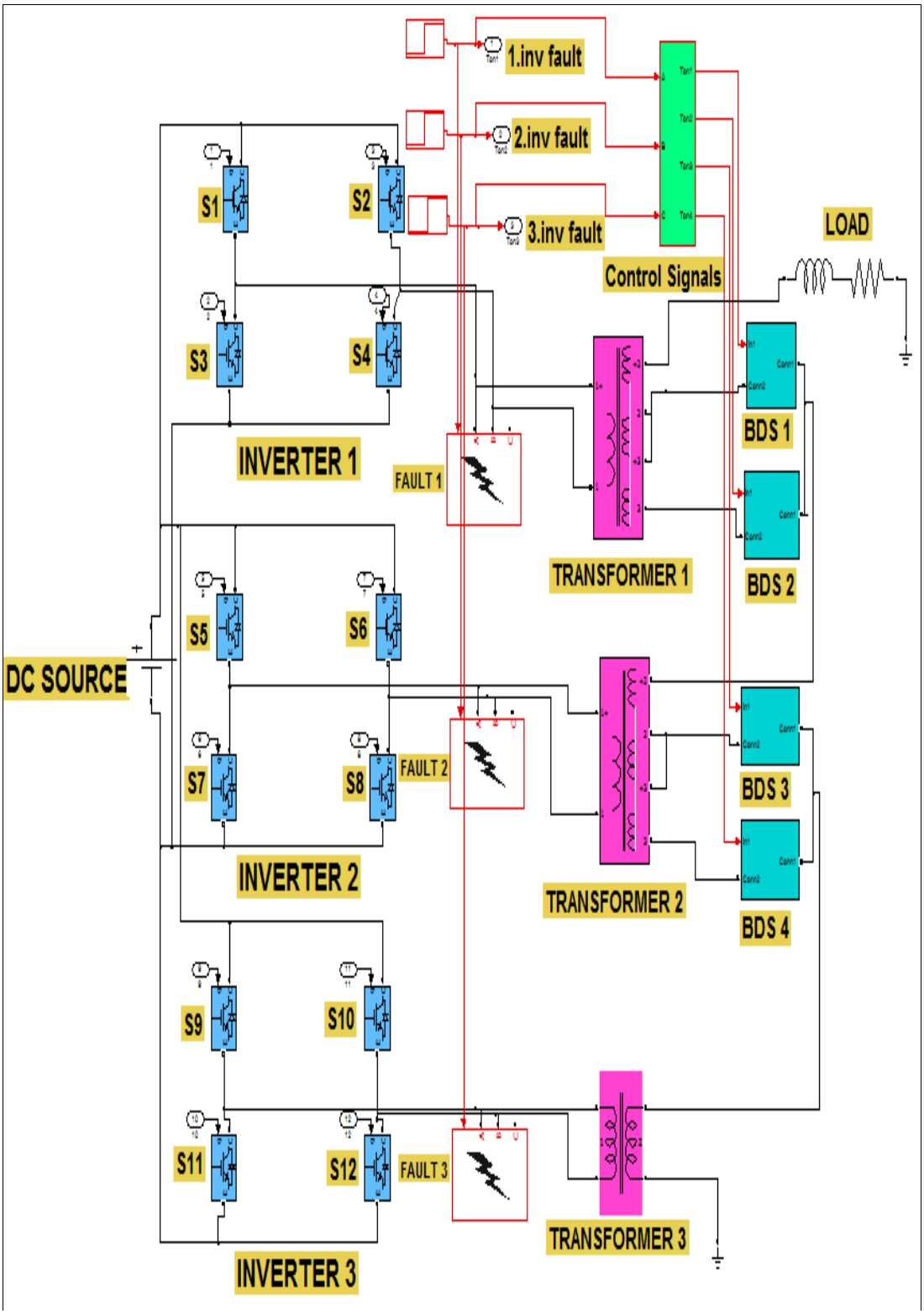


Figure 3.2 : Proposed multilevel inverter topology.

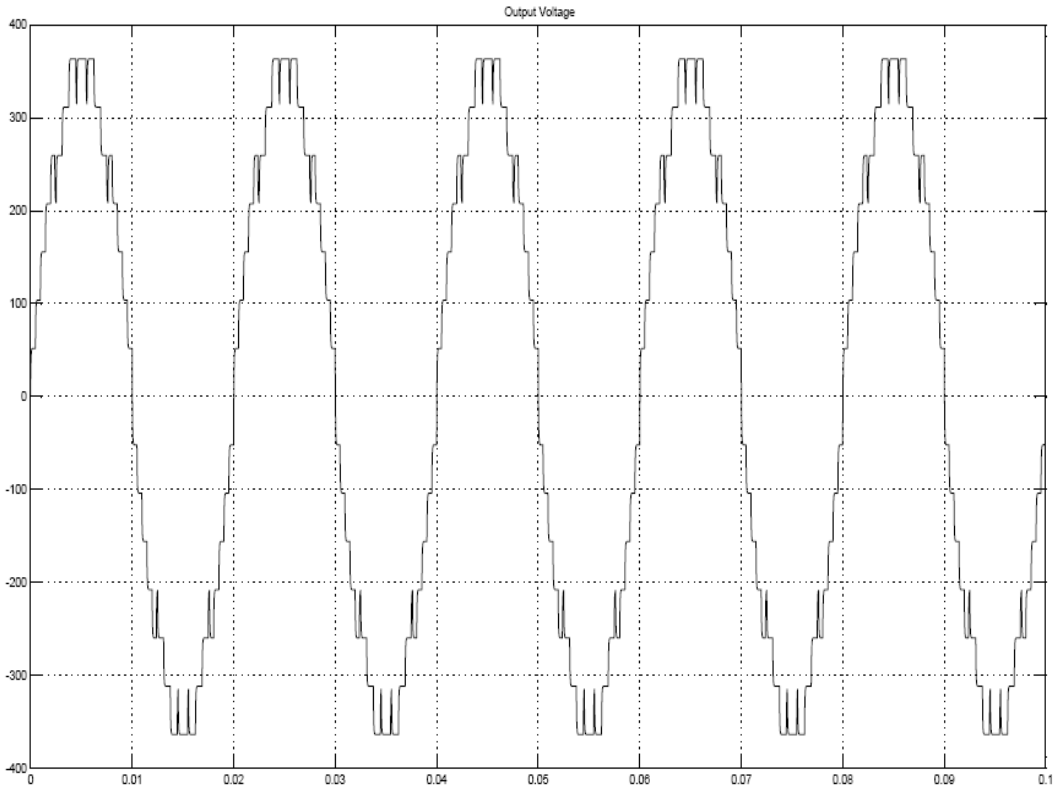


Figure 3.3 : Quasi-8-level inverter's output voltage.

3.1 System Components

This system consists of single DC source, three H-Bridge inverter stages, one fault detection element for per H-Bridge stage, two multi-winding and one linear transformer, four bi-directional switches and load unit.

3.1.1 H-Bridge inverter modules

The system is established on the base of three identical H-Bridge inverter modules which are fed by a 52V DC source. Each stage is identical which makes the system modular. The only difference between these stages is modulation technique.

One of the H-Bridge modules is shown in figure 3.4. It is composed of four semiconductor devices. In this configuration, the IGBT-Diode module is selected, because the system's switching frequency is not very high and it is suitable for the power level of the system.

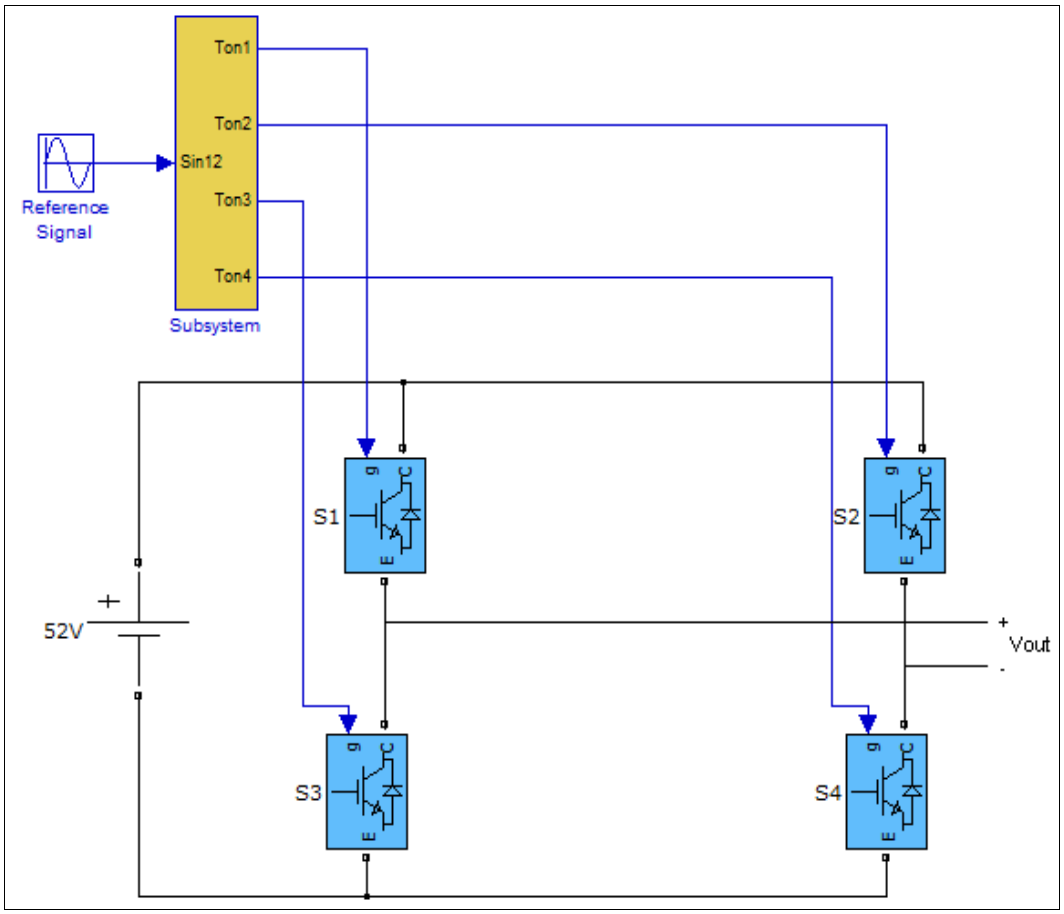


Figure 3.4 : Typical H-Bridge inverter module.

Each H-Bridge inverter module can produce +52V, -52V and 0 voltage at the output (Vout) according to the states of the switches. In order to produce +52V output voltage; the switches S1 and S4 must be in ON state while other switches are in OFF state. Controversially, to produce -52V; S2 and S3 must be conducting while other switches are non-conducted. There are two ways to achieve 0 voltage at the output of the inverter module. These are;

- S1 and S2 must be in ON state while other switches S3 and S4 are in OFF mode.
- S3 and S4 must be in ON state while other switches S1 and S2 are in OFF mode.

The working principle of the H-Bridge module is summarized in Table 3.1

Table 3.1 : Output voltage according to the switch states.

Output Voltage (V_o)	Switches' States			
	S1	**S2**	**S3**	**S4**
+52 (V)	1	0	0	1
-52 (V)	0	1	1	0
0 (V)	1	1	0	0
0 (V)	0	0	1	1

The simulation parameters for the IGBT-Diode devices are presented in Table 3.2.

Table 3.2 : Simulation parameters for the IGBT-Diode devices.

Simulation Parameters	Value
Internal resistance (Ω)	0.001
Snubber resistance (Ω)	10^{-5}
Snubber capacitance (F)	∞

When the levels of the inverter are increased, the number of H-Bridge modules must be increased. As a result, the number of semiconductors in the system is increased, too. This situation increases the probability of any fault in the system. However, H-Bridge modules are galvanically isolated from each other that make the system more reliable. A fault in any of the H-Bridge module does not affect the other modules. By using this advantage of the system, a fault tolerant system is designed and introduced in depth later in this chapter.

3.1.2 Transformers and bi-directional switches

In the proposed inverter system, each H-Bridge module is connected to a transformer. The objectives of using the transformers in the systems are;

- To achieve galvanic isolation between input and output stages.
- To avoid using separate DC sources.
- While primary sides of the transformers are parallel-connected to the output of H-Bridge modules, the secondary windings are connected serially to each other to sum up the produced voltages in H-bridge modules. By adjusting the turn ratios of the transformers to suitable values, more voltage levels can be obtained at the load.
- The use of multi-winding transformers and bi-directional switches allows us to reconfigure the system at fault instants by changing the turns-ratios of the

transformers. In addition, by appropriate switching patterns the system can stay at acceptable voltage levels.

The turns-ratios and some parameters of transformers are different from each other. The transformer that is connected to first H-Bridge module has turns ratio of 1:1/2, which means when no fault exists in the system this transformer has turns ratio of 1:1. However, when a fault occurs at one of any other H-Bridge inverter modules, the turns-ratio of the transformer is changed to 1:2. The equivalent circuit of the used transformer is shown in Figure 3.5, and its parameters are presented in Table 3.3.

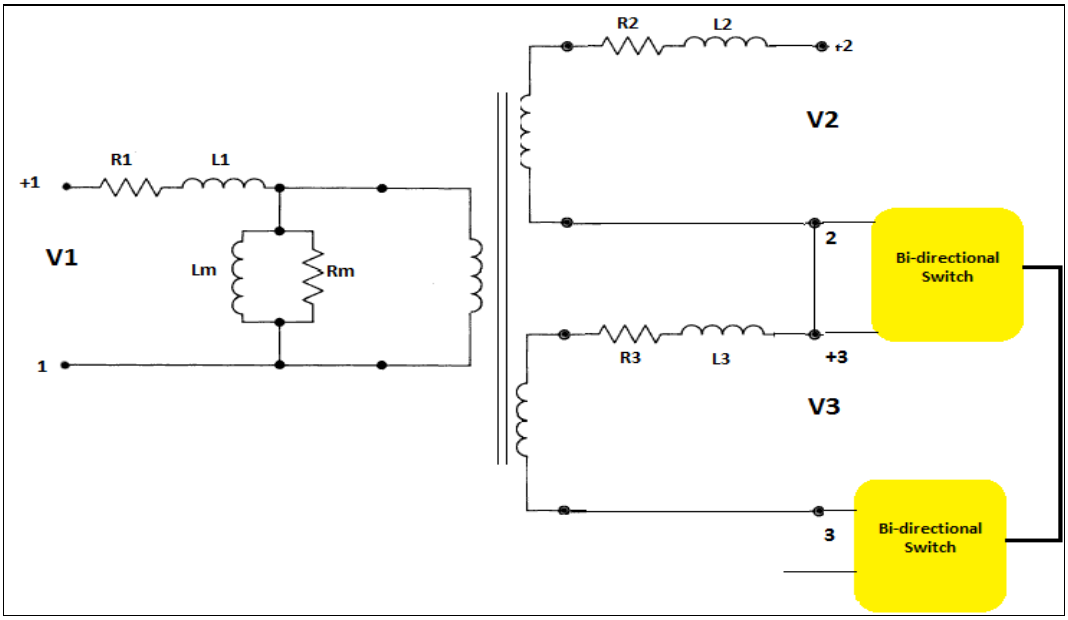


Figure 3.5 : Equivalent circuit of transformer connected to the output of first inverter.

The simulation parameters of the first transformer are given in SI units and per units (pu). The transformation from SI units to pu units can be done easily for the transformers by these formulas:

$$Z_{base} = R_{base} = X_{base} = \frac{(V_n)^2}{P_n} \quad \textbf{(3.1)}$$

$$L_{base} = \frac{X_{base}}{2\pi f} \quad \textbf{(3.2)}$$

$$R(pu) = \frac{R(\Omega)}{R_{base}} \quad \textbf{(3.3)}$$

$$L(pu) = \frac{L(H)}{L_{base}} \quad \textbf{(3.4)}$$

Table 3.3 : Simulation parameters of the first inverter's transformer.

Simulation Parameters	**Units**	
	SI	**Per Unit(pu)**
Nominal Power (VA)	1000	-
Frequency (Hz)	50	-
Winding Nominal Voltages-V1,V2,V3 (Vrms)	480 , 480 , 480	-
Winding Resistances-R1,R2,R3 (mohm)	3.68 , 3.68 , 3.68	$1.6x10^{-5}$
Winding Leakage Inductance-L1, L2, L3 (mH)	0.938 , 0.938 , 0.938	$128x10^{-5}$
Magnetization Resistance (Mohm)	1.152	5000
Magnetization Inductance (H)	3666.5	5000

The transformer connected to the second H-Bridge inverter has turn ratio of 1:2/4 whose equivalent circuit is same with the first transformer's circuit. However, the parameters of the transformer are different from first transformer's that is presented in Table 3.4.

Table 3.4 : Simulation parameters of the second transformer.

Simulation Parameters	**Units**	
	SI	**Per Unit(pu)**
Nominal Power (VA)	2000	-
Frequency (Hz)	50	-
Winding Nominal Voltages-V1,V2,V3 (Vrms)	480,960,960	-
Winding Resistances-R1,R2,R3 (mohm)	3.68, 1.47, 1.47	$3,2x10^{-5}$
Winding Leakage Inductance-L1, L2, L3 (mH)	0.469, 1.87,1.87	$128x10^{-5}$
Magnetization Resistance (Mohm)	0.576	5000
Magnetization Inductance (H)	1833.46	5000

The third and last H-Bridge inverter's transformer has turn ratio of 1:4 which is constant all the time, so this transformer is considered as linear transformer. Its

equivalent circuit and parameters are shown in Figure 3.6 and Table 3.5, respectively.

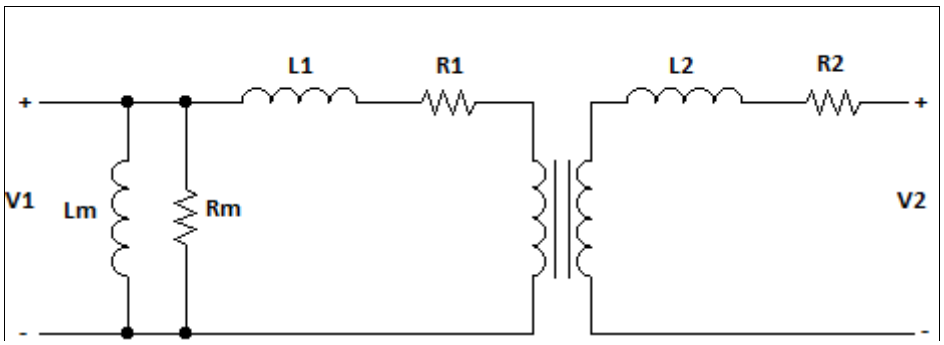


Figure 3.6: Equivalent circuit of third H-Bridge inverter's transformer.

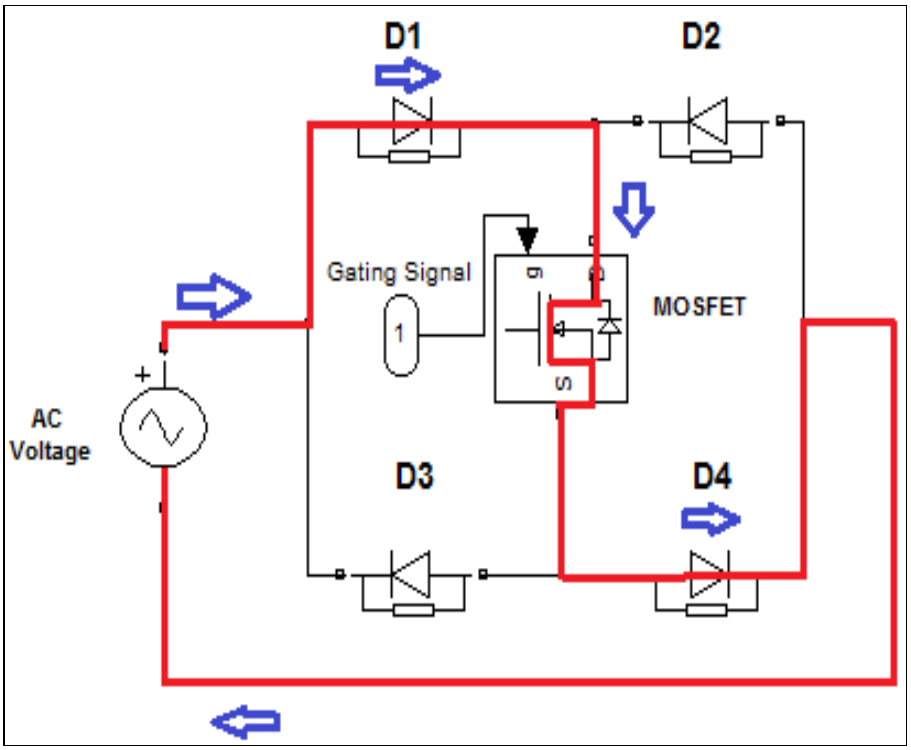
Table 3.5: Parameters of the third inverter.

Simulation Parameters	Units	
	SI	Per Unit(pu)
Nominal Power (VA)	2000	-
Frequency (Hz)	50	-
Winding Nominal Voltages- V1 ,V2 (Vrms)	480 , 1920	-
Winding Resistances-R1, R2 (mohm)	3.68 , 58.98	$3{,}2x10^{-5}$
Winding Leakage Inductance- L1, L2 (mH)	0.46 , 7.5	$128x10^{-5}$
Magnetization Resistance (Mohm)	0.576	5000
Magnetization Inductance (H)	1833.5	5000

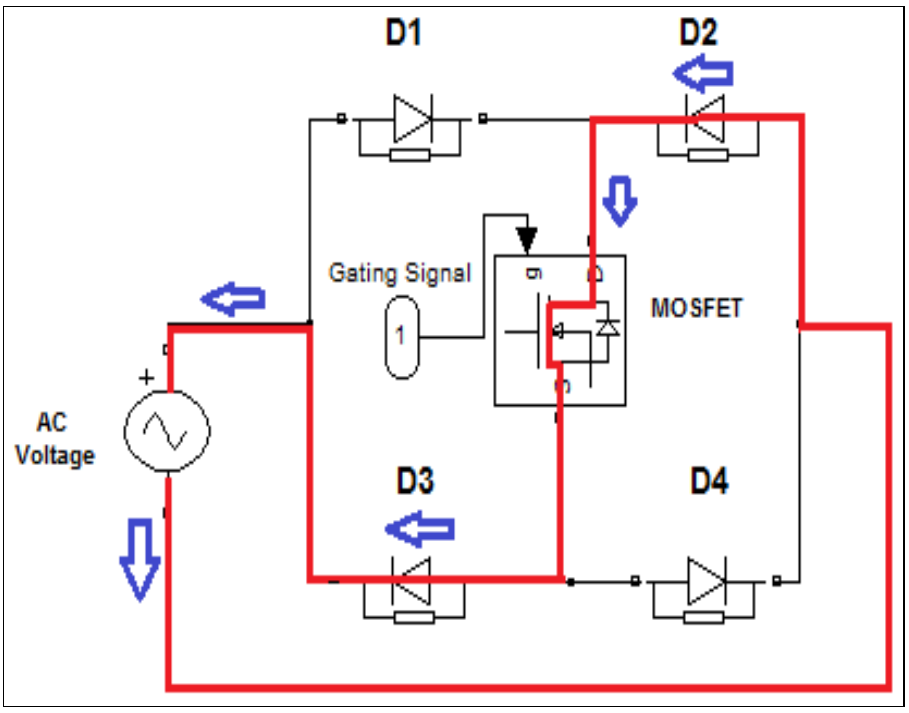
The bi-directional switches in the proposed system plays a key role which provides an opportunity to design a fault tolerant system and application of reconfiguration technique. The BDSs are connected to the output of the transformers so they act like being fed by AC voltage source. The BDS is also called as "AC Switch". In this thesis, two types of MOSFET based bi-directional switches are tested and compared in the simulation environment. These are:

- Diode Bridge MOSFET BDS (DB-MOSFET-BDS)
- Common-Source MOSFETs BDS (CS-MOSFET-BDS)

Diode Bridge MOSFET BDS is formed of four diodes and one n-channel MOSFET. According to the sign of alternation the current flow path is changed which provides bi-directional power flow. First of all, MOSFET must be in ON state for power flow. If the applied voltage is bigger than 0, the current follows the way; D1-MOSFET-D4 and, if it is less than 0, the current flows through D2-MOSFET-D3, as shown in Figure 3.7. At both conditions, current flows through two diodes and one MOSFET. The power dissipation can be calculated for this BDS by the formula;



(a)



(b)

Figure 3.7: Diode-Bridge MOSFET BDS current flow paths at a)Positive alternation b)Negative alternation.

$$P_{diss} = [(2 * R_d + R_{on}] * I_{BDS}{}^2 \quad \textbf{(3.5)}$$

Where R_d is the diodes internal resistance, R_{on} is MOSFET's ON state resistance and I_{BDS} current flowing in the circuit.

Common Source BDS only consists of two n-channel MOSFETs. Their source terminals are connected to each other. At positive and negative alternations, a current flows through one MOSFETs Drain-Source terminal and other MOSFETs internal diode as shown in Figure 3.8. The power dissipation over this type of switch can be expressed as;

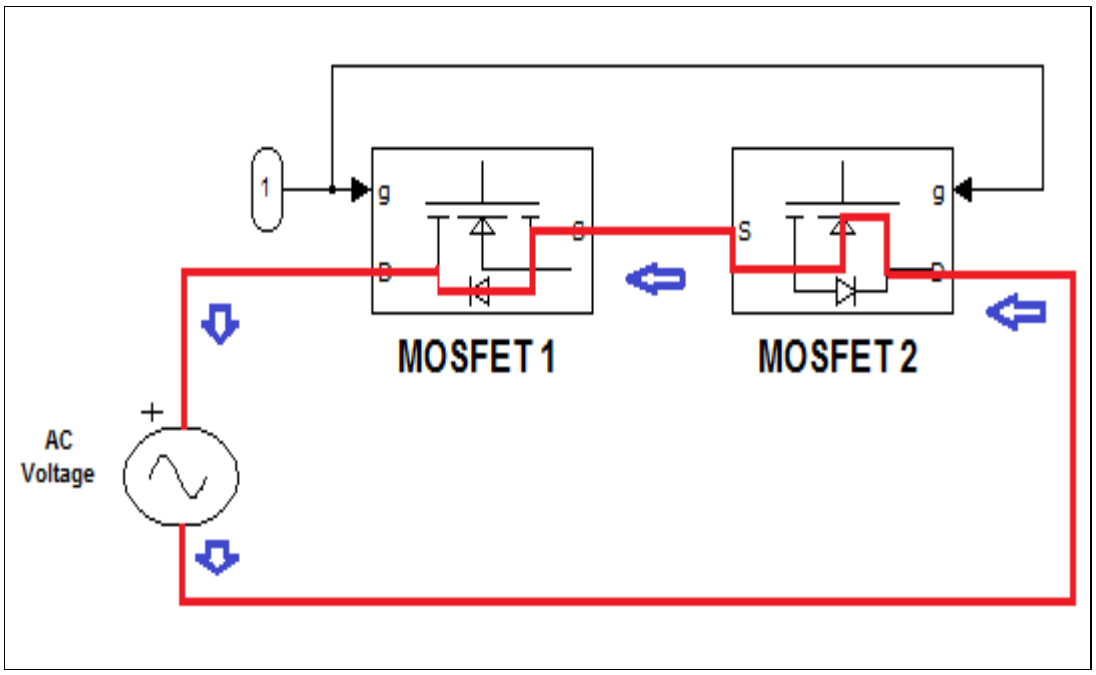
$$P_{diss} = [(R_{d-\text{int}} + R_{on})] * I_{BDS}{}^2 \quad \textbf{(3.6)}$$

where $R_{d\text{-int}}$ denotes the internal diode resistance of the MOSFETs. The power dissipation is decreased about four times when compared with the diode-bridge MOSFET BDS. Moreover number of components decreased to 2. The number of MOSFETs is doubled, so the price increases.

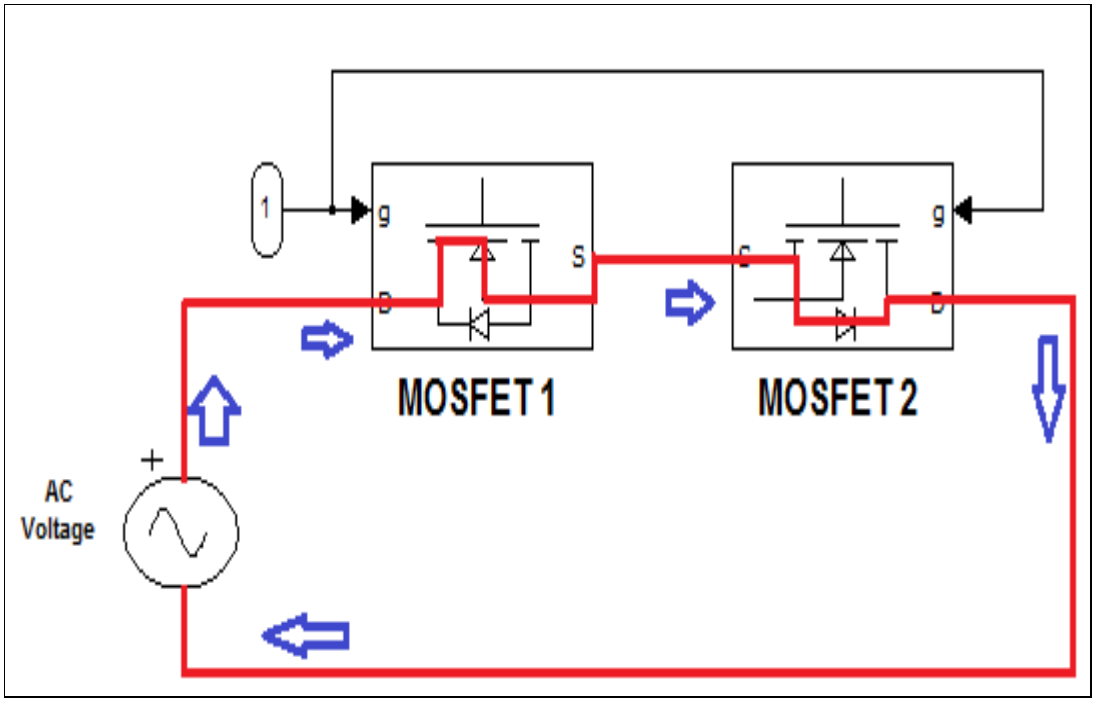
By taking the advantage of MOSFET's high switching frequency ability, we can quickly apply reconfiguration technique if a fault occurs in the system. The simulation parameters for the MOSFETs of the bi-directional switches are shown in Table 3.6.

Table 3.6 : Simulation parameters of MOSFETs

Simulation Parameters	**Value**
FET Resistance (Ω)	0.005
Internal Diode Resistance (Ω)	0.001
Internal Diode Inductance (H)	0
Internal Diode Forward Voltage (V)	0
Initial Current (A)	0
Snubber Resistance (Ω)	10^{-5}
Snubber Capacitance (F)	∞



(a)



(b)

Figure 3.8 : Common Source MOSFETs BDS current flow paths at

a)Positive alternation b)Negative alternation.

3.2 Fault -Tolerant Inverter System and Application of Reconfiguration Technique

The proposed system works under four different modes according to the fault conditions. When a fault exists in the system, the modulation techniques of H-Bridge inverters are changed and by the aid of bi-directional switches the turns-ratios of the transformers are reconfigured to hold the system at desired voltage level. At all modes one H-Bridge inverter module is modulated by PWM technique. The system is presented in two main parts:

- Normal Operation Mode
- Fault Condition Modes

3.2.1 Normal operation (no-fault) mode

This mode is valid when no fault exists in the system that is shown in Figure 3.9. The system keeps working at this mode until a fault occurred in the system. In this mode the system produces 8 voltage levels in quarter cycle including zero voltage level , and totally system has 15 voltage levels at the load. The turns-ratios of the transformers are 1:1, 1:2, 1:4, respectively. In order to have these turns-ratios the bi-directional switches BDS1 and BDS3 must be conducted while BDS2 and BDS4 are non-conducted.

The modulation techniques for H-Bridge modules are different from each other. The hybrid modulation technique is applied for the system. While high switching frequency (1-20 kHz) PWM is applied to the first H-Bridge inverter, other two inverters are modulated at low switching frequencies.

The first H-Bridge inverter module is modulated by sine-triangle PWM technique. The fundamental idea of this technique is, comparison of desired voltage waveform (sine) with carrier waveforms (triangular) and according to the comparison results producing gating signals for the semiconductor devices. The sine wave is compared with positive side triangular wave and negative side triangular wave separately to control left side and right side switches, respectively. As a result, a 3-level PWM signal can be generated with high, low, and zero voltage levels. The compared

signals are shown in Figure 3.10. The control signals that sent to the gates of the IGBTs of the first inverter is shown in Figure 3.11 where Ton1 is denotes the gating signal of S1, and the other signals are likewise. The voltage produced at the output terminal of the first inverter is shown in Figure 3.12.

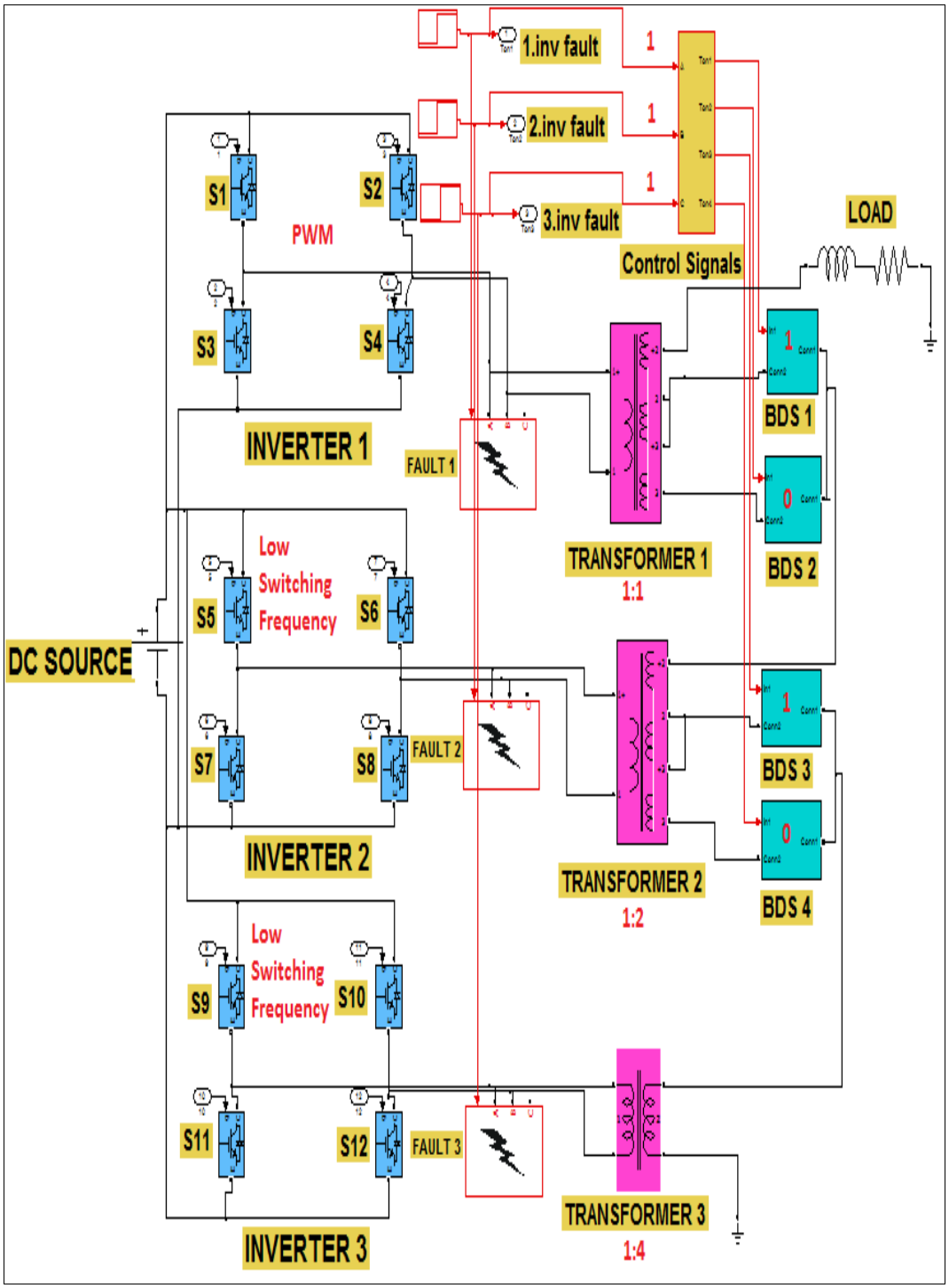


Figure 3.9 : The proposed inverter when no fault exists.

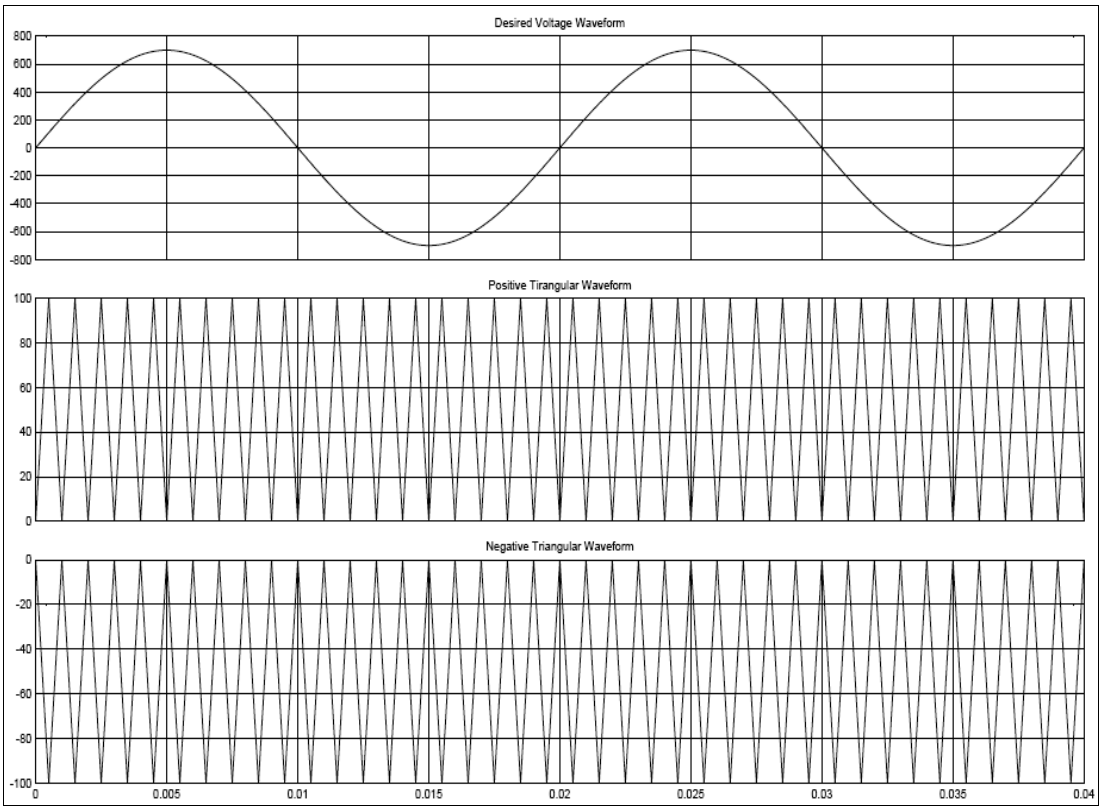


Figure 3.10 : Compared signals for PWM.

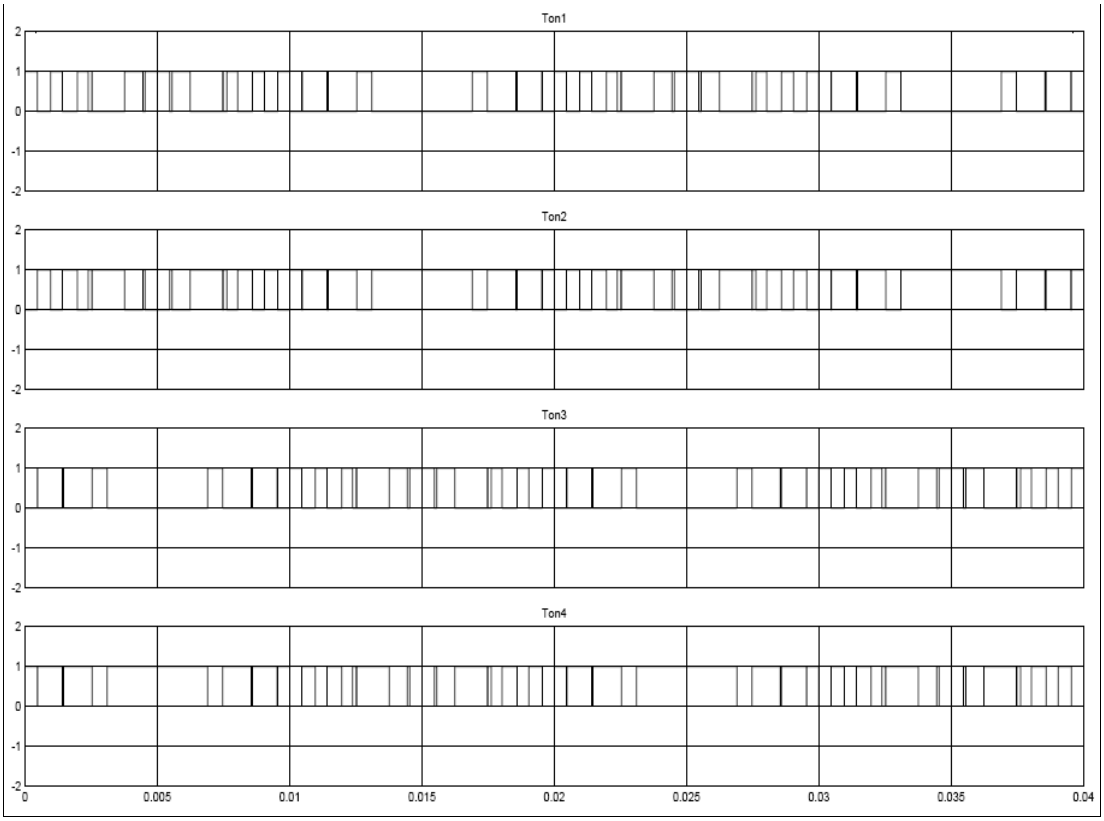


Figure 3.11 : The compared signal for production of PWM signal (fc=1000Hz and fm=50Hz).

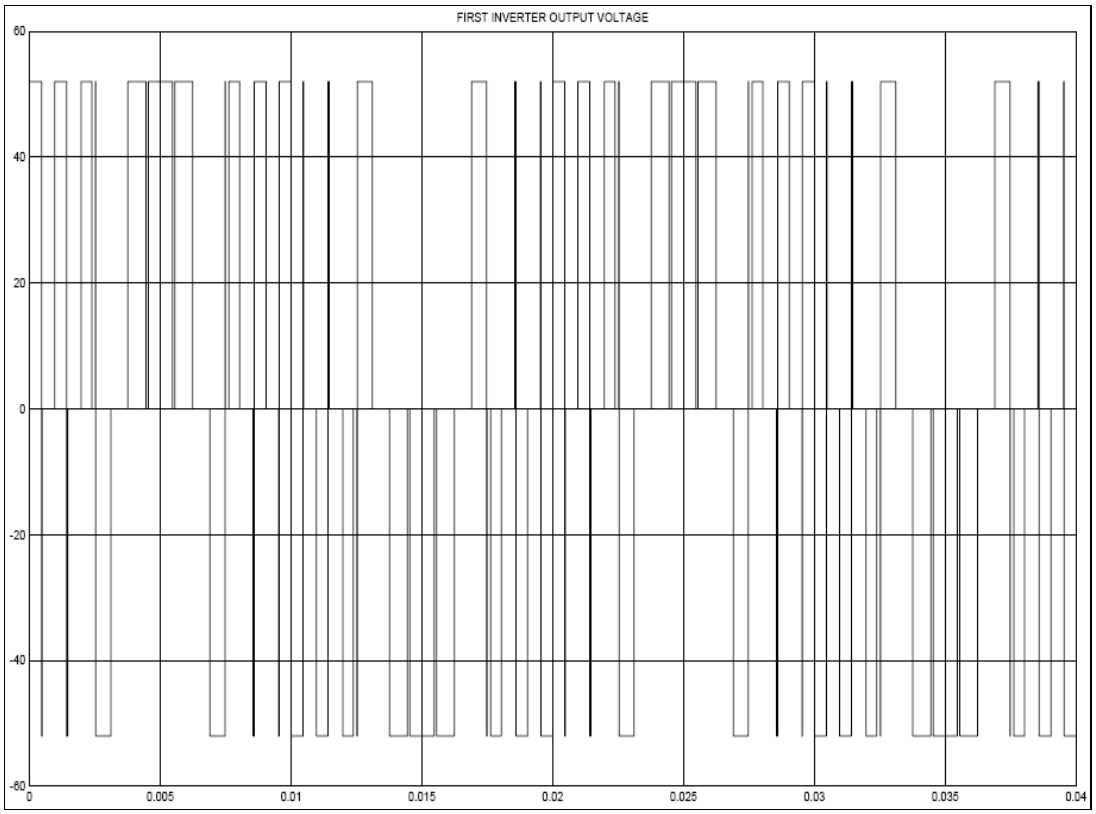


Figure 3.12 : The output voltage of the first inverter (fc=1000Hz).

If the sine wave is greater than the positive side triangular wave, the switches S1 and S4 conducts while S2 and S3 are in OFF state. If it is smaller, S1 turns OFF S3 turns ON and 0 voltage is achieved at the output.

If the sine wave is smaller than negative side triangular wave,S2 and S3 conducts while other switches are in OFF state to produce -52V.If it is greater,S2 turns off and S4 turns on to produce 0 voltage at the output. All of these switching functions are summarized in Table 3.7. In this table U_{sin} denotes the value of sine wave at any instant, while Ut_{+} and Ut_{-} represents the value of positive side triangular wave and negative side triangular wave, respectively.

Table 3.7 : PWM switching functions up to comparing conditions.

	Left Side Switches		**Right Side Switches**	
Conditions	**s1**	**s3**	**s2**	**s4**
Usin>Ut_{+}	1	0	0	1
Usin<Ut_{+}	0	1	0	1
Usin>Ut_{-}	0	1	0	1
Usin<Ut_{-}	0	1	1	0

The important parameters for the PWM technique are amplitude modulation index (Ma) and frequency modulation index can be defined as;

$$M_a = \frac{V(\sin)_{peak}}{V(triangle)_{peak}} \quad \textbf{(3.7)}$$

$$M_f = \frac{f_c}{f_m} \quad \textbf{(3.8)}$$

where fc denotes the frequency of the triangular wave and fm denotes the frequency of sine wave. The frequency of sine wave is 50Hz and carrier frequency is selected between 1 kHz and 20 kHz in simulations. In this work, amplitude modulation index is selected as 1.

This inverter is connected to a transformer which has turns ratio of 1:1 which means at normal operation mode one level PWM technique is applied. This modulation is technique is used to achieve better shaped output voltage (closer to the sine wave) with low total harmonic distortion (THD). Main objective of this inverter is to improve output voltage rather than energy transfer.

In order to reduce the conduction losses, the two inverters are modulated at low frequencies. Their main purposes are identified as setting a voltage ground for the PWM inverter. In one period; the second inverter conducts three times in positive direction and three times in negative direction like displayed in Figure 3.13. The second inverter is connected to a transformer with the turns ratio of 1:2 which means in a quarter periods this inverter is responsible for producing two voltage levels at the output side.

The third inverter conducts one time in positive direction and one time in negative direction as presented in Figure 3.14. This inverter feeds the transformer with the turn ratio of 1:4, responsible for producing four voltage levels in a quarter cycles at the output. Its main duty is power transfer rather than improving the output voltage.

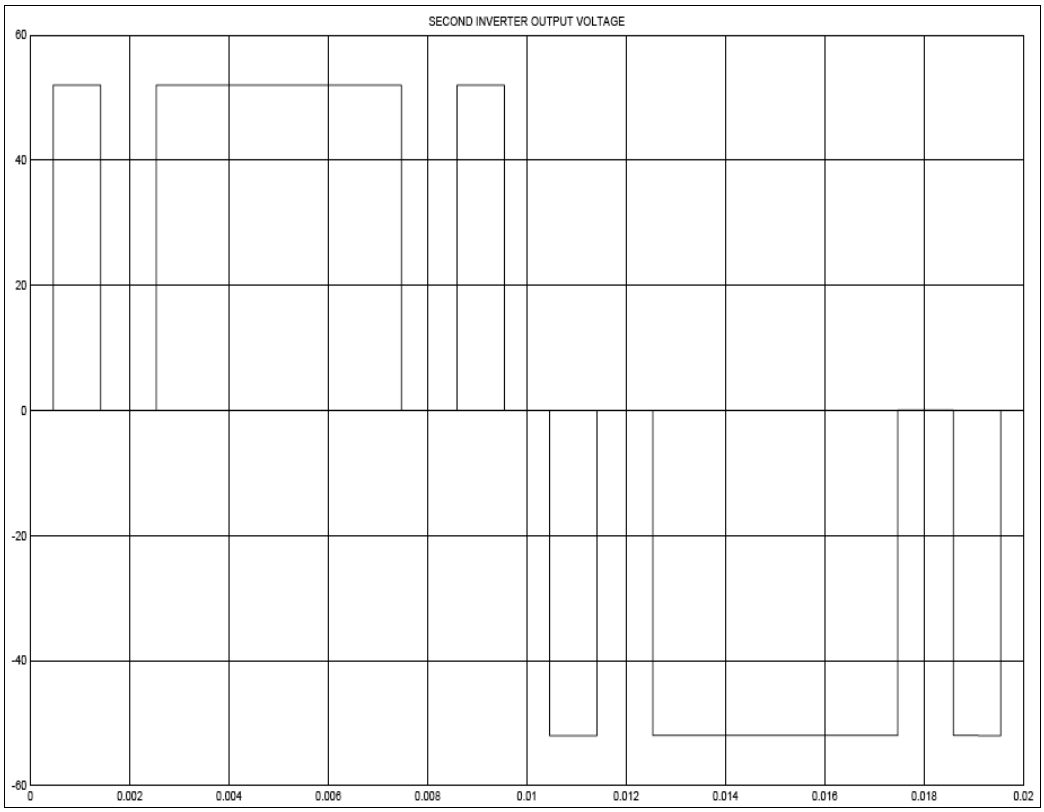


Figure 3.13 : The output voltage of the second inverter (f=150Hz).

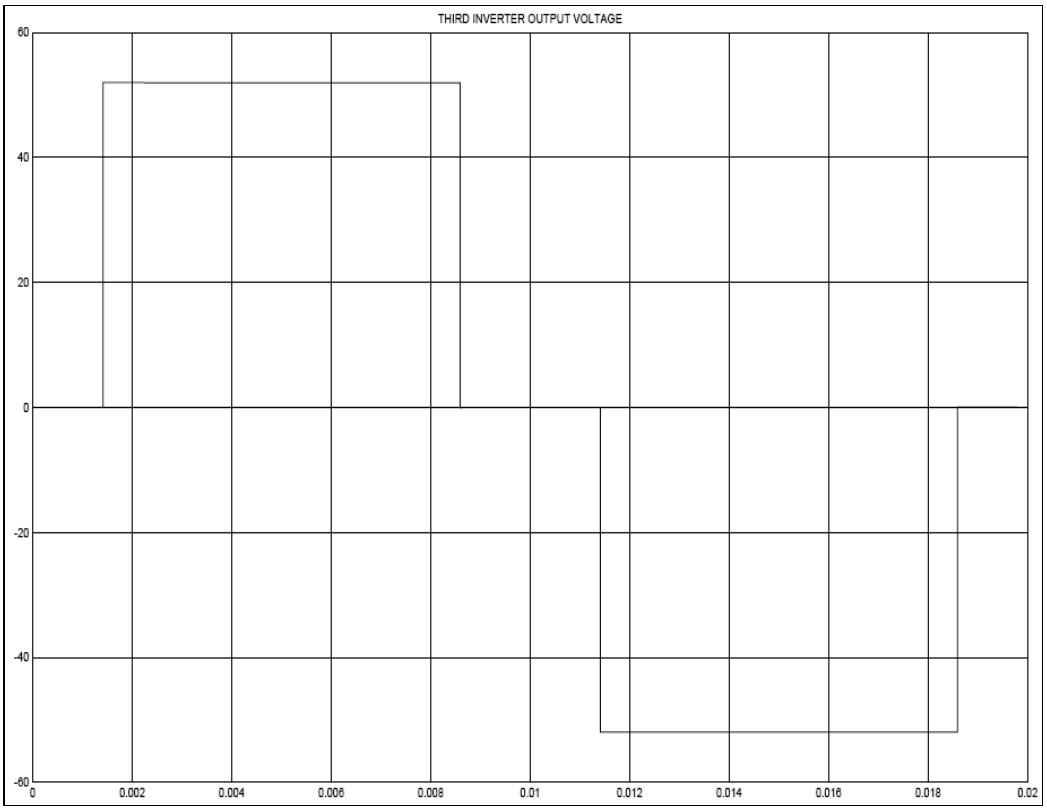


Figure 3.14 : The output voltage of the third inverter (f=50Hz).

The power imposed on each transformer is directly depends on the secondary parameter sof turns-ratio of cascaded transformers[66]. Therefore, power distribution for each transformer can be specified by the rate of secondary windings and formulized by

$$P_{TR,n} = \frac{T_{\text{turns,secondary}}}{\sum_{n=1}^{k} T_{\text{turns,secondary}}} \times 100 \qquad \textbf{(3.9)}$$

where $T_{\text{turn,secondary}}$ denotes the secondary parameter of turns-ratio of each transformer and k connotes the number of transformers. When no fault exists in the system, the percentage of power transferred via first inverter is can be calculated as P_{tr1}=1/(1+2+4)x100= 14.28%. Similarly, the percentage power transferred via second and third inverters are 28.57% and 57.14%, respectively. In order to achieve high efficiency, lower power distribution imposed on first transformer connected to PWM inverter by the reason that it operates at high frequency.

3.2.2 Fault conditions

Fault-tolerant system is designed for when only one H-Bridge inverter has a fault at any instant. When two or more H-bridge inverter have faults, the reconfiguration technique can not be applied. At fault conditions, the voltage level is reduced from seven level to six level in quarter period so we have 13 level inverter in one period. The proposed system requires $230V_{rms}$ output voltage and with the limit of ±10% of this voltage can be acceptable. In order to supply this voltage ratings under fault conditions, this limit is used.

The bi-directional switches stay as the most important of the proposed inverter system. These switches used for changing the secondary turn-ratio of the transformers to system keep working with acceptable voltage level. In addition, by the control system modulation techniques of the inverters are changed at fault conditions.

The BDS' states according to the fault conditions of H-Bridge inverters are shown in Table 3.8. In this table "X" means "don't care", "1" means that the switch is in conduction state, and "0" means the switch is in "OFF" state.

Table 3.8 : Bi-directional switches' states up to the fault conditions.

Fault-Condition			**Bi-directional Switches' States**			
First Inverter Has Fault?(A)	***Second Inverter Has Fault?(B)***	***Third Inverter Has Fault?(C)***	***BDS 1***	***BDS 2***	***BDS 3***	***BDS 4***
YES	YES	YES	X	X	X	X
YES	YES	NO	X	X	X	X
YES	NO	YES	X	X	X	X
NO	YES	YES	X	X	X	X
YES	NO	NO	1	0	1	0
NO	YES	NO	0	1	1	0
NO	NO	YES	0	1	0	1
NO	NO	NO	1	0	1	0

According to this table, Boolean algebraic presentation of the gating signals for BDSs can be shown as;

$$BDS1 = (B \wedge C) \quad \textbf{(3.10)}$$

$$BDS2 = \neg(B \wedge C) \quad \textbf{(3.11)}$$

$$BDS3 = \neg((A \wedge B)\neg C) \quad \textbf{(3.12)}$$

$$BDS4 = (A \wedge B) \wedge \neg C \quad \textbf{(3.13)}$$

where "Λ" and " ┐" denotes the digital operators "AND" and "NOT", in order. Moreover, simulation circuit for these signals is shown in Figure 3.15.

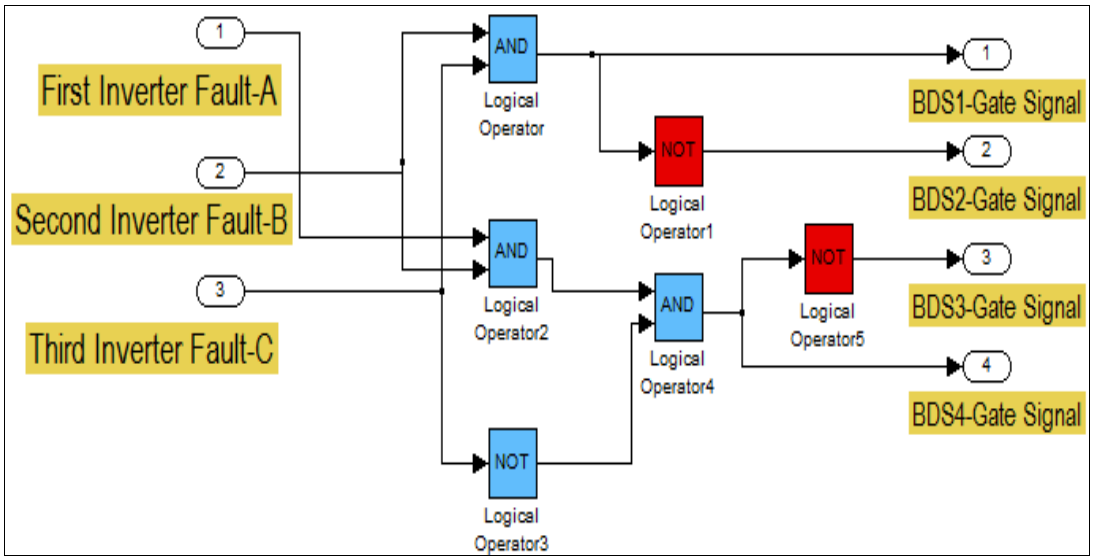


Figure 3.15 : The simulation circuits of gating signals of the BDSs.

3.2.2.1 First inverter fault

When a fault occurs in first inverter, this inverter no longer can not contribute any voltage to the output voltage. Hence, the modulation techniques and turn-ratios of the other inverters must be changed to achieve sufficient output voltage and acceptable THD value. In order to get smaller THD the modulation technique, the PWM modulation technique is transferred to second inverter while its transformer's turn ratio stays unchanged. Now, the second inverter is responsible for two-level PWM signals production.

The third inverter's modulation technique and its transformer's turn ratio stays as usual. Also, the states of the BDSs are not changed, because the turn ratios of the inverters are not changed. The schematic view of the proposed multilevel inverter at first inverter fault condition is shown in Figure 3.16.

At first invert fault, power distribution of the transformers are also changed. The total transferred power is shared between second and third inverter. At this time, the percentage power transferred via second inverter and third inverter becomes 33.3% and 66.7%, respectively. By the reason of this, the nominal power of the transformers are selected a bit high to meet the required power rate at fault instants.

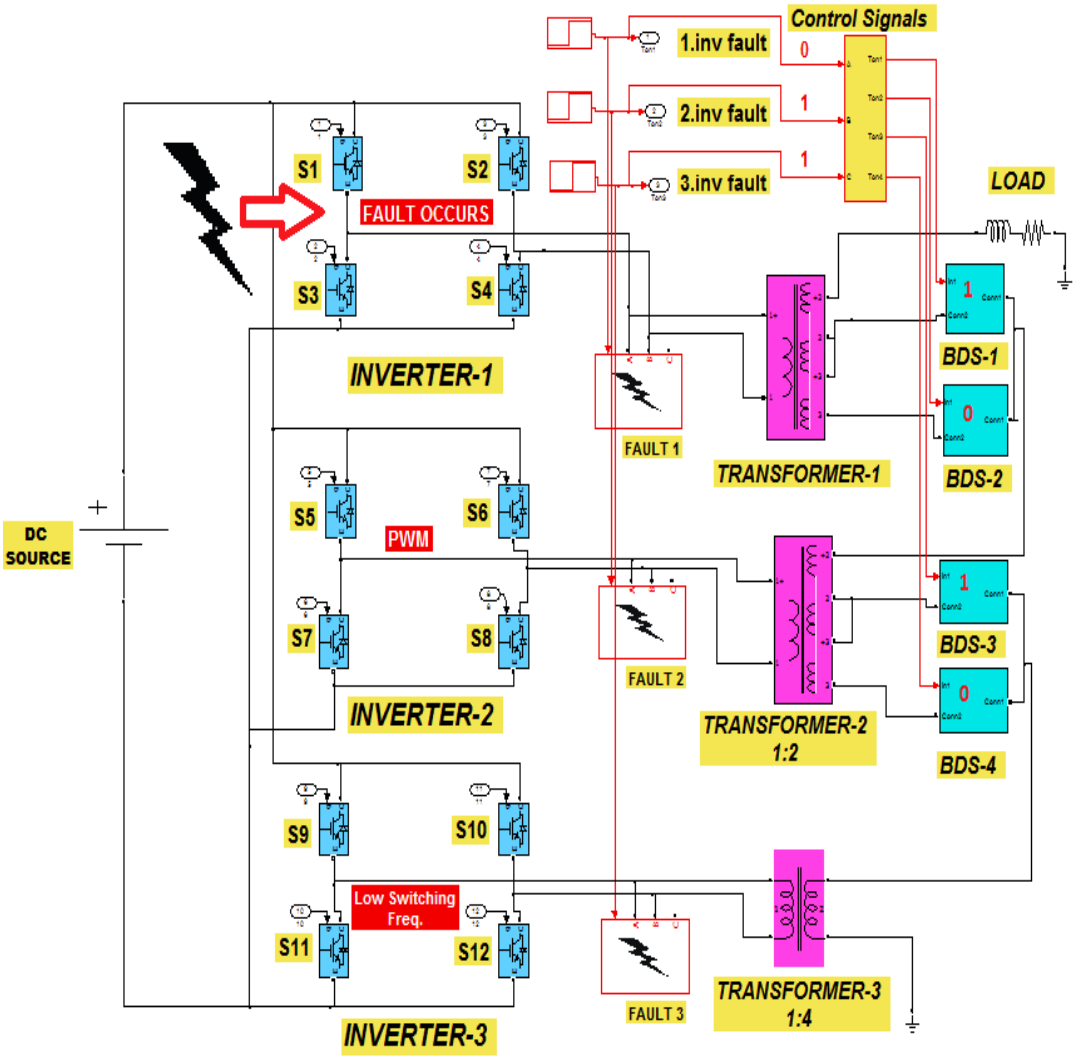


Figure 3.16 : Proposed multilevel inverter when a fault exists in the first inverter.

3.2.2.2 Second inverter fault

When a fault occurs in the second inverter, the same idea of reconfiguration technique works again. The first inverter's turn ratio is changed to the 1:2 by the aid of BDSs. The BDS1 turns to OFF state and BDS2 turns to ON, while BDS3 and BDS4 are hold their own states. Now the first inverter is responsible for 2 level voltage production with PWM in quarter cycle. The third inverter's modulation technique and its transformer's turn ratio stay unchanged again. It continues contributing 4 level at quarter cycle. The equivalent simulation circuit is shown in Figure 3.17. The percentage power transferred via first inverter increases from 14.28% to 33.3% and this power rate for the third inverter is increased from 57.14% to 66.7%.

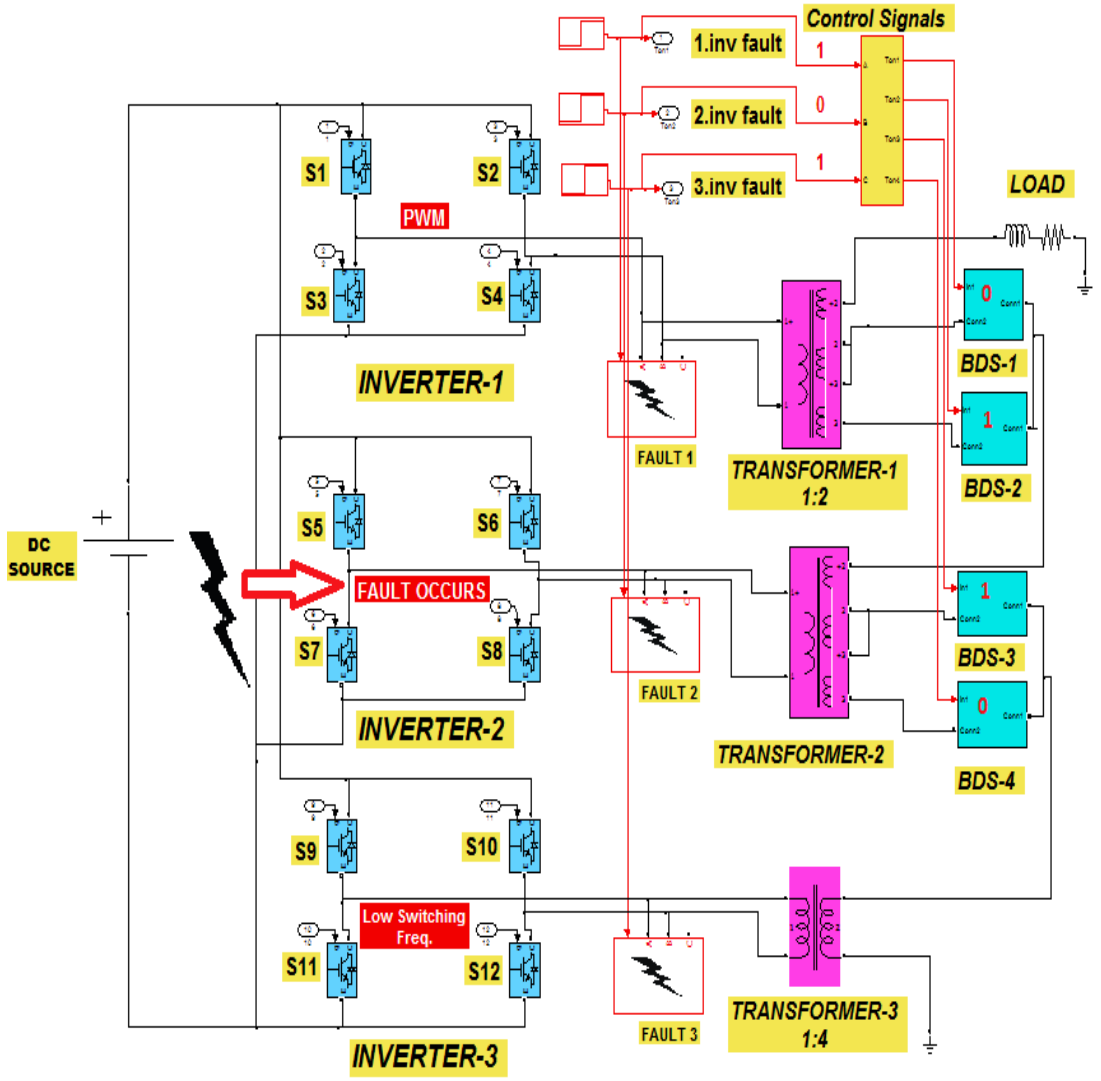


Figure 3.17 : Proposed multilevel inverter when a fault exists in second inverter.

3.2.2.3 Third inverter fault

This fault situation is the most critical situation for the system because this inverter transfers most of the produced power in the input stage to the output stage. When a fault occurred in the third inverter, the first inverter's transformer's turn ratio is changed from 1:1 to 1:2, and the second inverter's transformer's turn ratio is changed from 1:2 to 1:4 by reversing the all conduction states of the BDSs'. At this situation, BDS1 and BDS3 are turned OFF while BDS2 and BDS3 are turned to ON state as shown in Figure 3.18.

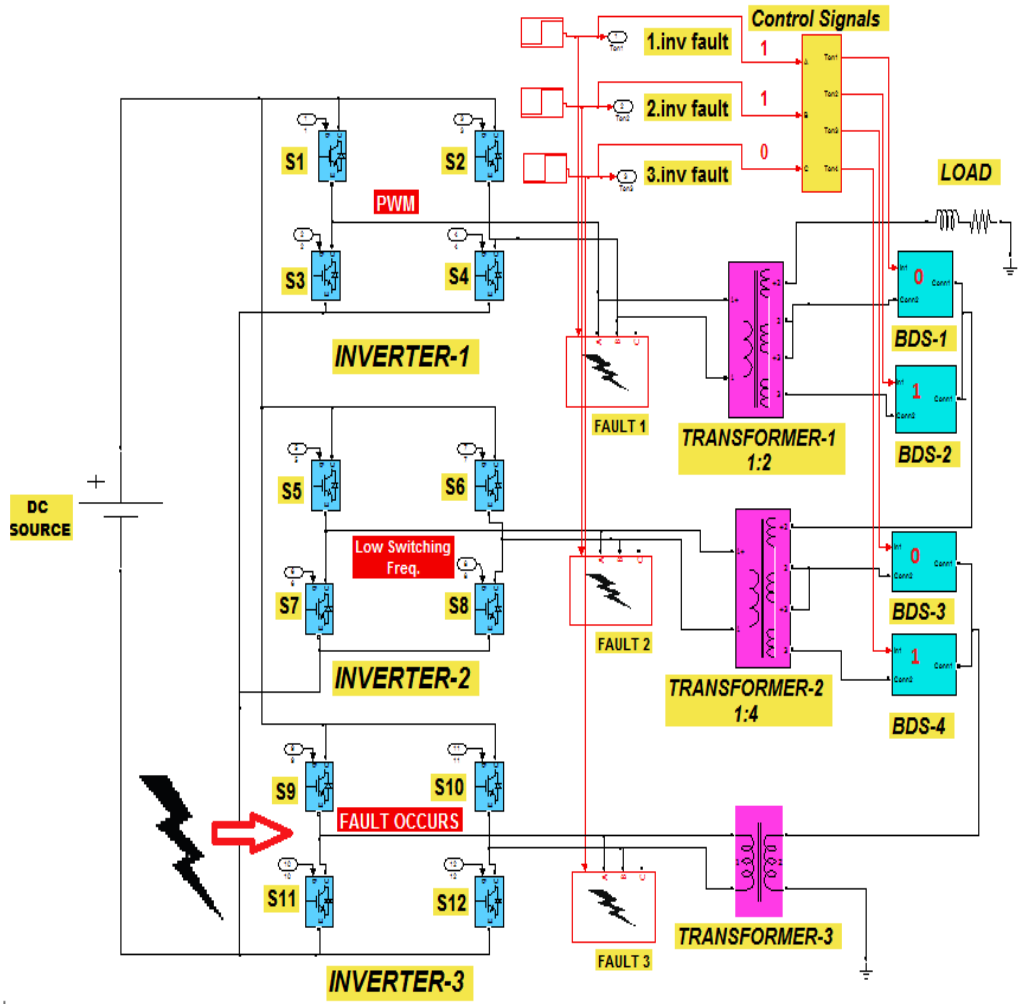


Figure 3.18 : Proposed multilevel inverter when a fault exists in third inverter.

4. RESULTS and DISCUSSIONS

In this chapter, the simulation results of the proposed inverter system according to the each fault conditions are presented. The simulations are made under different switching frequencies and with different load types (purely resistive and resistive-inductive loads). Moreover, Diode-Bridge MOSFET bi-directional switch and Common-Source MOSFETs bi-directional switch models are tested separately and compared with each other considering the quality parameters like total harmonic distortion and efficiency.

4.1 No Fault Condition

The proposed inverter system is fed by 52V DC source. In this mode, the inverter has 15 levels in one period at the output stage. The simulations are made for two different bi-directional switch configurations: DB-MOSFET-BDS and Common-Source-MOSFETs-BDS. Furthermore, two types of loads are tested: purely resistive (R=50Ω) and series connected resistive-inductive load (R=50Ω, L=10mH). The switching frequency is altered from 1 kHz to 20 kHz to achieve best results.

When DB-MOSFET-BDS is used with purely resistive load, the resulted output voltage and the output current with 2 kHz switching frequency are shown in Figure 4.1 and Figure 4.2, respectively. The peak value of the output voltage is 358.951 V and its effective value is 253.81 V_{rms}. If there were no voltage loss in the circuit, expected value of the output voltage would be 52*7=364V. Total voltage loss in the circuit is nearly 7V. Output current's peak value is 7.179A and its effective value is 5.076.The input current has 50.3A peak value and 32.04A average value. The efficiency of the system is calculated by the formula:

$$Efficiency = 100x\frac{P_{out}}{P_{in}} \quad \textbf{(4.1)}$$

Where P_{out} is defined as multiplication of the output voltage's effective value with output current's effective value and P_{in} is defined as multiplication of input voltage

(DC) with input currents(shaped as full-rectified wave) average value. The output power of the system becomes 1288.33W and input power becomes 1666W ,so the efficiency of the system becomes 77.3% when DB-MOSFET-BDS is used with purely resistive load under 2 kHz switching frequency.

When the THD of the output voltage and output current is checked at different switching frequencies, it can be seen that all THD values are less %5 than except 1kHz, as shown in Table 4.1. When the switching frequency is increased, the THD of voltage and current approaches to zero. However, switching losses increases with increased switching frequency and it reduces the output voltage magnitude.

Table 4.1 : Output voltage and current parameters with DB-MOSFET and with resistive load

Switching Frequency fs(kHz)	**DB-MOSFET-BDS**		
	V_{THD}=I_{THD} (%)	**$V_{AC-PEAK}$ (V)**	**$I_{AC-PEAK}$ (A)**
1	5,34	358,403	7,168
2	1,67	358,951	7,179
4	0,82	358,246	7,165
6	0,64	357,905	7,158
8	0,57	357,885	7,157
12	0,52	357,811	7,156
20	0,49	357,444	7,148

When we tested R-L load at the output stage, we see that output voltage reduces about 2V when compared with purely resistive load. The THD of the current decreases dramatically by the factor of load's inductance when switching frequency is increased, but THD of the voltage stays between the interval of %2-%3, as shown in Table 4.2. The efficiency becomes 77.5% for RL load under 2 kHz switching frequency. Output voltage and current waveforms are shown in Figure 4.3 and Figure 4.4, respectively.

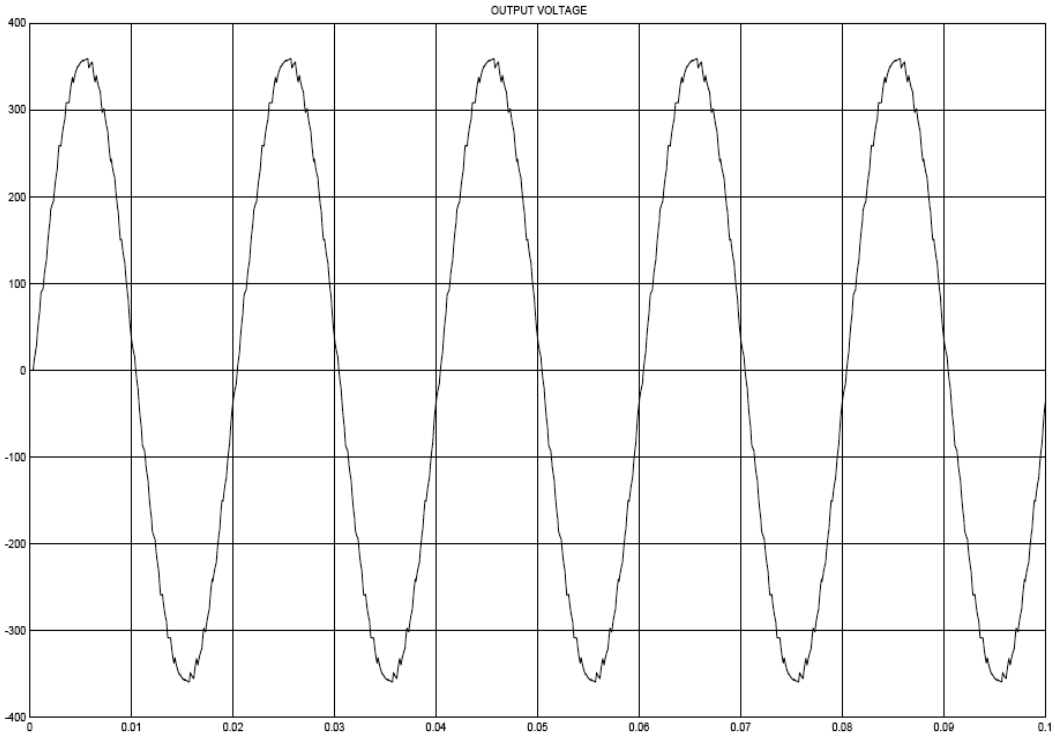


Figure 4.1 : Output voltage with DB-MOSFET-BDS with purely resistive load.

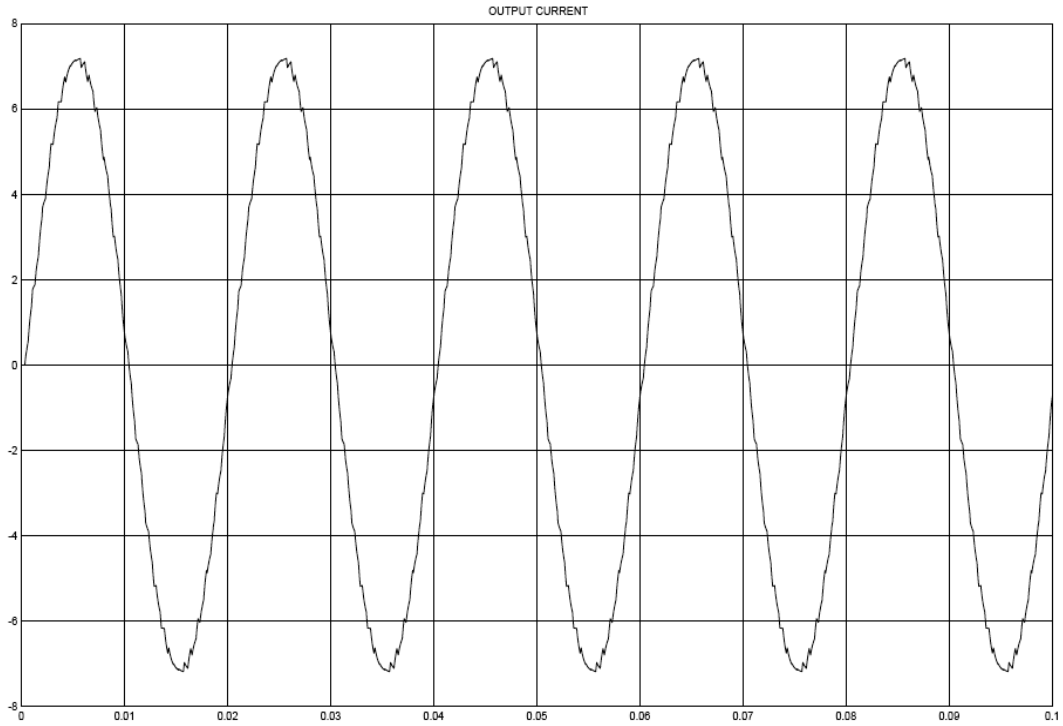


Figure 4.2 : Output current with DB-MOSFET-BDS with purely resistive load.

Table 4.2: Output voltage and current parameters with DB-MOSFET and with R-L load.

Switching Frequency fs(kHz)	DB-MOSFET-BDS			
	V_{THD}	I_{THD}	$V_{AC-PEAK}$	$I_{AC-PEAK}$
1	5,48	4,69	357,780	7,129
2	2,94	1,3	357,480	7,120
4	2,72	0,82	356,825	7,100
6	2,66	0,75	356,548	7,092
8	2,63	0,72	356,489	7,090
12	2,54	0,71	356,412	7,088
20	2,39	0,69	356,319	7,083

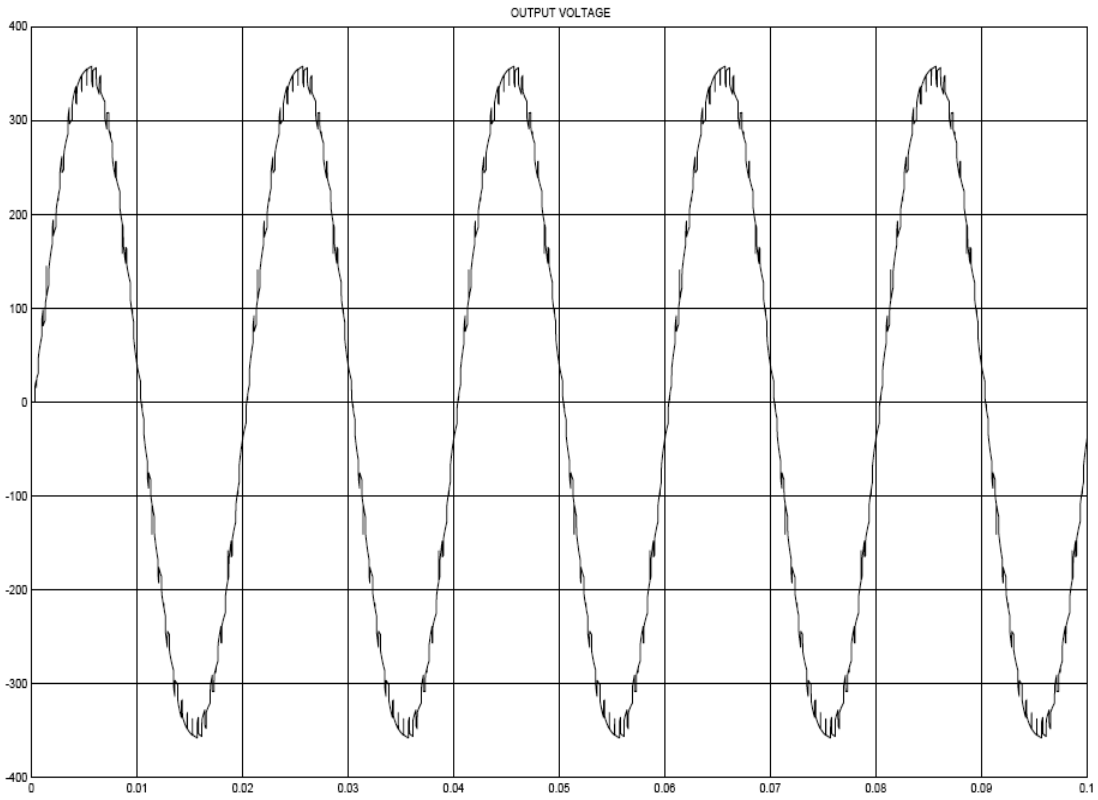


Figure 4.3 : Output Voltage with DB-MOSFET-BDS with R-L load.

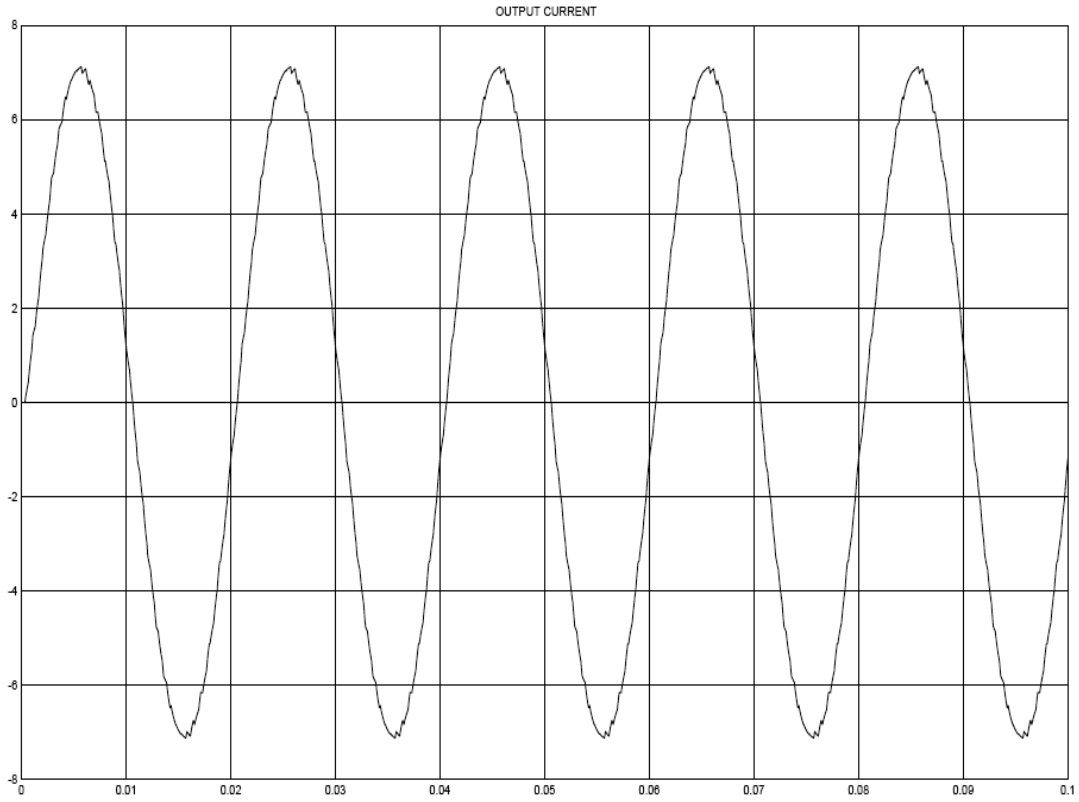


Figure 4.4 : Output current with DB-MOSFET-BDS with R-L load.

When CS-MOSFETs-BDS is used with pure resistive load, the voltage loss decreases nearly 2V when compared with DB-MOSFET-BDS. Total voltage loss of the system is approximately 4V. Furthermore, %0.1 improvement is provided in THD values.For different switching frequencies the THD value, peak values of output voltage and current are shown in Table 4.3. The efficiency becomes 77.81% for purely resistive load under 2 kHz switching frequency.

Table 4.3: Output voltage and current parameters with CS-MOSFETs-BDS and with resistive load.

Switching Frequency fs(kHz)	**CS-MOSFETs-BDS**		
	V_{THD}=I_{THD}	**$V_{AC-PEAK}$**	**$I_{AC-PEAK}$**
1	5,48	360.4	7.2082
2	1,63	360.95	7.2192
4	0,74	360.25	7.2051
6	0,55	359,91	7,1981
8	0,47	359.89	7.1978
12	0,41	359,815	7,1963
20	0,37	359,456	7,1891

When R-L load is tested, again 2V enhancement provided in output voltage peak value, but the THD values do not change significantly, as shown in Table 4.4. The efficiency becomes 77.48% for resistive-inductive load under 2 kHz switching frequency.

Table 4.4: Output voltage and current parameters with CS-MOSFETs-BDS and with R-L load.

Switching Frequency fs(kHz)	CS-MOSFETs-BDS			
	V_{THD}	I_{THD}	$V_{AC-PEAK}$	$I_{AC-PEAK}$
1	5,56	4,79	359.79	7.1692
2	2,9	1,25	359.483	7.16
4	2,7	0,74	358.83	7.1407
6	2,66	0,66	358,55	7,1324
8	2,69	0,63	358.487	7.1307
12	2,66	0,62	358,4	7,1282
20	2,68	0,6	358,325	7,1235

4.2 Fault Conditions

When a fault occurres in one of the H-Bridge inverters, the level of the output voltage decreases one level at quarter cycle, and system produces 13 voltage levels in one period. At fault instants the system is again fed by 52V DC source. Total simulation time is 0.1 second and fault instants are identified by the external signals at 0.04 second. Moreover, for fault conditions the comparisons of DB-MOSFET-BDS and CS-MOSFETs-BDS are made again. The fault conditions are examined for each H-Bridge inverter separately and output stage parameters are presented in depth.

4.2.1 First inverter fault condition

When a fault occurred at 0.04 second in the first inverter with resistive load, while switching frequency is 2 kHz, if we use DB-MOSFET-BDS, the inverter's output voltage peak value decreases to 307.45V whose effective value is 217.4V, and inverter's output current's peak value decreases to 6.148A ($4.34A_{rms}$), as presented in Figure 4.5 and Figure 4.6. The average value of drawn current from DC source

reduces to 23.5A. After fault condition the efficiency becomes 77.34% for purely resistive load under 2 kHz switching frequency.

If CS-MOSFETs-BDS is used the system's output voltage peak value decreases to 309.43V whose effective value is 218.8 V_{rms} as shown in Figure 4.7. Moreover, the proposed inverter's output current has 6.188A peak value whose effective value is 4.37A_{rms} which is illustrated in Figure 4.8. After fault condition the efficiency becomes 77.8% for purely resistive load under 2kHz switching frequency.

If it is taken into account that the system can continue working in voltage range ±10% of 230V, these output voltage levels are acceptable. When these two bi-directional switches are compared for different switching frequencies, which is shown in Table 4.5, CS-MOSFETs-BDS has less conduction losses and a bit lower THD values. The THD of voltage and current increases due to the level decrease, but still these THD rates are mostly less than 5% which are admissible. The THD analyses in Table 4.5 are made for the time interval 0.04-0.1 seconds.

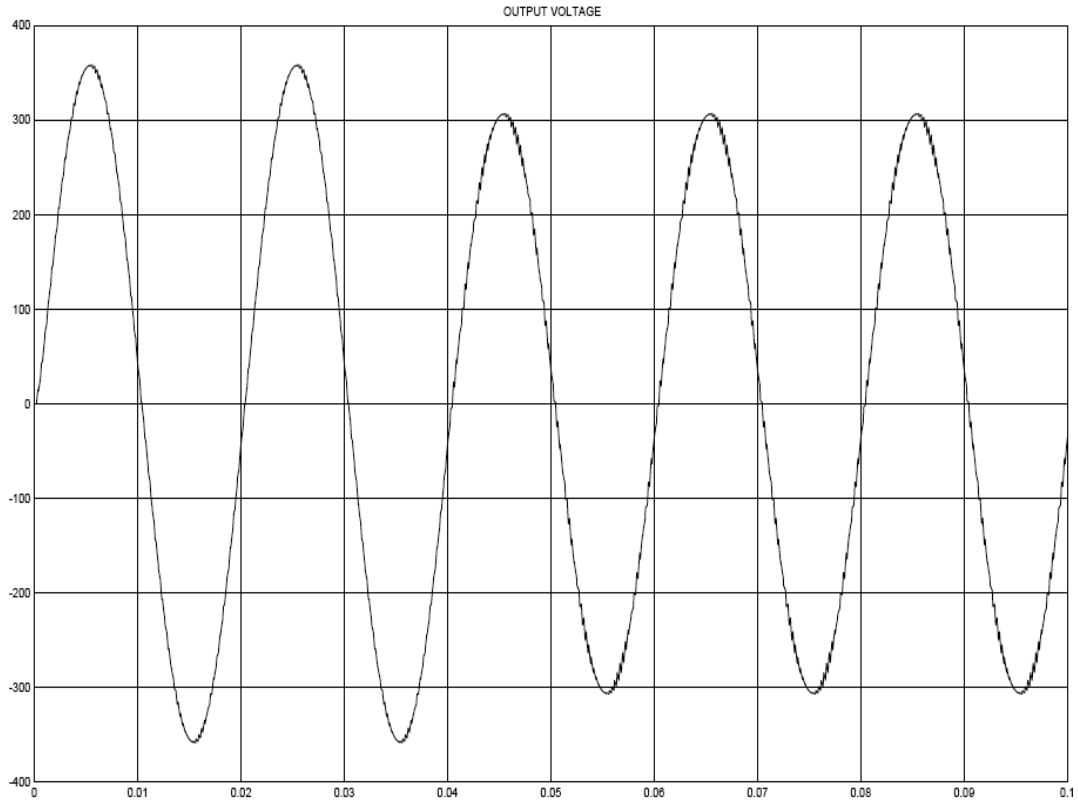


Figure 4.5 : Output voltage when a fault occurred in first inverter if DB-MOSFET-BDS used with resistive load.

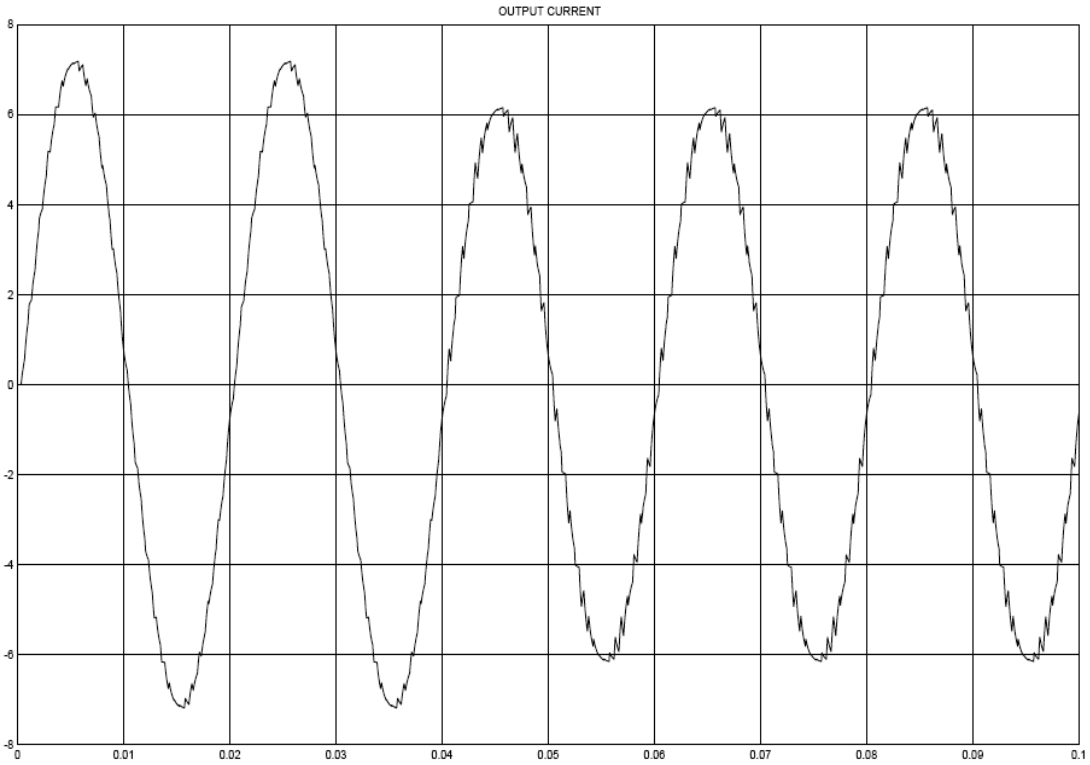


Figure 4.6 : Output current when a fault occurred in first inverter if DB-MOSFET - BDS used with resistive load.

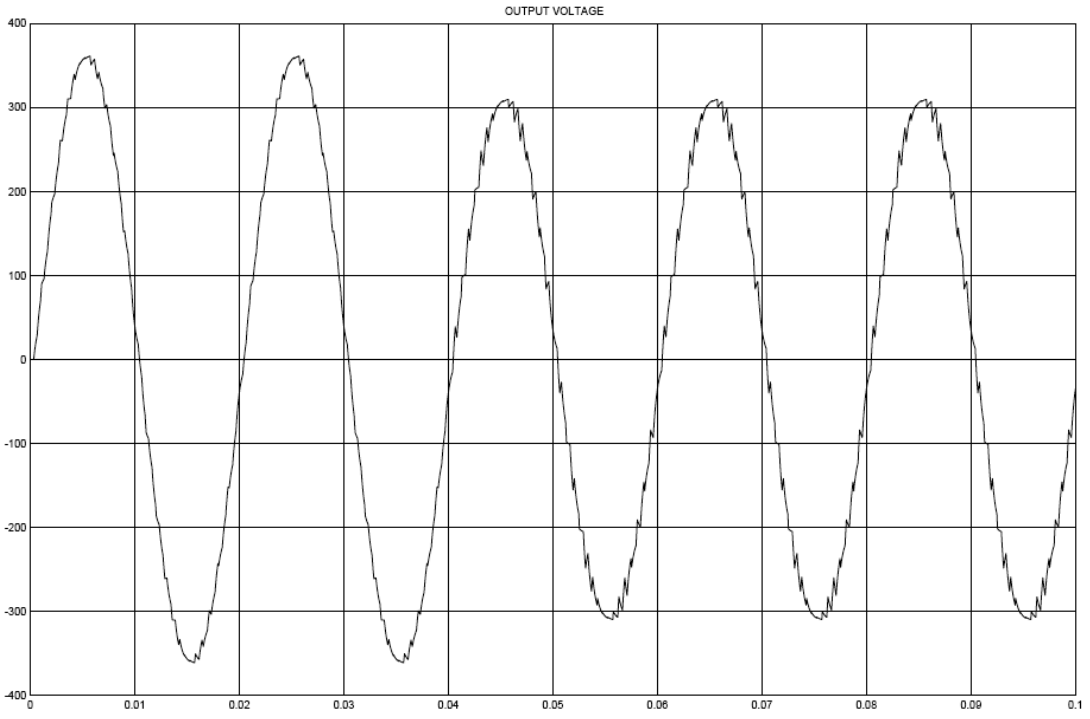


Figure 4.7 : Output voltage when a fault occurred in the first inverter if CS-MOSFET-BDS used with resistive load.

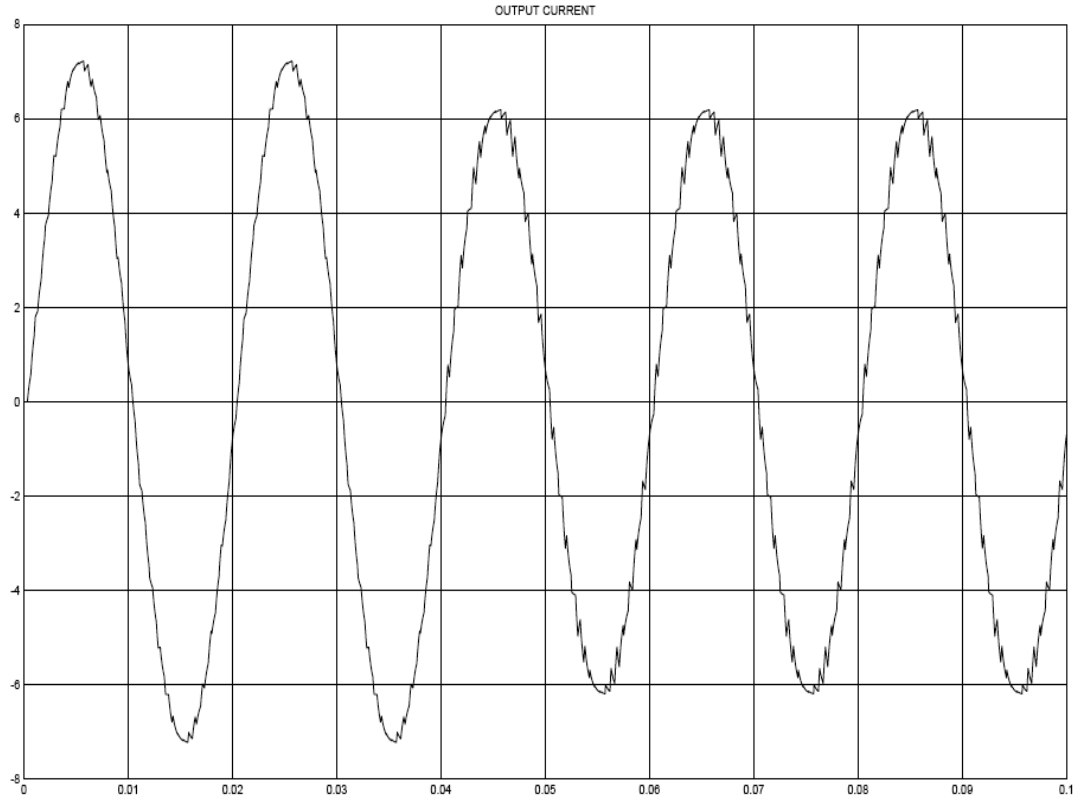


Figure 4.8 : Output current when a fault occurred in the first inverter if CS-MOSFET-BDS is used with resistive load.

When R-L load is tested, it can be seen from Table 4.6 that CS-MOSFETs-BDS has nearly 2V less conduction losses when compared with DB-MOSFET-BDS at different switching frequencies. As expected, THD of current decreases dramatically for both BDS types when the switching frequency is increased due to the load's inductance. However, this inductance prompts to output voltage's THD staying at 5-6% levels. Especially for the CS-MOSFETs-BDS, the ripples in the output voltage blocks the reduction of THD with increasing switching frequency.

After fault condition, the efficiency becomes 77.02% for purely resistive load under 2kHz switching frequency when DB-MOSFET-BDS is used and 77.51% when CS-MOSFET-BDS is used. Output voltage and output current waveforms are presented in the Figure 4.9 and Figure 4.10 for DB-MOSFET-BDS, and in Figure 4.11 and Figure 4.12 for CS-MOSFETs-BDS.

Table 4.5 : Output voltage and current parameters for a resistive load when a fault occurred in first inverter.

Switching Frequency fs(kHz)	DB-MOSFET-BDS			CS-MOSFETs-BDS		
	$V_{THD}=I_{THD}$ (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)	$V_{THD}=I_{THD}$ (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)
1	6,41	307,36	6,147	6,36	309,36	6,187
2	3,01	307,45	6,148	2,93	309,43	6,188
3	1,99	307,05	6,140	1,92	309,00	6,180
4	1,49	306,77	6,135	1,44	308,77	6,175
6	1,00	306,43	6,128	0,96	308,44	6,169
8	0,77	306,57	6,131	0,72	308,58	6,171
12	0,54	306,27	6,125	0,49	308,29	6,165
20	0,40	305,63	6,112	0,33	307,65	6,153

Table 4.6: Output voltage and current parameters for a R-L load when a fault occurred in first inverter.

Switching Frequency fs(kHz)	DB-MOSFET-BDS				CS-MOSFETs-BDS			
	V_{THD} (%)	I_{THD} (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)	V_{THD} (%)	I_{THD} (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)
1	7,64	4,68	306,91	6,119	7,58	4,66	308,88	6,159
2	6,39	2,08	306,23	6,100	6,37	2,02	308,21	6,140
3	6,04	1,37	305,91	6,090	6,11	1,32	307,88	6,130
4	5,94	1,04	305,63	6,081	6,12	0,99	307,60	6,120
6	5,68	0,71	305,33	6,072	6,01	0,67	307,32	6,113
8	5,49	0,56	305,35	6,073	6,07	0,52	307,30	6,113
12	5,12	0,41	305,10	6,066	6,05	0,37	307,09	6,106
20	4,57	0,33	304,81	6,052	6,09	0,28	306,89	6,093

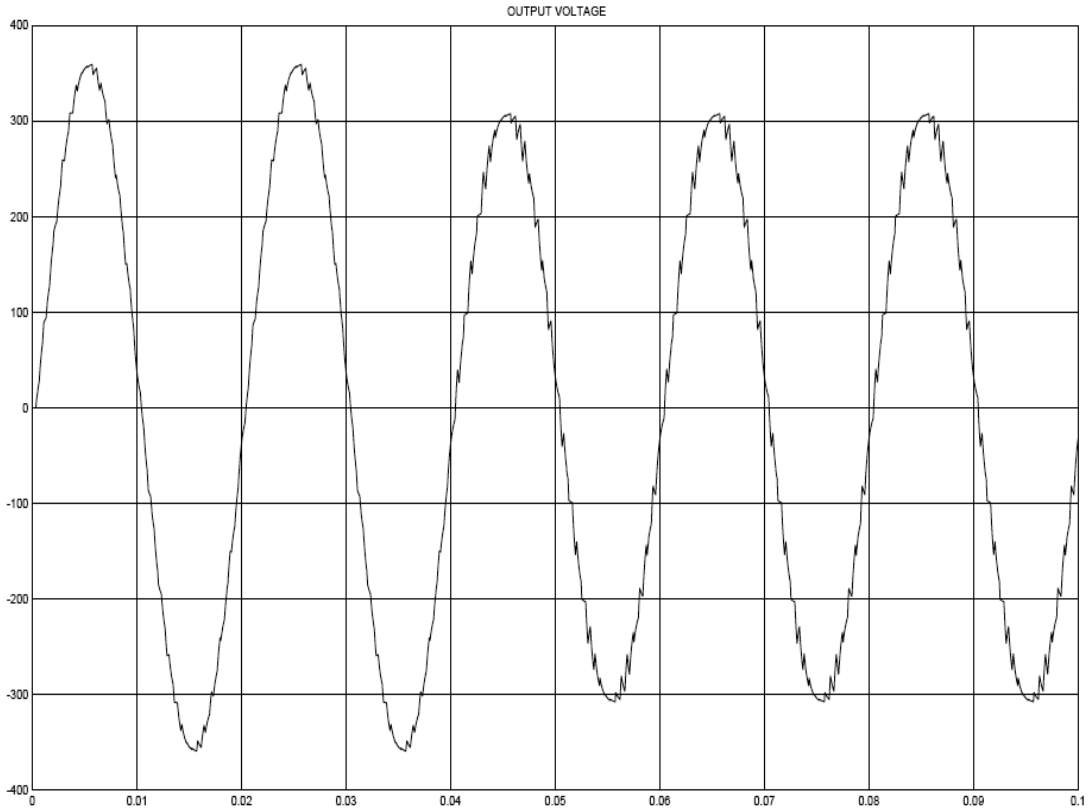


Figure 4.9 : Output voltage when a fault occurred in the first inverter if DB-MOSFET-BDS used with R-L load.

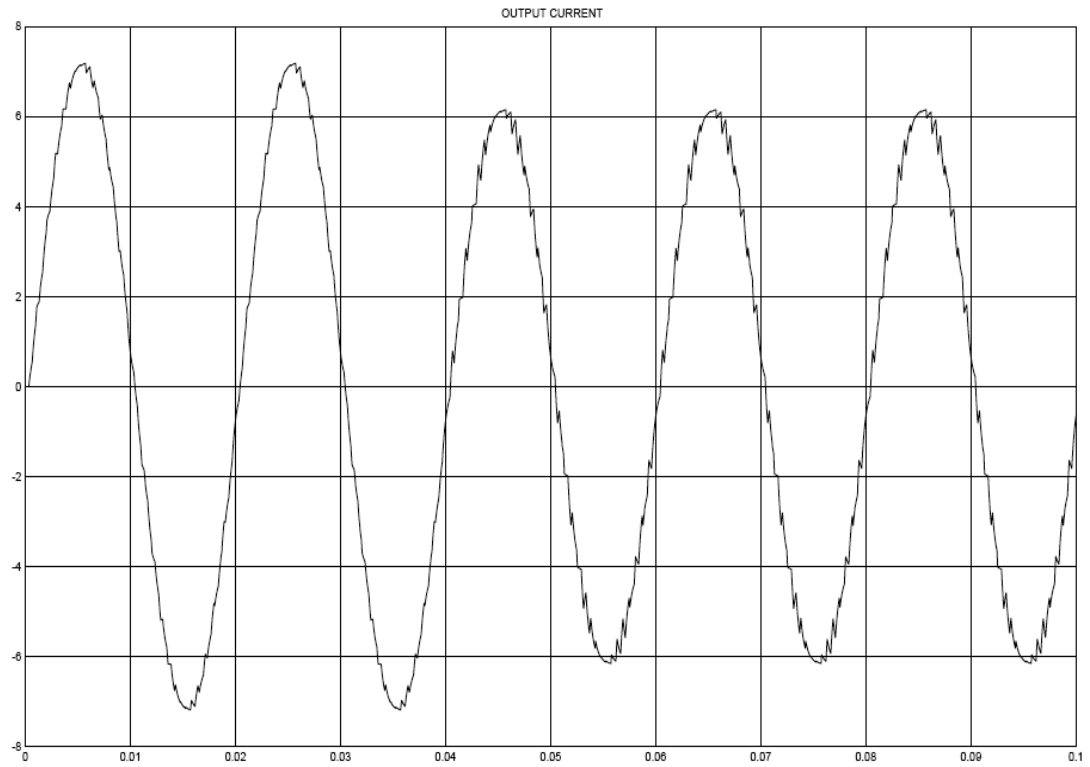


Figure 4.10 : Output current when a fault occurred in the first inverter if DB-MOSFET-BDS used with R-L load.

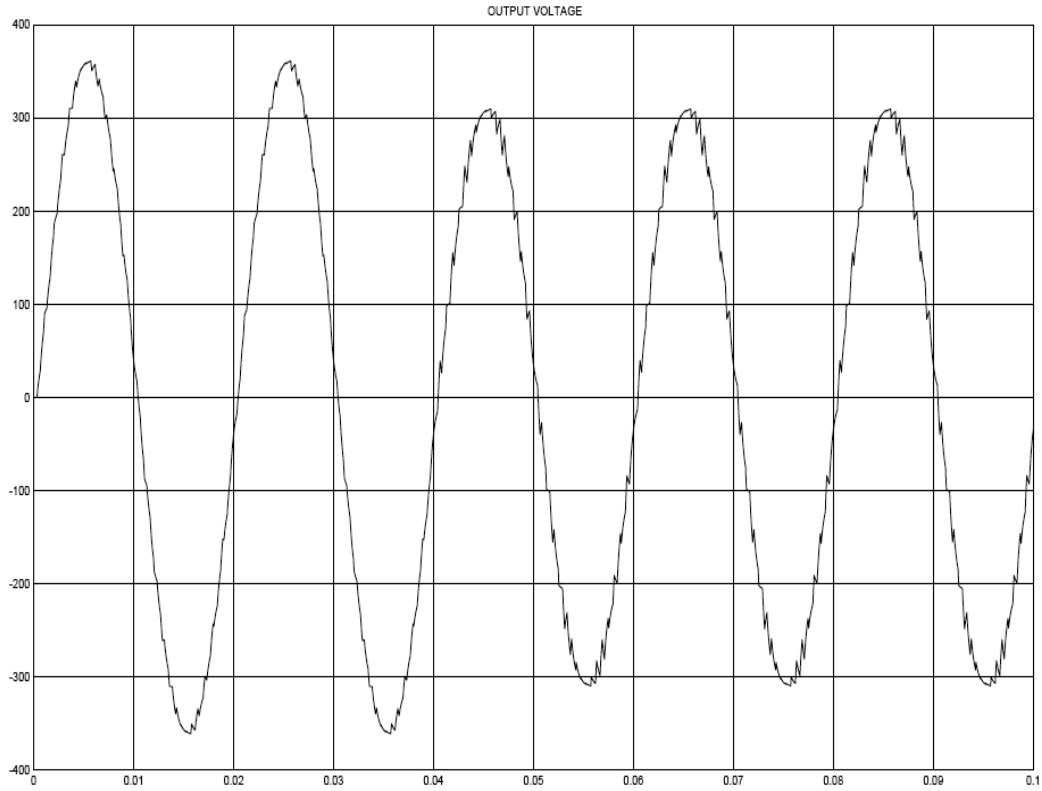


Figure 4.11 : Output voltage when a fault occurred in the first inverter if CS-MOSFET-BDS used with R-L load.

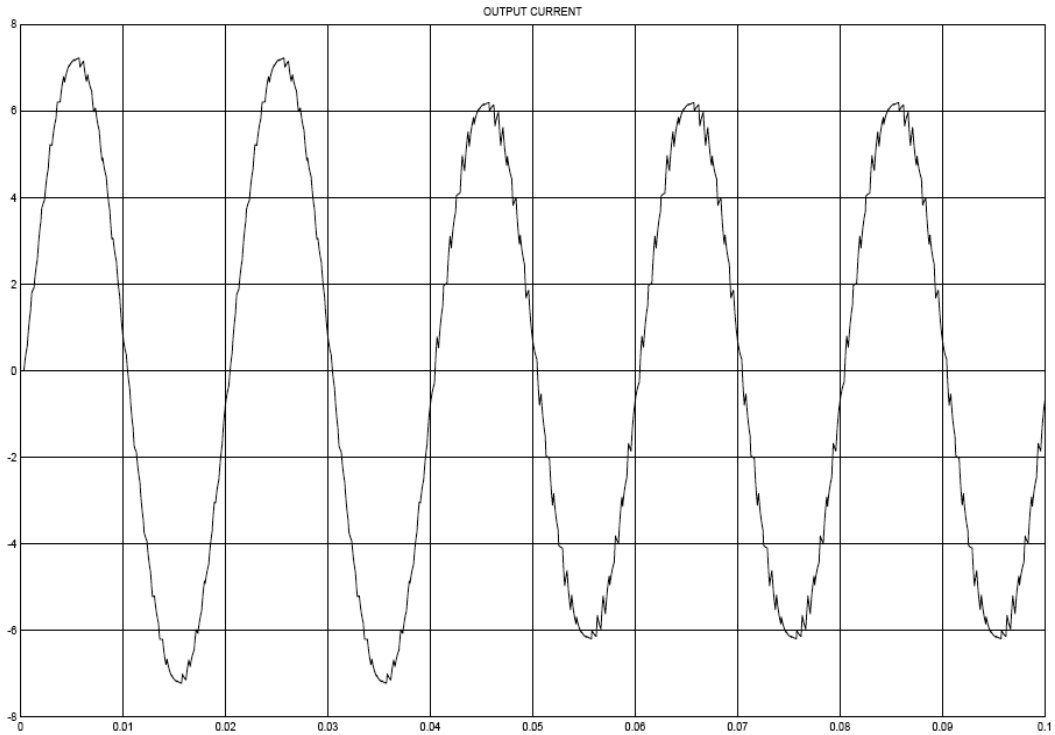


Figure 4.12 : Output current when a fault occurred in the first inverter if CS-MOSFET-BDS used with R-L load.

4.2.2 Second inverter fault condition

Once a fault occurres in the second inverter, similar results with first inverter fault emerges if a resistive load is tested. When DB-MOSFET-BDS is used; the output voltage's peak value falls to 306V in average and output current's peak value drops to 6,1A ,shown in Figure 4.13 and Figure 4.14 with 2 kHz switching frequency. Likewise, when CS-MOSFETs-BDS is used; the voltage's peak value falls to 308V in average, and current's peak value drops to 6,15A,represented in Figure 4.15 and Figure 4.16. Output voltage and current parameters are shown in Table 4.7. The CS-MOSFETs-BDS saves the advantage of less conduction losses and has 2V less voltage drop than DB-MOSFET-BDS. The average value of the DC current (input current) drops to 23.56A for CS-MOSFETs-BDS and 23.44A for DB-MOSFET-BDS. After fault, under 2kHz switching frequency, the efficiency becomes 76.81% and 77.7% for DB-MOSFET-BDS and CS-MOSFETs-BDS, respectively.

However, when R-L load is tested, as shown in Figure 4.17, a problem occurs if CS-MOSFETs-BDS is used that is at fault instant voltage reaches very rapidly up to 1900V for a very short time. After these impulses, the system recover itself and reaches to steady-state conditions. As can be seen in Table 4.8, these impulses makes the THD a bit higher than DB-MOSFET-BDS's results.

Table 4.7: Output voltage and current parameters for a resistive load when a fault occurred in the second inverter.

Switching Frequency fs(kHz)	DB-MOSFET-BDS			CS-MOSFETs-BDS		
	$V_{THD}=I_{THD}$ (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)	$V_{THD}=I_{THD}$ (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)
1	5,59	306,79	6,136	5,56	308,80	6,176
2	2,56	306,59	6,131	2,50	308,59	6,172
3	1,70	305,84	6,117	1,64	307,85	6,157
4	1,29	305,83	6,116	1,22	307,84	6,156
6	0,89	305,49	6,110	0,81	307,49	6,150
8	0,71	305,43	6,108	0,61	307,44	6,148
12	0,53	305,15	6,103	0,41	307,162	6,143
20	0,40	304,62	6,092	0,28	306,8	6,136

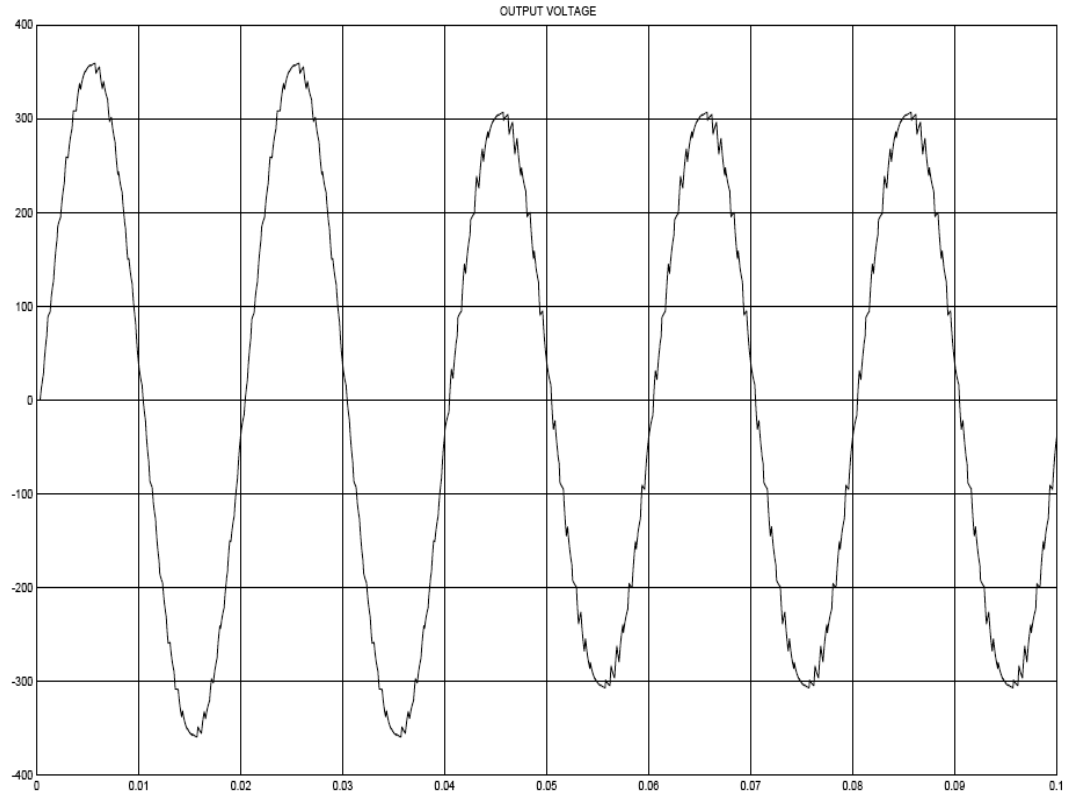


Figure 4.13 : Output current when a fault occurred in first inverter if DB-MOSFET-BDS is used with resistive load.

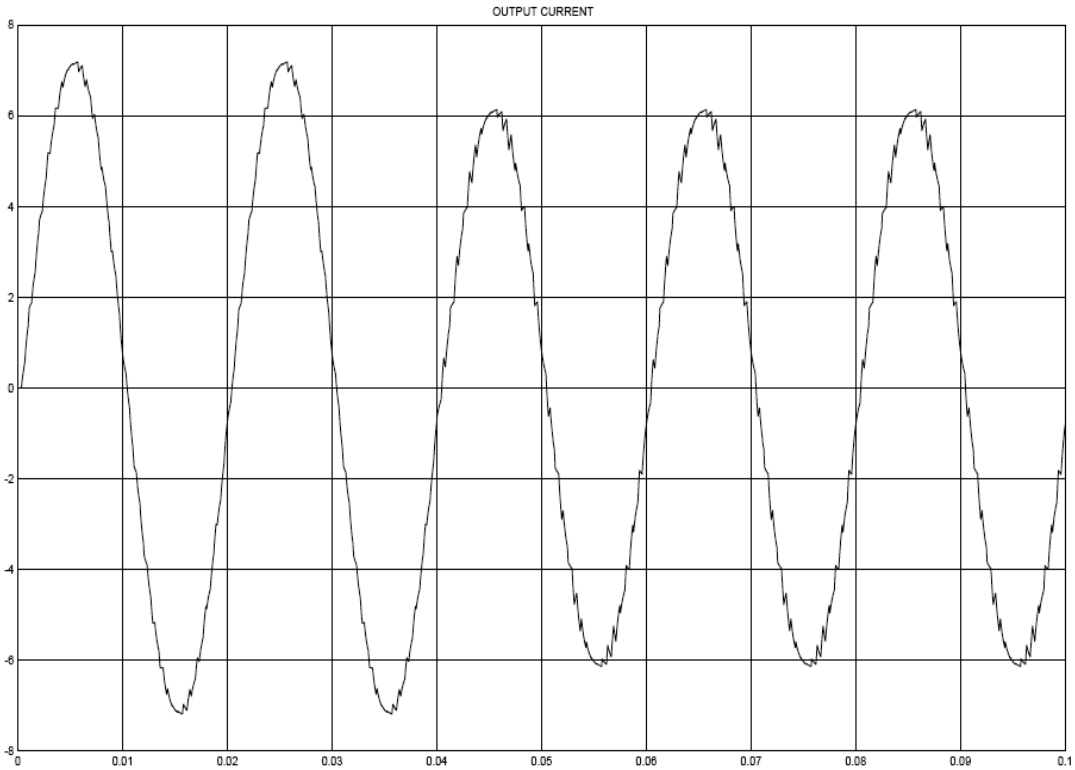


Figure 4.14 : Output current when a fault occurred in the second inverter if CS-MOSFETs-BDS is used with resistive load.

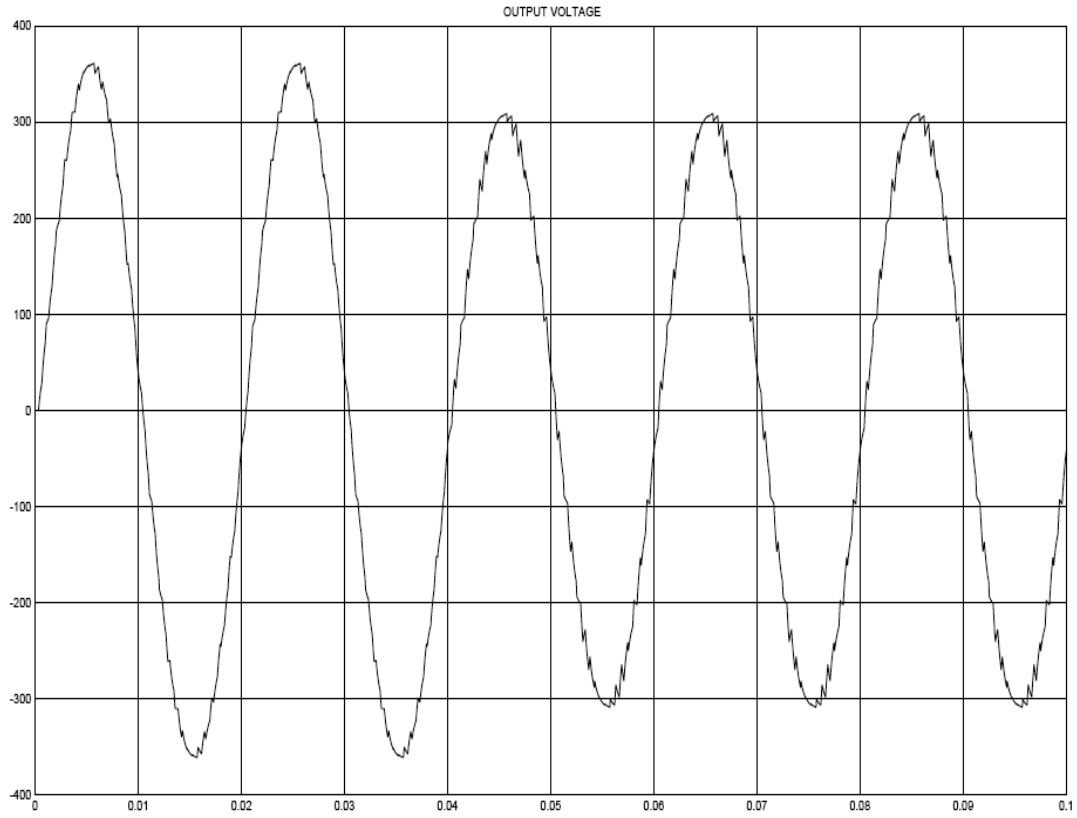


Figure 4.15 : Output voltage when a fault occurred in the second inverter if DB-MOSFET-BDS is used with resistive load.

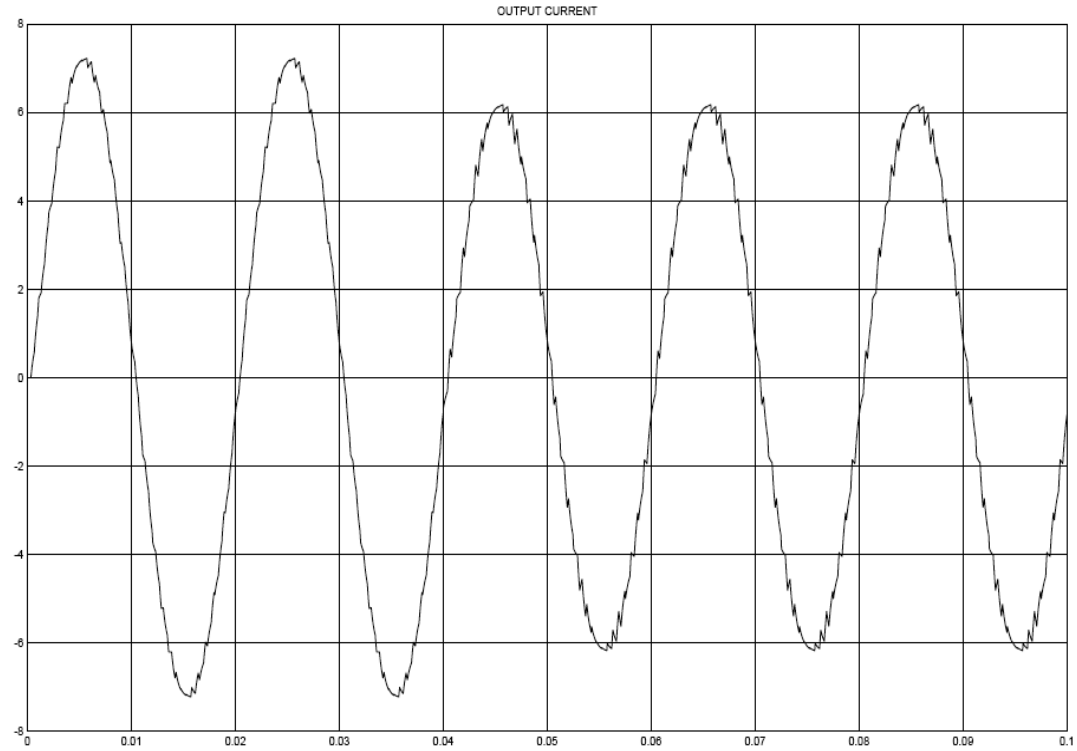


Figure 4.16 : Output current when a fault occurred in the second inverter if CS-MOSFETs-BDS is used with resistive load.

Table 4.8: Output voltage and current parameters for a R-L load when a fault occurred in the second inverter.

Switching Frequency fs(kHz)	DB-MOSFET-BDS				CS-MOSFETs-BDS			
	V_{THD} (%)	I_{THD} (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)	V_{THD} (%)	I_{THD} (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)
1	6,90	4,21	306,10	6,103	6,78	4,15	308,11	6,141
2	5,77	1,87	304,96	6,070	5,71	1,81	306,96	6,109
3	5,50	1,24	304,74	6,063	5,47	1,18	306,74	6,103
4	5,44	0,94	304,37	6,050	5,58	0,88	306,35	6,092
6	5,31	0,66	304,10	6,045	5,39	0,58	306,09	6,085
8	5,22	0,53	304,07	6,044	5,44	0,44	306,07	6,084
12	5,02	0,41	303,82	6,036	5,41	0,29	305,82	6,077
20	4,67	0,34	303,53	6,027	5,46	0,2	305,5	6,067

These impulses are not seen in the output current as illustrated in Figure 4.18 and THD of current decreases as usual with increasing switching frequency. Furthermore, this problem does not occur when DB-MOSFET-BDS is used as shown in Figure 4.19 and 4.20.After fault, under 2kHz switching frequency, the efficiency becomes 77.34% when CS-MOSFETs-BDS is used with R-L load. Moreover, the efficiency is 76.31% when DB-MOSFET-BDS is used with R-L load.

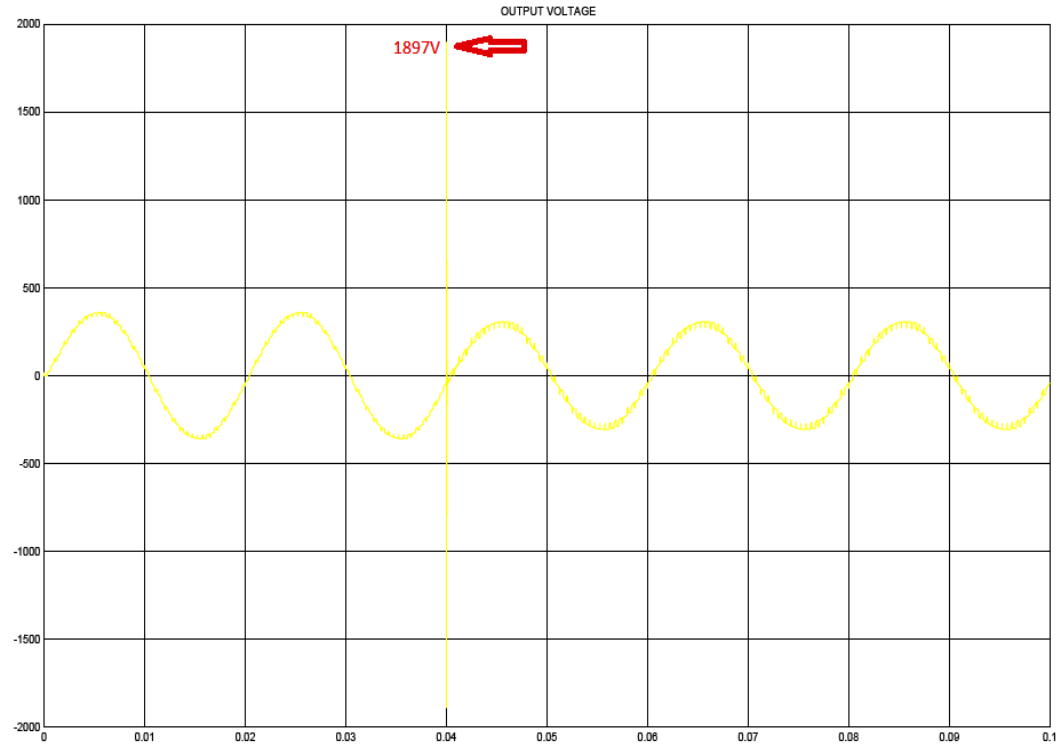


Figure 4.17 : Output voltage when a fault occurred in the second inverter if CS-MOSFETs-BDS is used with R-L load.

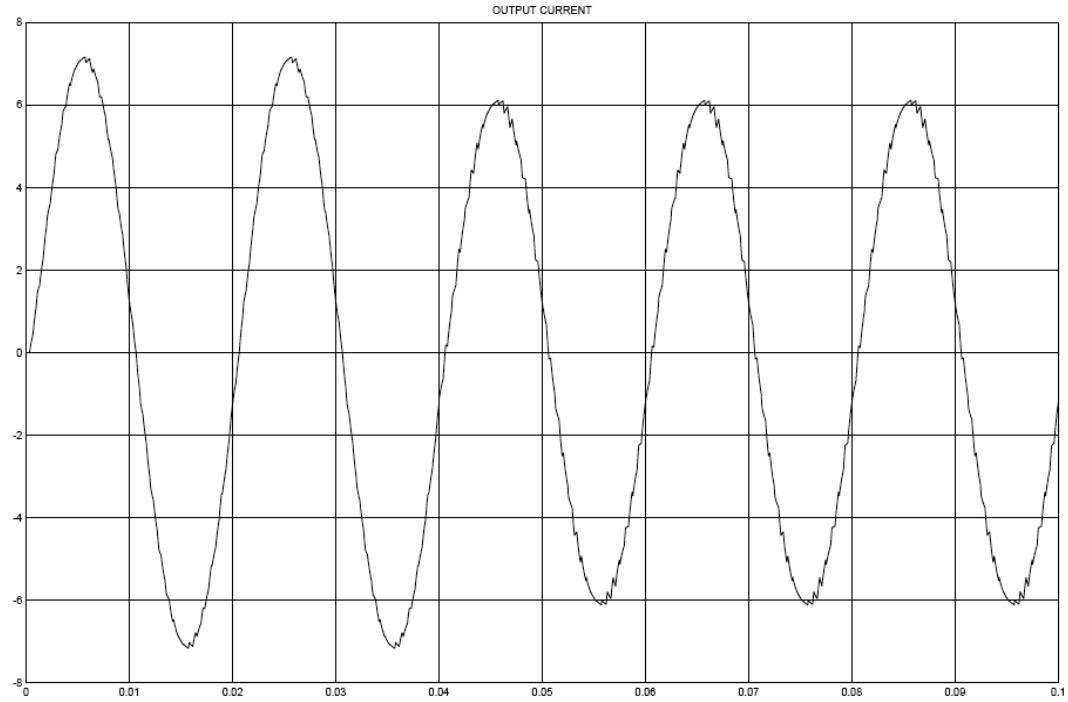


Figure 4.18 : Output current when a fault occurred in the second inverter if CS-MOSFETs-BDS is used with R-L load.

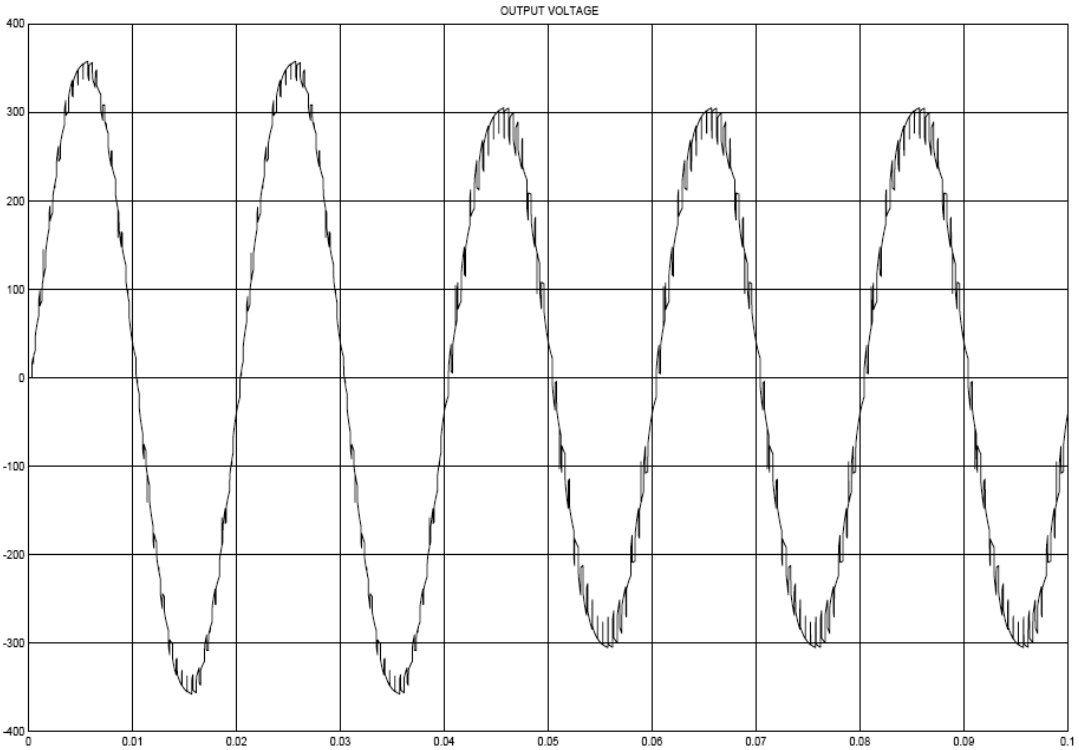


Figure 4.19 : Output voltage when a fault occurred in the second inverter if DB-MOSFET-BDS is used with R-L load.

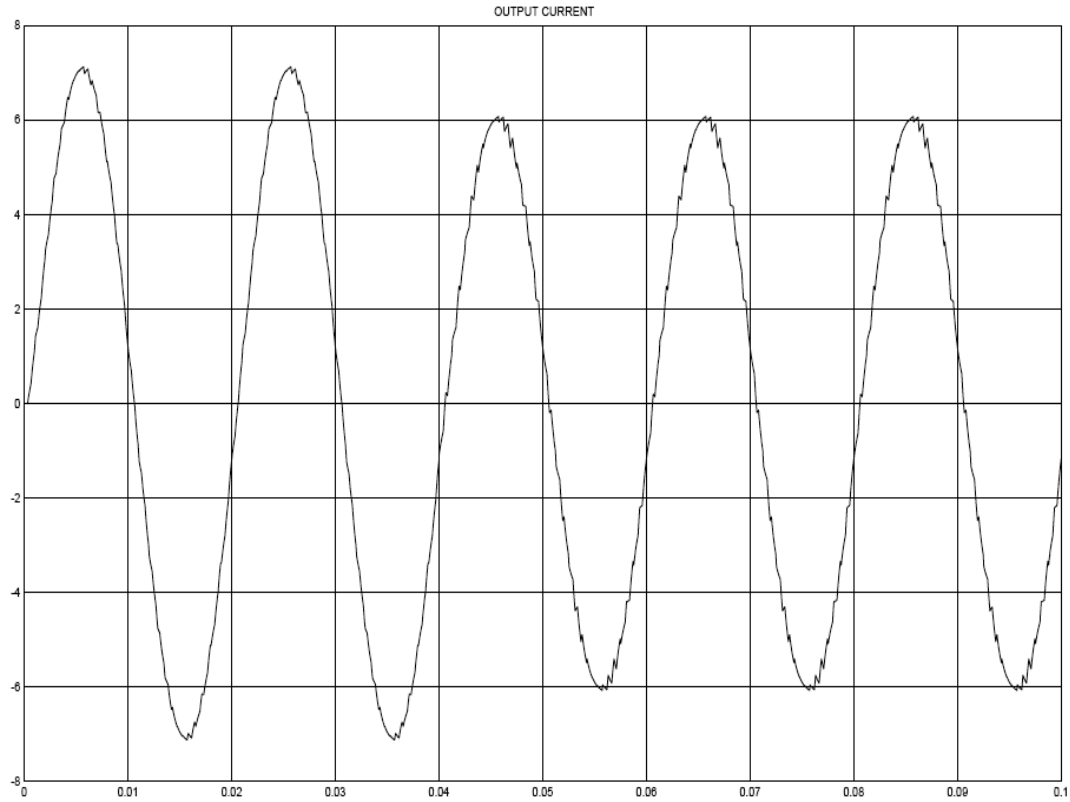


Figure 4.20 : Output current when a fault occurred in the second inverter if DB-MOSFET-BDS is used with R-L load.

4.2.3 Third inverter fault condition

The third inverter fault is the most important fault condition for the system because, most of the power is transferred to the load via this inverter's transformer. When the resistive load is tested, it can be seen from Table 4.9, again the CS-MOSFETs-BDS's has the 2V less conduction losses and less THD values when compared to DB-MOSFET-BDS. Output voltage and current waveforms under 2 kHz switching frequency are represented for both bi-directional switches in Figure 4.21-4.24. On the other hand, the voltage magnitudes after the fault is at the lowest level if we check against to the other fault conditions. In average, output voltage peak values are 4V less than first inverter fault condition and 3V less than second inverter fault condition, but still this voltage values are enough to keep system working. The average value of the DC current (input current) drops to 23.3A for CS-MOSFETs-BDS and 23.24A for DB-MOSFET-BDS. After fault, under 2kHz switching frequency, the efficiency becomes 76.45% and 77.24% for DB-MOSFET-BDS and CS-MOSFETs-BDS, respectively.

Table 4.9: Output voltage and current parameters for a resistive load when a fault occurred in the third inverter.

Switching Frequency fs(kHz)	DB-MOSFET-BDS			CS-MOSFETs-BDS		
	$V_{THD}=I_{THD}$ (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)	$V_{THD}=I_{THD}$	$V_{AC-PEAK}$	$I_{AC-PEAK}$
1	4,45	305,12	6,103	4,43	307,11	6,142
2	2,06	304,02	6,079	2,00	305,92	6,121
3	1,42	303,51	6,070	1,35	305,50	6,110
4	1,13	302,91	6,059	1,04	304,91	6,099
6	0,88	302,64	6,053	0,77	304,62	6,092
8	0,77	302,63	6,052	0,64	304,60	6,091
12	0,69	302,28	6,045	0,55	304,27	6,085
20	0,64	301,70	6,034	0,49	303,68	6,073

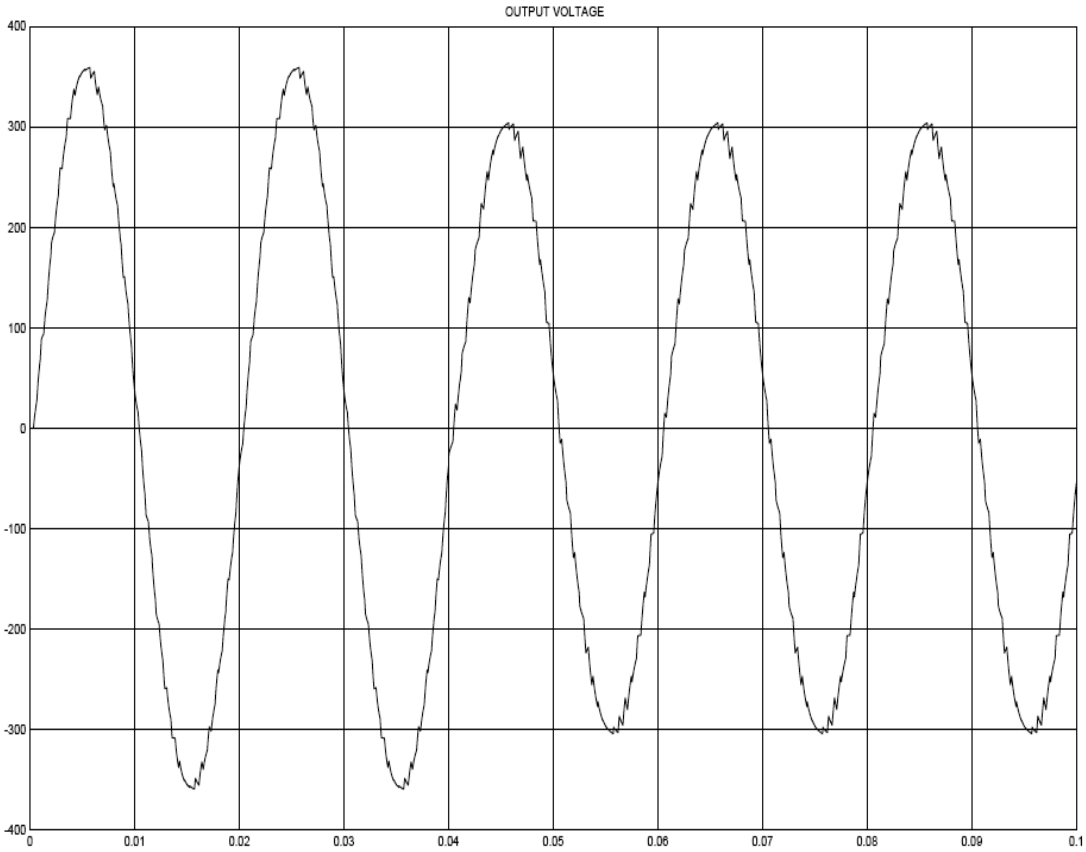


Figure 4.21 : Output voltage when a fault occurred in the third inverter if DB-MOSFET-BDS is used with resistive load.

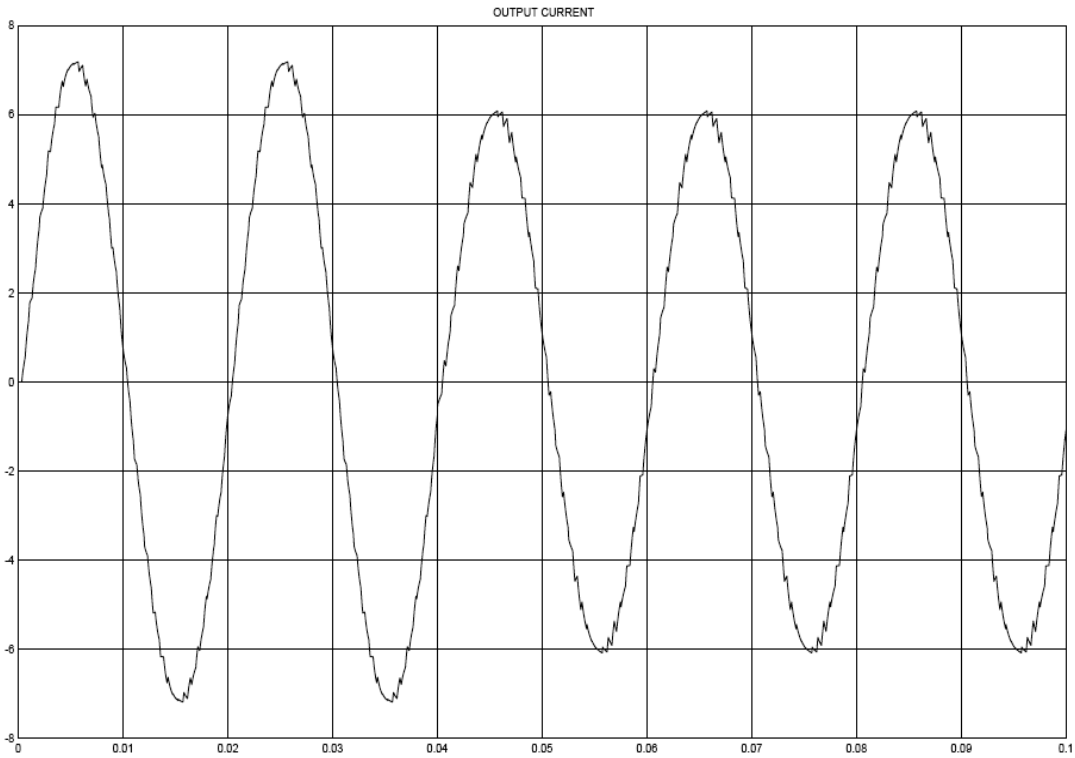


Figure 4.22 : Output current when a fault occurred in the third inverter if DB-MOSFET-BDS is used with resistive load.

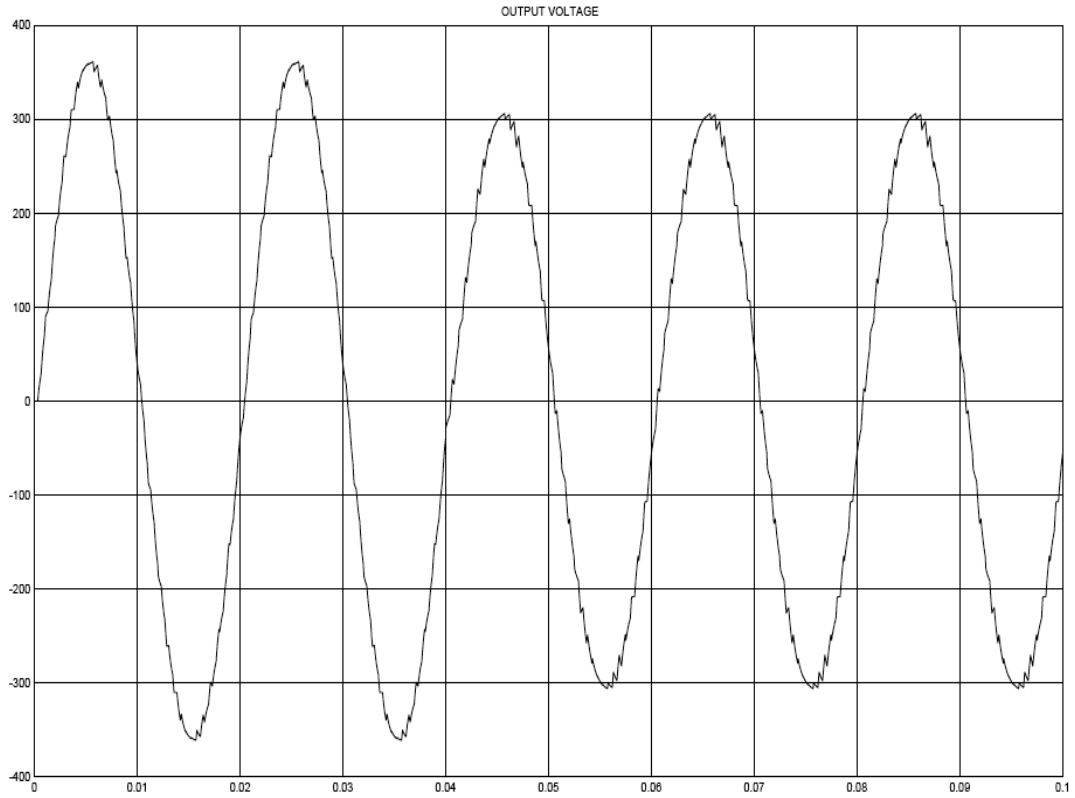


Figure 4.23 : Output voltage when a fault occurred in the third inverter if CS-MOSFETs-BDS is used with resistive load.

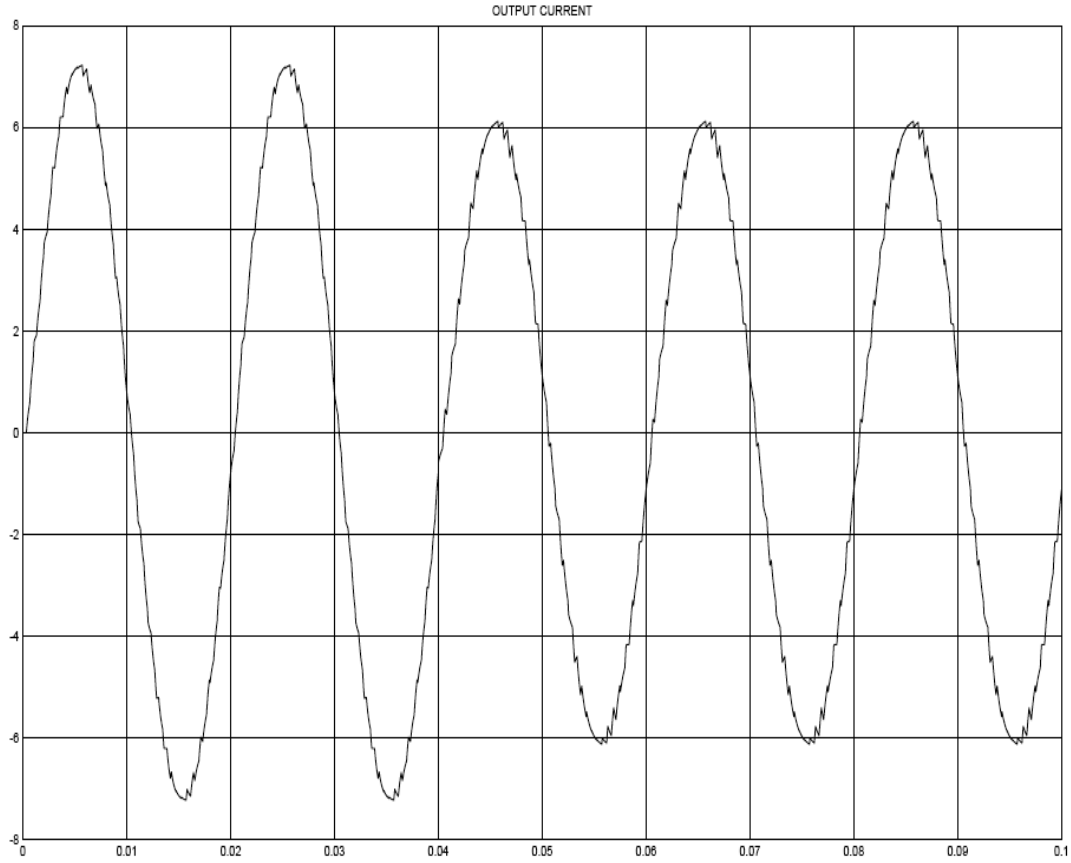


Figure 4.24 : Output current when a fault occurred in the third inverter if CS-MOSFETs-BDS is used with resistive load.

When RL load is tested with CS-MOSFETs-BDS, we faced again voltage impulses at fault instant like in the second inverter fault condition as shown in Figure 4.25. At fault instant voltage rises up to 4722V, but still THD of the system is not affected. When the switching frequency is increased, the THD of the voltage stays at 4-5% by the reason of small fluctuations caused by the load's inductance. If the Figure 4.26 is considered, it can be noticed that the output current does not involve any impulses at fault instant and its THD drastically decreases by increasing frequency. These mentioned voltage impulses are beside the point for DB-MOSFET-BDS. The output voltage and current waveforms under 2 kHz switching frequency are presented in Figure 4.27 and 4.28, respectively. Output voltage and current parameters for a RL load when a fault occurred in the third inverter is presented in Table 4.10. After fault, under 2kHz switching frequency, the efficiency becomes 76.43% when CS-MOSFETs-BDS is used with R-L load. Moreover, the efficiency is 76.15% when DB-MOSFET-BDS is used with R-L load.

Table 4.10: Output voltage and current parameters for a RL load when a fault occurred in the third inverter.

Switching Frequency fs(kHz)	DB-MOSFET-BDS				CS-MOSFETs-BDS			
	V_{THD} (%)	I_{THD} (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)	V_{THD} (%)	I_{THD} (%)	$V_{AC-PEAK}$ (V)	$I_{AC-PEAK}$ (A)
1	5,86	3,53	303,87	6,052	5,70	3,51	305,85	6,091
2	4,88	1,64	302,07	6,004	4,75	1,58	304,02	6,043
3	4,70	1,16	301,55	5,952	4,55	1,08	303,54	6,029
4	4,68	0,95	301,31	5,981	4,55	0,85	303,30	6,024
6	4,63	0,77	300,97	5,974	4,49	0,66	302,96	6,014
8	4,61	0,69	300,92	5,973	4,52	0,57	302,90	6,013
12	4,55	0,64	300,57	5,963	4,51	0,5	302,55	6,003
20	4,40	0,61	300,33	5,951	4,54	0,47	302,31	5,995

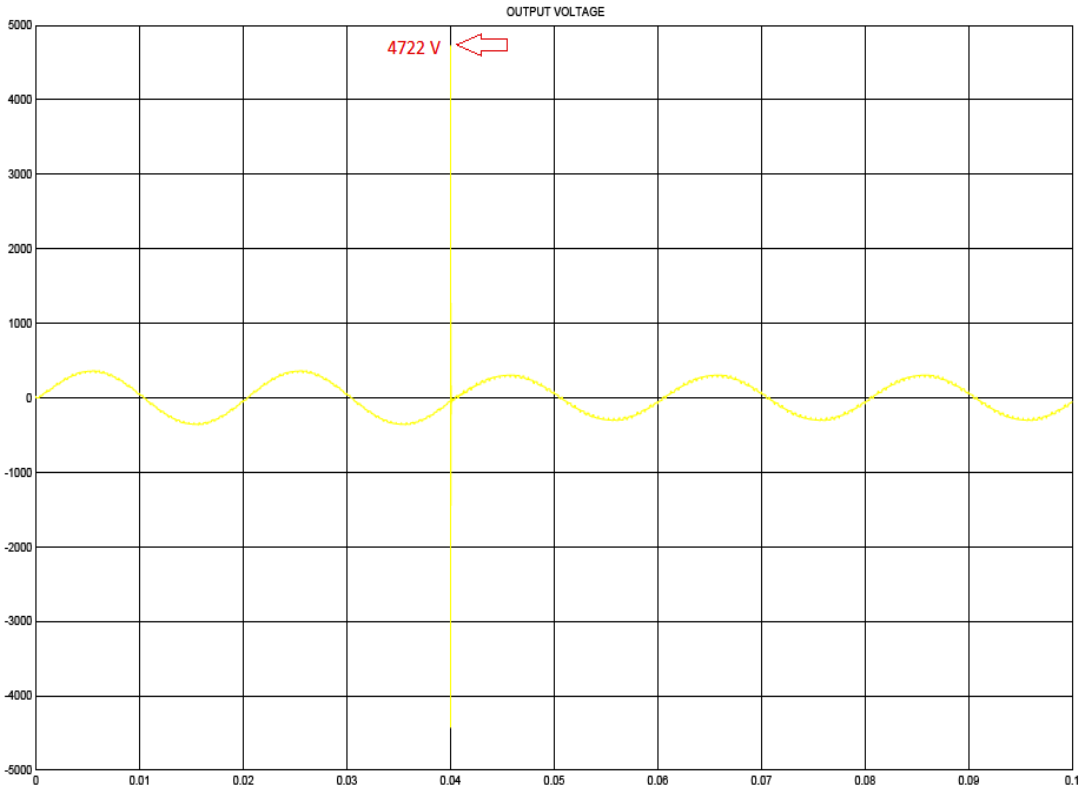


Figure 4.25 : Output voltage when a fault occurred in the third inverter if CS-MOSFETs-BDS is used with R-L load.

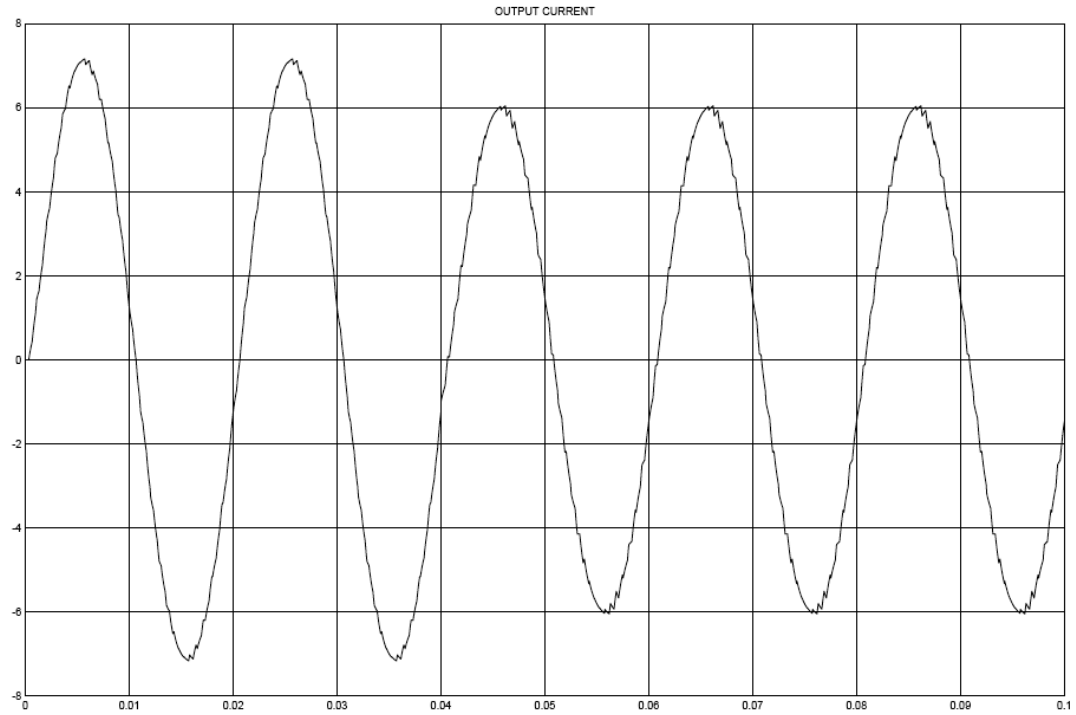


Figure 4.26 : Output current when a fault occurred in the third inverter if CS-MOSFETs-BDS is used with R-L load.

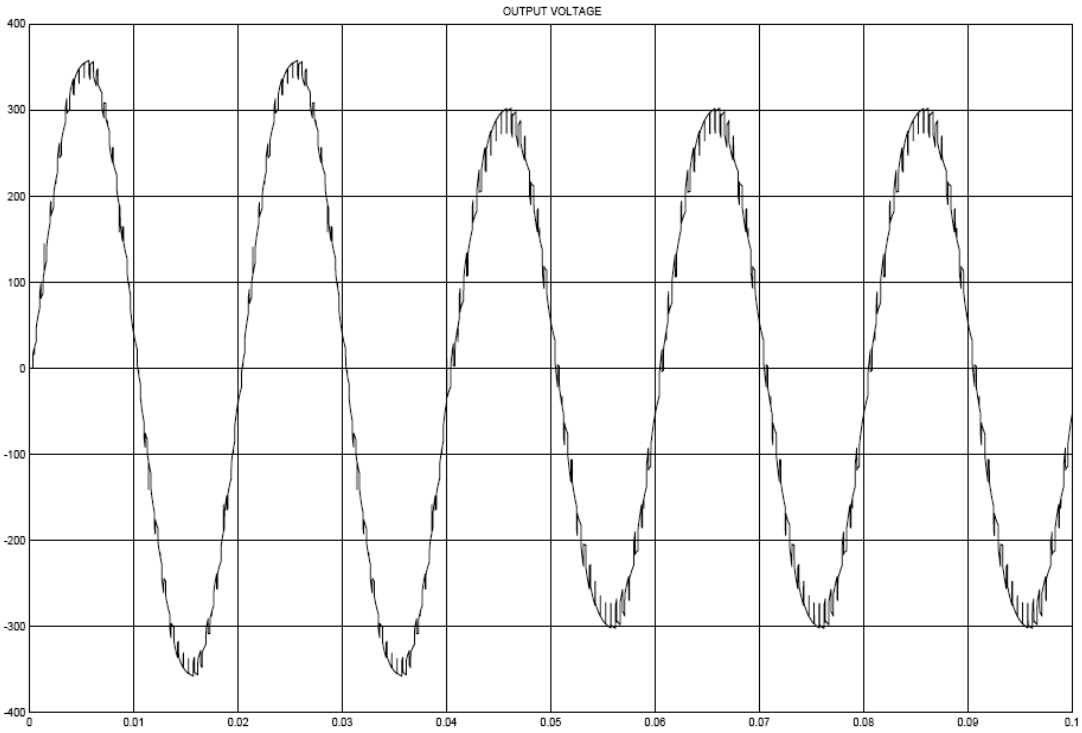


Figure 4.27 : Output voltage when a fault occurred in the third inverter if DB-MOSFET-BDS is used with R-L load.

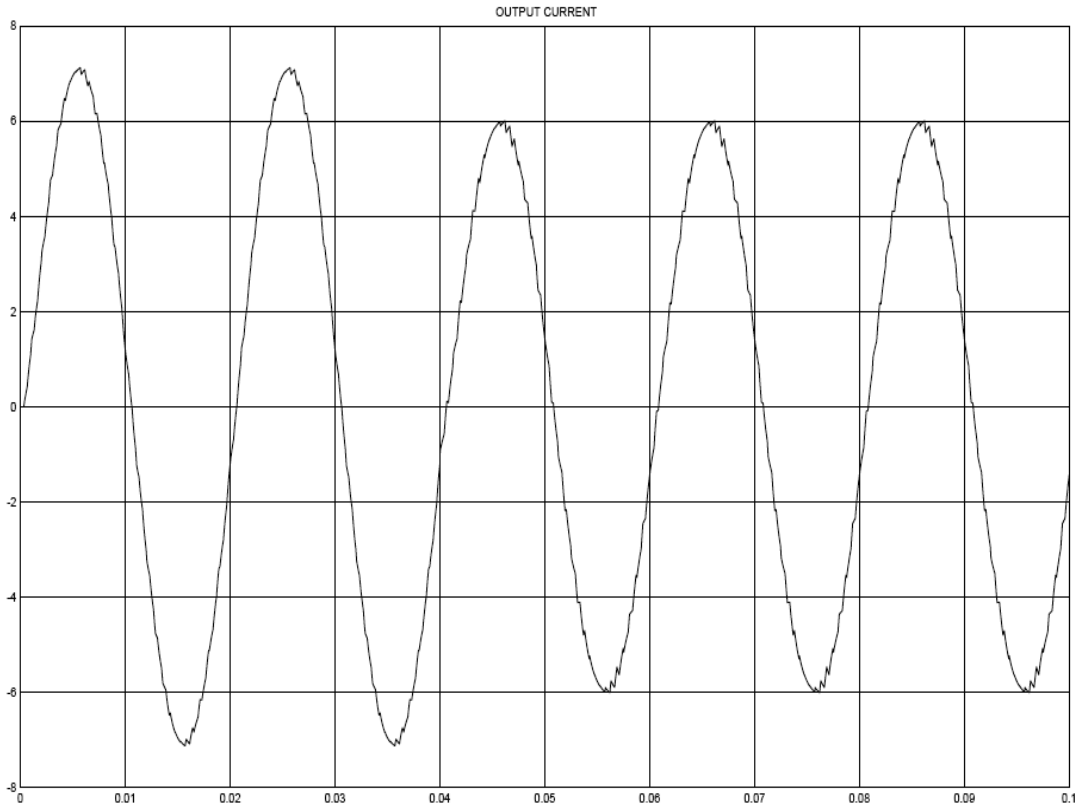


Figure 4.28 : Output current when a fault occurred in the third inverter if DB-MOSFET-BDS is used with R-L load.

5. CONCLUSION

In this thesis, a fault-tolerant cascaded H-Bridge quasi-eight level multilevel inverter with single DC source, output transformers is designed, and reconfiguration technique is applied. The simulations are done in MATLAB-SIMULINK environment. This thesis aims to increase the fault tolerance of the multilevel inverters, which have high number of semi-conductor elements, that is a critical issue for the buildings have vital importance like hospitals and for the institutions where the stopping the whole system causes very much financial loss.

The proposed inverter was grounded on three identical cascaded H-Bridge inverters, which are fed by a single 52V DC source. One of these inverters was modulated by pulse-width modulation while other two inverters are modulated at low switching frequencies to reduce the switching losses. Each H-Bridge inverter was connected to its own transformer and secondary windings of the transformers are connected in series to sum up the produced voltage. The turns ratios of the transformers are identified as exponent 2 which are 1:1, 1:2, and 1:4. In order to provide a fault-tolerant system, four bi-directional switches were used for changing the turns-ratios of the transformers to keep the system working at acceptable voltage levels. If any fault occurs in one of the H-Bridge inverters, the turn-ratios of the transformers and modulation techniques of the H-Bridge inverters are changed, so the proposed system can continue working with one level voltage decrease in quarter cycle. Two types of bi-directional switches: The Diode-Bridge MOSFET bi-directional switches (DB-MOSFET-BDS) and Common Source MOSFETs bi-directional switches (CS-MOSFETs-BDS) were tested separately for no-fault condition and fault conditions of each H-Bridge inverter. Moreover, comparisons were made for these bi-directional switches up to the quality parameters of the output voltage and current, total harmonic distortion and efficiency, with different switching frequencies (1-20 kHz). The simulation results show that the system has nearly 2% THD values when no fault exists and less than 5% THD values at fault conditions without any filtering stage at the output side the proposed system has 78% efficiency in average. Moreover, the results show that the CS-MOSFETs-BDS has 2V less conduction

losses and better THD values when compared to DB-MOSFET-BDS. However, if CS-MOSFETs-BDS is used, some voltage impulses occur at fault instants of the second and third inverters. The efficiency of the proposed inverter is nearly 78% at no fault condition and 77% at fault instants. Moreover, the efficiency is a bit higher when CS-MOSFET is used.

The usage of transformers and bi-directional switches in the designed system increases cost of production and volume of the whole system. However, this proposed inverter can find a place to itself in the inverter market under the class of "reliable inverters".

The future work of this thesis, an inverter can be designed by identifying the turns-ratios of the transformers as exponent 3 ($1:3^0$,$1:3^1$,…). Furthermore, fault tolerance of the system can be increased by designing a new control system, which can keep the system working even if more than one H-Bridge inverter has faults.

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