ULTRA LOW POWER 12-BIT 100 kS/s DIFFERENTIAL SAR ADC IN 65 nm CMOS TECHNOLOGY

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF
ENGINEERING AND NATURAL SCIENCES
OF ISTANBUL MEDIPOL UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL, ELECTRONICS ENGINEERING AND CYBER SYSTEMS

By
Muhammet Ali Dağdibi
February, 2020

ULTRA LOW POWER 12-BIT 100 kS/s DIFFERENTIAL SAR ADC
in 65 nm CMOS TECHNOLOGY
By Muhammet Ali Dağdibi
February, 2020

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Assoc. Prof. Hakan Doğan(Advisor)

Assoc. Prof. Mehmet Kemal Özdemir

Assist. Prof. Mustafa Aktan

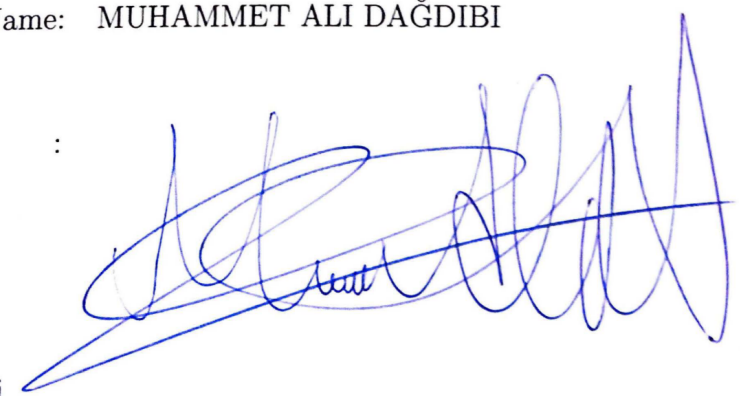
Approved by the Graduate School of Engineering and Natural Sciences:

Assoc. Prof. Dr. Yasemin Yüksel Durmaz
Director of the Graduate School of Engineering and Natural Sciences

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: MUHAMMET ALI DAĞDIBI

Signature :



To Allah, The Creator

"Unless you have a work that will save in the hereafter, do not attach importance to the works that you leave in this world"

- *Al Mathnawi al-Nuriya* -

ABSTRACT

ULTRA LOW POWER 12-BIT 100 kS/s DIFFERENTIAL SAR ADC IN 65 nm CMOS TECHNOLOGY

Muhammet Ali Dağdibi
M.S. in Electrical, Electronics Engineering and Cyber Systems
Advisor: Assoc. Prof. Hakan Doğan
February, 2020

Sensor nodes has preserved their importance in the last couple decades. One of the very fundamental elements of these devices are analog to digital converters. In today's world, the necessity of sensor nodes and implantable devices working with very low power levels requires converters which can work with low powers. In this thesis, the design of an ultra low power analog-to-digital converter which can satisfy this requirement is explained. Differential structure and monotonous switching technique is used in the design. While a maximum SNDR of 70.26 dB and a minimum power consumption of 2.3 uW is observed in spectre simulations, post-layout simulations showed that maximum of 64.36 dB SNDR and minimum of 2.1 uW power consumption values can be obtained. The circuit is designed with 65 nm CMOS technology in Cadence Virtuoso software, its layout is verified with Calibre and it is sent to UMC foundry through Europractice to be manufactured. When the ADC is received back, it will be measured for performance verification and results will be published in high impact journals or conferences.

Keywords: ADC, DAC, Converter, SAR, CMOS.

ÖZET

65 nm CMOS TEKNOLOJİSİNDE AŞIRI DÜŞÜK GÜÇLÜ 12-BİT 100 kS/s DİFERANSİYEL SAR ADC

Muhammet Ali Dağdibi
Elektrik-Elektronik Mühendisliği ve Siber Sistemler, Yüksek Lisans
Tez Danışmanı: Doç. Dr. Hakan Doğan
Şubat, 2020

Sensör düğümleri geçmişten bugüne önemini daima muhafaza etmiştir. Bu cihazların olmazsa olmaz parçalarndan biri de analog-sayısal çeviricilerdir. Günümüz dünyasnda oldukça düşük güçte çalışabilen sensör düğümleri veya insan vücuduna takılabilir cihazlara duyulan ihtiyaç yine beraberinde düşük güçte çalışabilecek çeviricileri de gerekli kılmıştır. Bu tez çalışmasında bu ihtiyaca cevap verebilecek şekilde aşırı düşük güçte çalışabilecek bir analog-sayısal çevirici tasarımı anlatılmştır. Tasarımda diferansiyel yapı ve monoton anahtarlama tekniği kullanılmıştır. 0.7V besleme voltajı, 100 kHz örnekleme hızı ve gürültü etkisi de dahil edilerek, serim öncesinde yapılan benzetimlerde maksimum 70.26 dB SNDR ve minimum 2.3 uW güç tüketimi gözlemlenirken serimin tamamlanmasıyla birlikte maksimum 64.36 dB SNDR elde edilmiş ve minimum 2.1 uW güç tüketimi gözlenmiştir. Devre 65nm CMOS teknolojisi ile Cadence Virtuoso programı kullanılarak tasarlanmış, serim kontrollerinde Calibre aracı kullanılmış ve Europractice aracılığıyla UMC fabrikasında üretime yollanmıştır. ADC'nin üretimden gelmesiyle birlikte ölçümlerinin yapılması planlanmakta ve yapılan çalışma etkili konferans veya makalelerde yayın haline getirilerek literatüre katkıda bulunulması hedeflenmektedir.

Anahtar sözcükler: ADC, DAC, Çevirici, SAR, CMOS.

Acknowledgement

Before acknowledging anyone or anything, first I would like to thank to Allah that he enabled me to finish my Master's study.
I also would like to express my deep gratitude to my advisor, Assoc. Prof. Hakan Doğan, for his great support, help, patience and tolerance during my research and during the time I have known him. He always answered my questions, helped to solve many of my problems, kept his doors open at all times and was quick on replying to me as well. I also would like to show my appreciation to Dr. Mustafa Aktan. He helped me whenever I ran into any trouble or got stuck somewhere in my project. Many times I knocked his door and he never complained even about my simple, basic questions and lack of understanding. I am grateful to my team mate Mohamed Kamar, too, as he has helped and motivated me in my study.
I also would like to express my heartful thanks to my mother, father, sister and many of my friends as they have been with me during this study.
I am grateful to my thesis committee member Assoc. Prof. Kemal Özdemir as he attended my thesis defence presentation.
This thesis was supported by TUBITAK under the Ardeb projetc with number 215E289.

Contents

List of Abbreviations

AAF Anti Aliasing Filter

ADC Analog-to-Digital Converter

CDAC Capacitive Array DAC

DNL Differential Nonlinearity

ENOB Effective Number of Bits

FOM Figure of Merit

INL Integral Nonlinearity

LSB Least Significant Bit

PSD Power Spectral Density

RMS Root Mean Square

S/H Sample and Hold

SAR Successive Approximation Register

SFDR Spurious Free Dynamic Range

SNDR Signal to Noise + Distortion Ratio

SQNR Signal to Quantization Noise Ratio

THD Total Harmonic Distortion

List of Figures

List of Tables

Chapter 1

Introduction

The physical features of the world that we, the glorious human beings, are living in can be expressed with analog signals in electrical domain. Those features like temperature, pressure, sound, color is sensed by transducers and a continuous analog voltage signal is generated for each of them to be used in media devices, for example.

Traditional systems like commercial audio power amplifiers are analog. Since they produce pure uncompressed sounds, they can directly use the analog signals. On the other hand, these analog signals generated by transducers might need to be compressed or processed in any entertainment device. Since computer world speaks with binary numbers which are digital, it doesn't understand the language of real world which is analog. Therefore an interface should be used in between the two worlds and it is Analog-to-Digital Converter (ADC) or Digital-to-Analog Converter (DAC).

An ADC converts the analog signal into digital bits which is illustrated in Figure 1.1 [3]. There are different types of ADC architectures. Each of them is preferable depending on the specifications of applications. Some of the requirements are accuracy (resolution), speed, power, size and complexity. Each of these parameters will be explained in detail in the coming chapters. The content of the rest of the

chapters are as follows.

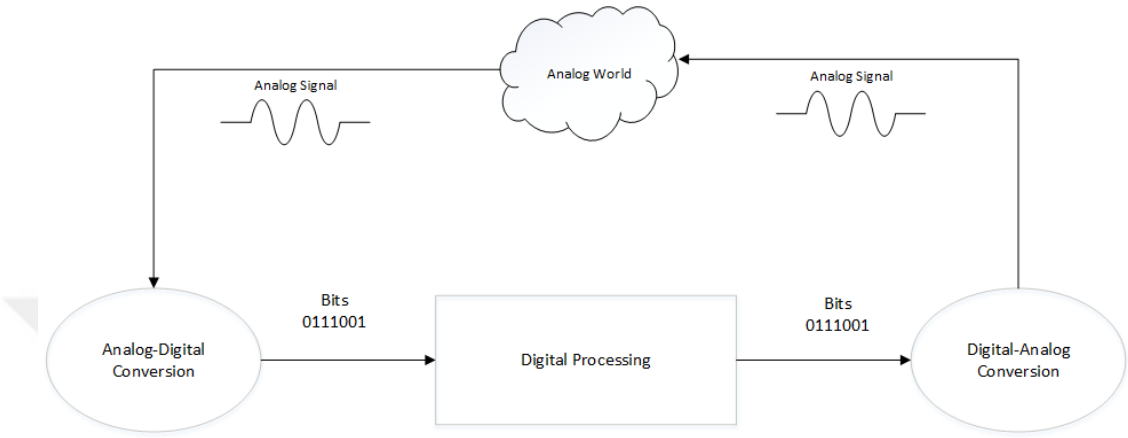


Figure 1.1: Illustration of the conversion between analog and digital world

Chapter 2 shows a literature review about ADCs. Chapter 3 reviews the fundamentals of SAR ADC. The implementation of proposed SAR ADC is explained in chapter 4. Thesis concludes with Chapter 5.

Chapter 2

Literature Review about ADC

2.1 Introduction

While real world signals are analog, computers talk with digital words. ADCs act as an interface in between the two worlds. They convert analog signals into digital words. Figure 2.1 gives a summary of this conversion. As also shown in figure, analog input is passed through an anti-aliasing filter (AAF) in order to keep bandwidth limited. By this way, the high frequency signals are prevented from being aliased back on top of the original signal. Then a Sample&Hold (S/H) circuit samples the input and gives it to the quantizer to be quantized. At the end, a digital signal processor (DSP) block produces the digital bits. This process will be explained in detail in the coming sections.

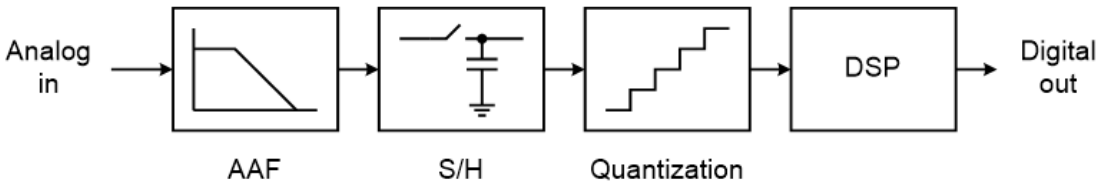


Figure 2.1: Analog to digital conversion block diagram

In this chapter, the fundamentals of ADC, its working principles and different ADC architectures will be explained.

2.2 Basics of ADC

ADC converts an analog signal into digital bits in the following way. Samples are taken from applied analog signal at certain time instants which is illustrated in Figure 2.2. By this way, discrete time representation of continuous analog signal is obtained as observed from the equation 2.1. However, there might be aliasing in this sampling stage. Aliasing is studied in subsection 2.2.1.

$$\begin{aligned} m(t) &= cos(\omega t) \quad with \quad t = nT_s \, (T_s : SamplingPeriod) \\ m(n) &= cos(\omega n T_s) \end{aligned} \tag{2.1}$$

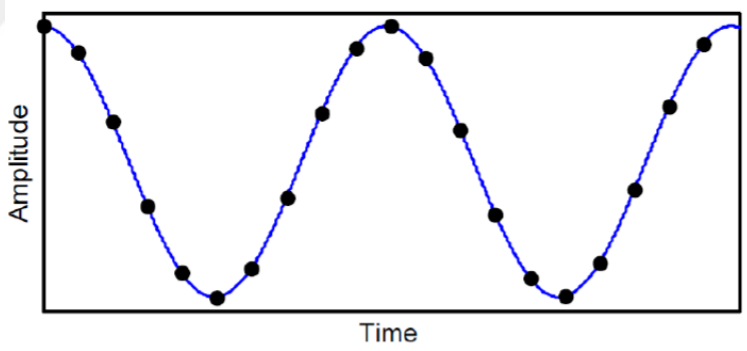


Figure 2.2: Discrete samples of analog signal

As shown in figure 2.1, digitized signal is then quantized and is ready to be expressed with a binary number. Figure 2.3 shows how the quantized signal is represented. Quantization is further investigated in subsection 2.2.3.

2.2.1 Aliasing

Aliasing happens when an unwanted signal folds over the desired signal and becomes inseperable from the original signal after sampling. To understand aliasing better, one can take a look at figure 2.4. As shown in figure 2.4, the signals at frequencies $N \cdot f_s \pm f_m$ fold back to main tone.

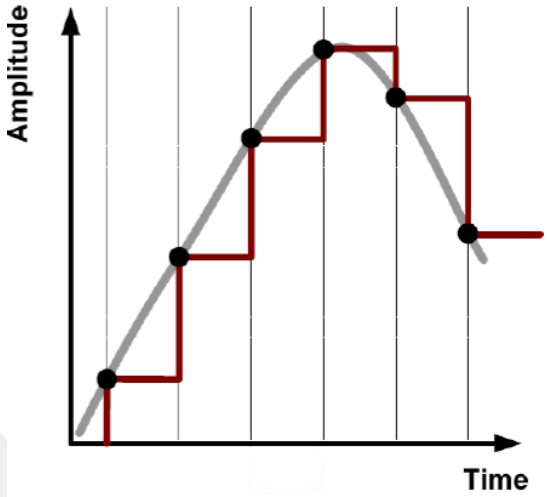


Figure 2.3: Quantized Analog Signal

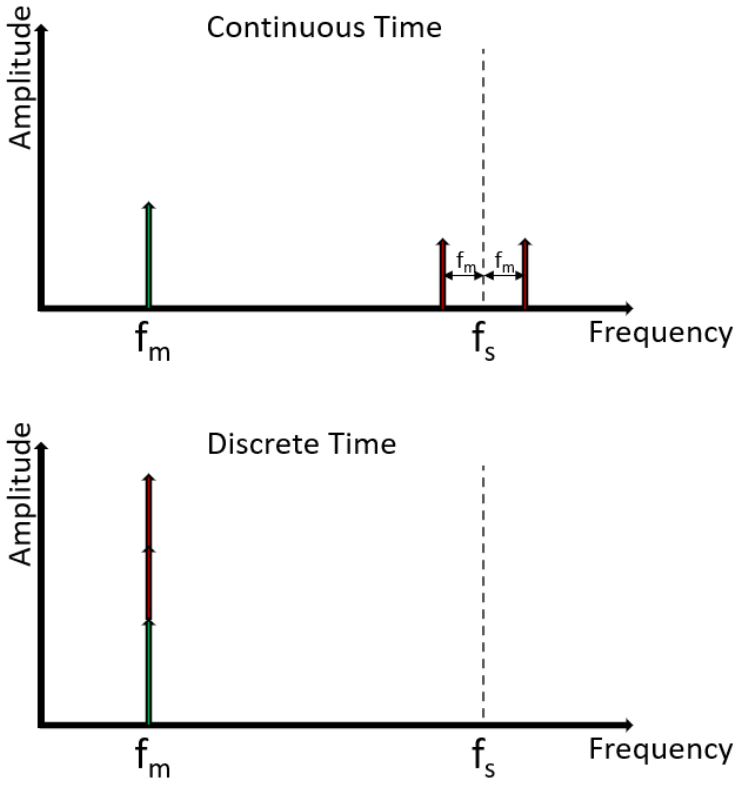


Figure 2.4: Aliasing effect on signal discretization

Aliasing can be examined through mathematical representations of the signals, too. Suppose the desired signal frequency is 201 kHz and sample rate is 1 MHz. According to equation 2.1, sampled signal becomes

$$\begin{aligned} m(n) &= cos(\omega \frac{n}{f_s}) \\ &= cos(2\pi \frac{201}{1000} n) \end{aligned} \tag{2.2}$$

If a signal with frequency 799 kHz comes to ADC, then its discrete version has the same frequency as the original signal, which is shown in equation 2.3.

$$\begin{aligned} m(n) &= cos(2\pi n \frac{799}{1000}) \\ &= cos(2\pi (1 - \frac{799}{1000}) n) \\ &= cos(2\pi \frac{201}{1000} n) \end{aligned} \tag{2.3}$$

Aliasing can be avoided by guaranteeing the maximum input frequency signal does not exceed half of the sampling rate. This is called the *Nyquist Theorem*. Otherwise signals might be interpreted with wrong frequencies after they are sampled. Moreover, putting an 'anti-aliasing filter' preceding the sampler, as seen in Figure 2.1, could also prevent aliasing. This filter has low-pass characteristics so it blocks high frequency signals.

2.2.2 Oversampling

Oversampling is sampling with a sample rate more than two times the maximum input frequency. It decreases the burden on anti-aliasing filter. Ideally, an anti-aliasing low-pass filter expected to have pure brick wall response, as shown in Figure 2.5, but the implementation of such a filter is not easy practically. Therefore, real filters have a non-zero roll-off factor and are not able to reject parasitic tones completely if sampling rate is not high enough, which is represented in Figure 2.6.

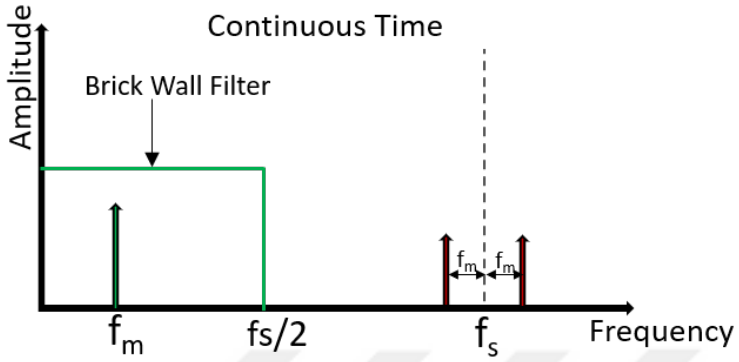


Figure 2.5: Sampling with Brick Wall filter

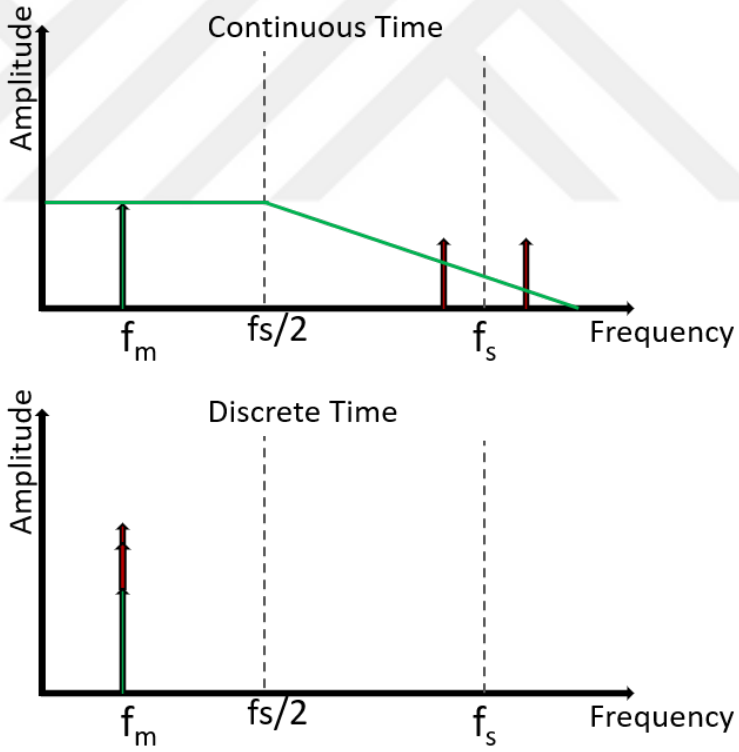


Figure 2.6: Sampling with practical filter

By utilizing high sampling rate, this problem might be overcomed. Then 'how fast should it be?' is a question, which may come to reader's mind. This question might be answered considering the trade-off between the sampling speed and filter steepness[4], which in turn sets the filter order, as shown in Figure 2.7.

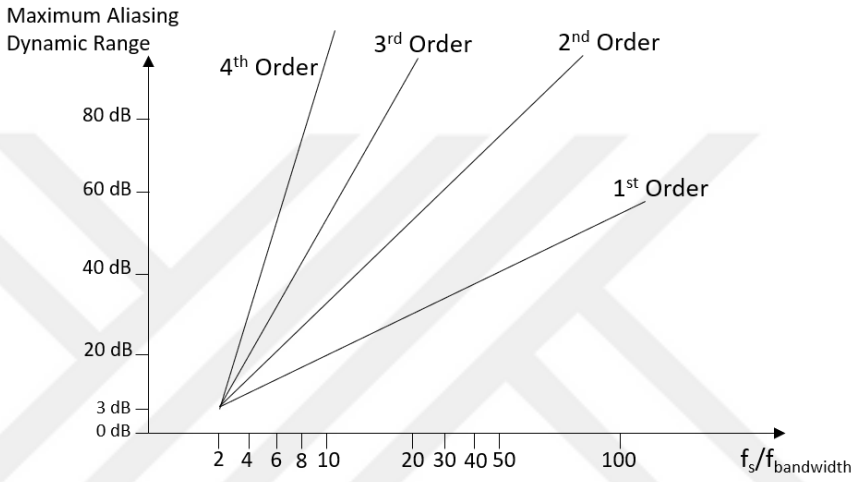


Figure 2.7: Relation between filter order, dynamic range and oversampling ratio

2.2.3 Quantization

Quantization is a process of assigning analog input values to predefined discrete levels. It is the combination of division, normalization and truncation [1]. Depending on the number of bit (n), there are 2^n intervals. Full scale voltage, which is highest accepted input signal value, is divided into 2^n intervals and every small voltage value in these intervals are assigned to a certain quantization level. The process could be imagined through the help of Figure 2.8.

The smallest amount of voltage change required for input to be assigned into the next quantization level is called '*least significant bit, LSB*'. In equation 2.4, the calculation of LSB is shown.

$$\Delta = \frac{V_{FS}}{2^n} \tag{2.4}$$

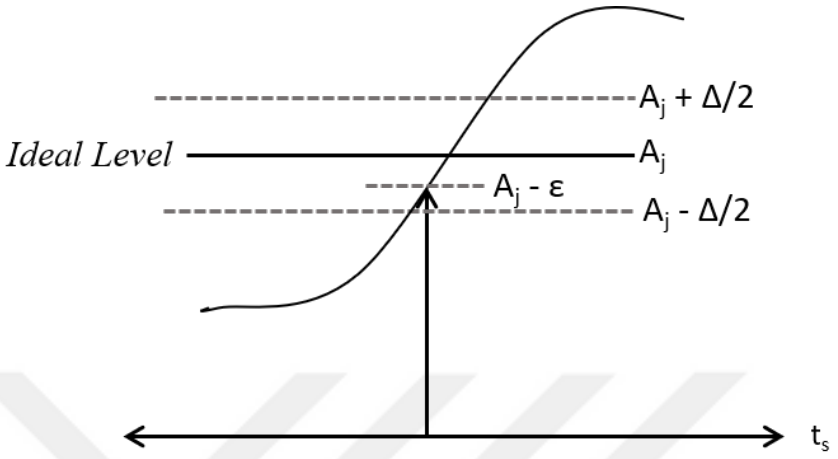


Figure 2.8: Assigning analog voltage values to set levels

Figure 2.9 shows an example of 3 bit quantization of a ramp signal. As shown in the figure, input is divided into $2^3 = 8$ intervals. On the other hand, some sources [4] does not count 'zero' as a level and they express the number of quantization levels with $2^n - 1$.

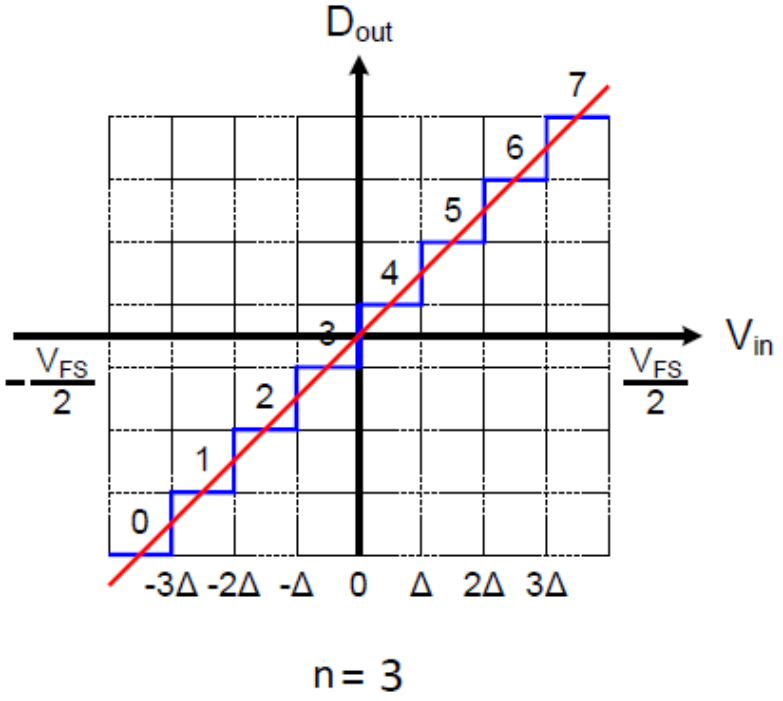


Figure 2.9: Quantization of a ramp signal for n=3

2.3 Performance Metrics

2.3.1 SNR

Since continuous signals have infinite number of levels and quantized signals have finite number of levels, there will always be a loss of information, which is called '*quantization error*'. Figure 2.10 shows the graph of this error for the previous example of $n = 3$. This error is also called '*quantization noise*' and could be calculated as shown in equation 2.5.

$$\varepsilon = D_{OUT}\Delta - V_{in} = D_{OUT}\left(\frac{V_{FS}}{2^n}\right) - V_{in} \tag{2.5}$$

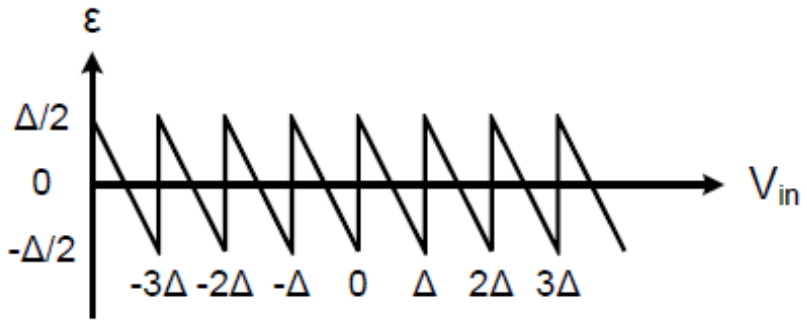


Figure 2.10: Quantization error signal for a ramp input for n=3

As seen from Figure 2.10, quantization error signal for a ramp input is *sawtooth* shape and it is always in between $-\frac{\Delta}{2}$ and $+\frac{\Delta}{2}$, as shown in equation 2.6. Furthermore the spectrum of quantization error is assumed flat from $-\frac{\Delta}{2}$ to $+\frac{\Delta}{2}$ with zero mean which is shown in Figure 2.11

$$-\frac{\Delta}{2} < \varepsilon < +\frac{\Delta}{2} \tag{2.6}$$

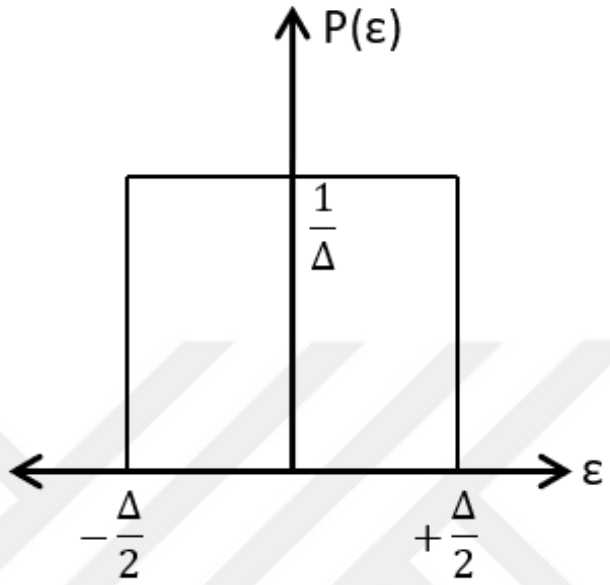


Figure 2.11: Power Spectral Density (PSD) of Quantization Noise

Based on this assumption, quantization error power could be calculated as,

$$\begin{aligned} q_{rms}^2 = E(\varepsilon^2) &= \int_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} \varepsilon^2 d\varepsilon \\ &= \frac{\Delta^2}{12} \end{aligned} \tag{2.7}$$

If a sine wave is applied to the ADC, its power can be represented as,

$$P_{sig} = \left(\frac{\frac{V_{FS}}{2}}{\sqrt{2}}\right)^2 = \frac{{V_{FS}}^2}{8} \tag{2.8}$$

Dividing eq. 2.8 by 2.7, SNR (Signal-to-Noise Ratio) can be obtained as,

$$\begin{aligned} SNR &= \frac{\frac{{V_{FS}}^2}{8}}{\frac{\Delta^2}{12}} \\ &= 1.5 \times 2^{2n} \end{aligned} \tag{2.9}$$

and its logarithmic representation is,

$$SNR = 6.02 \times n + 1.76 \quad dB \tag{2.10}$$

This is the ideal case, where only quantization noise is considered. It is also called SQNR(Signal-to-Quantization-Noise-Ratio) according to [1]. There are other noise sources as well and some of them can be listed as flicker noise, thermal noise, clock jitter, et al. While calculating actual SNR, all these noise sources are taken into account. Nonetheless, the designer generally tries to make these noise levels less than quantization noise so that it become the dominating noise source.

2.3.2 SNDR

The difference between SNDR and SNR is the nonlinear distortion terms generated by input sine wave. SNDR is the ratio of input signal power to circuit noise and harmonics. Both the amplitude and frequency of input signal affects the SNDR. Figure 2.12 [5] shows this relation. As shown in the figure, when the signal amplitude drops by 20dB, the SNDR only drops by around 17dB, which indicates that the distortion dominates when the input amplitude is high.

2.3.3 Dynamic Range

Dynamic range is the signal amplitude range that a converter can resolve. An 80 dB dynamic range ADC can resolve signals with amplitude ranging from k to $10^4 k$. Signals above this range might over-range (overload) the ADC input and signals below this range might not be detected as they are below the quantization noise floor. Figure 2.13 gives the graphical representation of the dynamic range.

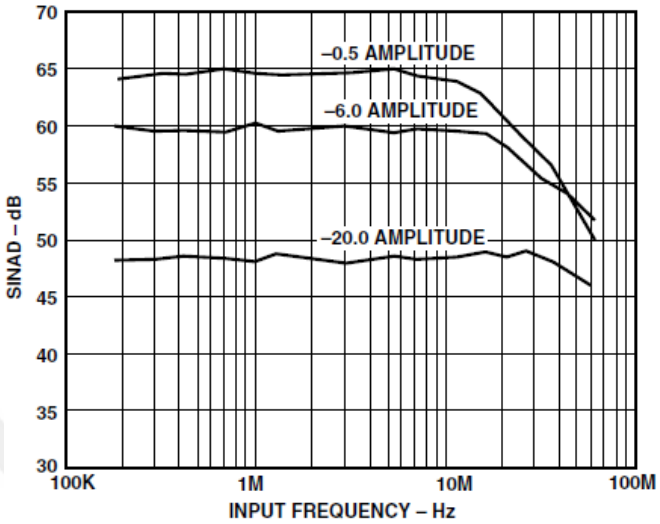


Figure 2.12: SNDR of a hypothetical converter with $f_s = 50MHz$

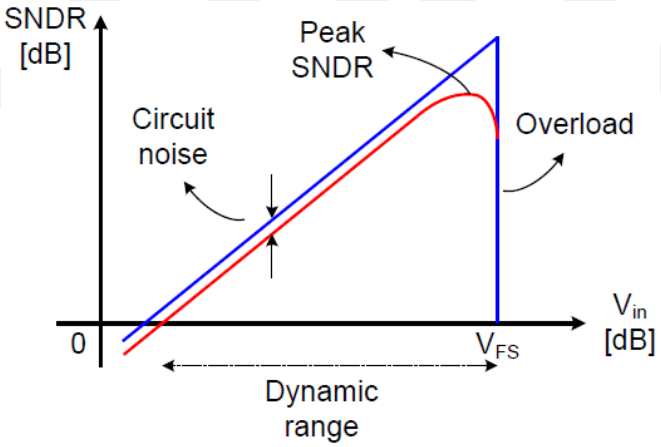


Figure 2.13: SNDR vs input amplitude graph

2.3.4 Total Harmonic Distortion

Although applied input is a sine wave with specific amplitude and frequency, the converter might give multiple output signals where each of which has a different frequency that are multiples of the fundamental one. These frequencies are called 'harmonics' of the input frequency and any nonlinearity in a practical converter results in harmonics.

As a measure of nonlinearity, the ratio between the sum of rms powers of signal's harmonics and the rms power of the input signal gives the total harmonic distortion (THD) which is also shown in 2.11.

$$THD(dB) = 20\log\left(\frac{V_{2,rms}^2 + V_{3,rms}^2 + V_{4,rms}^2 + V_{5,rms}^2 + ...}{V_{1,rms}^2}\right) \tag{2.11}$$

2.3.5 SFDR

The ratio between the rms amplitude of the fundamental signal and the next highest spurious spectral component gives *Spurious Free Dynamic Range*. Reader should mind that DC is not considered as one of the spurs.

SFDR does also depend on input amplitude. The highest spur might be one of the harmonics of a large signal. If the signal amplitude is well below the full scale, then other tones, due to converter's nonlinearity, might be dominating [5].

SFDR is generally expressed as a function of input amplitude and represented with dBc (dB below carrier). In this case, SFDR curve takes a linear form and it takes 0 dBc value when the highest spur's amplitude is eqaul to input. However it might sometimes be represented with dBFs (dB Full scale), too. In the latter case, it is always assumed that full scale input is applied and doesn't change as the input changes. Figure 2.14 [5] gives a good illustration about this phenomenon.

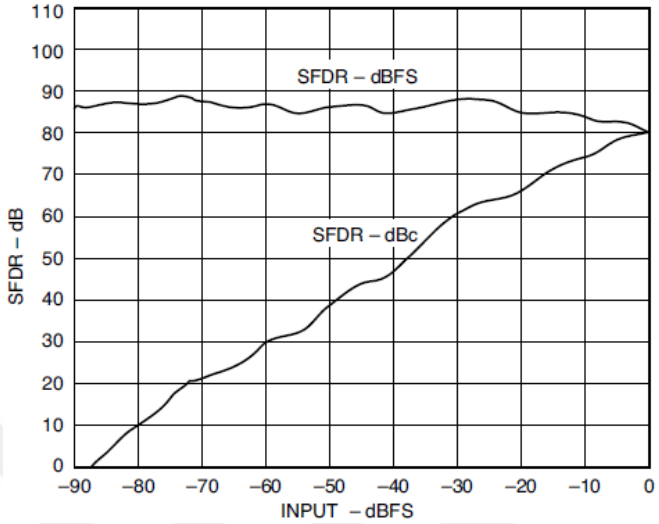


Figure 2.14: SFDR plot with dBc and dBFs units

2.3.6 ENOB

ENOB stands for '*Effective Number of Bits*'. Due to noise and distortion, the designer could not obtain the intended resolution. ENOB may be regarded as 'number of useful bits', too. For example, a 12-bit ADC can actually give 10.5-bit, effectively. Equation 2.12 gives this relation for a practical ADC.

$$SNDR = 6.02 \cdot n + 1.76\,dB,\ n : ENOB \tag{2.12}$$

2.3.7 Offset

Offset is the departure of starting point of transfer characteristic of ADC from the ideal value [1]. It is defined in terms of LSB. An offset is shown in Figure 2.15.

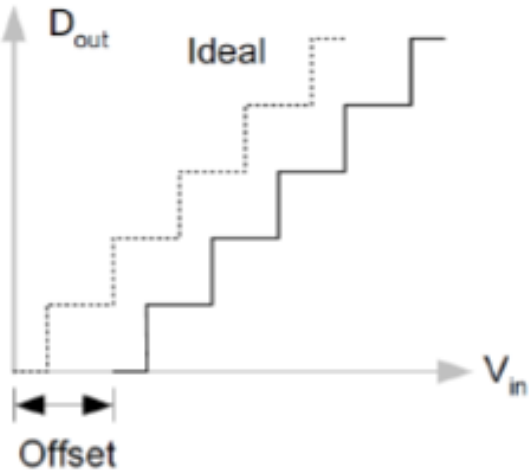


Figure 2.15: Offset in transfer curve of ADC

2.3.8 Gain Error

Gain error is the departure of last endpoint of transfer characteristic of ADC [1] from the ideal. Figure 2.16 shows the gain eror in transfer curve.

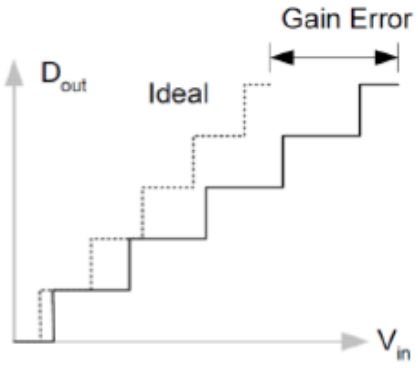


Figure 2.16: Gain error in transfer curve of ADC

Lots of converters are insensitive to both gain error and offset to certain degree. Furthermore, these errors could be corrected with some digital calibration techniques.

2.3.9 Monotonicity

In a monotonic ADC, output codes follow input. Output increases if input increases or decreases if input decreases. So, the output code changes in the same direction as the input [5]. In figure 2.17, a non-monotonic ADC transfer curve is shown.

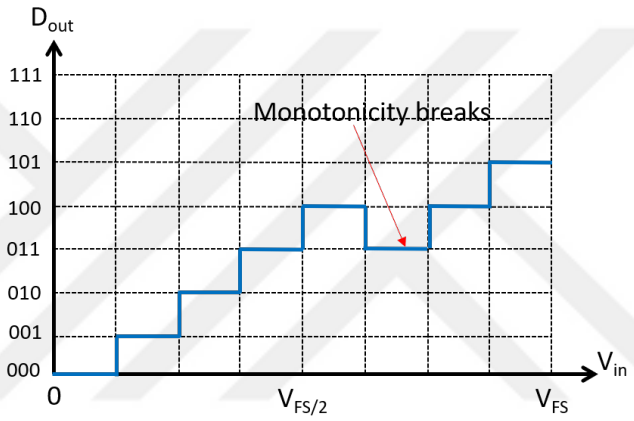


Figure 2.17: Sample nonmonotonic ADC transfer curve

As Figure 2.17 shows, although input increases at fifth step, output code decreases. This breaks the monotonicity feature.

2.3.10 Differential Nonlinearity

In a normal transfer characteristic of ADC, output code should change at every LSB step of input voltage. If this code change happens before or after an LSB change of input, then ADC looses its linearity. This type of step-wise error is named DNL, differential nonlinearity. Figure 2.18 shows an ideal voltage transfer characteristic of an ADC while Figure 2.19 shows a voltage transfer characteristic with 1 LSB DNL error.

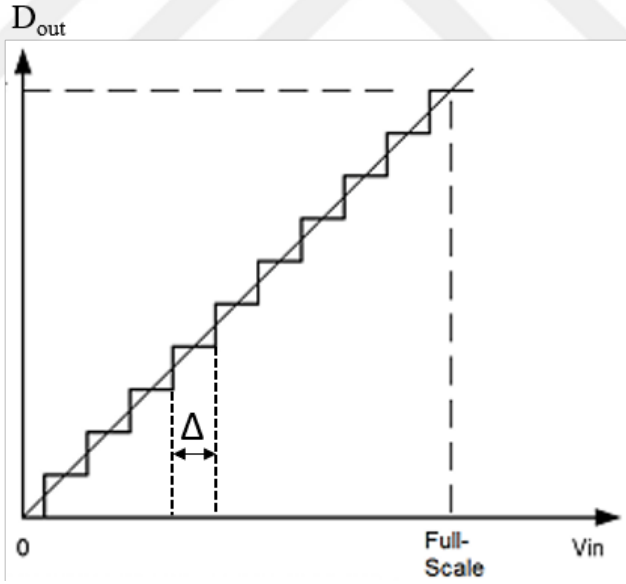


Figure 2.18: Ideal voltage transfer characteristic of ADC

Considering the explanations above, DNL can be formulated as

$$DNL_i = \frac{i^{th} StepSize - \Delta}{\Delta} \tag{2.13}$$

Moreover, one can see another type of DNL error, which also resulted in *missing code* in Figure 2.20.

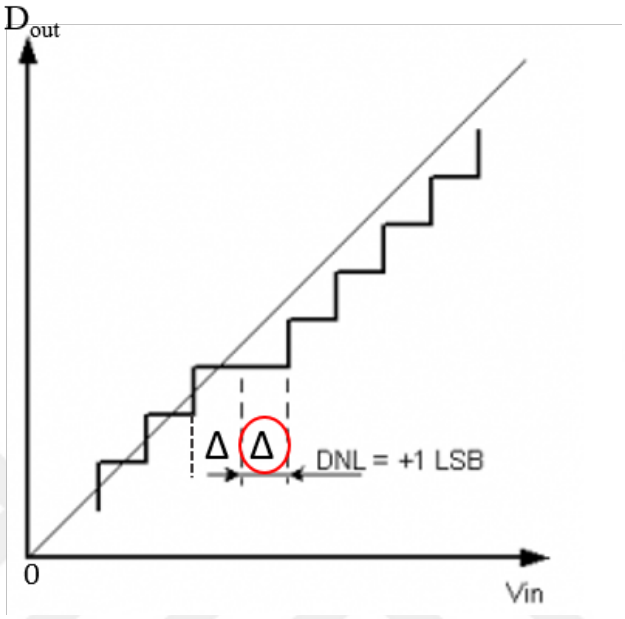


Figure 2.19: Voltage transfer characteristic of ADC with 1-LSB DNL error

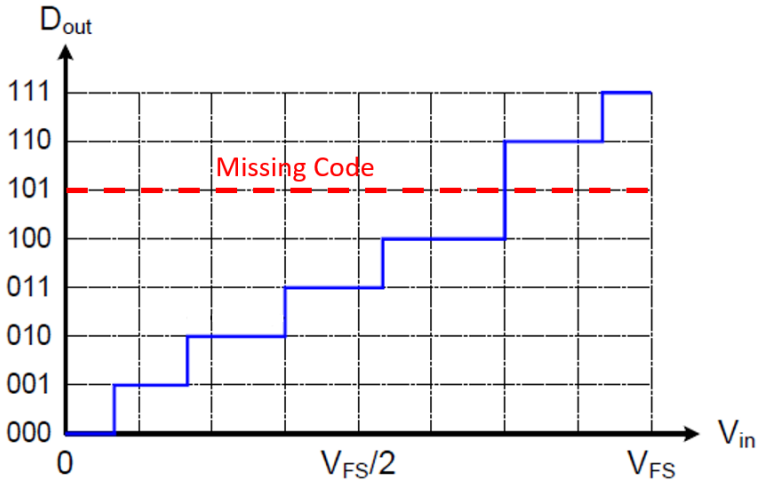


Figure 2.20: DNL error resulting in missing code

2.3.11 Integral Nonlinearity

The maximum deviation of the ADC transfer curve from the ideal line is defined as INL (Integral Nonlinearity) [6]. In order to express the error, a straight fictitious line passing through each end-point is drawn. This method is called 'end-point

line'. The maximum deviation of actual transfer curve from this line is considered as INL. This method is used to eliminate offset and gain errors in INL calculations [7]. Figure 2.21 illustrates the method.

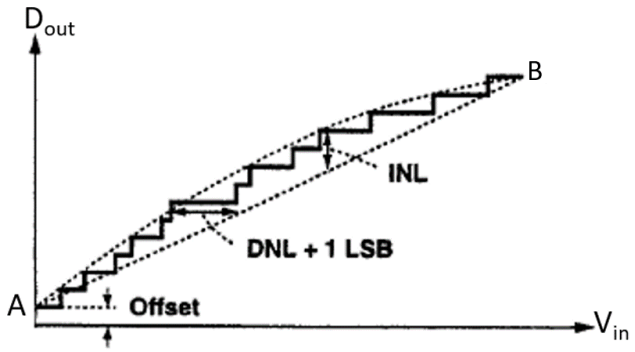


Figure 2.21: INL error of ADC

Another method is called 'best-fit line'. In this method, a best-fit line passing through each step is found and ideal converter steps are detected. The difference of the real line and the ideal line is the INL, as shown in Figure 2.22.

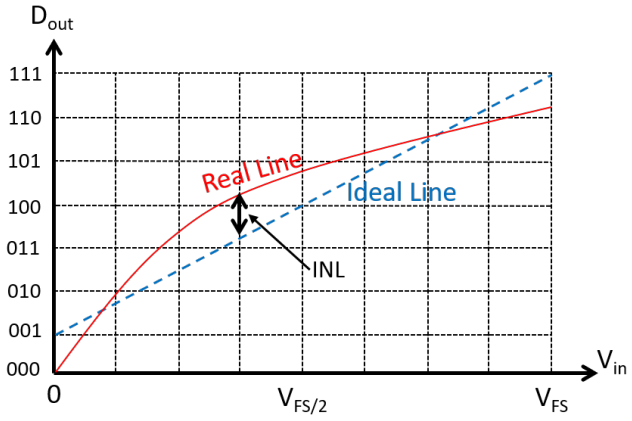


Figure 2.22: INL error using best-fit method

INL can also be considered as the cumulative sum of DNL as formulated in 2.13.

$$INL[m] = \sum_{i=1}^{m-1} DNL[i] \tag{2.14}$$

Large INL results in harmonic distortion and large DNLs lead to INL with large random components. All of these errors add up to noise and it causes SNR degredation [5].

2.3.12 Clock Jitter

Jitter is the deviation of the actual sampling time from the ideal sampling time. Sample-and-hold circuit should sample the signal periodically, i.e. at every certain time instant (T, period), however jitter breaks this periodicity. For example, if one sampling occurs at t_0, the other should occur at $t_0 + T$ ideally, but because of jitter it occurs at $t_0 + T + \epsilon$. Jitter adds to the noise of the converter and its spectrum is assumed to be white.

2.3.13 Figure of Merit (FOM)

As a numerical quantity, figure of merit is used as a measure of effectiveness, efficiency or performance of a system to compare it with its alternatives [8]. As mentioned in the previous sections, there are multiple performance metrics of an ADC. An ADC might be good in resolution (or in power, integrity, etc.), while it might not be fast enough. In order to construct a usable figure of merit FOM, only a subset of those metrics may be used. Used metrics typically are resolution, conversion rate and power consumption. These metrics are combined in different ways.

The combination of these metrics depend on the limitation factors of the designs. In [9], FOM is defined as

$$FOM_W = \frac{P}{f_s \cdot 2^{ENOB}} \tag{2.15}$$

This definition accepts the process technology, CV^2, as a limiting factor and power per conversion rate (P/f_s, energy) grows by 2 times per bit according to it.

In [10], FOM is defined as

$$FOM_{S,DR} = DR + 10\log(\frac{BW}{P}) \tag{2.16}$$

It accepts thermal noise as a limiting factor and ignores distortion. According to it, power per conversion rate (P/f_s, energy) grows by 4 times per bit.

In [11], FOM is defined as

$$FOM_S = SNDR + 10\log(\frac{f_s/2}{P}) \tag{2.17}$$

According to this definition, power grows by 4 times per bit and it includes distortion, too.

2.4 ADC Architectures

Depending on the users' needs, there are multiple types of ADC architectures. Each of them has different advantages and is useful for different types of applications. An illustration of their specialities is shown in Figure 2.23 [1]. In this section some of them will be explained. *

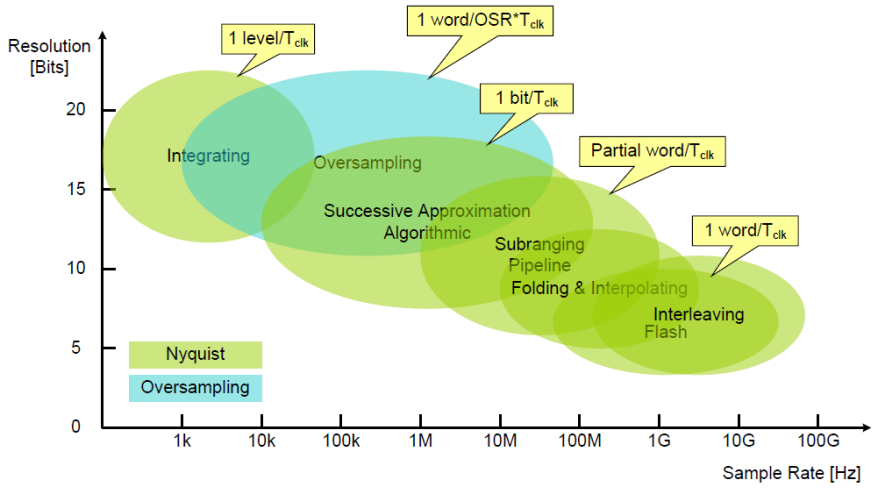


Figure 2.23: Accuracy vs speed comparison of different ADC architectures

2.4.1 Flash ADC

Converting an analog signal into digital bits in one clock pulse might be very effective for applications which require faster operations. Flash ADC is useful for

*Since SAR ADC is the main topic in this thesis, it is not explained in one sub-section but a complete chapter (Chapter 3) is reserved for it.

these kind of applications where high speed is required and medium resolution is acceptable. One of the factors that makes Flash ADC attractive for designers is its simplicity. As Figure 2.24 shows, there are limited building blocks in this structure. Flash ADC applies the basic working principle of analog to digital

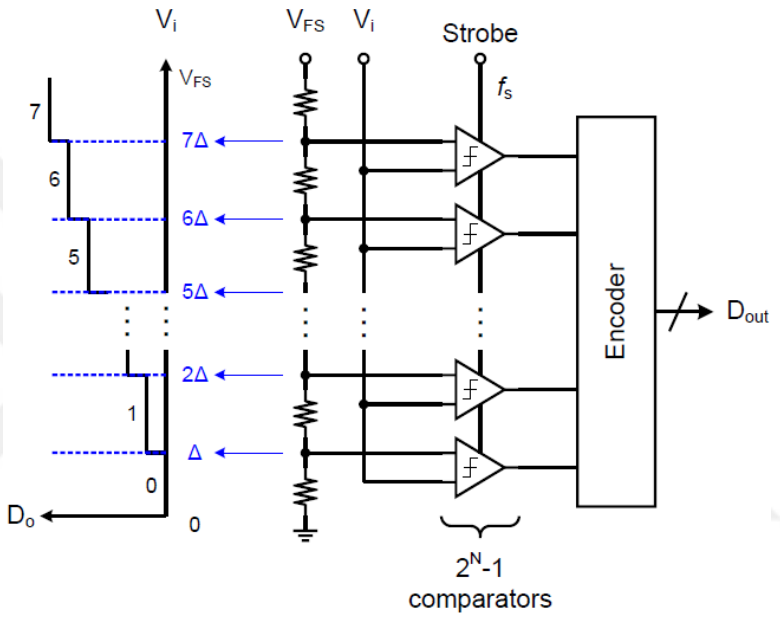


Figure 2.24: Flash ADC Architecture [1]

converters where reference voltage is divided into levels with a resistor ladder and each voltage is fed into a comparator. Then, each comparator compares the analog input voltage with a given voltage level and outputs zero or one. Through this process, the level of the analog input relative to a reference voltage is determined and a thermometer-like code is generated. This code is then converted into a binary digital code through an decoder.

Since the analog input is compared with all reference levels in one clock cycle, Flash ADC might be the fastest one among other ADC architectures. However, the factors like resolution and power consumption limits its usage. For an N-bit Flash ADC, 2^N equal size resistors and $2^N - 1$ comparators are needed. This means, for instance, for a 10-bit ADC designer needs to use 1024 resistors and 1023 comparators which is not that feasible. Considering process variations, it is really hard to obtain exact voltage references with this high number of resistors. Furthermore, since comparator is the most power consuming block in an

ADC, there will be extensive power consumption in high resolution Flash ADCs. Furthermore, total area for such high number of resistors and comparators is another concern. Therefore, it is not common to see Flash ADC's with resolutions greater than 7 or 8 bits in literature or industry.

2.4.2 Folding ADC

Full-scale input is applied to comparators in one step in Flash ADCs, however it may also be passed through a non-linear transformation [5]. One of the non-linear transformation techniques is folding the signal. In this method, signal is divided into segments and a linear response is obtained inside each segment which is shown in Figure 2.25. Instead of quantizing full dynamic range at once, those

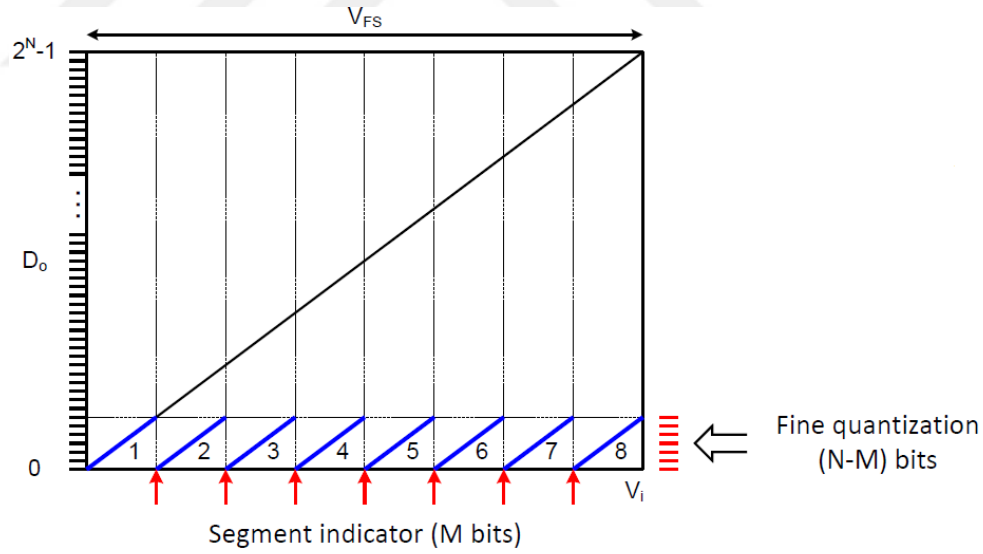


Figure 2.25: Dividing full-scale input into small segments [1]

small segments are quantized step by step. Therefore less number of comparators are used and accuracy is increased because of fine quantization. Looking from this perspective, folding ADC may be considered in the class of '*Multistage ADCs*'.

Segmenting the dynamic range not only increase the performance but also results in discontinuities as seen at the end of each segment. Enough amount of settling time should be given to proceeding stages responsible for the linear responses of

the next segments due to these discontinuities. This keeps designers away from going to high speeds. Folding comes into play here and removes discontinuities as shown in Figure 2.26.

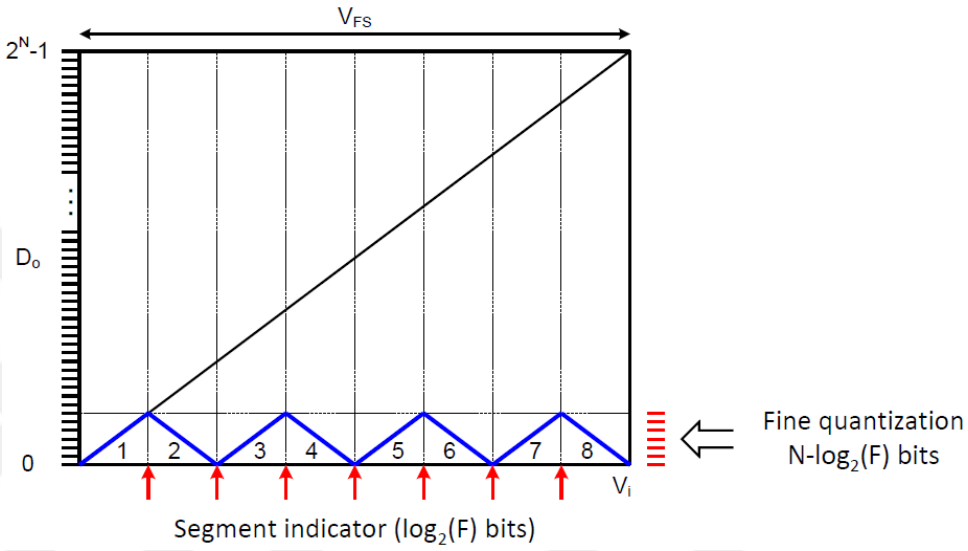


Figure 2.26: Folding dynamic range [1]

A possible block diagram of a folding ADC is shown in Figure 2.27. Coarse ADC determines MSBs or which segment the input signal is in. Then, fine ADC quantizes the folded signal. All of the bits are collected in the digital logic and released together.

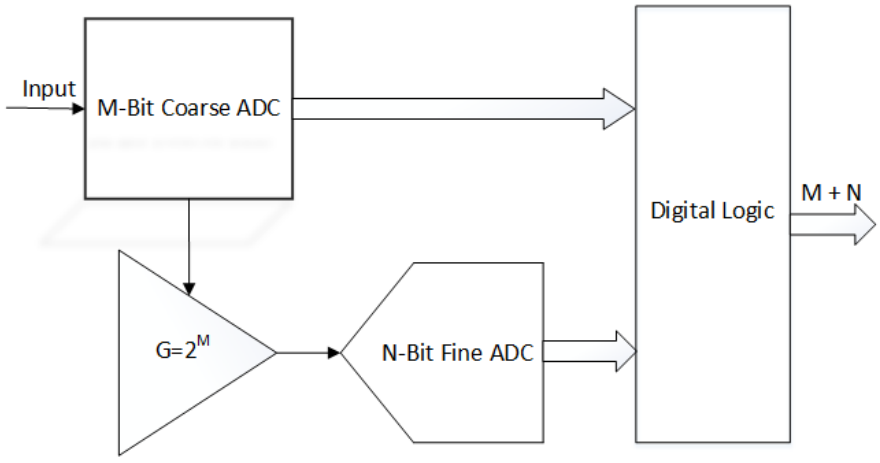


Figure 2.27: Folding block diagram

In a normal (M+N) bit flash ADC, $2^{M+N}-1$ comparators are needed, while only $2^M - 1 + 2^N - 1$ comparators are needed in the folding structure. So, folding method is a solution for the trade-off between resolution (or power) and speed of Flash ADC.

Like the other architectures, Folding ADC has limits, too. Firstly, the sharp transitions between segments are not easily realized with either bipolar or MOS transistors. Therefore, zero-crossings of the transfer curve of differential amplifiers are used to quantize the input levels [7]. Furthermore, while transitioning between segments, the parasitic capacitances of the switching elements need to be charged or discharged and this causes different delays. Besides, finite bandwidth and slew rate of the Folding ADC should also be considered when it is used for high speed and medium-high resolution applications [5].

2.4.3 Interpolation ADC

Another improvement technique for Flash ADC is interpolation. It might be applied to Flash ADCs in case their comparators are using pre-amplifiers and latches.

Pre-amplifiers are used to amplify the difference between input signal and reference voltages. For each reference level, one amplifier is used. It means $2^N - 1$ amplifiers for an N-bit Flash ADC. Figure 2.28 shows three input amplifiers' responses.

As seen from the figure, input is amplified in a limited area and then saturated. Since only the polarity of input amplifiers' output is important for the latches, zero-crossings play an important role in the transfer curves. Satisfying the zero-crossing, the rest of the curve could be *interpolated* through the help of adjacent amplifiers' outputs and a resistive ladder as shown in Figure 2.29. The resultant transfer curves are illustrated in Figure 2.30.

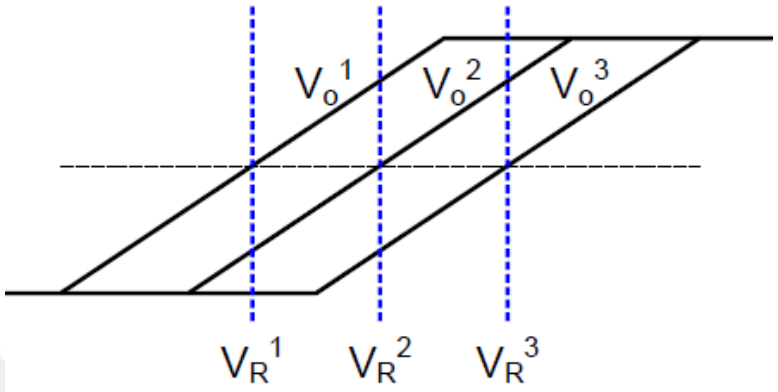


Figure 2.28: Transfer curve of three input amplifiers

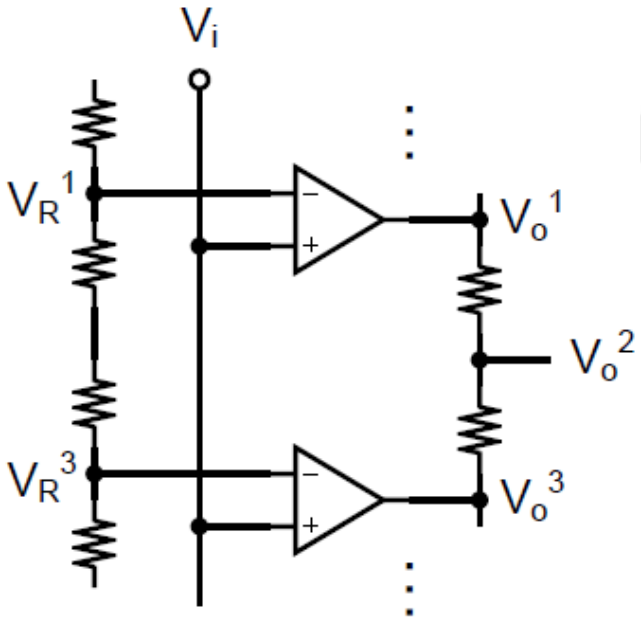


Figure 2.29: Interpolation Circuit

With the help of interpolation, DNL is improved but non-linearity of transfer curves results in errors in the interpolated zero-crossings [1] as shown in Figure 2.31 and this in turn makes DNL and INL worse again. This problem could be fixed using interpolation twice.

Interpolation can also decreases the number of pre-amplifiers and this lessens the burden on sample-and-hold circuits because input capacitance is decreased.

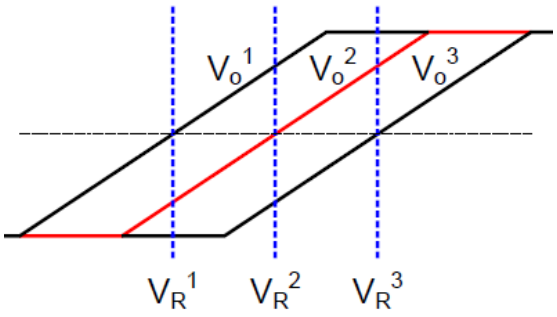


Figure 2.30: Interpolated transfer curves

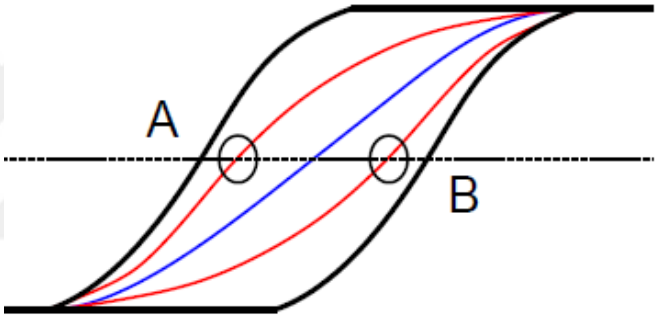


Figure 2.31: The effect of transfer function's non-linearity on zero-crossings

However, the number of latches still stay the same. For a better performance, interpolation and folding techniques should be used together. By this way, both the number of latches and input amplifiers could be decreased and a relatively high speed and medium-high resolution could be obtained.

2.4.4 Pipelined ADC

As its name implies, Pipelined ADC is composed of multiple ADCs lined up in series. Figure 2.32 shows a sample Pipelined ADC block diagram. The idea behind it is to cascade low-resolution ADCs to obtain a high-resolution one [7].

Stages in Pipelined ADC contain a sample-and-hold circuit, a coarse ADC, a DAC and a residue amplifier. Generally the type of ADC inside these stages is flash. The structure of one stage is shown in Figure 2.33.

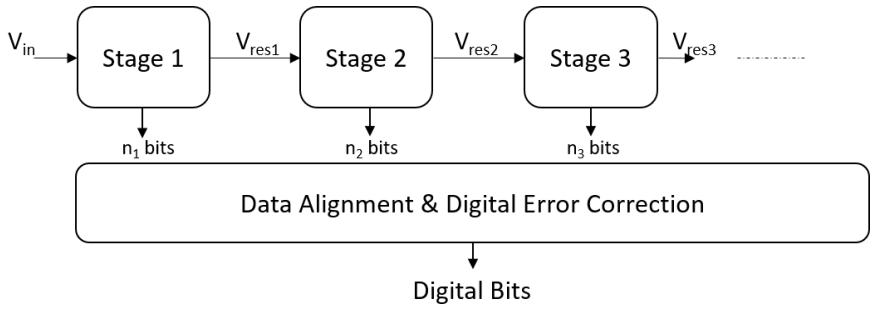


Figure 2.32: Block diagram of Pipelined ADC

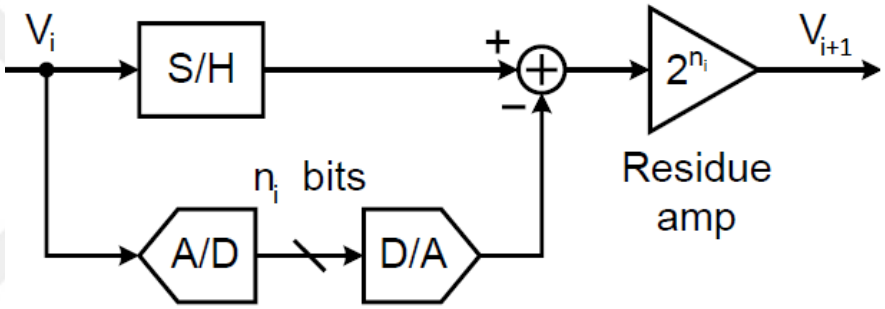


Figure 2.33: Block diagram of a stage of Pipelined ADC

In this type of ADC, input is given to sample-and-hold block and coarse ADC at the same time. That ADC quantizes the input roughly and gives the digital bits to the data alignment block. Then a DAC converts these digital bits back to analog and this analog input is subtracted from the input. Due to quantization error of the coarse ADC, there happens a residue voltage and it is amplified by *residue amplifier* to take it back to full range and is given to the next stage. The same procedure is followed by every stage. The digital bits obtained from stages at different time instants are aligned and corrected in data alignment and digital-error-correction block. Hence, in order to see the last digital bit of one input sample, one needs to wait for a number of clock cycles which depends on the number of stages and the particular ADC architecture [12]. This makes latency an issue for Pipelined ADCs. *Latency* is defined as the time needed to see the last digital bit of an analog input sample. Figure 2.34 shows a commercial ADC's [13] latency. According to the figure, n^{th} sample is seen at the output after 7 clock cycles, so latency is '7 clock cycle' here. On the contrary, *throughput* is not a big

problem for Pipelined ADCs since it depends only on one stage's response.

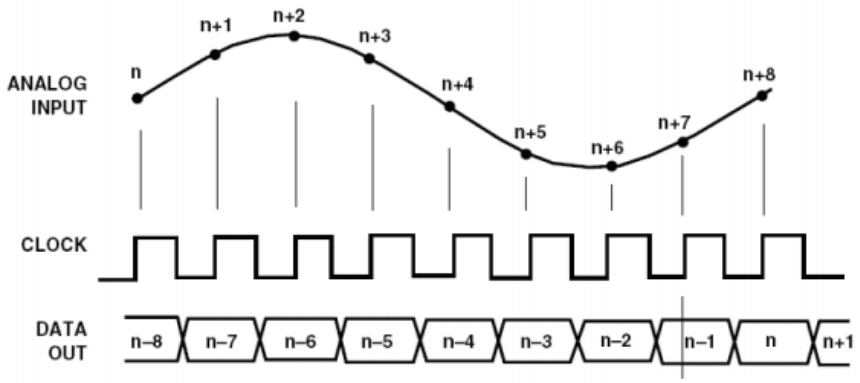


Figure 2.34: Latency graph of a Pipelined ADC

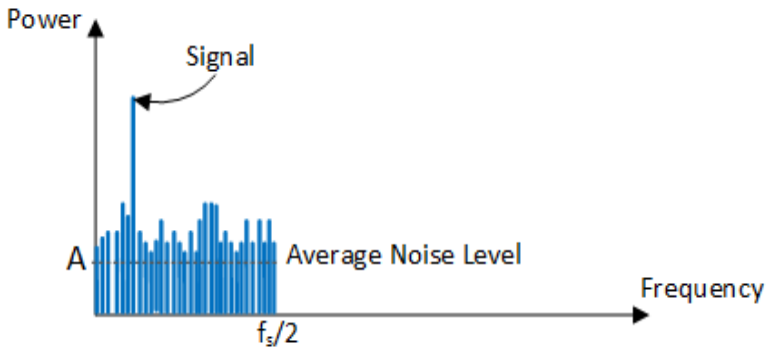
As it has been mentioned before, number of stages has an impact on latency but it also trades with complexity. Having large number of stages decreases bit amount per stage but then latency increases. Therefore, Pipelined ADC's are good choice for medium resolution and medium-high speeds. Moreoever, for the whole Pipelined ADC to be accurate enough, each sub-ADC must be as accurate as total number of bits.

2.4.5 Sigma-Delta ($\Sigma-\Delta$) ADC

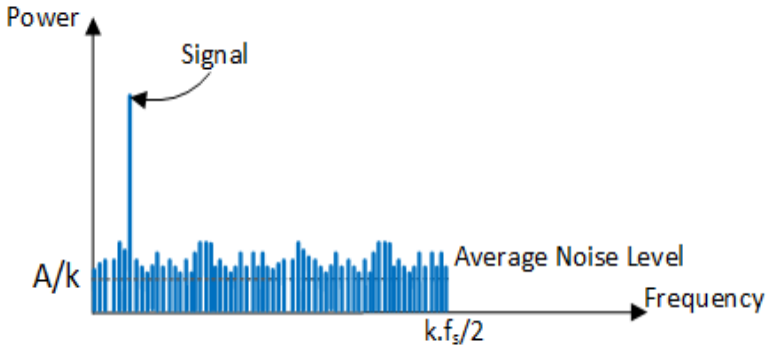
Σ–Δ ADC is a lenghty topic, in order to minimize the overhead, brief information on these converters will be given.

The ADC types mentioned till now were *Nyquist-rate ADCs* whose maximum input frequency is less than half of the sampling rate but Σ–Δ ADC is considered in the class of *'oversampling ADCs'* where maximum input frequency is multiple times less than half of the sampling rate.

The importance of oversampling is explained in sub-section 2.2.2. It removes strict requirements on anti-aliasing filter (AAF). Oversampling also extends noise bandwidth to a wider frequency range. By this way, noise floor drops as shown in Figure 2.35. This effect increases SNR as well. For every 4 times oversampling,



(a) Average noise floor without oversampling



(b) Average noise floor with oversampling

Figure 2.35: Noise floor drops with oversampling

SNR increases by 6 dB and this means 1 extra bit. As an example, in order to get a 16-bit resolution ADC from 1-bit version, it should be oversampled by 4^{15} times but this is not realizable. Therefore, $\Sigma-\Delta$ ADC uses an extra technique to resolve this issue, which is called *noise shaping*.

Consider the block diagrams of a $\Sigma-\Delta$ ADC and a first order $\Sigma-\Delta$ modulator shown in Figures 2.36 and 2.37 [14], respectively. Σ refers to an integrator and Δ refers to a difference amplifier. These two blocks push noise to the high frequencies and keep the signal in the low frequencies with the help of the 'feedback' mechanism, as illustrated in Figure 2.38. One should note that integrator and difference amplifier do not decrease noise power, they only change noise distribution towards high frequencies.

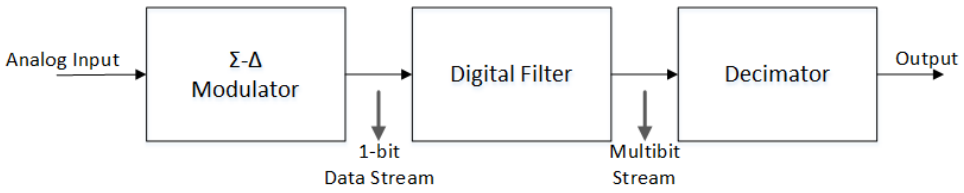


Figure 2.36: Block diagram of Sigma-Delta ADC

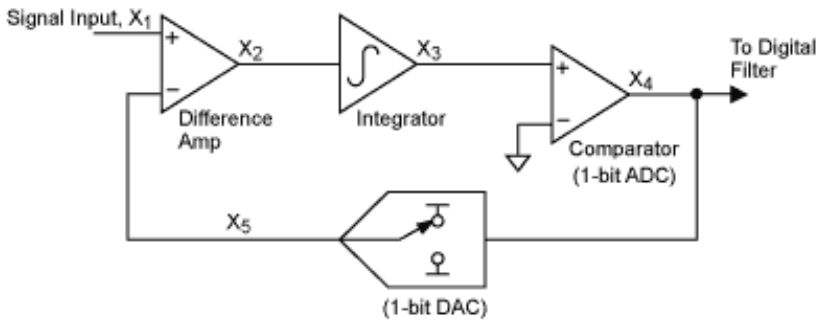


Figure 2.37: Block diagram of first order Sigma-Delta modulator

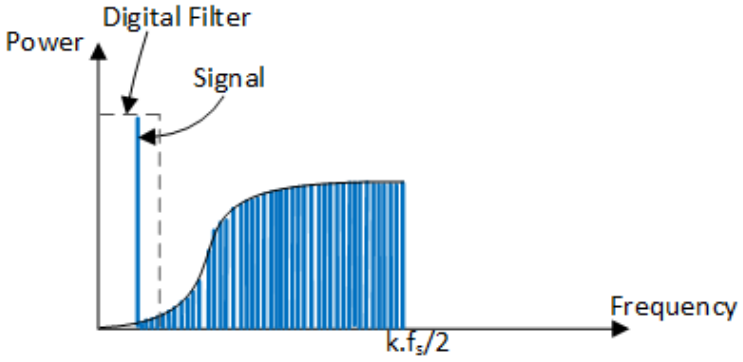


Figure 2.38: Noise shaping with filtering

With this type of modulator (first-order) an SNR increase of 9 dB per octave is obtained. This rate can also be increased using higher order modulators. Figure 2.39 shows the relation between SNR improvement and oversampling factor for different modulator orders [1]. Modulator order could be increased by adding more 'difference amplifier-integrator' sections at the expense of increasing complexity.

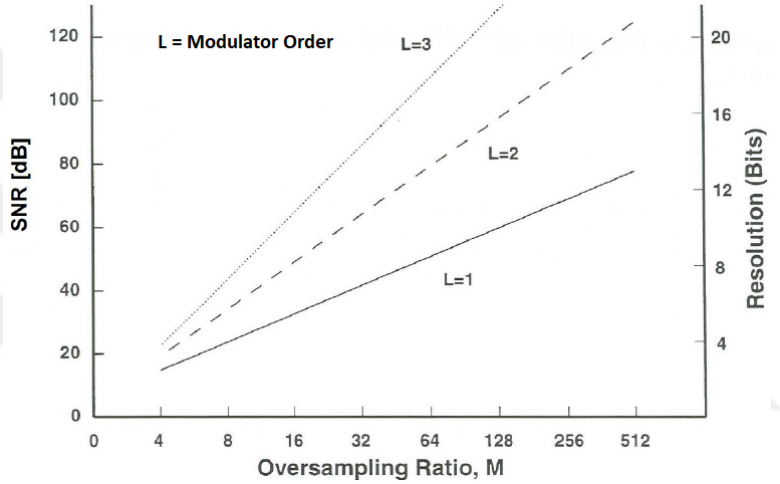


Figure 2.39: SNR oversampling relation for different modulator orders

Chapter 3

Fundamentals of SAR ADC

3.1 Introduction

SAR stands for *'Successive Approximation Register'*. This type of ADC does successive attemps to approximate input signals. During these attempts, it follows a binary search algorithm. Figure 3.1 [5] shows an example of this binary search algorithm for 3-bit ADC.

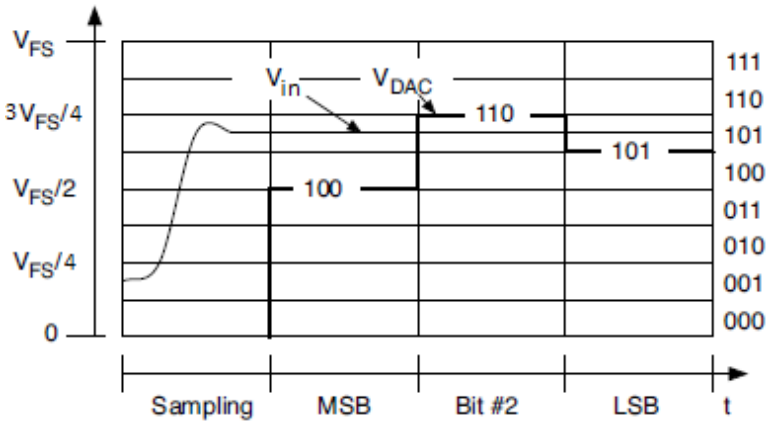


Figure 3.1: Binary search algorithm for 3-bit ADC

Having shown the block diagram of the SAR ADC in Figure 3.2, its conversion mechanism could be explained as follows. First, once analog input is sampled and the sampled value is held, the conversion starts. Held analog signal is compared through a comparator with the DAC output which had been preset to mid-scale by making MSB 1 and the rest of the bits 0 [3]. If the input is greater than the DAC output, then comparator gives an output high. Taking comparator's response, SAR control logic forces MSB to stay high and sets the next bit to 1. If the input is lower than mid-scale, then the comparator gives an output low and control logic makes MSB 0 and the next bit is again made 1. This conversion process repeats until determining LSB and then a new sample is taken and converted to digital following the same procedure mentioned above.

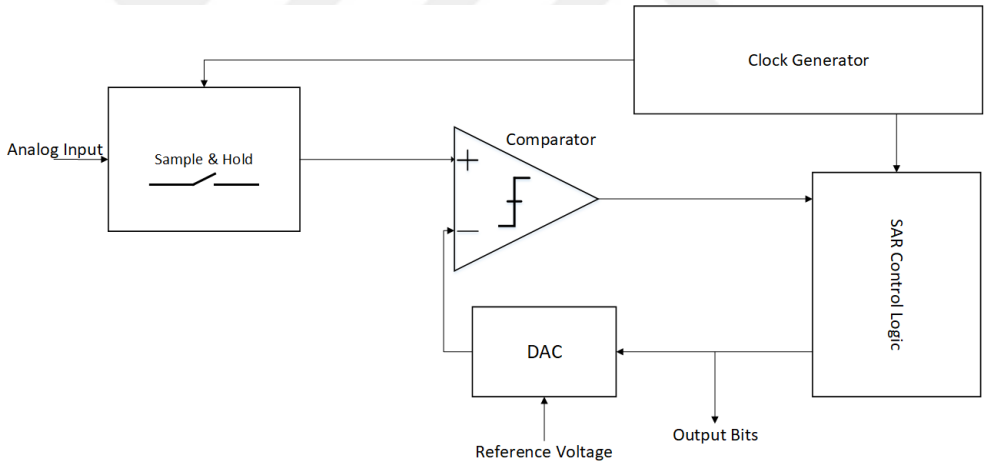


Figure 3.2: Basic block diagram of SAR ADC

Although fundamental principles and working mechanisms are similar for all SAR ADCs, they differ according to their DAC architectures generally. There are many different types of DAC architectures such as Pulse-Width Modulator, Delta-Sigma DAC, Oversampling DAC, Binary Weighted DAC, R-2R ladder DAC, Non-Binary Capacitor DAC, Time-Interleaved DAC, etc. Among these architectures, capacitor based ones are preferred more due to their zero-quescient current. Moreover, their mismatch and tolerance are lower than that of resistor based ones. Furthermore, the most common three types of topologies among these capacitive DACs are conventional binary weighted capacitive-array DAC, binary weighted capacitive DAC with attenuation capacitor and capacitor splitted DAC [15]. In this

chapter, mainly these three common architectures will be explained.

3.2 Conventional Binary Weighted CDAC

One of the most famous DAC architectures used for SAR ADCs is 'conventional binary weighted capacitor array DAC'. In this architecture, charge redistribution method is used [16]. The DAC consists of an array of capacitors which are binary weighted. Charged capacitors are switched to ground or V_{ref}, depending on the bits, in order to change the DAC output voltage. Binary search algorithm is followed in this charge redistribution topology. Figure 3.3 shows a 5-bit example of this architecture.

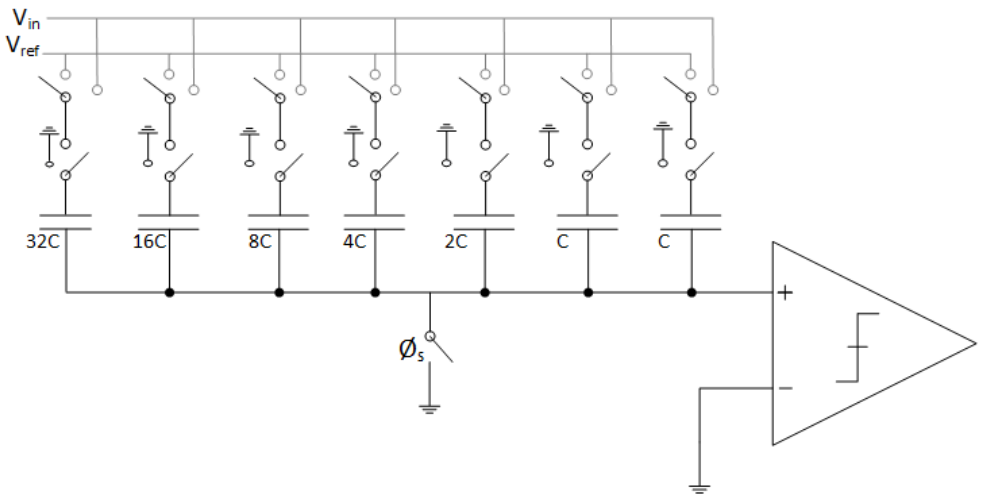


Figure 3.3: 5-Bit version of Conventional Binary Weighted CDAC with comparator

The process consists of multiple steps. In the first step, ϕ_s is closed and top plates of the capacitors are grounded while bottom plates are connected to V_{in}. By this way, a charge of $Q = -64CV_{in}$ is stored on the capacitor array. Then, grounding bottom plates, the switch ϕ_s is opened and top plates are made floated. By charge conservation, top plates' voltage becomes $-Vin$. This process is the 'sampling' and 'holding' of the signal. Although 'Sample&Hold' function is also included in this DAC, it may be realized seperately as well.

In the next step, conversion process starts. First, MSB capacitor's bottom plate is connected to V_{ref}. Due to charge conservation again, a voltage of $V_{ref}/2$ is added to the top plates. This can also be considered as voltage sharing, which is seen in Figure 3.4.

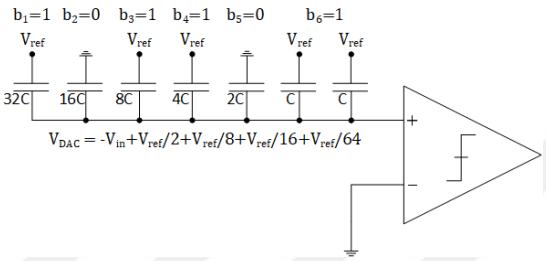


Figure 3.4: Voltage sharing after MSB transition

Once the DAC output voltage settles down, the comparator determines if the inequality shown in 3.1 is true or not.

$$-V_{in} + \frac{V_{ref}}{2} > 0 \tag{3.1}$$

If DAC output is greater than zero, then the next MSB capacitor's bottom plate is kept connected to ground, otherwise it is switched to V_{ref} in the next comparison cycle. When it is connected to the reference voltage, an excessive voltage of $V_{ref}/4$ is added to the bottom plates in order to keep the initial charge constant, making DAC output

$$V_{DAC} = -V_{in} + \frac{V_{ref}}{2} + \frac{V_{ref}}{4} \tag{3.2}$$

Then, the comparator decides again.

Following the same mechanism in each cycle, DAC output converges to sampled and held input voltage. This is how the '*binary search algorithm*' works. Figure 3.5 shows an illustrative example for the resolution of 101101 output.

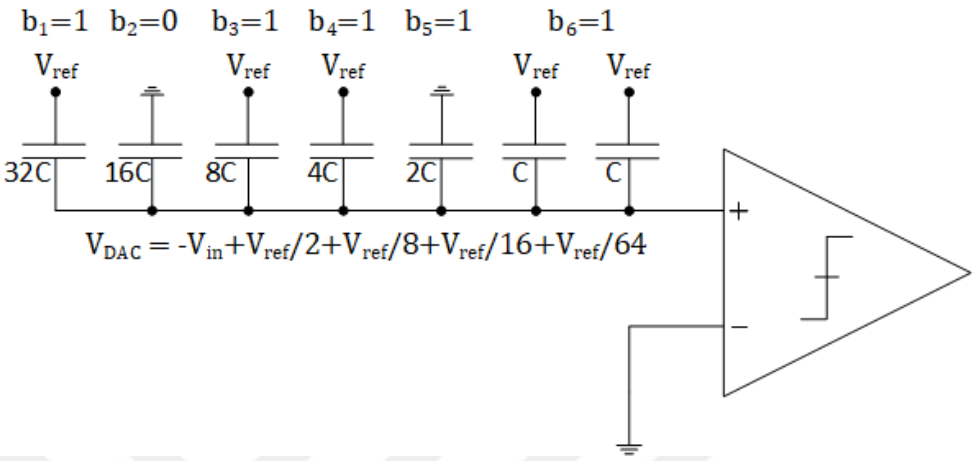


Figure 3.5: Final DAC configuration for 101101 digital bits

3.3 Binary Weighted Capacitive DAC with Attenuation Capacitor

Power consumption of a SAR ADC is mostly because of capacitor switching and it is directly related to the total capacitor value of the capacitor array of the DAC. Furthermore, total capacitance value together with the resistance of reference ladder and switches also affects the speed of the ADC since these two contribute to the RC time constant [15]. Therefore, these two parameters need to be kept as small as possible. However, in the conventional binary weighted DAC structure, capacitor value, hence the RC time constant, increases exponentially as the resolution increases.

Designers have come up with a solution for this problem. The complete array is divided into two sub-arrays and an attenuating capacitor is inserted in between them. Illustrated in Figure 3.6 is a 6-bit example of this topology. The summation of attenuation capacitor and total capacitance of LSB array should give one unit capacitor.

The charge recycling technique of this architecture goes as follows [17]. In the sampling phase, input voltage is stored on the capacitor array. When bottom plates are switched to reference voltage, equivalent output voltage becomes $-V_{in}$

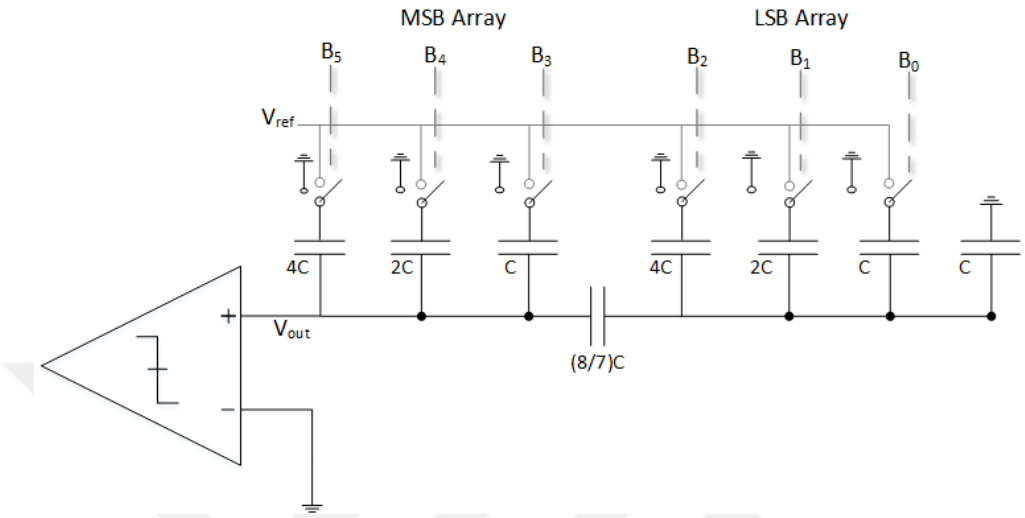


Figure 3.6: Binary weighted capacitor array with an attenuating capacitor

and the conversion starts. If

$$-V_{in} > 0 \tag{3.3}$$

then the bottom plate of biggest capacitor (here, 4C) switches to ground but the other capacitors are kept connected to V_{ref}. This makes the output voltage

$$V_{out} = -V_{in} - \frac{V_{ref}}{2} \tag{3.4}$$

If

$$-V_{in} < 0 \tag{3.5}$$

then all of the bottom plates are kept connected to V_{ref}.

The conversion cycles go on this way. Unlike the conventional binary weighted capacitor array, the stored charge is recycled in this structure instead of redistribution, which decreases the power consumption [18]. Detailed power consumption analysis is given in [15].

3.4 Capacitor Splitted DAC

Yet another type of DAC has been proposed to decrease the power consumption due to switching. It is known as 'Capacitor Splitted DAC', or split binary weighted DAC [19], [20].

In this structure, MSB capacitor is realized through another capacitor array, which may also be called 'MSB sub-array', as shown in Figure 3.7.

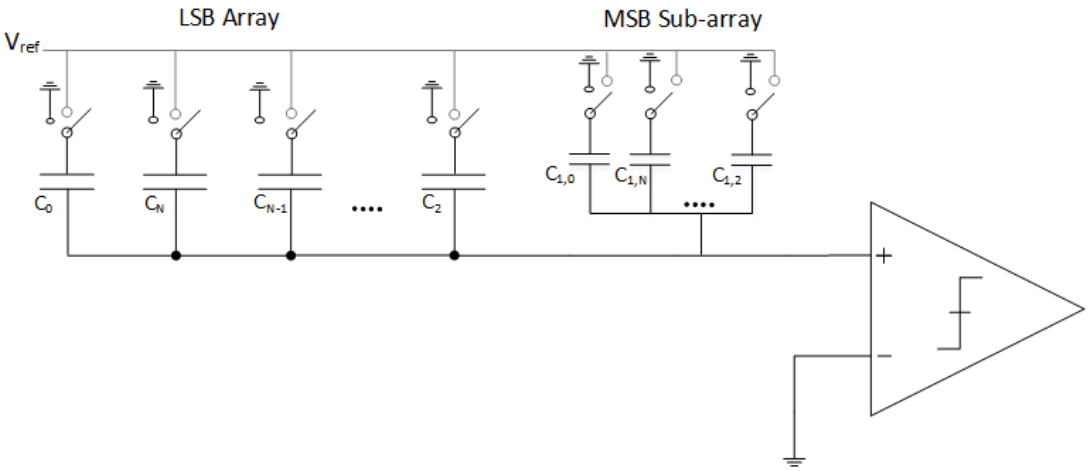


Figure 3.7: Split binary weighted capacitor array

The value of each capacitance in this sub-array can be expressed as

$$C_{1,i} = 2^{N-i} \cdot C_0 \qquad 2 \leq i \leq N \tag{3.6}$$

which is exactly the same with the capacitances of the rest of the array. This shows that the MSB sub-array is one-to-one copy of the rest. The switching algorithm goes in the following way. The capacitors of the MSB sub-array is connected to the V_{ref} and the rest is connected to ground when the conversion phase starts. This makes the DAC output voltage

$$V_{DAC} = -Vin + \frac{V_{ref}}{2} \tag{3.7}$$

Depending on the comparator's output, if it is high (i.e. $V_{in} < \frac{V_{ref}}{2}$) 'down-transition' happens. Otherwise 'up-transition' occurs. In the up-transition process, as in the case of conventional topology, the next MSB capacitor (C_2) is charged up to V_{ref} and the rest stays at zero. On the other hand, in the down-transition process the MSB capacitor of MSB sub-array, namely $C_{1,N}$, is lowered down to 0V and the rest is not changed.

The benefit of this split array compared to conventional one is its energy saving and fast settling. For a rail-to-rail sinusoidal input, split CDAC consumes 37% less energy compared to the conventional DAC. Furthermore, the settling time of the split CDAC is 10% faster than the one of the conventional DAC because less number of capacitors are switching in the down transition case in split array [20].

Chapter 4

Implementation of Proposed SAR ADC

4.1 Introduction

Previous chapters described the basics and building blocks of ADCs, specifically SAR ADCs. In this study, an ADC is designed for a sensor node. Having sensed the temperature and generated analog voltage level for it, this sensor node digitizes analog temperature value and uses these digital bits to modulate a carrier signal. Modulated signal is sent to a receiver wirelessly, using a transmitter. For this sensor application, a 12-bit moderate speed ADC was designed. Since SAR ADCs are the best option for these kind of applications requiring moderate resolution and speed [21], it was also preferred here. The most important specification for this work was its ultra low power consumption. Important measures have been taken throughout the design to satisfy this requirement.

4.2 Top Level Design

The topology for this SAR ADC is very similar to the conventional one, which is shown in Figure 3.2. Illustrated in Figure 4.1 is the chosen structure. Differential version of the conventional structure with improvements is used in order to cancel the common mode noise, leading to an improved SNR performance. All the blocks, either analog or the digital, are supplied with 0.7V. The reference voltage is 0.5V, so the full scale voltage of the ADC is

$$V_{FS} = 0.5 - (-0.5) = 1V \tag{4.1}$$

Figure 4.2 shows final layout of the whole ADC. The total area of the design is 285μm x 385μm as seen from the figure. Layout is verified by DRC and LVS checks using Calibre verification tool and post-layout simulations are completed. These results are provided in section 4.4.

A clock of 1.6 MHz is used in the ADC for the comparator and sampling clock is produced from it using a digital clock generator. In this topology, a differential analog signal, having both positive and negative sides, is sampled with a sample&hold circuit. When sampling is finished, comparison phase is started. Held positive and negative analog signals are compared with each other at each comparison cycle. Depending on the one being greater than the other, comparator pulls the relative output to high and passes this output to the SAR control logic. Furthermore, it releases a valid signal as a flag, implying that the current comparison cycle is over. This valid signal is used to generate control clocks. Control clocks start SAR control logic, and depending on the current comparison result, SAR control logic either switches the MSB capacitor from V_{ref} to ground (if high voltage comes from comparator) or keeps it as it is (if low voltage comes from comparator). In the next cycle (corresponding to $(MSB-1)^{th}$ bit), according to SAR logic's result, either positive signal (for the case of $V_+ > V_-$) or negative signal is decreased by half the reference voltage. The first step of this switching algorithm -MSB switch- can be seen in Figure 4.3. This comparison cycle is repeated 12 times. This way, positive and negative signals approach each other at

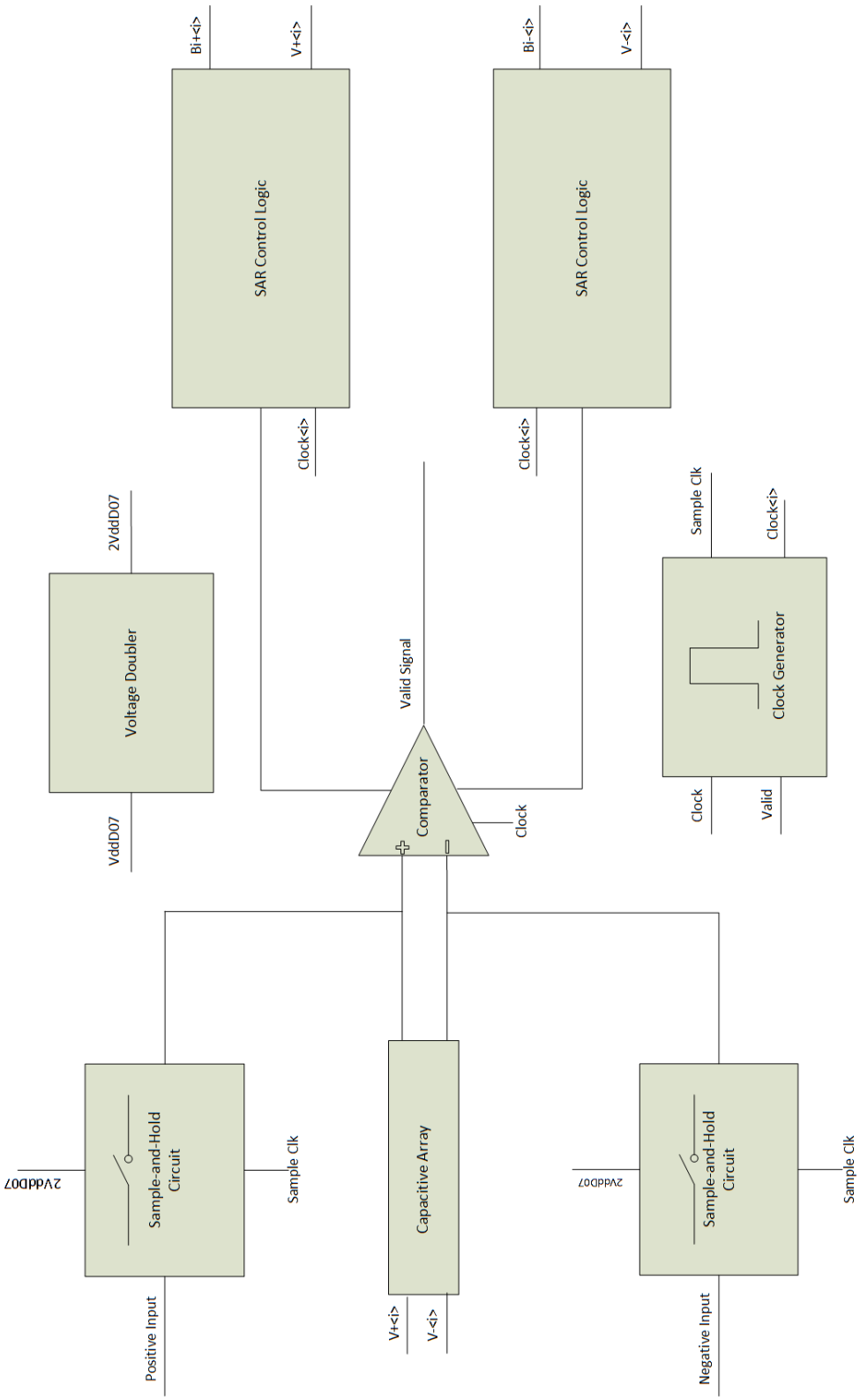


Figure 4.1: Preferred SAR ADC block diagram

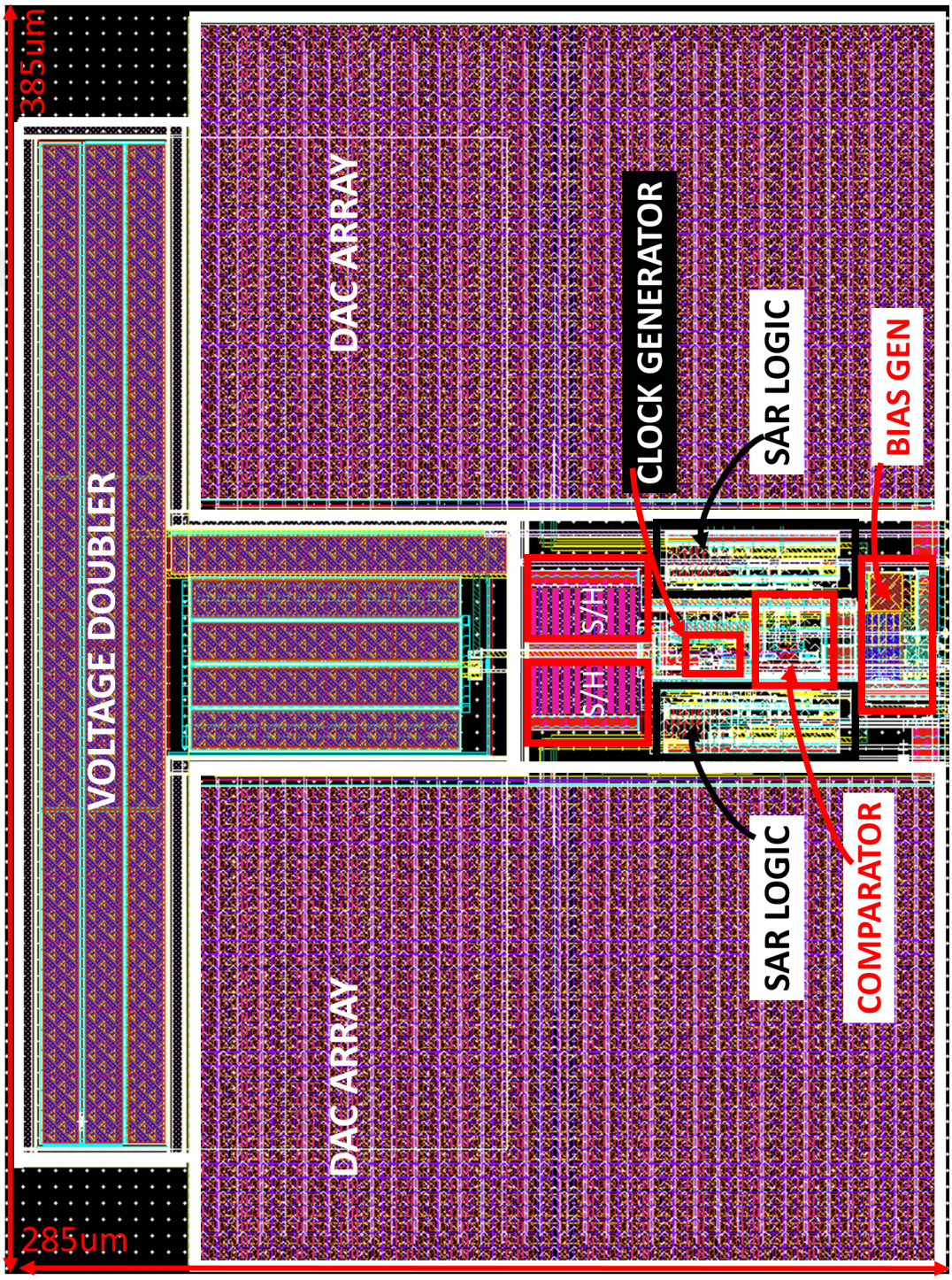


Figure 4.2: ADC Layout

the end of the comparison phase as the name SAR implies. Figure 4.4 illustrates the characteristic of the DAC output voltage.

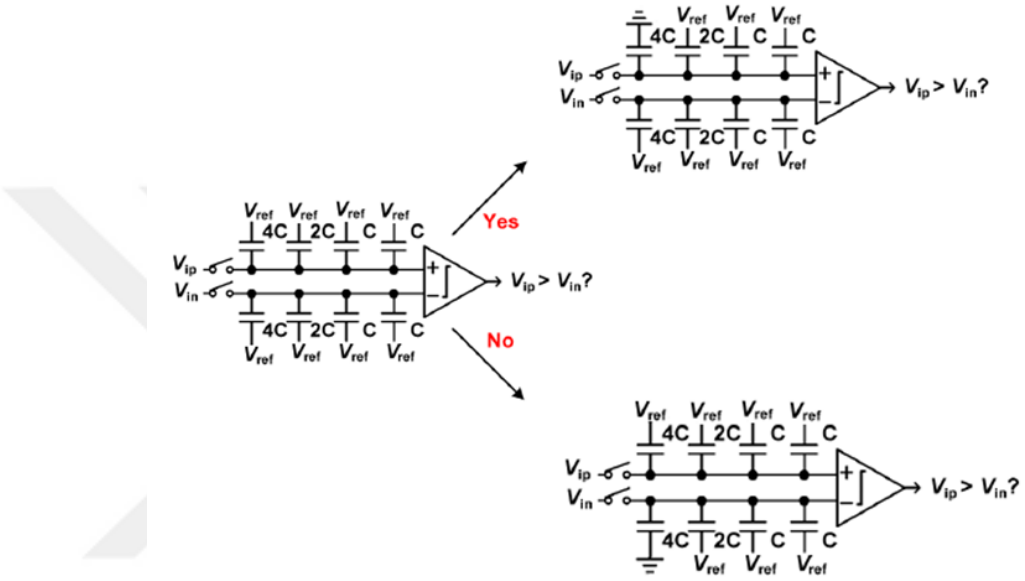


Figure 4.3: Small example of proposed capacitive array switching

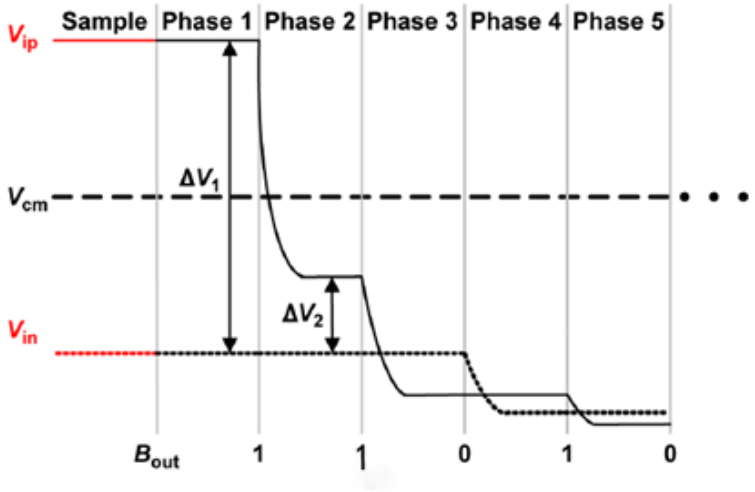


Figure 4.4: Proposed DAC Switching

As also seen from this figure, either positive or negative voltage is decreased at every cycle. This makes the proposed switching procedure 'monotonic'. In

a 'non-monotonic' switching algorithm, shown in Figure 4.5, up-transitions are observed as well. These up-transitions slow down the DAC settling because the on-resistance of a PMOS switch is 3 times greater than the one of NMOS switch [22]. The conventional switching also increases the power consumption.

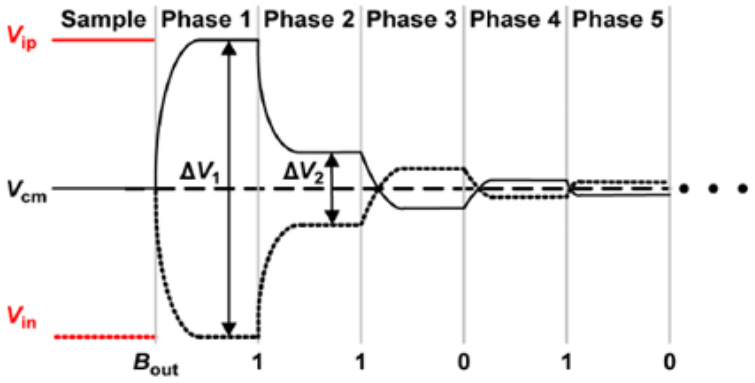


Figure 4.5: Conventional Non-Monotonic DAC Switching

4.3 Building Blocks

This ADC contains two sample&hold circuits, one voltage doubler, one dynamic comparator, two SAR control logics, one clock generator and two DAC arrays. Detailed explanation of each block is given in the coming sections.

4.3.1 Sample and Hold Circuit

Instead of using a simple MOS switch, a *bootstrapped* switch [23] is preferred. The schematic of this S/H circuit and its layout are shown in Figures 4.6 and 4.7, respectively. The advantage of this circuit comes from the fact that it keeps gate to source voltage (V_{GS}) of output switch (NM4, in this case) equal to the supply voltage (V_{DD}) in the sampling phase. This provides a constant, small on-resistance which improves the performance of signal tracking and hence the linearity.

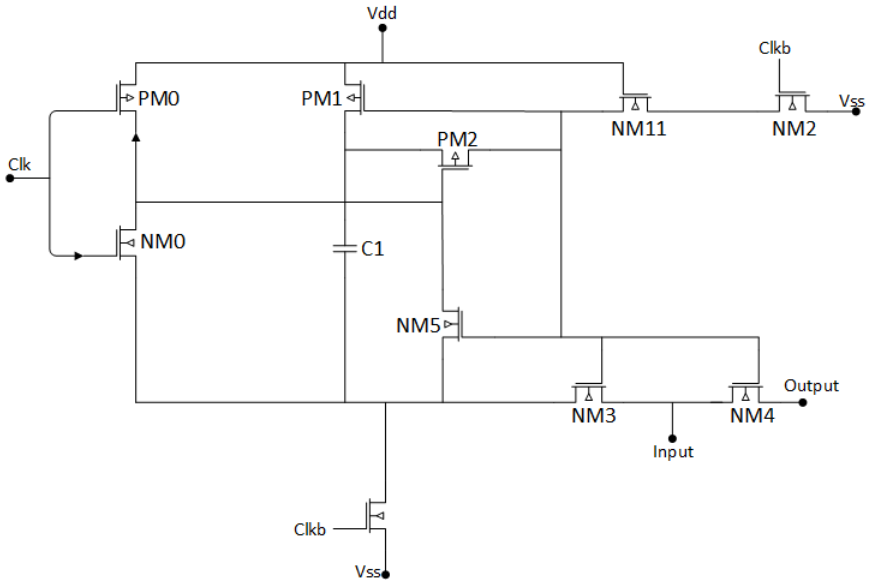


Figure 4.6: Bootstrapped Switch

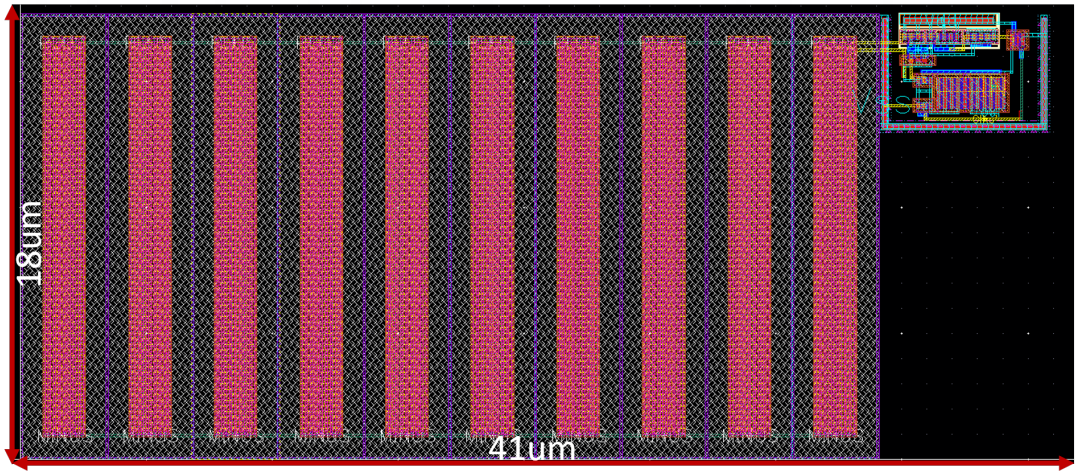


Figure 4.7: S/H Layout

The working principle of the S/H circuit is as follows. The capacitor, C1, is charged to supply voltage in the hold phase and is connected between the gate and the source terminals of the output switch in the sampling phase. Illustrated in Figure 4.8 is a summary of the operation.

Although the gate signal of the output switch is expected to be above the input signal by V_{DD}, as seen from Figure 4.9, simulations showed that the V_{GS} of output

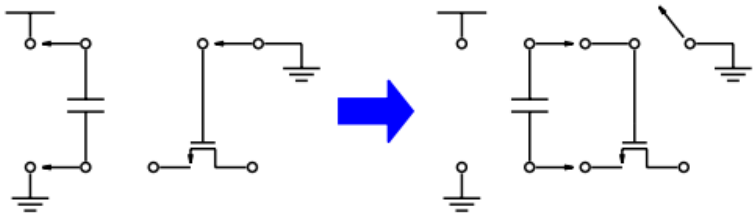


Figure 4.8: Operation of Bootstrapped Switch [2]

switch couldn't stay at supply voltage but instead lower than that because of parasitics and losses. Illustrated in Figure 4.10 is the simulated V_{GS} of the output switch.

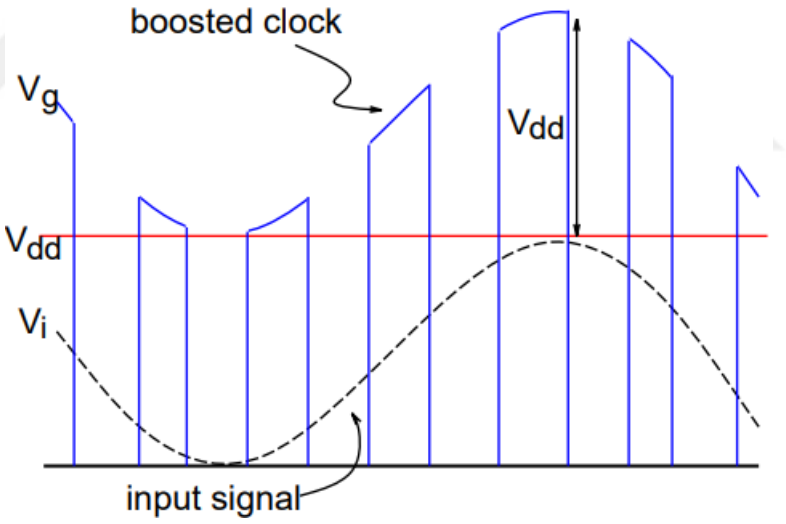


Figure 4.9: Output of Bootstrapped Switch [2]

Considering this fact, a voltage doubler is used as the supplier of S/H circuit in order to increase the V_{GS} of output switch at the sampling phase.

The schematic and extracted spectre simulations of S/H circuit can be seen in Figures 4.11 and 4.12, respectively.

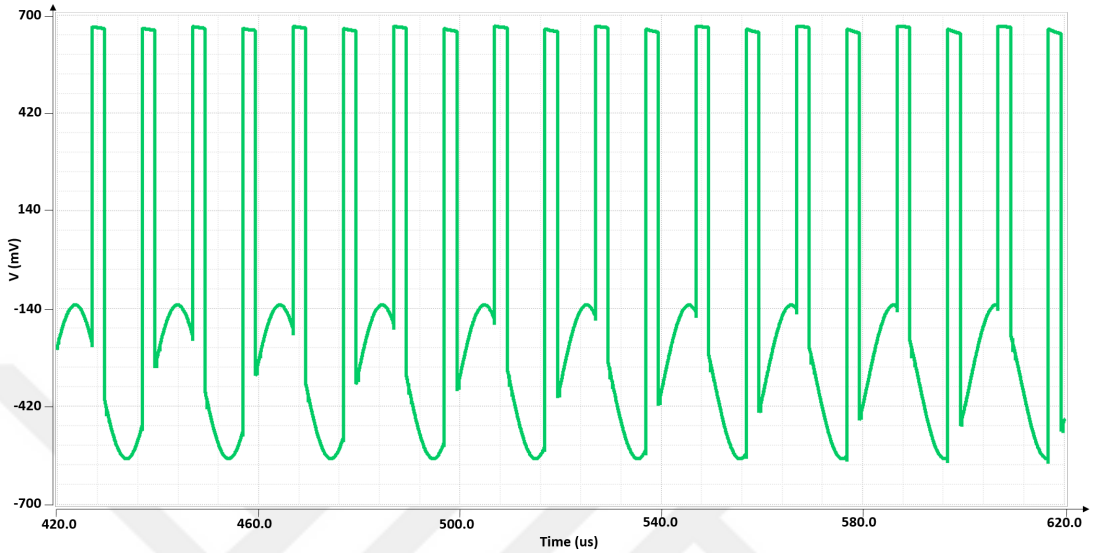


Figure 4.10: V_{GS} of output switch

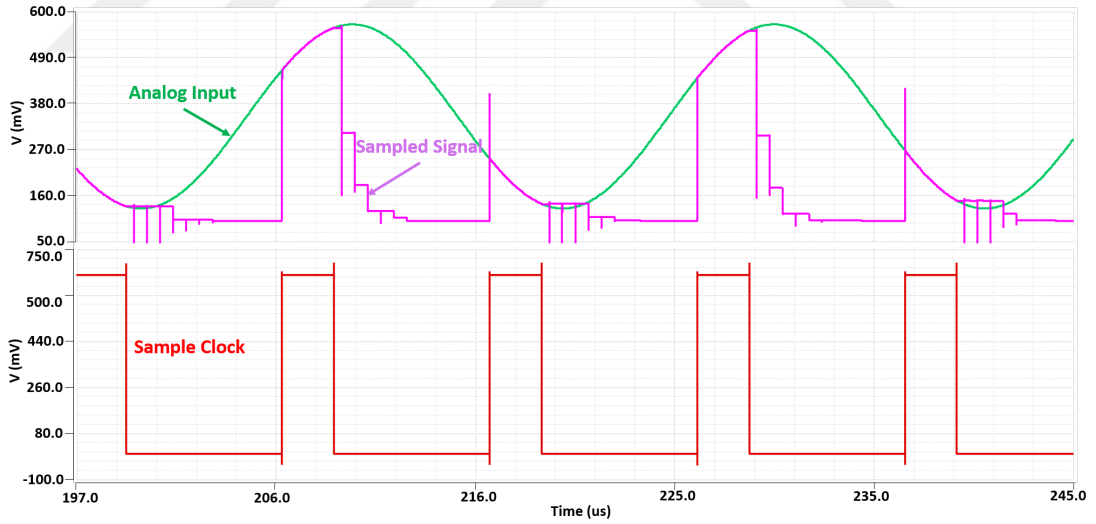


Figure 4.11: Spectre simulation of Sample&Hold circuit

4.3.2 Voltage Doubler

As mentioned in the previous section, voltage doubler is used to increase the V_{GS} of output switch at the sampling phase. This is accomplished by supplying S/H

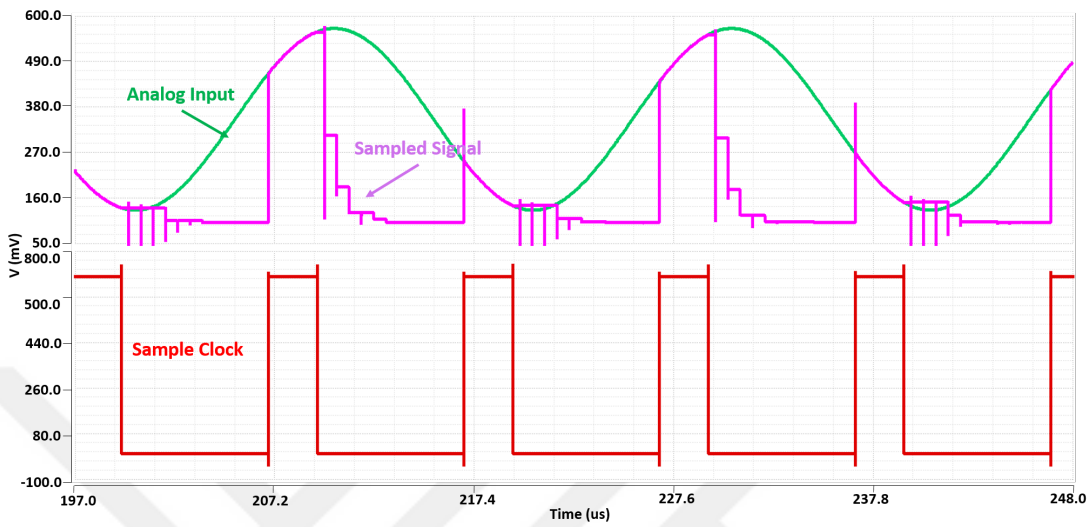


Figure 4.12: Extracted simulation of Sample&Hold circuit

with the voltage doubler output. This way, the on-resistance (r_{on}) of sampling switch is decreased and signal is tracked much better. Figure 4.13 shows the block diagram of the voltage doubler.

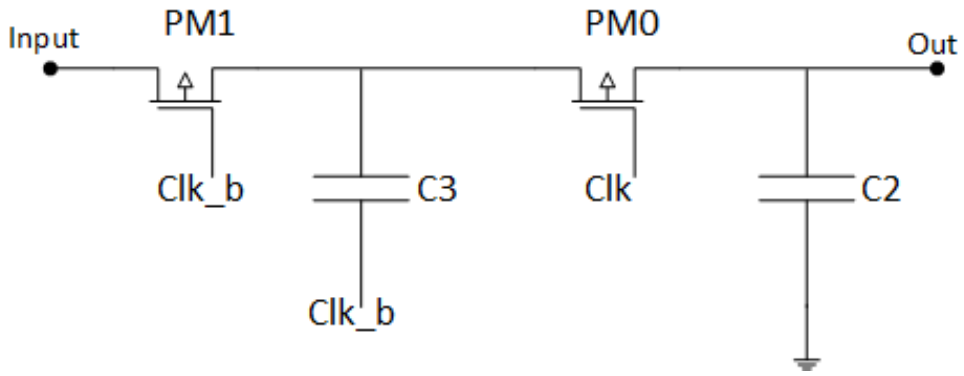


Figure 4.13: Block diagram of voltage doubler

The voltage doubler generates an average output voltage of 1.05 V because of the losses in the circuit and this causes a V_{GS} of around 0.970V at the output of the MOS switch. The difference causes an energy loss of;

$$
\begin{aligned}
Q &= C \cdot V \\
&= 400(\text{fF}) \times 80(\text{mV}) \\
&= 32 \text{ fJ}
\end{aligned} \tag{4.2}
$$

Figure 4.14 and 4.15 shows the voltage doubler output and gate-to-source voltage of the output switch, respectively.

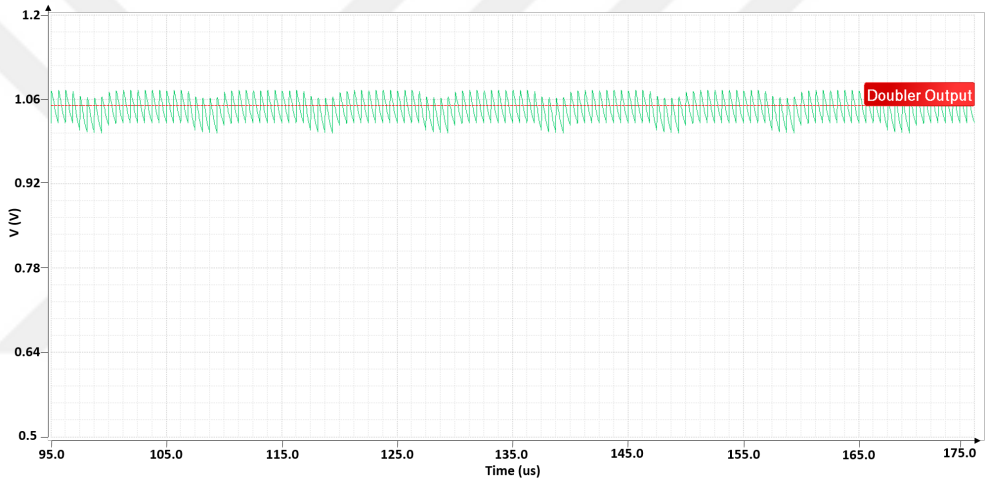


Figure 4.14: Voltage doubler output simulaton

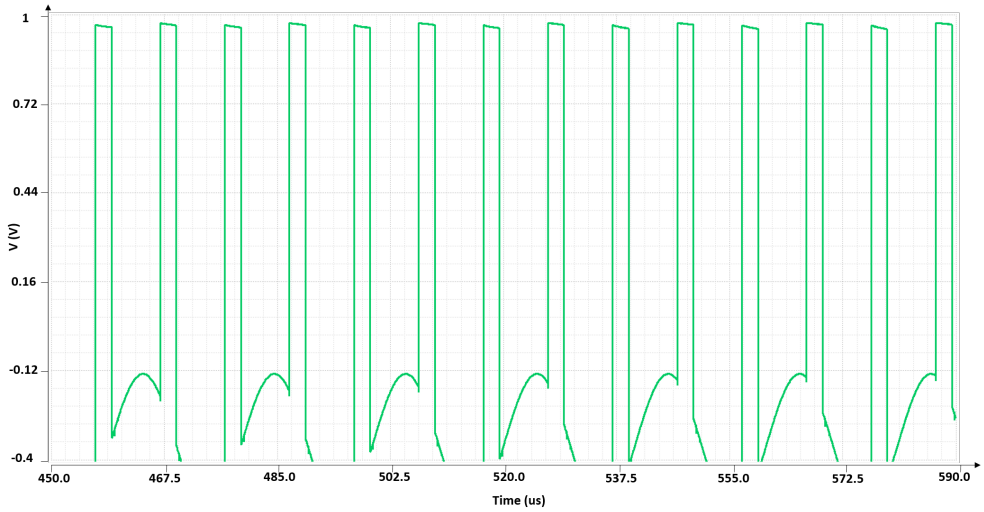


Figure 4.15: V_{GS} of output switch when S/H supplied with voltage doubler

The addition of the voltage doubler increases the power consumption, hence the conversion efficiency though. Furthermore, due to the switching nature of the

doubler, it may have degrading effect on the performance of the ADC in measurements, hence we've included the necessary circuitry to change the clocking frequency or bypass it altogether if needed. This way, a through assessment of the effectiveness of the doubler will be made.

The layout of voltage doubler is shown in Figure 4.16. Since it is supplied with digital V_{DD} and ground voltages, it is isolated from analog ground, which is common all over the substrate using the '*deep n-well (DNW)*' layer as can be observed in the top level layout given in Figure 4.2.

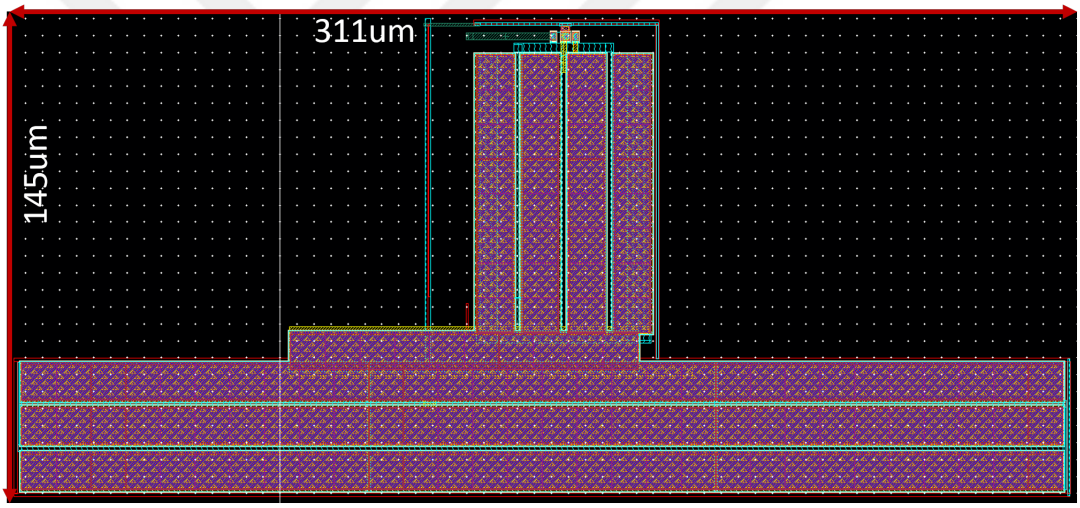


Figure 4.16: Voltage doubler layout

4.3.3 Dynamic Comparator

Comparator is one of the most critical blocks in ADC design. The linearity of an ADC is highly dependent on its performance. A dynamic version has been selected for our design, whose schematic is shown in Figure 4.17. The current source inside the comparator is controlled by the clock signal (Clk), which makes static power consumption zero. This is a very big advantage in an ultra low power design. Moreover, the input pair is implemented with PMOS in order for the comparator not to be affected from monotonically decreasing common mode voltage. The working principle of this comparator is as follows. When

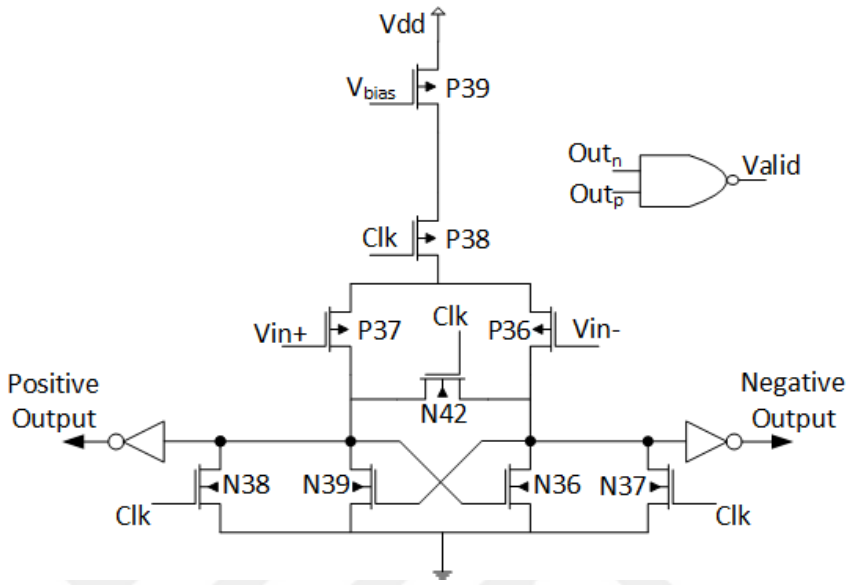


Figure 4.17: Dynamic Comparator Schematic

the 'Clk' is high, the output of N39 and N36 is grounded and both positive and negative outputs are pulled high and this is the reset mode. When 'Clk' goes low, latch starts working. Current flows through the differential pair (P37 and P38) forcing them to compare the two inputs. The latch pulls higher voltage up to the supply and lower voltage down to the ground. When the comparison is done, the comparator gives a valid signal to the 'clock generator' in order for it to generate the control clocks.

The most diffucult scenario for the comparator is switching from the highest possible input differential voltage to the lowest one in two consecutive comparison steps. To prevent comparator from making wrong decisions in such cases, the two outputs should certainly be reset in the reset mode. Although N39 and N36 does this job, another switch, N42, is asserted in between the differential outputs in order to guarantee the reset.

Equation 4.3 expresses the offset voltage of this comparator [22].

$$V_{OS} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2} \quad \left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R} \right) \tag{4.3}$$

Although the rest of the parameters are static, overdrive voltage $(V_{GS} - V_{TH})$ of the input pair is signal dependent. This may be the biggest factor degrading the

linearity of the comparator, hence should be kept as constant as possible.

An intelligent solution to this problem is stated in [22]. Cascoding an externally biased PMOS with P38, an almost constant drain current flowing through input differential pair is obtained. This makes their overdrive voltage less affected from a changing common mode voltage of the input pair.

Figure 4.18 shows the spectre simulation of the comparator. As observed from the figure, whenever the comparator finishes a comparison a valid pulse is generated.

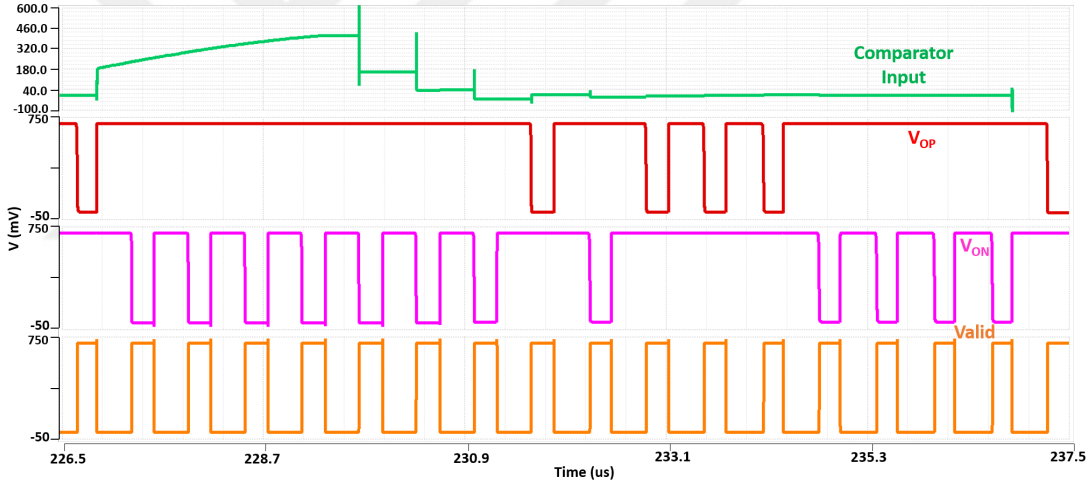


Figure 4.18: Dynamic Comparator spectre simulation

As it is one of the most sensitive elements of this ADC, the layout of the comparator is done as symmetric as possible in order to get much better linearity performance and limit the offset. Dummy transistors are placed around the actual ones. Moreover, the signal paths are encircled with substrate connections, as seen in Figure 4.19, to prevent undesired couplings. Increasing substrate connections decreases parasitics and resistivity. This approach is also utilized in some of the other sensitive sub-blocks' layout.

Having obtained clean DRC and LVS results, post-layout simulations of the comparator were also run, and the results are shown in Figure 4.20.

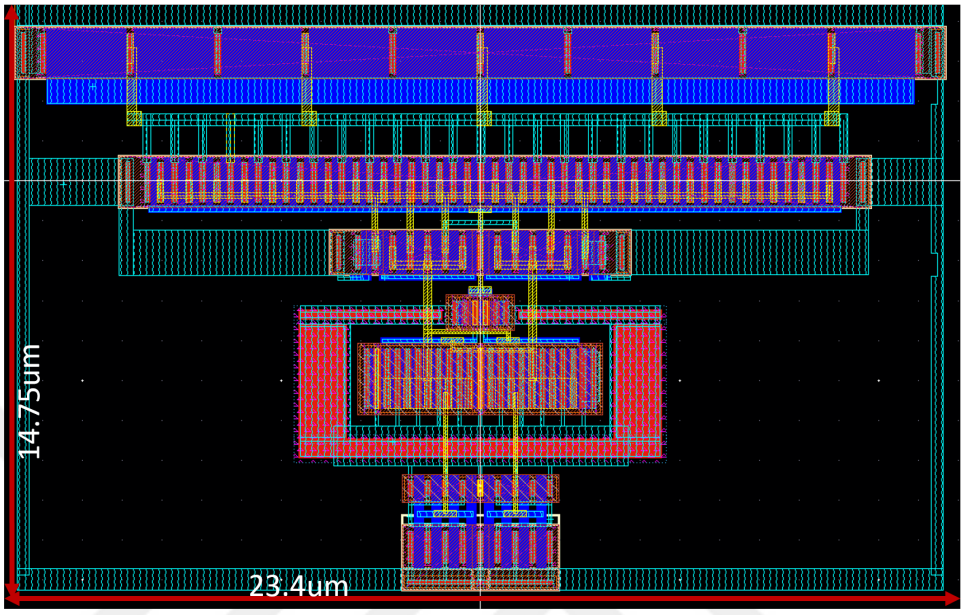


Figure 4.19: Dynamic Comparator layout

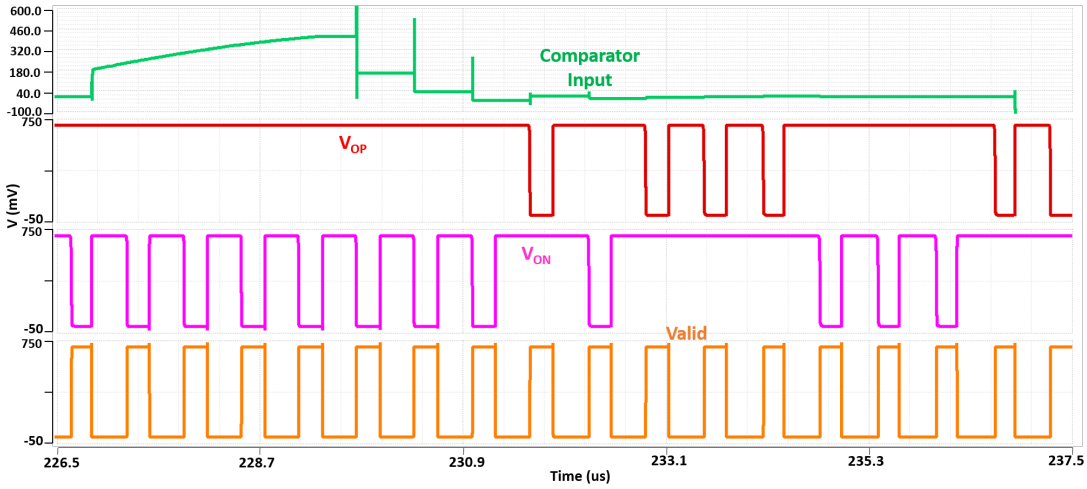


Figure 4.20: Extracted Dynamic Comparator simulation

4.3.4 SAR Logic

SAR conrol logic is a digital block which is responsible for bit generation and DAC switching. Shown in Figure 4.21 is the block diagram for the control logic. Although only one block is shown for each element in the figure, there are 12 of them in parallel since the resolution of the ADC is 12-bits. SAR logic works in

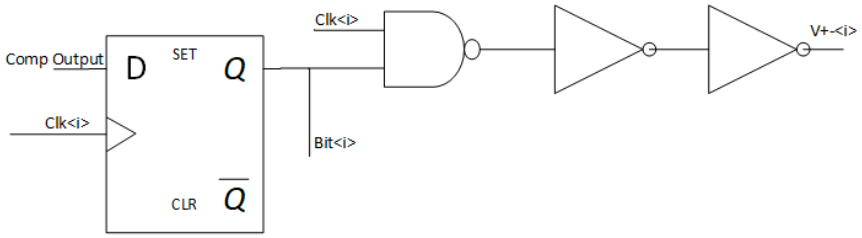


Figure 4.21: SAR Control Logic block diagram

the following way. Register i, realized with a D flip-flop and triggered with the control clock, takes comparator output and stores it. At the positive edge of the clock i, it releases the i^{th} bit. At the same time, this bit is given to a NAND gate with control clock as a second input. Assuming the current bit is high NAND gate gives a low output. Taking the low output, the buffer pulls reference voltage at the bottom plate of the corresponding capacitor to ground. This decreases the sampled signal by $\frac{V_{ref}}{2^i}$, which will be explained in section 4.3.5 in detail. The spectre simulation of the input-output voltage relationship of SAR control logic is shown in Figure 4.22. It is also seen in this figure that as the comparator gives high output, the relative DAC input voltage switches down to zero. Whenever a low output comes, SAR control logic keeps the DAC input voltage equal to the reference voltage, which is 500 mV. Figure 4.23 shows the layout of the SAR logic. Once the circuit was laid out, DRC and LVS checks were done using Calibre and post layout simulations were run. Figure 4.24 shows the extracted simulation of the input voltage and the output bits of the SAR control logic.

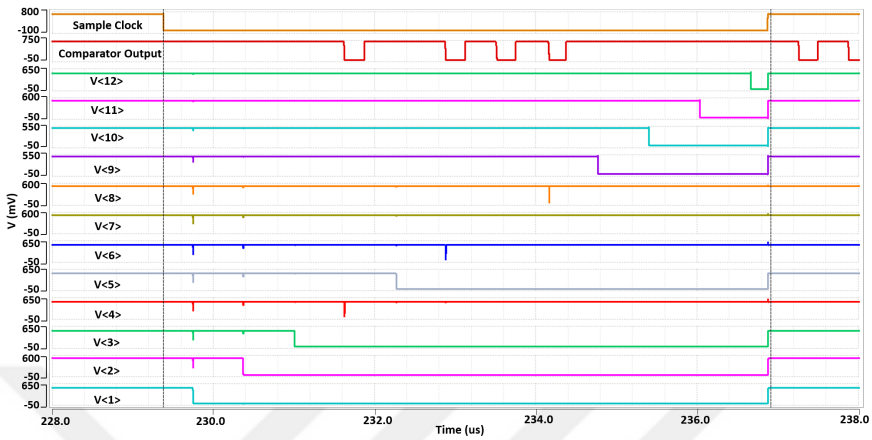


Figure 4.22: SAR Control Logic spectre simulation

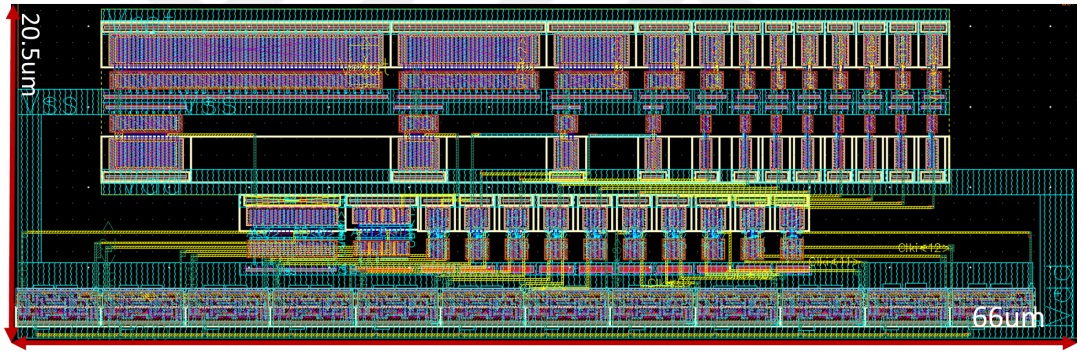


Figure 4.23: SAR Control Logic layout

4.3.5 DAC

Conventional binary weighted capacitor array structure is preferred in the DAC design and Figure 4.25 shows the schematic. Since the resolution of our ADC is 12-bits, the DAC consists of 12 capacitor whose bottom plates are connected to the reference voltage. Apart from the right-most capacitor, which is used to sustain binary weight balance ($C + C = 2C$), the capacitance value of each capacitor (in terms of unit capacitor) can be calculated as

$$C_i = 2^{i-1}C \tag{4.4}$$

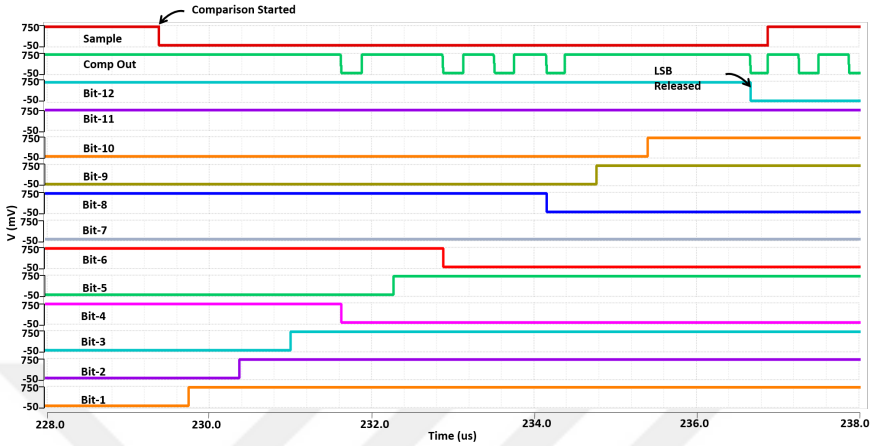


Figure 4.24: SAR Control Logic extracted simulation

Each side of the differential DAC (positive and negative) contains 2^{11} unit capacitors (C_u) where each unit capacitoris 5 fF. This corresponds to a total input capacitance of 10 pF given that the ADC is differential. As the unit capacitor value increases, the charge capacity increases and therefore the performance of the ADC improves but the power consumption increases as well. The capacitors are implemented with MOM caps since they are modeled even at as small values as what we use in this project.

As explained in section 3.2, the DAC stores the input charge on top of the capacitor array when S/H samples the signal. As the comparison proceeds, bottom plate voltages are switched from V_{ref} to ground depending on the bits. This monotonically decreases relative held signal (either positive or negative) by $\frac{V_{ref}}{2^i}$ at every i^{th} comparison cycle. Since only one side of the capacitor array switches at a time, either up or down, monotonic switching is advantageous from the perspective of power consumption, too.

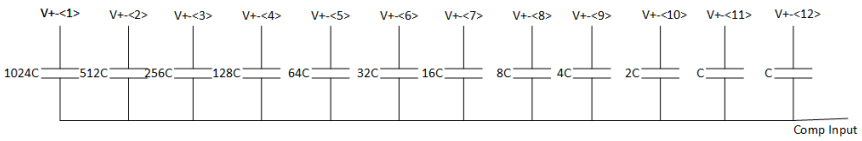


Figure 4.25: Conventional Binary Weighted Capacitive DAC Array

Illustrated in Figure 4.26 and 4.27 are the spectre simulations of the positive input voltage to the DAC and the corresponding output voltage, respectively.

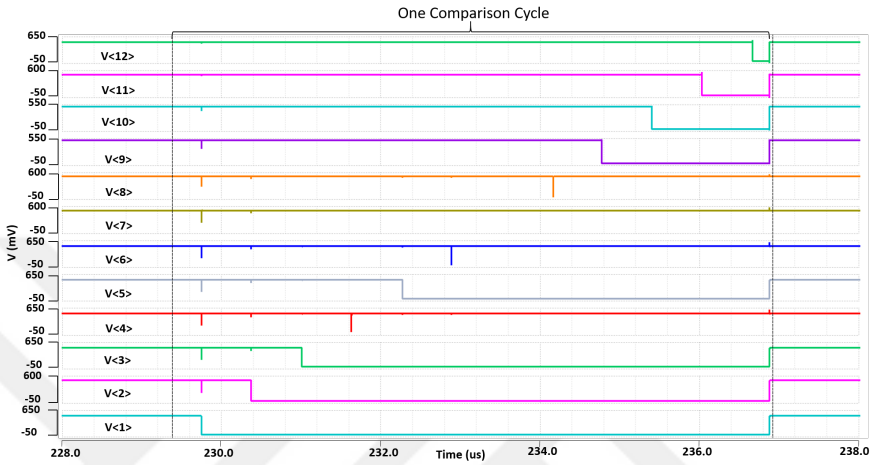


Figure 4.26: CDAC input voltages spectre simulation

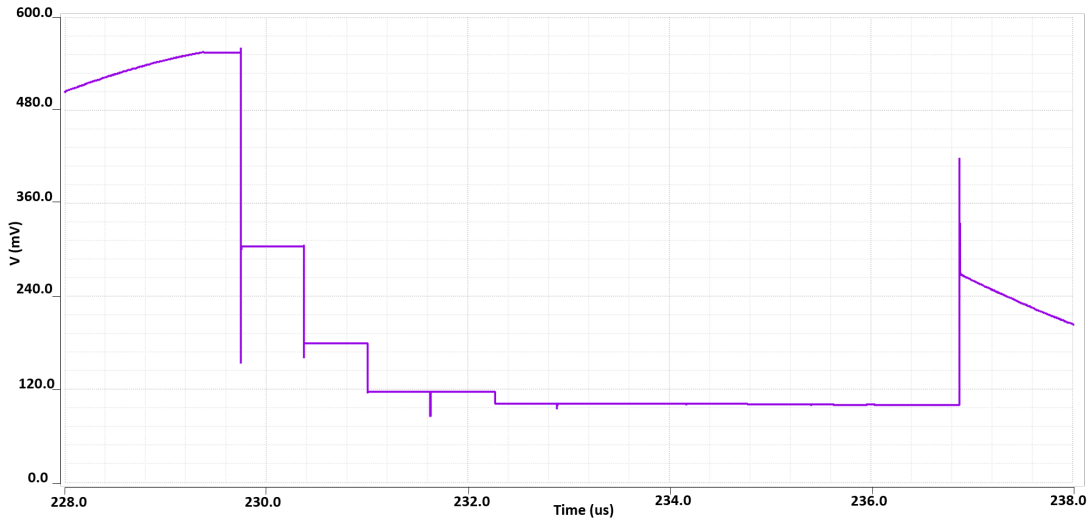


Figure 4.27: CDAC output voltage spectre simulation

As also seen in the figure, DAC output voltage decreases by 250 mV ($\frac{V_{ref}}{2}$) when the first bit (MSB) is released high. Once the second bit is again released high, output decreases by 125 mV ($\frac{V_{ref}}{4}$) this time and every subsequent bit, the output decreases by $\frac{V_{ref}}{8}$, $\frac{V_{ref}}{16}$ and so on, respectively. This way, the two voltages approach each other successively.

Since conventional topology is used, the layout of the DAC, shown in Figure 4.28, occupies almost all of the area of the ADC. Again, a special care is given to the symmetry between positive and negative DACs since it affects the linearity which is very important for ADC resolution. To that end, common centroid method is followed in layout floorplanning and dummy unit capacitors are placed around the actual capacitors.

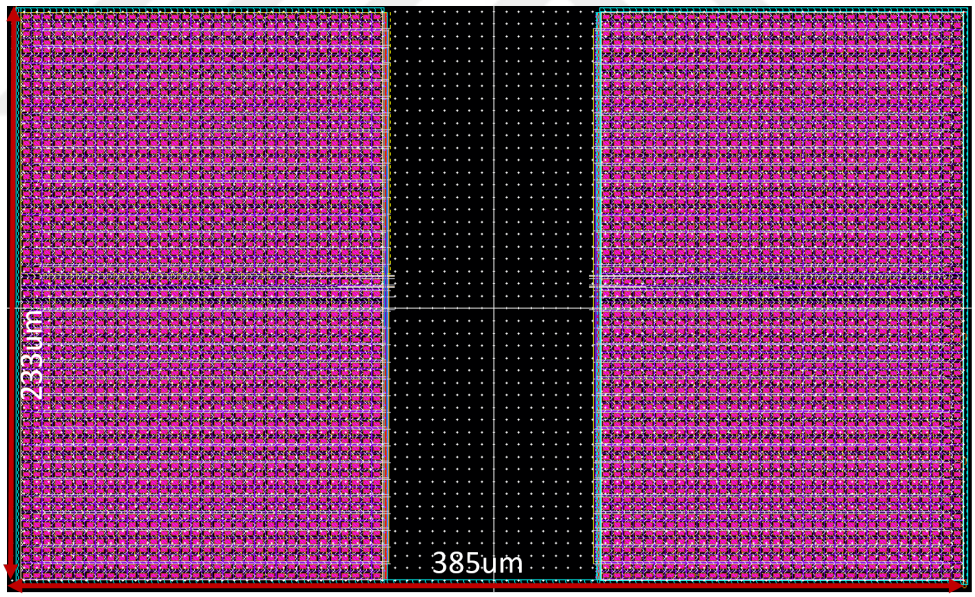


Figure 4.28: CDAC layout

Post layout simulations were run and are shown in Figures 4.29 and 4.30.

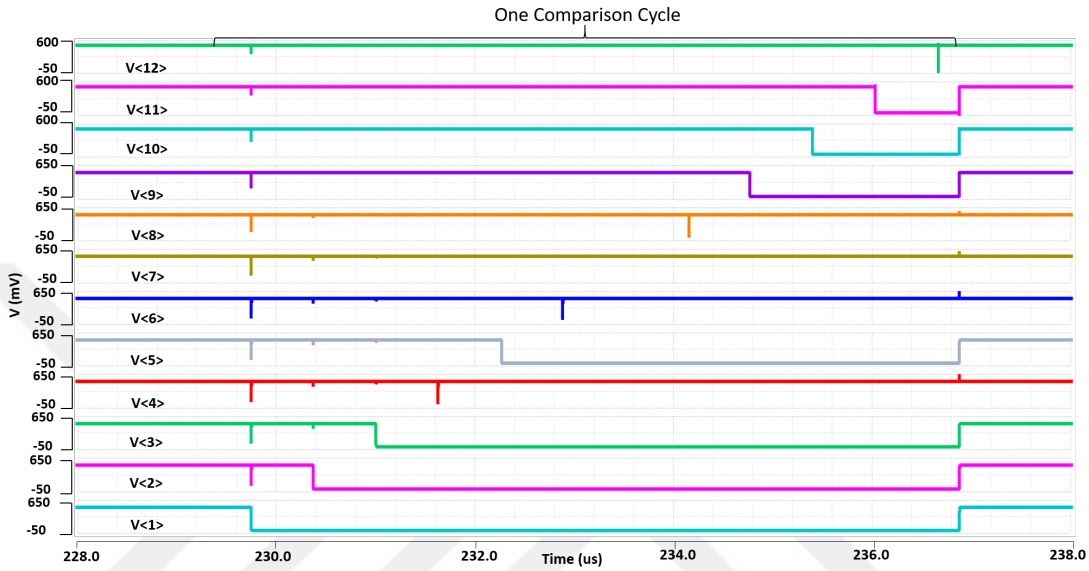


Figure 4.29: CDAC input voltages extracted simulation

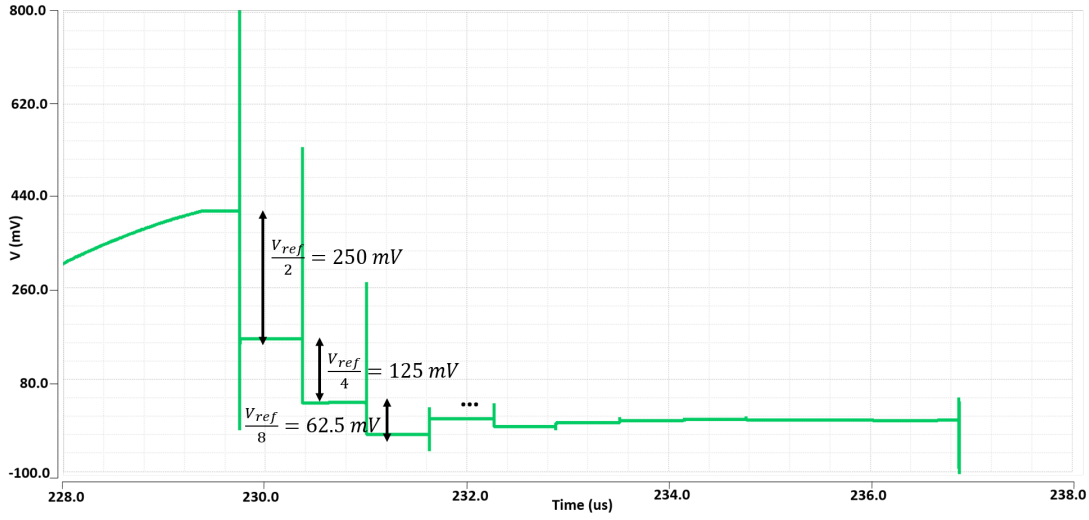


Figure 4.30: CDAC output voltage extracted simulation

4.3.6 Clock Generator

Clock generator is the block where ADC clocks used in the design are generated internally from an external low-noise clock source. Figure 4.31 shows the block diagram of the clock generator. As observed from the figure, 'valid' signal is

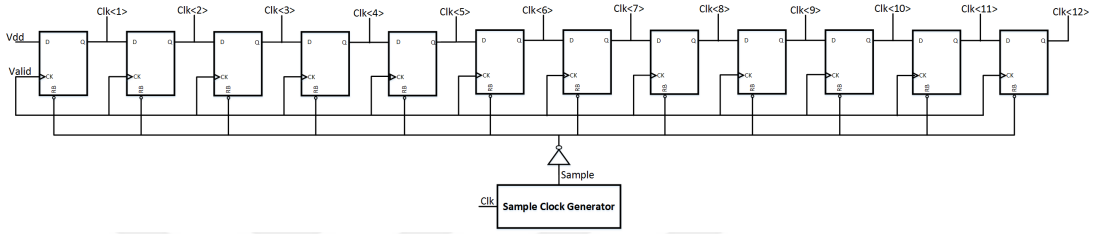


Figure 4.31: Clock Generator block diagram

given as input to clock generator. Valid is connected to the clock input of the D flip-flop's. At the rising edge of it, V_{dd} is passed to the next flip-flop and therefore relevant control clock is generated. Illustrated in Figure 4.32 is the spectre simulation results of the clock generator.

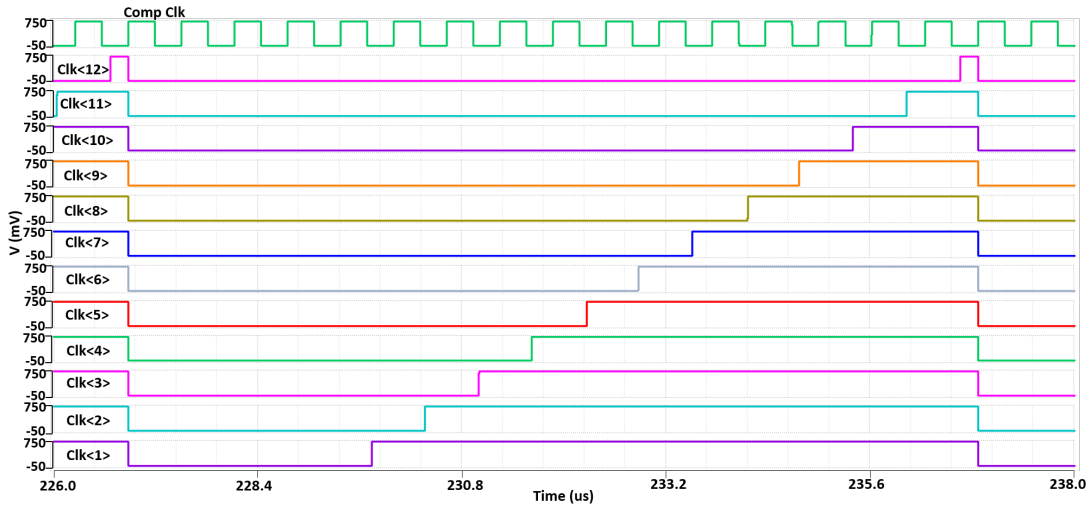


Figure 4.32: Control clocks spectre simulation

Clock generator also contains a sub-block, which is responsible from the generation of the sampling clock. Its block diagram is given in Figure 4.33.

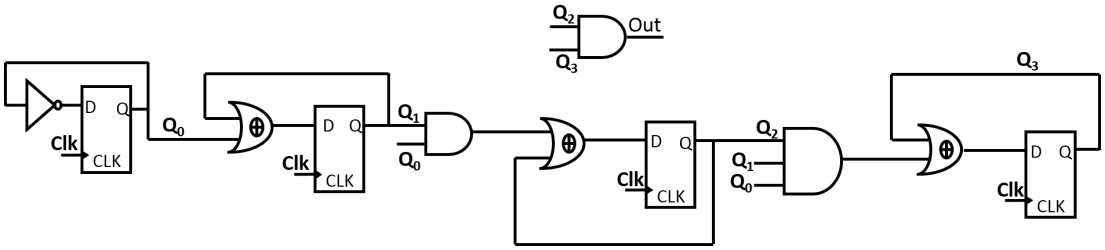


Figure 4.33: Sample clock generator block diagram

S/H control signal has a sample rate of 100 kHz and it is produced from the control signal of the dynamic comparator that runs at a frequency of 1.6 MHz, using a 4-bit synchronous counter. These two clocks are made synchronous with each other in order for S/H not to be affected from clock uncertainty. The spectre simulation results of these two signals are shown in Figure 4.34. The 4-bit counter counts up to 16, generating the frequency that is $\frac{1}{16}^{th}$ of the frequency of the control clock with a duty cycle of 25%. The truth table of this 4-bit counter can be seen in Table 4.1.

Table 4.1: Clock Generator Truth Table

Q_3	Q_2	Q_1	Q_0	out
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

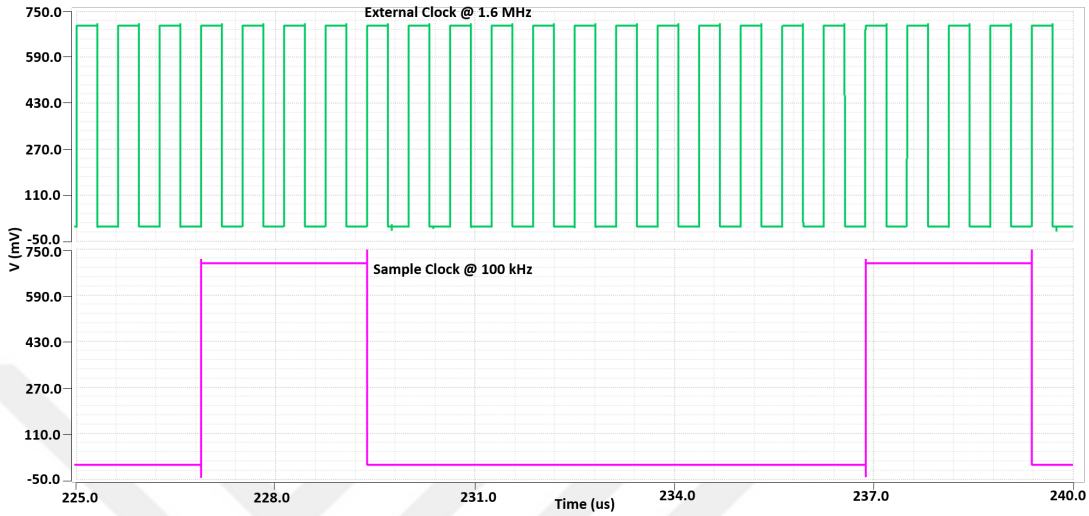


Figure 4.34: Spectre simulation of the sample clock and the control clock of the dynamic comparator

The layout of the clock generator is shown in Figure 4.35. Performing DRC and LVS checks and obtaining clear results, post layout simulations are completed and they are shown in Figures 4.36 and 4.37.

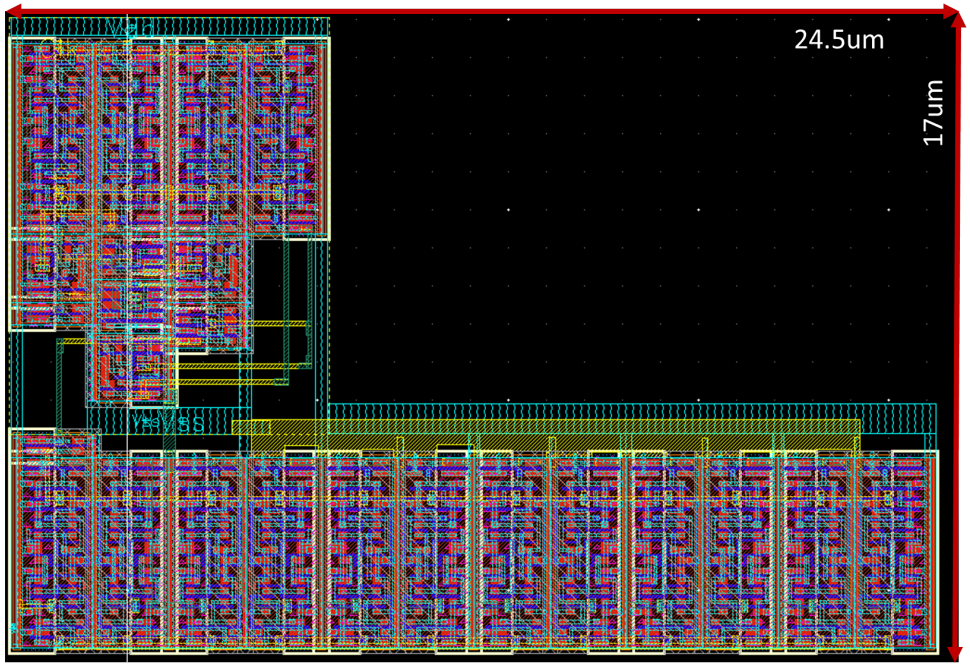


Figure 4.35: Clock generator layout

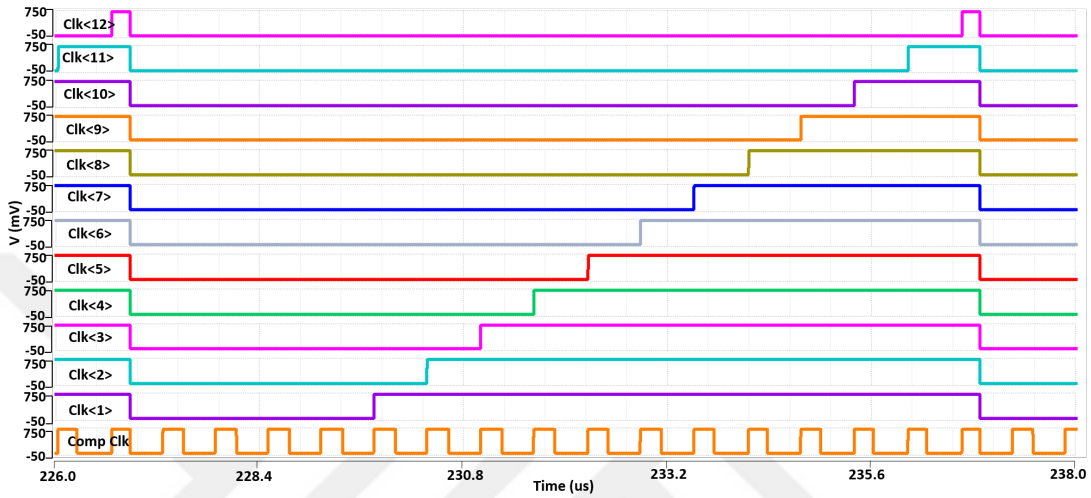


Figure 4.36: Extracted clock generator simulation

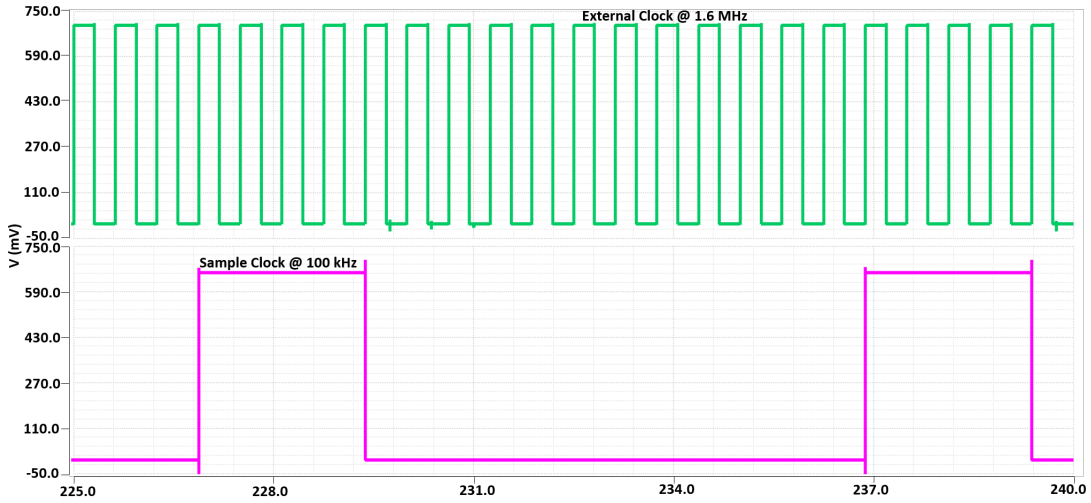


Figure 4.37: Extracted simulation of sample clock and control clock of dynamic comparator

4.4 Results

Having finished the design of the complete ADC, a testbench is prepared and it is simulated with schematic and post-layout spectre simulations. In this testbench, a differential analog signal is applied to the ADC and corresponding bits are observed. Figure 4.38 shows the spectre simulation results of the analog input and its corresponding digital bits. Observed from the figure is that, an analog

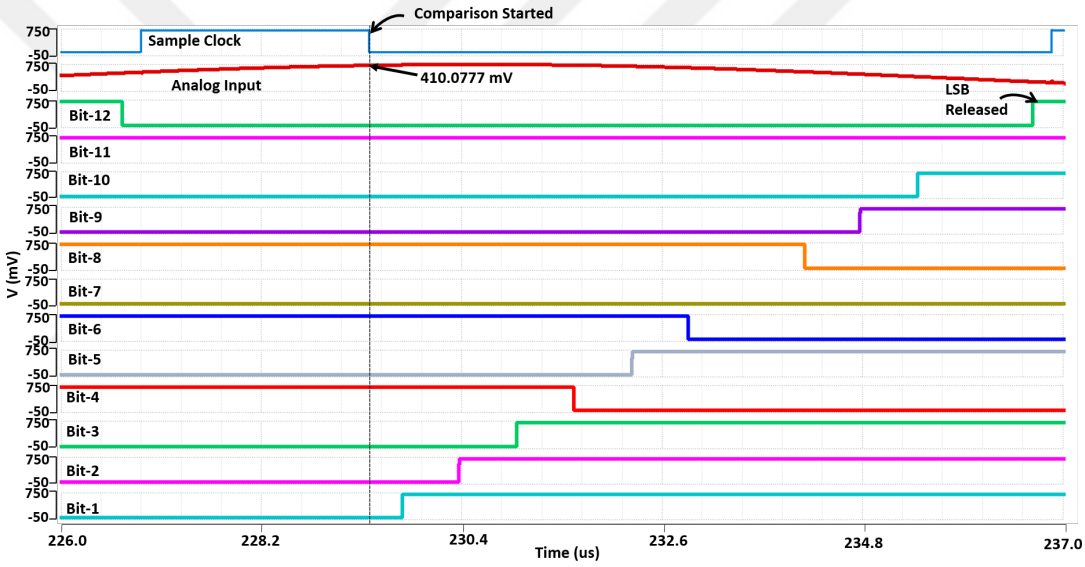


Figure 4.38: Spectre simulation of analog input and the corresponding digital bits

signal with a value of 410.0777 mV is converted to digital bits of '1110 1000 1111'. Keeping the two ends of full scale (+0.5 V, -0.5 V) in mind, the analog version of this digital result can be calculated as

$$\begin{aligned} V &= \frac{2048+1024+512+128+8+4+2+1}{4096} \cdot 1(V) - 0.5(V) \\ &= \frac{3727}{4096} - 0.5(V) \\ &= 409.91mV \end{aligned} \tag{4.5}$$

which is

$$410.077mV - 409.91mV = 167\mu V$$

different from the input and this value is smaller than 1 LSB, 244 μV. If all the conversion had been below 1 LSB an *ENOB* of 12 would have been obtained.

However, due to nonlinearity, noise and random mismatches, the simulated *ENOB* is less than 12. Furthermore, in order to get a more clear comparison, a Verilog DAC block is used in this testbench, which takes the generated digital bits and turns them into analog again using the equation 4.5, above. This is shown in Figure 4.39. The code used in the Verilog DAC is given in Appendix A.

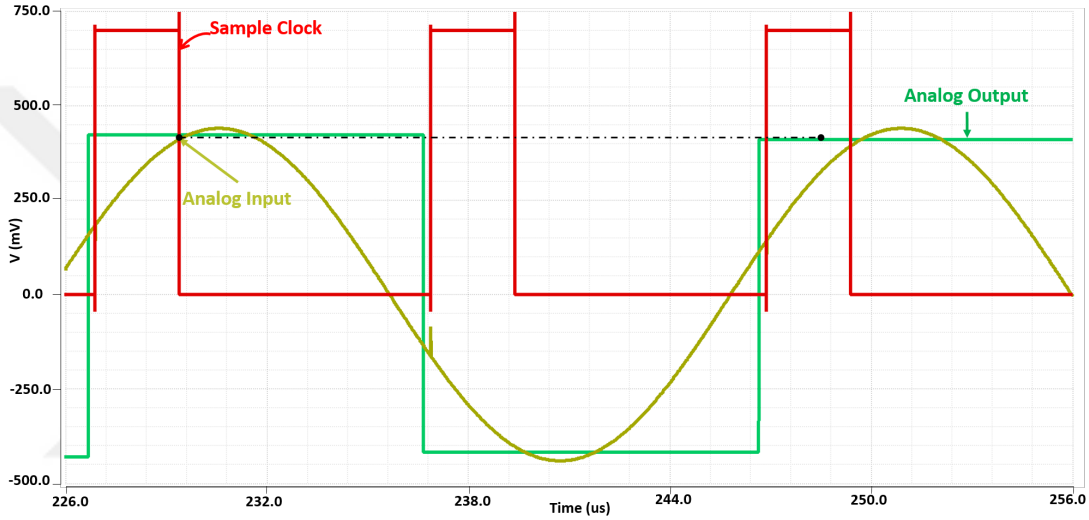


Figure 4.39: Spectre simulation of the comparison of input signal versus analog correspondence of digital bits

The analog input and its relevant analog output are quite close to each other such that the difference between them is not recognizable. Having shown this detailed analysis in Figure 4.39, the graph of a sinusoidal analog signal and its back converted analog version is given in Figure 4.40.

The post layout versions of spectre simulations for Figures 4.38 and 4.39 are given in Figures 4.41 and 4.42, respectively.

Moreover, FFT analysis of this digital output is also completed through its back converted analog version and its spectre and post-layout versions are shown in Figures 4.43 and 4.44, respectively. In these FFT analyses, a sinusoidal input signal with frequency of 49.21875 kHz (close to Nyquist rate, 50 kHz) is used and 128 samples are taken. The extracted performance results of the ADC is given in Table 4.2.

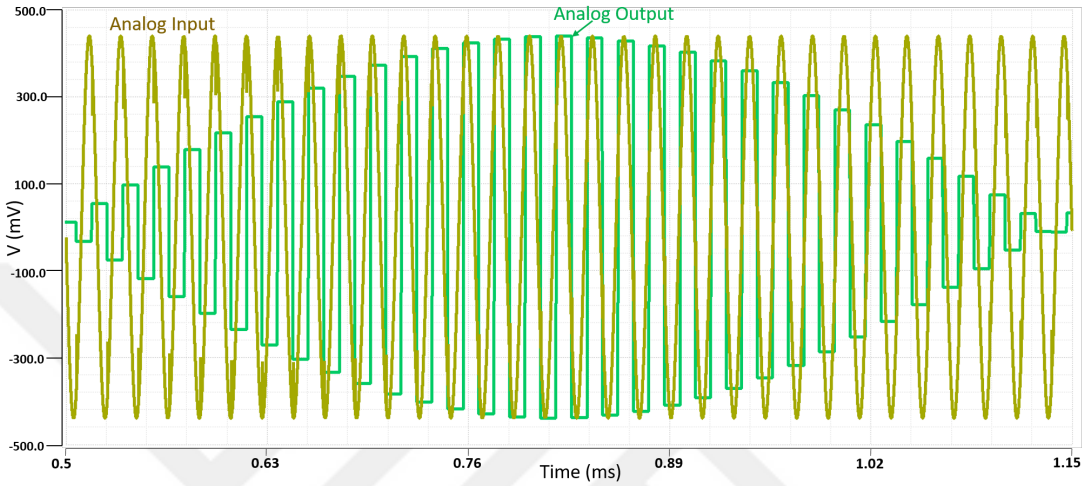


Figure 4.40: Simulation of analog input signal and its back converted analog correspondence

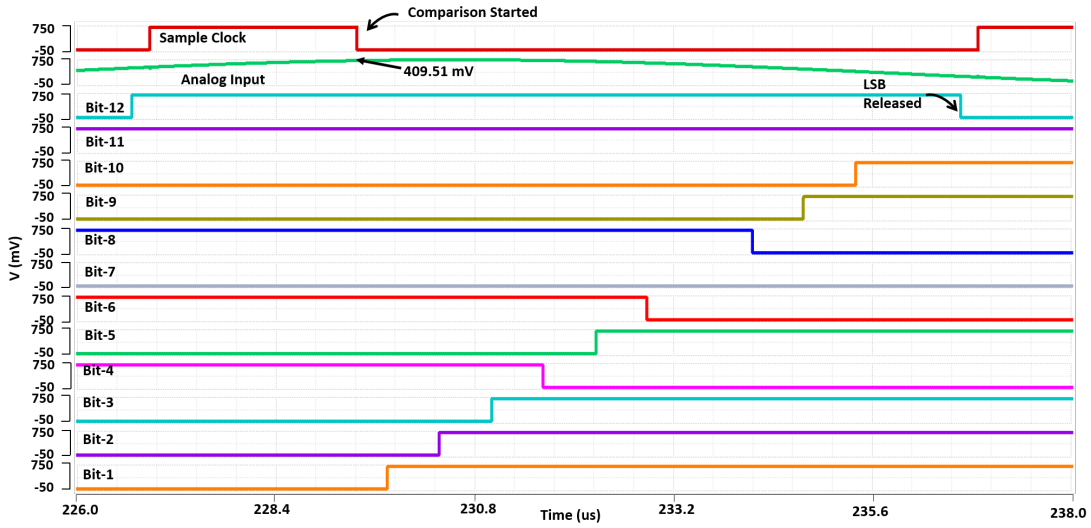


Figure 4.41: Extracted simulation of analog input and the corresponding digital bits

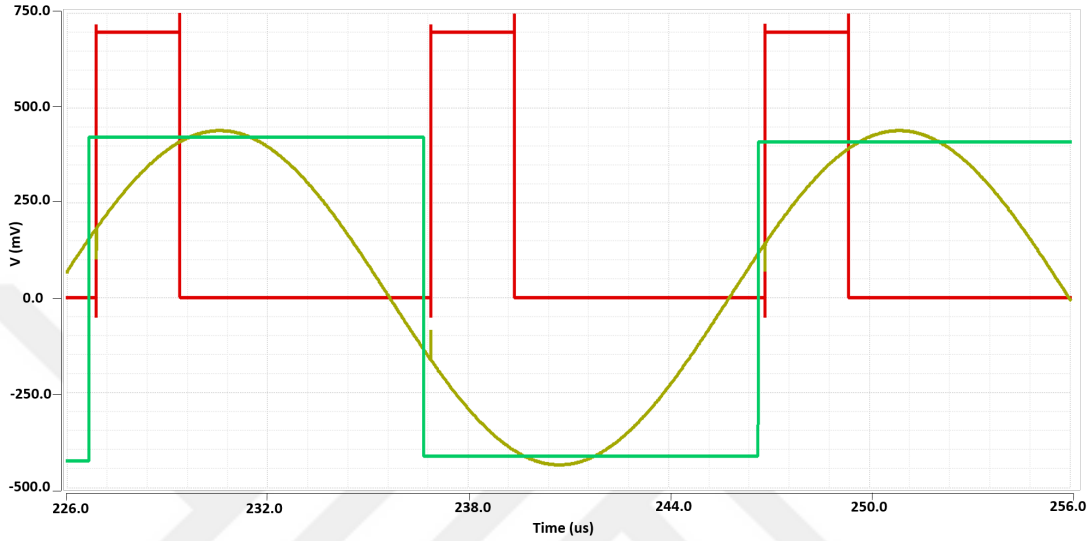


Figure 4.42: Extracted simulation of the comparison of input signal versus analog correspondence of digital bits

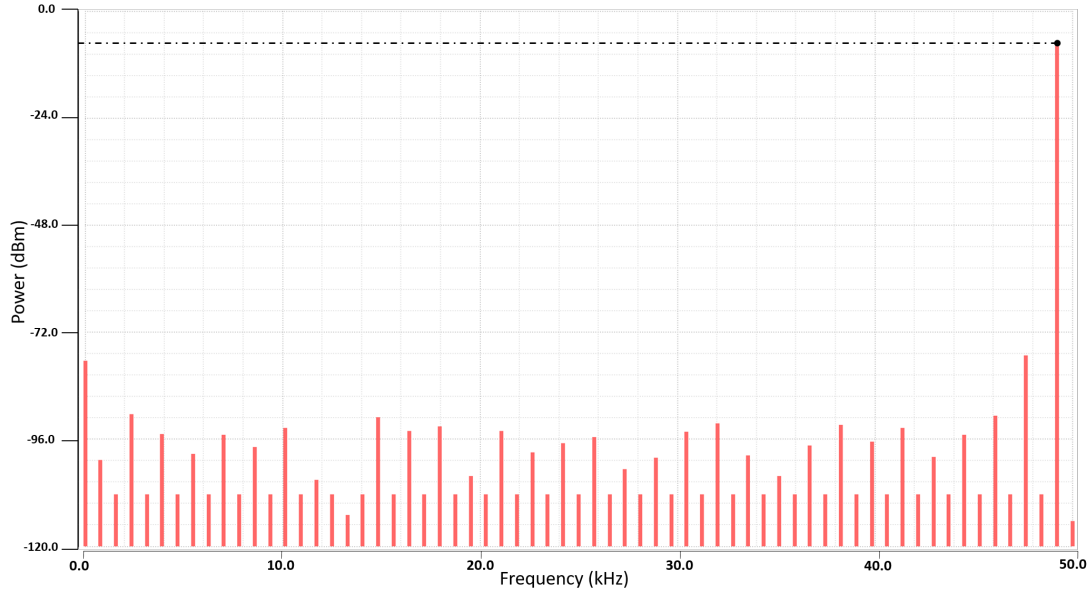


Figure 4.43: FFT of spectre simulation of back converted analog signal

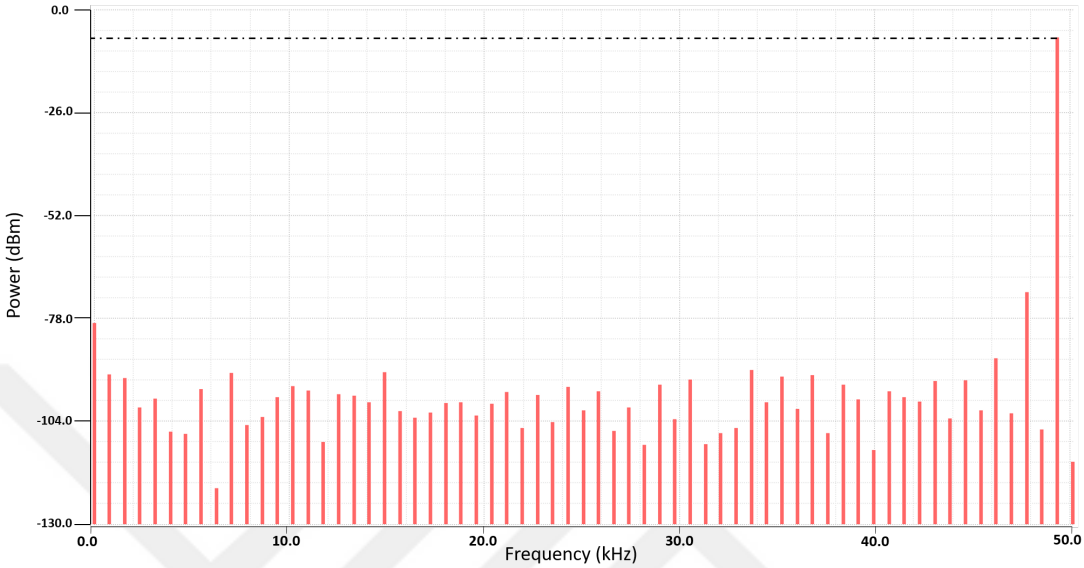


Figure 4.44: FFT of extracted simulation of back converted analog signal

The post and pre-layout simulations of each subblock, which have been shown above, seem almost the same with each other. The expected difference between the two simulation types shows up in FFT analyses. While SNDR was 68.58 dB in spectre simulations, it became 64.41 dB in post layout simulations. As a metric to compare the performance of this ADC with others, its figure of merit (FOM) can be calculated as in equation 4.6. This equation is very similar to the one which is given in equation 2.15, too.

$$\begin{aligned} FOM &= \frac{Power}{2^{ENOB} \times min\{2 \cdot ERBW, f_s\}} \\ &= \frac{2.16\ uW}{2^{10.41} \times 100\ kHz} \\ &= 15.9\ fJ/conv. - step \end{aligned} \tag{4.6}$$

Table 4.2: Extracted Performance Results

Technology	65nm CMOS
Resolution	12-bit
Input Capacitance	5 pF
Sampling Rate	100 kS/s
Input Range	1 V
ENOB	10.41
SFDR	65.48 dBc
SNDR	64.41 dB
SNR	71.92 dB
THD	-65.11 dB
Power	2.16 uW
FOM	15.9 fJ/conv.-step
Area	0.12 mm^2

Chapter 5

Conclusion

In this thesis, the design and implementation of a 12-bit 100 KS/s differential input SAR ADC for a sensor node in 65nm CMOS technology is reported. Thesis starts with an introduction part and continues with the literature review of ADCs and specifically talks about the SAR ADCs. Having completed those sections, detailed analysis of the proposed design of SAR ADC is given in Chapter 4.

Since it is for a sensor application, SAR ADC is preferred in this work as it is a good option for medium resolution and medium to high speed applications. One of the other reasons of choosing the SAR ADC is its high power efficiency needed in sensor nodes. Differential topology is used in order to double the dynamic range and cancel common mode noise. The ADC works with a 1.6 MHz clock source by generating a synchronous 100 kHz sampling clock.

Both schematic level design and layout are finished in Cadence Virtuoso. Clean DRC and LVS results are obtained from Calibre tool. The performance was verified using spectre with both schematic and extracted simulations. The design is sent to be manufactured through Europractice. Upon the arrival of the manufactured chips, measurements are going to be done for the verification of the design.

Bibliography

[1] Y. Chiu, "Data converters." EECT Lecture Notes, 2014.

[2] A. M. Abo, *Design for Reliability of Low-Voltage, Switched-Capacitor Circuits*. PhD thesis, UC Berkeley, 1999.

[3] Razavi, *Principles Data Conversion Design*. John Wiley & Sons, 1994.

[4] R. J. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*. Springer US, 2003.

[5] F. Maloberti, *Data Converters*. Springer US, 2007.

[6] A. S. Nastase, "An ADC and DAC integral non-linearity (inl)," 2009.

[7] H. Khurramabadi, "ADC Converters (Data Converter Metrics)." UC Berkeley Course, Analog-Digital Interfaces in VLSI Technology, Oct. 2007.

[8] M. W. Online, "Figure of Merit." https://www.merriam-webster.com/dictionary/figure

[9] R. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, pp. 539–550, apr 1999.

[10] G. C. T. Richard Schreier, *Understanding Delta-SIGMA Data Converters*. JOHN WILEY & SONS INC, 2004.

[11] A. M. A. Ali, A. Morgan, C. Dillon, G. Patterson, S. Puckett, P. Bhoraskar, H. Dinc, M. Hensley, R. Stop, S. Bardsley, D. Lattimore, J. Bray, C. Speir, and R. Sneed, "A 16-bit 250-MS/s IF sampling pipelined ADC

with background calibration," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2602–2612, dec 2010.

[12] Analog Devices, Inc. - Training Seminars, *High Speed System Applications*, 2006.

[13] Analog Devices, Inc., *AD9226[Data Sheet]*, 2000.

[14] "APP 1870, Sigma-Delta ADCs [Tutorial]." Retrieved from https://www.maximintegrated.com/en/app-notes/index.mvp/id/1870, Jan. 2003.

[15] M. Saberi, R. Lotfi, K. Mafinezhad, and W. A. Serdijn, "Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation adcs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, pp. 1736–1748, Aug 2011.

[16] J. McCreary and P. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. i," *IEEE Journal of Solid-State Circuits*, vol. 10, pp. 371–379, dec 1975.

[17] Y. Zhu, C. Chan, U. Chio, S. Sin, S. U, R. P. Martins, and F. Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1111–1121, June 2010.

[18] Yan Zhu, U-Fat Chio, He-Gong Wei, Sai-Weng Sin, Seng-Pan U, and R. P. Martins, "A power-efficient capacitor structure for high-speed charge recycling SAR ADCs," in *2008 15th IEEE International Conference on Electronics, Circuits and Systems*, pp. 642–645, Aug 2008.

[19] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," in *2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 184–187 Vol. 1, May 2005.

[20] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with Split Capacitor Array DAC," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 739–747, April 2007.

[21] W. Kester, "MT-021: ADC Architectures II: Successive Approximation ADCs." https://www.analog.com/media/en/training-seminars/tutorials/MT-021.pdf, 2009.

[22] C. Liu, S. Chang, G. Huang, and Y. Lin, "A 10-bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 731–740, April 2010.

[23] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 599–606, May 1999.

Appendix A

DAC Verilog Code

```
`include "discipline.h"
`include "constants.h"

// $Date: 1997/08/28 05:54:36 $
// $Revision: 1.1 $
//
//



//---------------------
// dac_12bit_ideal
//
// -  12 bit digital analog converter
//
// vd0..vd11: data inputs [V,A]
// vout:  [V,A]
//
// INSTANCE parameters
//    vref   = reference voltage that conversion is with respect to [V]
//    vtrans = transition voltage between logic high and low [V]
//    tdel,trise,tfall = {usual} [s]
//
// MODEL parameters
```

```
//    {none}

module dac_12bit_ideal ( vd11, vd10, vd9, vd8, vd7, vd6, vd5, vd4
   , vd3, vd2, vd1, vd0, vout,enable);
electrical vd11, vd10, vd9, vd8, vd7, vd6, vd5, vd4, vd3, vd2,
   vd1, vd0, vout,enable;
parameter real vref  = 1   from [0:inf);
real xref  = 1   from [0:inf);
parameter real trise = 1p from [0:inf);
parameter real tfall = 1p from [0:inf);
parameter real tdel  = 0.1p from [0:inf);
parameter real vtrans  = 0.35 from [0:inf);

    real out_scaled; // output scaled as fraction of 4096

    analog begin
    @(cross(V(enable)-vtrans,1))begin
    out_scaled = 0;
    out_scaled = out_scaled + ((V(vd11) > vtrans) ? 2048 : 0);
    out_scaled = out_scaled + ((V(vd10) > vtrans) ? 1024 : 0);
    out_scaled = out_scaled + ((V(vd9) > vtrans) ? 512 : 0);
    out_scaled = out_scaled + ((V(vd8) > vtrans) ? 256 : 0);
    out_scaled = out_scaled + ((V(vd7) > vtrans) ? 128 : 0);
    out_scaled = out_scaled + ((V(vd6) > vtrans) ? 64 : 0);
    out_scaled = out_scaled + ((V(vd5) > vtrans) ? 32 : 0);
    out_scaled = out_scaled + ((V(vd4) > vtrans) ? 16 : 0);
    out_scaled = out_scaled + ((V(vd3) > vtrans) ? 8 : 0);
    out_scaled = out_scaled + ((V(vd2) > vtrans) ? 4 : 0);
    out_scaled = out_scaled + ((V(vd1) > vtrans) ? 2 : 0);
    out_scaled = out_scaled + ((V(vd0) > vtrans) ? 1 : 0);
    end
    V(vout) <+ transition( ((xref*out_scaled/4096)-(xref/2)),
   tdel, trise, tfall );
    end
endmodule
```

ULTRA LOW POWER 12-BIT 100 kS/s DIFFERENTIAL SAR ADC IN 65 nm CMOS TECHNOLOGY

ORIGINALITY REPORT

16%	8%	7%	13%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Submitted to Nashville State Community College Student Paper	1%
2	Submitted to UT, Dallas Student Paper	1%
3	hdl.handle.net Internet Source	1%
4	Submitted to University of Macau Student Paper	1%
5	Submitted to University of Edinburgh Student Paper	1%
6	Submitted to Imperial College of Science, Technology and Medicine Student Paper	<1%
7	Submitted to CSU, San Jose State University Student Paper	<1%
8	Submitted to KTH - The Royal Institute of Technology	<1%