

HIGH FREQUENCY POWER SUPPLY DESIGN

A Thesis

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To my family...

ABSTRACT

Portability, power density, and energy efficiency are among the hottest topics of today. Therefore, the need for higher power-capacity, smaller size, and higher efficiency power supply is increasing day by day. At this point, the switching frequency has the most noticeable effect on the size of switching power converters. Utilizing high switching frequency, the converter size and weight can be reduced significantly; in other words, the power density can be increased. In addition, the high switching frequency decreases capacitor value and therefore electrolytic capacitors can be eliminated. As a result, reliable ceramic type capacitor can be employed.

The Switch Mode Power Supply (SMPS) converters utilize switching frequency as a basic feature of these converters and they have gained significant attraction recently due to their low weight, volume, and cost advantages. There are conventional SMPS topologies in the literature such as buck, boost, buck-boost, flyback, etc., which are hard switched topologies and their switching frequency can reach only 100 kHz levels. Increasing the switching frequency of these type of converters raises the losses inevitably. Hence, the switching frequency has to be chosen low for limiting the loss. As a result, these conventional topologies require a large capacitor and inductor values. In order to solve this problem, resonant converters which have soft switching behavior are proposed in the literature, and the switching frequency can reach up to MHz level. Among these converters, class E type resonant converter has a single switch which source (for MOSFET) has a ground connection hence it is easy to drive. Additionally, this converter has an easy design advantage because it uses a low number of components. Hence, in this thesis, class E resonant converter is chosen for these advantages. In this study, a class E DC/DC converter is analyzed,

simulated and implemented for in order to obtain 24 V/60 W output power from a 48 V input voltage. Additionally, 0.5 MHz and 1.2 MHz switching frequencies were selected for this particular research. On the other hand, the analyses were proven by PSIM simulations and experiments. From the experimental studies, it was seen that electrolytic capacitors can be eliminated by high switching frequency and ceramic type capacitors can be used instead of electrolytic counterparts.



ÖZETÇE

Taşınabilirlik, güç yoğunluğu ve enerji verimliliği bugünlerde en önemli konular arasında yer almaktadır. Dolayısıyla, yüksek güç yoğunluğuna, küçük boyuta ve yüksek verimliliğe sahip güç kaynaklarına ihtiyaç günden güne artmaktadır. Bu noktada, yüksek anahtarlama frekansı en önemli etkiye sahiptir. Yüksek anahtarlama frekansı yardımıyla dönüştürücü boyutu ve ağırlığı düşürülebilir, başka bir deyişle güç yoğunluğu arttırılabilir. Ek olarak, yüksek anahtarlama frekansının kapasitör boyutunu azaltmasıyla elektrolitik kapasitörler elimine edilebilir. Bunun sonucunda ise güvenilirliği ve ömrü yüksek seramik tipi kapasitörler kullanılabilir hale gelmektedir.

Anahtarlama Güç Kaynakları (AGK), anahtarlama frekansını devrenin temel özelliği olarak kullanır ve bu dönüştürücüler düşük ağırlık, hacim ve maliyet avantajından dolayı önemli bir ilgi kazanmıştır. Literatürde; buck, boost, buck-boost, flyback gibi sert anahtarlama yapan ve anahtarlama frekansı sadece 100 kHz seviyelerine kadar çıkabilen geleneksel topolojiler bulunmaktadır. Bu topolojilerde anahtarlama frekansını arttırmak istenmeyen bir şekilde kayıpları arttırmaktadır. Dolayısı ile kayıpları sınırlamak amacıyla anahtarlama frekansının küçük seçilmesi gerekmektedir. Anahtarlama frekansının küçük seçilmesinden dolayı bu dönüştürücüler yüksek kapasitör ve endüktans değerlerine ihtiyaç duyar. Bu problemi çözmek için literatürde yumuşak anahtarlama yapabilen ve anahtarlama frekansı MHz seviyelerine çıkabilen rezonant dönüştürücü topolojileri önerilmiştir. Bu dönüştürücüler içerisinde, E sınıfı topoloji tek bir anahtarlama elemanı kullanması ve bu anahtarlama elemanının sörs terminalinin toprağa bağlanmasından dolayı sürme avantajı sunar. Ayrıca, E sınıfı dönüştürücü kolay tasarıma ve düşük sayıda komponente sahiptir. Bundan dolayı bu tezde E sınıfı DC/DC dönüştürücünün 48 V giriş kaynağından 24 V/60 W çıkış

oluřturduėu durum iin analiz, simlasyon ve deneysel alıřmaları yapılmıřtır. Ek olarak anahtarlama frekansı iin 1.2 MHz ve 0.5 MHz seilmiř olup alıřmalar bu anahtarlama frekanslarında gerekleřtirilmiřtir. Diėer taraftan, analizler PSIM simlasyonları ve deneysel alıřmalarla ispatlanmıřtır. Deneysel alıřmalarda, yksek anahtarlama frekansında alıřmanın bir sonucu olarak elektrolitik kapasitr yerine seramik kapasitrlerin kullanılabilceėi ve elektrolitik kapasitrlerin elimine edilebileceėi grlmřtr.



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CHAPTER I

INTRODUCTION

Recently, researchers intend to decrease the size and weight of power converters for portability. The size and weight of the passive components is highly dependent on their values which decrease by the switching frequency proportionally. In other words, high switching frequency reduces the need for passive energy storage. Hence, the use of magnetic cores can be replaced by PCB planar magnetic core or air core magnetic [1], [2]. Additionally, the electrolytic capacitors can be exchanged with ceramic capacitors which serves high lifetime and reliability [3], [4].

In the literature, there are conventional type switch mode power supply (SMPS) converters such as buck [5],[6] boost [7], buck-boost, flyback, forward converters [8],[9] which eliminates the linear type power converters that use low frequency (50-60 Hz) transformer. However, these types of SMPS converters only operates up to 100 kHz switching frequency levels for limiting the power converter losses. In order to decrease the size and weight of the converter more, resonant type converters which operates under soft switching up to MHz switching frequency levels must be required. Among resonant converters, there are series, parallel, series-parallel, LLC, class DE, SEPIC [10], class EF2 (ϕ 2) [11],[12] and class E [13],[14] converters exist.

In series resonant converter, the input-to-output voltage transfer function can be maximum "1" and it cannot step up the voltage. On the other hand, parallel resonant converter has high circulating current which decreases the converter's efficiency. Additionally, series-parallel resonant converter includes high number of components and this make the design complex.

LLC type converters are mostly preferred in the industry due to isolation advantage. However, this converter uses H-bridge switches at the input stage, and it requires isolated gate drivers. Additionally, the converter operates wide switching frequency range for regulating the output voltage [15], and it can increase the AC resistance of the transformer and then this causes high conduction losses [16].

The other well-known resonant converter is the class DE topology [17]. Although this topology requires one inductance and provides low voltage stress on the switches, it has a high-side switch [17],[18], hence its gate driver design is complex at high switching frequencies. On the other hand, this converter can regulate the output voltage with a narrow change in the switching frequency range.

Additionally, in the literature, SEPIC [4] and class $\phi 2$ [19], [20] topologies are proposed. Although SEPIC has a low number of components, it has a more complicated design process. On the other hand, class $\phi 2$ converter uses more inductance than the SEPIC and class E converters [20]. Although it decreases the voltage-stress on the switch, it suffers from the high circulating current [18] which is resulted from the 3rd harmonic content of the resonant current.

On the other hand, one of the most promising topologies for the resonant converter is the class E based topology [21]. This topology has a single switch whose source terminal is connected to the low side (ground), which makes the gate driving relatively easy [22], [23]. Moreover, its inverter and rectifier stages can be designed independently and it has easy tuning advantages. On the other hand, this converter can regulate the output voltage with a narrow change in the switching frequency range.

In this thesis, class E SMPS converter topology is chosen for the conversion from 48 V input to 24 V 60 W output power. This thesis is organized as follows: The first chapter includes introduction about background and motivation, objectives and scope. Chapter II, the switch mode power supply topologies are introduced. On

the other hand, analysis, design, simulation and experimental results is presented in Chapter III. At the end, the results and conclusion are given in Chapter IV.

1.1 Background and Motivation

Today, the usage of electronic devices has become unavoidable. The most important part of electronic devices is the power stage. Generally, a switching power supply is used in the chargers of electronic devices such as mobile phone and computer that we use in daily life. The maximum power density can be obtained from small-sized converters and it is the required feature in power supplies.

The effective usage of the recently proposed topologies and the combinations paves the way for development. The size and weight of the power supplies are mainly due to passive components in the circuit. Nowadays in the current market, the power supplies work around at 20-120 kHz switching frequency. In order to reduce the size of these power supplies, it is necessary to switch to the MHz range. The value and therefore the size of passive components decreases with increasing the switching frequency. With these developments in power supply research, it has become possible to reduce the size of passive elements in power supplies. In addition, the passive components in the circuit (especially the electrolytic capacitor) are critical to the lifetime the circuit. The usage of the electrolytic capacitor will be eliminated [24] by decreasing the value of the capacitor and the use of long lifetime ceramic capacitors will be possible. On the other hand, the major source of cost in power boards is passive components such as inductance and transformer. Thus, the reducing value of passive components in the circuit is a positive development, in terms of the cost.

1.2 Objectives and Scope of the Thesis

The aim of this thesis is to examine power topologies suitable for high-frequency operation. After the investigations, the switching frequency of the selected power topology has been increased to 1.2 MHz and the topology has been analyzed, simulated and

designed.

The class E converters are used at a low voltage level due to high voltage stress on the switch. Hence 48V DC input, which can be obtained from a suitable isolated Power Factor Correction (PFC) circuit, is selected for experimental studies.

The aim of this study is to investigate the design consideration of a class E DC/DC converter without using an electrolytic capacitor.



CHAPTER II

SWITCH MODE POWER SUPPLY (SMPS) TOPOLOGIES

In this chapter; conventional, resonant and class E based SMPS topologies will be introduced.

2.1 *Conventional Non-isolated SMPS Topologies*

The conventional non-isolated SMPS topologies have high switching losses due to hard switching. Hence, low switching frequencies are chosen generally, which increases the size and weight of passive components in circuits. In this section, conventional SMPS topologies such as Buck, Boost, Buck-Boost, Forward and Flyback which operates under Continuous Current Mode (CCM), will be introduced briefly.

2.1.1 Buck Converter

The Buck converter, which can be seen in the Figure 1, step down the input voltage and forms low voltage at the output. The input to output voltage transfer function for CCM operated Buck converter is given in equation (1).

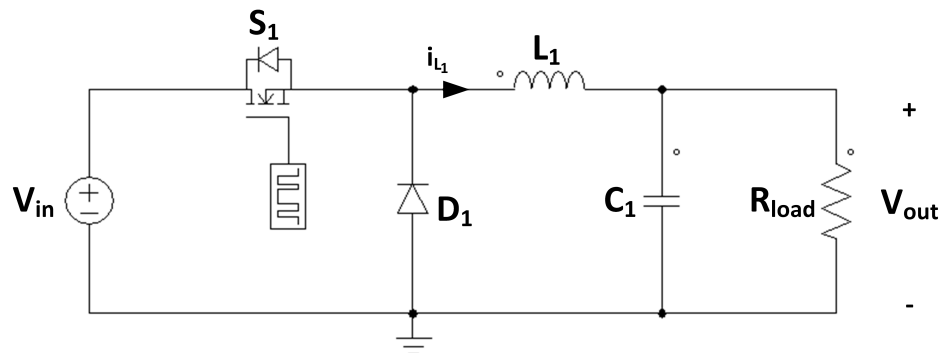


Figure 1: Schematic of the Buck converter.

$$\frac{V_{out}}{V_{in}} = D \quad (1)$$

In this equation, V_{out} represents output voltage, V_{in} is the input voltage and D is the duty ratio of the Pulse Width Modulation (PWM). From this equation it can be seen that, the output voltage only depends on the duty ratio which is the inherent characteristic of CCM operation and that makes the control simple. On the other hand, L_1 and C_1 can be chosen by using equation (2) and (3) [9], respectively.

$$L_1 = \frac{V_{out}(1-D)}{\Delta i_{L_1} f_s} \quad (2)$$

$$C_1 = \frac{1-D}{8L_1 \left(\frac{\Delta V_{out}}{V_{out}} \right) f_s^2} \quad (3)$$

In these equations, Δi_{L_1} is the peak to peak current ripple of the inductance, ΔV_{out} is the peak to peak voltage ripple of the output voltage, and f_s is the switching frequency of the circuit. It can be seen from these equations that L_1 and C_1 values decreases with the increasing of the switching frequency.

2.1.2 Boost Converter

The Boost converter which can be seen in Figure 2, step up the input voltage and higher output voltage can be obtained. The input to output voltage transfer function is given in (4).

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \quad (4)$$

From (5) and (6), L_1 and C_1 can be calculated [9], respectively.

$$L_1 = \frac{V_{in}D}{\Delta i_{L_1} f_s} \quad (5)$$

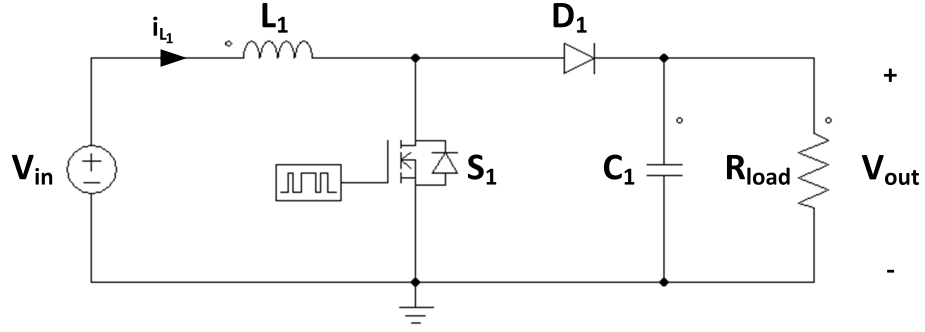


Figure 2: Schematic of the Boost converter.

$$C_1 = \frac{D}{R_{load} \left(\frac{\Delta V_{out}}{V_{out}} \right) f_s} \quad (6)$$

where, R_{load} is the output load resistance.

2.1.3 Buck-Boost Converter

Depending on the duty ratio of the switch, a higher or lower voltage than the input voltage can be obtained at the output of the Buck-Boost converter. The Buck-Boost converter schematic is given in the Figure 3. On the other hand, the input to output voltage transfer function is given in (7).

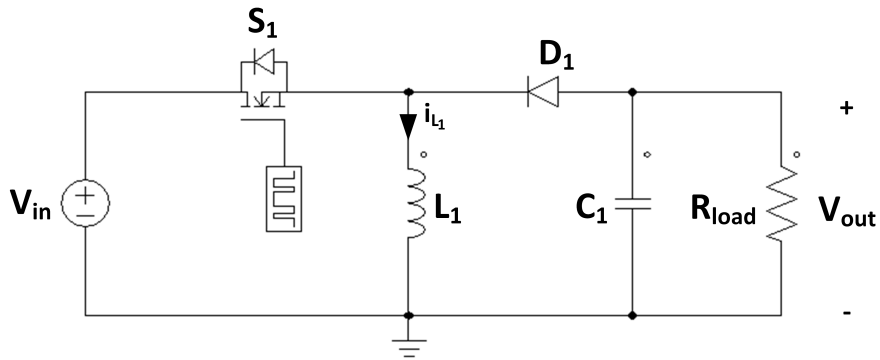


Figure 3: Schematic of the Buck-Boost converter.

$$\frac{V_{out}}{V_{in}} = -\frac{D}{1-D} \quad (7)$$

The required C_1 and L_1 values can be chosen by using (8) and (9) [8], respectively.

$$L_1 = \frac{V_{in}D}{\Delta i_{L_1} f_s} \quad (8)$$

$$C_1 = \frac{D}{R_{load} \left(\frac{\Delta V_{out}}{V_{out}} \right) f_s} \quad (9)$$

Conventional SMPS topologies have hard switching because the switching component is turned on without before reaching zero the voltage and/or current. The traditional converters are used up to 100 kHz switching frequency levels. In these topologies, when the frequency is increased to MHz level, switching losses dramatically increase and energy efficiency decreases.

2.2 Conventional Isolated SMPS Topologies

These topologies are preferred in order to eliminate the disadvantage of the common ground between the input and output at the conventional DC/DC converters (buck, boost, etc.). One way to electrically isolate the output and input is to use a transformer. Topologies such as Forward and Flyback provide isolation with the transformer for the circuit.

2.2.1 Forward Converter

The Forward converter [9] is derived from Buck converter which schematic is given in the Figure 4. This converter solves the leakage inductance current problem which increases the withstand voltage of the switch. However, it must use a reset winding with uses $D3$ diode. The input to output voltage transfer function is given in (10).

$$\frac{V_{out}}{V_{in}} = \left(\frac{D}{1-D} \right) \left(\frac{N_2}{N_1} \right) \quad (10)$$

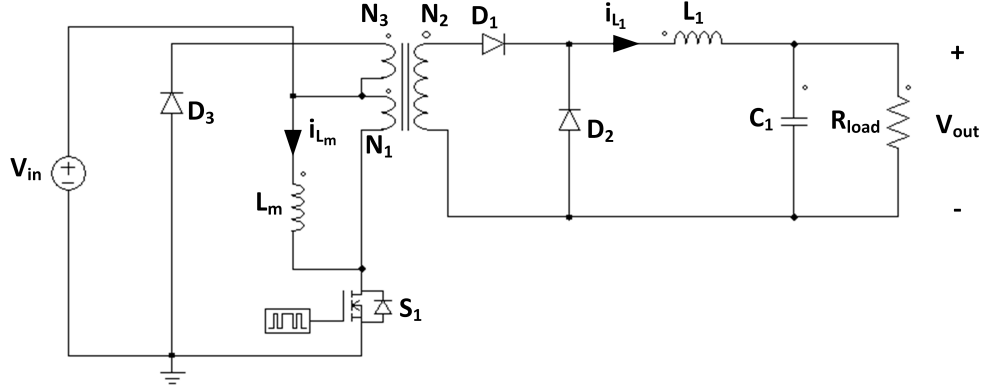


Figure 4: Schematic of the Forward converter.

In this equation, N_1 is the primary turn number and N_2 is secondary turn number of the transformer. The components values of this topology can be selected by (11), (12) and (13).

$$L_m = \frac{V_{in} D}{\Delta i_{L_m} f_s} \quad (11)$$

where L_m is the magnetising inductance.

$$L_1 = \left(1 - \frac{1}{V_{in}} \frac{N_1}{N_3} V_{out}\right) \frac{V_{out}}{\Delta i_{L_1} f_s} \quad (12)$$

N_3 is the reset winding turn number.

$$C_1 = \left(\frac{V_{out}}{\Delta V_{out}}\right) \left(\frac{1-D}{8L_1 f_s^2}\right) \quad (13)$$

For proper resetting of the transformer, the equation (14) is used.

$$D \left(1 + \frac{N_3}{N_1}\right) < 1 \quad (14)$$

2.2.2 Flyback Converter

The Flyback converter is derived from the Buck-Boost converter and the circuit schematic is given in Figure 5. Although the flyback converter uses low number

of components, it suffers from using high withstand switch. The input and output voltage transfer function is given in (15). The components of the converter is calculated by using (16) and (17) [9].

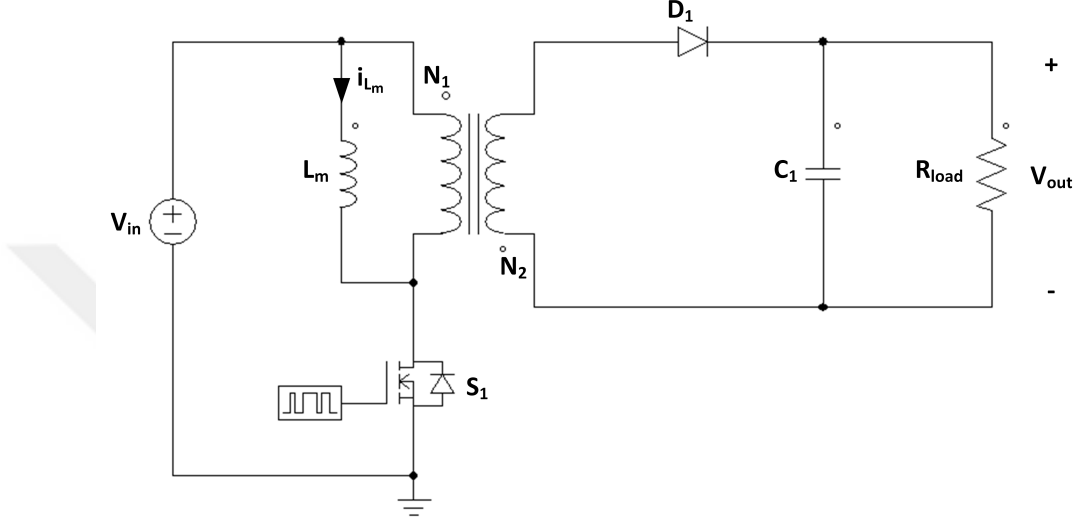


Figure 5: Schematic of the Flyback converter.

$$\frac{V_{out}}{V_{in}} = \left(\frac{D}{1-D} \right) \left(\frac{N_2}{N_1} \right) \quad (15)$$

$$L_m = \left(\frac{N_1}{N_2} \right)^2 \frac{(1-D)^2 R_{load}}{2f_s} \quad (16)$$

$$C_1 = \frac{V_{out}}{\Delta V_{out}} \frac{D}{R_{load} f_s} \quad (17)$$

The flyback based converters have a low number of components, low volume and cost, it has the problem of leakage inductance energy [25].

2.3 Resonant SPMS Topologies

The conventional resonant SPMS topologies comprise (6) a switch network (full or half bridge converter), a resonant tank network(7), a rectifier network, and a filter

network. These topologies can be classified as series, parallel, series-parallel, and LLC resonant converter which is given in Figure 6 and these topologies will be described briefly in this section.

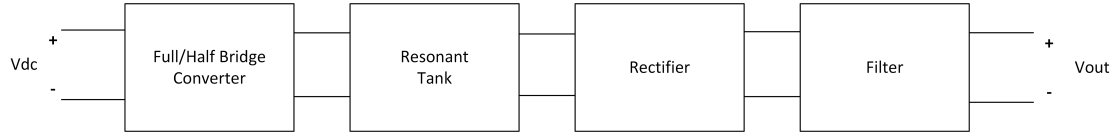


Figure 6: The architecture of resonant converters.

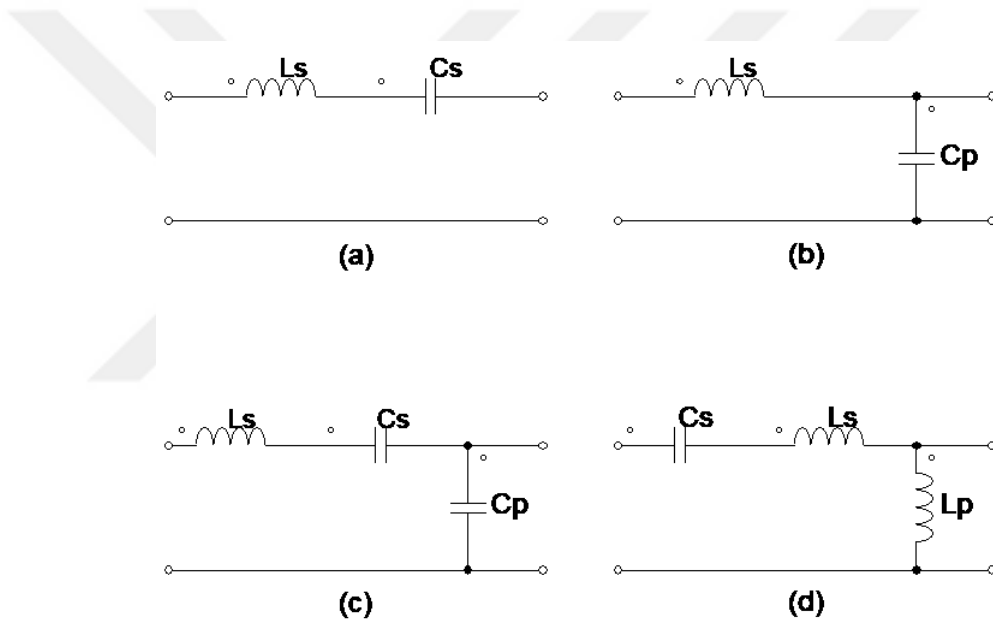


Figure 7: Resonant tank networks a) Series, b) Parallel, c) Series-Parallel, d) LLC resonant.

2.3.1 Series Resonant Converter

The series resonant converter [9] contains a resonant inductor L_r and a resonant capacitor C_r which are connected serially to the output (that is shown in Figure 8). Due to using the series capacitor, this converter blocks DC current for transformer. On the other hand, a large filter capacitor C_f which is used at the output, makes the output voltage ripple small.

The impedance of the inductance and capacitance can be expressed in (18) and (19), respectively. In these equations, f_s is the switching frequency in Hz and can be expressed as in (20) using the switching frequency in rad/sec.

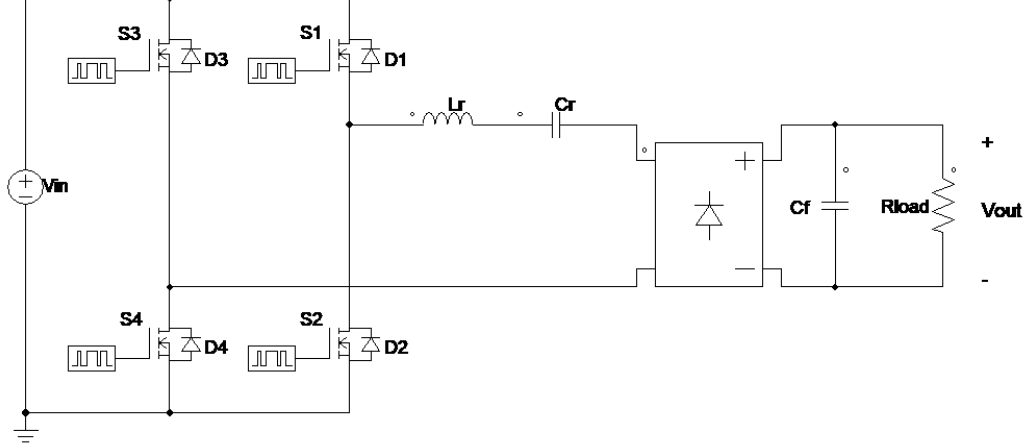


Figure 8: Schematic of the Series resonant converter.

$$X_{L_r} = 2\pi f_s L_r \quad (18)$$

$$X_{C_r} = \frac{1}{2\pi f_s C_r} \quad (19)$$

$$f_s = \frac{\omega_s}{2\pi} \quad (20)$$

For obtaining resonant case, X_{L_r} must be equal to X_{C_r} , by equating (18) and (19), the component values L_r and C_r can be calculated by using (21).

$$L_r C_r = \frac{1}{4\pi^2 f_s^2} \quad (21)$$

$$Q = \sqrt{\frac{L_r}{C_r}} \frac{\pi^2}{8R_{load}} \quad (22)$$

where the quality factor of the circuit Q is calculated with the equation (22) and most of the studies select Q is bigger than 7 for obtaining sinusoidal tank current. In the design stage, once the Q is selected, the L_r and C_r can be calculated from the equations (21) and (22) easily.

The resonant frequency of the converter can be calculated by using (21) and it can be expressed in (23).

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (23)$$

The input and output voltage transfer function M is shown in (24).

$$M = \frac{1}{\sqrt{1 + Q^2 \left(\frac{\omega_r}{\omega_s} - \frac{\omega_s}{\omega_r} \right)^2}} \quad (24)$$

where ω_s is the switching frequency in rad/sec. According to this equation, the input and output voltage transfer function depends on Q hence R_{load} , and the maximum value of M is calculated as 1. As a conclusion, the main disadvantage of this converter is that it cannot increase the voltage level.

2.3.2 Parallel Resonant Converter

The parallel resonant converter [9] is given in Figure 9. In this figure, the resonant tank capacitor C_r is connected in parallel to the output load. Although this converter can step up the voltage, it has high circulating currents in the circuit even in light load conditions [26]. The design stage of the parallel resonant converter is the same as series resonant converter, it only has different voltage transfer function which is given in equation (25).

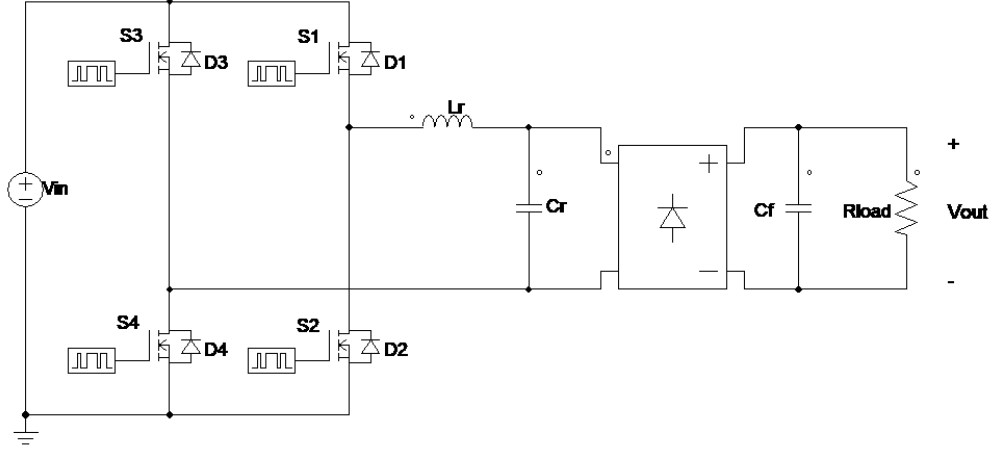


Figure 9: Schematic of the Parallel resonant converter.

$$M = \frac{8}{\pi^2} \frac{1}{\sqrt{\left(1 - \left(\frac{\omega_s}{\omega_r}\right)^2\right)^2 + \left(\frac{1}{Q} \frac{\omega_s}{\omega_r}\right)^2}} \quad (25)$$

2.3.3 Series-Parallel Resonant Converter

Series-parallel resonant converter [9] is a combination of series and parallel resonant converters. This converter includes one inductance and two capacitance for resonant circuit which can be seen in the Figure 10. The resonant frequency, quality factor of the converter, and the voltage transfer function of the converter are given in the equations (26), (27), and (28), respectively.

$$\omega_r = \frac{1}{\sqrt{L_s C_s}} \quad (26)$$

$$Q = \frac{8}{\pi^2 R_{load}} \sqrt{\frac{L_s}{C_s}} \quad (27)$$

$$M = \frac{1}{\left| \sqrt{1 + \left(\frac{C_p}{C_s} - \omega_s^2 L_s C_p\right) + j \left(\frac{8}{\pi^2 R_{load}}\right) \left(\omega_s L_s - \frac{1}{\omega_s C_s}\right)} \right|} \quad (28)$$

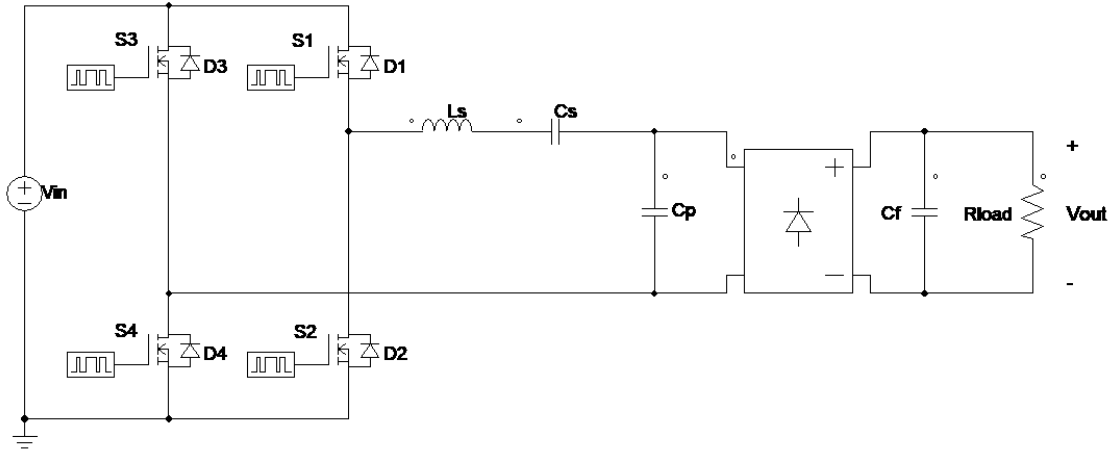


Figure 10: Schematic of the Series-Parallel resonant converter.

2.3.4 LLC Resonant Converter

The LLC resonant converter, which is the another combination of series-parallel resonant converter is given in the Figure 11. Among resonant converters, LLC type converters are mostly preferred in the literature due to isolation advantage. However, this converter operates wide switching frequency range for regulating the output voltage [15], and it can increase the ac resistance of the transformer and then this causes high conduction losses [16]. In the design stage, L_p/L_s is usually selected between 5 and 10 for the minimum voltage gain [27].

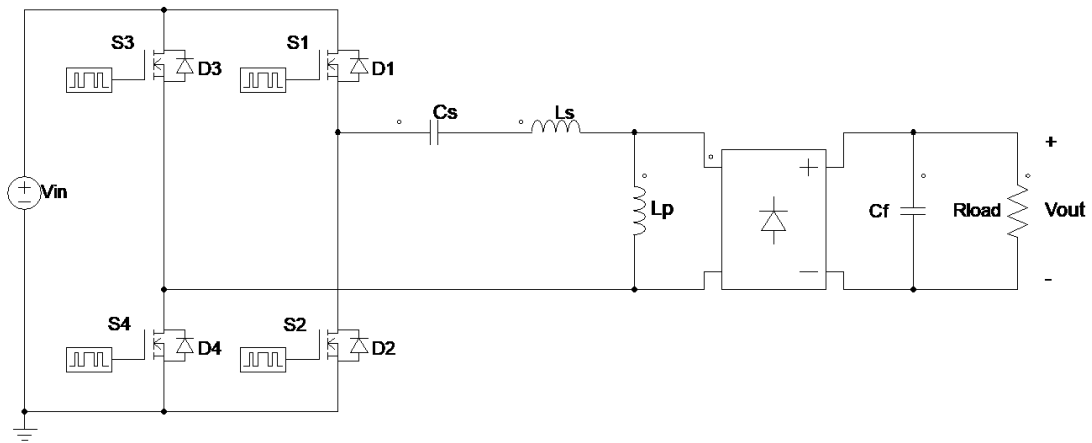


Figure 11: Schematic of the LLC resonant converter.

$$\omega_s = \frac{1}{\sqrt{L_s C_s}} \quad (29)$$

$$\omega_p = \frac{1}{\sqrt{L_p C_s}} \quad (30)$$

$$Q = \sqrt{\frac{L_s}{C_s}} \frac{\pi^2}{8R_{out}} \quad (31)$$

$$C_s = \frac{\pi}{16Qf_s R_{out}} \quad (32)$$

$$L_s = \frac{1}{(2\pi f_s)^2 C_s} \quad (33)$$

$$L_p = \frac{L_p^2}{L_s (2L_p + L_s)} + 1 \quad (34)$$

$$M = \sqrt{\frac{L_p}{L_p - L_s}} \quad (35)$$

As compared to the other resonant topologies (series, parallel, etc.), the LLC resonant converter has a simple and flexible structure, it works Zero Voltage Switching (ZVS) for switches [28] and Zero Current Switching (ZCS) for rectifiers. Conversion efficiency optimized at high input at the LLC. LLC converters are frequently used for step-down the input voltage and they are preferred 400-4000 W power range [29].

In order to eliminate the disadvantages of the aforementioned topologies (series, parallel, series-parallel and LLC) in high-frequency operation, the class E amplifier (inverter) based resonant converters which are also used in RF applications are examined.

2.4 Class E Based Resonant Converter Topologies

The topologies in this section are derived from class E resonant converter and are suitable for operation in the high-frequency range. class $\phi 2$, class DE and single-ended primary-inductor converter (SEPIC) will be introduced.

The high voltage stress on the switch is the biggest challenge in single-switch topologies, however, for high switching frequency operation, are preferred because of having a high side gate driver and fewer complexity advantages.

2.4.1 Class E Resonant Converter

The class E resonant converter which is given in the Figure 12 will be described in Section 3.1.

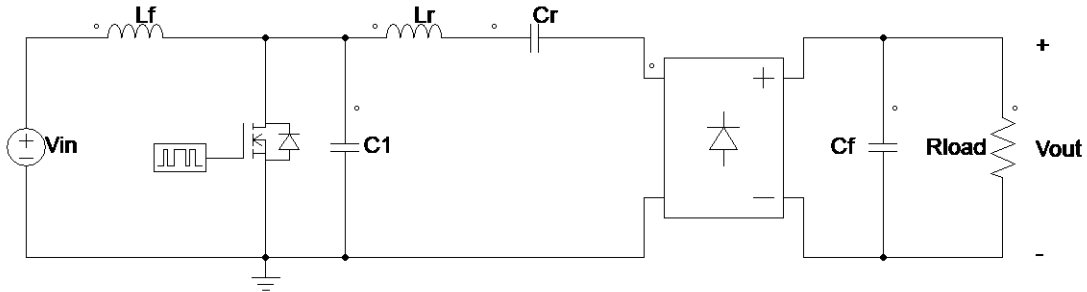


Figure 12: Schematic of the class E resonant converter.

2.4.2 Class DE Resonant Converter

The class DE resonant converter, given in the Figure 13, combines the advantages of the low voltage stress of class D converter and ZVS operation of class E converter [30]. Another advantage of this converter is that it uses only one inductor which is half of the class E topology.

Design equations of this topology for the component values are given below [30]:

$$R_{load} = \frac{V_{in}^2}{2\pi^2 P_{out}} \quad (36)$$

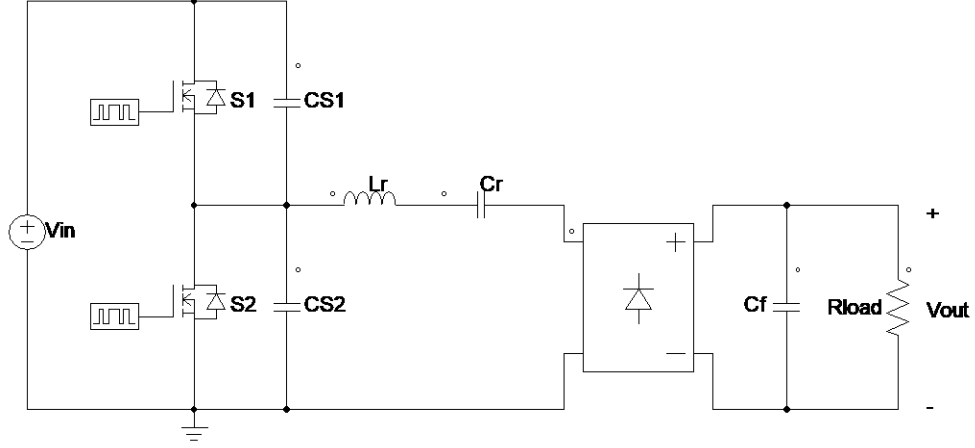


Figure 13: Schematic of the class DE resonant converter.

where P_{out} is the output power of the converter.

$$C_{S1} = C_{S2} = \frac{1}{2\pi\omega_s R_{load}} = \frac{\pi P_{out}}{\omega_s V_{in}^2} \quad (37)$$

C_{S1} and C_{S2} are the output capacitance of switches.

$$L_r = \frac{Q_L R_{load}}{\omega_s} \quad (38)$$

$$C_r = \frac{1}{\omega_s R_{load} (Q_L - \frac{\pi}{2})} \quad (39)$$

However, having a high-side switch is an important disadvantage of class DE converter in terms of driving difficulties of high-side switch. An application of the topology and a proposed driving technique can be seen in [17].

2.4.3 SEPIC Resonant Converter

The SEPIC resonant converter schematic is given in the Figure 14. It is difficult to select the inductance and capacity of this converter compared to other converters and

there are no fixed design equations. Therefore, the equations are not presented in this thesis, but one design method for the converter can be seen in [31, 32, 10].

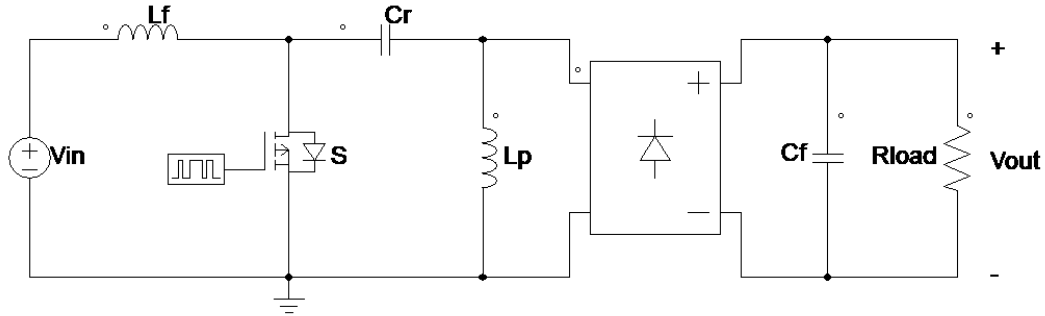


Figure 14: Schematic of the SEPIC resonant converter.

2.4.4 Class EF2 ($\phi 2$) Resonant Converter

As mentioned before, the problem of voltage stress on the switch has great importance in topologies which utilizes single switch such as class E and SEPIC converter. This high voltage stress drawback can be reduced to 2-2.5 times instead of 3.56 times the input voltage by using an additional multi-resonant network in front of the class E converter [33]. The class $\phi 2$ resonant converter schematic which is given in the Figure 15. However, it is an undesirable situation because it exploits additional resonant components which brings design complexity.

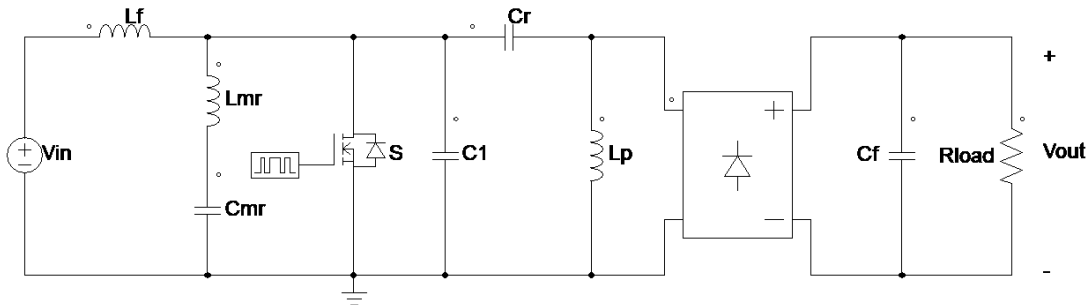


Figure 15: Schematic of the class $\phi 2$ resonant converter.

This converter cancels the third harmonic of the voltage on MOSFET (V_{ds}). As a

result of this, MOSFET's withstand voltage decreases [19]. The design stage of this converter is the same calculation as class E converter however it has two additional components which are specified by equation (40), (41) [34].

$$L_{mr} = \frac{1}{15\pi^2 f_s^2 C_1} \quad (40)$$

$$C_{mr} = \frac{15}{16} C_1 \quad (41)$$

In this topology, the resonant currents in the switching frequency are the same, but there are additional currents from the third harmonic, resulting in more losses than the class E due to the addition of third harmonics [21].

The comparison of class E based resonant converters are given in Table 1. From this table, it can be seen that class E is advantages and it will be analyzed in the next Section.

Table 1: Advantages and disadvantages of the class E-based topologies

	Advantage	Disadvantage
Class E	single switch low-side switch easy design	large-voltage stress
Class DE	low-voltage stress one inductor	high-side switch
SEPIC	low-side switch	complex design
Class $\phi 2$	reduced voltage stress low-side switch single switch	complex design

CHAPTER III

METHODOLOGY

3.1 Analysis of the Class E Topology

The analysis of the class E resonant converter is studied in this section and it can be represented with the basic schematic given in Figure 16. In this circuit, a PFC circuit provides DC voltage to the converter and the C_{pfc} is the output capacitor of the PFC circuit. The L_r and C_r are resonant components, C_1 is the parallel capacitance of the switch, L_f and C_f are the inductance and capacitance for filtering the input current and output voltage, respectively. According to the isolation requirements, the load can be connected to the tank circuit using a transformer Tr_1 as shown in the figure. I_{in} is the input, i_r is the current through the series resonant tank circuit and i_o is the output current.

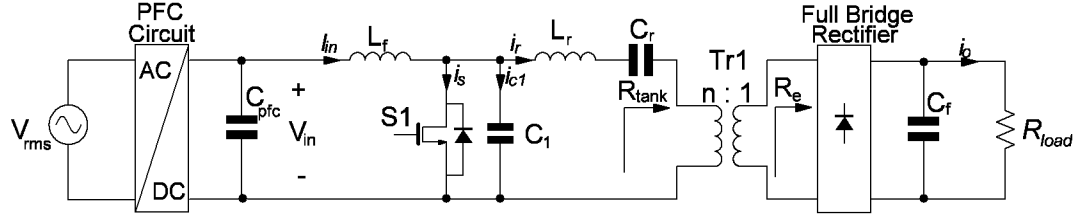


Figure 16: Schematic of the isolated class E resonant converter.

R_{tank} is the primary referred resistance of the transformer, R_e is the reflected resistance of the full-bridge rectifier, and R_{load} is the nominal output resistance of the converter (as shown in Figure 17). On the other hand R_e can also be described as the resistance which is seen from the secondary side of the transformer. This relationship of the resistances (R_{tank} , R_e , and R_{load}) will be given below.

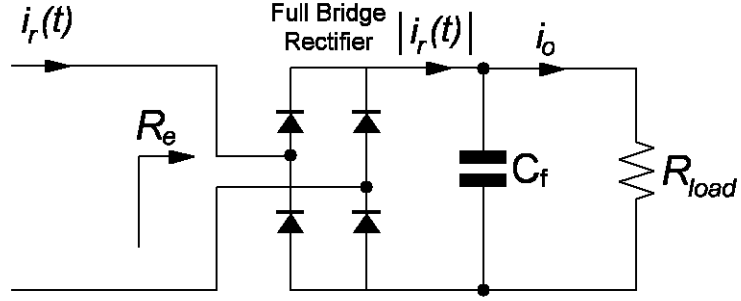


Figure 17: Rectifier and filter network of a resonant converter.

First, the equivalent circuit for the rectifier and filter network is calculated by using Fourier series [9] and this circuit can be depicted in Figure 18. In this figure, $|i_r(t)|$ is the rectified tank output current and its dc component must be equal to the steady-state load current I_o . Moreover, R_{load} , R_e , and I_o can be calculated by using equation (42), (43), and (44), respectively.

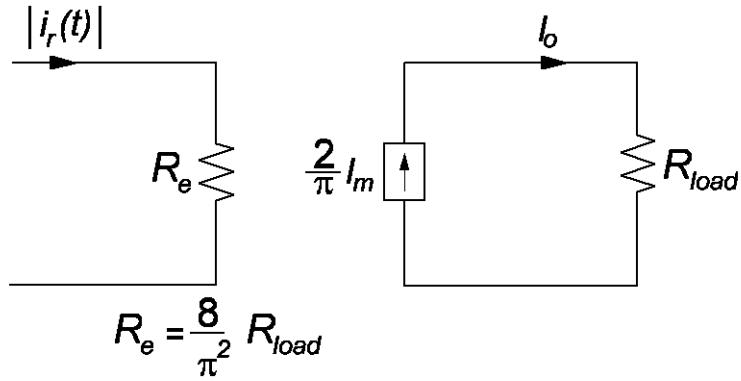


Figure 18: Equivalent circuit for the rectifier and filter network.

$$R_{load} = \frac{V_{out}^2}{P_{R_{load}}} \quad (42)$$

$$R_e = \frac{8}{\pi^2} R_{load} \quad (43)$$

$$I_o = \frac{2}{\pi} I_m \quad (44)$$

where I_m is the peak value of the resonant tank current which will be described later.

Second, the R_{tank} which can be seen in Figure 19 and it can be calculated [30] by DC input voltage V_{in} and input power of the transformer primary-side $P_{R_{tank}}$ (assuming lossless circuit) as follow (45) [35, 36]:

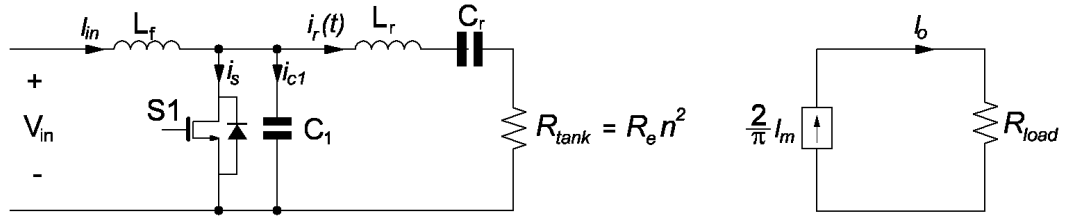


Figure 19: Equivalent circuit of Class E converter.

$$P_{R_{tank}} = \frac{8}{\pi^2 + 4} \frac{V_{in}^2}{R_{tank}} \quad (45)$$

where the $P_{R_{tank}}$ is equal to $P_{R_{in}}$ and $P_{R_{load}}$ according to the lossless assume.

On the other hand, the relationship between the resistances of R_{tank} and R_e is given in (46).

$$R_{tank} = R_e n^2 \quad (46)$$

From this equation, it can be seen that when $R_{tank}=R_e$, n must be "1" and there is no requirement for using transformer if isolation is not desired. However, in most application R_{tank} is not equal to R_e . Hence, the transformer is required for impedance matching and it also provides isolation advantage. After that, the detailed analysis of the class E converter will be described.

In the analysis, it is assumed that input power equals the output power and losses are neglected [30]. Additionally, the quality factor (Q_L) is defined as the ratio of energy stored in the circuit to the energy loss per cycle at the resonant frequency. For series resonant circuit, the quality factor is defined as $Q_L = \omega_s L_r / R_{tank}$, and chosen high enough to obtain a sinusoidal tank current (i_r) which can be expressed as follows:

$$i_r = I_m \sin(\omega_s t + \phi) \quad (47)$$

In this equation, i_r is assumed to be in the sinusoidal form for the analysis. ω_s is the switching frequency in rad/sec. ϕ is the initial phase of the current. According to the Figure 16, the input current I_{in} can be given as:

$$I_{in} = i_s + i_{C_1} + i_r \quad (48)$$

where i_s and i_{C_1} are the currents through the switch S1 and the capacitor C_1 , respectively. By using (47) and (48);

$$i_s + i_{C_1} = I_{in} - I_m \sin(\omega_s t + \phi) \quad (49)$$

When the switch is on, the difference between the input current I_{in} and tank current flows through the S1. When the switch is turned off, the same current goes through the C_1 . Therefore the current of the switch and the capacitor can be expressed, respectively, as follows;

$$i_s = \begin{cases} I_{in} - I_m \sin(\omega_s t + \phi), & \text{for } 0 < \omega_s t \leq 2\pi D \\ 0, & \text{for } 2\pi D < \omega_s t \leq 2\pi \end{cases} \quad (50)$$

$$i_{C_1} = \begin{cases} 0, & \text{for } 0 < \omega_s t \leq 2\pi D \\ I_{in} - I_m \sin(\omega_s t + \phi), & \text{for } 2\pi D < \omega_s t \leq 2\pi \end{cases} \quad (51)$$

It can be interpreted from (50) and (51) that the switch S1 is turned on between 0 and $2\pi D$. v_s is the switch voltage and it can be calculated by using the current of C_1 as follows [30]:

$$v_s = \frac{1}{(\omega_s C_1)} \int_{2\pi D}^{\omega_s t} i_{C_1} d(\omega_s t) \quad (52)$$

From (51) and (52), v_s can be expressed as:

$$v_s = \begin{cases} 0, & \text{for } 0 < \omega_s t \leq 2\pi D \\ \frac{1}{\omega_s C_1} \int_{2\pi D}^{\omega_s t} [I_{in} - I_m \sin \omega_s t + \phi] d(\omega_s t), & \text{for } 2\pi D < \omega_s t \leq 2\pi \end{cases} \quad (53)$$

In order to obtain ZVS; the switch voltage at $\omega_s t = 2\pi$ must be zero ($V_s(2\pi) = 0$) and by substituting this condition in (53), I_m can be expressed as:

$$I_m = I_{in} \frac{2\pi(1-D)}{\cos(2\pi D + \phi) - \cos(\phi)} \quad (54)$$

By using (53), (54) and the condition $dv_s/d(\omega t) = 0$ at $\omega t = 2\pi$, the relationship between duty cycle D and phase ϕ can be obtained as follows:

$$\tan(\phi) = \frac{\cos 2\pi D - 1}{2\pi(1-D) + \sin 2\pi D} \quad (55)$$

Using the trigonometric equality ($\tan(\phi) = x, \arctan x = \phi$) in (55), the initial phase of the current ϕ can be expressed as a function of the D as in the equation (56) and the relationship between D and ϕ is shown in Figure 20.

$$\phi = \pi + \tan^{-1} \left(\frac{\cos 2\pi D - 1}{2\pi(1 - D) + \sin 2\pi D} \right) \quad (56)$$

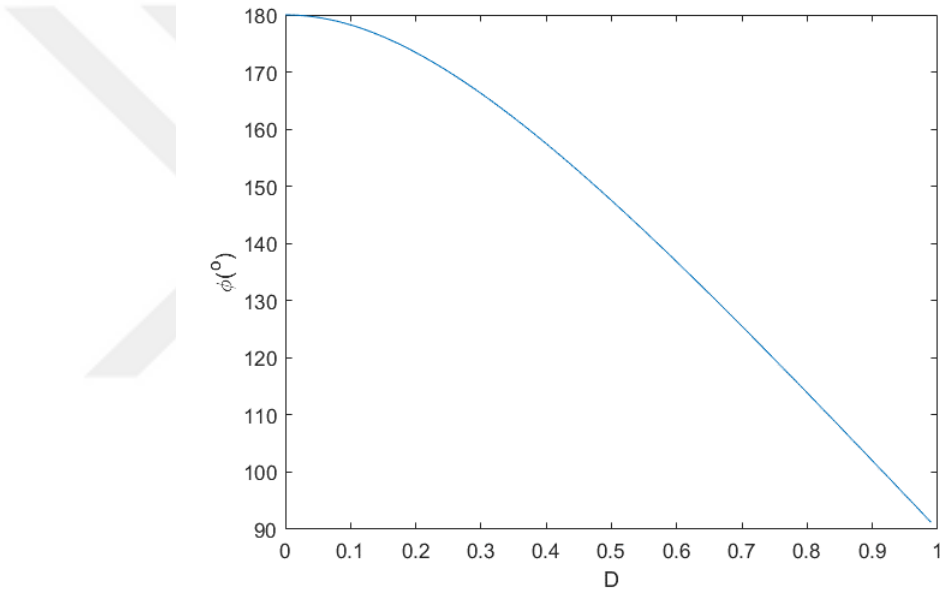


Figure 20: ϕ according to D .

The ratio of the peak voltage of the switch, which can be calculated by using (53) and (56), to the input voltage, i.e. V_{sm}/V_{in} ; and the ratio of the peak current of the switch, which can be calculated by (50) and (56), to the input current, i.e. I_{sm}/I_{in} are given in accordance with D in Figure 21. It can be seen from this figure that, when the duty ratio increases, the voltage stress of the switch increases but current stress decreases. Therefore, to get the maximum benefit from the switch, the switch utilization factor c_p can be calculated as (57) [30],

$$c_p = \frac{P_{R_{load}}}{I_{sm} V_{sm}} = \frac{I_{in} V_{in}}{I_{sm} V_{sm}} \quad (57)$$

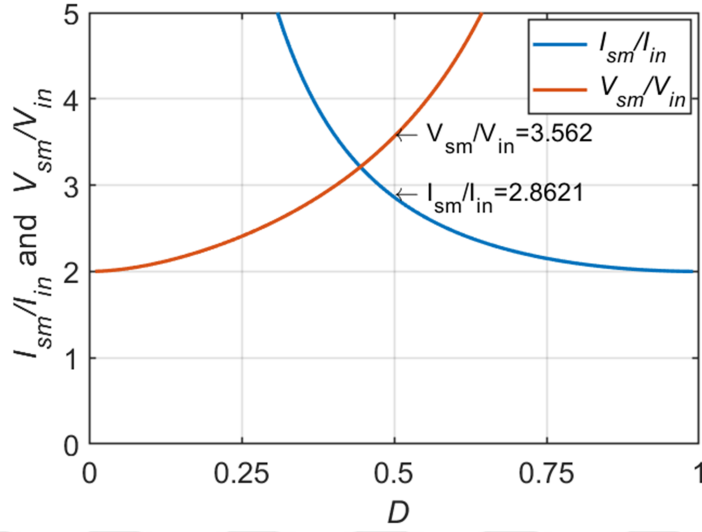


Figure 21: Maximum switch voltage and current versus D .

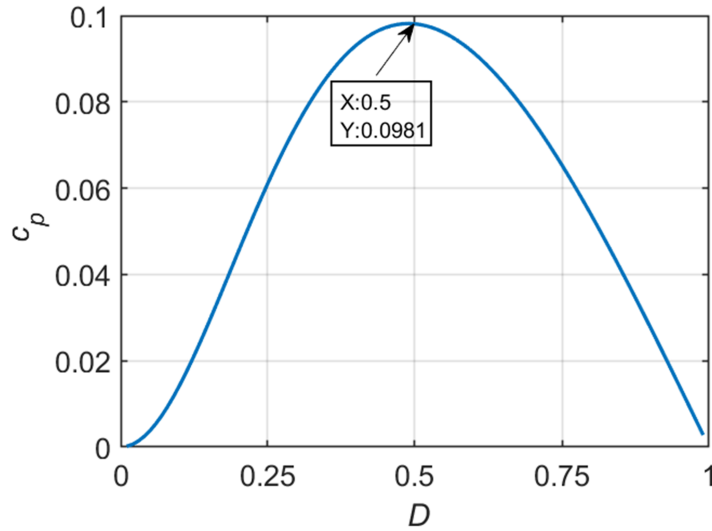


Figure 22: The switch utilization factor according to D .

Figure 22 shows the c_p with respect to D . It can be seen that the maximum switch utilization occurs at $D = 0.5$. Hence, $D = 0.5$ is used constant in this study. On the

other hand, when $D = 0.5$, the component values can be calculated from (58)-(62) [30].

$$L_r = \frac{Q_L R_{tank}}{\omega_s} \quad (58)$$

$$C_r = \frac{1}{\omega_s R_{tank} \left[Q_L - \frac{\pi(\pi^2 - 4)}{16} \right]} \quad (59)$$

$$C_1 = \frac{8}{\pi(\pi^2 + 4)\omega_s R_{tank}} \quad (60)$$

$$L_f = 2 \left(\frac{\pi^2}{4} + 1 \right) \frac{R_{tank}}{f_s} \quad (61)$$

$$C_f = \frac{I_{out} \Delta t}{\Delta V_{out}} \quad (62)$$

where Δt is the time duration (D/f_s) that the capacitor supplies energy to the output, which can be taken as $1/f_s$, and the ΔV_{out} is the desired peak to peak ripple of the output voltage.

3.2 Design of the Class E Converter

The design specifications are given in Table 2. It is assumed that a suitable PFC circuit provides 48 V constant voltage for the input of class E converter. The output voltage of class E is 24 V and the output power is 60 W.

It is seen from the Figure 21 that the duty ratio strongly affects the voltage and current stress of the switch. The switch voltage stress increases by the rise of duty ratio. On the other hand, if it is selected low, current stress will be high, hence, conduction losses increase. However, according to the Figure 22, the best compromise can be found as $D = 0.5$ which makes the switch utilization ratio maximum. When

Table 2: Design specifications

Parameters	Values
V_{in}	$48 V_{dc}$
V_{out}	$24 V_{dc}$
P_{out}	60 W
I_{out}	2.5 A
f_s	1.2 MHz
Q_L	7

$D = 0.5$, the V_{sm}/V_{in} ratio is found from the Figure 21 as 3.56 [14]. Since the V_{in} is $48 V_{dc}$, S1 must withstand to $48 V * 3.56 = 171 V$ peak. Moreover, I_{sm}/I_{in} ratio becomes 2.86, and therefore the peak current of the S1 must be higher than $1.25 A * 2.86 = 3.57 A$ peak. The CREE C2M0160120D SiC MOSFET whose breakdown voltage is $1200 V_{dc}$, the maximum drain current is 19 A, fulfills these requirements and can be selected for the prototype. The SiC MOSFETs have very low $R_{DS(on)}$ resistance and input capacitance with respects to the Si MOSFETs that makes the converter efficiency is high. The C1 must also withstand $171 V_{dc}$, it can be selected ceramic type capacitor instead of electrolytic capacitor. Its value can be calculated as 1.09 nF by using (60). However, the output capacitance of the selected MOSFET is 47 pF [37]. Hence, the $C1 = 1$ nF external capacitance can be connected to the S1 in parallel for fulfilling the soft-switching condition.

In order to obtain purely sinusoidal resonant tank current, Q_L should be in the range of $5 \cdots 10$ [30],[38]. In this design Q_L is selected as 7 and therefore, the resonant tank circuit components, L_r is calculated as $20.56 \mu\text{H}$ by using (58). In order to obtain L_r in prototype design, MAGNETICS 0055551A2 core can be used and the number of turns (N) can be calculated by the following equation.

$$N = \sqrt{\frac{L_r}{A_L}} \quad (63)$$

where A_L is the inductance per square turn and it is $14 \text{ nH} \pm 8\%$ for 0055551A2 core. From this equation, N can be calculated as 38 turns. However, L_r is selected as $19.46 \mu\text{H}$ because the leakage inductance of the transformer added serially to the L_r , so N is used as 36 turns in experimental studies.

On the other hand, maximum flux density also known as saturation flux density B_{max} can be calculated from (64) and it is found as 0.019 T for this inductance. In the equation, l is the length of the core which can be taken from datasheet of 0055551A2 core as 81.4 mm. μ_r is the relative permeability which is specified as 14 for this core and μ_0 is the permeability of free space (also known as the magnetic constant) and its value is $4\pi \times 10^{-7} \text{ H/m}$.

$$B_{max} = \frac{NI_m\mu_0\mu_r}{l} \quad (64)$$

Additionally, C_r is calculated as 1.024 nF by using (59). Instead of this capacitance, 1 nF ceramic capacitor can be used in experimental studies.

On the other hand, the voltage stresses of tank capacitor (C_r) and inductor (L_r) are high (nearly Q times of V_{in}) when compared to the input voltage. In order to reach high withstand voltage and because of the low value of the capacitor, the use of a ceramic capacitor is suitable. Additionally, this type of capacitors offers low Equivalent Series Resistance (ESR) and low size advantages.

L_f is calculated as 0.128 mH from (61) for ensuring 10% peak to peak current ripple [30]. However, the bigger inductance value can be used for obtaining smaller ripple and it is used as $300 \mu\text{H}$ in experimental studies. The $300 \mu\text{H}$ is designed by using E32 ferrite core, the air gap length l_g is calculated by using (65) as 0.15 mm and required number of turns is found by using (66) as 21 turns.

$$l_g = \frac{L_f I_{in}^2 \mu_0}{B_{max}^2 A_e} \quad (65)$$

In this equation, B_{max} is taken as 0.35 T in order to prevent saturation, A_e is the effective cross-sectional area of core which is given in the datasheet as 83 mm^2 for E32 ferrite core. Additionally, I_{in} can be taken as 2 A by considering inrush and ripple currents.

$$N = \sqrt{\frac{L_f I_g}{\mu_0 A_e}} \quad (66)$$

In order to obtain input-output isolation and the impedance matching between the load and resonant tank circuit (for obtaining $24 \text{ V}_{dc} / 60 \text{ W}$ at the output) [39], [40], [41] a transformer can be added by connecting before the rectifier diodes. The number of turn ratio of the transformer can be calculated by using (46) (it is calculated as 1.687). For transformer, the E25/N97 core can be used and its magnetizing inductance L_m should be minimum 10 times bigger than L_r for does not affect the resonant current. Hence, primary (from equation (46)) and secondary turns are used as 17 for primary winding, 10 for secondary winding. As a result of this, L_m is obtained as $552,9 \mu\text{H}$ (it can be seen in equation (63), where A_L is $1950 +30/-20\%$ for E25/N97 core). Additionally, the transformer leakage inductance is measured as $1.1 \mu\text{H}$ which will be added serially to the L_r .

Planar type cores can be implemented instead of E32, 0055551A2 and E25 ferrite cores. Planar type cores have the advantage of volume and weight compared to E cores, thus providing high power density. In addition, it has the advantages of excellent thermal characteristics, high repeatability, design flexibility, and low leakage inductance [42], [43].

Finally, the value of C_f is calculated by using (62) for 10% voltage ripple as 434 nF, and it can be employed 500 nF ceramic type capacitor for experimental studies.

The aforementioned design is presented for 1.2 MHz switching frequency and it

can be also exploited for 0.5 MHz switching frequency (the component values is also given in Table 3, 4, respectively) which will be used in experimental studies (Section 3.4) for investigating the effect of switching frequency on the efficiency.

Table 3: Calculated and experimental values of components for 1.2 MHz

Parameters	Calculated Values	Experimental Values
C_1	1.09 nF	1 nF
L_r	20.56 μ H	19.95 μ H
C_r	1.024 nF	1 nF
L_f	0.128 mH	0.3 mH
C_f	434 nF	500 nF
n	1.687	1.7

Table 4: Calculated and experimental values of components for 0.5 MHz

Parameters	Calculated Values	Experimental Values
C_1	2.64 nF	2.2 nF
L_r	49.35 μ H	48.04 μ H
C_r	2.45 nF	2.5 nF
L_f	0.3 mH	0.3 mH
C_f	1042 nF	500 nF
n	1.687	1.7

3.3 Simulation Studies

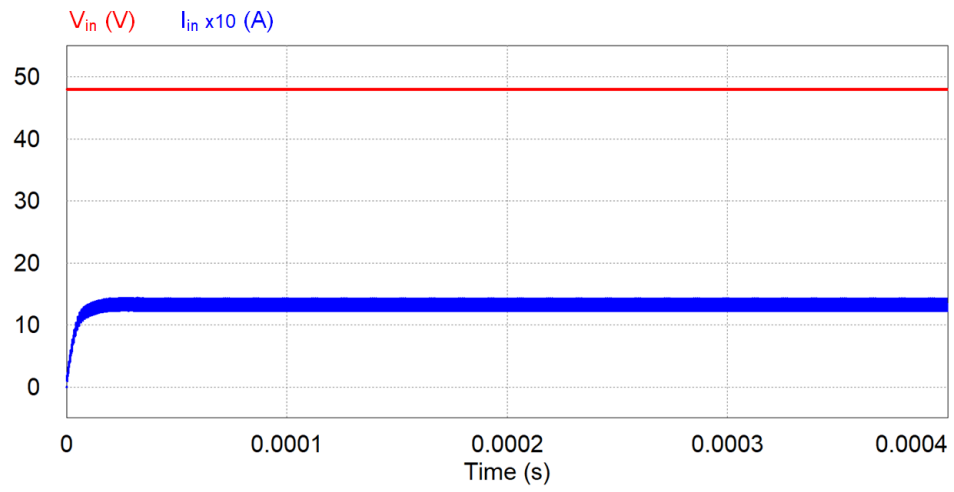
In order to verify the design, two different switching frequency: 1.2 MHz and 0.5 MHz were chosen and required component values (which are obtained from analysis) for these frequencies were given in Table 5. Additionally, PSIM schematics were presented in Figure 23-a and Figure 23-b for 1.2 MHz and 0.5 MHz, respectively.

other hand, the peak voltage of inductance and capacitance are 445 V and 360 V, respectively. These voltages are very high when compared to the input voltage, and it is the most important disadvantage of this converter. Additionally, RMS current values of these components are the same as 1.71 A.

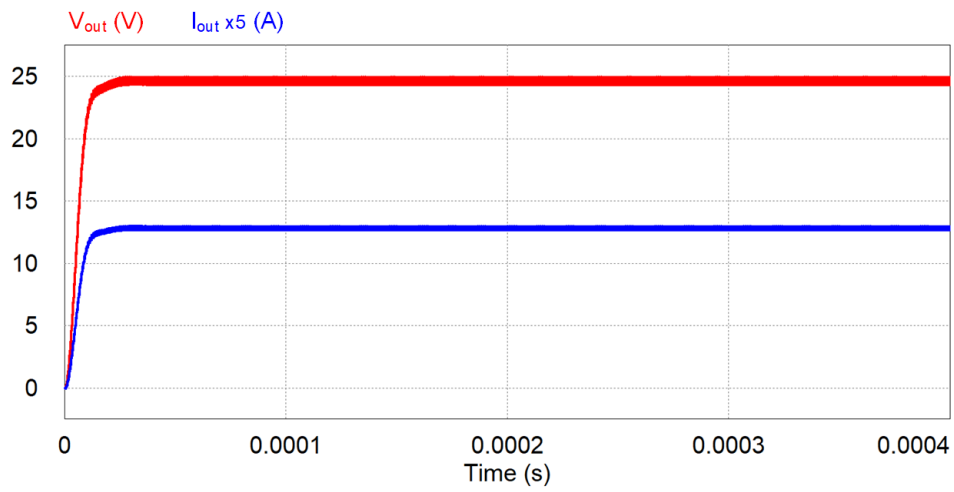
Table 6: Measurements from the circuit at 0.5 MHz and 1.2 MHz in simulation study

<i>Parameters</i>	<i>0.5 MHz</i>	<i>1.2 MHz</i>
$V_{in}(V)$	48	48
$I_{in}(A)$	1.35	1.33
$V_{out}(V)$	24.99	24.64
$I_{out}(A)$	2.60	2.56

In order to prove ZVS operation, the voltage and current waveform of S1 for the nominal power is given in Figure 28 for 0.5 MHz and 1.2 MHz. From the figure, it can be interpreted that, the class E converter achieves soft switching at nominal output power, however, under 65% power it enters hard switching region undesirably (which can be seen in Figure 29 for 0.5 MHz and 1.2 MHz). In Figure 29, while the MOSFET is turned on, the drain-source current starts from a positive value instead of a negative value which results hard switching.

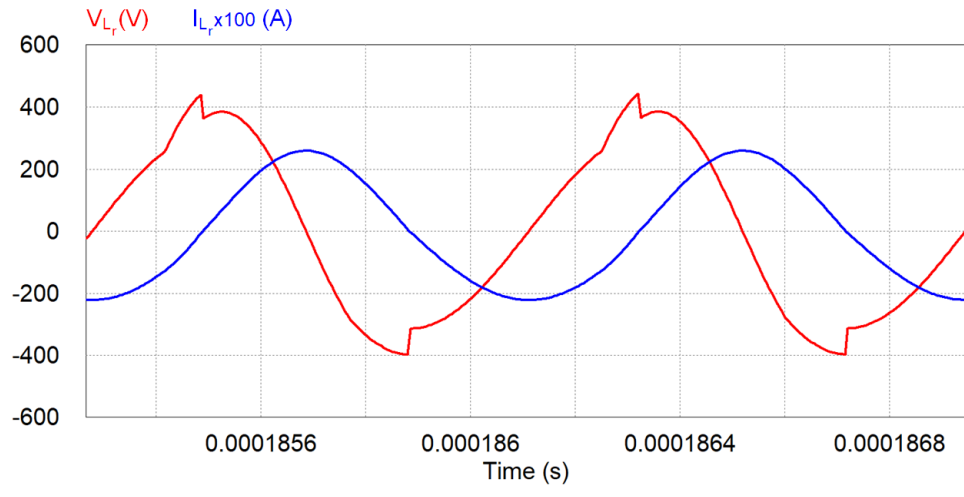


(a)

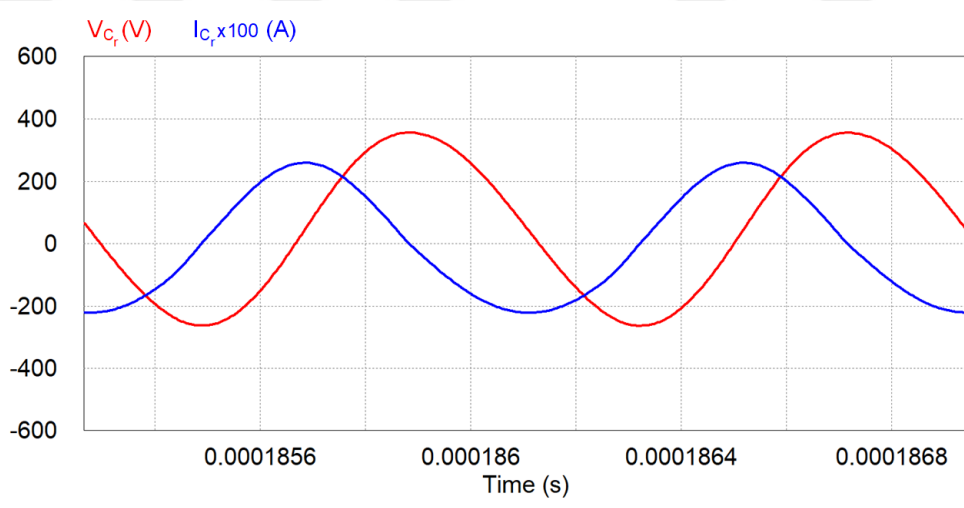


(b)

Figure 24: The voltage and current at 1.2 MHz a) input, b) output.

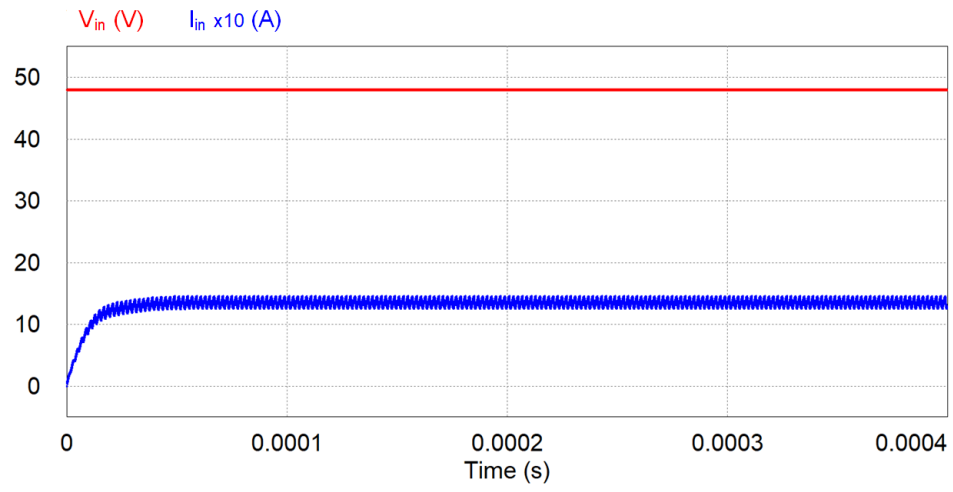


(a)

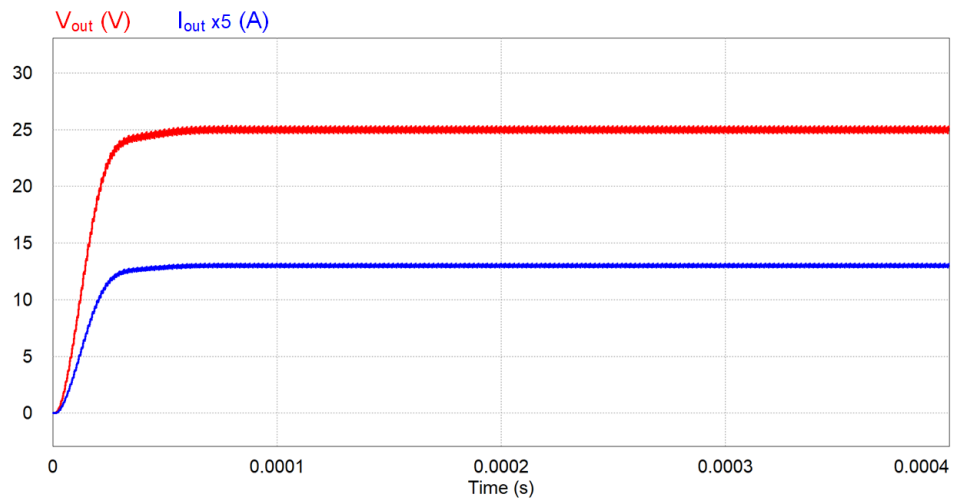


(b)

Figure 25: The voltage and current at 1.2 MHz on resonant a) inductance, b) capacitance.

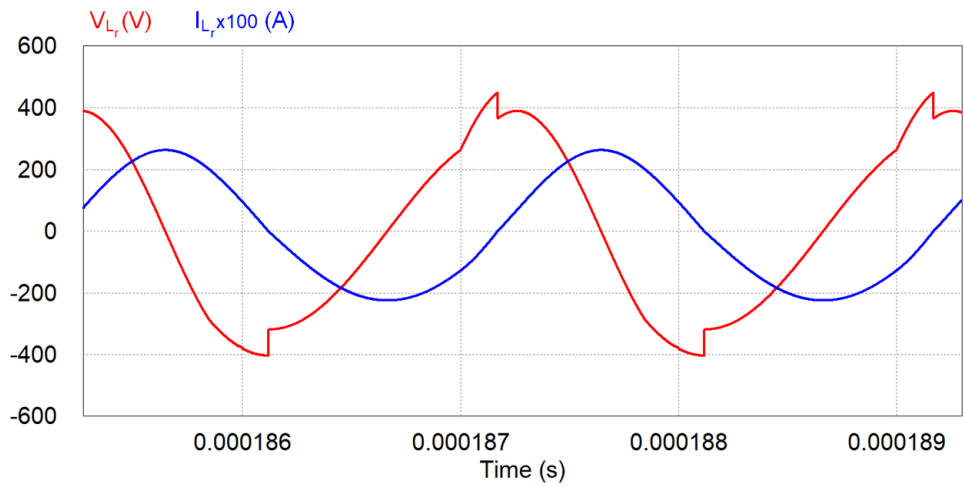


(a)

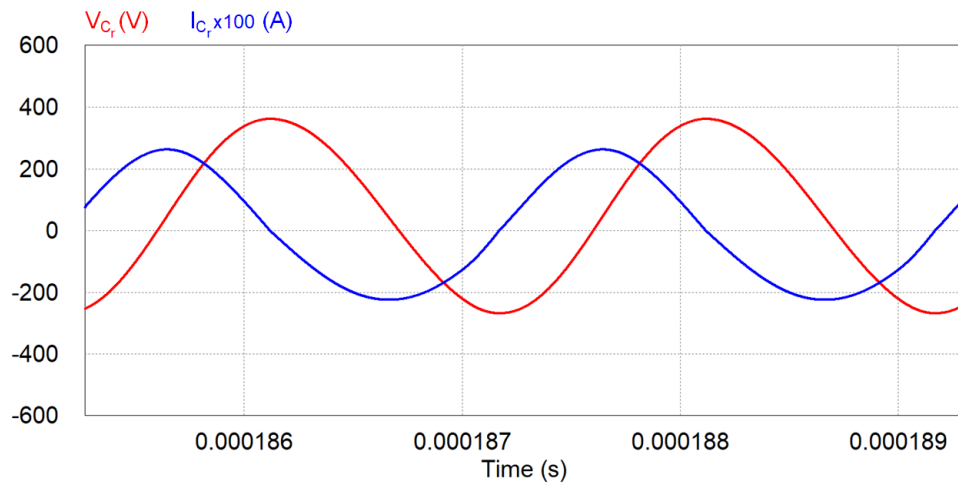


(b)

Figure 26: The voltage and current at 0.5 MHz a) input, b) output.

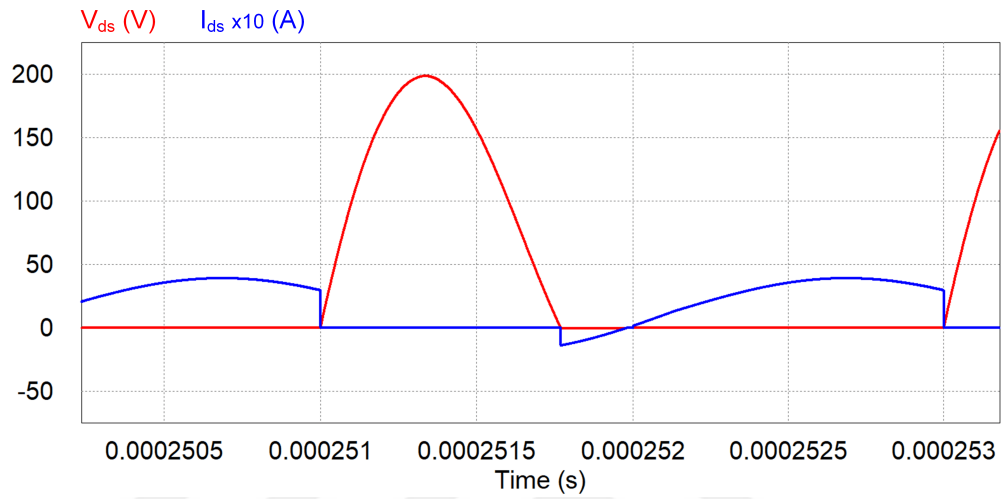


(a)

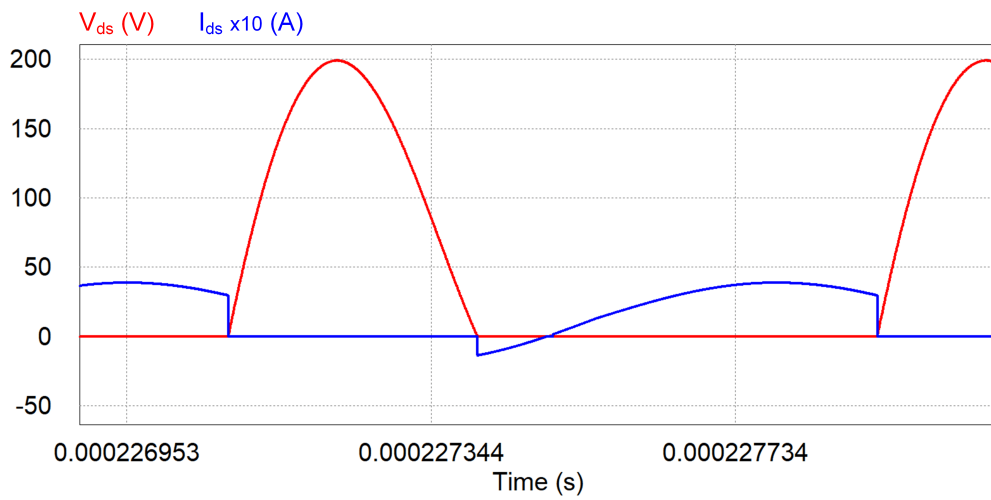


(b)

Figure 27: The voltage and current at 0.5 MHz on resonant a) inductance, b) capacitance.

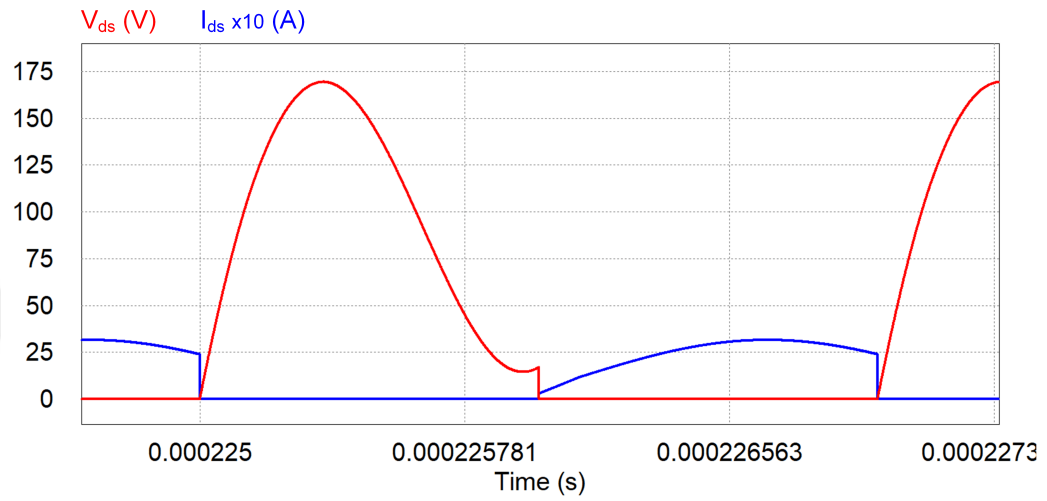


(a)

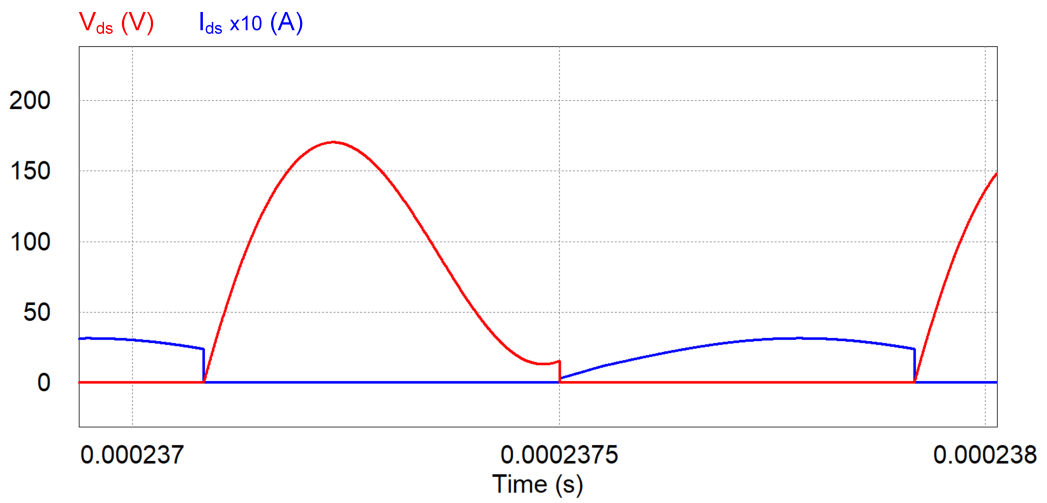


(b)

Figure 28: The drain-source voltage and current at nominal load for a) 0.5 MHz, b) 1.2 MHz.



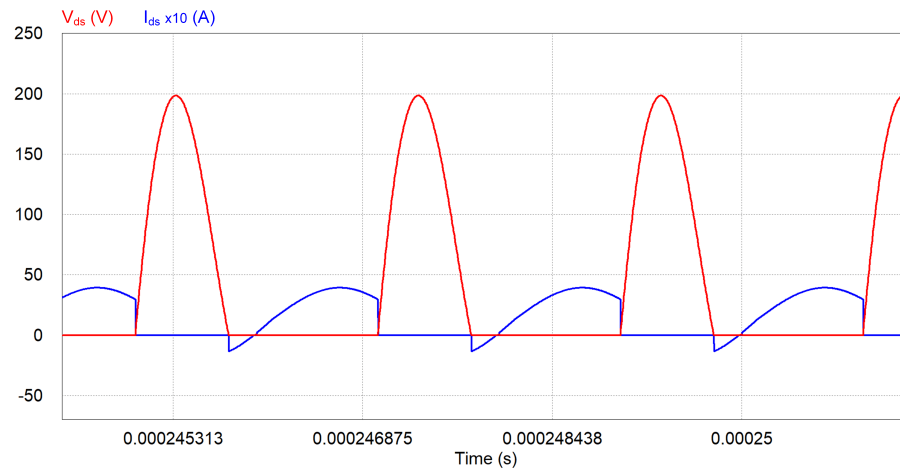
(a)



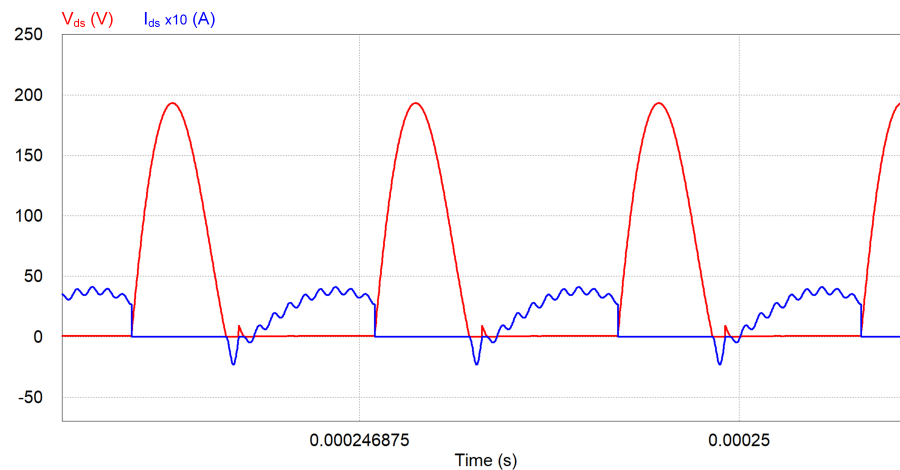
(b)

Figure 29: The drain-source voltage and current at 65% load for a) 0.5 MHz, b) 1.2 MHz.

In the simulations, when a series inductance is connected to the switch to model for the non-ideal situation, the drain-source current starts oscillating which can be seen 30 and 31 for 0.5 MHz and 1.2 MHz, respectively. This situation, may as well be observed in experimental studies due to the internal inductance of switch and inductance of measurement cables which has a significant effect at high switching frequencies at MHz levels.

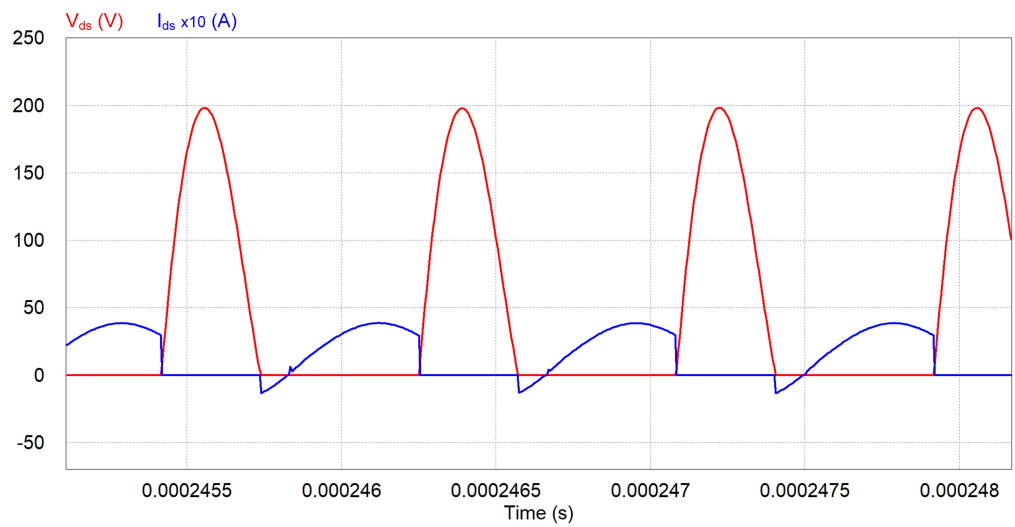


(a)

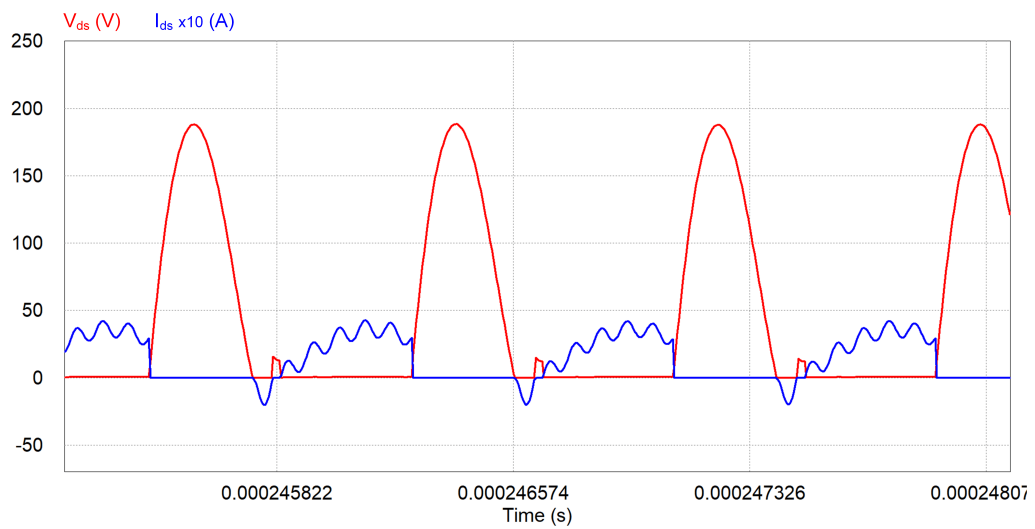


(b)

Figure 30: The drain-source voltage and current for 0.5 MHz with a) ideal components, b) non-ideal components.



(a)



(b)

Figure 31: The drain-source voltage and current for 1.2 MHz with a) ideal components, b) non-ideal components.

3.4 Experimental Results

In order to prove analysis and simulation studies two experimental setups were implemented for 1.2 MHz and 0.5 MHz switching frequencies. Component values for 1.2 MHz and 0.5 MHz switching frequencies are given in Table 3 and Table 4, respectively. The photographs of experimental environment are given in Figure 32, in experiments Tektronix MDO3014 Oscilloscope, Tektronix TCP0030A current probe, Keysight N2791A differential voltage probe, RIGOL DG1032 signal generator, GW INSTEK SPD-3606 DC power supply were used. On the other hand, a photograph also were taken from the circuits and they are shown in Figure 33. In these setups, a TC4420 was used as a MOSFET driver, the required PWMs were generated from a signal generator.

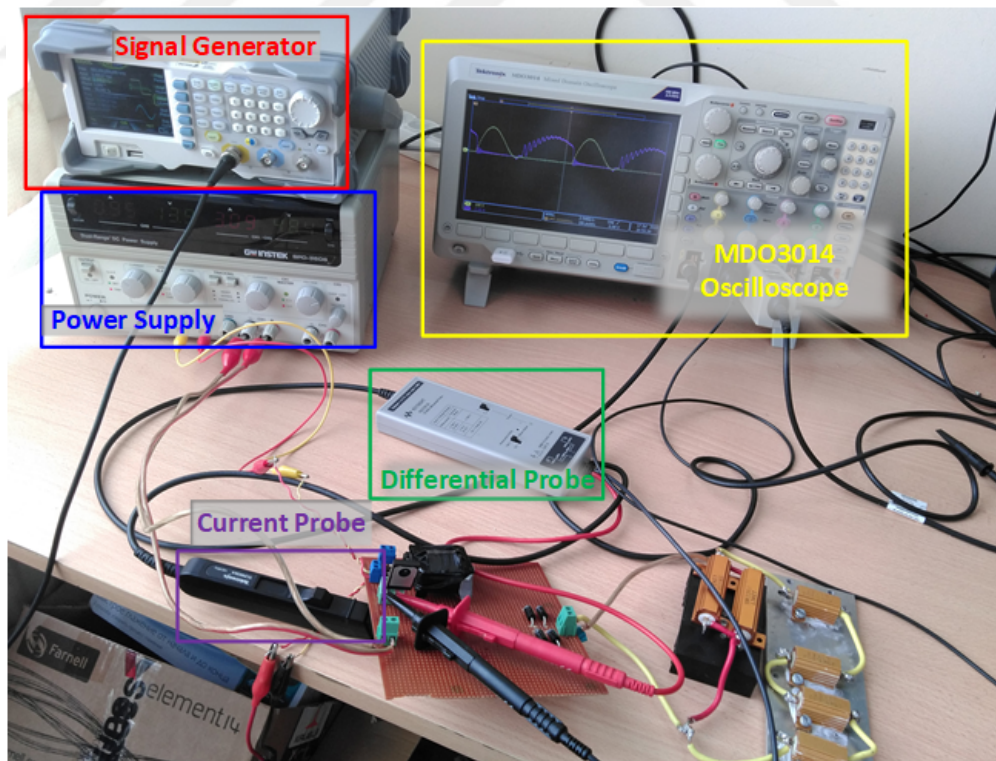
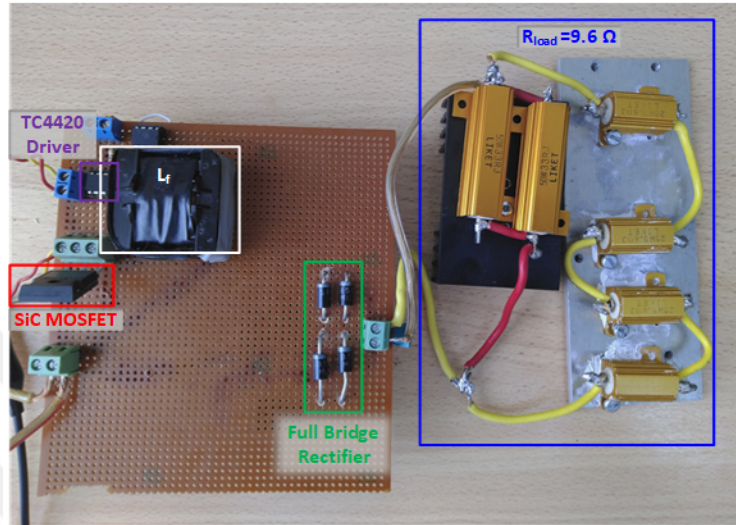
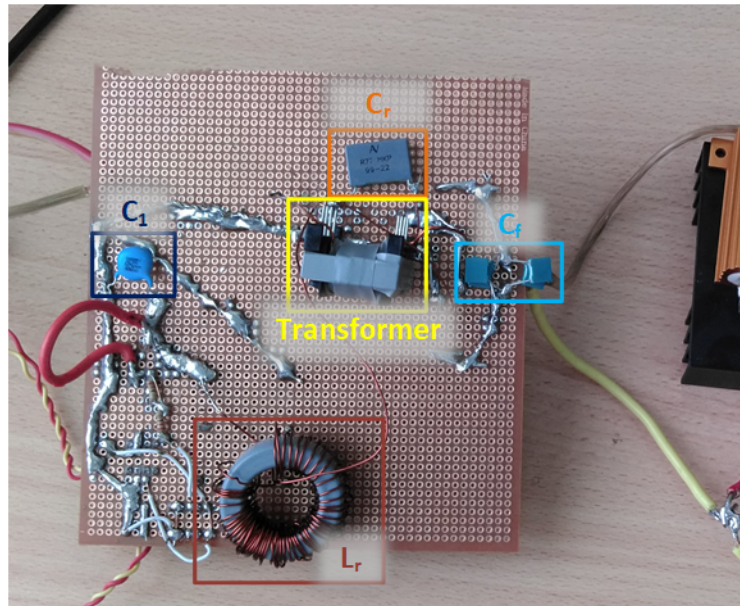


Figure 32: The experimental environment.



(a)



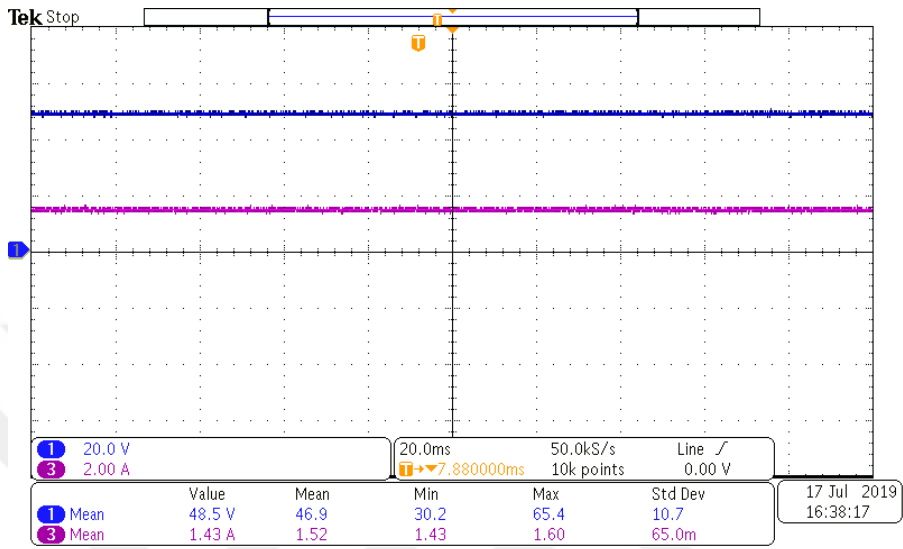
(b)

Figure 33: Experimental setup (front and back photographs).

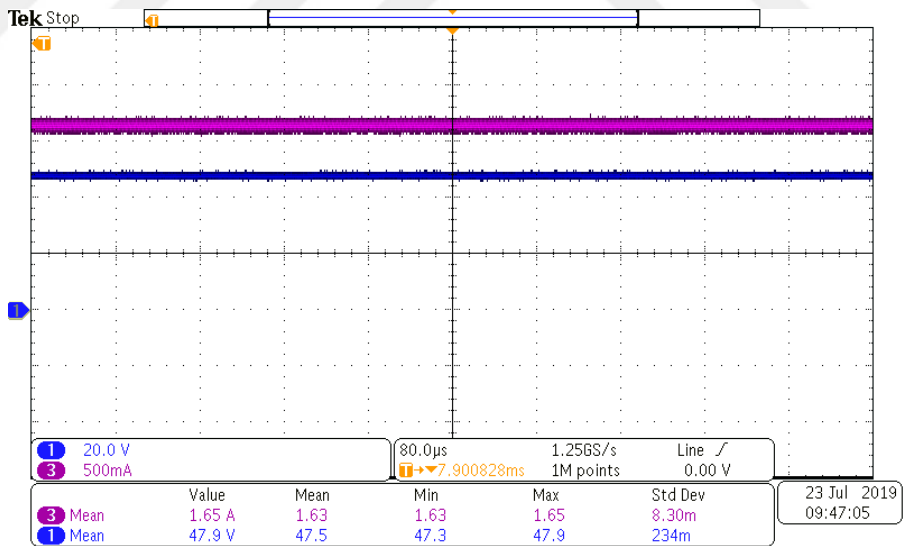
First of all, the average voltage-current of input and output are measured for both 0.5 MHz and 1.2 MHz experimental circuits, which are given in Figure 34 and Figure 35, respectively. These measurements are given in Table 7. From this table, it can be seen that 86.84% efficiency was obtained at 0.5 MHz switching frequency. However, the efficiency decreases at higher switching frequencies such as 1.2 MHz (79.86% efficiency) which is caused especially from core losses. With the increase in frequency, the core loss of the currently used ferromagnetic materials begins to increase [44] and this causes a decrease in efficiency [45]. On the other hand, increasing the switching frequency up to 20 MHz can reduce the core size hence it can allow the use of air cores [18]. Furthermore, from the outputs, it can be seen that the output voltage ripple decreases significantly by increasing the switching frequency from 0.5 MHz to 1.2 MHz.

Table 7: Measurements from the circuit for 1.2 MHz and 0.5 MHz switching frequency in experimental study

Parameters	1.2 MHz	0.5 MHz
V_{in} (V)	47.9	48.5
I_{in} (A)	1.65	1.43
V_{out} (V)	24.0	23.9
I_{out} (A)	2.63	2.52
η (%)	79.86	86.84

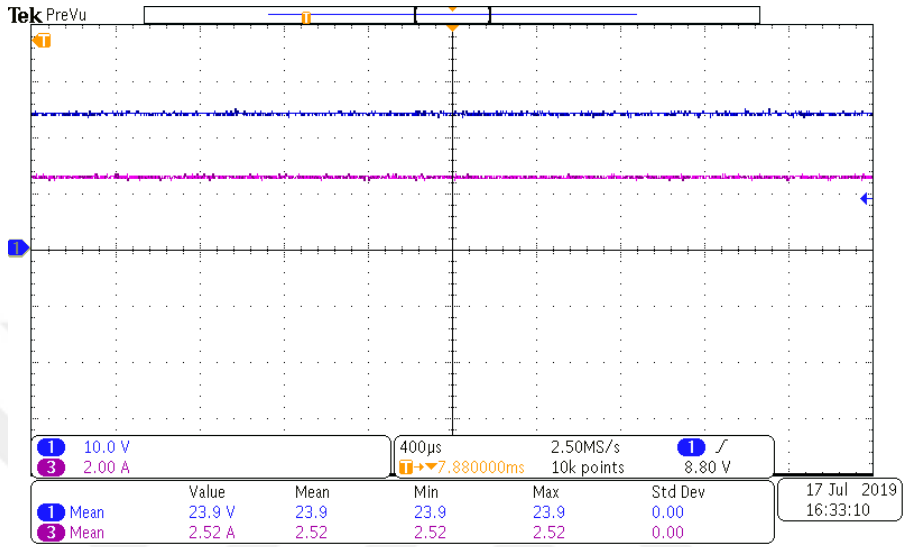


(a)

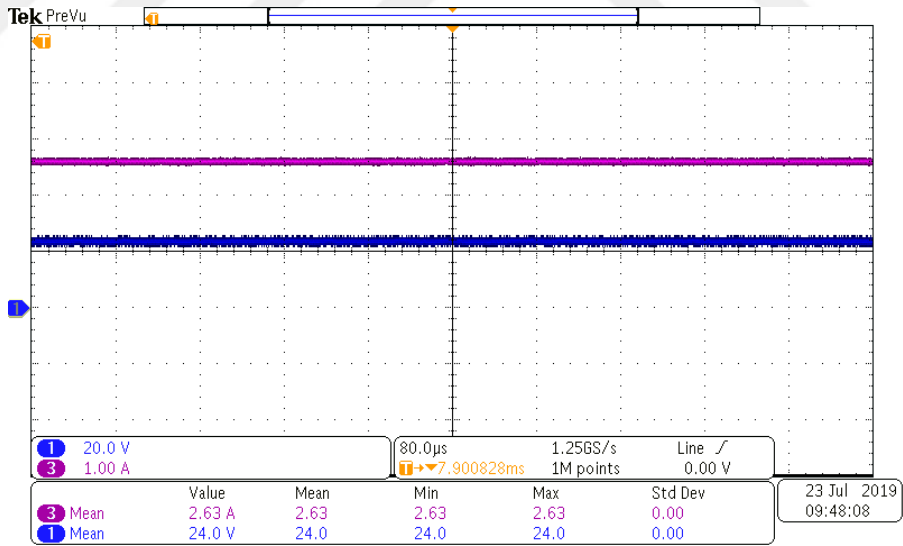


(b)

Figure 34: The input voltage and current for a) 0.5 MHz, b) 1.2 MHz switching frequency.



(a)

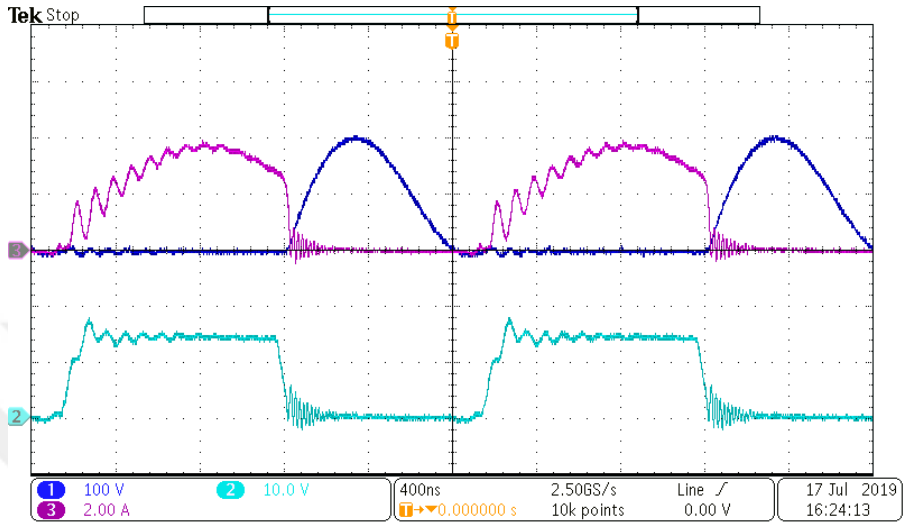


(b)

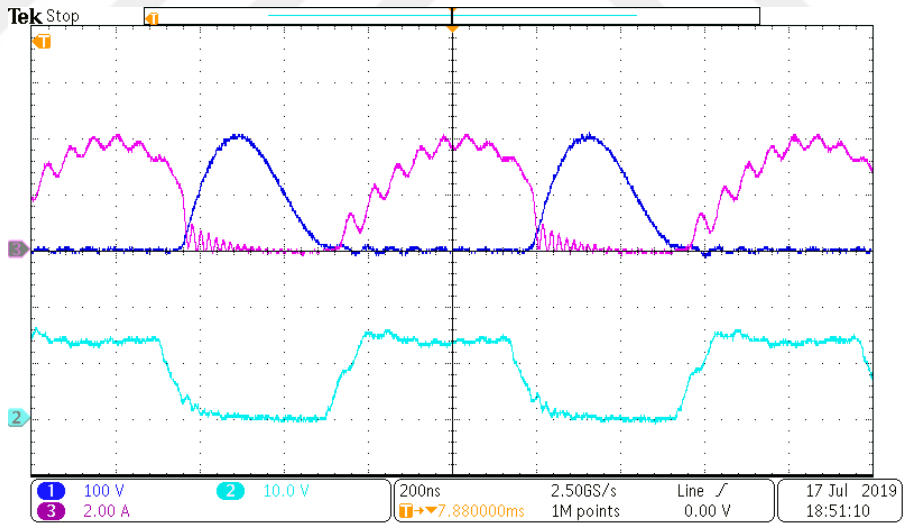
Figure 35: The output voltage and current for a) 0.5 MHz, b) 1.2 MHz switching frequency.

The gate-source voltage and drain-source voltage-current were measured for 0.5 MHz and 1.2 MHz switching frequency and they are given in Figure 36. In these measurements there are oscillations in current at high frequency ($\sim >16f_s$) which are caused from non-ideal characteristic of switch especially serial inductance (mentioned in Section 3.3, Figures 30 and 31). On the other hand, it can be interpreted from this figures that the converter achieves soft switching at turn on and turn off instants. In addition, it should be seen from the Figure 36 that the drain-source voltage of MOSFET is approximately 4 times the input voltage.

The voltage and current measurements of L_r and C_r were given in Figure 37 and Figure 38, respectively. These measurements show the same characteristics which were given in simulation Section 3.3.

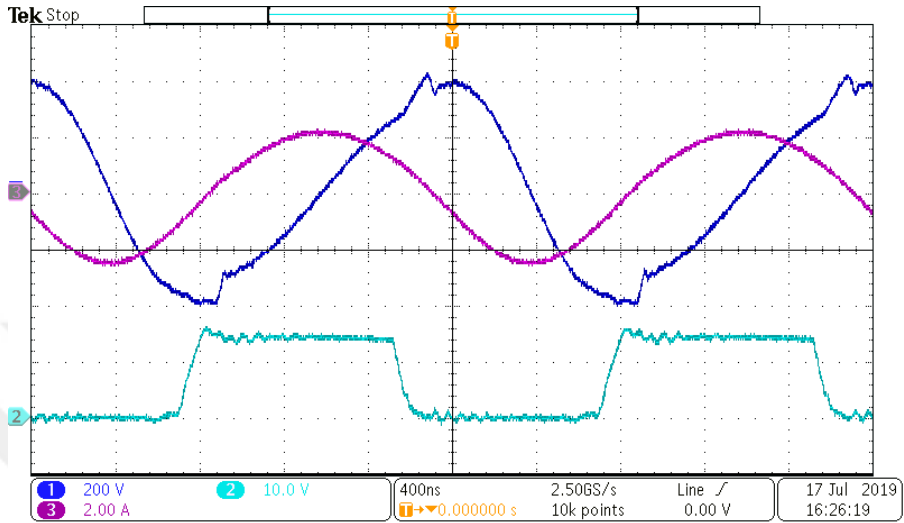


(a)

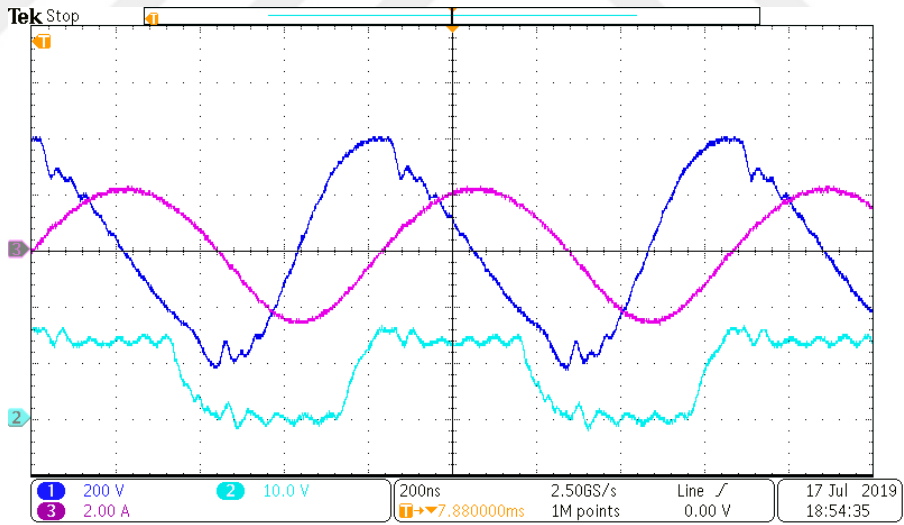


(b)

Figure 36: The drain-source voltage-current and gate voltage for a) 0.5 MHz, b) 1.2 MHz switching frequency.

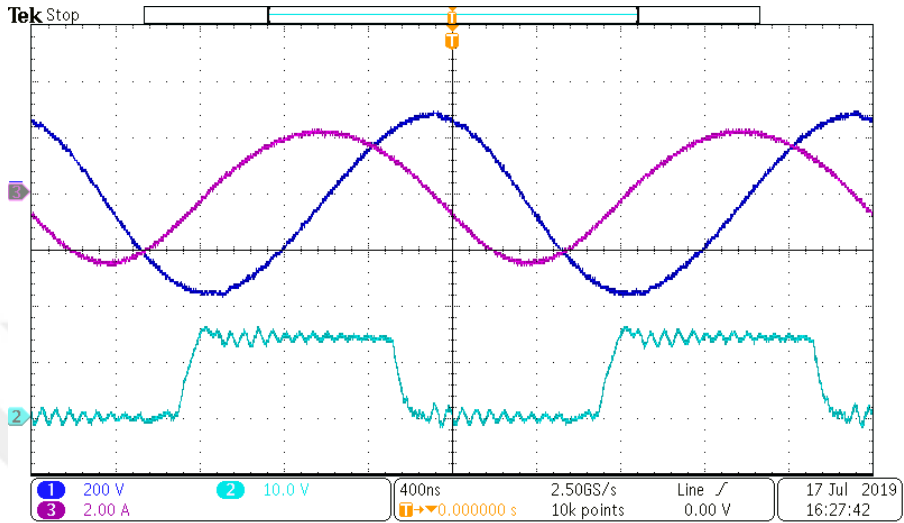


(a)

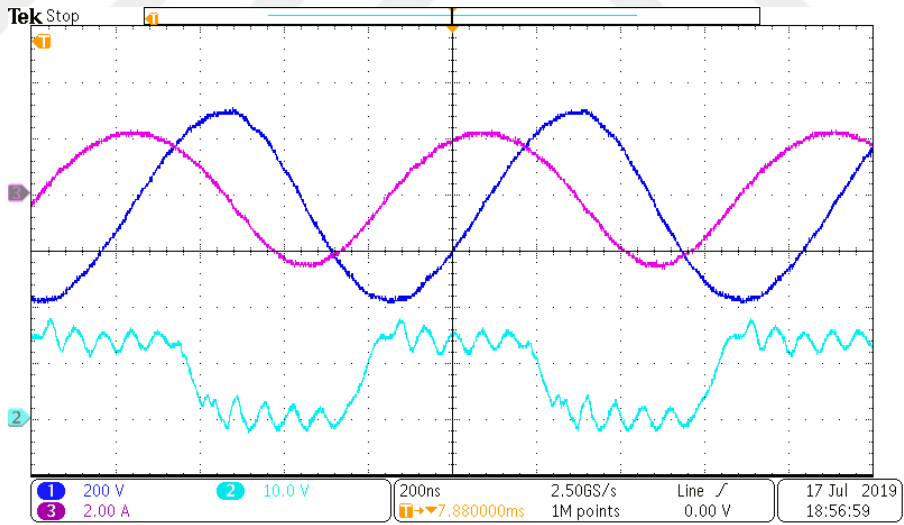


(b)

Figure 37: The voltage and current of L_r for a) 0.5 MHz, b) 1.2 MHz switching frequency.



(a)



(b)

Figure 38: The voltage and current of C_r for a) 0.5 MHz, b) 1.2 MHz switching frequency.

Additionally, in order to prove ZVS operation, an experiment perform under $\sim 60\%$ load ($R_{load}=16 \Omega$, instead of 9.6Ω) and the voltage and current waveform of switch for 0.5 MHz switching frequency which can be seen in Figure 39. According to the figure, it can be seen easily that the switch enters hard switching condition and the switching loss was increased.

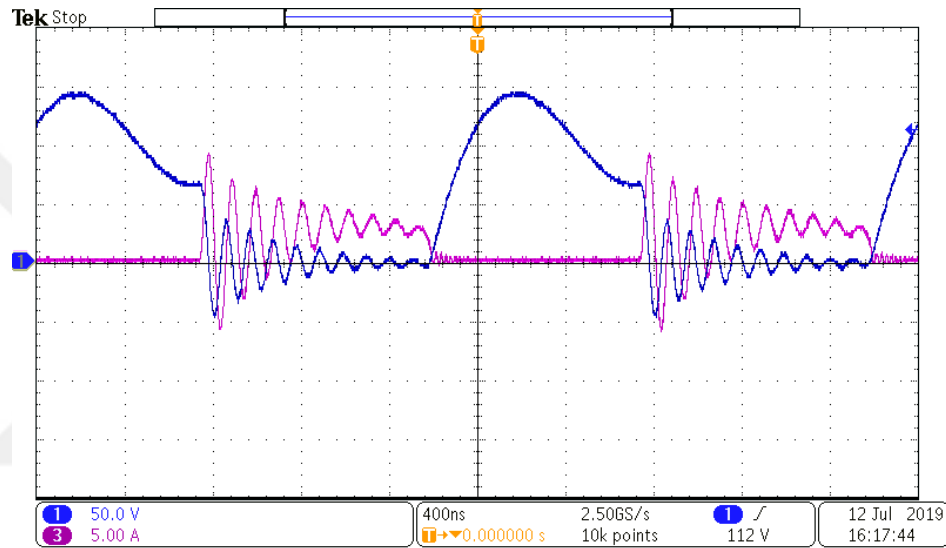


Figure 39: The drain-source voltage and current under 60% load for 0.5 MHz .

On the other hand, experimental studies were established by the help of the calculated parameters (give in Table 8) at switching frequencies of 0.1, 0.25 and 0.75 MHz and the results are summarized in Table 9. As can be seen from the results, the efficiency first increases with the frequency increase, but after a while, it starts to fall again. The most important reason for the increase in efficiency can be interpreted as the decrease in DC resistance (its changes are given in Table 10) of the resonant inductance. However, the increase in core losses is predicted the most important reason for the decrease in efficiency. Then, the efficiency curve according to the frequency is shown in Figure 40.

Table 8: Calculated circuit parameters for different switching frequencies

Switching Frequency (Hz)	L_f (mH)	C_1 (F)	L_r (μ H)	C_r (nF)	C_f (μ F)
0.1 M	1.5	13.2 μ	246.8	12.3	5.2
0.25 M	0.614	5.27 μ	98.7	4.9	2
0.5 M	0.3	2.64 n	49.35	2.45	1.042
0.75 M	0.2	1.76 n	32.9	1.64	0.694
1.2 M	0.128	1.09 n	20.56	1.024	0.434

Table 9: Measurements from the circuit at different switching frequencies

Switching Frequency (Hz)	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	η (%)
0.1 M	47.6	1.55	23.8	2.53	81.61
0.25 M	47.6	1.47	23.5	2.54	85.30
0.5 M	48.5	1.43	23.9	2.52	86.84
0.75 M	47.4	1.58	23.9	2.57	82.01
1.2 M	47.9	1.65	24.0	2.63	79.86

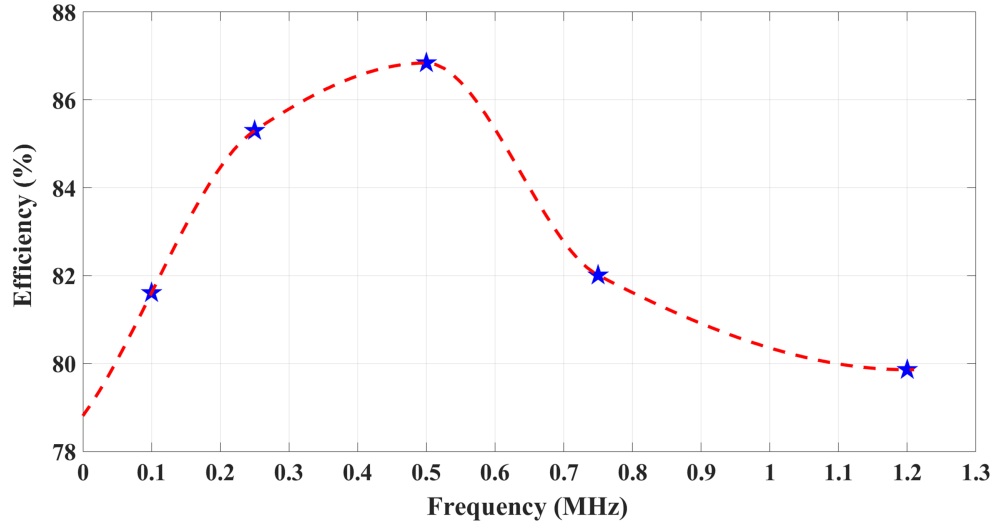


Figure 40: Efficiency curve with different switching frequencies.

Table 10: DC resistance of the resonant inductance at different switching frequencies

Switching Frequency	DC Resistance ($m\Omega$)
0.1 MHz	480
0.25 MHz	100
0.5 MHz	40
0.75 MHz	30
1.2 MHz	23.5

Furthermore, the Flyback converter which can supply 48V/60W output and operates at 1.2 MHz switching frequency, and the Class E converter which can operate under the same conditions are compared and their efficiency is given in Table 11. It can be seen that the Flyback converter is less efficient than Class E topology for MHz levels. The efficiency of the flyback converter is 44.53%, which are resulted from hard switching and loss of all leakage inductance energy. The MOSFET drain-source voltage and current waveforms of the flyback converter are shown in Figure 41. From this figure, it can be observed that Flyback performs hard-switching. In addition, Flyback input-output voltage and current waveforms can be seen in Figure 42.

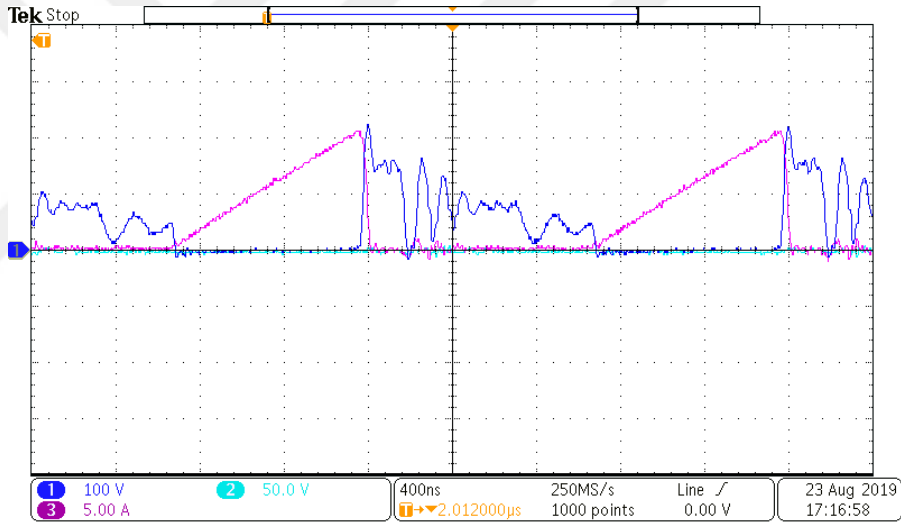
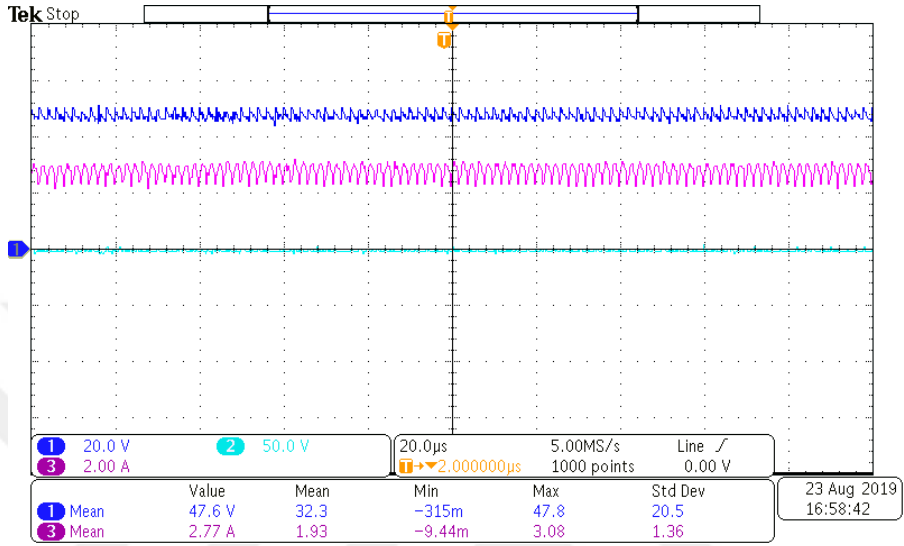


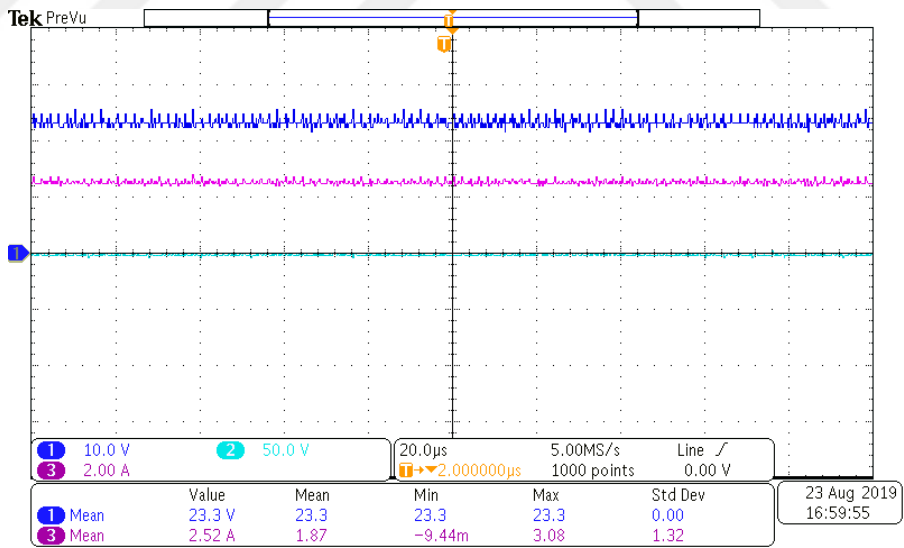
Figure 41: Mosfet drain-source voltage and current of Flyback Converter at 1.2 MHz.

Table 11: Efficiency Comparison Flyback and Class E for 1.2 MHz

	Class E	Flyback
V_{in} (V)	47.9	47.6
I_{in} (A)	1.65	2.77
V_{out} (V)	24.0	23.3
I_{out} (A)	2.63	2.52
η (%)	79.86	44.53



(a)



(b)

Figure 42: Flyback voltage and current a)input, b)output.

CHAPTER IV

RESULTS AND CONCLUSION

In this thesis, a class E resonant converter for DC/DC conversion is analyzed, simulated, implemented, and tested operating with 48 V DC input supply. In the analysis and simulation studies, 0.5 MHz and 1.2 MHz switching frequencies are selected and circuit parameters are calculated accordingly. In order to prove analysis and simulations, experimental circuits were implemented for both of 0.5 MHz and 1.2 MHz operation. From the experimental studies, 86.84% and 79.86% efficiencies were measured for 0.5 MHz and 1.2 MHz switching frequencies, respectively. It was observed that the conversion efficiency decreases by increasing the switching frequency due to core losses. On the other hand, it was experienced that the class E converter could accomplish soft switching. However, the circuit parameters strongly affect the soft switching region and also converter can enter the hard switching at light loads (such as 60% load). One of the disadvantages of this converter, the resonant tank capacitance and inductance are exposed to high voltage stress compared to the input voltage which restricts the use of this converter at high input voltages. On the other hand, decreasing the value of the inductance by high frequency allows for planar core design, and studies on the planar core are planned for the future studies.

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